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Design of a Class-D RF power amplifier in CMOS technology

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"Try not to become a man of sucess, but rather try to become a man of value"
Albert Einstein

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Abstract

In this thesis an RF Class-D Power Amplifier is presented. The analysis of the Class-D amplifier considering ideal components has shown that the drain efficiency of 100% can be achieved. The output power and the drain efficiency are degraded by the internal resistance of each component. A driver is used to drive the gate capacitances of the Class-D amplifier. Both driver and amplifier are implemented with CMOS inverters. The size of the inverters in the driver is scaled down by a factor of 3 relatively to the preceding stage. The first being the inverter of the Class-D amplifier. At the output a 3rd order Butterworth bandpass filter is implemented. A non-ideal analysis of the Class-D amplifier is performed to create a base model which is used to aid in the design of the circuit.

The RF Class-D Power Amplifier with the operation frequency of 2.4GHz was implemented with standard 130 nm CMOS technology. Two simulations were taken into account considering ideal and pre-layout components in the output filter. The following results were obtained when using ideal components: the output power of 6.91 dBm, the drain efficiency of 40% and the overall efficiency of 23%. Using pre-layout components the results were the following: the output power of 0.317 dBm the drain and overall efficiency of 8.6% and 4.9%, respectively.

Keywords: Class-D, RF power amplifier, CMOS, drain efficiency, radio-frequency, switching circuits.

RESUMO

Nesta tese um amplificador de potência Classe-D para aplicações de rádio frequência é apresentado. A análise do amplificador Classe-D considerando componentes ideais mostrou uma eficiência de dreno de 100% pode ser alcançada. A potência de saída e a eficiência de dreno podem ser degradadas pela resistência interna dos componentes. Um *driver* é usado para fornecer corrente necessária ao amplificador Classe-D. Tanto o *driver* como o amplificador são implementados com inversores em *CMOS*. O tamanho dos inversores do *driver* são escalados por um factor de 3 em relação ao inversor precedente. A factor de escalamento é feito a partir do inversor do amplificador. À saída do amplificador é implementado um filtro passa-banda *Butterworth* de 3 ordem. Uma análise não ideal do amplificador é realizada para cria um modelo base utilizado para o dimensionamento do circuito.

O amplificador Classe-D *RF* com uma frequência de operação de 2.4 GHz foi implementado em tecnologia *standard CMOS* de 130 nm. Duas simulações foram realizadas, uma considerando componentes ideais e a segunda considerando componentes de *pre-layout* no filtro de saída. Foram obtidos resultados na simulação considerando componentes ideais: potência de saída de 6.91 dBm eficiência de dreno de 40% e uma eficiência global de 23%. Usando componente de *pre-layout* os seguintes resultados foram obtidos: potência de saída de 0.317 dBm eficiência de dreno de 8.6% e uma eficiência global de 4.9%.

Palavras-chave: Classe-D, amplificador de potência RF, *CMOS*, eficiência de dreno, radio-frequência, circuitos comutados.

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GLOSSARY

$\sum\Delta$ Sigma-Delta.

BLE *Bluetooth* Low Energy.

CDVS Class-D Voltage-Switching.

CMOS Complementary Metal-Oxide-Semiconductor.

DC Direct Current.

DPSK Differential Phase-Shift Keying.

DQPSK Differential Quadrature Phase-Shift Keying.

GFSK Gaussian Frequency-Shift Keying.

IC Integrated Circuit.

IoT Internet of Things.

ISM Industrial Scientific Medical.

MIM Metal-Insulator-Metal.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

NMOS N-type metal-oxide-semiconductor.

PA Power Amplifier.

PAE Power Added Efficiency.

PMOS P-type metal-oxide-semiconductor.

PSK Phase Shift Keying.

RF Radio Frequency.

SoC System-on-Chip.

ZCS Zero Current Switching.

ZVS Zero Voltage Switching.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Nowadays communication is very important to society, leading to an exponential growth in the wireless market. As wireless connectivity arrives to the consumer's market the main goal of the Integrated Circuit (IC) manufacturers is to provide low cost solutions. The Power Amplifier (PA) is a key building block in all Radio Frequency (RF) transmitters. In order for the manufacturers to reduce the costs of communication devices and allow full integration (System-on-Chip (SoC)) it is desirable to integrate the entire transceiver and the PA in a single Complementary Metal-Oxide-Semiconductor (CMOS) chip. The CMOS technology enables such cost reduction while being able to operate at high frequencies.

An RF Class-D PA circuit was first proposed by Baxandall [1] in 1959, this amplifier topology has been widely used in various applications, and still remains one of the few amplifier topologies with an ideal Direct Current (DC) to RF conversion efficiency of 100%. Such an efficiency is obtained by operating the active devices as switches, this switching action generates a binary amplitude output signal that preserves the zero-crossing present on the input signal. Hence, one of the main limitations of the Class-D amplifier topology is the elimination of the signal envelope after amplification, which restrains the application of the amplifier to constant envelope signals.

The objective of this thesis is the design of an RF Class-D Voltage-Switching (CDVS) PA in standard 130 nm CMOS tecnhology, working at a frequency of 2.4 GHz which is suitable to be used in the Industrial Scientific Medical (ISM) band. Recently this band is being widely used for wireless communication for the Internet of Things (IoT).

1.2 Thesis Organization

The presented thesis is organized in five chapters including the introduction, the thesis organization is as follows:

Chapter 2 - RF Power Amplifiers Overview

In chapter 2 many classes of power amplifiers are presented. The classes are distributed between two groups and the distinction is made between them. Each class is briefly described. The main features of the RF amplifiers are described, which are the output power and the efficiency. Four transmitter topologies and *Bluetooth* modulation are discussed.

Chapter 3 - RF Class-D Power Amplifier With Sigma-Delta Modulation

In this chapter a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), working in the linear/triode region is presented along with the equations that characterize it. A CMOS inverter is also described, which has two transistors working as switches, P-type metal-oxide-semiconductor (PMOS) and a N-type metal-oxide-semiconductor (NMOS). The RF CDVS PA is analysed using and ideal an a non-ideal analysis. A power amplifier driver is also presented . A bandpass Butterworth filter is also described here with the design equations. Finally a 1-bit Sigma-Delta ($\sum\Delta$) modulator is discussed.

Chapter 4 - Design and Simulation of The Proposed RF Class-D Power Amplifier

In this chapter the RF CDVS PA is designed with an operation frequency of 2.4 GHz using 130 nm CMOS technology applying the analysis made in chapter 3. At last an ideal 1st order $\sum\Delta$ modulator is used to drive the RF CDVS PA.

Chapter 5 - Conclusion and Future Work

In this final chapter the obtained results are discussed and future research is suggested.

CHAPTER 2

RF POWER AMPLIFIERS OVERVIEW

In this thesis a RF Class-D PA is presented. In this chapter an overview is made between the major classes of RF amplifiers. The difference between two groups of RF amplifiers is described. Each group has different amplifiers' topologies that are classified into different classes. Each class is briefly described in order to provide an understanding of how they operate.

The main features of an RF amplifier are the output power and the efficiency, which are explained in this chapter. The RF PAs are used in the transmitters chain in wireless transmissions, they are responsible for the amplification of the desired signal before the transmission. Four transmitter topologies are discussed, two of them are mainly analog and other two are mainly digital.

During the transmission the wireless signals must be modulated. There are many different modulation techniques. This chapter describes the *Bluetooth* modulation as an example to be applied with the RF Class-D PA presented in this thesis. That is more suited to be used with the latest *Bluetooth* modulation technique, which is used in the IoT.

2.1 RF Power Amplifiers

There are many classes of power amplifiers, their classification depends on how the drive of the transistor is done and the drain voltage time behaviour and harmonic content [p. 30][2]. The need to classify power amplifiers into classes comes from the beginning of the electronic era. Nowadays most of the power amplifiers used in real-world applications are positioned between the many existent classes of power amplifiers. The requisites of each application can dictate which classes of power amplifiers are better suited. The most important requisites are output power, gain, efficiency and linearity most times a trade-off exists between these requisites.

PA can also be defined by their operation mode, and can be separated in two major groups that work in linear and non-linear mode as it is shown in 2.1. The latter refers to a PA that only has phase linearity but no amplitude linearity. Amplitude linearity exists when there is a linear correlation between the output magnitude and the input voltage.

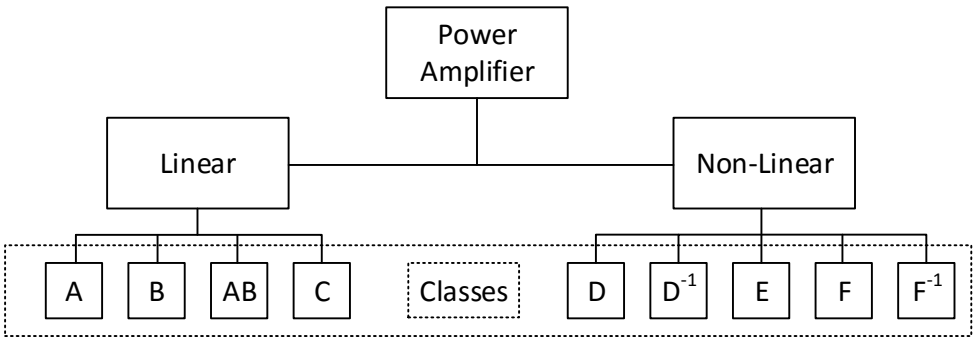


Figure 2.1: Power amplifiers groups and classes.

The inherent high efficiency of non-linear amplifiers is the main motivation for their wide usage. Several wireless systems and standards use only phase modulation and the corresponding waveforms do not have amplitude variations. As a consequence, the PA only needs to have phase linearity and the amplitude linearity is of no concern. Hence, the non-linear behaviour is not considered as a major drawback.

2.1.1 Linear Amplifiers

As it is seen from figure 2.1 the following classic topologies for linear power amplifiers are defined: A, AB and C. As mentioned before, this group of amplifiers is able to amplify signals with non-constant envelope, such as modulated amplitude signals. All these classes share a common topology. All of them can be implemented using the same circuit, which is depicted in figure 2.2. The amplifier class of operation is distinguished exclusively by the bias conditions. All these classes are driven with a sinusoidal waveform or approximately sinusoidal. The transistor behaves as a voltage-controlled current-source, at least for a certain portion of the wave cycle [3].

The tuned parallel LC filter, shown in figure 2.2, is not a part of the basic schematic circuit for this kind of amplifiers, even so it's recommended to filter the signal outside the fundamental frequency. This will ensure an improvement in the efficiency of the amplifier, because the device only affects the load at the fundamental frequency. At all the other frequencies the filter acts as a short-circuit to the ground.

The class of operation of linear amplifiers can easily be identified by observing the drain current waveform. The percentage of the wave cycle in which the transistor is conducting defines the power amplifier operation class. Table 2.1 shows the differences between the linear classes of amplification [p. 37][2].

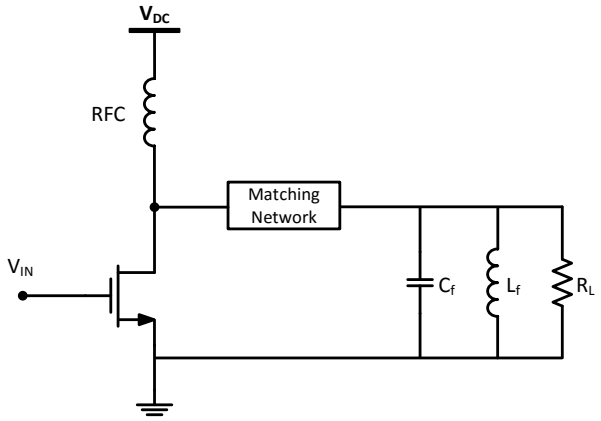


Figure 2.2: Linear power amplifiers schematic

Table 2.1: Transistor conduction angle.

Class	Conduction Angle (degrees)
A	360° (100%)
B	180° (50%)
AB	180°>and <360°
C	<180°

Class-A amplifier

For the amplifier to operate as a Class-A, the bias levels must be chosen so that the transistor is kept in the active region for all the time. Hence, the drain current waveform has a conduction angle of 360°, which is all of the wave period as shown in figure 2.3.

The Class-A has the highest conduction angle of all linear amplifiers, leading to the lowest efficiency achieved of all linear amplifiers. The maximum theoretical efficiency achieved by the Class-A is 25%, it can be calculated as,

$$\eta_D = \frac{P_{out}}{P_{DC}}, \tag{2.1}$$

$$= \frac{1}{2}\left(\frac{V_{out}}{V_{DC}}\right)^2, \tag{2.2}$$

where V_{out} is the output voltage amplitude.

Hence, it can be concluded that the amplifier only achieves its 50% of maximum efficiency, when the maximal output swing occurs ($V_{out} = V_{DC}$). If this amplifier is used with an amplitude modulated signal, the output voltage V_{out} will change according to the envelope signal $A(t)$. If we consider the probability density function of $A(t)$, the efficiency of the amplifier will fluctuate with it, leading to an average efficiency much lower than 50% [p. 32][2].

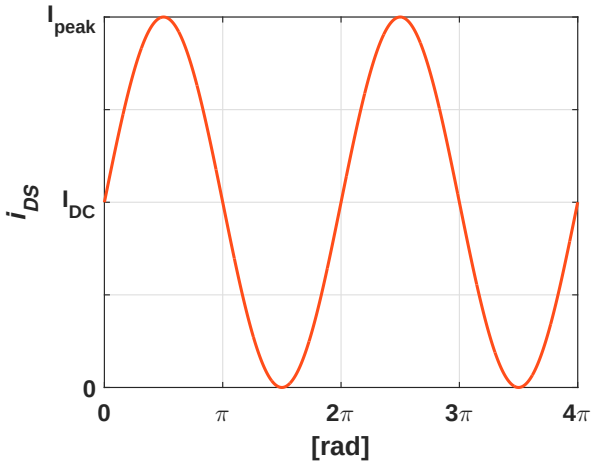


Figure 2.3: Class-A amplifier drain current waveform for two periods.

Class-B amplifier

The Class-B amplifiers have their bias levels chosen in a way that the drain current waveform has a conduction angle of 180°. The operation point of the transistor is located exactly at the boundary between the cut-off and the active region [p. 117][4]. The lower conduction angle compared with Class-A lead to an increase in efficiency, but the linearity of the amplifier is degraded. The drain current waveform is depicted in figure 2.4. The Class-B drain efficiency is given by,

$$\eta_D = \frac{\pi}{4}\left(\frac{V_{out}}{V_{DC}}\right)^2. \tag{2.3}$$

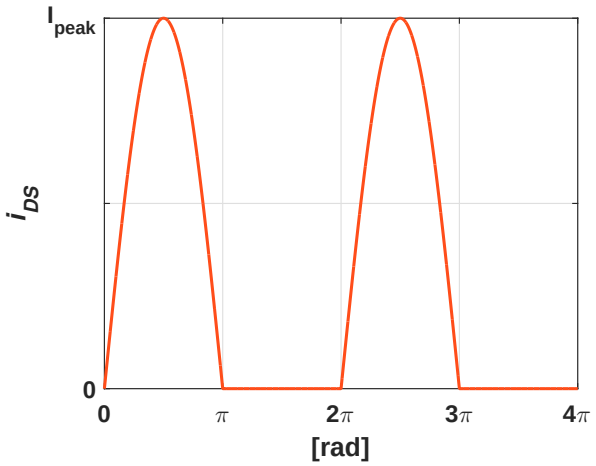


Figure 2.4: Class-B amplifier drain current waveform for two cycle.

Like in the Class-A amplifier, the maximum efficiency only occurs when $V_{out} = V_{DC}$, which leads to an approximated efficiency of 78.5% [p. 124][4]. If an amplitude modulated

signal is amplified, the average efficiency will also drop according to the envelope signal probability density function $A(t)$.

Class-AB and C amplifiers

The Class-AB configuration works between the Class-A and Class-B operation angle, which is between 180 and 360 degrees. Depending on its bias levels, this type of amplifier conducts somewhere between 50% and 100% in each cycle. Hence, the drain efficiency lays somewhere between the 50% maximum of the Class-A amplifier or the 78.5% of the Class-B. As shown in table 2.1 the Class-C amplifier has the lowest conduction angle of all the linear amplifiers. Although the efficiency rises when the conduction angle is lowered, the amplifier becomes less linear because turning off the transistor increases the number of higher harmonics generated [p. 34][2]. This non-ideal behaviour is not considered in the present analysis. The LC resonant tank is considered to have a high-quality factor, which becomes a short circuit to undesired frequencies besides the fundamental one. The drain current waveform is presented in figure 2.5.

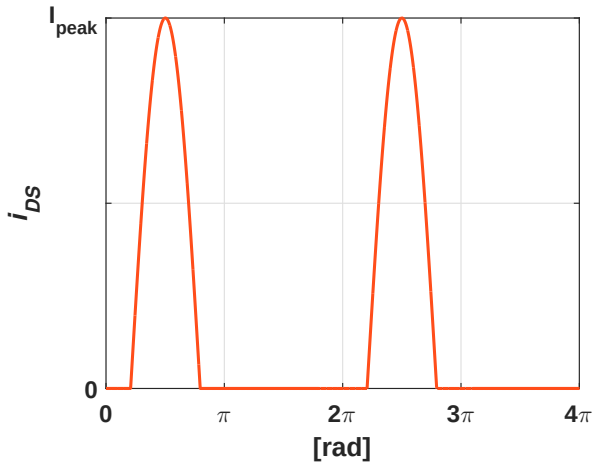


Figure 2.5: Class-C amplifier drain current waveform for two cycles.

Some authors do not consider the Class-C as part of the linear amplifiers group. This is due to its low conduction angle, which greatly reduces the drain current linearity. In fact, the amplifier drain efficiency can be arbitrary increased toward 100% by decreasing the conduction angle until zero. This has the drawback of also reducing the utilization factor of the amplifier toward zero and increasing the drive power to the infinity [5]. The drain efficiency of a Class-C amplifier can be obtained by,

$$\eta_D = \frac{\theta - \sin(\theta)}{4\left[\sin(\frac{\theta}{2}) - \frac{\theta}{2}\cos(\frac{\theta}{2})\right]}, \tag{2.4}$$

where θ represents the conduction angle [6], which for a Class-C will be between 0 and 180°.

The equation 2.4 is also valid for classes A, B and AB with their respective conduction angles. Table 2.2 contains the drain efficiency of the several linear amplifiers presented. Notice that the Class-AB and C amplifiers have a range of possible values that depend on the conduction angle, as previously mentioned.

Table 2.2: Efficiency of the linear amplifiers.

Class	Conduction Angle (degrees)	Maximum Efficiency(η)
A	360° (100%)	25%-50%
B	180° (50%)	25%-78.5%
AB	180°>and <360°	50% <-> 78.5%
C	<180°	78.5% <-> 100%

2.1.2 Non-Linear Amplifiers

The non-linear amplifiers group is also known as switch-mode power amplifiers. In this group of PAs the transistors act like switches that turn on and off during operation. The classes of non-linear amplifiers are D, D^{-1}, E, F and F^{-1} as shown in figure 2.1. Considering ideal switches, which don't dissipate any power at their terminal, either the voltage is zero or the current that flows through them is zero. Thus, the resulting product voltage-current is always zero. So, the transistor dissipates no power and the efficiency must be ideally 100% [p. 541][6] if there are no other losses in the amplifier circuit. This makes this group of amplifiers a good solution to amplify constant envelope signals. The class-D is the main subject of this thesis and will be discussed in detail in chapter 3.

Class-D^{-1} amplifier

A current-mode Class-D^{-1} amplifier topology is shown in figure 2.6. Both transistors are driven by two square waves with opposite phase that ensures that only one transistor is active at a time. The RFCs chokes act like DC current sources, therefore, combined with the switching action of the transistor, the current always flows from one branch of the circuit to the other and passing through the RLC circuit.

The RLC parallel network is tuned for the fundamental frequency f_c, for all other frequencies it behaves like a short-circuit. Therefore, the only current flowing at R_L is the current of the fundamental frequency, which is a sinusoid, assuming that the quality factor Q_L of the RLC network is high enough. The sinusoidal current at the load leads to a sinusoidal voltage at the terminals of R_L.

During the switching action of the transistors only one of them is connected at a time. When one of them is off it fells the sinusoidal voltage waveform of R_L at their drain. Since each of them is only connected for half of the period of the sine-wave voltage, the voltage felt at V_{DS} is a half sinusoid that is shown in the figures 2.7 and 2.8.

There is no voltage drop at the RFCs tanks. Each branch has a semi-sinusoidal waveform with a mean value of V_{DC}, and at each circuit branch, the peak drain voltage is πV_{DC}

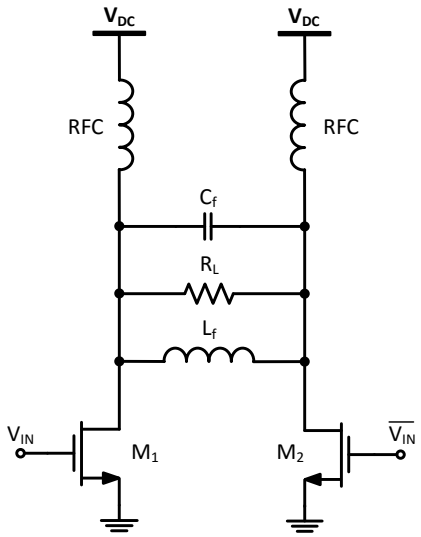


Figure 2.6: Class-D^{-1} power amplifier schematic.

[7].

Figures 2.7 and 2.8 show the current waveform for each transistor when they are on the on-state. In this state two DC currents flow through one of the transistors connecting both RFC chokes to the ground. The transistor has to be able to withstand these two currents.

A disadvantage comes from the situation when the current flows through each transistor ($I_{DS} = 2I_{DC}$) that leads to the conduction loss due to the internal resistance of each transistor.

To maintain the transistor conduction loss at low levels, the internal resistance of the transistor r_{DS} has to be smaller. This can be achieved by increasing the width of the transistors. Hence, large transistors have to be used.

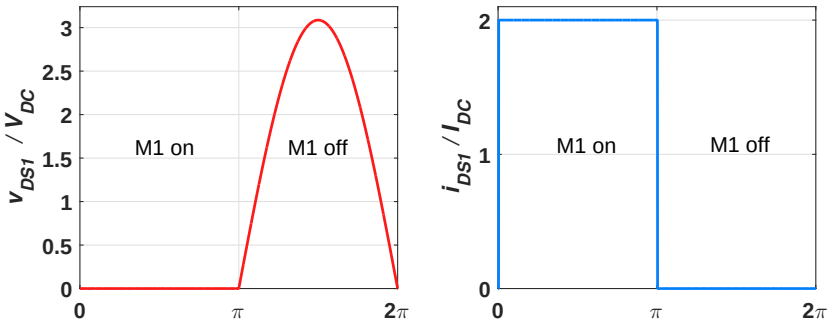


Figure 2.7: Class-D^{-1} transistor M_1 voltage and drain current waveforms.

Class-E amplifier

The basic configuration of a class-E power amplifier is depicted in figure 2.9. The output network is made of series tuned circuit RLC and a shunt capacitor C_s. This capacitor includes the inherent parasitic capacitance of NMOS transistors. The C_s capacitance value

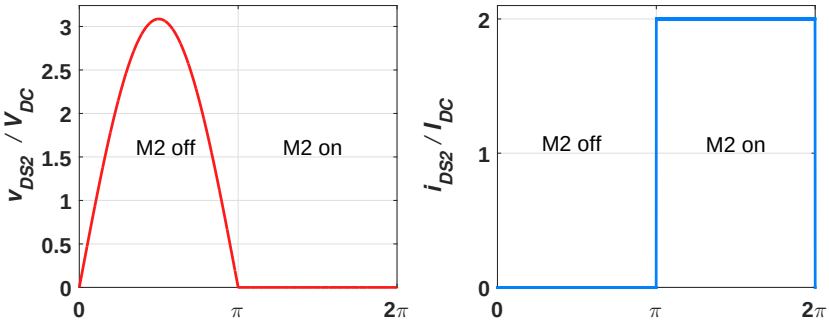


Figure 2.8: Class-D[-1] transistor M_2 voltage and drain current waveforms.

should be carefully designed, because it is responsible for the soft-switching capability of the class-E amplifier. Hard-switching devices suffer from switching losses. This occurs when the voltage across the transistor drops abruptly from a high value to zero. The shunt capacitance C_s charges and discharges between the ON and OFF state of the transistor. Therefore, C_s does not allow instant variation in the drain voltage. This guarantees a smooth transition between the ON-OFF states of the transistor [p. 246][4].

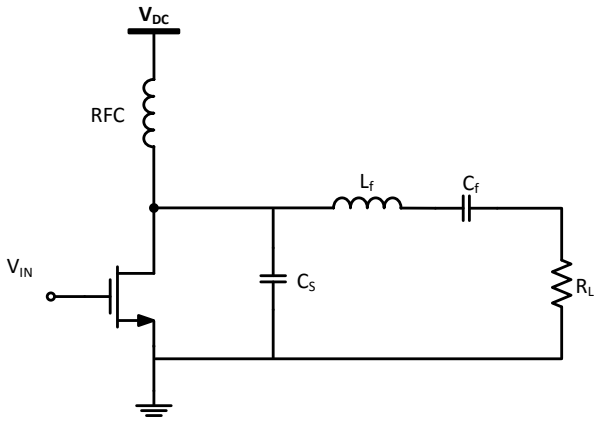


Figure 2.9: Class-E power amplifier schematic.

Since the class-E architecture absorbs the parasitic capacitance of the transistor with C_s, the so-called Zero Voltage Switching (ZVS) state is achieved. This prevents energy loss at each RF cycle, which is critical at high frequencies, thus, increasing the amplifier performance [p.53][2].

Another switch characteristic responsible for the efficiency drop in power amplifiers is the on resistance r_{on}, associated with MOSFET transistors. This parasitic component can be diminished by increasing the transistor size, but this also increases the parasitic C_{ds} capacitor and C_{gs}, increasing the driving requirements.The major drawback of the Class E amplifier is the high drain voltage that occurs when the switch is open. This value is, in the ideal case, given by $v_{DS} \approx 3.562 V_{DC}$.The voltage and current drain waveforms[1] of the device are presented in figure 2.10.

[1]The peak drain current value $i_{DS} = 2.862 I_{DC}$ is given in [p. 250][4]

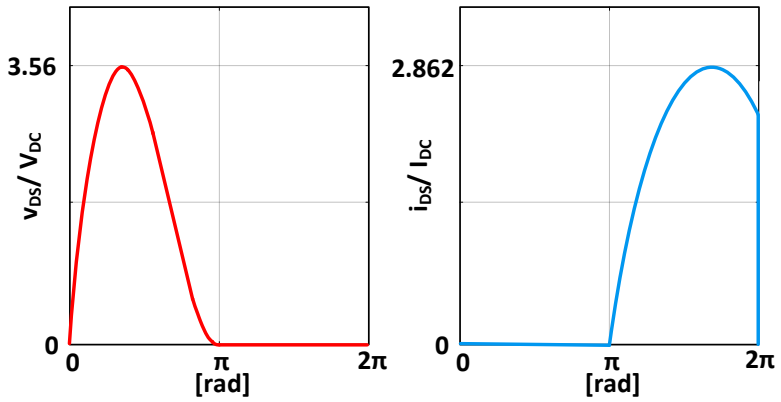


Figure 2.10: Class-E voltage and drain current waveforms.

Class-F amplifier

Class-F amplifiers shown in figure 2.11, present an elegant solution in order to achieve high-efficiency. This class of amplifiers is characterized by a load network with resonance frequencies at one or more harmonic. The tank resonators are tuned to odd-harmonics, which maintain a square voltage waveform at the transistor drain and simultaneously provides a half-sinusoidal current waveform [p. 104][8]. An infinite number of tanks must be used to set the ideal waveform shaping shown in figure 2.12.

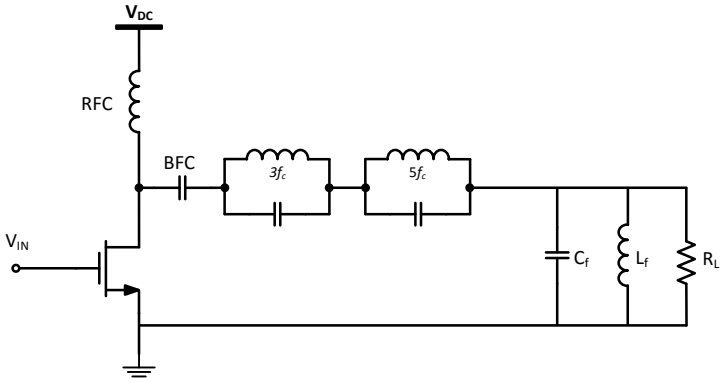


Figure 2.11: Class-F power amplifier schematic with 5th harmonic peaking.

Ideally, all parallel resonant circuits have infinite impedance at the corresponding harmonic resonant frequency and zero impedance at other harmonics [p. 105][8]. Consequently, the load impedance "felt" by the transistor is R_L at fundamental frequency, infinite at the tank resonators frequencies and zero otherwise.

From figure 2.12 we can see there is no overlap between voltage and current due to the harmonic filtering of the tank resonators, this happens assuming an ideal situation. Thus, no power dissipation is produced, leading to 100% of theoretical efficiency. In practice, the infinite harmonic tuning is not achievable. Most of the times the load network is setup by

harmonic filtering tuned up to the 3rd or 5th harmonic only[2]. This lowers the obtainable efficiency below the maximum theoretical efficiency.

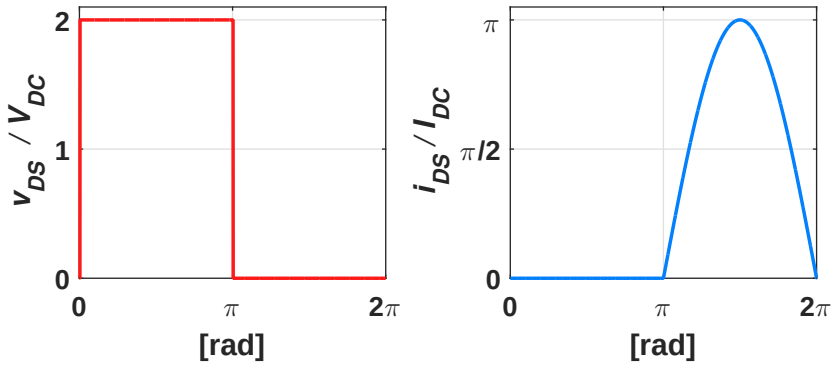


Figure 2.12: Class-F voltage and drain current waveforms.

Class-F^{-1} amplifier

The inverse class-F power amplifier can be implemented using the circuit shown in figure 2.13. The circuit shown in figure 2.12 can also be used, but now the tank resonators need to be tuned to even-harmonic resonant frequencies. This duality in the configuration can be applied also to the inverse class-F amplifier. Thereby, it is necessary, in this case, to perform the tuning only with even-harmonics [p. 161][8].

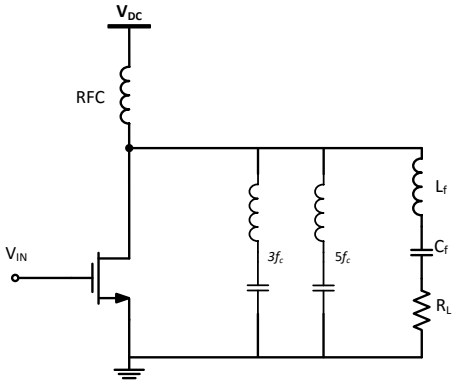


Figure 2.13: Class-F^{-1} power amplifier schematic with 5th harmonic peaking.

By analysing the schematic represented in figure 2.13 it can be seen that at the fundamental frequency and odd-harmonics, each resonant circuit has zero impedance, but for even-harmonics they have infinite impedance. This produces the idealized square current and the half-sinusoidal voltage waveforms at the drain terminal, as shown in figure 2.14. As a result, the active device feels the load resistance R_L at the fundamental frequency, while the odd-harmonics are shorted by the series resonant circuits [p. 161][8].

[2]commonly called harmonic peaking

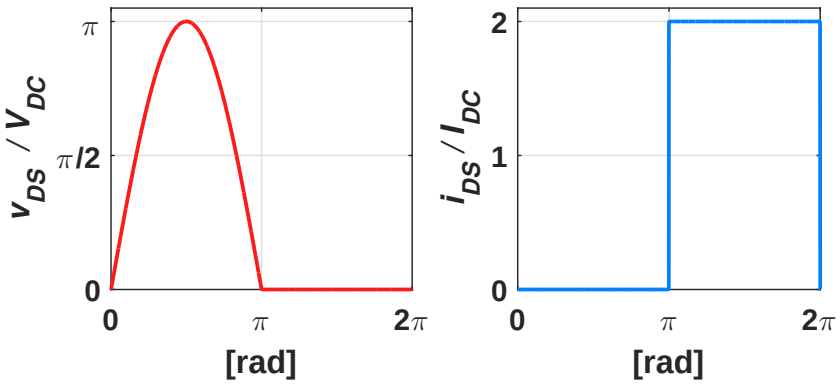


Figure 2.14: Class-F^{-1} voltage and drain current waveforms.

2.2 Definition of Output Power

Figure 2.15 shows a power amplifier connected to an antenna. The output power is characterized by the active power delivered by the power amplifier to the antenna. In the antenna the power delivered by the amplifier is disposed under the form of electromagnetic radiation. The antenna impedance $Z_{antenna}$ is usually designed to be entirely resistive at the frequencies of interest. Hence, at these frequencies the antenna can be represented by a load resistor R_{Load}. By definition the power dissipated in R_{Load} is equal to the power of the electromagnetic radiation transmitted by the antenna [Ch. 9 p. 5][9].

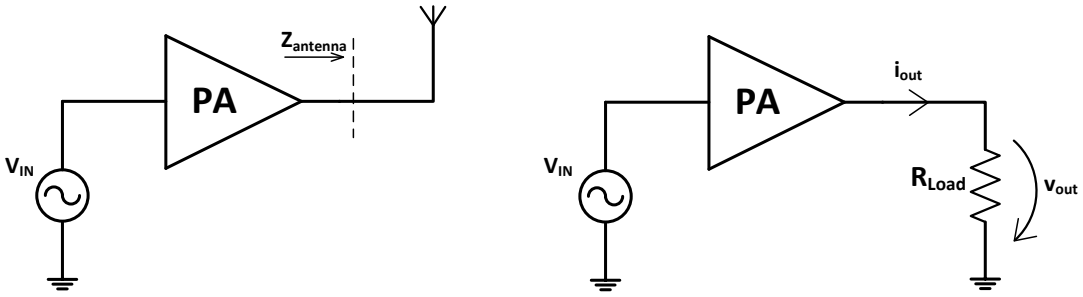


Figure 2.15: Definition of power output.

In RF and microwave system it is common to design R_{Load} to have 50 Ω . Antennas and microwave components typically have single-ended input and output impedances of 50Ω. Test equipments, as well as connector and cables used in test and modular systems, are made with such impedance value of 50 Ω that helps in the standardization [p. 6][10].

The instantaneous output power in a given moment is defined as,

$$p_o(t) = v_{out}(t) \cdot i_{out}(t). \tag{2.5}$$

The total (average) output power $P_{o_{tot}}$ is given by,

$$P_{out_{tot}} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} p_o(t)\mathrm{dt}. \tag{2.6}$$

If the output voltage is a sine wave with a frequency f_c and with a period T_c, the previous equation becomes,

$$P_{out_{tot}} = \frac{1}{T_c} \int_{-T_c/2}^{T_c/2} p_o(t)\mathrm{dt}. \tag{2.7}$$

Since the load is assumed to be purely resistive,

$$\begin{aligned} P_{out_{tot}} &= \frac{1}{T_c} \int_{-T_c/2}^{T_c/2} v_{out}(t) \cdot i_{out}(t)\mathrm{dt} = \frac{1}{T_c} \int_{-T_c/2}^{T_c/2} \frac{v_{out}(t)^2}{R_{Load}}\mathrm{dt} \\ &= \frac{V_{out_{rms}}^2}{R_{Load}}. \end{aligned} \tag{2.8}$$

Where the RMS value is given by,

$$V_{out_{rms}} = \sqrt{v_{out}^2(t)}. \tag{2.9}$$

One major factor is that the amplifier will not only produce power at the desired frequency, but also at the integer multiples of the fundamental frequency f_c. Usually, only the power of the fundamental frequency is desired and the harmony power has to be filtered at the output. Hence, there is only interest in the average output power of the fundamental frequency which is given by,

$$P_{outf_c} = \frac{V_{out}^2}{2R_{Load}}, \tag{2.10}$$

where V_{out} is the amplitude of the sinusoidal output voltage at the frequency f_c. To obtain this value the Fourier Series expansion of $v_{out}(t)$ has to be made.

2.3 Amplifier Efficiency

The aim of the power amplifier is to deliver a certain amount of power to the load, without consuming much DC power. Figure 2.16 shows the DC power consumption of the PA P_{DC} which is always larger then the output power P_{out}.
The drain efficiency η_d is defined as,

$$\eta_d = \frac{P_{out}}{P_{DC}}. \tag{2.11}$$

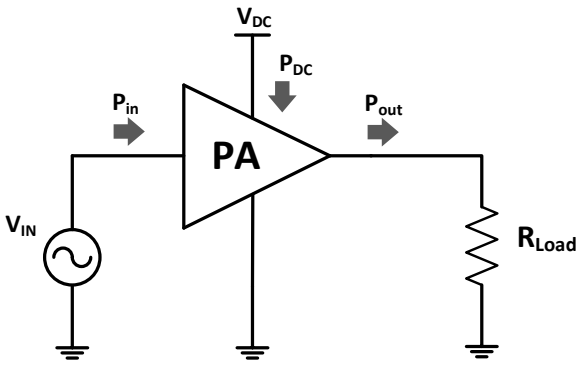


Figure 2.16: DC power consumption

The 2.11 equation is the efficiency at the fundamental frequency since the output power P_{out} is the power of the fundamental frequency defined in equation 2.10.

It can be desired to know the total conversion efficiency, which is the conversion of the total RF output power defined by equation 2.8. It includes the power of the fundamental frequency and the higher harmonics. The total conversion efficiency is given by,

$$\eta_{tconv} = \frac{P_{out_{tot}}}{P_{DC}}. \tag{2.12}$$

In most cases, driver stages are needed in the transmission chain as it is shown in figure 2.17. The drivers are used between the signal source and the last amplifier stage. The drivers will consume DC power, even so its not an easy task to define input and output power since the impedance levels at the input and output of each stage are different and normally composed of real and complex part.

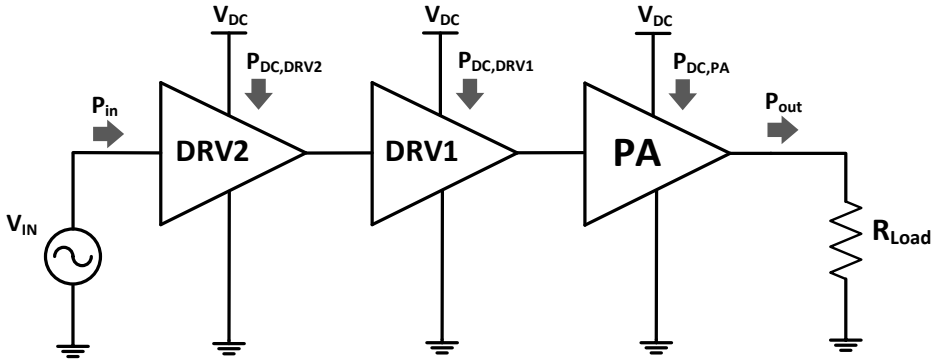


Figure 2.17: DC power consumption including driver stages.

If the DC power consumption of the drivers is taken into account the overall efficiency of the PA is given by [11],

$$\eta_{ov} = \frac{P_{out}}{P_{DC,PA} + \sum_{i=1}^{\infty} P_{DC,DRV,i}}. \tag{2.13}$$

The more stages the driver has, the higher power gain will be. However, it also depends on whether the amplifier is linear or non-linear. On the other hand, the amplifier overall efficiency η_{ov} will be degraded with the increasing number of driver stages.

If the RF input power P_{in} is taken into account then it leads to the Power Added Efficiency (PAE) which is given by,

$$PAE = \frac{P_{out} - P_{in}}{P_{DC,PA} + \sum_{i=1}^{\infty} P_{DC,DRV,i}}. \tag{2.14}$$

The drain efficiency of the PA in theory can be 100%. Yet the overall efficiency, even in the ideal case, will be less than 100%. This happens due to the power consumed in the driver stages. The power in the drivers will not reach the load, instead, it will be dissipated at the input of the next driver. Hence, even if the power amplifier and the driver stages have an efficiency of 100%, the overall efficiency will not reach such value.

So which definition of efficiency is more accurate? From the circuit point of view, the drain efficiency and the PAE seem to be more appropriate. From the system point of view, the PA is everything after the up-conversion. Hence, the overall efficiency η_{ov} is better suited to indicate how much power is needed to amplify the signal relatively to the output power.

2.4 Transmitter Architectures

In wireless communication systems the signal processing takes place in the digital domain at baseband frequencies, which are much lower than RF frequencies that are needed for transmission. In order for the transmission to be realized, an up-conversion from the baseband signal to RF is needed. This up-conversion can be realized with various techniques, including analogue mixing, direct digital conversion and the combination of digital/analogue up-conversion.

In a fully analogue up-conversion, the digital baseband signal is converted into an analogue signal and then up-converted into an RF analogue signal. The up-conversion can be realized in one or two steps. An RF transmitter preforms three main tasks: modulation, up-conversion and power amplification. The transmitter has three important performance specifications: modulation, spectral emissions and RF output power. In the transmitter band selection and noise are not critical parameters as in receivers, since the signal is created locally. The variations of the signal level are small, what leads to less restricted requirements in terms of the dynamic range. There are two transmitter architectures in a fully analogue up-conversion: heterodyne, that uses two step conversions from baseband to RF, and direct up-conversion, where the signal is converted directly from the baseband to RF.

At the output in the PA stage a high output power is generated, leading to a high DC power consumption. In some cases the transmitter can be shut down after the signal transmission to save power. Transmitter design requires a solid understanding of modulation

schemes because of their influence on the choice of the building blocks of the transmitter, such as, mixers, oscillators and Power Amplifiers PA.

2.4.1 Heterodyne Transmitters

Figure 2.18 shows a block diagram of a heterodyne architecture [p. 25][12]. In the baseband two digital signals are generated, I and Q, which are converted to analog signals. During the frequency up-convention into IF, the signal Q is phase-shifted by 90° with respect to the I signal. After the quadrature signals are summed, an IF bandpass filter is used to remove the harmonics of the IF signal, this reduces the noise present in the signal.

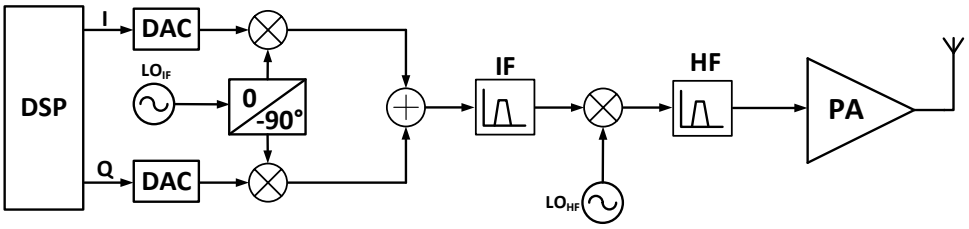


Figure 2.18: Heterodyne transmitter.

The quadrature signal I/Q is up-converted to RF and filtered again to remove the harmonic content. The PA receives and amplifies the RF signal and sends it to the antenna to be transmitted. Due to the off-chip passive elements in IF and RF filters this architecture does not allow full integration.

2.4.2 Direct Up-conversion Transmitter

The direct up-conversion transmitter, shown in figure 2.19, converts directly the baseband signal to the RF carrier frequency, this frequency is given by the local oscillator. In this topology modulation and up-conversion occur in the same circuit. This architecture can be integrated in a better way than the heterodyne one, because there is no need for the suppression of any mirror signal generated during the up-conversion [p. 26][12]. Since the up-conversion is made in quadrature, the upper and lower sideband of the wanted signal are each others mirror signal and unwanted interference is prevented.

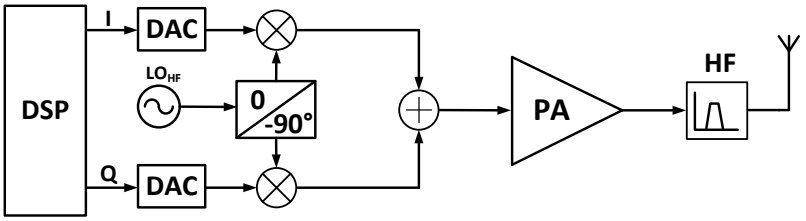


Figure 2.19: Direct up-conversion transmitter.

The disadvantage of the direct up-conversion appears from the fact that the local oscillator(LO) frequency is equal to the carrier frequency of the RF signal. Two drawbacks

appear from this situation. First, the crosstalk[3] of the LO signal to the RF output of the up-conversion mixer will be transmitted. Since the crosstalk effect is situated at the same frequency as the RF signal, the output bandpass filter will not be able to suppress this effect.

The second drawback is the self modulation of the local oscillator that may occur. The RF signal is up-converted and amplified by the PA to the necessary signal power to be transmitted. If the signal output power is too large it can easily couple with the sensitive local oscillator when both are at the same frequency. This effect can degrade the performance of the circuit.

2.4.3 Direct Digital Conversion

In direct digital conversion, all the signal processing and up-conversion is made in digital domain. Further, the signal is converted to the analogue domain to be amplified by the PA. The direct digital conversion architecture can be seen in figure 2.20. The baseband signal is generated with a digital modulator using a Direct Digital Frequency Synthesizer (DDFS). The signal is up-converted with an up-mixer to radio frequency. The digital RF signal is fed into D/A converter to be converted into the analogue domain to be amplified in the PA stage. The usage of a multi-bit D/A converter is susceptible to glitches and spurious noise as the RF frequency increases. The generated noise is difficult to remove by filtering the signal. The digital circuit is processing the signal in RF frequencies, leading to very high sampling frequencies causing high power dissipation[14].

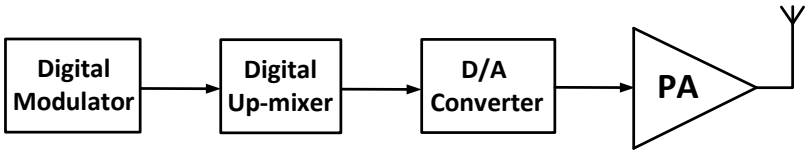


Figure 2.20: Block diagram of a direct digital up-converter.

2.4.4 Sigma-Delta Direct Digital Conversion

A direct digital converter that uses a Sigma-Delta DAC[4] is presented in figure 2.21. This topology is similar to the previously mentioned Direct Digital Conversion. The main difference is the replacement of the multi-bit D/A converter for a 1-bit $\sum\Delta$ D/A converter, which solves some problems of the multi-bit D/A due to its noise shaping. But it is suitable only for relatively narrowband signal. This narrowband nature of the $\sum\Delta$ D/A converter is suitable for many wireless communication standards, since the signal bands are relatively narrow compared to the RF carrier frequency [15].

[3]This effect is explained in [p. 118][13]
[4]Digital to analogic converter.

The 1-bit $\sum\Delta$ DAC surpasses some of the problems related to the multi-bit DAC. Since the output of the 1-bit $\sum\Delta$ DAC only has two levels, any mismatch of the levels results in gain error or offset. None of these effects are of great importance in many transmitter applications. Since the $\sum\Delta$ D/A converter is a full digital circuit, it has many advantages over analogue signal processing, such as, noise immunity, reliability, performance and power consumption that is due to the scaling of the technology. The use of a DDFS with $\sum\Delta$ D/A converter is an attractive solution for digital transmitter because it allows the usage of switching-mode power amplifier. This implementation may lead to a high efficiency transmission [15].

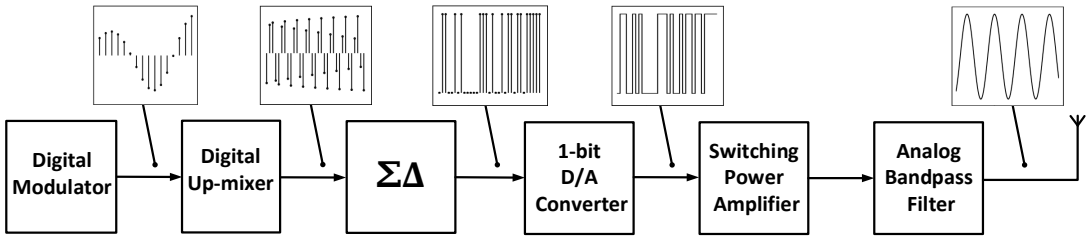


Figure 2.21: Block diagram of a direct digital up-converter using a Sigma-Delta DAC.

2.5 Transmission Modulation Technique Example: *Bluetooth*

Considering the technical requirements for the PA used in this thesis, such as operating frequency, output power and the modulations schemes, the communication standard that is suited for this project is the *Bluetooth*. It operates in the ISM 2.4 GHz frequency band, uses low power schemes and most modulations use constant envelope signals, which can be used in switching amplifiers [p. 216][2].

The table 2.3 shows the different levels required by the Bluetooth standard [16]. It is generally used for short-distance wireless communication between several devices up to 100 meters distance. *Bluetooth* technology operates in the frequency range of $2400 - 2483.5$ MHz including guard bands, 2 MHz wide at the bottom frequency and 3.5 MHz wide at the top frequency. The *Bluetooth* band is composed of 79 channels [5], each channel has 1 MHz of bandwidth.

Table 2.3: *Bluetooth* Classes.

Class	Power		Range (m)
	(mW)	(dBm)	
1	100	20	100
2	2.5	4	10
3	1	0	1

[5]The *Bluetooth* channels are numbered from 0 to 78.

Table 2.4: *Bluetooth* ACPR requisites.

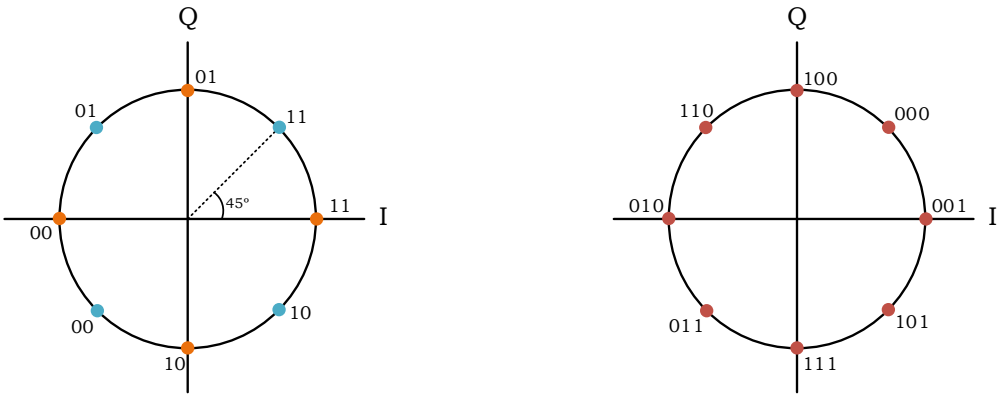
Frequency Offset	Transmit Power
$\pm$ 500 kHz	-20 dBc
2 MHz	-20 dBm
3 MHz	-40 dBm

An important measurement of the *Bluetooth* standard is the Adjacent Channel Power Ratio (ACPR). Most standards define ACPR measurements as the ratio of the average power in the adjacent frequency channel to the average power in the transmitted frequency channel. It describes the amount of power generated in the adjacent channel due to nonlinearities in RF components. The spectral regrowth causes interference with adjacent channels, a high spectral regrowth value can ruin the system transmission capability.

The transmitted power is measured at 100 kHz bandwidth, at maximum power. Table 2.4 shows the ACPR requirements for the *Bluetooth* standard [p. 33][16]. At $\pm$500 kHz frequency offset, the transmitted power should be 20 dB below the power at zero frequency offset. In the *Bluetooth* specification it is denoted as -20 dBc, but it is actually 20 dB below the power in a 100 kHz frequency band around the carrier frequency. An adjacent channel power requirement is the integrated power over 1 MHz band and it should be low enough in the neighbouring or adjacent channels. For a channel spacing of two channels, the power transmitted at 1 MHz band should be lower than -20 dBm. For a channel spacing of more than three channels, the power should be lower than -40 dBm [p. 33][16].

The first *Bluetooth* used Gaussian Frequency-Shift Keying (GFSK) modulation in which the positive and negative frequency deviations represented the binary 1 and 0. With the appearance of the *Bluetooth* 2.0 + Enhanced Data Rate (EDR) the EDR brings two Phase Shift Keying (PSK) modulation scheme. The $\frac{\pi}{4}$-Differential Quadrature Phase-Shift Keying (DQPSK) and the 8-Differential Phase-Shift Keying (DPSK) can achieve speed of 2 Mb/s and 3-Mb/s, respectively, in comparison to the 1 Mb/s from the older *Bluetooth* version(1.2) [p. 34][16].

A $\frac{\pi}{4}$-DQPSK constellation is shown in figure 2.22a. It consists of two equal constellations, 45° ($\frac{\pi}{4}$) out-of-phase from each other. A jump between two symbols is always made with $\frac{3\pi}{4}$,$\frac{\pi}{4}$,$\frac{-\pi}{4}$ or $\frac{-3\pi}{4}$ radians. Hence, the symbols are always jumping between the two existing constellations [p. 305][17]. In figure 2.22b a 8-DPSK modulation is depicted. With this scheme it is possible to achieve the data rates up to 3 Mb/s. The utilization of 3 bits instead of 2, presented in the $\frac{\pi}{4}$-DQPSK modulation, ensures a higher data rate for the 8-DPSK modulation [p. 35][16].



(a) $\frac{\pi}{4}$-DQPSK constellation.

(b) 8-DPSK constellation.

Figure 2.22: *Bluetooth* Modulation Schemes.

Further *Bluetooth* technology evolved into version 3.0+HS. This evolution brings improvements to the modulation scheme by achieving high data rate speeds comparing to *Bluetooth* 2.0 + (EDR). Even so, this version uses the non-constant envelope signals. Therefore, a linear power amplifier should be used, whose efficiency is usually low. There are alternative solutions which use non-linear amplifiers, such as class-D with digital polar modulation[18]. However, this is outside of the scope of this thesis.

Recently a new technology, called the *Bluetooth* V4.0+ also known as *Bluetooth* Low Energy (BLE), was developed. With the objective of providing a reduced power consumption and cost while maintaining a similar communication range comparing to classic *Bluetooth*, it achieves an energy efficiency 20 times higher. The extremely low peak, average and idle currents of BLE chipsets, shown in table 2.5, enable BLE devices to work with very small battery power sources for a year or more [19].

Table 2.5: BLE chipsets current consumption.

Peak Current	Idle Mode Current	Average Current
tens of mA	tens of nA	$\approx \mu A$

BLE uses the same frequency range as Classic Bluetooth $2400 - 2483.5$ MHz. BLE uses only 40 channels, 2 MHz wide, while Classic Bluetooth uses 79 channels, 1 MHz wide. BLE uses special channels selection techniques to save energy [19]. Also, the modulation scheme is the same: both technologies use a Gaussian Frequency Shift Keying (GFSK) modulation. BLE, however, uses a modulation index of 0.5 compared to 0.35 for Classic Bluetooth technology. This change lowers power consumption and also improves the range of BLE versus classic *Bluetooth* [19]. The use of constant envelope signal make this technology suitable for non-linear PA.

Table 2.6: BLE Output Power requisites.

Minimum Output Power	Maximum Output Power
0.01 mW (-20 dBm)	10 mW (+10 dBm)

One of the main features of BLE is the low output power shown in table 2.6[p. 16][20]. The operation frequency, high efficiency, low power output requirements and constant envelope modulation make BLE a suitable communication standard to be used with a RF Class-D PA.

CHAPTER 3

RF CLASS-D POWER AMPLIFIER WITH SIGMA-DELTA MODULATION

In this chapter a RF CDVS PA is discussed. The switching devices are MOSFET transistors. Certain conditions have to be achieved so they can operate as switches. The waveform of the Class-D will be presented and explained, it will be shown analytically that the Class-D amplifier can achieve an ideal efficiency of 100%, that is due to the Zero Current Switching (ZCS), which can be achieved in an ideal CDVS PA. A non-ideal analysis is preformed to give some insights about which factors will be involved in the degradation of the efficiency.

A MOSFET transistor, working in the linear/triode region, is presented in this chapter along with the equations that characterize it. The CMOS inverter is also described, which has two transistors working as switches, PMOS and a NMOS. The CDVS PA is analysed using and ideal and a non-ideal analysis. The CDVS PA needs to be driven due to the high capacitance present at the gate, therefore, a gate driver that solves this problem is presented in this chapter. The output series-resonant circuit is a bandpass Butterworth filter that is also presented here with the design equations.

A 1-bit Sigma-Delta $\sum\Delta$ modulator is described at the end of the chapter. It produces a pulse train that is used to drive the CDVS PA, some examples of previous applications of $\sum\Delta$ modulators with class-D amplifiers are presented.

3.1 MOSFET as a Switch

The active devices employed in the CDVS PA are MOSFET transistors, in this case the expressions given are for NMOS transistor. It is desirable that the transistors work as switches. For this to be achieved the transistor is set to work on the triode/linear region which is given by,

$$\begin{cases} V_{GS} > V_{tn}, \\ V_{DS} \leq V_{eff} = V_{GS} - V_{tn}. \end{cases} \tag{3.1}$$

If $V_{GS} > V_{tn}$, the transistor operates in the strong inversion, and if $V_{DS} \leq V_{eff}$, the transistor is operating in the triode region. After both conditions are set, a current starts to flow trough the transistor from the drain to the source. The triode region equation for a MOSFET transistor, that relates the drain current to the gate-source and drain-source voltages, is given by,

$$i_D = \mu_{n0} C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2}). \tag{3.2}$$

Where μ_{n0} is the low-field electron mobility of the channel and Cox is the gate oxide capacitance per unity area[1]. The channel resistance of a MOSFET in the ohmic region[2] is as shown,

$$r_{DS} = \frac{1}{\frac{i_D}{V_{DS}}} = \frac{1}{\mu_{n0} C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) - \frac{V_{DS}^2}{2})}, \tag{3.3}$$

since V_{DS} is very small, the previous expression can be simplified to

$$r_{DS} \approx \frac{1}{\mu_{n0} C_{ox} \frac{W}{L} (V_{GS} - V_{tn})}. \tag{3.4}$$

The accurate small-signal modelling of the high-frequency operation of a transistor in the triode region is non-trivial. Therefore, a simplified model is used for a small V_{DS} as shown in figure 3.1a. The resistance r_{DS} in the figure is given by (3.4). Here the gate to channel capacitance has been evenly divided between the source and drain nodes,

$$C_{gs} = C_{gd} = \frac{1}{2} C_{ox} W L. \tag{3.5}$$

This equation neglects overlap between the gate and source junction, which is $C_{ov} = WL_{ov}C_{ox}$, where L_{ov} is the effective overlap distance. If accuracy is very important then this equation should be taken into account. The capacitances C_{sb} and C_{db} are highly non-linear, their equations and explanation are quite endeavouring.[3]

[1] $K_n = \mu_{n0} C_{ox}$ is the intrinsic transconductance of the transistor.

[2] Also known as Triode or Linear region, in this region the MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and the drain voltage [21].

[3] C_{sb} and C_{db} are reviewed in [p. 35] [22].

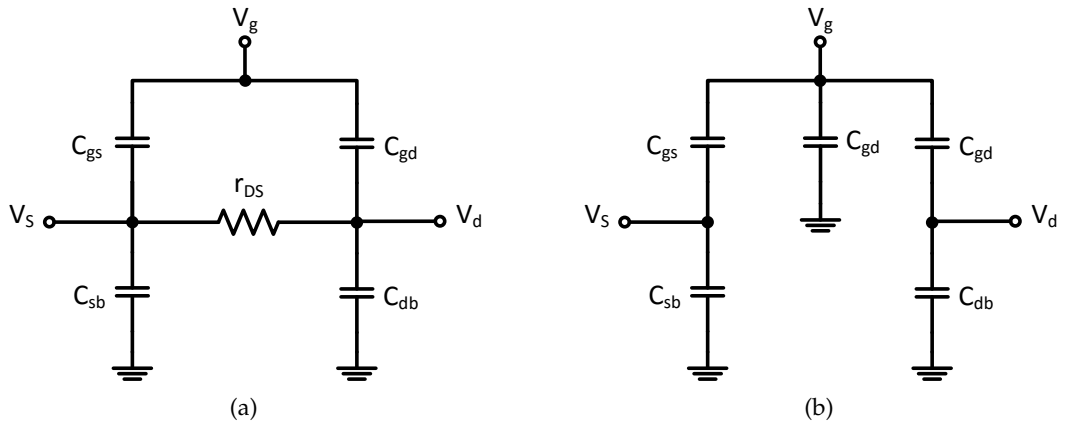


Figure 3.1: Small-signals models. (a) Simplified triode-region model for a small V_{DS}. (b) MOSFET model when is turned off.

When the transistor is on the off state, the small signal model changes substantially this new model as it is shown in figure 3.1b. One of the major differences is that r_{DS} is now infinite. Another difference is that C_{gs} and C_{gd} are now much smaller. Since there is no channel, these capacitors only exist due to the overlap capacitance. Hence, we have

$$C_{gs} = C_{gd} = WL_{ov}C_{ox}. \tag{3.6}$$

The reduction of the C_{gs} and C_{gd} doesn't mean that the total gate capacitance will be smaller. This model contemplates a new capacitor C_{gb}, which is the gate to substrate capacitance and is given by $C_{gb} = WLC_{ox}$. The capacitances C_{sb} and C_{db} are not taken into account for reasons stated above.

Making a quick review, for the MOSFET to behave like a switch, the following conditions have to be achieved $V_{GS} > V_{tn}$, $V_{DS} \leq V_{eff}$. If the first condition isn't achieved, the transistor will behave like an open switch[4], no current will be able to flow through. After the first condition is met, the second one will ensure that the transistor will be on the triode region. In the triode region the MOSFET will behave like a closed switch with a small resistance(r_{DS}), and current is able to pass. In the other hand the gate capacitances C_{gs}, C_{gd} will require a driver before the Class-D PA, this issue will be discussed further ahead.

[4]The resistance r_{DS} will have very high values, ideally would be infinite.

3.2 CMOS Inverter

The main building block of the CDVS PA (figure 3.4) is the CMOS inverter (figure 3.2), which is used in digital circuit design. This block is the PA and it is responsible for converting DC power into RF power. The MOSFET transistors PMOS (M_p) and NMOS (M_n) work as switches. When the input of the inverter is connected to the ground($V_{IN} = 0$), the output is connected directly to V_{DC} thought the PMOS transistor M_p.

When at the input $V_{IN} = V_{DC}$, the output is connected to GND thought the NMOS transistor M_n. With the switching action at the output of the CMOS inverter the voltage swings between the DC supply voltage V_{DC} and the ground. The switching threshold can be set to different values by changing the device size (width), that will also affect the output voltage-swing. Another important fact is that the static power dissipation in the CMOS inverter is practically zero.

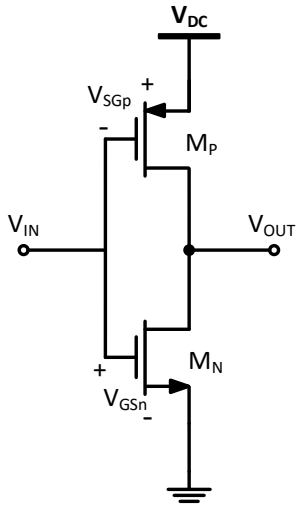


Figure 3.2: CMOS inverter schematic.

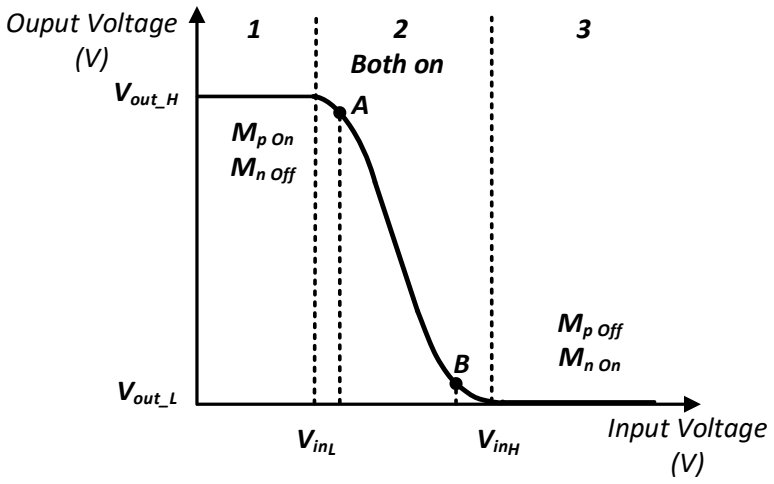


Figure 3.3: CMOS inverter transfers characteristics.

The inverter from the figure 3.2 has the transfer characteristics shown in figure 3.3. When the input voltage is low enough $V_{IN} < V_{in_L}$, the inverter is in the region 1. Here $V_{SGp} > V_{th}$[5], the transistor M_n is off and M_p is on, and the output voltage becomes V_{out_H}. When $V_{IN} > V_{in_H}$, the inverter is in the region 3. Here $V_{GSn} > V_{th}$, M_n is on, M_p is off and the output voltage is V_{out_L}.

In region 2, if $V_{in_H} > V_{in} > V_{in_L}$ then both transistors M_n and M_p are on. Therefore, the current flows from V_{DC} to the ground and, thus, power is lost during this transition. This is the main loss mechanism in the CMOS inverter also known as dynamic power loss.

[5] V_{th} is the threshold voltage of the transistor

3.3 Class D Voltage-Switching Power Amplifier

A CDVS PA circuit is shown in figure 3.4, where the switching devices are a PMOS (M_p) and a NMOS (M_n) transistors. Such configuration is known as an inverter device which is shown in figure 3.2. This topology requires only one driver, however, the cross conduction of both transistors during the MOSFETs transitions may cause spikes in the drain currents. Solutions can be found to avoid this problem, but they are used for low frequency applications, and at RF frequencies the driver complexity increases considerably [23].

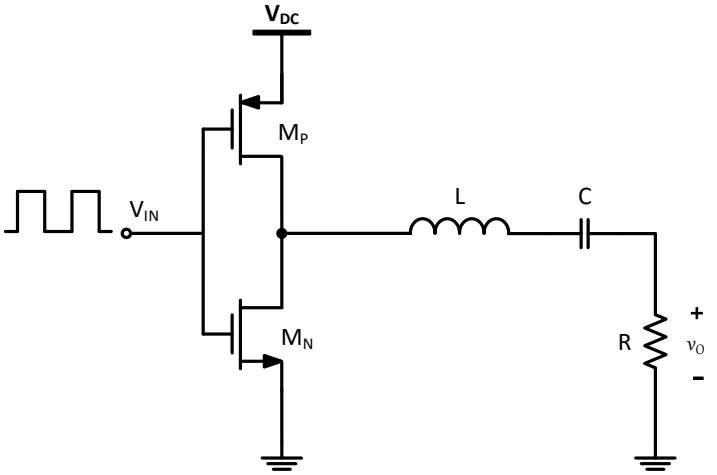


Figure 3.4: A CMOS CDVS PA with a series-resonant circuit.

The peak-to-peak value of the gate-to-source driver voltage V_{IN} is equal or close to the DC supply voltage V_{DC}. This circuit is appropriate only for low values of V_{DC}. For high values of V_{DC}, V_{IN} will be high as well, this may cause voltage breakdown of the gate oxide. The oxide breakdown is a very harmful effect, since it limits the maximum signal swing on the transistor drain. This is one of the main issues of designing PA in sub-micron CMOS technology.

Another issue is the hot carrier effect, it reduces the reliability of the transistor by increasing the threshold voltage, and consequently the performance is degraded. A detailed explanation of this effect can be found in [p. 56][2].

3.3.1 Ideal Analysis

The analysis of the circuit from figure 3.4 will be explained. The following considerations have to be made for this analysis:

- The on-resistance r_{DS} and the parasitic capacitances of the transistor are neglected, and the switching between on and off state is instantaneous.
- The elements of the series-resonant circuit are passive,linear, time invariant, without ohmic resistance and parasitic reactive components.

- The quality factor of the series-resonant is high enough so that the current through the load resistance R is sinusoidal.
- The total resistance of the circuit R_t will only take into account the load resistance R.

The waveforms of a CDVS PA are illustrated in figure. 3.5. The influence of the input signal V_{IN} can be seen here. When $V_{IN} = 0$ the source-gate voltage of the PMOS is $V_{SGp} = V_{DC}$ and the transistor M_p is turned on, while M_n is off. Since the transistor is considered ideal it has no internal resistance, the drain-source voltage is $V_{SDp} = 0$ while $V_{DSn} = V_{DC}$. Subsequently, a current i_{M_p} flows from V_{DC} through M_p, the series-resonant circuit and the load resistance R. Due to the high quality factor of the series-resonant circuit the current sensed by the resistance R is a positive half-sinusoid with amplitude I_m when M_p is on .

On the opposite side, when $V_{IN} = V_{DC}$ the gate-source voltage of the NMOS is $V_{GSn} = V_{DC}$ and the transistor M_n is turned on, while M_p is off. Consequently, $V_{SDp} = V_{DC}$ and $V_{DSn} = 0$. A current i_{M_n}, flows from the load resistance R through the series-resonant circuit, M_n and to the ground. Since the current flows on the opposite side of how the voltage is felt at R the current i is a negative half-sinusoid with amplitude I_m.

One question can be raised here. When M_n is on and M_p is off, the current flows from R to M_n, and a closed loop is created connecting both ends to the ground, no power supply is present. So how can current flow in the circuit? The reason for this to happen is the series-resonant circuit, which is an LC series filter, composed of an inductor and a capacitor. The inductor has the capacity of storing energy in its magnetic field when current is flowing, and the capacitor also has the habitability to store charge in its electrical field.

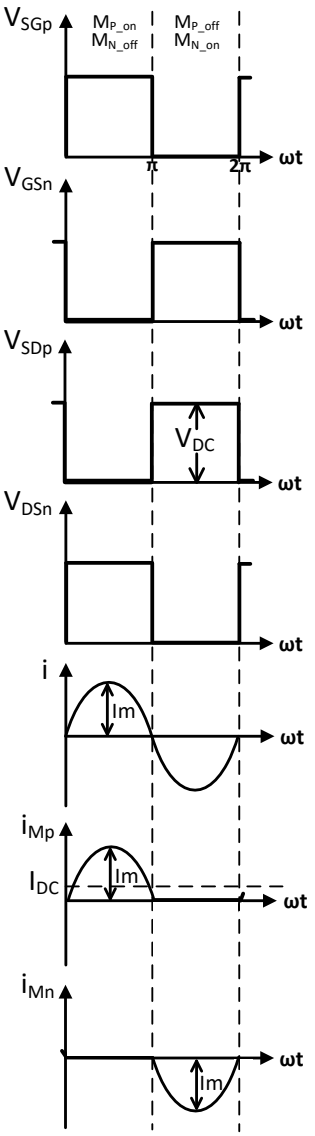


Figure 3.5: Waveforms of a CDVS PA.

When power is drained from V_{DC} to the load, current flows to the circuit and energy is stored in the inductor's magnetic field. After the switches commute, M_n is turned on and M_p is off. At this time the current i_{M_n} starts to flow from the drain to the source. Consequently, the energy stored in the inductor starts to be channelled in the direction of M_n to the ground.

As stated above the series-resonant circuit is an LC filter and has the function of filtering the fundamental frequency present in the signal V_{IN}, delivering it to the load resistance R. The filter has to be tuned for the fundamental frequency of V_{IN}. This frequency is called resonant-frequency (f_0) of the series-resonant circuit.

In figure 3.5 it is noticeable that the voltage waveforms at the transistors' terminals V_{DS} don't overlap with the current waveforms, thus, no power is dissipated. When the transistor switches from one state to the other the current at their terminal is 0, so we can say that the ZCS is achieved.

The transistors are considered to be ideal, therefore, with the switching action at their terminals a square-wave is produced with the same frequency of V_{IN}. So the input voltage at the series-resonant circuit is a square wave (v)

$$v \approx V_{DSn} = \begin{cases} V_{DC} & \text{for } 0 < wt \leq \pi, \\ 0 & \text{for } \pi < wt \leq 2\pi. \end{cases} \tag{3.7}$$

This voltage can be expressed by the trigonometric Fourier series

$$\begin{aligned} v \approx V_{DSn} &= V_{DC}\left[\frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1-(-1)^n}{2n}\sin(nwt)\right] = V_{DC}\left\{\frac{1}{2} + \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{\sin[(2k-1)wt])}{2k-1}\right\} \\ &= V_{DC}\left(\frac{1}{2} + \frac{2}{\pi}\sin(wt) + \frac{2}{3\pi}\sin(3wt) + \frac{2}{5\pi}\sin(5wt) + ...\right). \end{aligned} \tag{3.8}$$

Ideally, the even harmonics ($n = 2, 4, 6, \cdots$) in a square-wave signal are zero.

For frequencies lower than the resonant frequency f_0, the series-resonant circuit represents a high capacitive impedance. On the other hand, for frequencies higher than the resonant-frequency f_0, the series-resonant circuit represents a high inductive impedance. The series-resonant circuit acts as a bandpass filter. If the load quality factor Q_L is high enough, the voltage across the resistance R at $f = f_0$ is only the fundamental component present in (3.8),

$$v = V_m \sin(wt), \tag{3.9}$$

where its amplitude is given by,

$$V_m = \frac{2}{\pi}V_{DC}. \tag{3.10}$$

And the current through the resonant circuit at $f = f_0$ is approximately sinusoidal and equal to,

$$i = I_m \sin(wt), \tag{3.11}$$

where

$$I_m = \frac{V_m}{R_t} = \frac{2V_{DC}}{\pi R_t}. \tag{3.12}$$

At the resonant-frequency $f = f_0$, the current i_{DC} drawn from the DC power supply is equal to the current that flows through the upper transistor M_p and is given by,

$$i_1 = i_{M_p} = \begin{cases} I_m \sin(wt) & \text{for } 0 < wt \leq \pi, \\ 0 & \text{for } \pi < wt \leq 2\pi. \end{cases} \tag{3.13}$$

The DC component of the supply current is,

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i_{M_p} \mathrm{d}wt = \frac{I_m}{2\pi} \int_0^{\pi} \sin(wt) \mathrm{d}wt = \frac{I_m}{\pi} = \frac{V_m}{\pi R_t}. \tag{3.14}$$

From 3.12 and 3.14, the power requested from the DC power supply is,

$$P_{DC} = V_{DC} I_{DC} = \frac{2V_{DC}^2}{\pi^2 R_t}. \tag{3.15}$$

And, the power delivered to the output is,

$$P_O = \frac{R I_m^2}{2} = \frac{2V_{DC}^2 R}{\pi^2 R_t^2}. \tag{3.16}$$

The drain efficiency of the Class-D with ideal transistor ($r_{DS} = 0$, and with instantaneous switching time) is,

$$\eta_D = \frac{P_O}{P_{DC}} = 1. \tag{3.17}$$

Therefore, the ideal efficiency of the Class-D voltage-switching PA is 100%.

3.3.2 Non-Ideal Analysis

A more accurate analysis of the real efficiency of the Class-D PA will be presented in this section. The expressions presented here do not describe the real system, but instead provides a more realistic approach to understand which factors will degrade the efficiency of the amplifier. For the non-ideal analysis we assume that:

- The transistor has an on-resistance r_{DS} which is linear. It is assumed that the resistance of both PMOS and CMOS transistors is the same $r_{DS} = r_{DS_p} = r_{DS_n}$.
- The transistors' parasitic capacitances are considered to be linear.
- The elements of the series-resonant circuit are passive,linear, time invariant and without parasitic reactive components.
- The inductor in the series-resonant circuit has an internal resistance r_L.
- The capacitor in the series-resonant circuit has an internal resistance r_C.

- A distinction must be made between R_t and R, the first one is the circuit's total resistance,

$$R_t = r_{DS} + r_L + r_C + R. \tag{3.18}$$

R being the load resistance[6], and r_{DS} the internal resistance of the of both transistors, since each one conducts for only half the period, their equivalent resistance is given by,

$$r_{DS} = \frac{r_{DS_{Qp}} + r_{DS_{Qn}}}{2}. \tag{3.19}$$

To calculate the losses in the circuit it is desirable to know the rms value of the current that flows in each transistor, which is given by,

$$\begin{aligned} I_{Srms} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{Q_p}^2 \mathrm{d}(wt)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (I_m \sin wt)^2 \mathrm{d}(wt)} \\ &= I_m \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \frac{1}{2}(1-\cos 2wt)\mathrm{d}(wt)} = \frac{I_m}{2}. \end{aligned} \tag{3.20}$$

Since this current passes through each transistors resistance r_{DS} the conduction power loss in each MOSFET is,

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{r_{DS} I_m^2}{4}. \tag{3.21}$$

The sinusoidal current with the amplitude I_m passes through each transistor's on-resistance for the entire period $T = \frac{1}{f}$, since each transistor conducts for only half period, the total power loss on both transistors is,

$$2P_{rDS} = r_{DS} \frac{I_m^2}{2}. \tag{3.22}$$

The switching loss in a transistor is given by([p. 6][2]),

$$P_{switching} = \frac{1}{2} f C_o V_{DC}^2. \tag{3.23}$$

Where C_o[7] is the output capacitance of each transistor. Only the parasitics capacitances C_{gd} of each transistor are considered and the parasitic capacitances C_{db} aren't consider for reasons already stated in section 3.1.

[6] In our case the load is an antenna, which have a radiation resistance of 50Ω [p. 6][10].

[7] C_{ds} - drain-source capacitance [24]

Since we use two different devices, a PMOS and an NMOS, and it is desirable for them to have the same internal resistance, their size will be different as a consequence of the characteristics of the technology. This leads to a different output capacitance for both devices. We make this distinction by calling them Co_n and Co_p. As such the switching loss in each transistor is,

$$P_{swMn} = \frac{1}{2} f Co_n V_{DC}^2, \tag{3.24}$$

$$P_{swMp} = \frac{1}{2} f Co_p V_{DC}^2. \tag{3.25}$$

The total switching power loss can be expressed as,

$$P_{swMnMp} = P_{swMn} + P_{swMp} = \frac{1}{2} f Co_n V_{DC}^2 + \frac{1}{2} f Co_p V_{DC}^2$$

$$P_{swMnMp} = \frac{1}{2} f (Co_n + Co_p) V_{DC}^2. \tag{3.26}$$

Then the total power loss in both transistors is,

$$P_{Trans_{Loss}} = 2P_{rDS} + P_{sw} = \frac{I_m^2}{2} \left(r_{DS} + \frac{1}{2} f (Co_n + Co_p) V_{DC}^2 \right). \tag{3.27}$$

The drain efficiency can be expressed as ,

$$\eta_D = \frac{P_O}{P_O + 2P_{rDS} + P_{sw}} = \frac{R}{R + r_{DS} + \frac{1}{2} f (Co_n + Co_p) V_{DC}^2}. \tag{3.28}$$

The power loss in the series-resonant circuit is given by,

$$P_{rLrC} = (r_L + r_C) \frac{I_m^2}{2}. \tag{3.29}$$

Then the overall efficiency of the circuit is,

$$\eta = \frac{P_O}{P_{DC}} = \frac{P_O}{P_O + 2P_{rDS} + P_{rLrC} + P_{sw}} = \frac{R}{R + r_{DS} + r_L + r_C + \frac{1}{2} f (Co_n + Co_p) V_{DC}^2}. \tag{3.30}$$

The non-ideal components will degrade the drain and overall efficiency, the frequency of the signal V_{IN} has a major contribution in this degradation due to the switching loss. Therefore, it is not possible to achieve the ideal efficiency of 100%.

3.3.3 Gate Driver

The gate-to-source and the gate-to-drain capacitances of the CDVS are quite big, therefore, they need to be driven. This means that a gate driver is needed to provide enough current

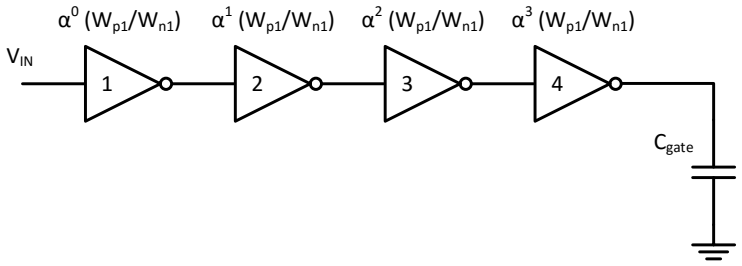


Figure 3.6: Cascade of inverters used to drive a big capacitance.

to charge the gate capacitances of the amplifier, to grantee a minimum delay response from the Class-D PA. For this to be achieved a string of inverters(buffers) is added between the V_{IN} signal and the amplifier gate shown in figure 3.6.

The cascade is composed by N inverters, each inverter is larger than the previous one by a factor of α, by larger means that only the gate width will change in size. A minimum delay can be obtained as long as α and N are picked correctly. Each inverter's input capacitance is larger than the previous inverter's input capacitance by a factor of α. The scale factor that will be used in the chapter 4.2 is $\alpha = 3$. This scale factor is used to minimize propagation delay, as it is done in digital CMOS design for output buffers [p. 64][25].

3.4 Series-Resonant Circuit

At the output of the PA a square-wave is produced. This signal contains a DC component, the fundamental frequency and the respective harmonics. A bandpass filter is used to filter only the fundamental frequency and reject the DC and all of the high frequency harmonics. The main features of bandpass filters will be reviewed here.

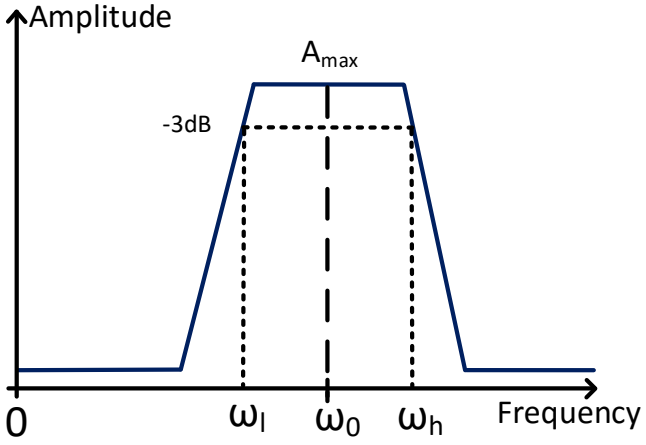


Figure 3.7: Bandpass filter frequency response.

Figure 3.7 shows the frequency response of a bandpass filter, where ω_0 is the fundamental frequency. The frequencies ω_l and ω_h are the frequencies for which the amplitude response of the filter drops $3dB$ relatively to the maximum amplitude(A_{max}). The bandwidth of the filter is given by,

$$BW = \omega_h - \omega_l. \tag{3.31}$$

The quality factor(Q) of bandpass filter measures the filter performance. It measures selectivity of the filter, which means the bigger the quality factor the smaller is the bandwidth. The quality factor is given by,

$$Q = \frac{\omega_0}{BW}. \tag{3.32}$$

Butterworth Bandpass Filter

A bandpass Butterworth filter will be implemented since it uses reactive components, which can be made on-ship. Figure 3.8 shows the schematic of a Butterworth bandpass filter. It uses the minimum capacitor topology, where the filter is connected to the source via the series resonant arm instead of the minimum inductor topology, where parallel resonant shunt arm is connected to the source. The series resonant arm is connected to the

source, that allows the blockage of the DC component of the square-wave presented at the input of the filter.

The order of the Butterworth bandpass filter depends on the number of resonant arms, figure 3.8 shows 5 resonant arms. Hence, it is a 5th order bandpass filter. In the minimum capacitor topology the source is connected to a series resonant arm if the resonant arm is connected directly to the load, it will be a 1st order bandpass filter. If a 2nd or higher order filter is desired, the series resonant arm has to be followed by a parallel resonant arm and vice versa. For each resonant arm used, the order of the bandpass filter is increased by one.

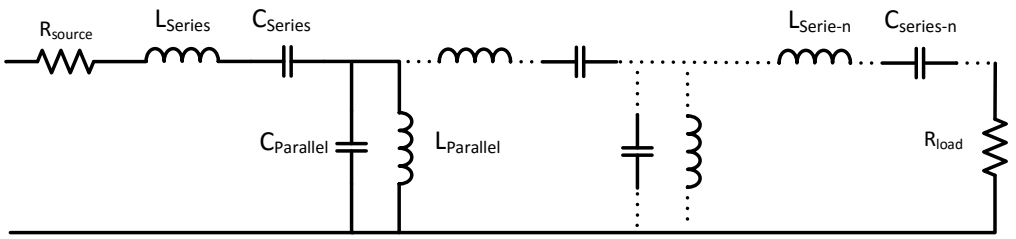


Figure 3.8: Butterworth Bandpass filter circuit.

The bandpass filter can be designed with a lowpass to bandpass transformation, which requires the design of a lowpass filter. In order to avoid this, a much faster way to design the bandpass filter can de used. The expressions to calculate the components in each resonant arm are given by,

$$C_{Series} = \frac{\omega_h - \omega_l}{2\pi\omega_h\omega_l RX}, \tag{3.33}$$

$$L_{Series} = \frac{RX}{2\pi(\omega_h - \omega_l)}, \tag{3.34}$$

$$C_{Parallel} = \frac{X}{2\pi(\omega_h - \omega_l)R}, \tag{3.35}$$

$$L_{Parallel} = \frac{R(\omega_h - \omega_l)}{2\pi\omega_h\omega_l X}. \tag{3.36}$$

Where X is the normalized element value from the tables A.1 or A.2 that are shown in the appendix A. The same value of X must be used for both elements in the same resonant arm. If the load and source resistance are the same ($R = R_{Source} = R_{Load}$) the values for X are taken from the table A.1. In the class-D amplifier R_{Source} will be the resistance of transistor. Hence, $R_{Source} < R_{Load} = R$ and the values of X are taken from the table A.2. After the order of the filter is chosen, the component for each resonant arm can be calculated using the equations (3.33),(3.34),(3.35) and (3.36).

3.5 Sigma-Delta Modulation

The purpose of the $\sum\Delta$ modulator is to encode the source signal into a binary level train pulse shown in figure 3.9. This train pulse will drive the RF class-D amplifier. $\sum\Delta$ modulators are classified into discrete-time(DT) and continuous-time(CT) model designs, the difference between them resides on the noise shaping filter. DT designs are better at low frequencies and are commonly implemented with switched capacitor techniques[26], which are difficult to implement at RF frequencies. Therefore, DT designs are converted to an equivalent CT model. In the CT design the noise shaping filters are usually implemented with passive high Q resonators, which can be integrated into IC design [27].

A digital direct conversion transmitter using a bandpass 1-bit $\sum\Delta$ modulator with D/A conversion and a possible integration with a RF class-D amplifier is presented in [15]. A $\sum\Delta$ modulator coupled with a class-D amplifiers for digital pulse modulation transmitters is presented in [28]. A RF class-D amplifier with a 1-bit bandpass $\sum\Delta$ modulator including the modulation of time varying envelope signals is presented in [29]. In this chapter a first order $\sum\Delta$ is presented to understand how the modulator converts the analog signal into a train pulse.

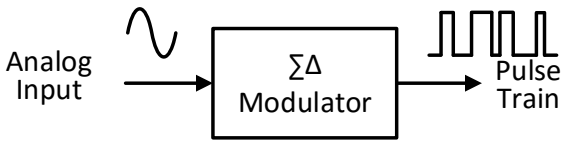


Figure 3.9: $\sum\Delta$ Modulator.

3.5.1 Noise Shaping due to Oversampling

When an ideal converter digitalizes a signal, the maximum output error is $\pm\frac{1}{2}V_{lsb}$ [8] since an ADC converter (figure 3.10) is used. As an example, V_{lsb} is the minimum voltage step that will make a change in the least significant bit of the converter. When the quantization process occurs, the signal is degraded due to quantization error (q_e). The value q_e can be seen as the difference between the input signal amplitude and the closest amplitude level of the quantizer. The quantization error is equally probable to occur at any point within the range of $\pm\frac{1}{2}V_{lsb}$. Considering that the input signal is random and that it changes rapidly, and if the quantization steps are large enough, the quantization error can be considered white noise.

In a N-bit quantizer, the minimum input voltage (V_{lsb}) that results in a change of the least significant bit is given by,

$$V_{lsb} = \frac{F_{scale}}{2^N}. \tag{3.37}$$

[8] lsb-least significant bit

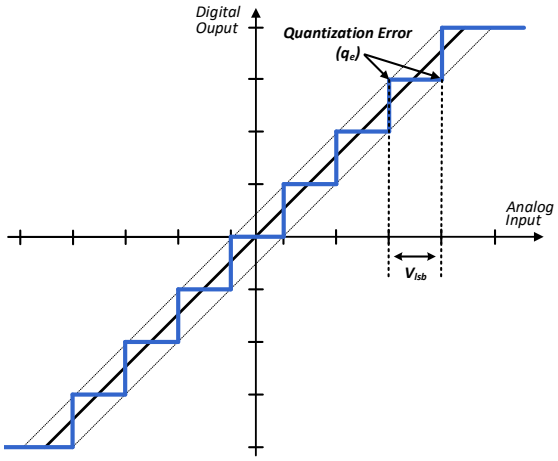


Figure 3.10: Ideal n-bit ADC quantization error e_n.

Where F_{scale}[9] is the full-scale output range of the N-bit quantizer. Since quantization can be viewed as white noise, the quantization error(q_e) shows a uniform probability density function(PDF) between $\pm\frac{1}{2}V_{lsb}$ [p. 25][30]. The quantization noise power is given by,

$$q_{e,rms}^2 = \frac{1}{V_{lsb}} \int_{-V_{lsb}/2}^{+V_{lsb}/2} q_e^2 \cdot \mathrm{d}q_e = \frac{V_{lsb}^2}{12}. \tag{3.38}$$

The input signal has to be sampled in order to be quantified. According to the Nyquist theorem, the minimum frequency f_s required to sample a signal without loss of information is twice the signal bandwidth as in the following equation,

$$f_s \geq f_N = 2 \cdot BW \tag{3.39}$$

where f_N is the Nyquist frequency.

The quantization power will be uniformly distributed in the band between $\pm\frac{1}{2}f_s$, since the quantized signal is sampled at the rate of f_s. Hence, the quantization error will exhibit a constant Power Spectral Density (PSD) in that frequency interval and is given by,

$$Sq_{e,rms}^2 = \frac{q_{e,rms}^2}{f_s} = \frac{V_{lsb}^2}{12f_s}. \tag{3.40}$$

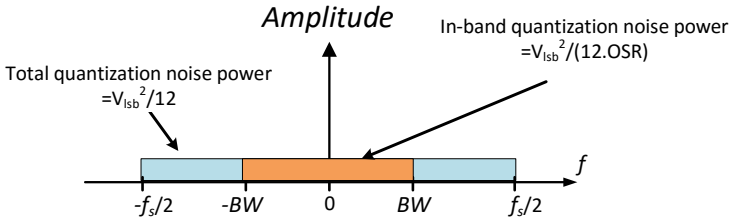


Figure 3.11: Frequency Spectrum of a input signal S_{in} and quantization noise.

[9]This value can be commonly refereed as V_{ref}.

Oversampling

Oversampling is a technique that samples the signal at a higher frequency than the Nyquist frequency(f_N) in order to avoid the aliasing effect. The sampling ratio of a signal at a frequency bigger than f_s is called the oversampled ratio and is given by,

$$OSR = \frac{f_s}{2 \cdot BW}. \tag{3.41}$$

When a signal is oversampled and quantized, the quantization noise is uniformly distributed in the band between $[-\frac{f_s}{2}, \frac{f_s}{2}]$. Only a fraction of the total power stays in the signal band $[-BW, +BW]$ as shown in figure 3.11. Using the oversample ratio(4.10) in the equation 3.40, the quantization noise present in the signal band is given by,

$$P_{sband} = \int_{-BW}^{+BW} Sq_{e,rms}^2 \cdot \mathrm{d}f = \int_{-BW}^{+BW} \frac{V_{lsb}^2}{12 f_s} \cdot \mathrm{d}f = \frac{V_{lsb}^2}{12 \cdot OSR}. \tag{3.42}$$

Considering an input signal V_{in}, which is a sinusoid with amplitude V_{ref}, which is the maximum value that the N-bit converter can accept. With the power spectral density of the quantization noise the signal-to-noise ratio(SNR) can be calculated as,

$$\begin{aligned} SNR &= 20 \cdot log\left(\frac{V_{in}^2}{Psband^2}\right) \\ &= 20 \cdot log\left(\frac{V_{ref} \cdot \sqrt{12}}{2\sqrt{2} \cdot V_{lsb}} \cdot \sqrt{OSR}\right) \\ &\approx 6.02 \cdot N + 1.76 + 10 \cdot log(OSR). \end{aligned} \tag{3.43}$$

3.5.2 First order Sigma-Delta

A first order Continuous Time $\sum\Delta$ modulator is presented in figure 3.12. The analysis of quantization noise and oversampling mentioned above will be used to show how the modulator shapes the quantization noise. The 1-bit ADC of the circuit can be represented as a sum of the signal received from the integrator(H(s)) and the quantization noise (q_e) inherent of the ADC. The feedback loop forces the average value of the quantized output to track the average input. Any difference between these signal is accumulated in the integrator and the feedback loop will be corrected by itself.

The transfer function of the integrator is given by,

$$H(s) = \frac{1}{s}. \tag{3.44}$$

The $\sum\Delta$ modulator exhibits two different transfer functions, the noise transfer function (NTF) from the quantization error signal, and the signal transfer function (STF) which are given by,

$$STF(s) = \frac{H(s)}{1+H(s)} = \frac{1}{s+1}. \tag{3.45}$$

$$NTF(s) = \frac{1}{1+H(s)} = \frac{s}{s+1}. \tag{3.46}$$

In the S domain the $\sum\Delta$ modulator can be represented as,

$$Y(s) = STF(s) \cdot X(s) + NTF(s) \cdot q_e(s). \tag{3.47}$$

The SNR for a 1st order $\sum\Delta$ modulator is given by,

$$SNR = 6.02 \cdot N + 1.76 + 30 \cdot log(OSR) - 5.17. \tag{3.48}$$

When the OSR ratio is doubled, the SNR has a 9 dB improvement[p. 85][31]. High order $\sum\Delta$ modulators have higher SNR for the same OSR. Their implementation can be more difficult and for higher order modulators the stability problems can be developed.

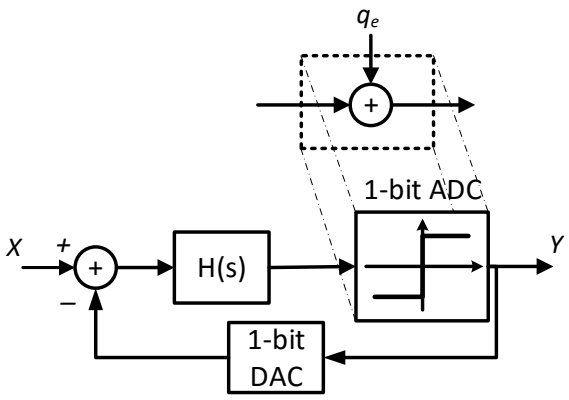


Figure 3.12: First order ADC $\sum\Delta$ modulator.

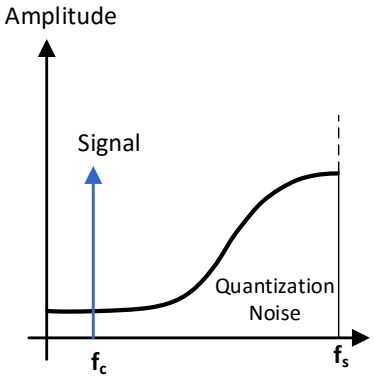


Figure 3.13: Signal and Noise Spectrum

The $\sum\Delta$ has noise shaping attributes, that are shown in figure 3.13. Where f_c is the frequency of the input signal and f_s is the frequency at which the signal is sampled. By increasing f_s the oversampling ratio increases and the quantization noise is shifted to higher frequencies, that can be easily filtered with a low pass filter.

CHAPTER 4

DESIGN AND SIMULATION OF THE PROPOSED RF CLASS-D POWER AMPLIFIER

In this chapter the RF CDVS PA is designed. Using the non-ideal analysis a high-level model of the amplifier is implemented. In the simulator the high-level model is used as a baseline to design the circuit of the RF Class-D amplifier, a driver is introduced which is used to drive the high capacitances felt at the input of the amplifier. Results are obtained and compared between the high-level model and the simulation model. At last an ideal 1st order $\sum\Delta$ modulator is used to drive the RF CDVS PA.

4.1 Class-D PA High-Level Model

In this section the equations from section 3.3 are used to create a high-level model of the RF CDVS PA shown in Fig. 4.1, this model is used to predict the output power total power loss and the overall efficiency of the Class-D amplifier.

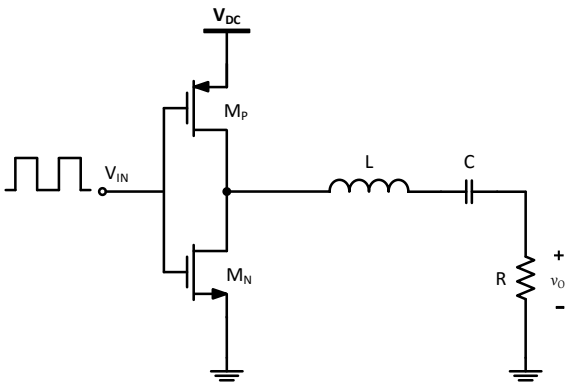


Figure 4.1: High-level model circuit of the RF CDVS PA.

First, the output power is calculated considering the ideal analysis, where all DC

power is transferred to RF power. To calculate the output power the equation 3.16 is used. Since the ideal analysis is considered, the total resistance of the circuit is equal to the load resistance $R_t = R = 50\ \Omega$. The following voltage value for the DC source was used $V_{DC} = 1.2\ V$. Therefore, the output power is given by,

$$P_O = \frac{2V_{DC}^2}{\pi^2 R_t} = \frac{2 \cdot 1.2^2}{\pi^2 \cdot 50} = 5.83\, mW, \tag{4.1}$$

the conversion from watts to dBm is made,

$$10 \cdot log_{10}(\frac{P(mW)}{1mW}) = 10 \cdot log_{10}(\frac{5.83mW}{1mW}) = 7.66\ dBm. \tag{4.2}$$

This is the maximum output power that can be achieved in ideal conditions. From the expression can be seen that the voltage V_{DC} is the major player in therms of power output, since it is the only variable that can be changed. Next step is to analyse the output power considering the non-ideal case.

To design the high-level model of RF CDVS PA the equations from the chapter 3.3.2 are considered. For the calculations we consider two typical transistors a NMOS and a PMOS, which are made with in 130 nm technology, their parameters are given in the table 4.1. Where K_P and K_N represent the intrinsic transconductance of the transistors.

Table 4.1: Transistors Parameters.

V_{DC}	f	K_n	K_p	V_{tn}	V_{tp}	$L_{n/p}$	C_{ox}
$1.2V$	$2.4GHz$	$500\mu AV^-2$	$100\mu AV^-2$	$0.38V$	$0.33V$	$130nm$	$12.3\frac{fF}{\mu m}$

For the power output to be calculated, the series resonant circuit has to be designed first, since its internal resistance will degrade the power delivered to the load. The resonant frequency is given by the following expression,

$$\omega_o = \frac{1}{\sqrt{LC}}. \tag{4.3}$$

Table 4.2: Series-resonant circuit parameters.

L	C	Q_{L0}	Q_{C0}
$13nH$	$340fF$	10	50

From the previous expression the values of L e C were calculated for a frequency of 2.4 GHz, their values are shown in the table 4.2. The quality factors of the inductor and the capacitor, Q_{L0} and Q_{C0}, are typical values of integrated reactive components.

In [p. 78][32] it was said that spiral integrated inductors in silicon substrate have typical Q_L of 10, that is due to losses at high frequencies ($1GHz$ to $5GHz$). Although in

[33] it was reported an Q_L of 40 for an inductor of $20nH$ working at $3.5GHz$ due to layout optimization. We assume the lowest value of quality factor since we will not perform any layout optimization for the integrated inductors.

Integrated capacitors such as Metal-Insulator-Metal (MIM) are reported in [p. 134][34] to have Q_C of 20 at $20GHz$, the value Q_C is higher for lower frequencies. In [p. 142][35] it was said that a MIM capacitors can have a quality factor from 50 to 150. Therefore, we chose a value of $Q_C = 50$, which is reasonable value for $2.4GHz$. Hence, the resistance of the series resonant circuit is now calculated as,

$$r_L = \omega_0 \frac{L}{Q_{L0}} = 19.6\Omega, \tag{4.4}$$

$$r_C = \frac{1}{\omega_0 C Q_{C0}} = 3.9\Omega. \tag{4.5}$$

Next step is to define the transistor's size[1]. Both transistors work as switches and their size will only define their internal resistance, shown in equation 3.4. It is desired that both transistors have the same internal resistance. For this to be achieved the PMOS will have a bigger width than the NMOS, this is due to the internal characteristics of the PMOS transistor. The width of the PMOS transistor is calculated prior to the width of the NMOS, due to the fact that the PMOS transistor will have bigger area. The output power will be influenced by the internal resistance of each transistor as it is shown,

$$\begin{aligned} P_O &= \frac{2 \cdot V_{DC}^2 \cdot R}{\pi^2 \cdot R_t^2} = \frac{2 \cdot V_{DC}^2 \cdot R}{\pi^2 (R + r_L + r_C + r_{DS})^2}, \\ &= \frac{2 \cdot V_{DC}^2 \cdot R}{\pi^2 (R + r_L + r_C + \frac{1}{K_n \frac{W}{L}(V_{gs} - V_{tn})})^2}. \end{aligned} \tag{4.6}$$

The previous expression(4.6) is used to calculate the output power as a function of the width from the PMOS and NMOS transistors, as shown in figures 4.2 and 4.3. The output power is in dBm. The chosen width for the PMOS and NMOS is $0.5mm$ and $0.106mm$, corresponding to a power output of $3.97dBm$. Figures 4.2 and 4.3 show that after the chosen value of width there is no change in the power output, that is due to the internal resistance of the transistor which is already very small. After this point, increasing the width will no longer have any impact on the resistance r_{DS}.

The width of PMOS and NMOS is established, using of the equation 3.4 the resistance of both transistors is calculated. These results are shown in the table 4.3.

Table 4.3: Internal resistance and width of the PMOS and NMOS.

$r_{ds_{PMOS}}$	$r_{ds_{NMOS}}$	W_{PMOS}	W_{NMOS}
2.98Ω	2.98Ω	$0.5mm$	$0.106mm$

[1]The size of the transistor in this case is only influenced by its width since the minimum length is used(130nm).

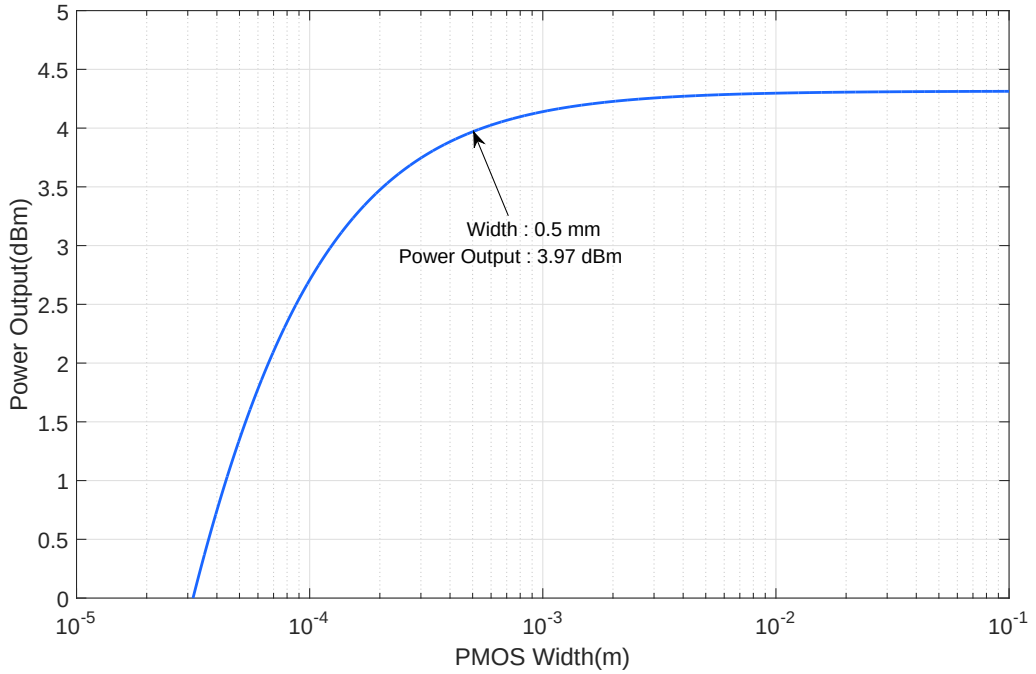


Figure 4.2: Power output in function of PMOS width(equation 4.6).

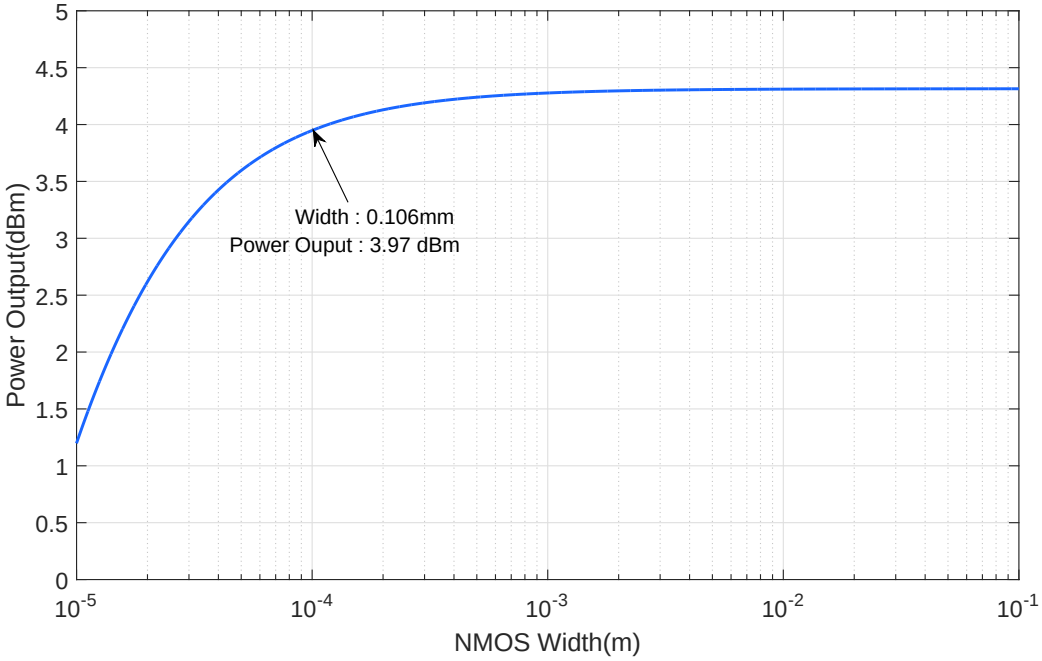


Figure 4.3: Power output in function of NMOS width (equation 4.6).

The switching power loss can be calculated by the equation 3.26, using the values presented in the table 4.1 the output capacitance Co_n and Co_p are given by,

$$Co_n = C_{gd,n} = \frac{1}{2} C_{ox} W_n L = 84.747fF, \tag{4.7}$$

$$Co_p = C_{gd,p} = \frac{1}{2} C_{ox} W_p L = 399.75fF. \tag{4.8}$$

Hence the switching power loss is given by,

$$P_{swMnMp} = \frac{1}{2} f(Co_n + Co_p) V_{DC}^2 = 0.837mW. \tag{4.9}$$

In table 4.4 the results of the high-level model are shown, using the equations from the non-ideal analysis. The results obtained are the voltage and current peaks of the output signal, the DC power consumption, output power, switching power loss and the drain and overall efficiency. The overall efficiency is less than the ideal value of 100%.

Figure 4.4 shows how the overall efficiency varies with the width of the PMOS transistor which is given by the equation 3.30.The equation shows that there are two capacitances that depend on both transistor's sizes, hence, two variables are needed. For equation to depend on one variable only the solution found is to set the width of the NMOS transistor so it has the same internal resistance of the PMOS transistor. This width ratio is given by $\frac{W_p}{W_n}$.

Figure 4.4 shows that the efficiency doesn't degrade with the increasing width of both transistors. This is due to the parasitic capacitances having values in the order of the femto farad. Therefore, the switching power loss doesn't increase above the power saved by lowering the internal resistance of both transistors with the increase width of both transistors. This is the advantage of using a nano-scale technology.

Table 4.4: High-level model RF CDVS PA design results.

Reference	Expression	Value
3.18	$R_t = r_{DS} + r_L + r_C + R.$	76.48 Ω
3.10	$V_m = \frac{2}{\pi} V_{DC}$	0.76 V
3.12	$I_m = \frac{2V_{DC}}{\pi R_t}$	10 mA
3.15	$P_{DC} = \frac{2V_{DC}^2}{\pi^2 R_t}$	3.82 mW
3.16	$P_O = \frac{2V_{DC}^2 R}{\pi^2 R_t^2}$	2.5 mW (3.97 dBm)
3.26	$P_{swMnMp} = \frac{1}{2} f(Co_n + Co_p) V_{DC}^2$	0.837mW
3.28	$\eta_D = \frac{R}{R + r_{DS} + \frac{1}{2} f(Co_n + Co_p) V_{DC}^2}$	92.9%
3.30	$\eta = \frac{R}{R + r_{DS} + r_L + r_C + \frac{1}{2} f(Co_n + Co_p) V_{DC}^2}$	65.4%

Next step is to use the simulator to verify these results. It is expected that the simulator results will be worse since it makes more realistic approach than this model.

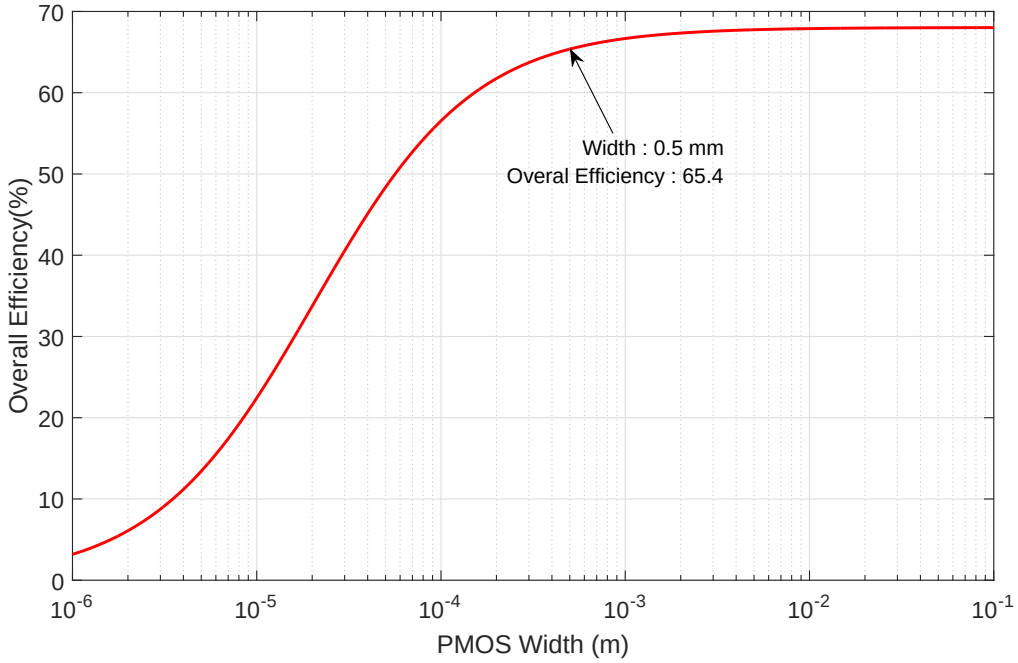


Figure 4.4: Overall efficiency in function of the PMOS width(equation 3.30).

4.2 Pre-Layout Simulation Model

In this section the design of the RF CDVS PA is presented using the high-level model as an approach model. To validate the design the simulator CADENCE VIRTUOSO is used. Figure 4.5 shows the designed circuit. The circuit is composed of a driver stage, a Class-D amplifier and the series-resonant circuit, which is a 3rd order Butterworth bandpass filter. The bandpass filter is designed with ideal and pre-layout components, which have a behaviour similar to integrated components.

All transistors and pre-layout components are designed in 130nm CMOS process. In the simulator the circuit simulation uses the BSIM3V3 device model. The transistors used in the design are from library UMC 0.13μm L130E RFCMOS and are the following,

- 1.2V PMOS RF model.
- 1.2V NMOS PWell RF model.

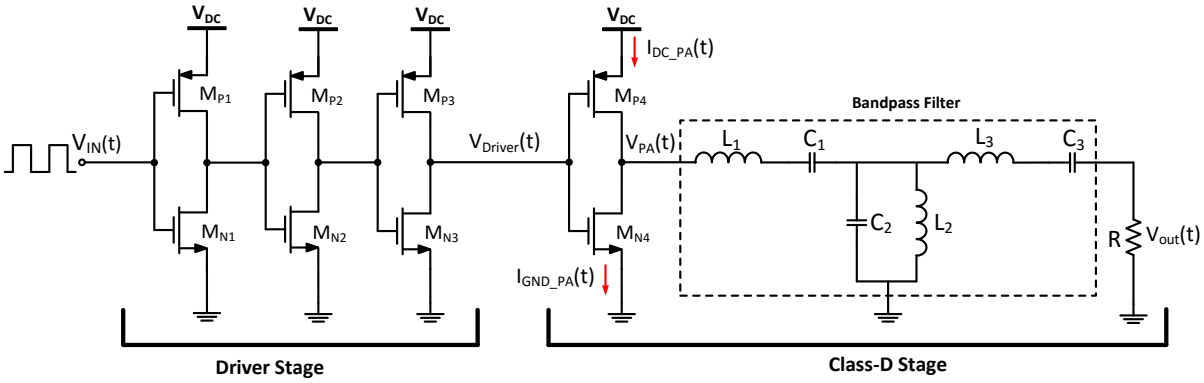


Figure 4.5: Schematic of the CMOS driver and CDVS PA circuits.

In the figure 4.5 a driver stage is presented. The driver is made of 3 inverters of decreasing gate width, this decreasing is made from the Class-D inverter as it is shown in table 4.5, where the PMOS and the NMOS transistors are scaled down relatively to the PMOS and the NMOS transistors of the preceding inverter. This decrease in the gate width of the inverters is made by a factor of $\alpha = 3$ relatively to the preceding stage as mentioned in the section 3.3.3. Since each inverter changes the input signal in 180 degrees an odd number of inverters were chosen for the driver so that the output of the PA has the same phase as the signal V_{IN}.

The transistors' size of the Class-D inverter is shown in the table 4.5 in the last row. The NMOS transistor width is bigger compared to the high-level model, this is due to the fact that it is desired for both transistors to have the same internal resistance. A DC simulation was performed to measure the resistance of both transistors. Their value was different, it is more advantageous to increase the size of the NMOS until it matches the internal resistance of the PMOS. The internal resistance of both transistors is 3.5 Ω.

Table 4.5: Transistor width of the inverters' stages.

Stage	PMOS width(μm)	NMOS width(μm)	
1	18.5	4.4	Driver Stage
2	55.5	13.3	
3	166.7	40	
4	500	120	Class-D Stage

Table 4.6 shows the values of each component of the 3rd order Butterworth bandpass filter with a center frequency $f_c = 2.4GHz$ and with bandwidth of $BW = 800MHz$. The particular order of the filter was chosen in order to maintain the inductor's size at low values. The major problems of integrated inductor are the area cost and the high resistance at high resonant frequencies, which lead to power loss. A 2nd and 4th order Butterworth bandpass filters were tested. The 2nd order filter showed problems in filtering the desired frequency, the output signal showed some distortion. When using pre-layout components the 4th order filter dissipates most of the power present in the circuit. Therefore, the 3rd order filter is considered to be the most suitable.

Table 4.6: 3rd order Butterworth bandpass filter values.

Inductors		Capactiors	
L_1	10nH	C_1	440fF
L_2	803pH	C_2	5.428pF
L_3	2.09nH	C_3	2.1pF

Figure 4.6 shows the waveforms of the circuit presented in figure 4.5, respective signals are marked on the circuit. The signal V_{IN} is a perfect square-wave with instant rise and fall time with a frequency of 2.4 GHz. The driver output signal is V_{Driver} which is no longer a perfect square-wave. The charge and discharge of the gate capacitance in each stage causes a delay in the signal, both rise and fall time, are no longer instantaneous. This rise and fall causes a short circuit between V_{DC} and the ground leading to power loss. This is due to both transistors being in saturation leading to the short circuit between the DC source and the ground this effect is described in section 3.2. This effect is present in every stage of the driver and the Class-D amplifier.

In figure 4.6 the time when both transistors are on can be seen in the current waveforms drain from the DC source $I_{DC_{PA}}$ to the amplifier stage, and the current that is sent to the ground $I_{GND_{PA}}$ through amplifier. During the rise-time of V_{Driver} at 5.25 ns marked with a A (figure 4.6), a current peak is felt in both $I_{DC_{PA}}$ and $I_{GND_{PA}}$ this means that current is sent directly from the DC source to the ground. At 5.5 ns marked with a B (figure 4.6) during the fall-time of V_{Driver} the same effect can be seen.

The voltage at the output of the PA stage V_{PA} is a square-wave as predicted in the high-level model, the same occurs for the sinusoidal waveform at the output V_{out}.

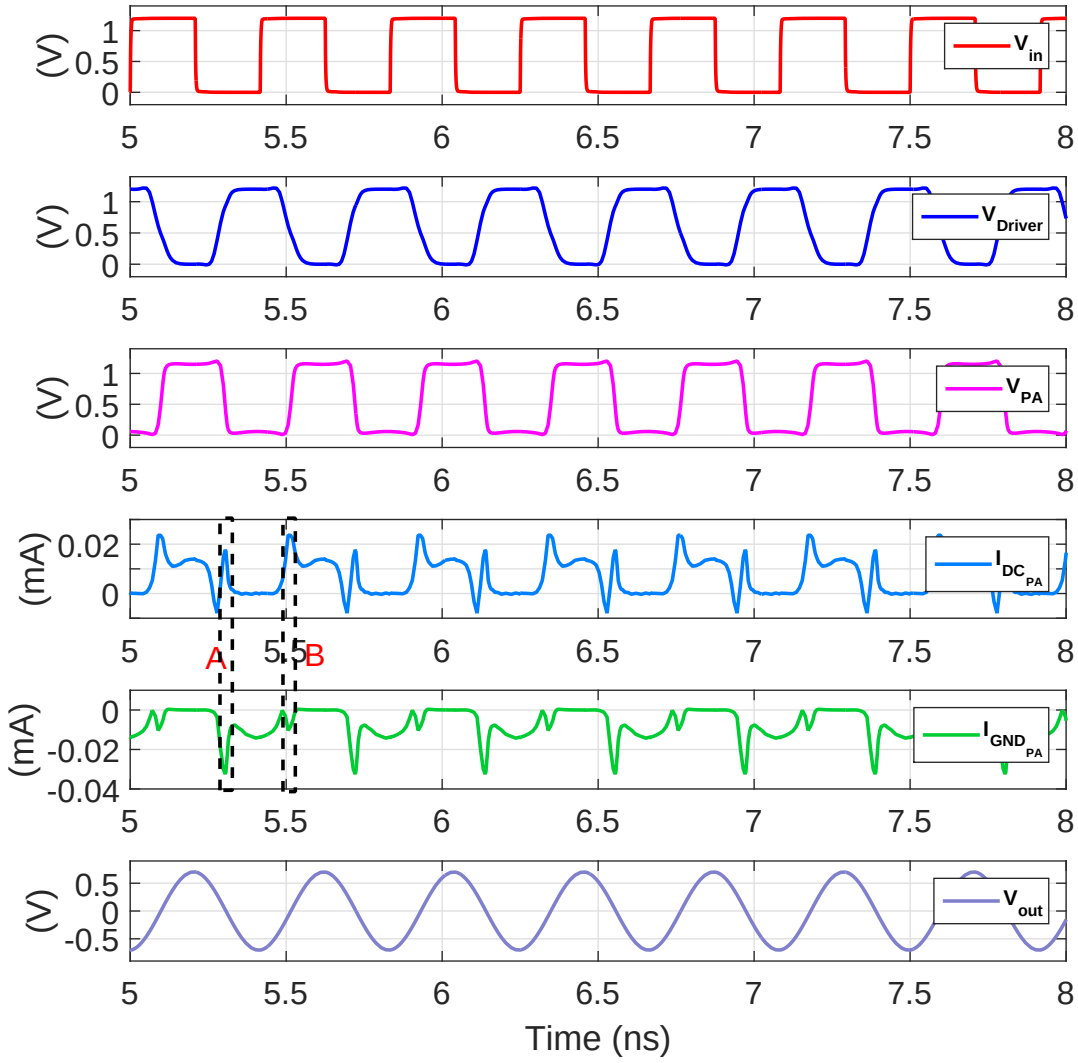


Figure 4.6: RF CDVS PA circuit waveforms.

Table 4.7 shows the results obtained by using the ideal analysis, high-level model and the simulations model which uses a filter with ideal and pre-layout components. In the first two cases the power consumption of the driver is not calculated since the main purpose is to study the RF Class-D PA.

In the ideal analysis the power consumption is bigger than in the high-level model due to the lower internal resistance of the circuit therefore more power is drawn form the DC source. In the ideal analysis the efficiency reaches 100% meaning that all power is transferred from the DC source to the load. Since all components have internal resistance in the high-level model, the DC power consumption is less than in the ideal analysis. Also the internal resistance of the filter degrades the output power delivered to the load, therefore, the efficiency is lowered reaching 65%.

In the simulation model which uses a 3rd order Butterworth bandpass filter with ideal

and pre-layout components it is shown that the DC power consumption of the PA is three times larger than the value predicted in the high-level model. The more accurate switching power losses due to parasitic capacitances and the short circuit between the DC source and the ground are responsible for such high consumption. The power consumption of both drivers and amplifiers stages are similar, that is due to the fact that each driver has three inverter, all suffering from the same power losses mechanism as the inverter of the amplifier stage.

Table 4.7: RF CDVS PA results considering ideal analysis, high-level model and the simulation model using a filter with ideal and pre-layout components.

	Ideal analysis	High-level model non-ideal analysis	Filter with ideal components	Filter with pre-layout components
PA Power Consumption	5.83 mW	3.82 mW	12.38 mW	12.30 mW
Driver Power Consumption	–	–	9.371 mW	9.382 mW
Pout (dBm)	7.66 dBm (5.83mW)	3.97 dBm (2.5mW)	6.91 dBm (4.91mW)	0.317 dBm (1.07 mW)
THD	–	–	0.251%	0.231%
PAE	–	–	36.0%	12.7%
Drain Efficiency	100%	94%	40%	8.6%
Overall Efficiency	100%	65%	23%	4.9%

In the simulation model the output power which uses a 3rd order filter with ideal components is almost the same as in the ideal case where it is the maximum output power that can be achieved in ideal conditions. This difference comes from the internal resistance in each transistor which is taken into account in the simulation model ($3.5\Omega > 2.98\Omega$). Also the output power is much higher comparing with the high-level model, since, the latter one considers a filter with non-ideal components which have resistive part. Therefore, the power is lost in the filter and the output power is lowered.

In the simulation model which uses a 3rd order filter with pre-layout components the output power is almost four times lower compared with the filter which uses ideal components (see Figures 4.7 and 4.8), where the output power spectrum is shown for each filter. The inductors present in the filter are the main cause for power loss, and also responsible for the low Total Harmonic Distortion (THD) which leads to a low distortion in the output signal. The low distortion means that the harmonics present in the signal are being rejected by the filter as shown in figures 4.7 and 4.8, where only the fundamental frequency has considerable power. The THD remains the same in both analyses due to the quality of the filter which was not changed.

The PAE, drain and overall efficiency are greatly degraded by the filter when using pre layout components. This is due to the power loss in the filter leading to less power

delivered to the load. This result shows that in reality there is a trade-off between power output and quality of the filtered signal.

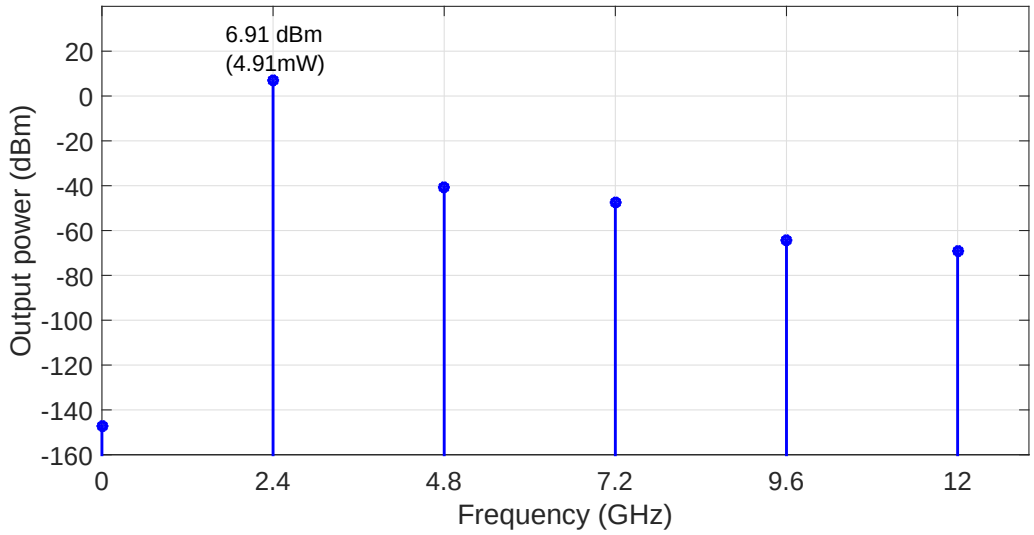


Figure 4.7: Output power spectrum using a filter with ideal components.

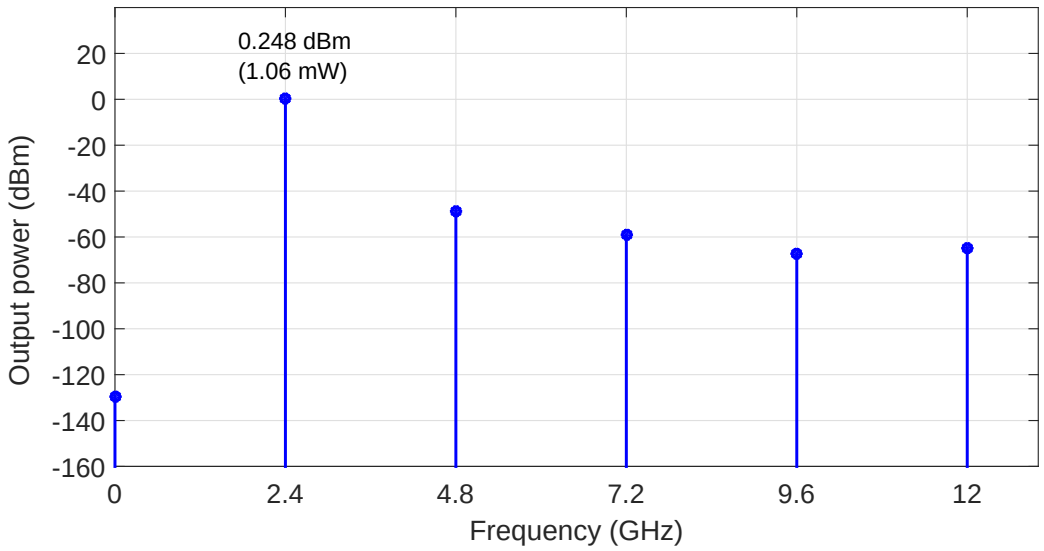


Figure 4.8: Output power spectrum using a filter with pre-layout components.

4.3 RF Class-D PA With Sigma-Delta Modulator

In this section an ideal 1st order $\sum\Delta$ modulator is chosen to drive the RF CDVS PA, the circuit is shown in the figure 4.9. The ideal 1st order $\sum\Delta$ modulator is implemented by using hardware description language (VerilogA) and the code can be found in the appendix B. The Level Shifter block is responsible for converting the output of the $\sum\Delta$ modulator [-1,1] to [0,1.2], this block is also ideal and implemented in VerilogA which can be found in appendix C.

Figure 4.10 shows the waveforms of the circuit of the figure 4.9. The signal V_{IN} is a sine wave with a frequency of 2.4 GHz, the clock signal V_{CLK} has a frequency of the 8.2 GHz which leads to the following oversampling ratio,

$$OSR = \frac{8.2GHz}{2 \times 2.4GHz} = 1.7. \tag{4.10}$$

The output signal of the $\sum\Delta$ modulator is a square-wave with a varying duty-cycle. The signal at the output of the Class-D stage V_{PA} preserves the duty-cycle imposed by the $\sum\Delta$ modulator, with some delay which was introduced by the driver stage. The output signal V_{Vout} is a sine-wave with varying amplitude. This effect is due to the changing duty-cycle of the $\sum\Delta$ modulator. The output signal is at the same frequency as the input signal as it is desired.

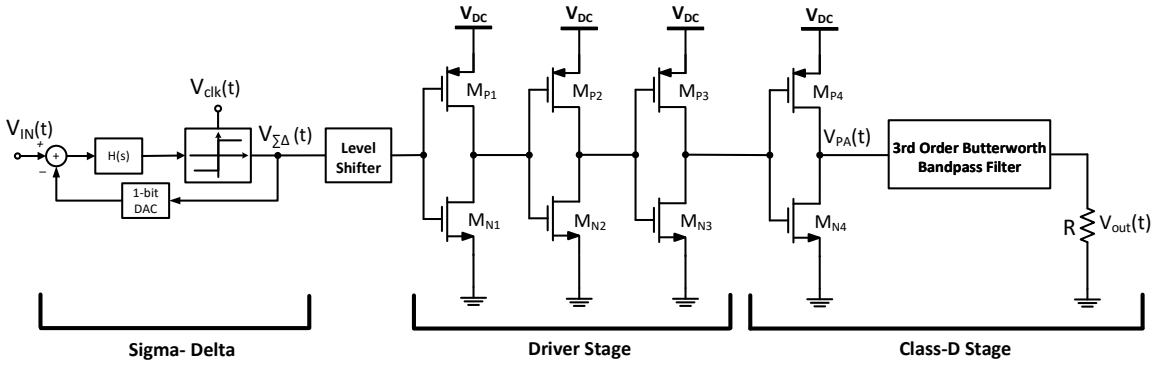


Figure 4.9: $\sum\Delta$ modulator with the RF CDVS PA circuit.

As stated before the non-linear amplifier don't preserve the envelope variations of the input signal, and the obtained results show that. If the input signal would be modulated using frequency modulation or phase modulation the output signal would preserve such modulation.

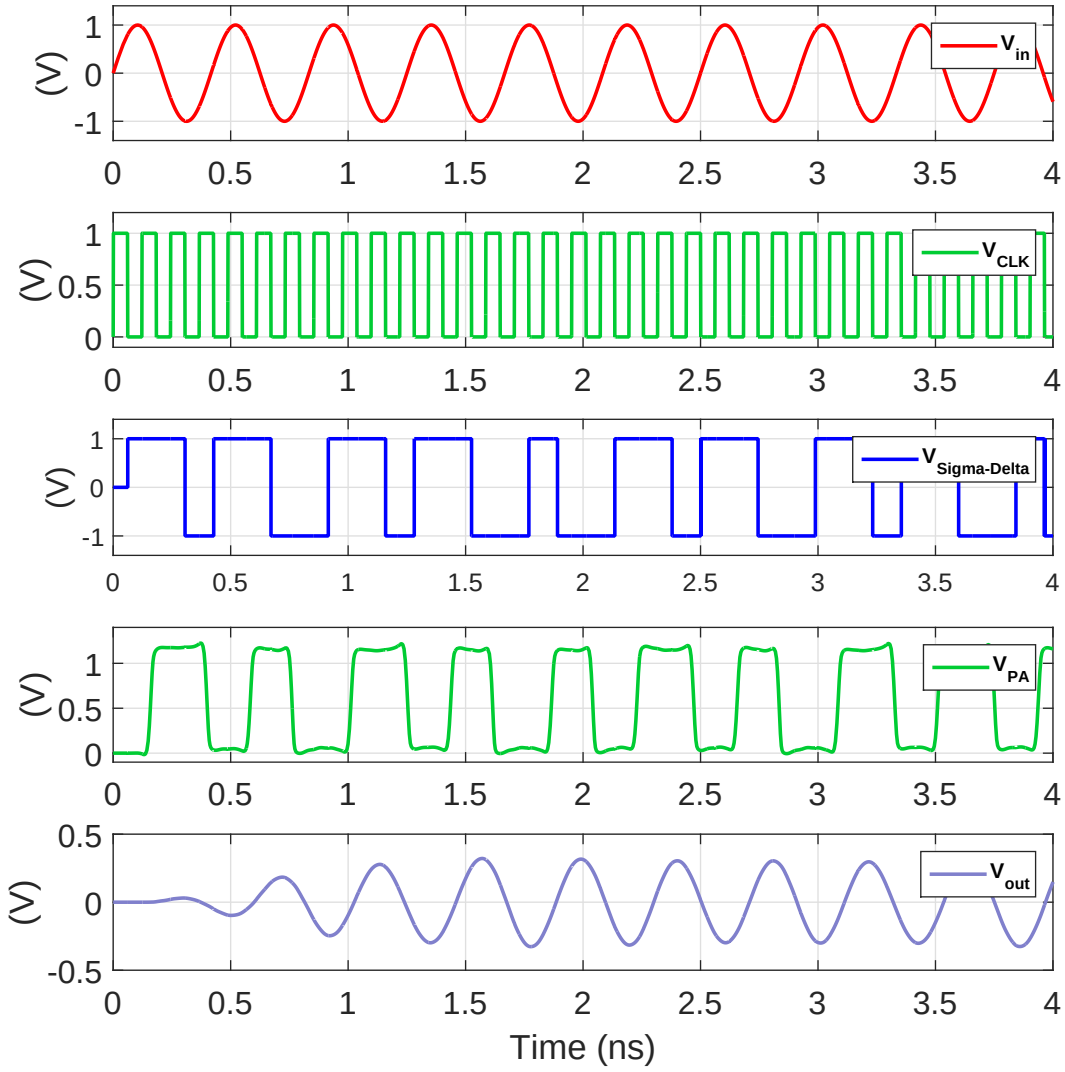


Figure 4.10: $\sum \Delta$ modulator with RF CDVS PA circuit waveforms.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

The objective of this thesis was to design the CMOS RF CDVS PA. Several classes of amplifiers were studied including linear and non-linear classes. The linear classes have the advantage of amplifying non-constant enveloped signal, but their drain efficiency is typically low. The non-linear classes have a theoretical drain efficiency of 100%, and they are a good solution for amplification of constant enveloped signal like the *Bluetooth* modulation.

In the analysis of the Class-D amplifier considering ideal components it was shown that drain efficiency of the 100% can be achieved. Considering the non-ideal analysis of the RF Class-D it was showed that power output is greatly influenced by the voltage of the DC source and the total resistance of the circuit. Also the drain efficiency is degraded by the total resistance of the circuit.

In the design of the high-level model RF CDVS PA, the transistors' width was chosen in a way so that their internal resistance is the lowest possible without getting oversized transistor. It was also shown that the quality factor of the components present in the filter has a great influence on their internal resistance at the resonant frequency. Since the quality factor of integrated inductors and capacitors is low this leads to a considerable internal resistance of each component at the resonant frequency. Therefore, output filter is a major player in the power loss of the circuit. This is shown in the simulation results.

In the simulated model it was shown that the amplifier suffers from a significant increase in DC power consumption due to the fact that in each working cycle there is a short circuit between the DC source and the ground. With a 3^{rd} order Butterworth bandpass filter using ideal components an output power of 6.91dBm was achieved with a drain efficiency of 40%. Using pre-layout components the power output was decreased to

0.317 dBm and the drain efficiency went to 8.6%. This shows that circuit design is not a simple task and when considering real components the result can be greatly degraded.

5.2 Future Work

During current work several interesting points that can be addressed in the future work were revealed. These points are :

- Implementation of the IC layout design of the RF Class-D amplifier circuit and comparison of the simulation results obtained in the layout design with the pre-layout simulation;
- Implementation of IC manufactured chip and comparison of the results with the one obtained in the simulation of the IC layout design;
- Implementation the RF Class-D amplifier in different CMOS technology to compare which advantages and disadvantages they will bring to the circuit performance;
- The simulation of the RF Class-D amplifier using *Bluetooth* modulation techniques to understand which impact it would bring on the performance of the circuit.

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APPENDIX A

BUTTERWORTH BANDPASS FILTER DESIGN TABLES

Table A.1: Normalized Butterworth $R_{Source} = 1, R_{Load} = 1$ [p. 58][36].

Order										
1	1.0									
2	1.41421	1.41421								
3	1.0	2.0	1.0							
4	0.76537	1.84776	1.874776	0.76537						
5	0.61803	1.61803	2.0	1.61803	0.61803					
6	0.51764	1.41421	1.93185	1.93185	1.41421	0.51764				
7	0.44504	1.24698	1.80194	2.0	1.80194	1.24698	0.44504			
8	0.39018	1.11114	1.66294	1.96157	1.96157	1.66294	1.11114	0.39018		
9	0.34730	1.0	1.53209	1.87938	2.0	1.87938	1.53209	1.0	0.34730	
10	0.31287	0.90798	1.41421	1.78201	1.97538	1.97538	1.78201	1.41421	0.90798	0.31287

Table A.2: Normalized Butterworth $R_{Source} = \infty$ or $R_{Source} = 0$ [p. 58][36].

Order										
1	1.0									
2	1.41421	0.70711								
3	1.5	1.33333	0.5							
4	1.53074	1.57716	1.08239	0.38268						
5	1.54509	1.69443	1.38196	0.89443	0.30902					
6	1.55292	1.75931	1.55291	1.20163	0.75787	0.25882				
7	1.55765	1.79883	1.65883	1.39717	1.05496	0.65597	0.22521			
8	1.56073	1.82464	1.72874	1.52832	1.25882	0.93705	0.57755	0.19509		
9	1.56284	1.84241	1.77719	1.62019	1.40373	1.14076	0.84136	0.51555	0.17365	
10	1.56435	1.85516	1.81211	1.68689	1.51000	1.29209	1.04062	0.76263	0.46538	0.15643

APPENDIX B

IDEAL 1ST ORDER ∑Δ MODULATOR BLOCK.

```
1  `include "disciplines.vams"
2
3  (*ignore_hidden_state*) module Sigma_Delta(in,clk,out);
4
5  //module Sigma_Delta(in,clk,out);
6
7  input in, clk;
8  output out;
9  voltage in,clk,out;
10 parameter real quantizer_vth = 0;
11 parameter real d2a_gain_vref = 1;
12
13 real vsum;
14 real vd;
15 real vint;
16 real vout;
17 real hi,lo;
18
19 analog
20 begin
21   @(initial_step)
22   begin
23     vd=0; vint=0; vout=0;
24     hi = 1; lo = -1;
25   end
26
27   @(cross(V(clk),1))
28
29   begin
30
31     //Summing Junction
```

```
32
33      vsum = V(in)-vd;
34
35      //Integrator
36      vint = vint + vsum;
37
38      //Quantizer
39
40      if(vint > quantizer_vth)
41        vout = hi;
42      else
43        vout = lo;
44
45      // Digital  to Analog
46
47      vd= d2a_gain_vref*vout;
48
49      end
50
51      V(out) <+ vout;
52
53    end
54
55 endmodule
```

APPENDIX C

LEVEL-SHIFTER BLOCK.

```
56  `include "disciplines.vams"
57
58  (*ignore_hidden_state*) module Sigma_Delta(in,clk,out);
59
60  //module Level_Shifter(in,clk,out);
61
62  input in, clk;
63  output out;
64  voltage in,clk,out;
65
66  real vout;
67
68  analog
69
70  begin
71    @(initial_step)
72    begin
73      vout=0;
74    end
75
76    @(cross(V(clk),1))
77    begin
78      if(V(in) > 0)
79        vout = 1.2;
80      else
81        vout = 0;
82    end
83
84    V(out) <+ vout;
85
86  end
```

```
87
88 endmodule
```