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# 8-Phase Ring Oscillator for Modern Receivers

Dissertação para obtenção do Grau de Mestre em
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*À minha mãe, que é essa grande mulher, a quem eu devo tudo o que sou.*

# Agradecimentos

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# Abstract

The evolution of receiver architectures, built in modern CMOS technologies, allows the design of high efficient receivers. A key block in modern receivers is the oscillator. The main objective of this thesis is to design a very low power and low area 8-Phase Ring Oscillator for biomedical applications (ISM and WMTS bands).

Oscillators with multiphase outputs and variable duty cycles are required. In this thesis we are focused in 12.5% and 50% duty-cycles approaches. The proposed circuit uses eight inverters in a ring structure, in order to generate the output duty cycle of 50%. The duty cycle of 1/8 is achieved through the combination of the longer duty cycle signals in pairs, using, for this purpose, NAND gates. Since the general application are not only the wireless communications context, as well as industrial, scientific and medical plans, the 8-Phase Oscillator is simulated to be wideband between 100 MHz and 1 GHz, and be able to operate in the ISM bands (447 MHz-930 MHz) and WMTS (600 MHz).

The circuit prototype is designed in UMC 130 nm CMOS technology. The maximum value of current drawn from a DC power source of 1.2 V, at a maximum frequency of 930 MHz achieved, is 17.54 mA. After completion of the oscillator layout studied (occupied area is 165 µm x 83 µm). Measurement results confirm the expected operating range from the simulations, and therefore, that the oscillator fulfil effectively the goals initially proposed in order to be used as Local Oscillator in RF Modern Receivers.

**Keywords:** CMOS Inverters, Layout, Ring Oscillator, Multi-Phase Oscillator, Low-IF Receivers

# Resumo

A evolução das arquitecturas de receptores, construídos através de tecnologias modernas CMOS, permite o dimensionamento de receptores altamente eficientes. Um bloco importante nos receptores modernos é o oscilador. O principal objectivo desta dissertação, passa pelo estudo de um Oscilador em Anel de 8 Fases de área e consumo muito reduzidos, para uso em aplicações biomédicas (bandas ISM e WMTS).

São cada vez mais necessários, osciladores capazes de fornecer variadas fases e fabricar diferentes *duty cycles*. Nesta tese o foco encontra-se em aproximações com *duty cycles* de 12.5% e 50%. O circuito apresentado utiliza 8 inversores em formação de anel, de forma a gerar os *duty cycles* de 50%. O *duty cycle* de 1/8 é alcançado através da combinação dos sinais já existentes, dois a dois, nas entradas de uma porta lógica NAND. Tendo em conta que o Oscilador de 8 Fases não é projectado apenas com vista a comunicações sem fios, mas também com vista os planos industriais, científicos e médicos, o Oscilador de 8 Fases é simulado de forma obter uma largura de banda entre os 100 MHz e 1 GHz, e ser capaz de funcionar dentro das bandas ISM (447 MHz-930 MHz) e WMTS (600 MHz).

O circuito protótipo é implementado numa tecnologia UMC 130 nm CMOS. A corrente máxima, fornecida pela fonte de tensão DC de 1,2 V, alcançada a uma frequência de oscilação de 930 MHz, é 17,54 mA. Após a conclusão do *layout* do oscilador em estudo (área ocupada de 165 µm x 83 µm), resultados das medições confirmam a banda de funcionamento prevista pelas simulações e, também, que o oscilador cumpre de forma eficaz todas as metas propostas inicialmente com a finalidade de ser utilizado em Receptores RF Modernos como Oscilador Local.

**Palavras-chave:** “Layout”, Inversores CMOS, Oscilador em anel, Oscilador de várias fases, Receptores “Low-IF”.

# Abbreviations

| | |
|---|---|
| ADC | Analog-To-Digital Converter |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| DC | Direct Current |
| DT | Discrete-Time |
| HR | Harmonic-Rejection |
| IF | Intermediate Frequency |
| IIP | Intermodulation Intercept Point |
| IIR | Infinite Impulse Response |
| ISM | Industrial, Scientific and Medical |
| LNA | Low Noise Amplifier |
| LO | Local Oscillator |
| NF | Noise Figure |
| NMOS | Nchannel Metal-Oxide-Semiconductor |
| PLL | Phase Locked Loop |
| PMOS | Pchannel Metal-Oxide-Semiconductor |
| RF | Radio Frequency |
| SC | Switched-Capacitor |
| VCO | Voltage-Controlled Oscillator |
| WMTS | Wireless Medical Telemetry Service |
| LPF | Low Pass Filter |
| BPF | Band Pass Filter |

# Contents

# List of Figures

# List of Tables

1

# 1 Introduction

## *1.1 Background and Motivation*

Modern transceivers for wireless communications require circuits with low power consumption, size, cost, noise, while increasing the frequency and bandwidth. The successful travel of wireless communications led to new and more challenging requirements such as: low supply voltage, low cost, and low area circuits. The use of modern CMOS nanotechnologies allows, by adjusting old architectures or by employing new circuit designs, to find a way to reach these objectives [1].

The circuit between the antenna and the digital part, is generally defined as the RF front-end. Due to very tough specifications for RF blocks, the receiver front-end has a very important role in communications. Receiver architectures can be divided into: heterodyne and homodyne. The first converts the signal to an intermediate frequency (IF), while the second downconverts directly to the baseband. Combining the main advantages of both architectures, the Low-IF receiver is a modified version of the homodyne and is becoming a good alternative [1, 2].

Due to development of wireless receiver architectures, image-rejection topologies require accurate quadrature voltage-controlled oscillator (VCO). The way to keep an oscillator outputs stable in frequency and phase, is to connect two oscillators in a feedback structure, in order to be able to generate signals with a precise 90° phase shift. There's many ways to obtain accurate quadrature outputs. Due to this, new architectures have emerged using RC and LC oscillators, some of them have inherent quadrature outputs, for example the two integrator oscillator [1].

On the other hand, oscillators with wide operating range, they can provide different carrier frequencies and data rates for wireless transmissions in the existing variety of

communication standards. A polyphase filter can produce quadrature signals using differential outputs of a VCO [3], [4]. Another technique to get quadrature output is to design a VCO, which works at double the desired frequency, followed by frequency division [5]. Coupled VCOs structure [6] and [7], coupled resonators in a ring structure [8], and multiphase ring oscillators [9] are other alternatives to produce quadrature outputs [10]. The architecture proposed in this thesis uses a combination of cross-coupled inverters and ring oscillators concept, for generating multiphase outputs.

## *1.2 Thesis Organization*

This thesis is presented into six chapters, including the present introduction. Since each chapter begins with a small introduction presenting that specific topics, here it is just a brief and general reference to each chapter.

**Chapter 2 - Receiver Architectures and RF Blocks:** this chapter is the literature review of the dissertation, introducing and describing the main architectures related to both receivers and the RF blocks.

**Chapter 3 - Oscillators:** is hereby continued the previous chapter, but with a more detailed view only on the RF block in which this thesis focuses properly. It is also included, in the final part, the chosen architecture for the oscillator design.

**Chapter 4 - 8 Phases Oscillator:** is dedicated to the context of the proposed circuit, that is, will be presented the actual topology where the oscillator in study came from. Following that first half, a more detailed study of the proposed topology and sizing of the projected oscillator and its most intimate blocks will also be presented.

**Chapter 5 - Simulation and** Measurement Results**:** it is a chapter that, in addition to combine all types of simulations, either pre or post-layout, also includes presenting the designed layout. It is possible to finish all this experimental stage realizing, in a clear way, with the measurements carried out on the test board, that the oscillator behaved according to its initial premises.

**Chapter 6 - Conclusions and Future Work:** here are woven final considerations about the work, in kind of a summary of the main conclusions to be drawn. It also made the transposition into prospects and future work in order to improve the originated contribution.

## *1.3 Main Contributions*

The contributions of this thesis consist essentially in the redesign and layout of an architecture of 8-phases oscillator previously proposed [11]. The redesign allowed to evaluate the architecture made previously, which contributed to the confirmation by measurements of operating at 1 GHz with precise 8 phases with 12.5% and 50% duty cycle (The results have resulted in one submitted paper [12]).

2

# 2 Receiver Architectures and RF Blocks

The receivers are used in demodulating a signal sent by a transmitter, first the signal received by the antenna is amplified using an LNA, and then, downconverted to a lower frequency. In the end, it is possible to obtain at the outputs a demodulated signal. The receivers can be divided into two basic architectures: heterodyne or homodyne [13]. In the heterodyne one, signal is downconverted to an intermediate frequency (IF), in homodyne, a conversion is made directly to baseband. Today's favourite architecture is the homodyne for its simplicity, low power consumption and low cost [14]. In recent years new architectures have appeared that take clear advantage of the qualities of each of the aforementioned architectures. Low-IF receiver is precisely one that is being used in FM receivers [2].

The signal received by the antenna is processed by several receiver blocks, each with a specific function. One of the major blocks is LNA, since the intention involves amplifying the received signal in order to minimize noise. Another crucial block is the oscillator, this block generates a frequency, which combined with the mixer will change the signal frequency.

Modern receivers require quadrature outputs, because of this, the oscillator should be capable of generating more than one waveform. Thus, and for obvious reasons, will be dedicated one chapter just for literature review of the oscillators [13].

## *2.1 Receiver Architectures*

There are 3 very popular receivers architectures, they are: heterodyne, homodyne and Low-IF [2,14]. The first one is widely used and is characterized for taking the RF signal to an

Intermediate Frequency (IF) in a first stage and, just at a second plane, is that the signal is brought to baseband. The second type of receptor announced is also known as direct IF or zero-IF up, which results in a direct translation to RF baseband. The low-IF receiver architecture is similar to the heterodyne where the RF signal is brought to a low-IF frequency, and only brought to the baseband after being converted into the digital domain.

### 2.1.1 Heterodyne or IF Receivers

The block diagram of a heterodyne receiver is shown in Figure 2.1. Before being amplified by the LNA, the input signal undergoes the action of a bandpass filter to select the frequencies of interest. To mitigate the signs on the image frequency band outside the LNA, is used an image rejection filter. The mixer together with the oscillator, bring the signal to the IF, and thus, the signal again passes through a band pass filter to isolate the bandwidth of the IF and finally be amplified by an IF amplifier. For the mixer to bring the signal to baseband, and make downconversion, both in-phase (I) and quadrature (Q) components are necessary. Then, to be converted to digital domain, the signal passes through a low-pass filter.

In order to be possible to obtain a high quality factor (Q), used filters should be implemented off-chip, this is one of the reasons why this architecture is avoided in modern technology. The need for a high performance oscillator and the image frequency, are two main disadvantages of this architecture [13].

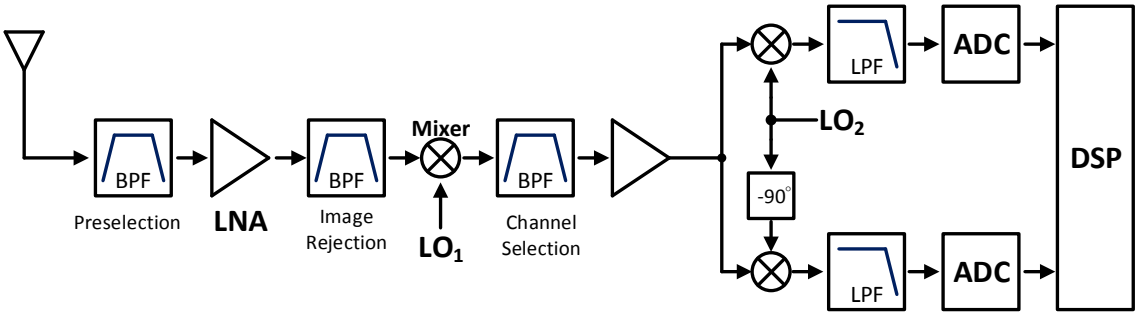



**Figure 2-1 – Basic Heterodyne Architecture [1].**

The mixer causes the problem of frequency image, moving both the sum and the difference frequencies, converting them for the same IF. If the downconvertion of a signal with a frequency $\omega_{RF}$ has to be done to a frequency $\omega_{IF}$, but the frequency image in $\omega_{IM}$ (as shown in Figure 2.2) is also downconverted. Even after the image rejection filter there is a small signal

at that frequency. When the signal is pushed into the mixer, both frequencies are downconverted to $\omega_{IF}$. A practical example to follow is assuming that: $\omega_{IF}$ is 50 MHz, $\omega_{RF}$ is 850 MHz, $\omega_{LO}$ 900 MHz and $\omega_{IM}$ is a signal at the 950 MHz that will also be "downconverted" by the mixer to $\omega_{IF}$.

There is a trade-off about this architecture, related to the IF frequency. Some receiver blocks are influenced by the frequency chosen. With a higher frequency, it becomes easier to design an image rejection filter, because the image is far from the desired frequency. But the band-pass filter next to the mixer will necessarily be less demanding, making it easier to implement for a lower value of IF, the same applies to the IF amplifier.

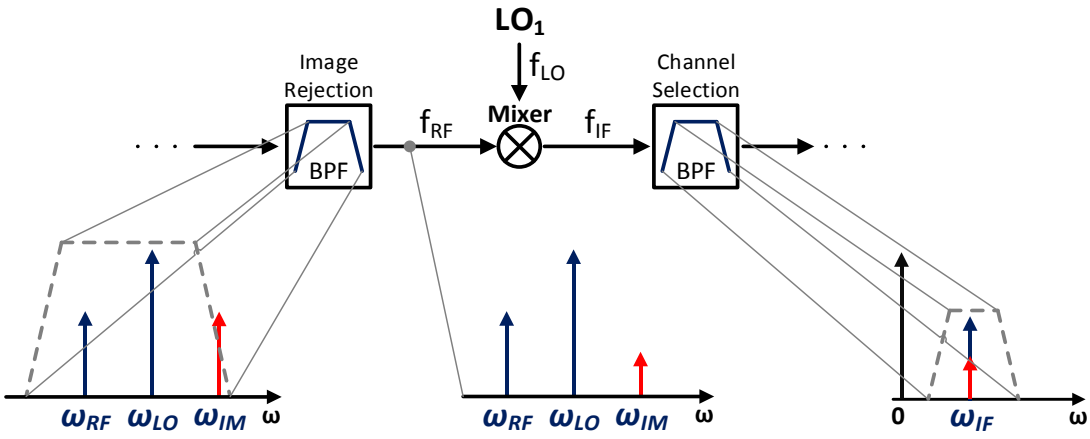



**Figure 2-2 – Image Rejection fundamentals [13].**

### 2.1.2 Homodyne or Zero-IF Receivers

Zero-IF receivers are known for carrying the signal directly from RF to baseband. The lack of a first mixer, before downconvertion itself, is the most obvious difference between homodyne and heterodyne, which is why filters are implemented only for the signal before LNA and after the downconvertion.

In heterodyne, as already had the opportunity to check, the first mixer causes an overlap between two signals in IF, in this case, since the IF is zero, the desired frequency is the same as the image one, so there is no need for an image rejection filter. Another advantage lies in the amplification, as it is done in the baseband, the power consumption is reduced. Additionally, there is no need to use a bandpass filter, instead, only a low pass filter is used, after the downconvertion. Whereas there is no image rejection filter, the LNA does not need to be

matched to 50 ohms at the output. This architecture has fewer blocks, as shown in Figure 2.3, therefore, has lower power consumption than the heterodyne receiver [1, 2, 14].

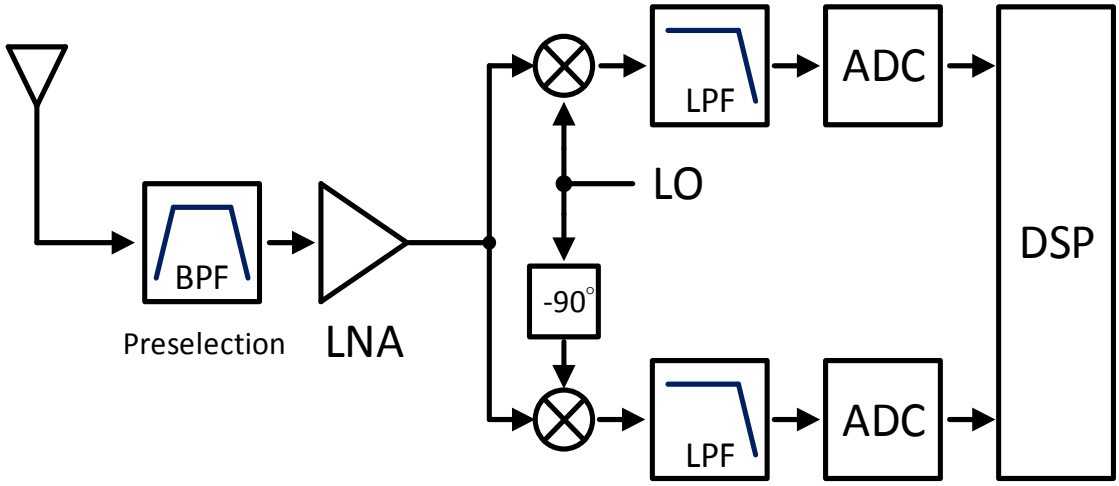



**Figure 2-3 – Basic Homodyne Architecture [1].**

When compared to heterodyne, this architecture have some disadvantages, but is still under research for more picky applications [1]. These disadvantages are:

- Named local oscillator leakage, this means that, between the local oscillator and the input port of the mixer and LNA, can be some kind of imperfect isolation. This leakage mixed with the original wave from the oscillator, create DC offsets in the mixer output. Antenna can also be the target of this leakage, which interferes with other receivers at the same frequency;
- DC offsets, because of the previous leakage from the oscillator, a voltage offset at mixer output appears and causes the saturation of the successive blocks.
- Flicker noise due to the spectrum close to DC from active devices, may corrupt the base band signals;
- Quadrature mismatch and error, the most critical aspect of direct-conversion receivers, where the main goal is to have equal I and Q branches with a phase difference of 90°, to create the ideal baseband signals. The mismatch between the branches contaminate the signal;
- Even order distortion (in intermodulation), creates a DC offset so the receiver shall have a high IIP2 (second-order intermodulation intercept point).

Once again, the low cost, low area, and low power consumption of this receiver, are the main reasons for this architecture to be used. Even though the performance is better than the

homodyne, the heterodyne needs external high quality components. The next architecture combines both receivers' advantages into one.

### 2.1.3 Low-IF Receivers

Similar structure to the one of the homodyne type, but instead of downconverting to the baseband it converts to an IF close to the baseband. The signal path comprise, in first place, a band pass filter, then it is amplified and mixed in quadrature to a low IF. Finally, and before suffering the action of the ADC, the signal is amplified and filtered once again. To avoid the DC offset problems caused by LO leakage in the homodyne, but introducing the image frequency disadvantage of the heterodyne, IF must be once or twice the bandwidth of the desired signal.

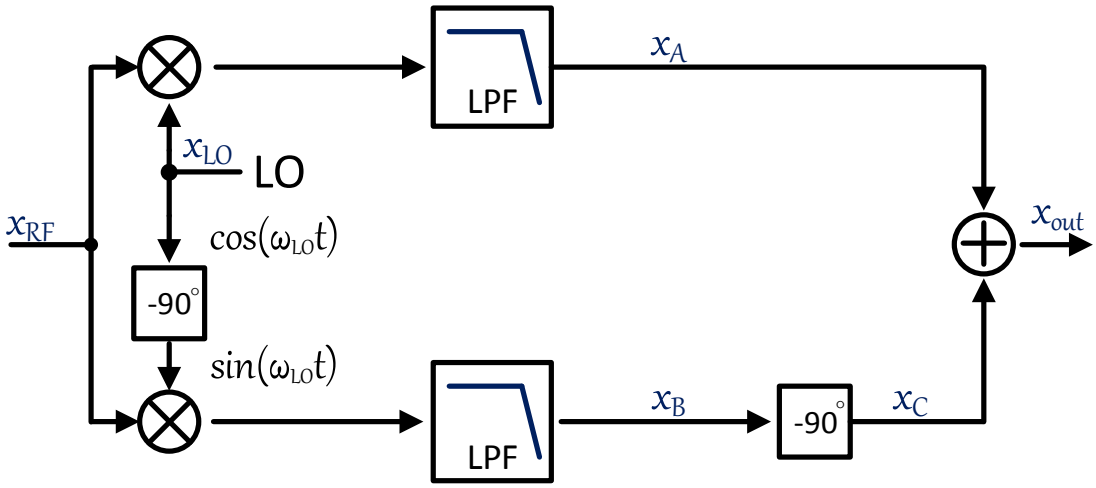
In opposite to the heterodyne, by the fact that it would require a filter with an extreme quality factor (Q) for the low IF, will be dropped the hypothesis of using an image rejection filter. Hartley and Weaver architectures have been proposed, as image reject techniques. These techniques only make sense implemented after the low pass filter, combining both outputs into a single one (variations of these architectures were also made for quadrature outputs).

The image rejection ratio (IIR) is the way to quantify the degree of image rejection in a receiver, which is given by (2.1). $P_{IM}$ and $P_S$ are the average power of the image and the signal respectively at the output, $V_{IM}$ and $V_S$ their amplitude at the input. The best of the cases would be where the image signal level is zero, making IRR = ∞.

$$IRR = \frac{\frac{P_{IM}}{P_S}}{\frac{V_{IM}^2}{V_S^2}} \tag{2.1}$$

We assume that the oscillator produces a phase difference of 90° with no mismatches. In Figure 2.4 is shown the Hartley solution that shifts the signal from Q branch another 90° and then both are summed. This solution works as follows, since there was already a shift of 90°, the image signal will be in opposition of the I channel, when adding both (Figure 2.4 shows in detail), the signal at $\omega_{RF}$ is maintained and both images are cancelled mutually.

A shift of -45° on in-phase signal and 45° to the quadrature one, instead of using simply a single 90° shift, is a variation of this architecture, but the principle is the same [13].




$$x_{RF} = A_{RF}\cos(\omega_{RF}t) + A_{IM}\cos(\omega_{IM}t) \qquad x_{LO} = A_{LO}\cos(\omega_{LO}t)$$

$$x_A = \frac{1}{2}A_{LO}A_{RF}\cos((\omega_{LO} - \omega_{RF})\,t) + \frac{1}{2}A_{LO}A_{IM}\cos((\omega_{IM} - \omega_{LO})\,t)$$

$$x_B = \frac{1}{2}A_{LO}A_{RF}\sin((\omega_{LO} - \omega_{RF})\,t) + \frac{1}{2}A_{LO}A_{IM}\sin((\omega_{IM} - \omega_{LO})\,t)$$

$$x_C = \frac{1}{2}A_{LO}A_{RF}\cos((\omega_{LO} - \omega_{RF})\,t) - \frac{1}{2}A_{LO}A_{IM}\cos((\omega_{IM} - \omega_{LO})\,t)$$

**Figure 2-4 – Hartley Architecture [1].**

The simplified Weaver architecture does exactly the same as the Hartley architecture. Replicating the previous quadrature mixing stage after that, as shown in Figure 2.5, the same image cancelling effect is obtained. It is possible to use for quadrature outputs, if some changes to this architecture would be drawn. Anyways the Hartley architecture is more suitable for a single output, because a second mixing stage could produce more phase deviations.

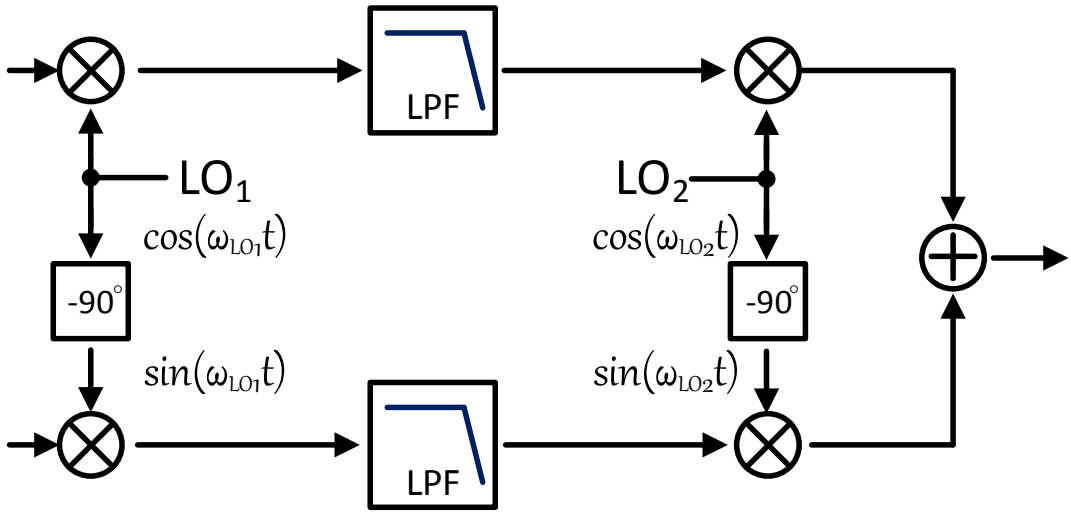



**Figure 2-5 – Weaver Architecture [1].**

The remaining circuit is affected by a mismatch in phase and amplitude. The phase error is quite difficult to correct, but in the other hand, the amplitude imprecision is not so influential because, after the band pass filter, the signal is amplified. What can also take influence in both image and signal of interest average power, is the phase error. Assuming that actually there is a quadrature mismatch in the oscillator, (2.1) can lead us to (2.2), where ($\theta$) represents the phase error. Then, it is possible to conclude that the main variable to image suppression success is the accuracy of the oscillator [13].

$$IRR = \frac{\theta^2}{4} \tag{2.2}$$

## *2.2 LNA Basic Concepts*

A crucial structure block for receivers of a wireless circuit, is the LNA, Low Noise Amplifier. The signals in the antennas are expected to be very weak, so there's a necessity to amplify them in order to be properly handled. However, this amplification must be done carefully, taking into account the reduction of the noise but amplifying to the maximum the wanted signal. In that regard the signal progresses in the best conditions to the rest of the circuit [15].

### 2.2.1 S-Parameters

It is important to study some parameters defined by S11, S12, S21 and S22, to correctly analyse the performance of a LNA. S11 is the input port voltage reflection coefficient, S12 and S21 represent the reverse and forward voltage gain, respectively, and S22 the output port voltage reflection coefficient. An example on how these parameters are represented in a circuit of a LNA is shown in Figure 2.6 [2]. Usually when a LNA is developed, it is possible to assume if some simulated values corresponds to a decent circuit or not [2]. In other words, parameters S11 and S22 are important in this study and their values represent the input and output matching of the LNA. S12 is the reverse gain and it is a kind of response in relation to S21, therefore it is required to this parameter to be very small to grant good isolation. Finally, S21 is related to the capacity of a LNA to amplify the signal in good conditions, so the bigger this parameter is, the better is the performance of the LNA [16].

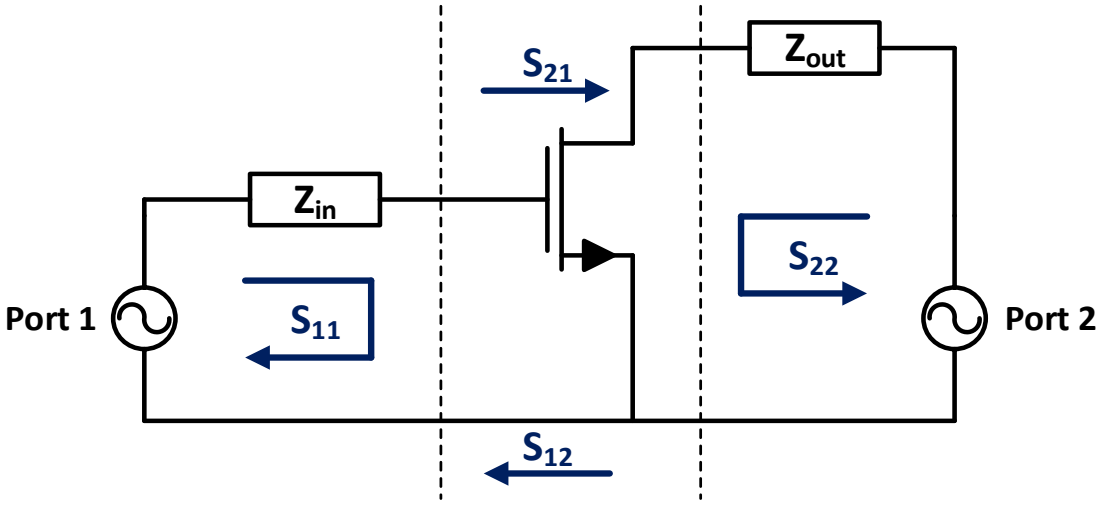



**Figure 2-6 – S-Parameters [16].**

In conclusion, the importance that the output, i.e., the parameters S21 and S22 have is reduced when talking about a complete global receiver architecture, makes sense only refer to the circuit input, which is the most critical. This will only occur upon the detailed and isolated LNA study from all other blocks.

First of all, before taking into account the LNA development itself, are the stability requirements. As it is possible to verify in the equations (2.3) and (2.4) [2], this factor takes advantage of the S-Parameters to calculate and verify the circuit stability.

$$\Delta = S_{11} * S_{22} - S_{12} * S_{21} \tag{2.3}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 * |S_{12} * S_{21}|^2} \tag{2.4}$$

### 2.2.2 Stability

The premises that, when K > 1 and $|\Delta|<1$ lead to a conclusion of actual stability, are usually directed for bipolar transistors, but can also be noted for CMOS transistors. Important to say that S-parameters give the power gain, and it is possible to confirm with (2.5) and (2.6).

$$Power\ Gain = 10 * \log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (2.5)$$

$$Voltage\ Gain = 20 * \log_{10}\left(\frac{V_{out}}{V_{in}}\right) \quad (2.6)$$

### 2.2.3 Noise Figure

The other great and crucial parameter to rate the quality of a LNA is the Noise Factor. The lower the F, the lower will be the final F of the complete receiver, so it is extremely important to optimize it. Because of this value can depend on what application is measured, and also it has a close trade-off with the maximum gain reachable, usually, it is tough to define the best value for a circuit.

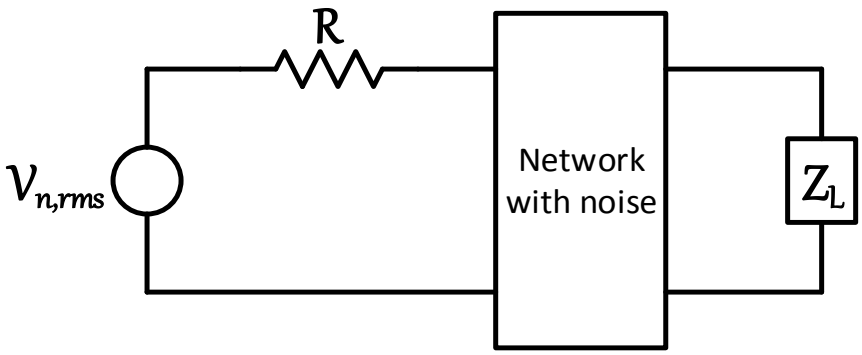



**Figure 2-7 – Noise Network [16].**

In general, and about this kind of noise, is common sense that it is related with thermal noise. Thus, the noise factor is defined as the ratio of the output noise power, of the LNA, to the portion thereof attributable to thermal noise in the input, at standard noise temperature $T_0$= 17°C (290 K), this ratio can be expressed by (2.7) [2].

$$F = \frac{P_{No}}{P_{Ni} * G_A} = \frac{P_{No}}{P_{Ni} * \frac{P_{So}}{P_{Si}}} = \frac{\frac{P_{Si}}{P_{Ni}}}{\frac{P_{So}}{P_{No}}} = \frac{SNR_{in}}{SNR_{out}} \quad (2.7)$$

The noise figure is simply the noise factor expressed in decibels (2.8).

$$NF = 10 * \log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) = SNR_{in,dB} - SNR_{out,dB} \quad (2.8)$$

$P_{No}$ and $P_{Ni}$ are the available noise power presented at the output and input, respectively. $P_{Si}$ and $P_{So}$ are the available signal power at the input and at the output too. At the start of this chapter the LNA was treated as one of the most important blocks in a receiver, and now it will be shown why. If (2.9) [2] can be take into account, it is easy to understand that the gain of the LNA is present in every block of the receiver, so it is extremely important to have a good gain in the first block (LNA) to compensate the others [2]. A basic configuration can be shown in Figure 2.7 [16] and Figure 2.8 [2].

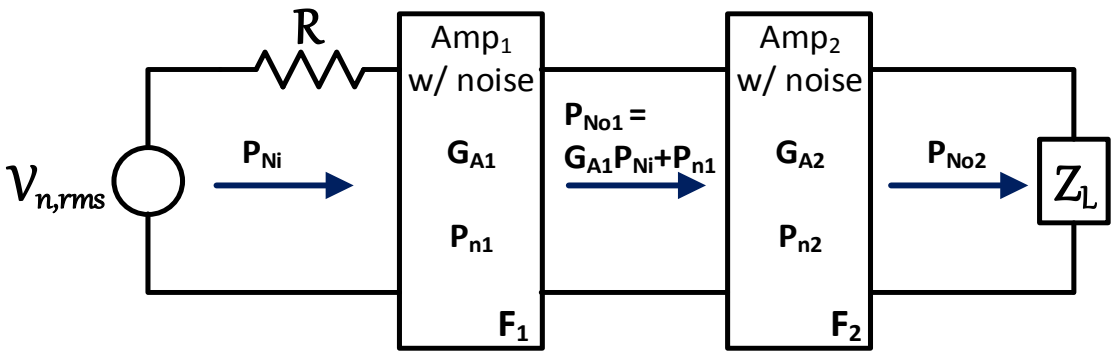



**Figure 2-8 – Noise Network [2].**

$$F = \frac{P_{No2}}{P_{No1} * G_{A2}} = \frac{G_{A2} * (P_{Ni} * G_{A1} + P_{n1}) + P_{n2}}{P_{Ni} * G_{A1} * G_{A2}} = F1 + \frac{SNR_{in}}{SNR_{out}}$$
$$F = F1 + \frac{F2 - 1}{G_{A1}} + \frac{F3 - 1}{G_{A1} * G_{A2}} + \cdots \quad (2.9)$$

## *2.3 Mixers*

The responsibility for the process of translating the frequency to an Intermediate frequency (IF), or to baseband (known as down-conversion), belongs to one important receiver element. That important role is played by the mixer. In Figure 2.9 is possible to verify that it is just a multiplicative operation between two high frequency inputs. The inputs are the RF signal and the other is the LO signal. From this operation results two signals (shown in Figure 2.10 and considering the translations to IF only), the frequency of the signals are, respectively the sum and the difference of the frequencies from the input signals [1].

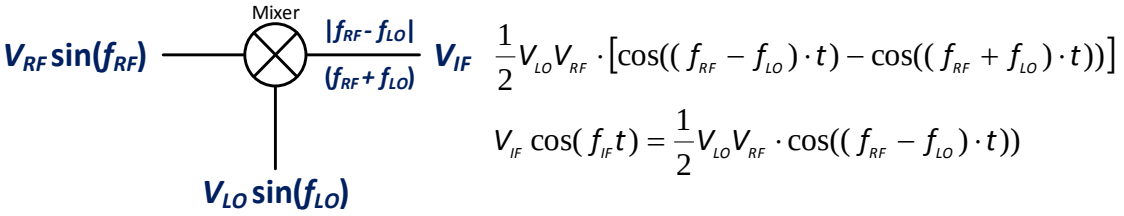



**Figure 2-9 –Mixing Operation.**

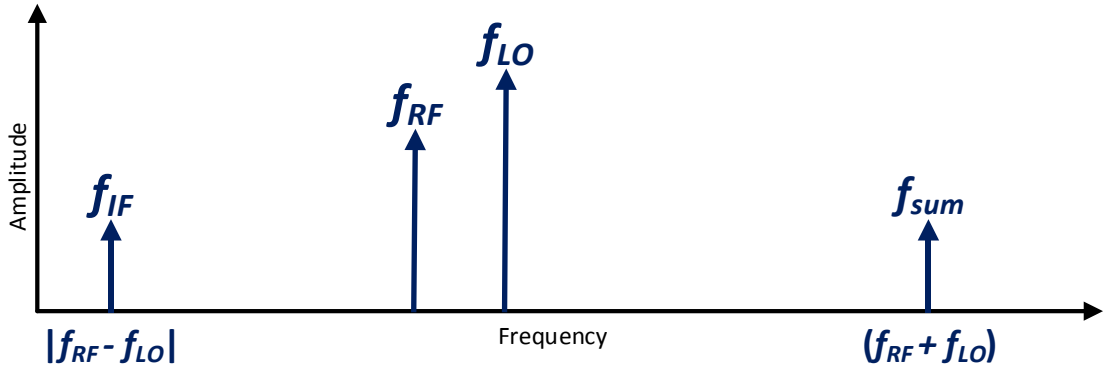



**Figure 2-10 – Down-Conversion Resulting Spectrum.**

Having in mind that the mixing process have nonlinear behaviour so, it's natural to predict higher order effects and intermodulation issues, when using MOS transistors (which are non-linear devices). This way, both phase and amplitude of the wanted signal, get compromised, thanks to those effects and issues mentioned before, complicating the design process.

Forward on this chapter will be possible to overview two kinds of MOS transistors mixers as well as their properties and characteristics.

### 2.3.1 Performance Parameters of Mixers

***Conversion Gain***

As studied in the beginning of this chapter, for a mixer to be useful, it must be followed by a filter that removes the high frequency component. Assuming an ideal filter, the output is given by equation 2.10.

$$\frac{1}{2}V_{LO}V_{RF}\cos\left((f_{RF}-f_{LO})t\right) \tag{2.10}$$

Keeping an ideal scenario, the quotient between IF and RF signals define the gain (expressed in dB) and it is given by:

$$20\log\left(\frac{V_{LO}V_{RF}}{2V_{RF}}\right)=20\log\left(\frac{V_{LO}}{2}\right) \tag{2.11}$$

The appearance of unwanted signals is originated by the fact that the mixer is implemented through a not so simple non-linear system [17]. A frequency dependent gain is lead to by the non-ideal filtering (less or greater than one). All of these effects together results in equation 2.11.

$$20\log_{10}\left(\frac{V_{LO}A}{2}\right) \tag{2.12}$$

***Noise***

The efficiency of the energy conversion from a mixer is the same either in the upper or lower sidebands. The same way as the original signal, every noise source will be replicated and translated up and down as well. In the IF band domain, the aliasing effect generated by both LO and LNA noise, will be noticeable at the output. This is a consequence of the wideband nature of the noise. The noise contributions decrease, can avoid some of these effects and lower the mixer noise as well (equation (2.8) and (2.9)).

A final note to this matter regards to the IF frequency selection. This must be done carefully. The flicker noise can be unpleasant if the IF frequency is below flicker noise corner frequency while the frequency translation of the noise occurs.

***Linearity and Intermodulation Products***

There is a need for an indication of the 3rd order products levels that a mixer is most likely to produce under multi-tone excitation. That spurious products in a mixer are harmonics that, when generated, can be difficult to filter without eradicating the wanted IF signal. This is problematic.

To describe this effect there is the necessity of IIP3 measurement. This named Input Referred Intercept Point is defined as the input power of the RF signal at which, the output power of the third order intermodulation products become equal or greater than the IF signal.

With the intersection of the extrapolated IF response with the third-order intermodulation IF product, it becomes possible to achieve this abstract point shown in Figure 2.11.

Summarising, the higher intercept point will allow to handle more input power without causing undesired products, which would interfere with the desired IF output product, and, mainly, it will allow mixer to have a greater dynamic range [17].

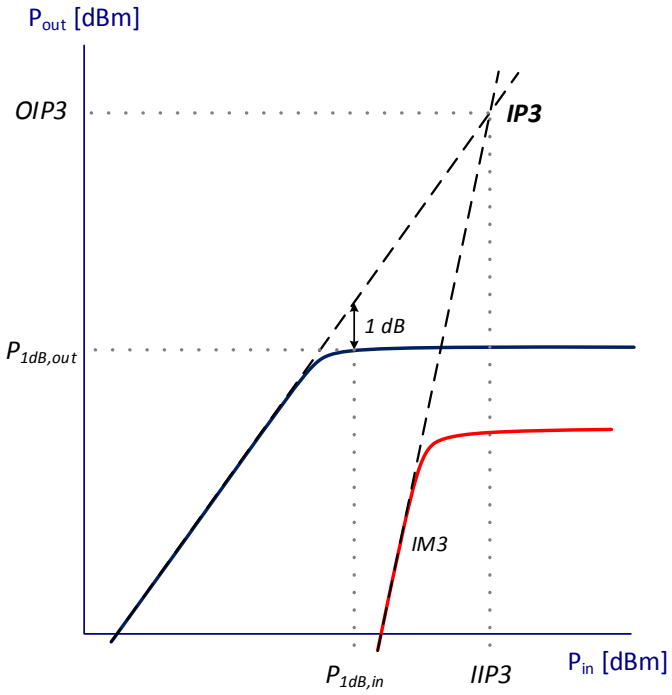



**Figure 2-11 – 3rd Order Intercept Point (IIP3).**

These calculations gives an indication of the capability of the mixer, to handle the signal. That justifies why it is so important, in terms of performance measurements of a mixer, to calculate this parameter.

### 2.3.2 Different Types of Mixers

***Passive Mixers***

In order to produce the mixing operation, by the simplest way, the switching method can be used. This process consists of shifting the input RF signal to the output at lower frequency

(IF). It also explains that LO signal at high level implies an open switch, consequently, the RF input signal is transferred, and at low level the switch is off and the input signal is not transferred.

The passive mixer, which implements the mentioned process, can be designed by using CMOS transistor, shown in Figure 2.12. The gate of the transistor is driven by the LO signal, the RF signal is applied at its source and the IF signal is taken at its drain [2].

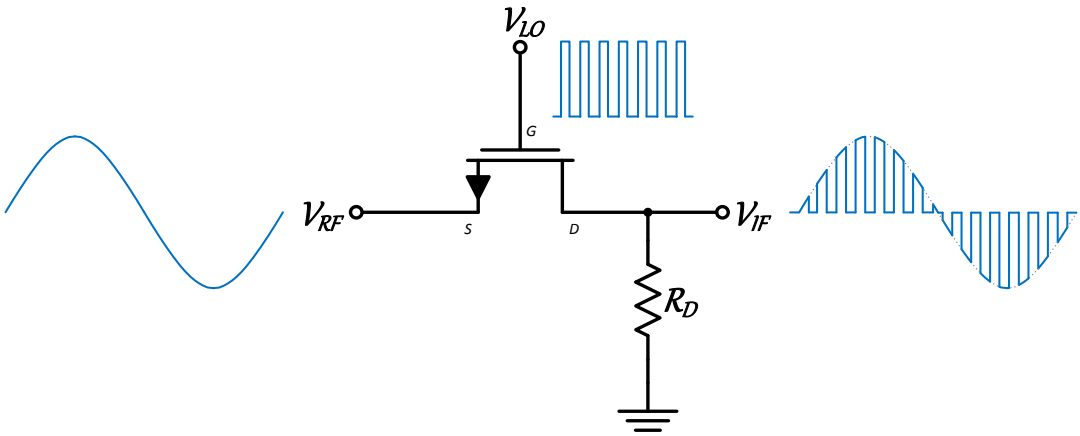



**Figure 2-12 – Passive Mixer Using Active Device [2].**

The transistor presented operates as a switch, because the LO signal induces voltage variation on the gate, which changes the operation region of the transistor. More specifically, and with the help of the equation 2.13, whenever the voltage of LO exceeds the voltage of the RF by at least a threshold voltage ($V_{TH}$) the transistor will conduct.

$$\begin{cases} V_{LO} - V_{RF} \geq V_{TH}, & Switch\ on \\ V_{LO} - V_{RF} < V_{TH}, & Switch\ off \end{cases} \tag{2.13}$$

Basically, the transistor will swing between the cut-off region (transistor off) and triode region (transistor on).

***Active Mixers***

In the other hand, there are two other simple alternatives, which are inserted on the active type of mixers, that, contrary to the last one, provide gain and strength to the IF signal, and for that reason these are widely used in RF systems.

In this type of mixer, the mixing operation is achieved with the same commutation behaviour mentioned previously, yet a differential pair is used instead of using a single active device. These transistors operate in the saturation region (when active) and they acquire not only a current gain, but also a high output impedance, which allows to achieve gain. Not to mention that a differential output is retrieved and, consequently, the amplitude of the IF output is doubled [1, 17].

The alternatives, that are discussed here, are named as: Single-Balanced and Double-Balanced Mixers. The first architecture is represented in Figure 2.13.

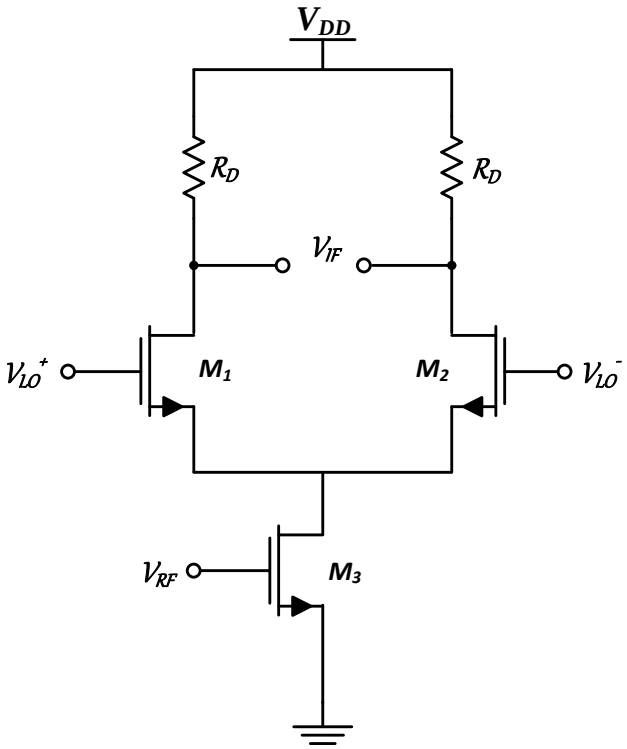



**Figure 2-13 – Single Balanced Mixer [1].**

This mixer has a differential pair of inputs driven by LO signal and also has a RF unbalanced input signal, which is converted into a current and this current is drawn alternately by the two sides of the differential pair. This mixer is a simple active mixer that allows to achieve a moderate gain and noise figure and high input impedance. As disadvantages, it has low 1dB compression point, low IIP3 and low isolation on port-to-port.

The double-balanced mixer is also called Gilbert Cell and is shown in Figure 2.14.

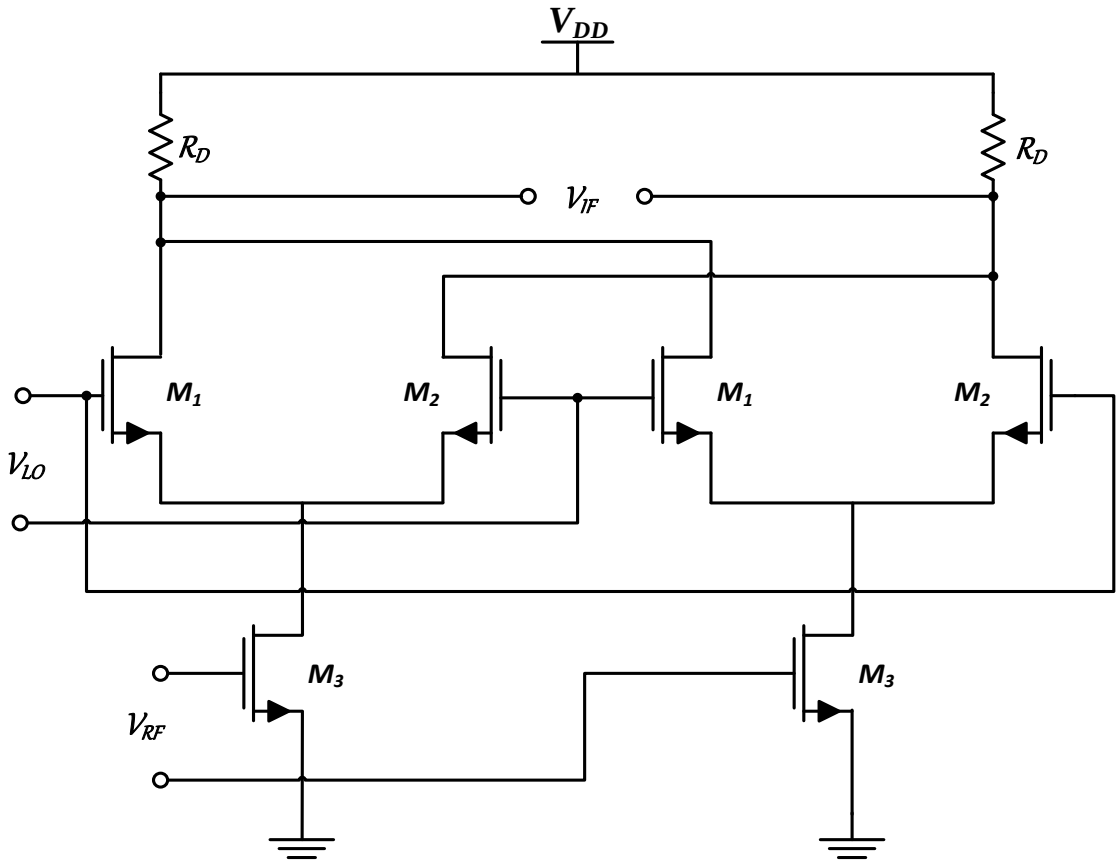



**Figure 2-14 – Gilbert Cell.**

This mixer is more complex because of having only differential inputs, even so, it achieves the same conversion gain as the single-balanced mixer, this can be explained by the circuit symmetry and phase shifts on the inputs and, for that reason, the extra differential pair does not enables gain doubling. Anyhow, it presents a lot of advantages, such as: a better linearity, better port-to-port isolation, it is less sensitive to even order distortion and, due to symmetry, the LO harmonic is removed from the output. The last advantage is useful to ensure a proper function of the following blocks, when considering a more complex RF structure like the receiver. However, these improvements increase the power consumption, the circuit area and its cost [1, 17].

3

# 3 Oscillators

At this particular chapter, it is plausible to begin the explanation related to one of the most important blocks in a receiver, since the quality of a down-conversion depends on the quality of his work. In this sense, it is the oscillator and it can be said that it converts a given DC level in pure sine or square-wave signal.

The performance and some other important parameters of the oscillator, in terms of measures, will be detailed and characterized in the present chapter [1, 18, 19].

## *3.1 Barkhausen Criterion*

It is well known that the basic function of an oscillator is to convert a DC signal into a periodic signal. A sinusoidal oscillator generates a sinusoid with frequency $\omega_0$ and amplitude $V_0$, that is:

$$v_{OUT}(t) = V_0 \cos(\omega_0 t + \theta_0) \tag{3.1}$$

Regarding digital applications, it is fair to mention that oscillators generate a clock signal, which is a square-waveform with period $T_0$. Sinusoidal oscillators can be analyzed as feedback systems, shown in the next Figure, with the transfer function given by (3.2):

$$\frac{v_{out}(j\omega)}{v_{in}(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)\beta(j\omega)} \tag{3.2}$$

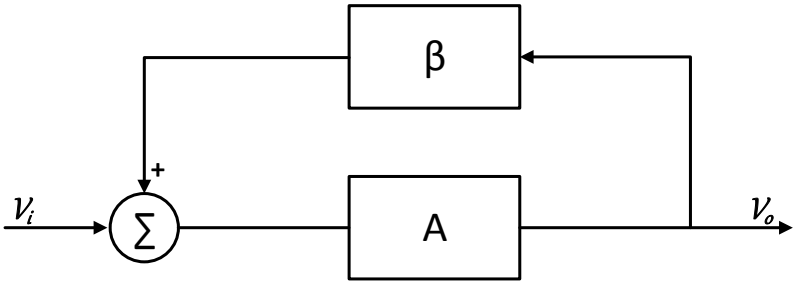



**Figure 3-1 – Simple feedback system [1].**

The necessary conditions regarding the loop gain for steady-state oscillation with frequency $\omega_0$ are known as the Barkhausen conditions.

It is very important to highlight the aforementioned conditions, since they play a vital role in the field of electronics. The loop gain (as show in Figure 3.1) must be unity (gain condition), and the open-loop phase shift must be $2k\pi$, where $k$ is an integer including zero as it can be seen at (3.3) (phase condition).

$$\begin{aligned} |A(j\omega_0)\beta(j\omega_0)| &= 1 \\ arg[A(j\omega_0)\beta(j\omega_0)] &= 2k\pi \end{aligned} \tag{3.3}$$

The Barkhausen criterion gives the necessary conditions for stable oscillations, but not for start-up. For the oscillation to start, triggered by noise, when the system is switched on, it is mandatory that the loop gain must be larger than one, $|A(j\omega_0)\beta(j\omega_0)| > 1$.

## *3.2 Phase-Noise*

Phase noise is an important measure of performance of an oscillator. Ideally an oscillator should generate a perfect sine-wave which corresponds in the frequency domain to two Dirac signals. According to what we said above, the output signal presents a corruption of its spectrum (3.1).

Those undesired components (noise sidebands) that are now present in the spectrum can be quantified and will be reffered as phase-noise (Figure 3.2). This is represented by $\mathcal{L}_{(\Delta\omega)}$ and can be expressed as the ratio between the power in a 1 Hz bandwidth at the offset frequency to the total power of the carrier hence specified in dBc/Hz. Equation 3.4 represents the aforementioned relation.

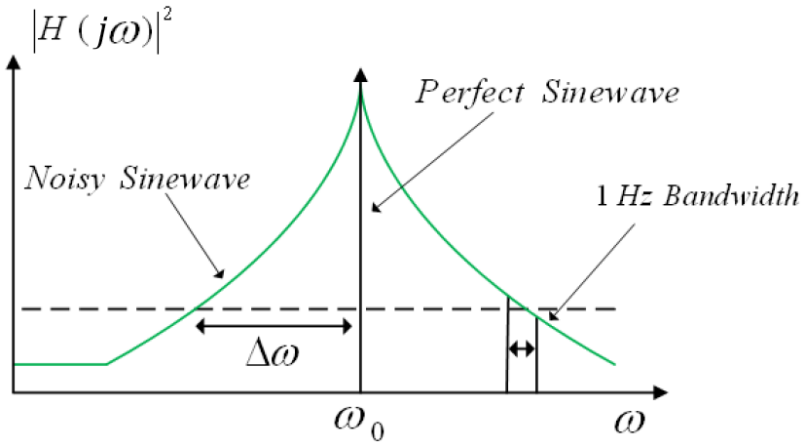



**Figure 3-2 – Ideal Carrier and Carrier with Phase-Noise (adopted from [17]).**

$$\mathcal{L}_{(\Delta\omega)} = \frac{P(\Delta\omega)}{P(\omega_0)} \tag{3.4}$$

The arising of the components previously indicated as noisy sidebands, can compromise the receiver performance. If the receiver mixer performs a down-conversion using an oscillator signal with a considerable amount of phase noise, it could happen that nearby frequencies from the signal of interest can be also down-converted (Figure 3.3). Clearly, this situation will result in overlapped signals (aliasing) which is not wanted [17]. This is the main reason why phase-noise measurement can be useful to quantify the receiver immunity level against nearby channels.

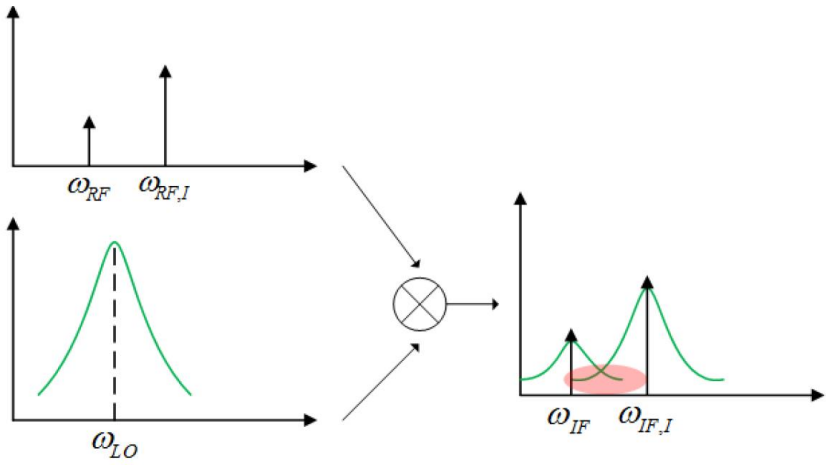



**Figure 3-3 – Phase-Noise Effect in Down-Conversion (adopted from [17]).**

The phase noise can be divided, by considering the single side band (SSB) spectral density in three regions as shown in Figure 3.4. The very first region symbolizes the noise of the active

devices, the second region is the white noise within the oscillator and the last one is the white noise introduced by neighbor devices.

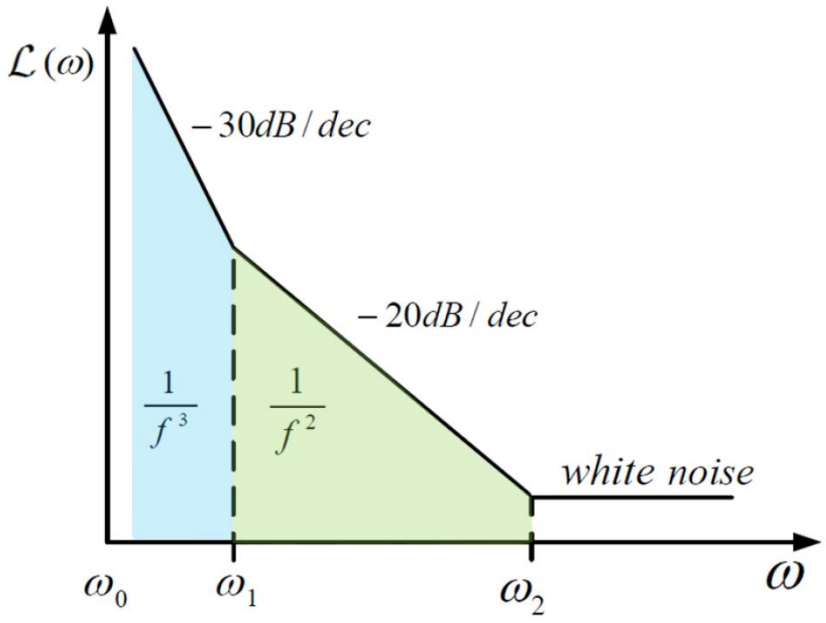



**Figure 3-4 – Phase-Noise Single Side Band (adopted from [17]).**

## *3.3 Quality Factor*

The quality factor is another way of characterizing the carrier spectrum, given the fact that it is related to the oscillator phase-noise (see Figure 3.5). Considering a second order system, there are three plausible designations or definitions for the quality factor.

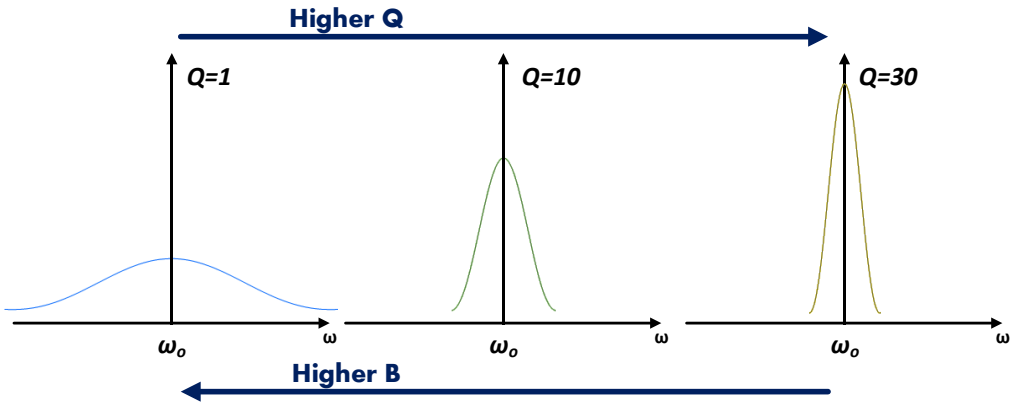



**Figure 3-5 – Carrier Spectrum Regarding Variations in The Quality Factor.**

1. The first definition is related to a second order resonant circuit with bandwidth measured at -3db of the output signal and a carrier frequency $\omega_0$:

$$Q = \frac{\omega_0}{B} \tag{3.5}$$

This is applied to filters and oscillators characterized as second order resonator circuits [1].

2. The second designation is expressed as the measure of the rate of how the energy is lost, regarding to the oscillator stored energy (usually the loss of energy is related to resistive devices and the stored energy with the reactive devices). This is typically applied to a generic RLC circuit and the equation 3.6 expresses the ratio previously discussed:

$$Q = 2\pi \frac{Maximum\ energy\ stored\ in\ a\ period}{Energy\ dissipated\ in\ a\ period} \tag{3.6}$$

3. The third definition takes into consideration, not only the amplitude (A) but also the phase ($\theta$) variations of the open-loop transfer function, $H(j\omega)$, of the oscillator (which is considered as a feedback system). This definition is often considered to calculate the quality factor of a two-integrator oscillator.

$$Q = \frac{\omega_0}{2} \sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\theta}{d\omega}\right)^2} \tag{3.7}$$

The quality factor has an inherent relation with the phase noise, that is, the higher the quality factor more the slopes $1/f^3$ and $1/f^2$ will come close to the carrier frequency which reflects on the decrease of the phase noise [17].

A high Q oscillator will be more difficult to tune and to design, given the fact that it requires several reactive elements (as a consequence, area consumption will increase). Regardless this aspect, it will be more stable and immune to nearby channels.

## *3.4 Examples of Oscillators*

### 3.4.1 LC Oscillator

In Figure 3.6 it is possible to notice the first example presented. To assure the phase shift for oscillation, the LC Oscillator uses pure reactance feedback. Like the CMOS mixers, this circuit acts as a commutator, and is constituted by a differential pair that alternate the current conduction path through the feedback network. The alternate signal is created then.

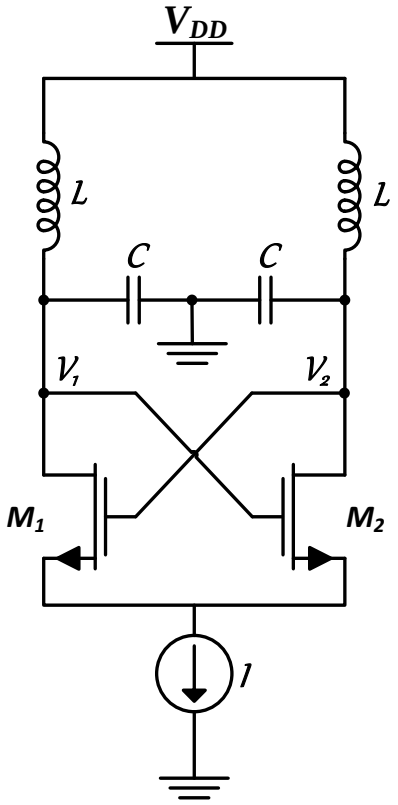



**Figure 3-6 – LC Oscillator [1].**

To meet the Barkhausen conditions, the differential pair presents cross-coupled outputs compensating the losses (installed by the feedback network). In Figure 3.7 is modelled the small signal equivalent of the differential pair, simulating the behaviour of a negative resistance.

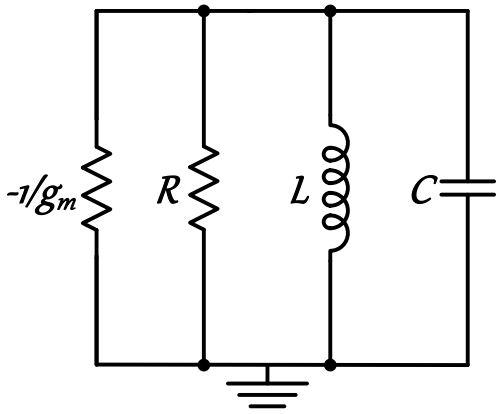



**Figure 3-7 – LC Oscillator Linear Model.**

The main drawback of this kind of oscillator lies on its low frequency tuning capability, since the feedback network parameters are fixed (equation 3.10). On the other hand, a quasi-linear behaviour, low phase-noise and usually a high quality factor represent some of the advantages of the LC oscillators.

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.10}$$

In terms of CMOS technology area consumption, LC oscillators integration have not the most desirable area consumption. Completing, modern receivers require quadrature outputs, which this oscillator alone is not able to provide. The solution lies in coupling an additional oscillator, which will increase even more the area used as well as it will degrade the frequency response due to the additional parasitic capacitances [17].

### 3.4.2 Relaxation Oscillators

In the last years, most of the attention was held to another type of oscillators. Known as RC oscillators (the feedback network is now formed by a capacitor and a resistor) with very similar structure and behaviour to the ones studied in the LC oscillator. Equation 3.8 shows the integrator effect of the capacitor, transforming the DC current into voltage. The resistor is used for biasing purposes [17].

$$v(t) = \frac{1}{C}\int_{t_0}^{t} i(\tau)\, d\tau + v(t_0) \tag{3.8}$$

RC oscillators occupy far less area than a LC oscillator and are highly integrable due to the absence of the inductor which cause a lower quality factor. It has the same differential pair that

is responsible for the loss compensation and commutation behaviour. A common RC oscillator (Relaxation Oscillator) can be observed in Figure 3.8 and the resonant frequency is shown in equation 3.9, where it was given by [1] that this oscillator integration constant is $I/C$, and the amplitude is $4IR$.

$$f = \frac{I}{2C(4RI)} = \frac{1}{8RC} \tag{3.9}$$

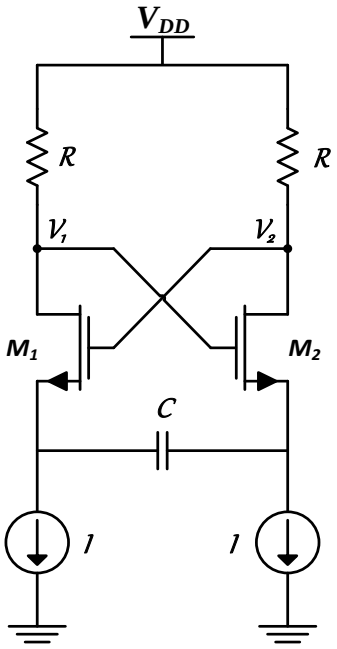



**Figure 3-8 – Relaxation Oscillator [1].**

### 3.4.3 Coupled Ring Oscillators

The most basic CMOS ring oscillator employs an odd number of static single-ended inverters as delay cells ( as shown in Figure 3.9).

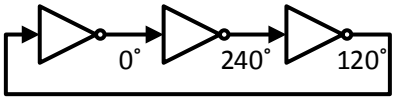



**Figure 3-9 – 3-stage single-ended ring oscillator.**

The transition travelling around the ring has to pass through each inverter twice to arrive at the initial state. Therefore, the oscillation frequency is given by Equation (3.10).

$$f_{osc} = \frac{1}{2 * \tau_{Chain}} = \frac{1}{2 * N * \tau_{Inverter}} \quad (3.10)$$

Unfortunately, quadrature outputs require a ring with an even number of stages [34]. Although coupled ring oscillators are not very conventional, they can provide high speed operations as well as multiphase quadrature outputs. This specially designed, single ended, inverter based coupled ring oscillators are also attractive for the capability of generating quadrature outputs in different variations. Before presenting different varieties of coupled oscillators, it is possible to say that this kind of oscillators may be useful in noisy environments. When compared with conventional ring oscillators, coupled ring oscillators have better phase noise and jitter performance, for a given power dissipation and oscillation frequency [20].

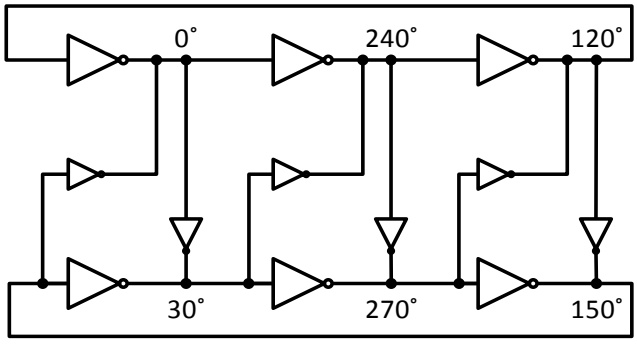



**Figure 3-10 –Two sets of 3-stage ring oscillators coupled together [20].**

In Figure 3.9 is shown two conventional, single ended, three stage ring oscillators [21]. In order to produce multi-phase outputs and high speed oscillation, they are coupled together. This simple linear model of the ring oscillator is used to predict the oscillation frequency of the coupled oscillator. Creating three sets of outputs with 30° phase difference between the neighbour vertical nodes can make this structure to oscillate. To be able to prove that this coupled oscillator is 1.57 times faster than conventional three-stage ring oscillator frequency, [20] were done analytical studies to find a valid function of the transfer matrix of the system. Moreover it is possible to say that compared to conventional ring oscillator, this coupled ring oscillator has double the area occupied by the conventional one and dissipates also the double of the energy supplied.

Another way to produce the quadrature outputs was reported by [10], using a three stage coupled ring oscillator. But this time, were added two delay cells to couple the conventional ring oscillators in Figure 3.9. This ring topology can produce two sets of quadrature outputs with 90°

phase shift as shown in Figure 3.10, and is considered as a Quadrature four-stage ring oscillator [34]. When comparing to conventional ring oscillators performance, it is possible to say that these coupled oscillators have better phase noise, and that the oscillation frequency turns to be just the same as the conventional, single ended, inverter based version of the ring oscillator. In the next chapter a particular coupled ring oscillator will be detailed, the 8-Phase Ring Oscillator, where more useful considerations will be made.

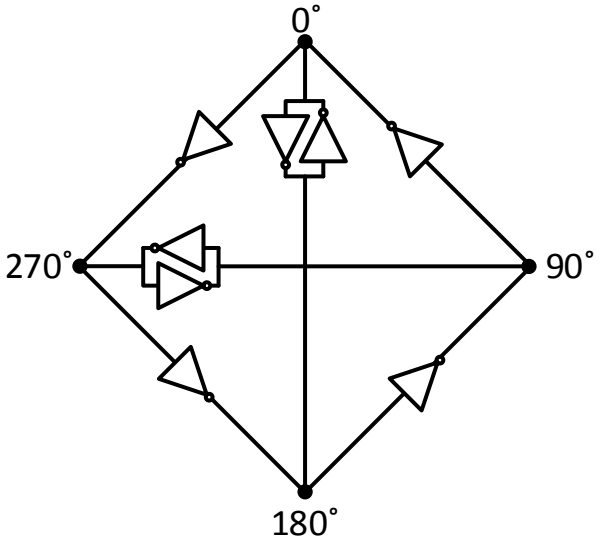



**Figure 3-11 – Quadrature four-stage ring oscillator [34].**

In contrast to a ring oscillator with an odd number of inverters, now two transitions are travelling through the ring. Therefore, the oscillation frequency in now given by Equation 3.11.

$$f_{osc} = \frac{1}{\tau_{Chain}} = \frac{1}{N * \tau_{Inverter}} \tag{3.11}$$

As there is a rising and falling transition ate any time, the single-ended quadrature ring oscillator draws a nearly constant supply current and minimises switching noise on supply lines.

To finally settle this chapter, [22] describes a way to use coupled ring oscillators, to generate accurate delays (with a resolution equal to an inverting buffer delay, divided by the number of rings). Figure 3.11 shows what it a two-dimensional array oscillator. The concept is to force numerous rings to oscillate at the same frequency. This way, each frequency can be evenly shifted in phase by an exact fraction of a buffer delay. Nevertheless, the oscillation frequency is controlled mainly by the number of buffers per ring regardless to the number of rings in the array. Additional output phases can be introduced, and the delay resolution will

improve just by adding rings to the array. This kind of array oscillator can be realized using both single ended or differential inverting buffer.

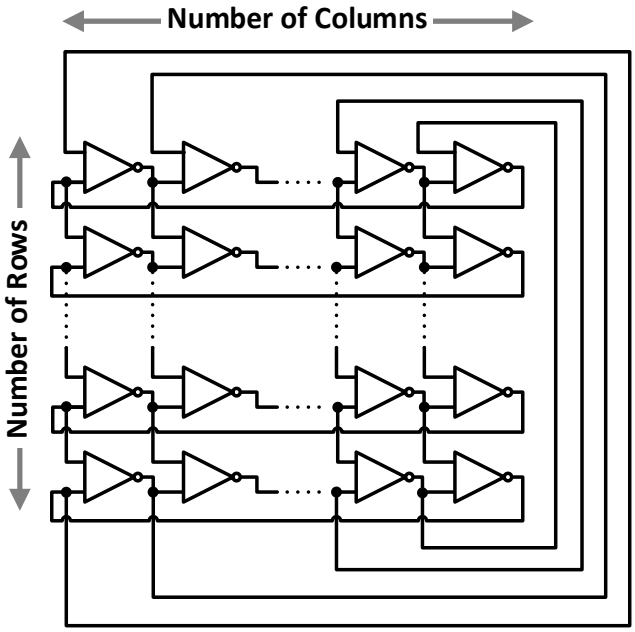



**Figure 3-12 – Two dimensional array oscillator [20].**

4

# 4 8 Phases Oscillator

## *4.1 Introduction*

In order to describe and validate the 8 Phases Oscillator, there is a need to begin with a background introduction and the reason that led this work to be done. In [11] it was started to be developed a discrete-time (DT), harmonic rejection (HR) mixer with the objective of relaxing the RF filter requirements and reducing the noise folding, as seen in [23]. Contemporary CMOS technologies have allowed effective discrete-time, switched-capacitor (SC), applications of RF receiver front-ends. To obtain decent Image rejection, accurate I and Q quadrature signals are essential [2, 24] so, as already studied in Chapter 2, it is possible to consider low-IF front-ends, to overcome some of the restrictions of the zero-IF approach (mainly flicker noise and DC offset).

When compared to active mixers, the passive Mixer/IIR filter used in [23], have the benefits of low power consumption when dealing with RF signals, and considerable smaller flicker noise (as there isn't any DC current) [2, 24]. But the central drawbacks of passive mixers is the lack of conversion gain, which disturbs the global gain and entire noise budgets for the whole receiver. To beat this limitation, [11] suggest to apply the MOS Parametric Amplifier (PA) technique to the Mixer/IIR filter proposed in [23].

Analog and DT SC mixing receiver designs from [23] can combine quadrature mixing for I/Q demodulation and wideband HR. Although, its circuit suffers from signal attenuation and forces higher gain and linearity requirements on the LNA. A charge-transfer low-pass (LP) SC filter [2] can be used, which includes a passive SC amplifier cascaded with a recursive SC filter (IIR), in order to amplify the signal amplitude. The circuit projected in [11] alone consumes 4.2 mW and occupies 0.11 mm2, without having the mixing stage into account. It also uses PA to increase the gain with reduced power and much lower area.

## 4.2 Downconverter Architecture

The SC downconverter offered by [11] associates quadrature (I/Q) mixing and wideband HR in the VHF-III band (174 to 248 MHz). In Figure 4.1 is possible to see the block diagram of the IC from where the 8 Phases Oscillator in study, was adopted. An input-driver containing a low-gain RF amplifier and two enhanced voltage-followers (EVFs) drives the fully-passive SC core circuit. Once the objective of this IC is only to measure the SC core circuit performance, it's possible to say that it have about 0 dB conversion gain and provides 50 Ω input matching. The SC downconverter core consists of three stages:

- An oversampler with fs = 8 fc (fs is the sampling frequency and fc the carrier frequency);
- Two I/Q DT mixers for downconversion;
- Two LP IIR filters.

At the output, there are four simple source-followers (SFs). And, finally, the main subject of this thesis, an on-chip local oscillator (LO) that provides the required 1/8 duty-cycled clock phases to drive the SC circuit presented in [11].

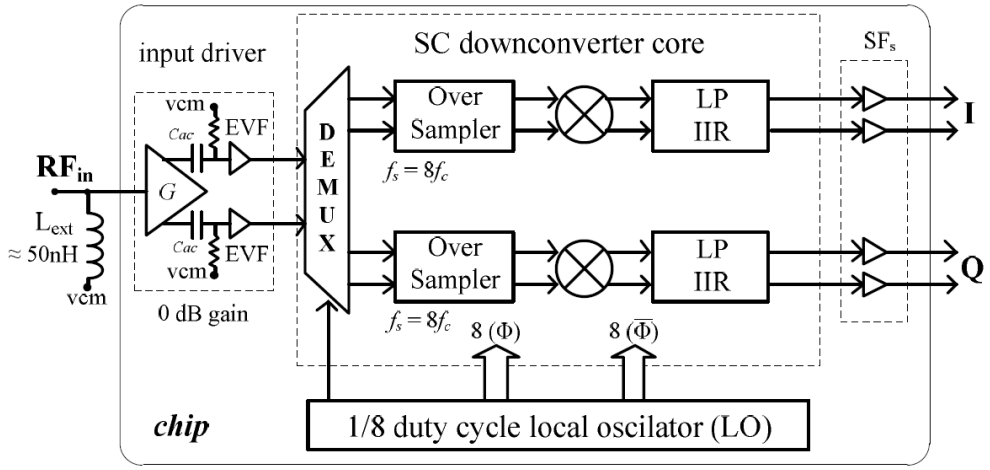



**Figure 4-1 – Block diagram of the implemented DT mixing circuit comprising the input driver, SC downconverter core and the LO (adopted from [11]).**

Figure 4.2 shows the oversampler/mixer/IIR circuit (SC core) which encloses eight time-interleaved sampling units (SU) controlled by an 8-phase non-overlapping clock with 12.5 % duty-cycle phases ϕ0 - ϕ7 (there is a total of 16 SUs in the differential implementation) produced by the LO.

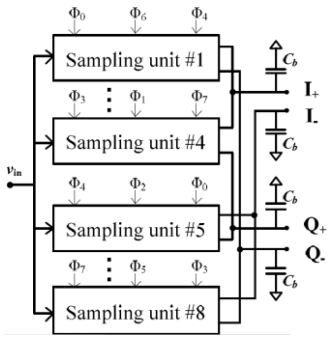



**Figure 4-2 – SC core of the downconverter (adopted from [11]).**

## *4.3 Circuit Blocks: Sampling Cell and Local Oscillator*

### 4.3.1 Sampling/IIR filter cell

Figure 4.3a shows a SU in detail, which embraces four NMOS I/O bootstrapped switches, driven by two clock-bootstrapping circuits (CBT), two NMOS switches, and two sampling capacitors. During fs, input switches turn ON, and the input signal is sampled into C1 and C2, while ϕm perform the mixing function and ϕr the reset one. The wanted IIR filtering is realised through the charge sharing between the sampling (C1, C2) and buffer capacitors (Cb). In [11], C1 and C2 were realised based on a double complementary NMOS (M1, M4) and PMOS (M2, M3) varactor structure, contrarily from [23], as shown in Fig. 4.3b. In order to reduce sensitivity to overlap parasitics, and, thus, getting the most out of the parametric gain, two internal terminals from the SU are left floating.

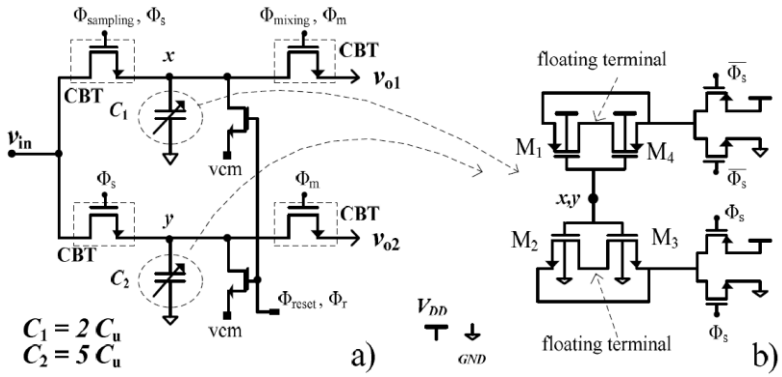



**Figure 4-3 – a) Schematic of a SU; b) MOS caps with embedded PA (adopted from [11]).**

The basic SC circuit works as follows: while the gates of the varactors are connected to the input (the drain terminals of M1, M4 and of M2, M3 are connected to VDD and VSS, respectively), it is called sampling phase (ϕs) and the varactors are operating in inversion mode. During the amplification phase, the four varactors have their gates connected to the output (the drain terminals of the PMOS and NMOS transistors are switched to VSS, and to VDD, respectively, forcing the varactors to operate in the depletion mode). Since the varactors capacitances drop when they move from inversion into depletion, it turns possible the parametric amplification (PA) [25].

### 4.3.2 The Local Oscillator

A LO based on an eight-phase ring oscillator is accessible on-chip (Fig. 4.4). It uses 16 current starved single-ended inverters. Eight in the main loop together with eight connected as latches, in between opposite nodes of the main loop.

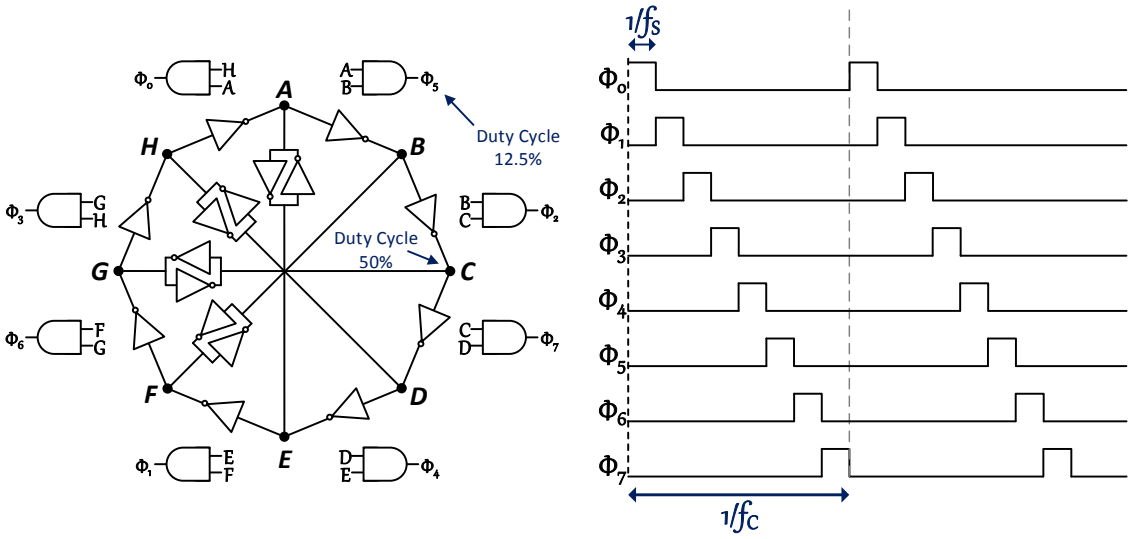



**Figure 4-4 – (a) Local oscillator; (b) 8-phase 12.5 %-duty-cycle wave forms.**

The multiple phase ring oscillator presented in [26] in addition with the four-phase ring oscillator in [27], resulted in this kind of topology for an 8-Phase Ring Oscillator. The frequency of oscillation is easily set just by adjusting the current through the inverters. All the inverters have the same dimensions, the PMOS/NMOS dimension ratio was adjusted for the better phase-noise results [11]. In Equation (4.1) is possible find the adopted ratio between $W_P$ and $W_N$, as a result of the need to have a balanced current that flows through the inverter PMOS and NMOS. To achieve the required clock duty cycles of 12.5 %, necessary for the receiver, NAND gates have

been used. This LO has a phase error below 1º in all eight phases [11], essentially avoiding phase overlapping, which is vital for proper mixing process.

$$\text{Considering } k_N = 3 * k_P, Vdsat_N = Vdsat_P \text{ and } L_N = L_P$$
$$\text{Then } I_{d_N} = I_{d_P} \Leftrightarrow \frac{1}{2} * k_N * \frac{W_N}{L_N} * {Vdsat_N}^2 = \frac{1}{2} * k_P * \frac{W_P}{L_P} * {Vdsat_P}^2 \Leftrightarrow \quad (4.1)$$
$$\Leftrightarrow k_N * W_N = k_P * W_P \Leftrightarrow \frac{W_P}{W_N} = 3$$

***NAND***

The conventional CMOS gate NAND has the configuration of the Figure 4.5. It is constituted by two blocks, a PMOS block (pull-up) and a NMOS block (pull-down). The output should be '0' only if the inputs control the NMOS block to connect the ground to the output. The same happens to the relation with PMOS, Vdd and the 'high' value of the output [28].

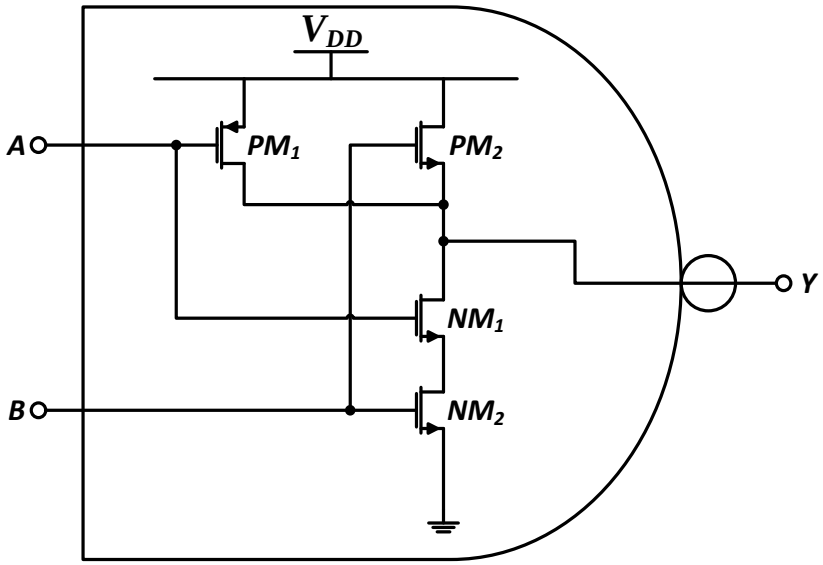



**Figure 4-5 – NAND gate schematic.**

So it is easy to understand that for this circuit to provide '0' at the output, it needs both inputs to be 'high', and if at least one of them is 'low' the output would be '1', as we can see, in the truth table (Table 4.1) of the theoretical NAND gate.

**Table 4.1 – Truth table of a NAND gate.**

| A | B | **Y** |
|---|---|---|
| 0 | 0 | **1** |
| 0 | 1 | **1** |
| 1 | 0 | **1** |
| 1 | 1 | **0** |

What to do next is considering the transistors dimensioning (PMOS/NMOS ratio adopted was 3). And the essential to get about this, as said in [28], a NAND with N inputs has a certain relation with the inverters studied before

$$(W/L)_{nNAND} = N * (W/L)_{nINV} \tag{4.2}$$

as NMOS relation and

$$(W/L)_{pNAND} = (W/L)_{pINV} \tag{4.3}$$

as PMOS relation.

In Figure 4.6 is possible to see how does the AND block create the 12,5% duty cycle with strategic 50% duty cycle inputs.

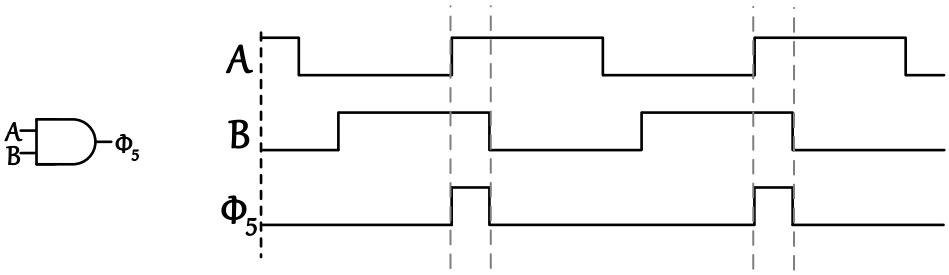



**Figure 4-6 – Transformation of 12,5% to 50% duty cycle wave.**

## *4.4 8 Phases Oscillator Architecture*

Regarding to the eight phases oscillator, before the presentation of the final architecture, it is important to mention the starting point, that is, the “basic circuit” that allowed the development of the present oscillator.

Indeed, Figure 4.6 shows the “initial” circuit that was the motto for the project later developed.

In this Chapter the most relevant premises associated to the configuration of the eight phases oscillator, were detailed with the maximum possible depth.

Thus, it would be redundant to emphasize considerations previously discussed. At this level, especially in this particular chapter, it is crucial to highlight the objectives related to the configuration presents, which led the basic circuit to a more robust architecture. From a practical point of view, the designation of the number of each phase, differs from the number regarding the phases that constitute Figure 4.4.

In other words, while in Figure 4.4, phases vary from $\phi_0$ to $\phi_7$, in terms of development were considered phases from $ph1$ to $ph8$ and the ones from A to H became out1 to out8. The phase inverted outputs are represented with the following approach: by adding the letter 'n' to the respective name of each output (Figure 4.6).

The main purpose of the first part of the present dissertation, consists of developing an eight-phase oscillator capable to operate for a 400 MHz to 1 GHz range.

Evidently, the realization of this goal required changes and optimizations of the circuit initially aforementioned.

To make absolutely clear all the most relevant decisions taken, it is fundamental to detail not just the set of options chosen, since the first stage of the present work, but also highlight the reason that led to the evolution of the circuit.

Thus, the original oscillator is related to the domain of another project [11]. Regardless this fact, let it be known that in that particular project was given only an example of realization for 400 MHz.

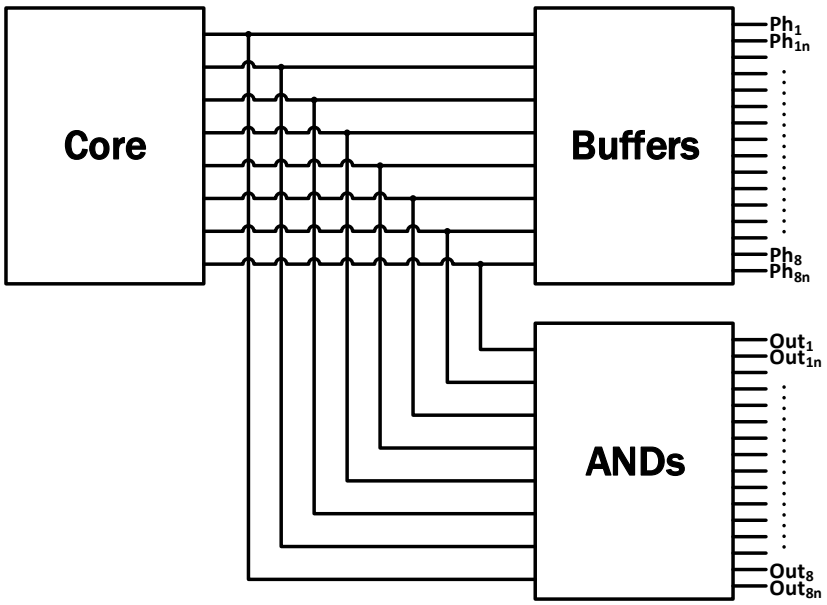



**Figure 4-7 – Oscillator Core plus AND and Buffer blocks in a block diagram.**

It was considered relevant to carry out the study of this particular oscillator, for a couple of reasons: not only because on a past subject of the course (“Oscillators and PLLs”) was developed an eight phase clock oscillator that functioned approximately in 630 MHz range, but also because it was a firm conviction that it was possible to evolve the circuit in order to operate for a 1 GHz range.

## *4.5 8 Phases Oscillator Sizing*

After presenting the global architecture, it is time to detail its constitution, that is, individualize every single relevant element, present in the circuit.

Out of respect to the work previously developed by colleagues, design process of past project was considered.

### 4.5.1 Inverters

Taking into consideration this fact, Figure 4.7 is shown, related to Outside and Inside Ring Inverters.

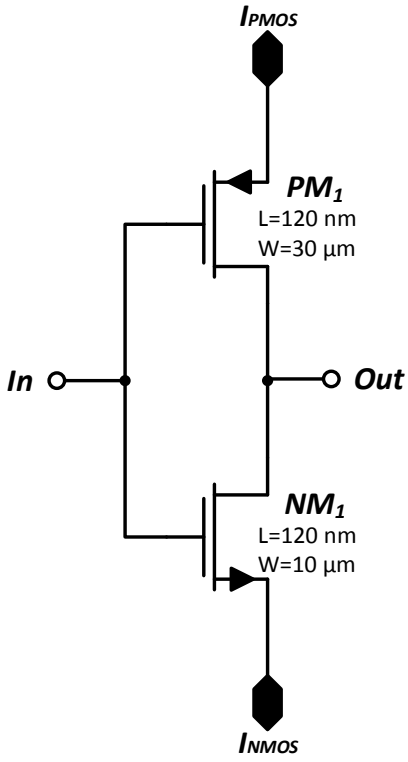



**Figure 4-8 – Inverter block schematic.**

To reach the main goal (realization for 1 GHz range), as mentioned before, was considered sizing that guarantee full operation of the circuit for a frequency of 400 MHz in [11].

Moreover, one relation $W_{pmos}/W_{nmos}$ = 3.5 with W = 10$\mu m$. For this initial design, was chosen L = 240 $nm$.

Further, in order to study the behaviour of the circuit with the most possible certainty, it was investigated the influence of the increase/decrease of the values of W's, by setting to 3, the relation $W_{pmos}/W_{nmos}$. Through the visualization of Figure 4.7, it is possible to confirm the relation previously expressed. To be more precisely, $W_{pmos}$ = 30 $\mu m$ and $W_{nmos}$ = 10 $\mu m$.

The value of L is 120 $nm$, which represents the standard value for $L_{min}$ in 130 nm CMOS technology, increasing in this way the velocity of the circuit to its maximum.

### 4.5.2 Buffer

Next, it is presented the architecture associated to the buffer used for 50 % duty cycle outputs. Duty cycle and phases that were already discussed in the present chapter.

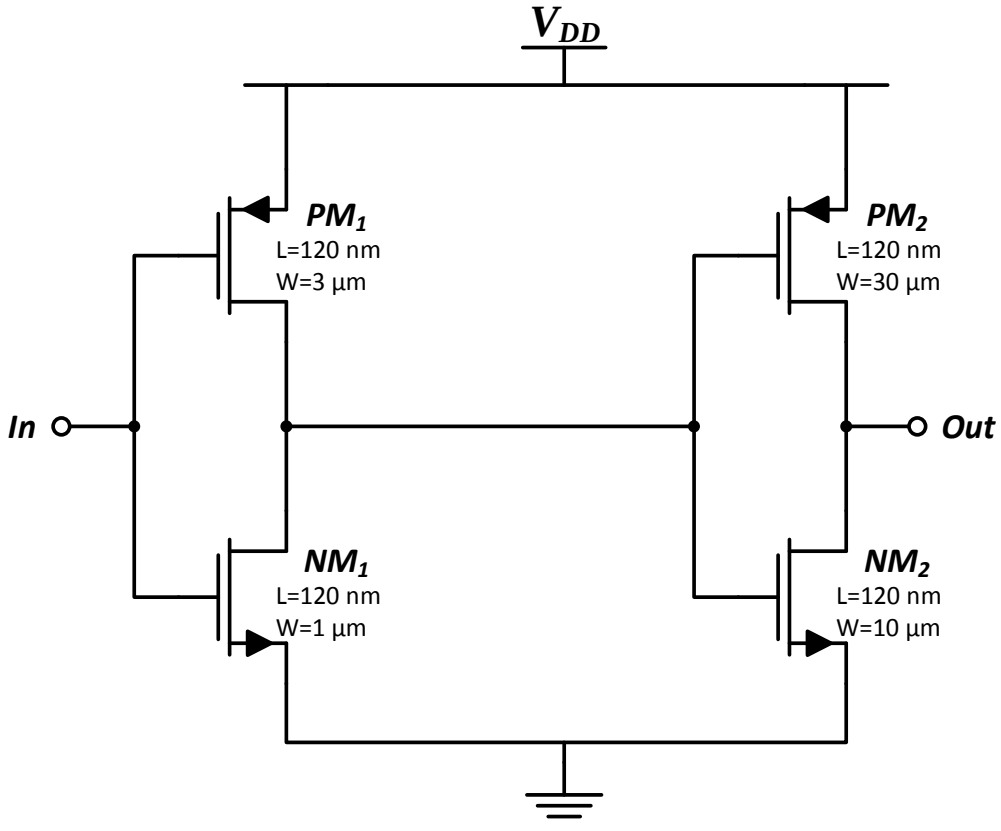



**Figure 4-9 – Buffer block schematic.**

Regarding to the constitution of the buffer, were designed two relations.

The first one is equal to the aforementioned relation. However, in terms of the second relation, although $W_{pmos}/W_{nmos}$ stays equal to 3, W = 1 $\mu m$.

Regarding to the relation between the two cascaded inverters, the theoretical considerations taken into account, suggested a very objective approach.

Basically, the recommended idea consists of adopting a chain of multiple cascaded inverters. In this sense, obviously it was decided to follow this strategy.

In [35] it is said that, for a given load, $C_L$, a given input capacitance, $C_{in}$, and a given number of stages N, one can find the optimal multiplicity factor, M, through the Equation (4.4).

$$C_L = M^N * C_{in}$$
$$200fF = M^2 * 2{,}1fF \iff M = \sqrt{\frac{200fF}{2{,}1fF}} \iff M \simeq 10 \quad (4.4)$$

By analysing Figure 4.8 and Equation (4.4), we can identify a multiplicity equals to 10. In other words, the size of W's of the next cascaded inverter is, indeed, greater 10 times the previous cascaded inverter (1 $\mu m$ -> 10 $\mu m$ and 3 $\mu m$ ->30 $\mu m$).

This multiplicity actually offers important advantages, especially in terms of rising/fall, in order to increase its speed.

This is why it is fundamental to choose higher sizes regarding to the second inverter, not just to make the aforementioned advantage a reality, but also increase the isolation.

Regardless the fact that the capacitive load associated to these outputs, is approximately 200 fF, it was decided to embrace cascaded inverters, also to cover eventually higher values in terms of the capacitance of the load, and to be sure that the circuit is properly isolated.

### 4.5.3 AND

In this particular chapter, it is crucial to analyse the sizing of the AND block, which is represented in Figure 4.9.

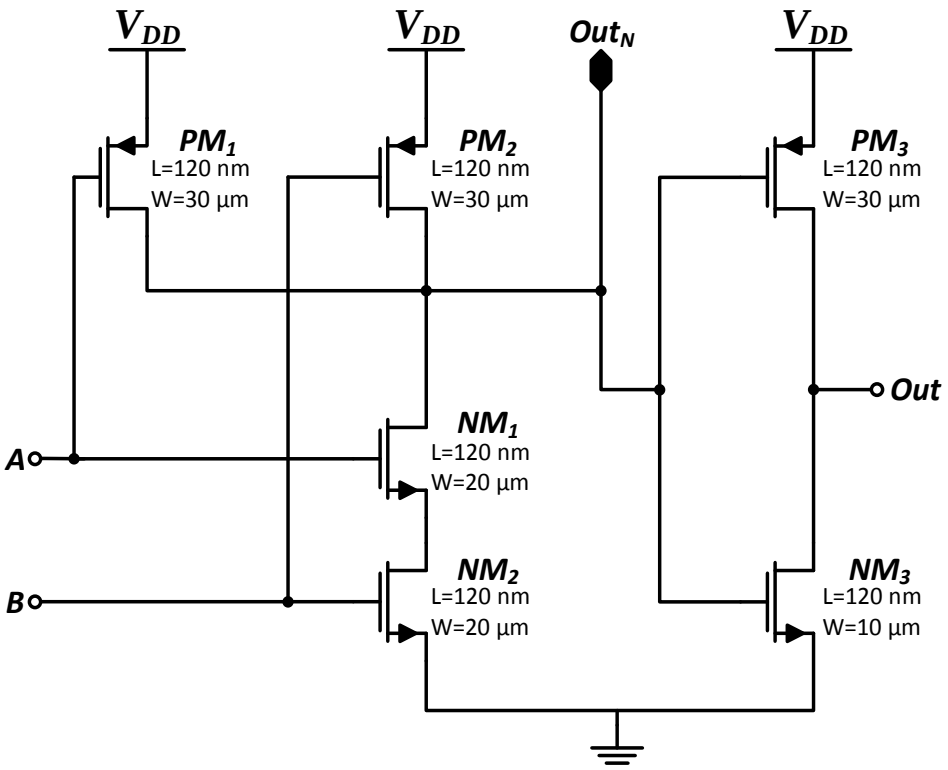



**Figure 4-10 –AND block schematic.**

In terms of the constitution of the AND block, it is fair to say that it is a consequence of the denial of an NAND (phase inversion).

Moreover, as we can see in Figure 4.9, the denial is done by an inverter already detailed, and previously discussed.

Again, when discussing the architecture of the NAND, it is mandatory to note that there was necessary to fulfil a relation previously known in the literature.

This means that, in order to the NAND present two inputs, by setting L = 120 nm for all of the transistors, the relation W/L of transistors NMOS, must be necessarily the double of relation (W/L) of inverter NMOS transistors.

This consideration explains the design process carried out, as we can see in the previous Figure, that is, $W_{nNAND}$ = 20 $\mu m$, $W_{nINV}$ = 10 $\mu m$.

After making clear the design associated to the architecture that constitutes an AND, it is worth to emphasize the relevant role that AND played in the transformation of the two signals, that is, not only with a duty cycle of 50 per cent, but also with a duty cycle of 12.5 per cent.

Initially, by mistake, and as we can confirm by analysing Figure 4.9, it was directly connected the “OutN” output of the AND (corresponding to the signal of a duty cycle of 87.5 %, that is, the denied signal with duty cycle of 12.5 %) to the oscillator load output.

This connection resulted in unwanted delays (rising/fall), and in a difficulty to reach operating frequencies of interest.

Thus, to overcome the constraints indicated, it was decided to add the inverter (Figure 4.7) in output named “Out” of the AND cell, in order to obtain the denied phase in regard to the signal with a duty cycle of 12.5 %, and not before that one.

### 4.5.4 Current Mirrors

Finally, the design of transistors that realize the current mirrors.

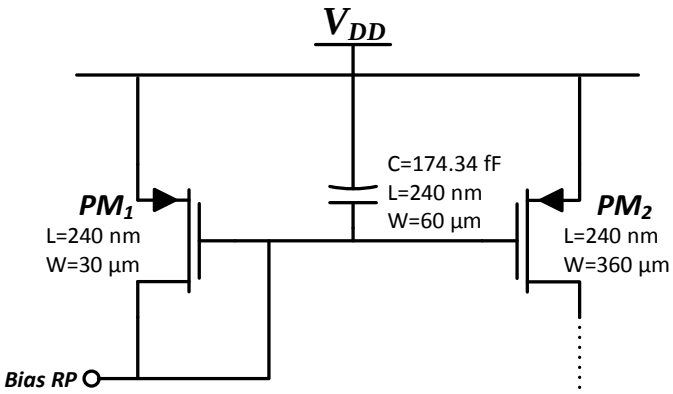



**Figure 4-11 – PMOS Current Mirror block schematic.**

Since there is a necessity of generate more current, it is determinant to increase the size of W of both current mirrors (PMOS and NMOS).

Figure 4.10 concerns to the first current mirror, and initially was chosen W = 300 $\mu m$. But given the fact that the main purpose is to increase the current, this value turned out to be small. Having said that, is decided to increase the size to W = 360 $\mu m$.

Concerning to the second current mirror, NMOS, the procedure is similar. The first sizing (W = 100 $\mu m$) also revealed to be small, and only a W = 120 $\mu m$ was considered a satisfactory result.

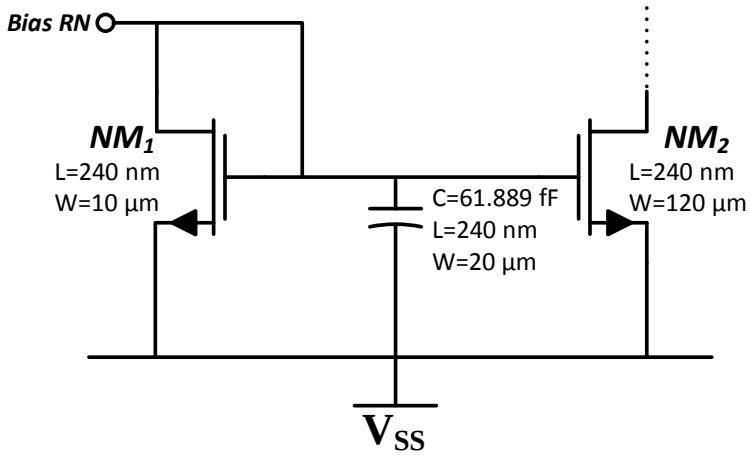



**Figure 4-12 – NMOS Current Mirror block schematic.**

With regard to the design of the current mirrors, it is important to mention that the addition of a capacitor was considered (decoupling capacitor). Moreover, between the node of the respective mirror and the ground, with a very clear purpose:

To filter not only the crosstalk noise, as well as EMI (Electromagnetic Interference).

All theoretical considerations concerning the aforementioned interferences, are explained in [29].

By analysing Figure 4.11 it is possible to confirm the value of the capacitor, which is $61.89$ fF, and the justification for this particular value, is based on the same logic supported and defended in previous points of this chapter.

This means that the relations $\mathrm{Wpcap} = 2 * \mathrm{Wpinv} = 30\ \mu m * 2 = 60\ \mu m$ and $\mathrm{Wncap} = 2 * \mathrm{Wn_{inv}} = 10\ \mu m * 2 = 20\ \mu m$, led to insignificant capacitances.

Nevertheless, in terms of fulfil the objectives already discussed, the values obtained are perfectly effective.

5

# 5 Simulation and Measurement Results

## *5.1 Schematic Simulations*

With regard to the chapter Simulation Results, will be dedicated a specific sub-chapter to discuss all the assumptions related to the layout and post-layout. The simulations were made with Cadence Spectre RF using BSIM3v3 for a 130 nm MOS technology.

That said, it is crucial refer that two types of simulations were made: the first type concerns exclusively to the schematic itself, and the second one that though inaccurately, will be called as the simulation with the extraction of the parasitics, that will be presented in greater depth in future sub-chapter.

At this level and in the first place, the achieved results are presented below through the simulations of the schematics.

From the point of view of the objectives, was intended to obtain two types of sequential outputs, each of them referring to the one of the duty cycles previously discussed.

The Figure 5.1 concerns to the signal of each of the eight sequential phases, with duty cycle of 12.5 %, while the Figure 5.2 is related to the duty cycle of 50 %.

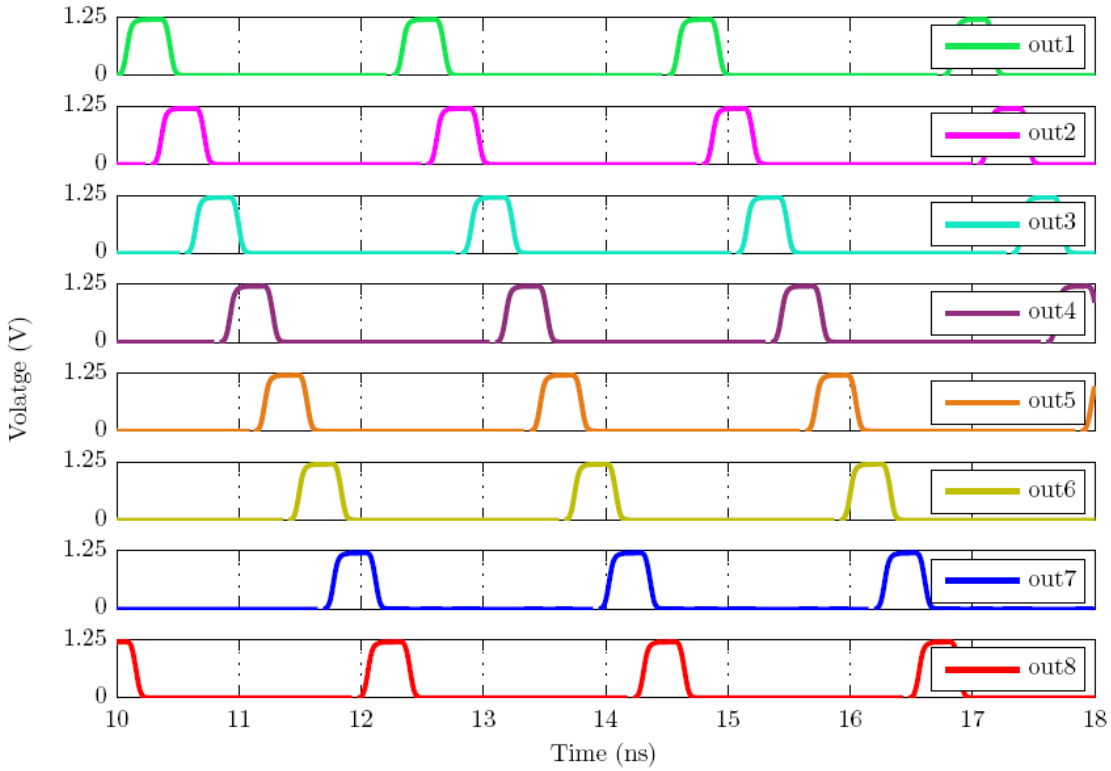



**Figure 5-1 – Schematic sequential signals with duty cycle of 12.5 %.**

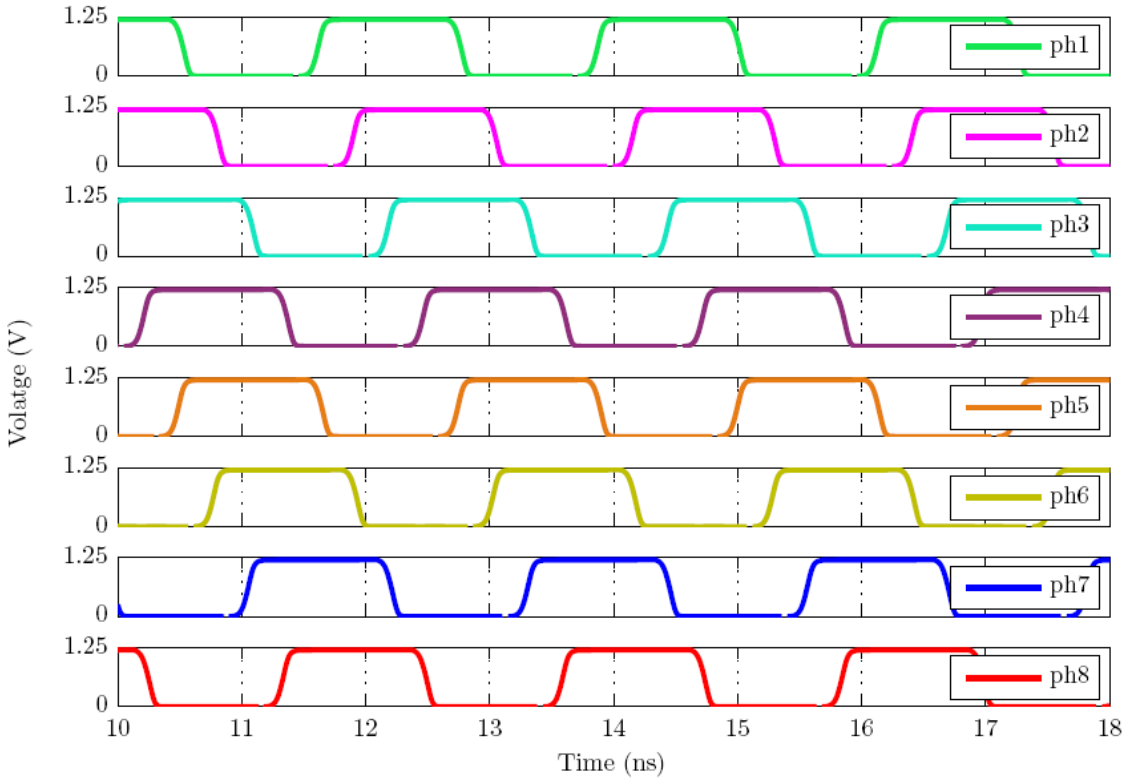



**Figure 5-2 – Schematic sequential signals with duty cycle of 50 %.**

The Figures 5.1 and 5.2 make clear that there are sequential follow of each of the eight phases. In addition to the purpose, associated to the two types of the indicated signals, it was analysed the performance of another specific purpose: with $200\ fF$ load, that represents the estimated value of the inputs which the oscillator is attached to, with the aim of ensuring the rising time, in the output signals of the oscillator, less than $100\ ps$.

$$t_s = t_d \ll \frac{1}{N * f_{MAX}} = \frac{1}{8 * 1 * 10^9} = 125\ ps$$
$$100\ ps < 125\ ps \ll 1ns \tag{5.1}$$

Consequently, and as we can see in eq. (5.1), this limits the times of the rising/fall, to a value much lower than the maximum period that certain system will support. Thus, it is assumed that a value 10 times lower than $1\ ns$ will be a much lower value. This way, a safety level sufficiently comfortable is resulted, so as to be possible ensure the proper functioning of the mixer and the parametric amplification.

### 5.1.1 12.5 % Duty Cycle

Initially, the referred rising time was explored/ensured for a frequency of 900 MHz, where this analysis ended up being transversal for a frequency range of 400 MHz to 900 MHz.

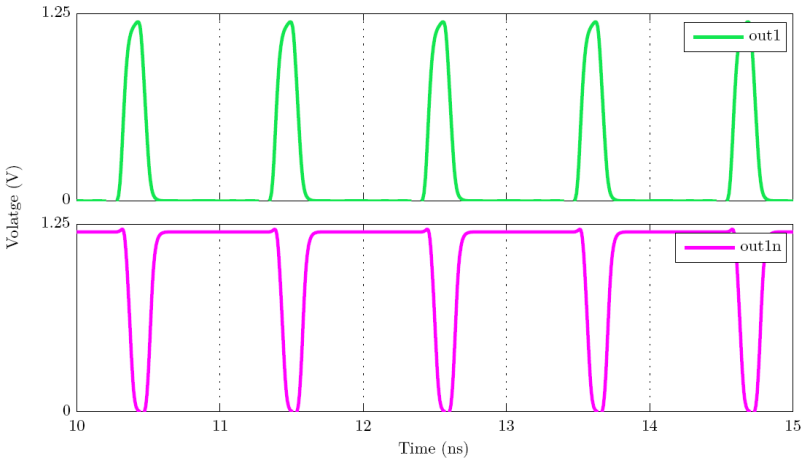



**Figure 5-3 – Schematic simulations of the signals with duty cycle of 12.5 % at 900 MHz, in-phase and in phase inversion.**

For this simulation, at frequency of 900 MHz, it was necessary to adjust the biasing resistance to 1.5 KΩ, giving a total current consumed of 16.76 mA. Note that, strictly speaking, the associated frequency is of 938.7 MHz.

Through this calibration, as the image itself suggests, it has become possible to fulfil the requirements.

In the Figures 5.4 and 5.5, are presented images concerning the simulations for the other frequencies, already mentioned previously.

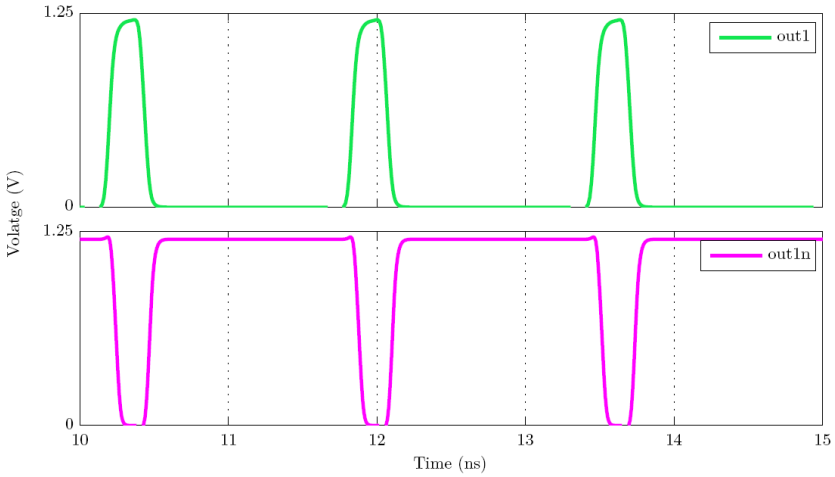



**Figure 5-4 – Schematic simulations of the signals with duty cycle of 12.5 % at 600 MHz, in-phase and in phase inversion.**

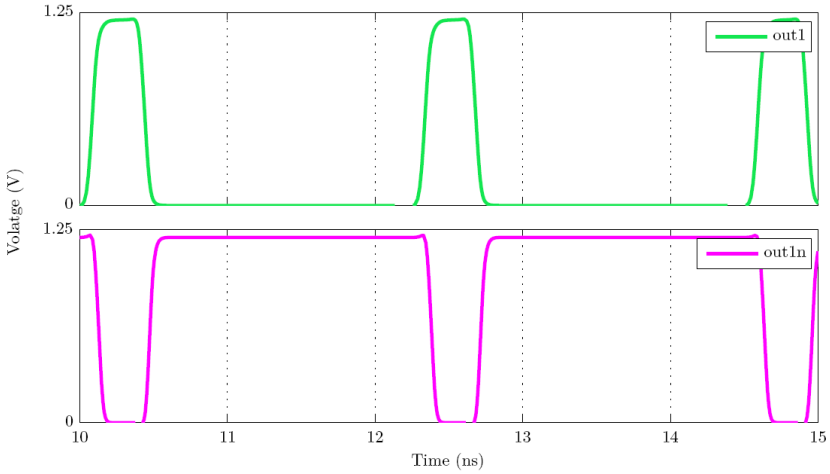



**Figure 5-5 – Schematic simulations of the signals with duty cycle of 12.5 % at 400 MHz, in-phase and in phase inversion.**

The conclusions to be drawn are similar to the ones described about the 900 MHz frequency.

The Figure 5.4 regards to the frequency in the range of 600 MHz, more precisely 613.6 MHz, where the biasing resistance associated was readjusted to 4 KΩ, and total current consumed is 11.97 mA.

Finally, regarding to the Figure 5.5 analogously to the previous considerations, the frequency at issue is of 446.2 MHz and biasing resistance was calibrated to 7.2 KΩ, giving the total current consumption of 9.946 mA.

To make more obvious, all these results are presented in Table 5.1.

**Table 5.1 – Summary of signal characteristics for schematic simulations.**

| Resistor | Frequency | Current consumption | Duty cycle 12.5 % | | Duty cycle 50 % | |
|---|---|---|---|---|---|---|
| | | | Rise/Fall time (ps) | Phase inversion (ps) | Rise/Fall time (ps) | Phase inversion (ps) |
| 7.2 KΩ | 446.2 MHz | 9.946 mA | 79.38/73.26 | 59.73/58.8 | 108.9/103.6 | 110.9/103.9 |
| 4 KΩ | 613.6 MHz | 11.97 mA | 73.25/68.56 | 59.6/57.96 | 104.7/97.27 | 103.1/95.86 |
| 1.5 KΩ | 938.7 MHz | 16.76 mA | 66.88/65.76 | 58.53/57 | 95.53/88.23 | 93.35/87.77 |
| 5 Ω | 1.516 GHz | | | $N/A$ | | |

All these simulations refer only to a duty cycle of 12.5 %. Clearly, there was a need to do the same for a duty cycle of 50 %.

### 5.1.2 50 % Duty Cycle

Regardless of the associated duty cycle, it must be said that the oscillation frequency of the circuit is the same for both cycles.

For that reason, and avoiding redundancy of the concerned chapter, even because the current consumption and biasing resistance already were presented and properly discussed, only results referring to the times of the rising/falling will be revealed.

Thus, for the duty cycle specified, the subsequent figures corresponding to the simulations for the three frequencies are presented.

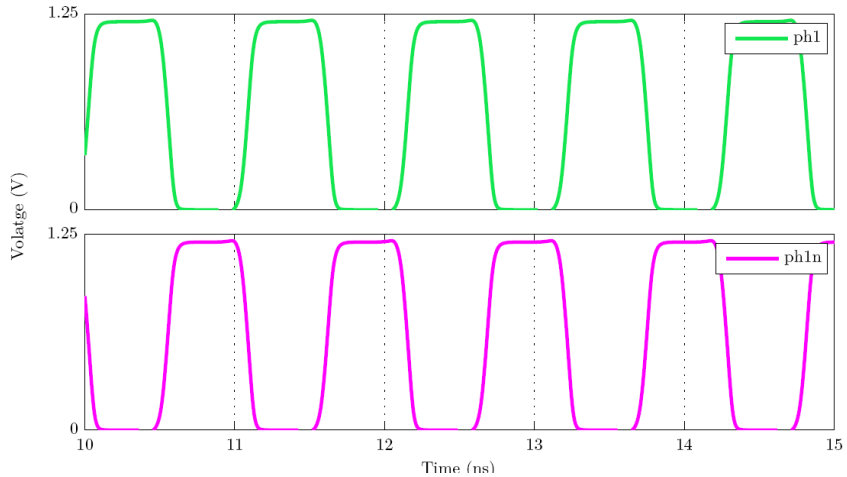



**Figure 5-6 – Schematic simulations of the signals with duty cycle of 50 % at 900 MHz, in-phase and in phase inversion.**

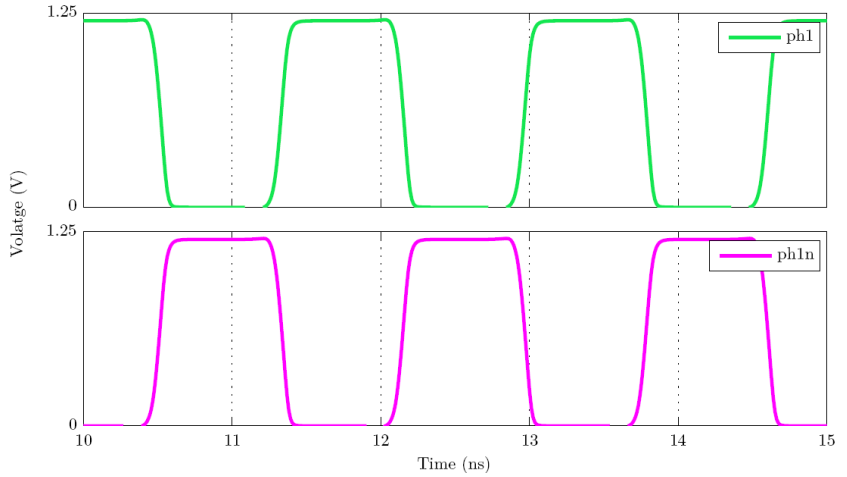



**Figure 5-7 – Schematic simulations of the signals with duty cycle of 50 % at 600 MHz, in-phase and in phase inversion.**

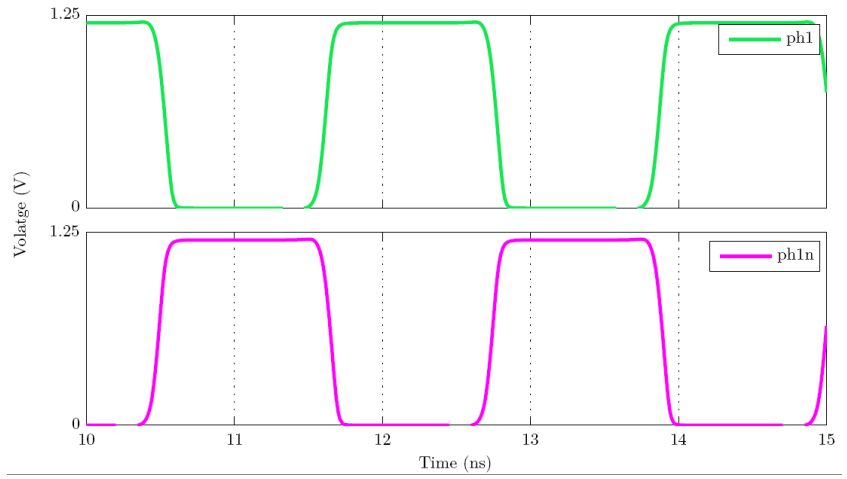



**Figure 5-8 – Schematic simulations of the signals with duty cycle of 50 % at 400 MHz, in-phase and in phase inversion.**

Once again, it is perfectly clear that the required specifications, in order to connect to the receiver, were achieved.

### 5.1.3 Phase Noise

The Phase Noise was simulated through Cadence and was set to give the result for the offset of 10 MHz in a range of relative frequencies from 100Hz to 100MHz

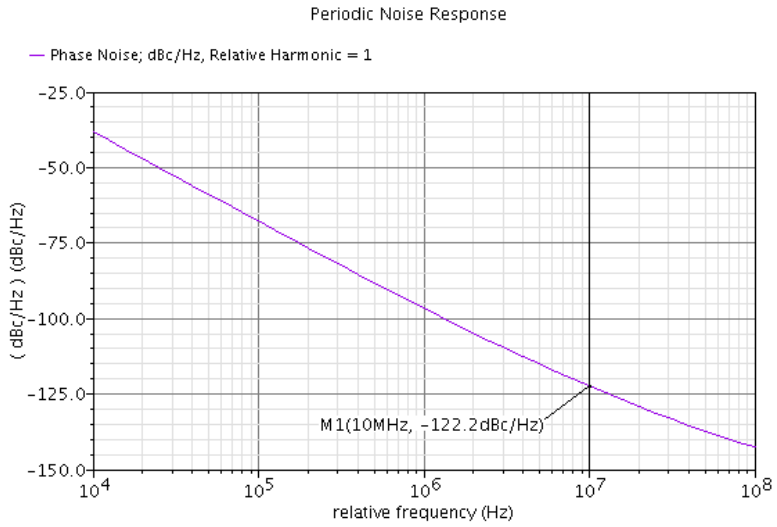



**Figura 5-9 Phase Noise of the oscillator at 900MHz oscillating frequency.**

After results of the schematic simulations having been discussed, it is relevant and necessary to introduce the layout of the developed circuit.

## *5.2 Layout*

This section focuses on the layout of the studied circuit, represented in Figure 5.13, where are performed some physical verifications. The physical verifications are the design rule check (DRC), the layout versus schematic (LVS) and the layout parameter extraction (LPE), where is verified if the design of the layout circuit is correct and robust [30, 31]. These verifications are done through the software Caliber from Mentor Graphics Then, are accomplished and demonstrated some post-simulations plots which are more realistic because of the inclusion of

RC parasites. Thus, the post-layout results are compared with the schematic simulations results after the Table 5.2. This comparison is inevitable to understand, if in terms of circuit's implementation and design, the choices that were made allow the circuit to work in more realistic circumstances [15].

Resorting to the Cadence, was possible to accomplish the full Layout shown in Figure 5.13, is composed by the current mirror (shown at the Figure 5.9 and represented as the letter 'M' in Figure 5.13) that is responsible by setting the same current for the current-starved inverters (Figure 5.12) from the oscillators' core (C from Figure 5.13).

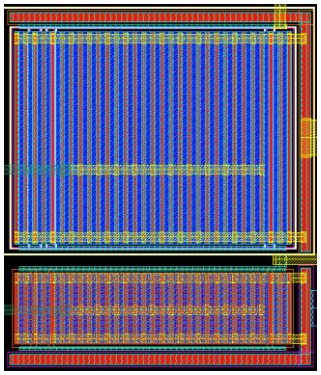


**Figure 5-10 – Current mirror layout.**

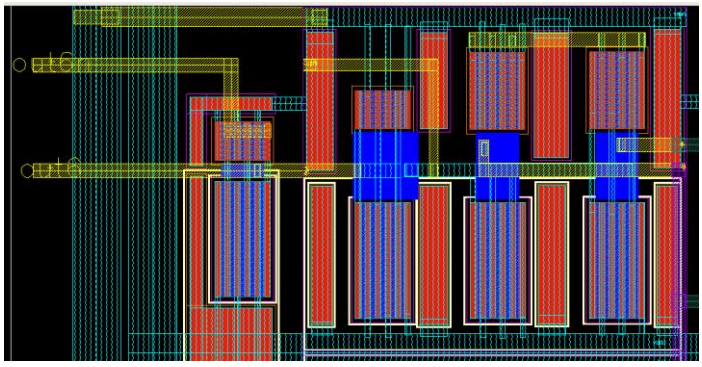


**Figure 5-11 – NAND layout.**

Buffer and NAND blocks are represented by the letter 'B' and 'N' from Figure 5.13 and are shown in Figures 5.11 and 5.10 respectively.

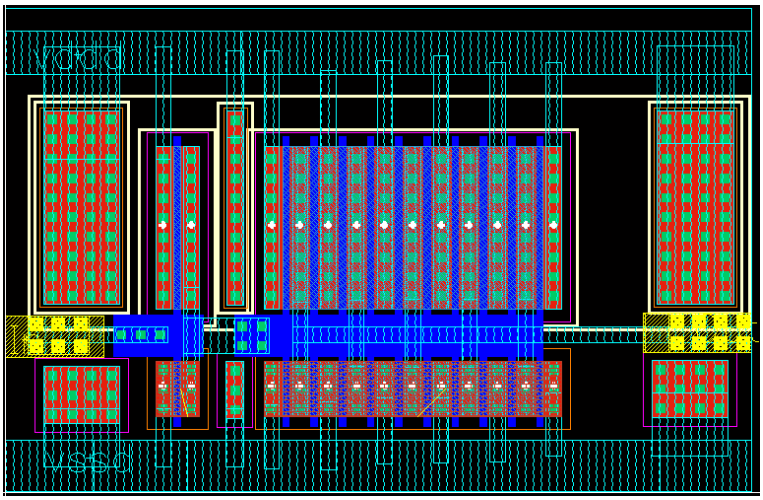


**Figure 5-12 – Buffers layout.**

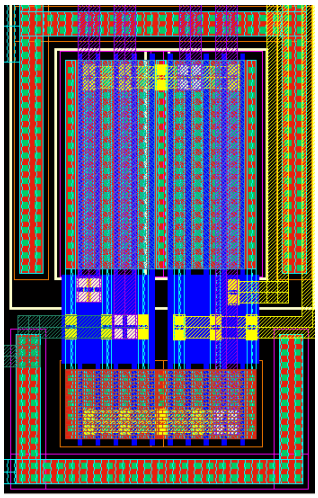


**Figure 5-13 – Inverters layout.**

It all makes a total die area of 165x83 $\mu m^2$. The devices that are connected were properly adjacent positioned in the whole circuit layout, in order to have perfect simetry and vias with equal vias. In order to guarantee the current flowing through the circuit, the maximum current density values are defined by the dimensioning of the widths of the metal connections and the number of contacts and vias [15].

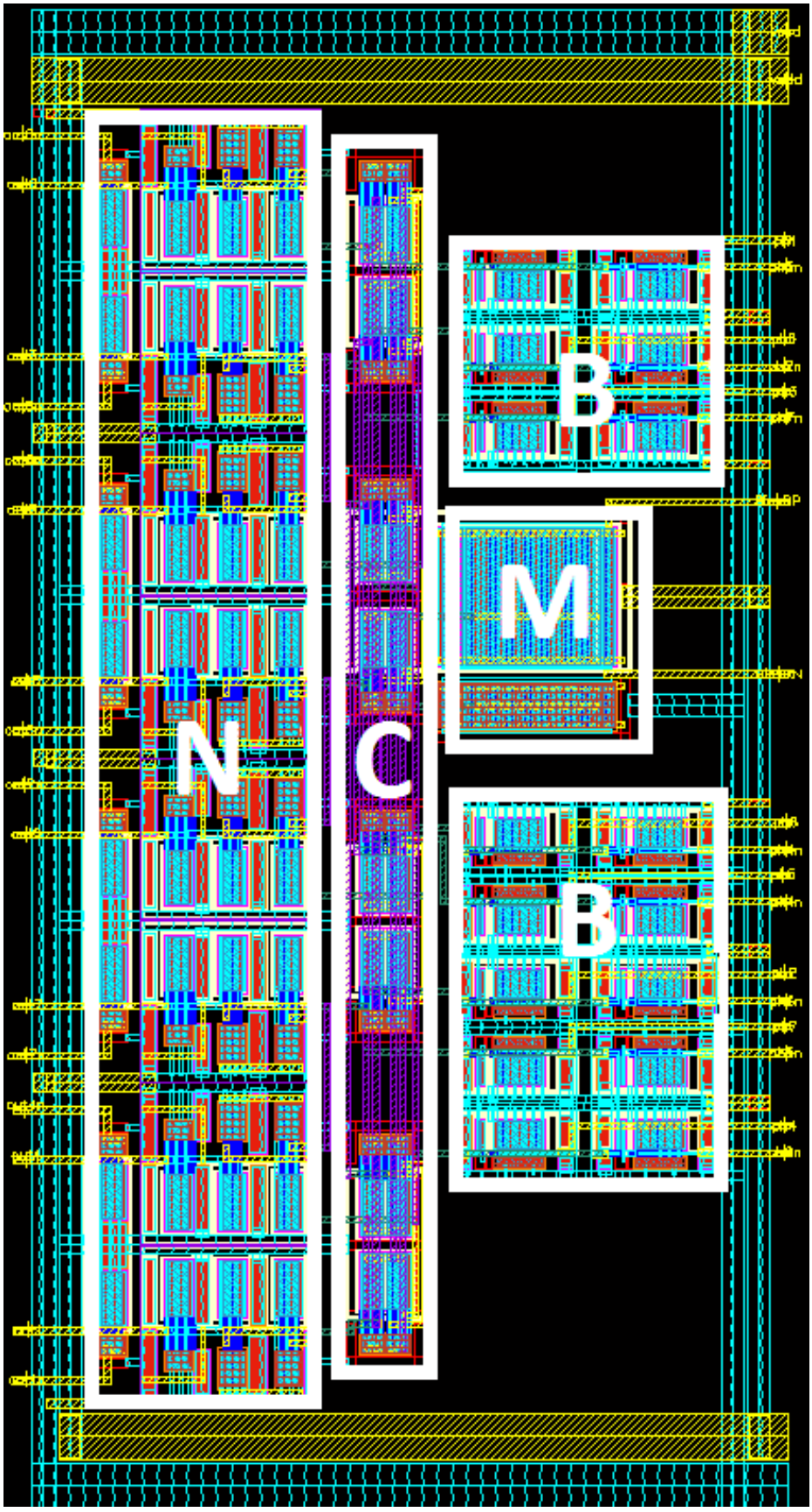



**Figure 5-14 – Layout of the 8-Phases Ring Oscillator (165 x 83 µm$^2$).**

Given the fact that it is impossible to simulate the layout, there was the need to adopt a strategy that allowed, even indirectly, the evaluation of the performance of the circuit, as close to the real model as possible.

Through the tool known as Parasitic Extraction [32] (this tool implicates the respect of a set of rules that will not be discussed), it was possible to proceed to the simulation (all the parasitic elements, such as resistances, capacitances of layout traces, coupling capacitances were considered).

Below it is shown the simulations associated to post-layout. The procedure used to these simulations were exactly the same as previously discussed, when referring to the schematic.

## *5.3 Post-Layout Simulations*

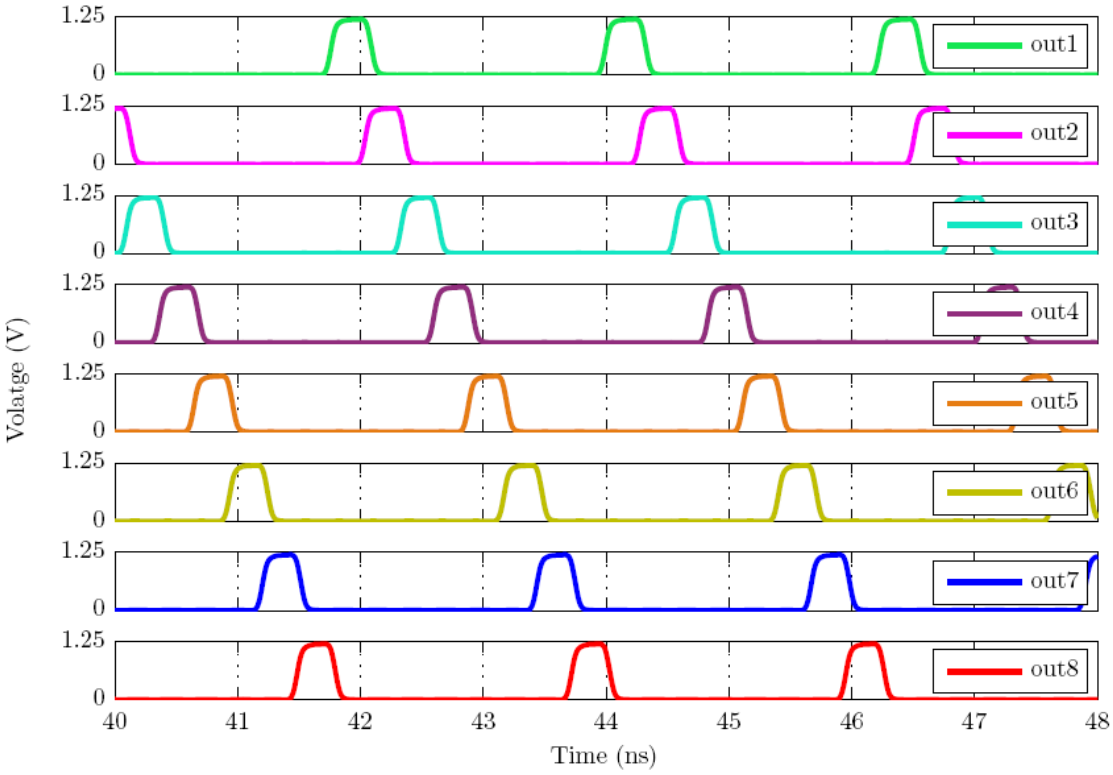



**Figure 5-15 – Calibre sequential signals with duty cycle of 12.5 %.**

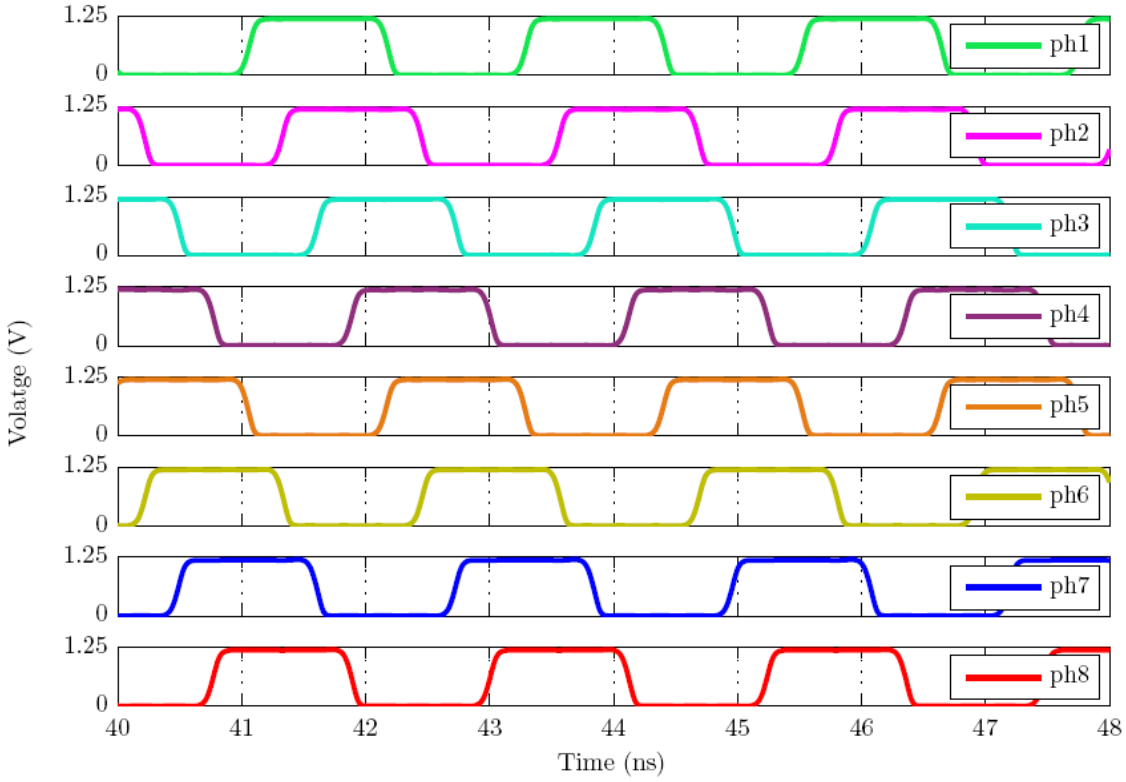



**Figure 5-16 – Calibre sequential signals with duty cycle of 50 %.**

If we establish a comparison between Figures 5.10 and 5.11 (images of the two duty cycles of calibre simulations) and Figures 5.1 and 5.2, the existing difference is not totally clear. For this reason, in order to highlight the existing differences are shown the Figures 5.12 to 5.17. The specifications enunciated in the beginning of the present chapter, stay mandatory, that is, the need to guarantee a rise/fall of the output signals of the oscillator less than 100 ps.

### 5.3.1 12.5 % Duty Cycle

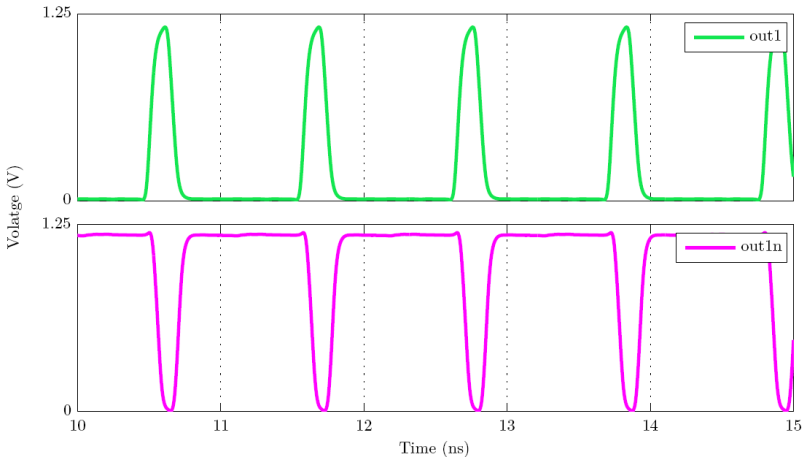



**Figure 5-17 – Calibre simulations of the signals with duty cycle of 12.5 % at 900 MHz, in-phase and in phase inversion.**

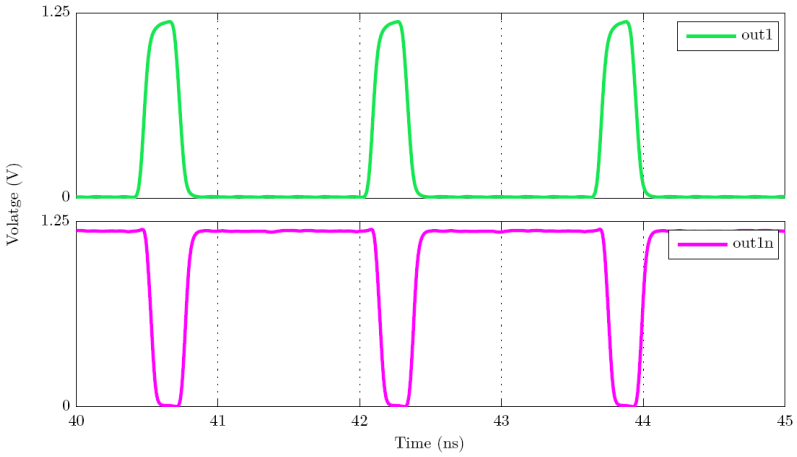



**Figure 5-18 – Calibre simulations of the signals with duty cycle of 12.5 % at 600 MHz, in-phase and in phase inversion.**

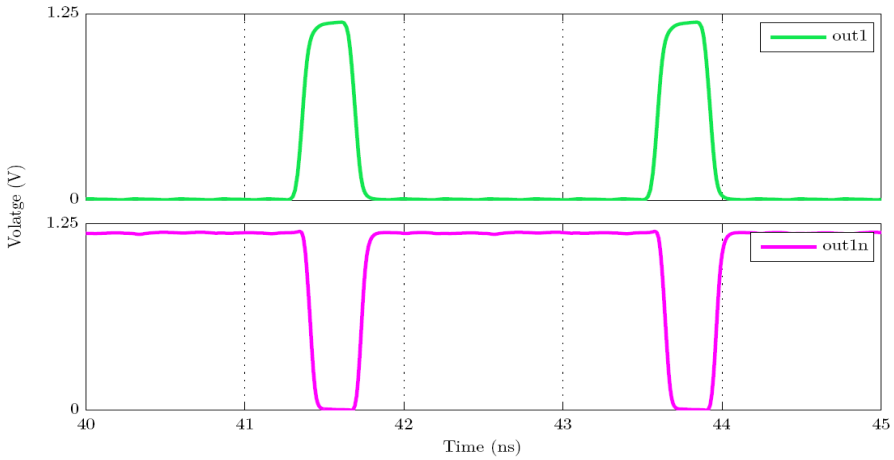



**Figure 5-19 – Calibre simulations of the signals with duty cycle of 12.5 % at 400 MHz, in-phase and in phase inversion.**

### 5.3.2 50 % Duty Cycle

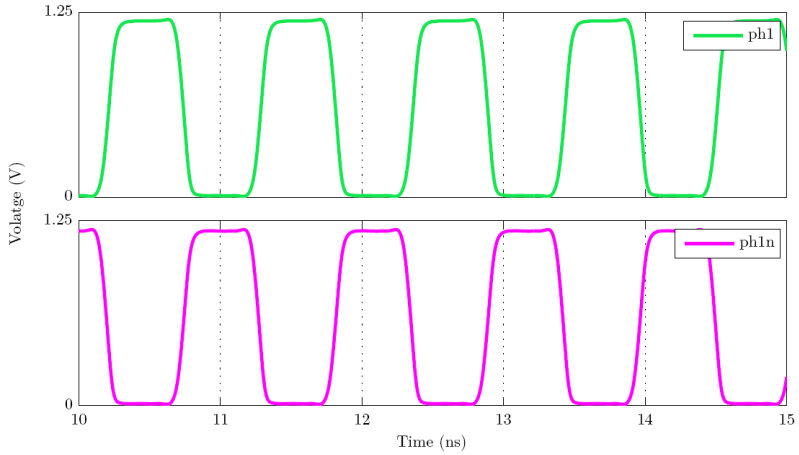



**Figure 5-20 – Calibre simulations of the signals with duty cycle of 50 % at 900 MHz, in-phase and in phase inversion.**

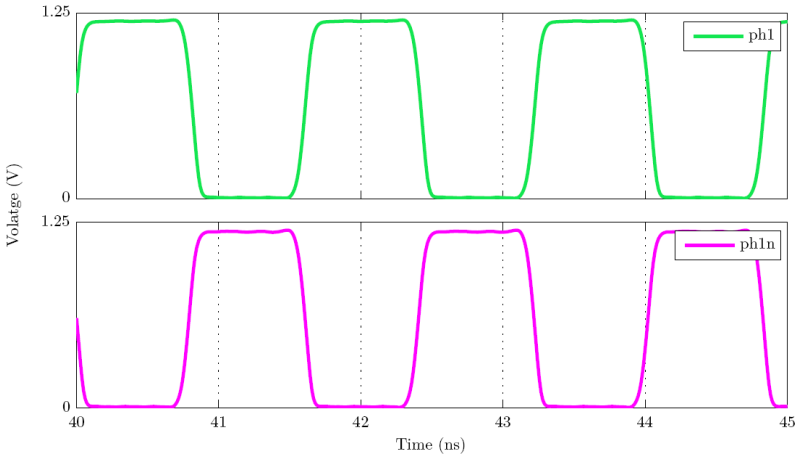



**Figure 5-21 – Calibre simulations of the signals with duty cycle of 50 % at 600 MHz, in-phase and in phase inversion.**

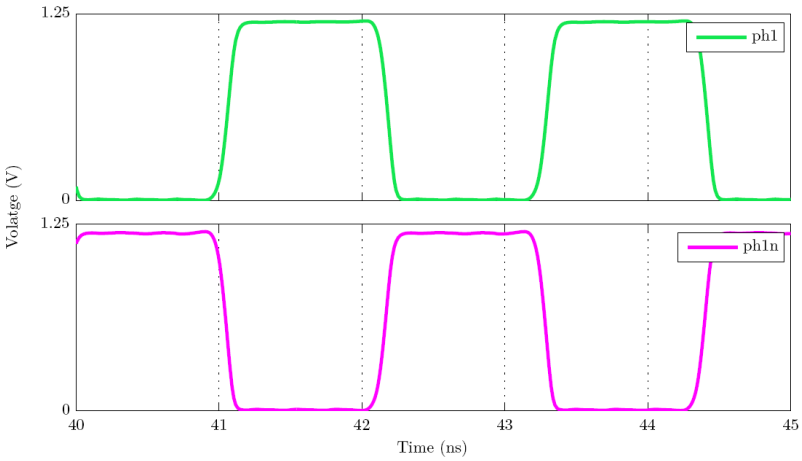



**Figure 5-22 – Calibre simulations of the signals with duty cycle of 50 % at 400 MHz, in-phase and in phase inversion.**

Considering the results obtained, the Table 5.2 presents the values of the current consumption, biasing resistance, rise/fall and the oscillation frequency for both simulations carried out.

**Table 5.2 – Summary of signal characteristics for calibre simulations.**

| Resistor | Frequency | Current consumption | Duty cycle 12,5% | | Duty cycle 50% | |
|---|---|---|---|---|---|---|
| | | | Rise/Fall time (ps) | Phase inversion (ps) | Rise/Fall time (ps) | Phase inversion (ps) |
| 4.5 KΩ | 447.6 MHz | 9.82 mA | 87.55/81.38 | 68.59/66.48 | 122.4/111.5 | 121.7/110.8 |
| 2.2 KΩ | 619.9 MHz | 12.32 mA | 82.8/78.4 | 68.27/65.36 | 114.2/104.6 | 114.1/104.7 |
| 0.5 KΩ | 930.1 MHz | 17.54 mA | 79.16/76.66 | 69.2/66.37 | 107.9/95.78 | 107.4/96.02 |
| 5 Ω | 1.081 GHz | | | $N/A$ | | |

### 5.3.3 Phase Noise

The pos-layout Phase Noise was simulated through Cadence and was set to give the result for the offset of 10 MHz in a range of relative frequencies from 100Hz to 100MHz

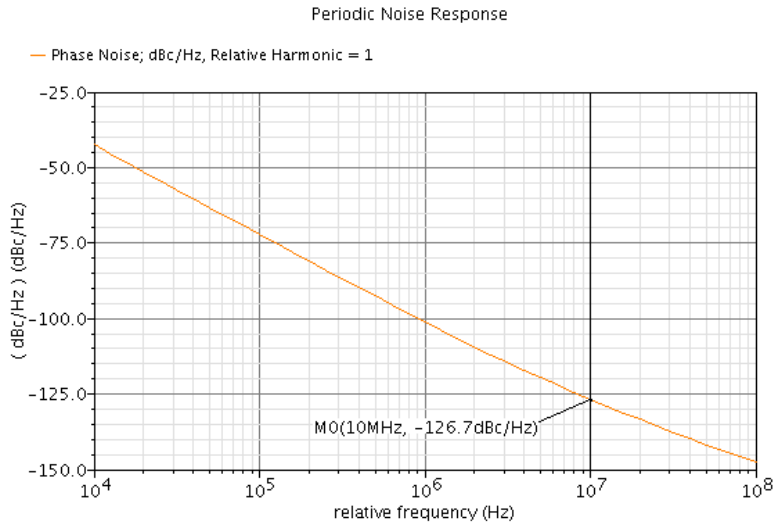



**Figure 5-23 - Phase Noise of the oscillator at 900MHz oscillating frequency.**

### 5.3.4 Schematic vs. Post-Layout Simulations

Through the analysis of Tables 5.1 and 5.2, considering the simulation results for the three frequencies, it is possible to conclude that for 900 MHz and 600 MHz, the current consumption associated to the schematic simulation is less than the current consumption related to the post-layout simulation.

Concerning the values of the oscillation frequency, in general terms, are higher in the case of post-layout simulations. The biasing resistance assumes lower values, when referring to the post-layout simulation. The bypass capacitor at the mirror node of the current mirror, used to avoid supply and crosstalk noise, can justify the occurrence.

Although the simulation related to a biasing resistance of 5 Ω, was not explored with much depth, it is presented the respective oscillation frequency, for one particular motive: to emphasize the fact, that regardless the use of an extremely insignificant biasing resistance, it still would be possible to guarantee an oscillation frequency above the 1 GHz range.

In the caliber simulations with a duty cycle of 12.5 % there is an increase of the rise/fall time, if we take into consideration the premises related from Figures 5.6 to 5.8. Nevertheless, this increase does not exceed the specification standard as a primary goal. These conclusions cannot be extended to the other duty cycle. Moreover, for a frequency of 900 MHz it is fair to mention that times are very close to 100 ps. For the two other cases, it is possible to confirm an excess of the limit imposed. About this hypothetical "excess" it should be said that, firstly, this is considered as a mere result of the number of buffers used, since it might be forcing a delay in the rise/fall time of the signal, causing failures in the read of sequential phases, in regard with the receptor. The simulated current consumption versus oscillation frequency are shown in Figure 5.22.

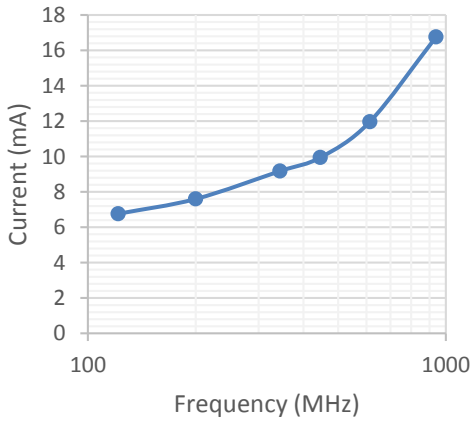



**Figure 5-24 – Core current versus oscillation frequency for schematic simulations (schematic on the left, post layout on the right).**

The currents are roughly proportional to the operation speed. Nevertheless, later, as it will be detailed in the next chapter, it is possible to conclude that the delay previously indicated, is not significant, which means that the results obtained are uniquely satisfactory.

## *5.4 Measurement Results*

Given the fact that, unfortunately there is no way to grant fiscally access to the Oscillator's outputs and measure his functionality, it had to be done through measurements done in [12]. A receiver like the one in the block diagram of Figure 4.1 of chapter 4 [11] was designed.

Two RF receiver front-end circuits were designed and fabricated in the UMC CMOS 130nm technology. For comparison purposes it was implemented two versions of the receiver, one with the DFB LNA, and the other with the basic LNA circuit using active loads. Thus, the only measurement results that will be shown are related to the basic LNA circuit. This is due to the fact that, the comparison between the two receivers, brings nothing relevant to the context of this document. Therefore, it only makes sense to show that the Ring Oscillator works properly on the wideband for which it was designed.

The layout and die photo are shown in Figures 5.19 and 5.20, respectively. The main blocks, alongside with the Oscillator, and signal pads are highlighted. The other pads are for supply and voltage references as well for external biasing circuits. Example of that, lies on the highlighted signal pads in Figure 5.19 ("rp_bias" and "rn_bias"), that represent where the terminals of the biasing resistor will connect.

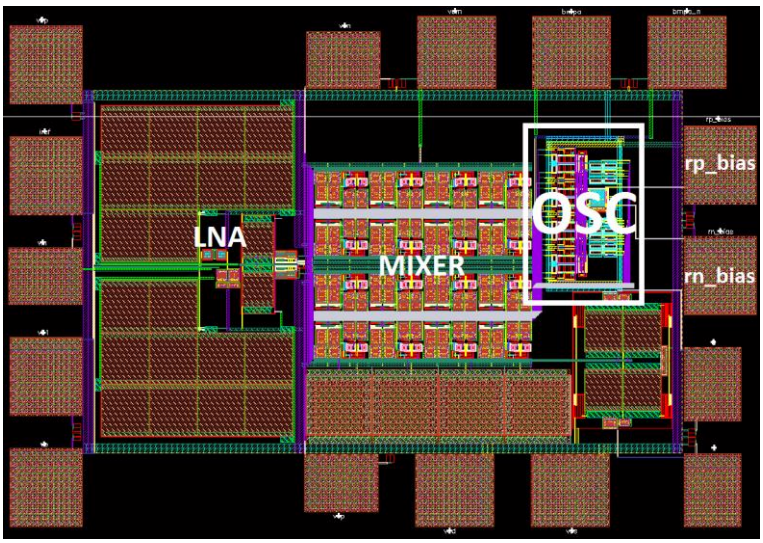



**Figure 5-25 – Layout of the front-end with the LNA with active loads (800 x 550 µm$^2$).**

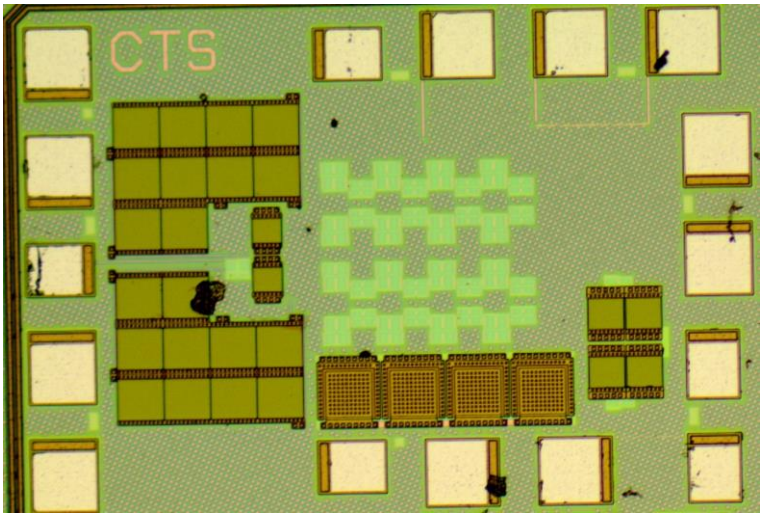



**Figure 5-26 – Die photo of the front-end with the LNA with active loads (800 x 550 µm$^2$).**

All the measurements were done with a spectrum analyser with a software option for noise figure measurements. The test board developed for the measurements is shown in Figure 5.21. The circuit was measured with an RF signal ranging from 250 to 900 MHz, which was limited by the designed internal VCO, in terms of frequency. The LNAs performance can be inferred from the relative measurement results. For each measurement step, the internal VCO has to be tuned to convert the RF signal to a low IF of 10 MHz. This tuning is performed by adjusting an external trimmer.

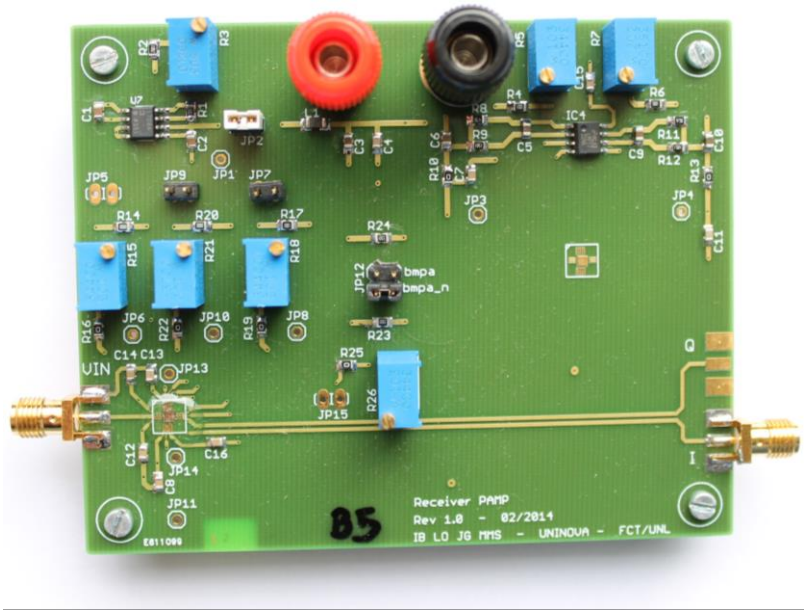



**Figure 5-27 – Prototype Board (adopted from [12]).**

Regardless of the results in qualitative terms, Figure 5.22 and 5.23 are presented to make it clear that was possible to keep the LNA operating in the entire frequency range for which the oscillator is designed to operate. In other words, without this thesis oscillator, and all this work done, the receiver would never have worked.

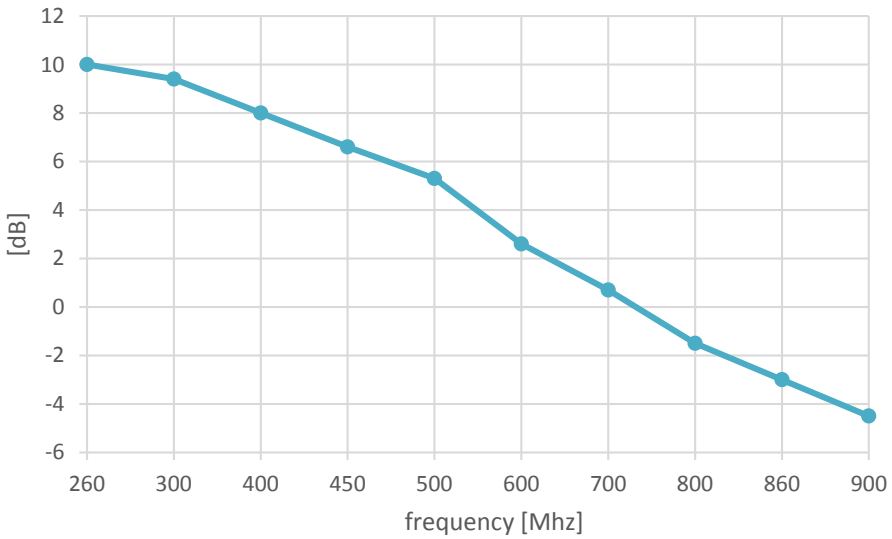



**Figure 5-28 – Front-end gain**

6

# 6 Conclusions and Future Work

## *6.1 Conclusions*

In this thesis we have presented an 8-Phase Oscillator for Modern Receivers. It is an inductorless wideband MOSFET-only Ring Oscillator with low area, low cost, and low power, capable of covering part of the WMTS and ISM bands, and intended for biomedical applications. The circuit prototype is validated by simulations (schematics and post-layout) and by measurements.

The oscillator presented is capable to have outputs with 12.5 % and 50 % duty-cycles. It was possible to verify that, the rising/fall times were not strongly affected by the parasitics, thus, it was possible to get reliable measurements from the test boards. Measurements results confirm that the oscillator is able to operate between 200 MHz - 900 MHz. This leads to an important conclusion, which confirm the comfortable margin settled for the rising/fall times.

The value of the current drawn from the DC power source of 1.2 V, ranged from 9.82 mA to 17.54 mA, in a band of working frequencies of 447.6 MHz - 930.1 MHz. Thus, after verifying the occupied area was 165 µm x 83 µm, it was possible to make sure that the oscillator fulfil effectively the goals initially proposed in order to be used as Local Oscillator in RF Modern Receivers.

## 6.2 Future Work

A possible evolution of this work, could be to adjust the number of buffers presented at the outputs of the accomplished architecture in order to optimize the isolation.

Another possible future project could focus on reducing power consumption, using a modern CMOS technology 65 nm and 28 nm. At this level, obviously that should take into account the rise and fall times, i.e., both must be located in the same order of values discussed previously. It must be noted that the receiver proper functioning, will not be conditioned even when exceeded the value of the signal set as default rise/fall times. This fact is due to the imposed safety margin, mentioned in Chapter 4.

Although this type of oscillators present a very small phase error and phase overlapping, would be interesting to carry out simulations (Monte Carlo) with greater depth around these two aspects. Thus, it would be possible to draw conclusions (or even comparison with some existing works) with greater relevance to the phase errors and phase noise, and consequently draw conclusions with much more know-how of the oscillator's own behaviour.

The optimization of occupied area is also a possible future challenge. This strategy came to be embraced, but the need to meet deadlines regarding the deployment circuit to factory prevented its completion (regardless of the decrease in the area, the total area of the receiver would not be changed).

Assuming that the oscillator is designed as a ring, a future job may go through the proper restructuring of the layout, that is, to shorten the wiring, approaching the core inverters to each other, thus resulting in a reduction of parasitics and minimizing the phase-error.

Although the technique used (ring oscillator with cross coupled inverters as latches) is one of the faster and more efficient to produce multiple phases, a possible future project may be based, the resort or investigation of different techniques in order to increase the range of frequencies on which the oscillator can operate.

A final future work is possible to elaborate through a comparison between a Shift Register approach for 8-phase generator, and the traditional approach discussed in this thesis as it is done in [33], where it is possible to validate a Shift Register that would accomplish the same power consumption with a reference clock and less jitter. Those advantages will increase in applications where clocks with larger number of phases at lower frequencies are needed.

7

# 7 References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