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Licenciatura em Ciências da Engenharia Electrotécnica e de Computadores

A Piezoelectric Based Energy Harvester Interface for a CMOS Wireless Sensor IC

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Universidade Nova de Lisboa

Resumo

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestrado em Engenharia Electrotécnica de e Computadores

por Nuno Lemos Braamcamp de Mancelos

Esta tese apresenta a implementação de um sistema *energy harvesting* piezoeléctrico que tem o objectivo de alimentar um receptor RF com um consumo de 6 mW. Para tal é necessário que o sistema regule a saída de um transdutor piezoeléctrico submetido a vibração. A caracterização do transdutor escolhido é o ponto de partida do projecto, sendo que seguidamente é apresentado o rectificador responsável por rectificar a saída *AC* do transdutor, um *full-bridge cross-coupled rectifier*. O conversor DC-DC utilizado é um *low-dropout regulator*, que garante que a saída do sistema é mantida a um valor constante e com *ripple* reduzido. Este valor é 0,6 V, que corresponde à tensão de alimentação requisitada pelo receptor. O circuito é desenhado recorrendo à tecnologia CMOS 130 nm UMC, e apresenta uma arquitectura sem bobines, com reduzida área e custo. As simulações eléctricas feitas para o sistema completo levam a concluir que o circuito é uma solução plausível no que toca à alimentação do receptor RF, tendo em consideração níveis moderados de vibração do transdutor piezoeléctrico.

Palavras-chave: Energy Harvesting Piezoeléctrico, Rectificador Full-Bridge Cross-coupled, Conversor DC-DC, LDO Regulator, Wireless Sensor Networks.

Universidade Nova de Lisboa

Abstract

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestrado em Engenharia Electrotécnica de e Computadores

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In this thesis a piezoelectric energy harvesting system, responsible for regulating the power output of a piezoelectric transducer subjected to ambient vibration, is designed to power an RF receiver with a 6 mW power consumption. The electrical characterisation of the chosen piezoelectric transducer is the starting point of the design, which subsequently presents a full-bridge cross-coupled rectifier that rectifies the *AC* output of the transducer and a low-dropout regulator responsible for delivering a constant voltage system output of 0.6 V, with low voltage ripple, which represents the receiver's required supply voltage. The circuit is designed using CMOS 130 nm UMC technology, and the system presents an inductorless architecture, with reduced area and cost. The electrical simulations run for the complete circuit lead to the conclusion that the proposed piezoelectric energy harvesting system is a plausible solution to power the RF receiver, provided that the chosen transducer is subjected to moderate levels of vibration.

Keywords: Piezoelectric energy harvesting, Full-Bridge Cross-coupled Rectifier, DC-DC Converter, LDO Regulator, Wireless Sensor Networks.

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Abbreviations

AC	Alternating Current
ADC	Analog-to-digital Converter
CMOS	Complimentary Metal-Oxide-Semiconductor
DC	Direct Current
LDO	Low-dropout
LNA	Low Noise Amplifier
MCU	Microcontroller
NMOS	N-Channel Metal-Oxide-Semiconductor
PMOS	P-Channel Metal-Oxide-Semiconductor
PSRR	Power Supply Rejection Ratio
PZT	Lead Zirconate titanate
RF	Radio Frequency
SHM	Structural Health Monitoring
SoC	System on Chip
WSAN	Wireless Sensor Actuator Node
WSN	WSN Wireless Sensor Network

1

Introduction

1.1 – Background and Motivation

Energy harvesting comprises a wide variety of techniques that make use of ambient energy to power different types of electronic devices. It differentiates itself from conventional renewable sources mainly due to its small scale, and is suitable to power devices like Wireless Sensor Actuator Nodes (WSAN), which are used to collect physical or environmental information, like temperature, humidity, radiation and other physical quantities, usually spread across vast or hardly accessible areas. These devices are commonly required to operate in locations surrounded by one or several sources of residual energy, which can be ambient light, thermal gradients, kinetic energy in the form of vibration or energy present in propagating radio waves, just to name a few. The WSAN devices are wirelessly connected in Wireless Sensor Networks (WSN) formed by several energy autonomous nodes. The common solution to independently power these nodes is the use of batteries, which demand periodic replacement and costly maintenance, since they generally store insufficient amounts of energy, when considering each node's life cycle duration.

Using energy harvesting techniques that are specifically designed to scavenge certain types of residual energy is a plausible answer to the energy demands of the devices that constitute some WSNs. By enabling the energy self-

sufficiency of each node, these techniques enhance their wireless and widespread operations, allowing the devices to be installed in increasingly hard to reach or hazardous locations, and giving an incentive to the use of these wireless networks, since their reduced need for maintenance is likely to reduce their overall associated costs.

Some possible uses for WSNs are medical applications, in which the sensor nodes may be worn or implanted, environmental applications like forest fire detection, water quality and air pollution monitoring, structural health monitoring regarding buildings or different large-scale structures, industrial monitoring directed to factory environments or agriculture, and even military monitoring.

In terms of distribution and density values, kinetic energy is a relevant source of energy in some of the applications' environments. Vibration is a common source for this type of energy. One of the most interesting solutions to convert the energy contained in vibrations, in terms of typical power density values, is to use inertial piezoelectric transducers. These transducers explore the piezoelectricity of certain ceramics and crystalline materials, which is a property that is defined by the accumulation of charge inside the structure of piezoelectric materials when mechanical strains are applied to them.

This work presents the design of a piezoelectric energy harvesting system, intended to supply a low-power RF receiver whose design is not part of this work but was the focus of another master's thesis, included in the same multidisciplinary project, a WSAN System on Chip (SoC). The energy harvesting system includes a full-bridge cross-coupled rectifier that rectifies the AC output of the inertial piezoelectric transducer. In order to convert the rectifier's output, a DC-DC converter is used, consisting in a low-dropout (LDO) regulator that is responsible for delivering a constant voltage supply, with reduced voltage ripple, to the RF receiver's voltage supply rail.

The mentioned RF receiver presents power demands that are known and serve as a goal to be achieved by the power output capabilities of the system. The design was adjusted to meet the power requirements having in mind the predicted outputs of different piezoelectric transducers, which vary with the

vibration conditions to which they are subjected. These variations were taken into account in order to understand if typical vibration levels generate enough energy in the chosen piezoelectric transducers for the energy harvesting system to be able to meet the power demands of the RF receiver.

1.2 – Structure

After this introductory chapter, this thesis contains five chapters, with the contents that are summarised in this section.

Chapter 2 – Towards self-powered Wireless Sensor Nodes

The second chapter approaches the concept of synergy between wireless sensor networks and energy harvesting. A comparison of typical WSN power demands and energy harvesting power outputs proves the relevance of this type of techniques as a solution to power these devices. The main energy harvesting techniques are briefly presented, with special focus on the piezoelectric case. The RF receiver that is to be powered by the designed system is briefly presented, along with its power requirements.

Chapter 3 – Energy Harvesting from Piezoelectric vibration transducers

The particular case of energy harvesting from piezoelectric sources is explored in detail in this chapter. The equivalent circuit for the inertial piezoelectric transducer is presented, after which some examples of passive and active rectifiers are introduced. The chapter ends with the presentation of the several types of DC-DC converters and their main characteristics and operation principles.

Chapter 4 – Proposed System and Circuit Design

This is the chapter where the proposed system is presented. A system overview is offered, in which the typical transducer output values are given for different vibration conditions, according to the chosen transducer family's datasheet. The system overview also includes the dimensioning of the system's external components. After this, the rectifier is presented, along with the dimensions of its devices and the considerations made for the sizing process. The presentation of the DC-DC converter is separated into three parts, each one including schematics and sizing: the switch, the comparator and the clock generator circuit.

Chapter 5 – Electrical Simulations and Layout

The electrical simulations, and the main conclusions they lead to, are presented in this chapter. These simulations are divided into two sections: related to the rectifier, and regarding the complete system. For those related to the complete system, some adjustments were tested in the load requirements and transducer predicted outputs, in order to test the system's versatility and overall performance under different conditions and requirements.

Chapter 6 – Conclusions

Some conclusions are finally offered in the last chapter, followed by some future work suggestions.

1.3 – Contributions

This thesis originated from an experimental validation that was done for the operation of a commercially available piezoelectric transducer. This study provided insight related to piezoelectric energy harvesting and resulted in a publication in the 5th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS) 2014, entitled "Piezoelectric Energy Harvester for a CMOS Wireless Sensor".

The study of low-voltage techniques resulted in another publication in the same conference, entitled "Stability Improvements in a Rail-to-Rail Input/Output, Constant Gm Operational Amplifier, at 0.4 V Operation, Using the Low-Voltage DTMOS Technique".

The multidisciplinary project in which this thesis is integrated includes the design of an RF receiver that is to be supplied by the proposed energy harvesting system. The design of this receiver was done having in mind this type of power supply and its requisites became the energy harvesting system's power output goals. An article regarding this RF receiver, entitled "A Low-Voltage LNA and Current Mode Mixer Design for Energy Harvesting Sensor Node" was published in the 21st Mixed Design of Integrated Circuits & Systems (MIXDES) conference, 2014.

The previous paper resulted in an invitation to publish in the International Journal of Microelectronics and Computer Science. A new contribution entitled "Co-design of a Low-power RF Receiver and Piezoelectric Energy Harvesting Power Supply for a Wireless Sensor Node" was submitted for that purpose. This publication approaches a System on Chip concept that includes the RF receiver and the piezoelectric energy harvesting power supply.

2

Towards self-powered Wireless Sensor Nodes

The concept of synergy between wireless sensor networks and energy harvesting is presented in this chapter.

In section 2.1, a system overview is offered, including an introduction to wireless sensor networks' applications, structure and typical power consumptions. The advantages of self-powered wireless sensor nodes in relation to battery-powered ones are emphasized, and energy harvesting is presented as a solution to guarantee energy self-sufficiency for the sensor nodes, with some typical power output values given for different energy harvesting solutions.

Section 2.2 gives an overall notion of the most important energy harvesting generators, focusing on piezoelectric energy harvesting. This section presents important considerations about the design of piezoelectric energy harvesting power supplies.

The structure and typical power consumption values of the transceivers used in wireless sensor nodes are introduced in section 2.3. The Low-voltage RF receiver that is intended to be supplied by the energy harvesting system is briefly presented, and its power requirements are highlighted.

2.1 – System Overview

There are many applications in which physical or environmental information is scattered and needs to be collected by sensors in order to be used and processed. Some examples may be catalogued in four main areas: environmental monitoring, industrial monitoring, health care monitoring and military monitoring. The sensors are usually connected by a wireless network, commonly referred to as a Wireless Sensor Network (WSN). Figure 2.1 presents some examples of applications for WSNs.

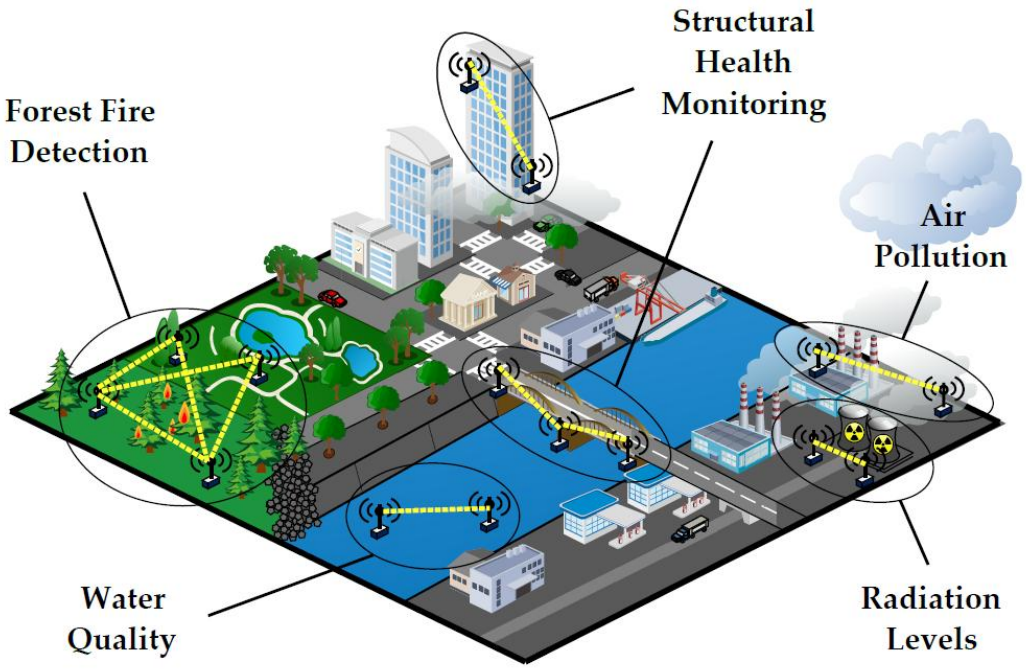

Figure 2.1: Wireless Sensor Network Applications

Concerning the environment, there are several physical conditions and quantities that are often measured, such as temperature, humidity, radiation and the presence of certain gases, just to name a few. The measurement of these quantities or properties over widely scattered areas allows forest fire detection, air pollution monitoring, weather sensing capabilities, water quality monitoring or even radiation levels monitoring in areas adjacent to nuclear power plants.

Industrial environments often include restricted or hazardous areas containing important machinery that needs to be under constant supervision, in order to monitor equipment and operation conditions. That supervision is made possible by sensing and collecting particular physical parameters, in each situation, making use of strategically located devices, which can be subjected to extreme or hazardous environments. The agricultural sector also represents an example of widely scattered industrial areas where it is convenient to collect and process information regarding temperature, humidity and sunlight, for example. Structural Health Monitoring (SHM) is also an important field in which sensors are spread, in this case in structures or buildings, with the objective of monitoring their overall condition and conservation state, analysing changes to the materials, vibration patterns or alterations in geometry.

Health care monitoring consists in collecting physical information regarding a person's body that gives competent medical staff, or even the patient, the ability to define a realistic and real-time medical condition. This information might be, for example, body temperature, heart rate, respiratory rate or blood pressure and the sensors that enable the monitoring can be implanted inside the patient's body or simply be wearable devices.

Among military monitoring applications, measuring acoustic intensity in vast areas may help detect and map explosions or enemy fire, and chemical or biological sensing of the environment can be useful to prevent intoxication and serious damage caused by chemical weapons.

In order to create a WSN, several Wireless Sensor Actuator Nodes (WSAN) are wirelessly interconnected. These are autonomous sensor nodes that collect information making use of their sensors, process that information using their analog-to-digital converters (ADC), microcontrollers (MCU) and additional electronic circuitry and then wirelessly transmit that information through their radio transceivers. These nodes may also be equipped with actuators in order to interact with their environment. The transceivers allow the individual nodes of the network to receive and transmit information, thus connecting them all, forming a WSN.

A standard structure for a single WSAN is presented in Figure 2.2.

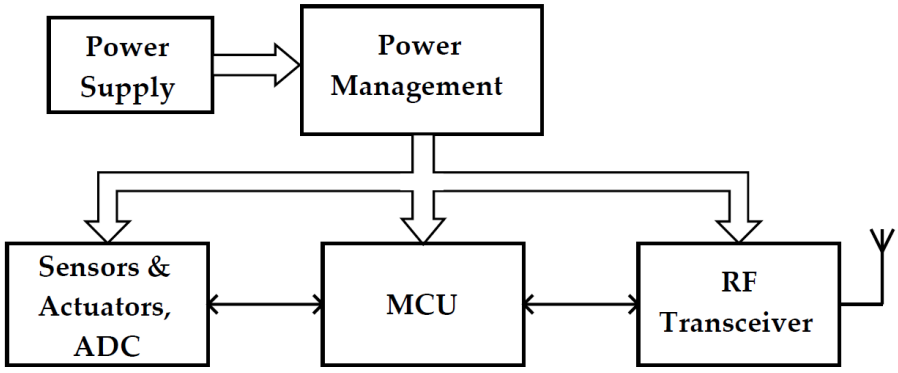

Figure 2.2: Structure of a Wireless Sensor Actuator Node

Depending on data rate, range of communication, number of sensors and actuators and processing requirements of each WSAN, just to give some relevant examples, the total power consumption varies for different devices. Table 2.1, [1], presents power consumption values for different commercial sensor nodes and includes some of their specifications.

Table 2.1: Power Consumption values for different commercial sensor nodes, [1]

	Crossbow MICAz	**Intel Mote 2**	**Jennie JN5139**
Radio standard	IEEE802.15.4/ZigBee	IEEE802.15.4	IEEE802.15.4/ZigBee
Typical range	100 m	30 m	1 km
Data rate (kbps)	250	250	250
Receiver consumption	19.7 mA	44 mA	34 mA
Transmitter consumption	17.4 mA (+0 dbm)	44 mA	34 mA (+3 dbm)
Minimum supply voltage	2.7 V	3.2 V	2.7 V
Average total power consumption	**2.8 mW**	**12 mW**	**3 mW**

Each WSAN's total power consumption is the sum of the power consumption of all of its modules, which in turn have very different power demands among them. Even if distinct WSANs have different data rates for their wireless communications and their transceivers are not continuously communicating, the wireless transceiver is generally the module with the highest power consumption in the node. Modules like the power management, the microcontroller and the actual sensor also represent a relevant consumption value, as can be seen in Figure 2.3, [2], where the contribution of the most relevant modules in terms of power consumption is presented for two different WSAN devices.

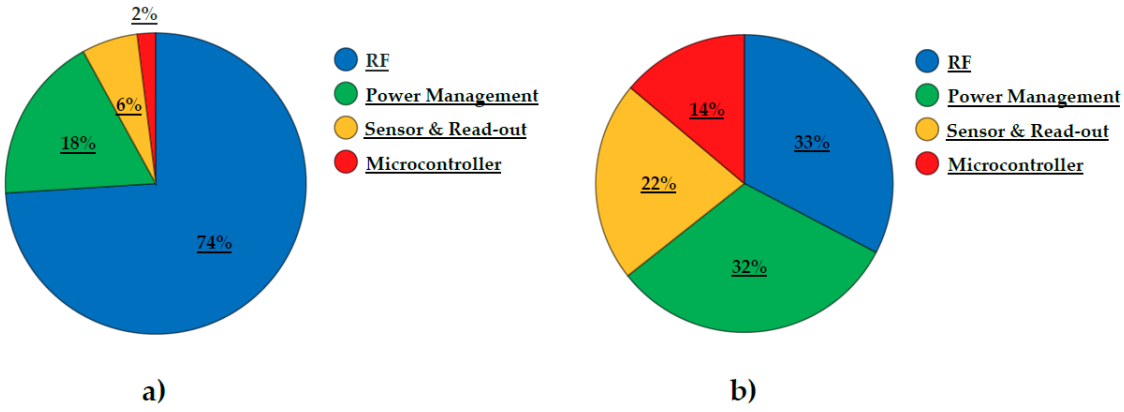

Figure 2.3: Distribution of Power Consumption for two different WSANs, a) sensor node based on the Nordic RF24L01, b) sensor node based on the imec's ULP wireless, data from [2]

The sensor node with the power distribution described on the first graph in Figure 2.3 has an average power consumption of 1.3 mW, and 74% of that power consumption corresponds to the node's wireless transceiver. The second graph in Figure 2.3 presents the power consumption distribution for a wireless sensor node with an ultra low-power transceiver. This ultra low-power operation is achieved using duty cycling techniques, which consist in switching the transmitter or receiver on only when they need to be working, having them switched off the rest of the time. This is possible because the nodes do not have to be continuously transmitting or receiving information via the transceiver, which allows some energy saving techniques to be employed. The total average

power consumption for this second approach is 362 µW. Even with the reduction in the power consumption values of the transceiver, this module is still responsible for one third of the total power consumption. Having these two examples in mind, the main conclusion taken from the distribution of the power consumption of a WSAN is that the wireless transceiver is not only a very important module in terms of the creation of the network of nodes but also a crucial module to take into account when considering each node's power consumption. Further attention will be dedicated to these wireless transceivers in section 2.3.

Since the wireless sensor nodes must be energetically autonomous, they must be powered individually. Their wireless characteristics allow them to be installed in virtually any place inside a reasonably sized area, dependent on their communication range. The freedom of operation in a vast area given to the devices by their wireless capabilities would be compromised if they had to be powered by an external source, using wires, so the common solution to power these nodes is to use batteries. Even if they address the wireless operation issue, batteries have limited supplies of energy and must be replaced after they are depleted, which happens in a time interval that is much smaller than the typical lifetimes of the wireless sensor nodes they power. Replacing a battery for a WSAN can be a difficult and consequently expensive procedure, especially if the nodes are situated in hard-to-reach locations, as many of the WSN applications demand.

In terms of powering a wireless sensor node, the ideal situation is having a node that is self-sufficient in terms of energy, or self-powered. This means that the node is installed in its designed operations position and is able to remain there, autonomous and unattended, during its entire lifetime. This is often referred to as the place-and-forget concept, and it is made possible by energy harvesting.

There is residual energy present in many of the different environments where WSANs need to be installed. This energy can be present in many different forms and have numerous sources but, for the sake of definition, residual energy can be described as energy that is present and would otherwise not be used. Its origin may be light, thermal gradients, electromagnetic radiation or

movement of different natures like rotation, vibration or water and air flow. Energy harvesting power supplies deal with the challenge of scavenging this residual energy and making it available to the circuits they supply. Table 2.2 presents some power supply capabilities of different types of energy harvesting generators, which will be explored with greater detail in section 2.2. Having its values compared with the ones presented in Table 2.1, this table leads to the conclusion that these harvesting power supplies have typical power densities that guarantee that they can provide sufficient power to be able to supply wireless sensor nodes, as long as the nodes and power supplies are carefully adjusted and matched.

Table 2.2: Typical power output densities for different energy harvesting solutions

Source type	Reference	Typical power density [3]
Solar	[4]	10 mW/cm^2
Thermal	[5]	1 - 10 mW/cm^3
Vibration; Piezoelectric	[6]	0.1 – 10 mW/cm^3
Vibration, running person; Electromagnetic	[7]	0.1 – 0.8 mW/cm^3

The typical power density values for the different energy harvesting techniques allow comparison by stating power output in terms of volume occupied by the transducer (for the solar energy harvesting type, the power density value is given for each square centimetre of solar cell).

There are many considerations that have to be made in order to fully characterise the power outputs of different energy harvesting generators. The examples given in Table 2.2 serve the purpose of demonstrating how the power outputs of several energy harvesting solutions may be matched with the power requirements of some wireless sensor nodes. However, the power output values depend, for example, on the loads that each implementation uses in order to test the generator, and these loads vary from one implementation to the

other, making comparisons difficult and inequitable. Additionally, some values represent the power output after conditioning, suffering from a reduction due to the converter's efficiency; others are simply the power outputs of the transducers, directly connected to an optimal load. Moreover, it should be noted that for testing energy harvesting prototypes and solutions, the sources of energy are emulated in many different ways. Some authors test their prototypes with conditions that are as similar as possible to the real environments. Other authors prefer to optimise their energy source conditions in order to be able to maximise their prototype's conversion efficiency. For these reasons, the calculation of each generator's power output may be highly influenced by these differences in the approach to the tests.

2.2 – Energy Harvesting

Energy harvesting techniques have the goal to power small electronic devices, allowing them to be ever more mobile, self-sufficient in terms of power and increasingly maintenance-free. There are four main types of energy harvesting power supplies, and they are distinguished by their source of energy, which can either be solar (or light), thermal, electromagnetic or electromechanical, [8].

Solar energy harvesting uses photovoltaic cells to convert solar radiation into a flow of electrons in the form of direct current. It uses the photovoltaic effect, which consists in the absorption of photons by a semiconductor material that results in the increase in energy of its electrons. Given enough absorption, (superior to the band gap of the semiconductor material), these electrons transit from the valence band and become available to flow.

Energy harvesting from thermal sources is divided into two types, one that makes use of the thermoelectric effect and one of the pyroelectric effect. The thermoelectric effect includes three separate effects, the Seebeck effect, the Peltier effect and the Thomson effect. It consists in the creation of voltage in the

terminals of a thermoelectric device when those terminals are subjected to different temperatures, and it is reversible, meaning that an applied voltage will create a thermal difference. It derives from the fact that different metals respond in distinct ways to the application of a thermal gradient, and for that reason create a current in a closed loop consisting of those adjacent metals. In its turn, the pyroelectric effect refers to the creation of a voltage when certain crystalline materials are heated or cooled, which is not the same as the thermoelectric effect, because in this case there is no temperature gradient in the material but rather a uniform distribution of temperature, at each instant, through the whole device.

Electromagnetic energy harvesting, or radio frequency (RF) energy harvesting, consists in scavenging the energy contained in propagating radio waves. This is possible with the use of antennas that receive these RF waves not to collect the information it carries but rather to harvest the energy it contains.

2.2.1 – Electromechanical Energy Harvesting

Different kinds of mechanical energy can also be scavenged to power small-scale devices, like the energy present in vibrations, relative movement of objects, airflow and pressure applied to certain structures, among others. This is called electromechanical energy harvesting and it is divided into three types of generators: the electromagnetic generators, the electrostatic generators and the piezoelectric generators.

Before presenting the characteristics of these three types of transducers, it should be noted that they fall into two categories: the ones that operate under direct application of force and those that exploit inertial forces acting on a proof mass, [3]. The concepts behind these two categories will be introduced before some examples are given, for both classifications, inside each of the three types of generators.

Direct-force generators rely on mechanical contact with two structures that move relative to each other. By doing so, they apply force on a proof mass that is connected to one of the structures by a suspension with a spring behaviour, to which a damper element containing the transducer is also attached. When the proof mass moves, the damper opposes that motion and the mechanical energy involved is converted to electrical energy by the transducer. Figure 2.4 is a representation of the direct-force generator concept.

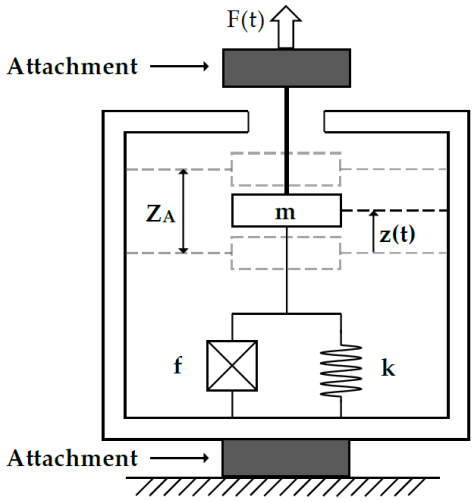

Figure 2.4: Direct-force Generator Diagram, adapted from [3]

In the figure, m relates to the actual proof mass, k represents the spring's stiffness, f is the transducer, z(t) is related to the proof mass displacement and Z_A is the amplitude of the inertial mass motion.

For the fact that direct-force transducers require two points of attachment to two different structures, their use in very small-scale energy harvesting solutions is less desirable in relation to the use of generators that make use of inertial forces acting on a proof mass, since these generators require the attachment to only one moving structure. Inertial generators can have their transducers contained inside compact and enclosed structures, favouring miniaturization, and include a proof mass, also connected to a spring-like suspension and a damper attached to the transducer. For inertial generators, however, the work done against the damper is not caused by the direct application of force to the

proof mass, but rather by the relative displacement of the proof mass in relation to the rest of the moving structure, by means of the resistance to the change in its state of motion, *i.e.* its inertia. Figure 2.5 shows a model of a generic inertial-force generator.

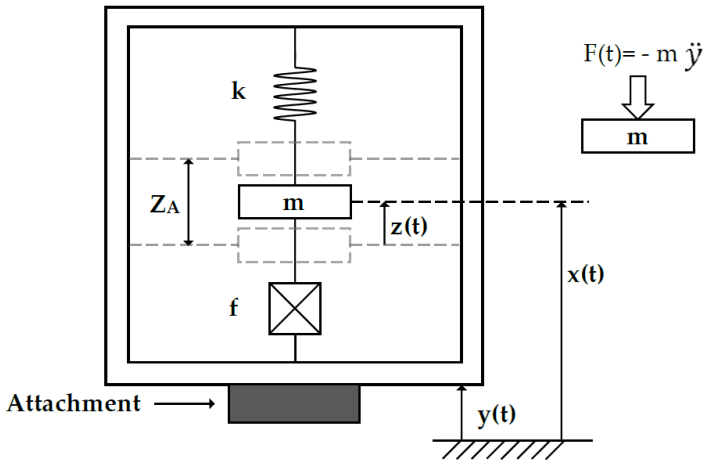

Figure 2.5: Inertial-force Generator Diagram, adapted from [3]

For this case, x(t) is the absolute motion of the proof mass and y(t) the absolute motion of the structure. In its turn, z(t) relates to the relative motion between the proof mass and the structure.

Electromagnetic Generators

The principles that govern electromagnetic generators' operations make use of a direct application of Faraday's law of induction, which states that when subjected to a change in magnetic flux, a coil will have a voltage induced in its terminals. Therefore, they operate using the same principles that are in the core of large-scale electrical generators with synchronous and asynchronous machines.

Paradiso *et al.*, [9], have investigated three different methods of harvesting energy from the human gait, adapting energy harvesting transducers to different shoes. One of these approaches was the one presented in [9], where a rotating electromagnetic generator was installed in the heel of a shoe, and rotated by

the pressing of a lever for each step, as the heel touches the ground. This approach is one example of an electromagnetic generator designed to make use of direct application of force.

Two examples of electromagnetic generators that are inertial generators are the ones presented in [7] and [10]. The first is a magnetic spring generator and it is suitable for applications involving human walking or slow running. Figure 2.6 shows a conceptual model of the magnetic spring generator.

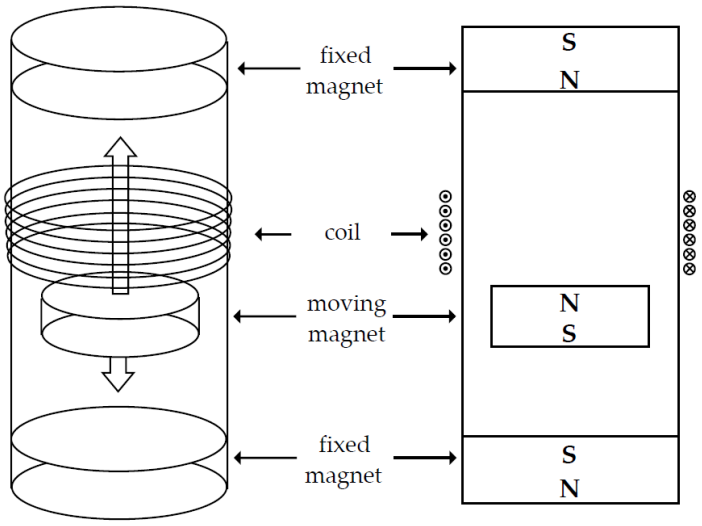

Figure 2.6: Magnetic Spring Generator Diagram, adapted from [7]

An unattached and free to move permanent magnet is placed inside a tube, with each of its magnetic poles facing one end of the tube. At each of these ends, two other permanent magnets are placed, each of them presenting a matching pole to the moving magnet, so that it is repelled by both ends. A coil is wrapped around the tube, allowing a voltage to be induced in it when the magnet moves inside, an occurrence that is provided by the magnet's relative movement to the tube, caused by its inertia, during the movement of the tube along its own axis.

The second example is more suitable to vibrations and consists of a resonator with a movable planar inductor, a cylinder case and two sets of magnets, one at the top of the case and the other at the bottom. Attached to a vibrating

object or structure, the cylinder case vibrates with it, making the magnets, which are fixed to it, also move. The planar inductor, which is free to move between the magnets, inertly resists the vibration and consequently exhibits movement relative to the magnets, which induces a voltage in the coil's terminals. Figure 2.7 is a representation of this generator.

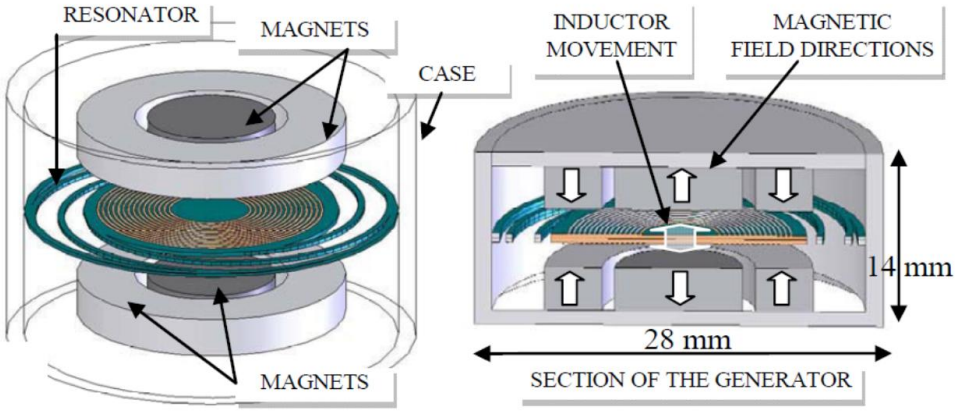

Figure 2.7: Resonator Electromagnetic Generator, figure taken from [10]

Electrostatic Generators

Electrostatic transducers use capacitor structures whose charged plates move in relation to one another, when subjected to movement, usually vibration. This relative movement of the charged plates changes the absolute values of the electric field in the capacitor's dielectric, thus guaranteeing energy storage capabilities. The relative movement of the plates can either be the separation and approximation of the plates or the lateral relative movement of two parallel plates, both cases resulting in the variation of the volume of the dielectric between them.

These transducers have two different principles of operation, one in which the charge of the plates is maintained during movement and the other where potential is maintained. In both cases, an electrostatic force generated by the opposition of the attraction of the plates and the relative movement they experience enables the conversion of mechanical energy into stored electrical energy, either by strengthening the electric field, in the constant charge case, or by

forcing a flow of charge from the plates, creating a current, for the constant potential case.

Microelectromechanical Systems (MEMS) are very suitable for electrostatic transducer implementations, since they allow integration of the capacitor plates that can be produced at micrometre-scale dimensions. When integrated, these MEMS technology transducers can be included inside the integrated circuits they power, and are subjected to the same physical laws that govern their energy harvesting concepts in a larger scale, making the integration a very interesting possibility for electrostatic transducers.

Piezoelectric Generators

While electromagnetic transducers explore the technical implications of Faraday's law of induction and electrostatic transducers make extended use of the properties of mechanically variable capacitors, piezoelectric transducers rely on a property of some crystalline materials and certain ceramics, called piezoelectricity. The piezoelectric effect derives from this property, and refers to the accumulation of electrical charge in piezoelectric materials, when mechanical strains are applied to them. This is what makes piezoelectric materials an interesting prospect for energy harvesting purposes. The effect is reversible, meaning that a mechanical stress, *i.e.* movement, is generated in a piezoelectric material when an electrical field is applied to it. This is called the converse piezoelectric effect. Figure 2.8 shows a representation of these effects.

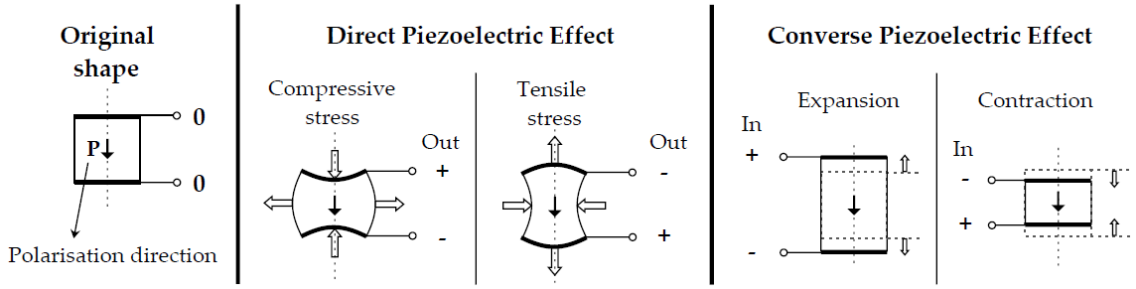

Figure 2.8: The Direct and Converse Piezoelectric Effects

The most common piezoelectric materials used in energy harvesting generators are lead zirconate titanate (PZT), barium titanate (BaTiO3) and polyvinylidene flouride (PVDF), [1]. PZT is commonly used in vibration energy harvesting because it exhibits high energy conversion efficiency from mechanical to electrical forms.

Piezoelectric generators are usually included in energy harvesting solutions that involve vibrations, so inertial generators are more common among piezoelectric energy harvesting systems than direct-force generators.

An example of a direct-force piezoelectric generator is developed in [11], where a piezoelectric material is placed in the heel of a shoe, inside the sole. Each time the shoe hits the floor, during the walking process, the piezoelectric material is pressed by the person's weight, and generates electric charge that is conveniently processed and stored by the associated power circuit. The same principle of operation has been studied for inclusion of piezoelectric materials under the steps of some busy public stairways or under the pavement of some public spaces with considerable movement, in order to generate electricity.

The most common way to make use of piezoelectric materials for energy harvesting purposes is to include them in inertial generators designed for vibration energy harvesting. These usually consist of a rectangular beam structure that bends in response to ambient vibration and that is clamped in one extremity and free to move in the other. The extremity that is free to vibrate usually has an attached proof mass. The piezoelectric material is added to each of the beam's surfaces, both the upper and the lower surfaces, in the shape of thin rectangular wafers that are completely fastened to the beam's structure. When the beam bends up and down, as a result of the ambient vibration, these wafers suffer mechanical strains that are complementary: if the beam bends upward, the upper wafer contracts, creating a certain potential at its terminals, and the lower wafer is stretched and expands, creating a potential with an opposite polarity. When the beam curves downward, the opposite occurs. Figure 2.9 exemplifies the process, presenting a conceptual diagram of a typical piezoelectric inertial transducer.

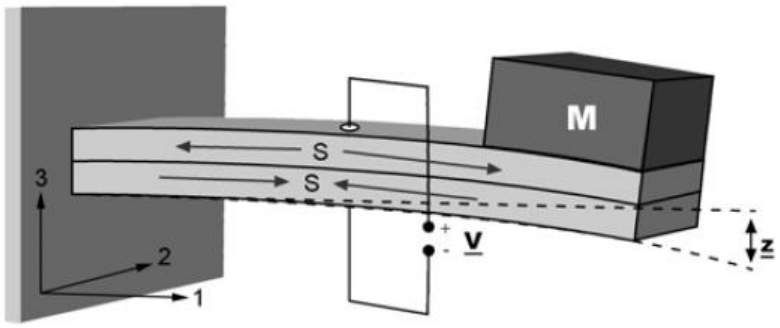

Figure 2.9: Diagram of a Piezoelectric Transducer with a beam structure, figure taken from [12]

This is the chosen type of piezoelectric transducer for the energy harvesting system developed in this thesis. For that reason, a detailed analysis of this type of transducer, including some important equations, is presented in section 3.1.

Examples of the use of piezoelectric materials as piezoelectric inertial generators designed to work with ambient vibrations are developed in [1, 13, 14]. Two of these implementations are designed to power wireless sensor nodes and the other is intended to give energetic autonomy to a wireless structural health monitoring system. Regardless of the level of complexity and optimisation of each of these piezoelectric generator developments, some considerations are common to all the works in the literature concerning this subject. One of the most important considerations to have in mind when developing this type of energy harvesting solution is that the vibration that represents the source of energy must be well characterised. The vibration characteristics that must be defined are its frequency, the acceleration and the type of vibration (which relates to whether it consists of sudden bursts, impacts or if it is more or less even and continuous). The knowledge of the characteristics of the source vibration is very important because the piezoelectric transducers of this kind have a natural frequency, or resonant frequency, that can be regulated, mainly by adjusting the proof mass, and that should be matched with the ambient frequency to which it is subjected, in order to maximise the power output. Additionally, piezoelectric transducers' datasheets present their open circuit voltage output values for the

transducers in terms of different vibration frequencies, matched with the regulated natural frequencies, but also in relation to the vibration's acceleration, which is directly related to the amount of physical displacement of the extremity of the beam that is free to move. The greater the acceleration, the greater the displacement of the tip, which results in a more substantial mechanical strain applied to each wafer. All of these considerations are very important in order to correctly design an energy harvesting system with a specific circuit to power, which in turn has its own requirements and specifications. For the three examples given above, a shaker table was used in order to create the vibrations necessary to test the energy harvesting system prototypes. These shaker tables create vibrations with frequency and acceleration values that are defined during tests, allowing a good testing setup for the prototypes.

A real concern for vibration-based piezoelectric energy harvesting design is the difficulty in defining the characteristics of the ambient vibration to which the generators are to be matched. Either way, the transducers present a certain power bandwidth, which corresponds to the bandwidth of frequency values around the resonant frequency to which the power output is still close to the desired value. The same is true for different values of acceleration. Even if the transducer is optimised to work for a certain acceleration value, other values might also guarantee satisfactory power output results. Summing-up, the better the vibration characteristics of the ambient source are defined, the better power output predictions can be made for the generator, after a careful dimensioning of both the transducer and the subsequent power circuit. For cases in which the vibration is less predictable, a piezoelectric energy harvesting solution may also be a good option, as long as it is considered a possibly intermittent power supply, which completely fits applications for some WSN, where nodes don't have to be constantly communicating with each other and can send and receive information only when they have sufficient power available to do so.

2.2.2 – Considerations regarding Energy Harvesting Applications

When designing any kind of energy harvesting generator, the target application should be considered from the beginning, not only because different applications are surrounded by different environments with different kinds of residual energy, but especially because the circuit that needs to be powered is the source of specific electrical requirements that need to be met.

Considering the present power output limitations of most energy harvesting solutions, related to the reduced residual amounts of energy that are available in certain environments and the sometimes low conversion efficiencies, the target applications for which they are considered as a potential power supply are generally low-power circuits, intended to operate in an intermittent way, meaning that the circuits operate only after sufficient energy is converted and stored. The integrated circuits that are part of WSANs have been recently developed in order to be less and less power-demanding, with a tendency to reduce supply voltage and current consumption as the integrated technology gets smaller and new power-aware integrated circuit designs are developed. This development has an increasing focus on reducing energy consumption, in part motivated by the interesting prospects given by the rising development of energy harvesting solutions.

The concept of synergy between WSANs and energy harvesting generators is therefore a very interesting and recent focus of several departments and investigators worldwide, in the field of microelectronics. It is fuelling the effort to increase the power outputs and conversion efficiencies of the energy harvesting solutions and also motivating the substantial reduction in integrated circuit power demand even further.

2.3 – Low-voltage RF Receiver

2.3.1 – Transceivers designed for Wireless Sensor Networks

As previously stated in section 2.1, the wireless transceiver is a crucial module for a WSAN, not only because it guarantees the wireless network is created but also in terms of power consumption, since it is generally the module with the highest power consumption in the node. Figure 2.10 presents a generic architecture of a wireless transceiver used in a WSAN.

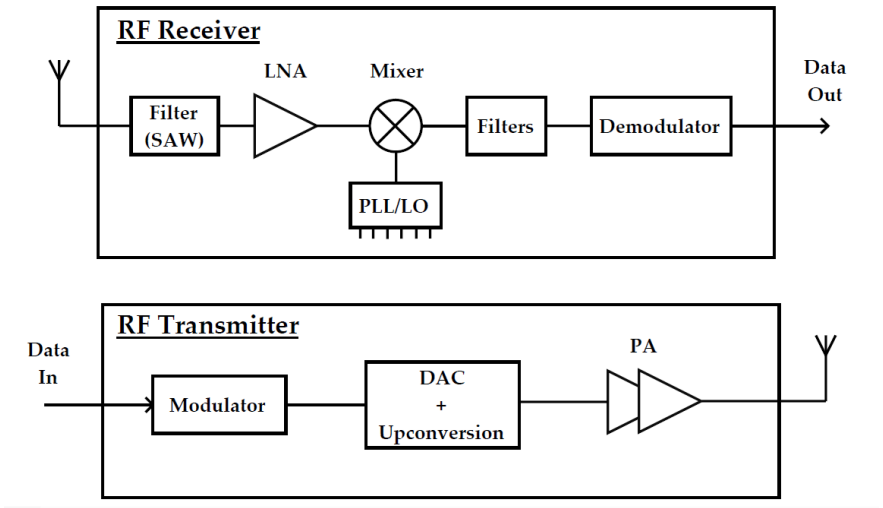

Figure 2.10: Block Diagram for a WSAN's Wireless Transceiver

The power consumption values of a wireless transceiver depend on some different requirements of the application it serves, like its data-rate, its communication range, its receiver sensitivity or (especially) its transmitter's needed output power, which is related to the communication range and directly influences the power consumption of the transmitter's power amplifier (PA), a block responsible for a considerable amount of power consumption in the transceiver. Transceivers that are intended to work with low-power consumption values are designed to be as simple as they can be, as long as the application's require-

ments are met. This effort leads to simpler modulation schemes, which in turn allow simpler receiver and transmitter architectures. For applications that involve close-range communications and low data-rates, for example, modulation schemes like the on-off keying (OOK) modulation are chosen, which employ a smaller number of electronic components and blocks. The overall reduction of the circuits' supply voltage also plays an important role in reducing the power consumption.

In order to have a sense of the typical power consumption values of recently developed wireless transceivers for WSN applications, some examples of wireless transceivers are presented in Table 2.3, which contains the power consumption values of their receivers and transmitters, as well as the supply voltage and modulation scheme.

Table 2.3: Examples of different WSN transceivers and correspondent power consumption values

Block	Parameters	[2]	[15]	[16]
Receiver	Power consumption	1.8 mW	4.8 µW	0.88 mW
	Supply voltage	-	0.9 V	1 V
	Modulation	OOK	OOK	OOK
Transmitter	Power consumption	2.3 mW	1.68 mW	2.5 mW
	Supply voltage	-	1 – 1.2 V	1 V
	Modulation	OOK	FSK	OOK

2.3.2 – RF Receiver to be powered by the Energy Harvesting System

As previously stated in the first chapter, this work's goal is to design and simulate an energy harvesting system that is capable of converting the power output of an inertial piezoelectric transducer and supply a low-power RF receiver that was part of the same multidisciplinary project, with the analysis of a prospective WSAN System on Chip (SoC) as the final goal of the joint endeavour. For the reasons that have been explained in this chapter, especially in section 2.2.2, it is important to briefly present the main characteristics and power requirements of the RF receiver that is to be supplied by the energy harvesting system. In this section, the receiver will be briefly presented, having in mind that the most important characteristics that have to be considered are its power requirements.

Receiver's Architecture

There are several classic RF receiver architectures with different complexities and performances. However, only some of them are suited for low-power applications, namely the Low-IF and the Direct conversion architectures. The receiver under discussion is the one presented in [17], and it follows a Low-IF architecture. Figure 2.11 presents a block diagram of this kind of receiver architecture.

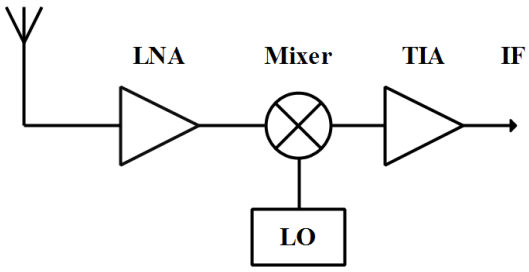

Figure 2.11: Low-IF Receiver Architecture

Complete Receiver Circuit

The complete schematic of the receiver implementation is shown in Figure 2.12. The design includes a MOSFET-only wideband balun Low-noise Amplifier (LNA), which includes noise and distortion cancelling capabilities. A passive mixer is also designed, intended to work in current mode. Although the design of the amplifier itself is not included, the system incorporates the transimpedance amplifier (TIA) module, which is essential for the current mode operation of the mixer, as explained in [17].

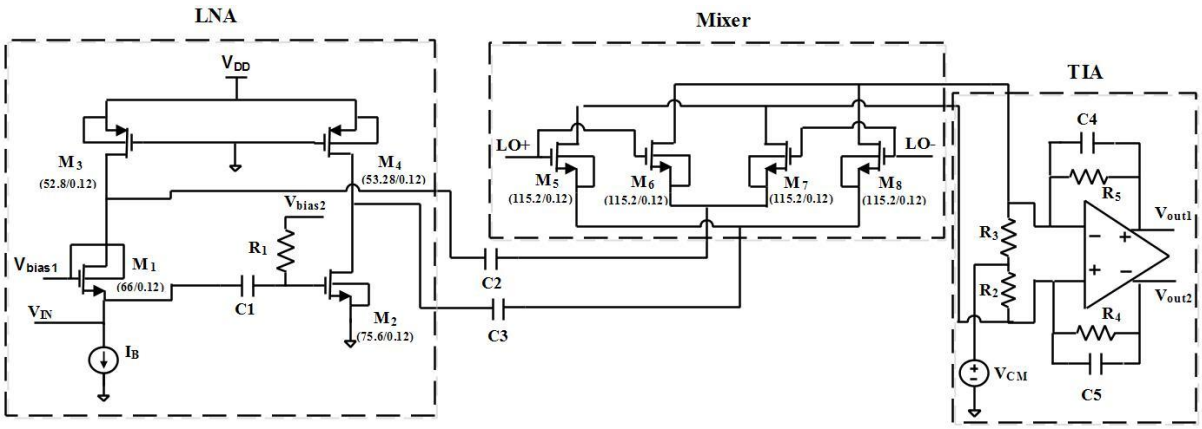

Figure 2.12: Complete Receiver Circuit with all transistor sizes (W/L) in µm, taken from [17]

Intended to work as a low-power receiver, targeting simple modulation schemes like OOK, the system design includes a passive mixer, which doesn't influence the overall power consumption. Since low power consumption was a major requirement for this receiver, as it was intended to work in an energy harvesting supplied WSAN, the design of the LNA was successfully optimised to work with a 0.6 V supply voltage, a value that represents half the supply voltage for which some important works in the literature were designed, namely the works that served as a starting point for the actual design of the LNA, like the one presented in [18].

Receiver's Power Requirements

The important considerations to have in mind in order to successfully design an energy harvesting power supply for this receiver circuit are directly related to its power consumption and its supply voltage.

As previously stated, the intended supply voltage is 0.6 V. This means that in order to be able to supply this circuit with satisfactory results, the power supply must guarantee a 0.6 V output to be connected to the receiver's power supply rail. Given the simplicity of the actual design and the precise optimisations that were made for the receiver to be able to work at a 0.6 V supply, the power supply must be designed to deliver a 0.6 V regulated output with as little ripple or variation as possible. This is a very important and decisive requirement, and it will be explored with more detail in the fourth chapter. This concern is directly related to the receiver's low Power Supply Rejection Ratio (PSRR), which is a consequence of the design's simplicity. For these reasons, the energy harvesting power supply's output must be regulated with considerable precision.

Regarding the power consumption, the receiver presents a 1.95 mW value for the joint operation of the LNA and mixer. This value represents the average power consumption of these two receiver modules. It is directly calculated as the sum of the currents flowing in the two LNA's stages, approximately 1.63 mA each, times the voltage supply. The mixer, being passive, does not contribute directly to this calculation. This 1.95 mW value refers to the consumption of the designed receiver modules. However, the calculation does not include the power consumption of the TIA or the local oscillator (LO). Nonetheless, an approximation of the receiver's total power consumption had to be made, because the goal is to eventually supply an entire receiver with the energy harvesting power supply. The estimation that was made was that the entire receiver would consume approximately 10 mA from the power supply, during operation. So that was the figure taken into consideration for the dimensioning of the power supply. During operation, the receiver would request 10 mA with a 0.6 V voltage supply, which results in an estimated power consumption of 6 mW.

Table 2.4 summarizes the receiver's power requirements.

Table 2.4: Summary of the RF Receiver's Power Requirements

	LNA + Mixer	**Complete Receiver**
***DC* current**	3.26 mA	10 mA
V_{DD}	0.6 V	0.6 V
Power Consumption	1.95 mW	6 mW

3

Energy Harvesting from Piezoelectric vibration transducers

The main modules that constitute a piezoelectric energy harvesting power supply are presented in this chapter, including some relevant examples.

An overview of the piezoelectric energy harvesting power supply is offered in section 3.1. This overview introduces the system's modules.

Section 3.2 presents the equivalent circuit of the inertial piezoelectric transducer, as well as the most important equations that model its operation.

Different types of rectifiers are presented in section 3.3, divided by the passive and active categories. The rectifier designs and correspondent equations are presented, and each rectifier's operation is modelled having the piezoelectric transducer's equivalent circuit connected to its input.

The most important types of DC-DC converters are approached in section 3.4, giving special focus to linear regulators and offering the main concepts that govern the operation of switched capacitor converters and magnetic converters.

3.1 – Piezoelectric Energy Harvesting Overview

For the case of inertial piezoelectric energy harvesting, the piezoelectric transducer converts residual mechanical energy, present in vibrations, into electrical signals, by means of its piezoelectric properties. These electrical signals typically consist in a varying output voltage, usually in the form of irregular voltage bursts. These are *AC* periodic power signals, with the same frequency as the vibration source. As previously stated in subsection 2.2.1, the ambient vibration's most important characteristics are its frequency and acceleration. While the vibration frequency defines the output signal's frequency, the vibration's acceleration is what sets the output signal's magnitude, often characterised by the output voltage amplitude values. The piezoelectric transducer can be electrically modelled, meaning that it has an electrical model for which the internal parameter values can be changed, namely internal capacitance and impedance, in order to model transducers of different sizes and materials. The input vibration is also characterised in this model by adjusting the model's source, most commonly a current source, in terms of frequency and amplitude.

For the fact that the output of the transducer is an *AC* signal, an AC-DC converter is needed right after the transducer. This module is a rectifier, preferably a full-wave rectifier, so that the transducer's output energy can be scavenged to the full extent. Passive rectifiers rely on diodes connected in different configurations. Mainly because of the voltage drop at each diode's terminals, the passive rectifier's power efficiency is lower than the efficiency achieved with active rectifiers, which operate using actively controlled switches, usually MOSFET transistors or Bipolar Junction Transistors (BJT). These switches present a substantially lower voltage drop when compared to the diode case. The rectifier's output presents a *DC* signal, which means that there is unidirectional current flow, but not a constant voltage. In order to make this output voltage as constant as possible, a capacitor is usually added at the rectifier's output, so that an output voltage smoothing can be implemented. Even with the added capacitor, the output presents a voltage ripple that depends on the capacitance value and load current. Adding to the typically undesirable voltage ripple, this

rectifier's output presents an average voltage value that varies with the input's amplitude values, failing to guarantee a stable and constant output during voltage amplitude variations of the unstable *AC* input. For these reasons, and for the fact that the load circuits need to be fed at specific and regulated voltage values, a DC-DC converter is needed after the rectifier.

The DC-DC converter is responsible for converting the *DC* signal coming from the rectifier's output to a different voltage level. The converter's output is regulated, meaning that it delivers a constant voltage output value, with minimum voltage ripple. The converter's output requirements are set by the circuits that represent the energy harvesting system's load. The target output voltage is the load's required supply voltage, which should be as constant as possible, to ensure reliable operations. Electronic DC-DC converters used for piezoelectric energy harvesting systems may be linear regulators, switched capacitor converters (referred to as charge pumps), or magnetic converters, which rely on inductors (called step-down or buck and step-up or boost).

After rectification, DC-DC conversion and voltage regulation, the energy is then stored in the energy storage device, often chosen as a supercapacitor. Supercapacitors are double-layer capacitors with high capacitance values, that can be charged and discharged faster than batteries and store much more energy per unit mass than electrolytic capacitors. As previously mentioned, the load circuit is intended to operate only after enough energy is converted and stored. Typical WSAN applications present this intermittent operation.

Figure 3.1 presents a simple block diagram of a typical piezoelectric energy harvesting system.

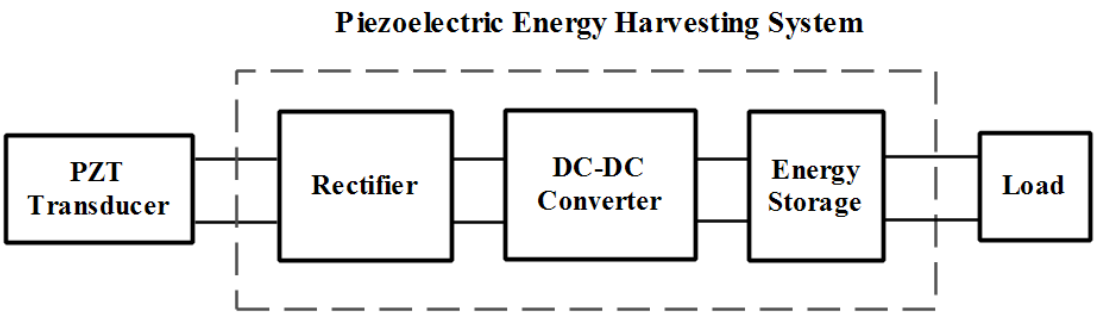

Figure 3.1: Block Diagram of a generic Piezoelectric Energy Harvesting System

3.2 – The Piezoelectric Transducer

Inertial piezoelectric transducers with a beam structure, introduced in subsection 2.2.1, are the type of transducer that is considered for the designed energy harvesting system that will be presented in the fourth chapter.

As previously stated, these transducers have a resonance frequency (also called natural frequency) that represents the optimal vibration frequency for scavenging mechanical energy contained in vibrations. This means that when the vibration to which the transducer is subjected has a frequency that is close to its resonance frequency, the power output is maximised. This resonance frequency is a characteristic of the piezoelectric transducer, and can be tuned by adjusting its proof (or tip) mass, as explained in [19]. From a mechanical energy conversion point of view, a transducer of this kind should have its tip mass adjusted so that its natural frequency matches the typical predicted vibrations frequencies to which it will be exposed in its destined environment.

If the piezoelectric transducer vibrates at a frequency that is close to its resonance frequency, the piezoelectric wafer can be modelled by its equivalent circuit, shown in Figure 3.2, where i_p is the AC current source, C_i the transducer's equivalent internal capacitor, R_i the internal resistance and V_{OC} the open circuit voltage at the transducer's output, [20, 21].

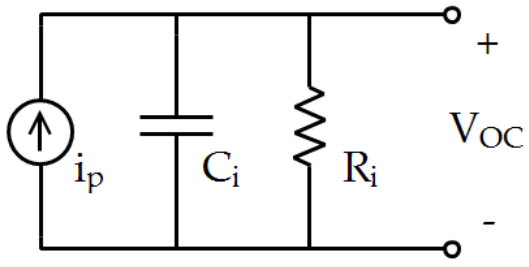

Figure 3.2: Equivalent Circuit of a single wafer on an inertial piezoelectric transducer vibrating near the resonance frequency

The equivalent circuit presented above refers to a single piezoelectric wafer. As discussed in the previous chapter, some beam structured piezoelectric transducers have two identical piezoelectric wafers, one for each surface of the beam. These wafers have two terminals each, which is why some specific transducers, namely the ones detailed in the datasheet for the Midé Volture™ piezoelectric transducers family, [19], have four electrical leads. This accessibility to each of the two independent wafers allows two different connections: in parallel, in order to maximise current output, and in series, which maximises voltage output. The equivalent circuit for each of these configurations is given by the parallel or series connection of two of the single wafer equivalent circuits. A parallel configuration, chosen for maximum current output, was experimentally tested in [22], a work that is part of this thesis' contributions. The piezoelectric transducer used for the experimental validation in the referred work was the piezoelectric energy harvester Midé Volture™ V21BL, presented in Figure 3.3.

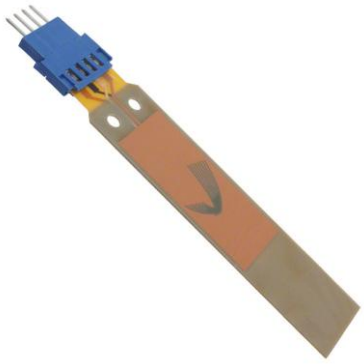

Figure 3.3: Midé Volture™ V21BL

The parallel equivalent circuit used in [22] is presented in Figure 3.4.

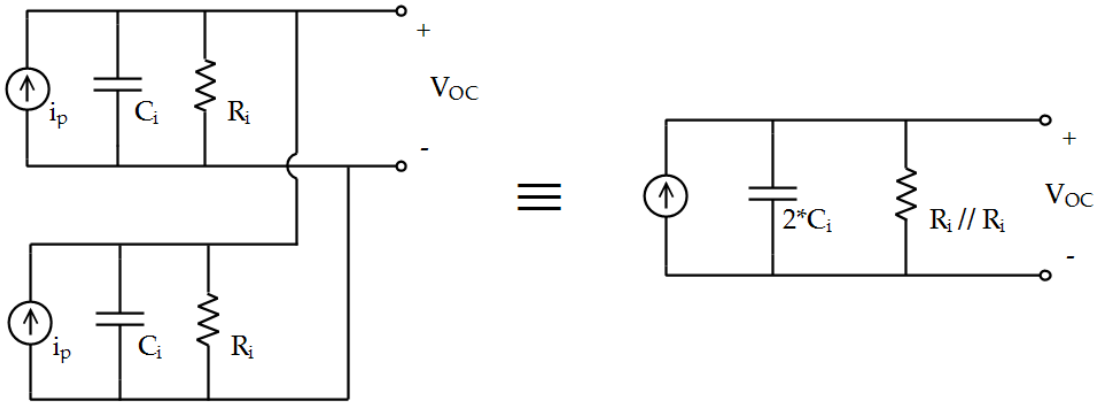

Figure 3.4: Equivalent Circuit of a parallel configuration for a two-wafer piezoelectric transducer

The piezoelectric transducer presented above was a reference for the present work, as well as some of the devices included in its transducer family. The most important details regarding these devices that must be retrieved from their datasheet are their electrical characteristics and power output levels.

The internal characteristics of the piezoelectric transducer are modelled by the internal capacitance and resistance values. The *AC* current source generates a sine wave with the vibration's frequency and peak current values that are proportional to the vibration's amplitude, also called tip-to-tip displacement, which translates into how much the beam bends during vibration, a measure directly related to the vibration's acceleration. Equation (3.1) models the transducer's sinusoidal current source $i_p(t)$, where I_p is the current source amplitude and $\omega = 2\pi f$, with f as the vibration's frequency in hertz, [20].

$$i_p(t) = I_p . \sin(\omega t) \tag{3.1}$$

The open-circuit voltage of the piezoelectric transducer can be calculated by (3.2), ignoring the internal resistance, [21].

$$V_{OC} = \frac{I_p}{\omega . \mathrm{C_i}} \tag{3.2}$$

The internal capacitance and resistance values are usually measured by the transducer's manufacturer for different resonance frequencies. These electrical characteristics are therefore available in the transducer's datasheet, as well as the correspondence between different tip mass values and resonance frequencies, making it possible to tune the transducer for different frequencies by adjusting the tip mass. For each relevant resonance frequency chosen by the manufacturer, different vibration acceleration values are also tested, in order to provide a series of measured outputs of the transducer for each set of vibration conditions. These outputs are often given in terms of open circuit voltage, which is why the Thevenin equivalent version of the circuit presented in Figure 3.4 is used in this work for simulation purposes. This circuit consists of a sinusoidal voltage source in series with the parallel of the internal capacitance and resistance.

The information regarding the electrical model of the transducer combined with the correct characterisation of the ambient vibration can be used to predict typical power outputs of the chosen piezoelectric transducer, which is essential for the design of the subsequent power circuit.

3.3 – Rectifiers

3.3.1 – Passive Rectifiers

Full-Bridge Rectifier

The full-bridge rectifier is a full-wave rectifier, meaning that the whole AC input waveform is converted to a constant polarity waveform at the output. The four diode bridge configuration allows this rectifier to deliver the same output polarity during both the positive and the negative halves of the AC wave. For the output to maintain a relatively constant value that does not drop to zero every half cycle, a capacitor is added to smooth the output signal. This capacitor should have a considerably high capacitance value in relation to the internal capacitance of the piezoelectric equivalent circuit, in order to be able to keep the output voltage of the rectifier as constant as possible. Figure 3.5 presents the schematic for this rectifier, including the piezoelectric transducer's equivalent circuit, the actual diode bridge and the smoothing capacitor, C_{rect}, [21, 23, 24]. The piezoelectric transducer's output voltage will be named V_{OC}, even though it does not correspond to an open circuit voltage.

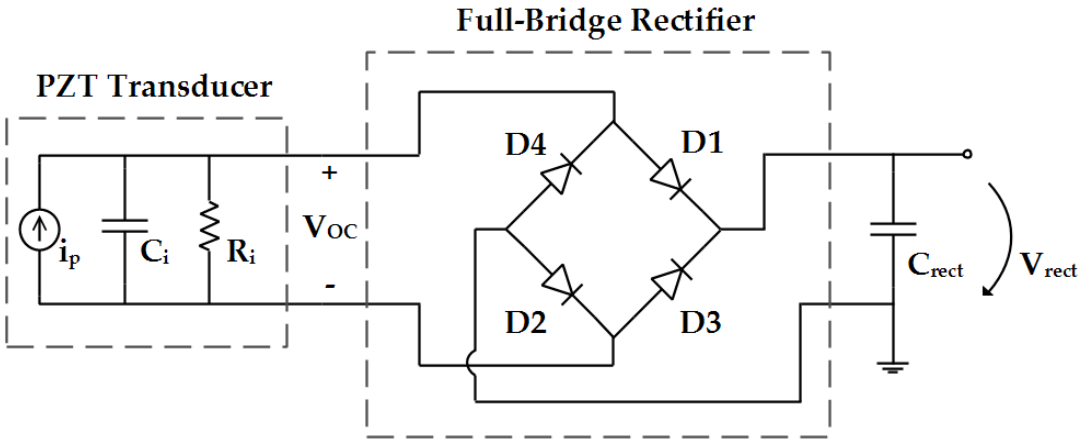

Figure 3.5: Full-Bridge Rectifier

For positive half waves at the AC input, diodes D1 and D2 are conducting, and the other two diodes conduct for negative half waves. Since non-ideal diodes have turn-on voltages that are not zero, there is a voltage drop at each conducting diode. This fact limits the rectified output voltage, which consequently reduces the power efficiency of the rectifier.

In order to simplify the output power analysis of a full-bridge rectifier connected to a piezoelectric transducer, the internal resistance of the transducer, represented as R_i in the equivalent circuit, shall not be considered.

The predicted voltage and current waveforms for this rectifier are presented in Figure 3.6, including the i_p sine wave current at the transducer's current source and the voltage across the transducer's internal capacitor C_i, which corresponds to the voltage waveform at the rectifier's input. This prediction includes diode non-idealities, meaning that each diode presents a voltage drop of V_D when conducting, and it is valid when considering that the C_{rect} capacitance value is much higher than the C_i capacitance value.

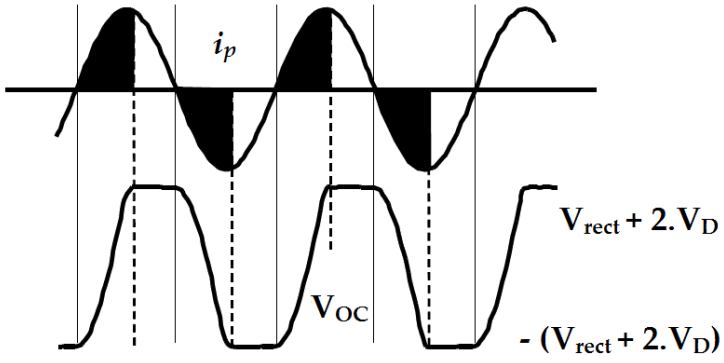

Figure 3.6: Predicted Input current and voltage waveforms for the Full-Bridge rectifier, adapted from [25]

For an initial approach, the diode non-idealities will be ignored (V_D=0 V). Since the transducer's internal capacitor must be discharged and then charged every half cycle, some charge is wasted during each half cycle. The total amount of charge that is made available by the transducer for each complete cycle is

given by Equation (3.3) and is the integral of i_p over a cycle's time interval. This time interval corresponds to the period of the sine wave, given by $T = \frac{1}{f} = \frac{2\pi}{\omega}$. Equation (3.3) and subsequent equations are derived and presented in [25].

$$Q_{total} = \int_0^{\frac{2\pi}{\omega}} i_p \, dt = \frac{4.I_p}{\omega} = 4.\mathrm{C_i}.V_{OC} \tag{3.3}$$

The charge lost per cycle is given by Equation (3.4). This equation is a result of the fact that the internal capacitor $\mathrm{C_i}$ is charged (and discharged) twice per cycle. For the positive half wave, the capacitor is charged from $-V_{rect}$ to V_{rect}, with this charging process represented with a shaded area under the positive half wave of the i_p waveform represented in Figure 3.6. In the negative half wave, the capacitor is charged from V_{rect} to $-V_{rect}$.

$$Q_{lost} = 2.\mathrm{C_i}.\left(V_{rect} - (-V_{rect})\right) = 4.\mathrm{C_i}.V_{rect} \tag{3.4}$$

The amount of charge that flows to the rectifier's output for each cycle is therefore given by

$$Q_{rect} = Q_{total} - Q_{lost} = 4.\mathrm{C_i}.V_{OC} - 4.\mathrm{C_i}.V_{rect}\,. \tag{3.5}$$

The energy delivered to the capacitor at the rectifier's output, C_{rect}, per cycle, is the charge delivered times the rectifier's output voltage, as in

$$E_{rect} = Q_{rect}.V_{rect} = 4.\mathrm{C_i}.V_{rect}.(V_{OC} - V_{rect})\,. \tag{3.6}$$

Having in mind that power is a measure of work done per unit of time, which translates into delivered energy per unit of time, $P = E/t$, and that the

time duration of each cycle is the cycle's period, $T = \frac{1}{f}$, the power delivered by the full-bridge rectifier is given by

$$P_{rect} = E_{rect} \cdot f = 4.C_i.V_{rect}.f.(V_{OC} - V_{rect}) . \quad (3.7)$$

The output power is maximised when $V_{rect} = V_{OC}/2$, which results in

$$P_{rect\,MAX} = C_i.{V_{OC}}^2.f . \quad (3.8)$$

Considering non-ideal diodes, with a voltage drop of V_D, the power output of the full-bridge rectifier is given by Equation (3.9). This equation considers that the C_i capacitor is charged up to $\pm(V_{rect} + 2.V_D)$, as depicted in Figure 3.6.

$$P_{rect} = 4.C_i.V_{rect}.f.(V_{OC} - V_{rect} - 2.V_D) \quad (3.9)$$

Voltage Doubler Rectifier

Figure 3.7 presents the voltage doubler rectifier circuit connected to the piezoelectric transducer's equivalent circuit and the smoothing capacitor, C_{rect}, [21, 26].

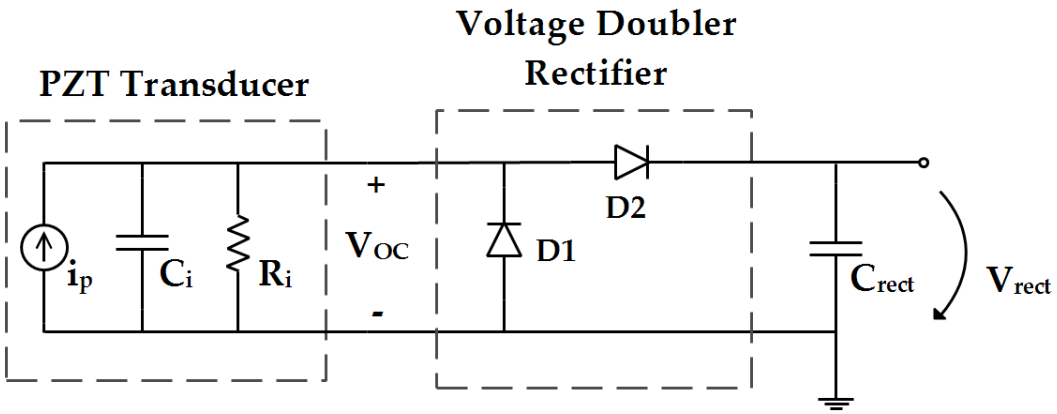

Figure 3.7: Voltage Doubler Rectifier

The voltage doubler is a half-wave rectifier and includes only two diodes. For this case, there is no current flowing to the rectifier's output during negative half waves. During those periods, the parallel diode, D1 in Figure 3.7, sets the output of the transducer at a $-V_D$ voltage value, and for that reason helps to pre-discharge capacitor C_i, which during negative half waves is charged with a polarity that must be reversed afterwards, so that current may flow to the output. At the beginning of the positive half wave, the current flowing from the source charges capacitor C_i until it reaches the $V_{rect} + V_D$ voltage value. This charging process starts earlier in relation to the full-bridge rectifier's positive half wave, because the voltage across capacitor C_i was already close to 0 V. After charging the internal capacitor, the current starts flowing through the D2 diode towards the output, because this diode is turned on. Figure 3.8 presents the relevant waveforms for the voltage doubler rectifier's operation.

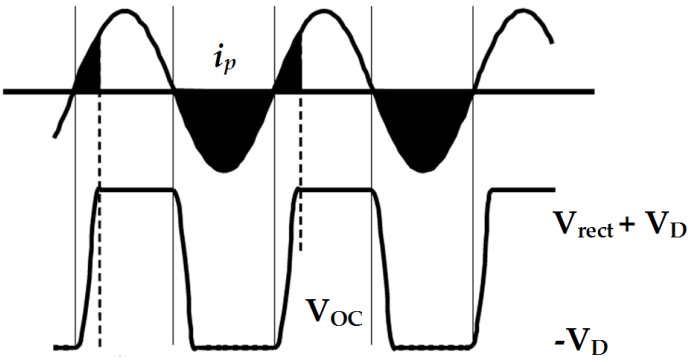

Figure 3.8: Predicted input current and voltage waveforms for the voltage doubler rectifier, adapted from [25]

As it happens for the full-bridge rectifier, some charge is lost in this case and does not reach the rectifier's output. For the negative half waves there is no charge flowing to the output, as is depicted in Figure 3.8 in the shaded areas. In the positive half waves, charge flows to the output only after the charging of the internal capacitor is finished. For simplicity, ideal diodes will be considered for this initial approach, which means that the internal capacitor C_i is charged from 0 V to V_{rect} and vice versa. The charge delivered to the rectifier by the transducer for each cycle is the same as in the full-bridge rectifier case, Equation (3.3), but the lost charge is different, and is given by

$$Q_{lost} = 2.C_i.V_{OC} + C_i.V_{rect} . \tag{3.10}$$

The amount of charge delivered to the rectifier's output, for each cycle, is given by

$$Q_{rect} = Q_{total} - Q_{lost} = 2.C_i.V_{OC} - C_i.V_{rect} . \tag{3.11}$$

Following the same reasoning used for the full-bridge rectifier, the power output per cycle of the voltage doubler rectifier is given by

$$P_{rect} = C_i . V_{rect} . f . (2 . V_{OC} - V_{rect}) . \quad (3.12)$$

This power output is maximised for $V_{rect} = V_{OC}$, which leads to a maximum power output that is the same as the one reached for the full-bridge rectifier, given by Equation (3.8).

If non-ideal diodes are considered, some additional charge is lost every cycle, since the internal capacitor must be charged from $-V_D$ to $V_{rect} + V_D$, and the other way around. This consideration leads to an alteration in Equation (3.10), which in turn results in a new power output equation,

$$P_{rect} = C_i . V_{rect} . f . (2 . V_{OC} - V_{rect} - 2 . V_D) . \quad (3.13)$$

Comparing equations (3.13) and (3.9) leads to the conclusion that the full-bridge rectifier presents an increased output power, in relation to the voltage doubler rectifier. However, the voltage doubler presents an optimal output voltage (V_{rect} voltage for maximum output power) that is higher up to two times, which may be an advantage in certain applications. Moreover, when considering ideal diodes with no turn-on voltage, $V_D = 0\,V$, the maximum power outputs are the same for the two rectifiers, given by Equation (3.8).

3.3.2 – Active Rectifiers

Switch-Only Rectifier

Given the characteristics of the piezoelectric transducer, the full-bridge and the voltage doubler rectifiers cannot overcome the problem associated with the loss in charge that is a consequence of the charging and discharging of the C_i capacitor, for each half-cycle of the AC input signal. The problem relates to the fact that as the source changes polarity, the internal capacitor is charged with alternate polarities for each half-cycle. As a consequence, at the beginning of each of these half-cycles the capacitor must be discharged to 0 V before it is charged according to the new polarity.

As a relatively simple solution for this problem, the switch-only rectifier is proposed in [21]. Figure 3.9 presents the schematic.

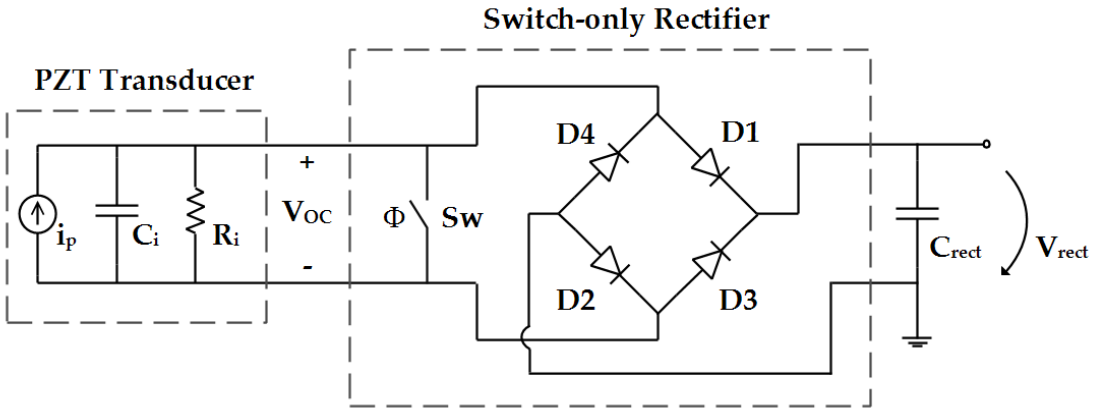

Figure 3.9: Switch-only Rectifier, [21]

This rectifier includes the diode bridge from the full-bridge rectifier, adding a controlled switch at the transducer's output, which makes it an active rectifier. This switch is a MOS transistor, with its gate driven by a control circuit. The details involved in the development of the control circuit that drives the transistor's gate are presented in [21] and will not be explored here.

The inclusion of the switch is a response to the loss of charge problem associated with the passive rectifiers presented above. By turning on the switch every time the i_p current crosses zero, for a very short period of time in comparison with the whole cycle duration, the output of the piezoelectric transducer is momentarily short-circuited. This causes the internal capacitor to discharge completely, after which the switch is turned off. For the subsequent half-cycle, the current coming from the source only has to charge the internal capacitor from 0 V to $\pm(V_{rect} + 2.V_D)$, not having to waste charge to discharge the capacitor, a situation that is similar to what happens during the voltage doubler rectifier's positive half-wave. Figure 3.10 shows the relevant current and voltage waveforms for this process.

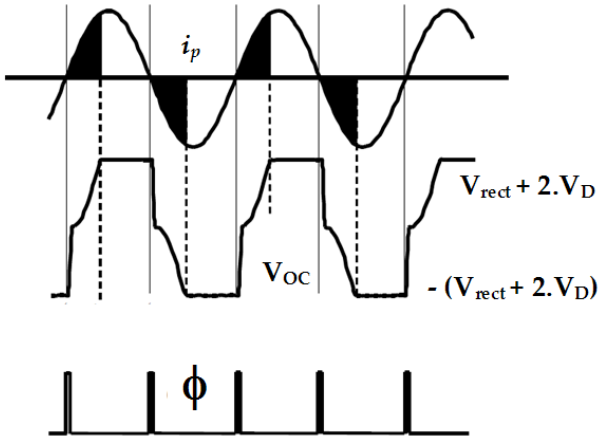

Figure 3.10: Relevant current and voltage waveforms related to the Switch-only rectifier's operation, adapted from [21]

Provided that the switch is driven in the desired way, the charge that does not flow to the output in each cycle corresponds to the wasted or lost charge, given by Equation (3.14), for which ideal diodes are considered.

$$Q_{lost} = 2.C_i.V_{rect} \tag{3.14}$$

The charge that flows to the output each cycle is given by Equation (3.15), which presents the difference between the total available charge delivered by the transducer's source and the lost charge, as for the previous rectifiers.

$$Q_{rect} = Q_{total} - Q_{lost} = 4.\mathrm{C_i}.V_{OC} - 2.\mathrm{C_i}.V_{rect} \tag{3.15}$$

The product of the output voltage, V_{rect} , the delivered charge, Q_{rect} , and the source frequency, f, is the power delivered to the rectifier's output, given by

$$P_{rect} = 2.C_i.V_{rect}.f.(2.V_{OC} - V_{rect}) . \tag{3.16}$$

This power output is doubled in relation to the voltage doubler rectifier power output, as can be concluded by comparing equations (3.16) and (3.12). The maximum power output is achieved with $V_{rect} = V_{OC}$, like for the voltage doubler, giving a maximum power output given by (3.17), which is twice the maximum power output that can be delivered by the full-bridge rectifier and the voltage doubler, as can be concluded by comparing this equation with (3.8).

$$P_{rect\,MAX} = 2.C_i.{V_{OC}}^2.f \tag{3.17}$$

For the case of non-ideal diodes, with a turn-on voltage drop of V_D, the power output of the rectifier is given by (3.18).

$$P_{rect} = 2.C_i.V_{rect}.f.(2.V_{OC} - V_{rect} - 2.V_D) \tag{3.18}$$

Full-Bridge Cross-coupled Rectifier

The full-bridge cross-coupled rectifier, also called CMOS full-bridge rectifier or differential-drive CMOS rectifier features two NMOS and two PMOS transistors connected in a bridge structure, as depicted in Figure 3.11, [27, 28].

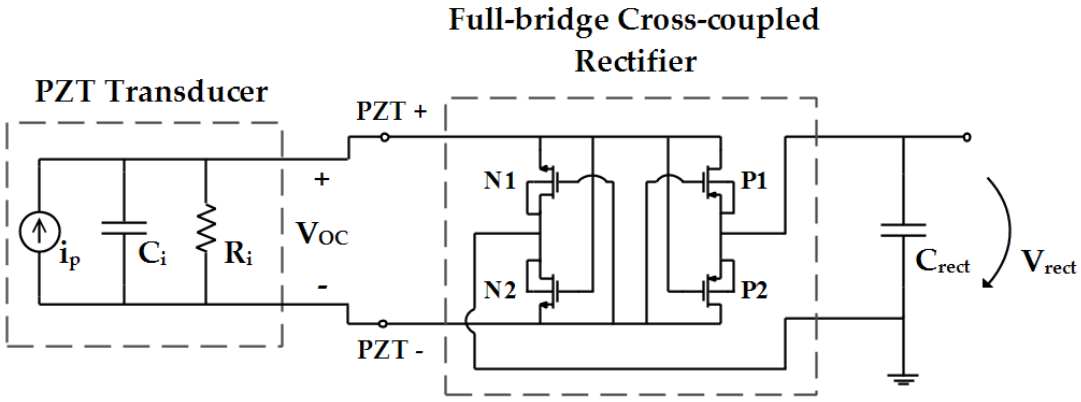

Figure 3.11: Full-Bridge Cross-coupled Rectifier

This bridge structure follows the same operation principles of the passive full-bridge rectifier, but instead of diodes it consists of two pairs of switches, implemented with CMOS transistors. The switch transistors have their gates directly driven by the rectifier's input terminals. For positive half waves, switches P1 and N2 are on, and for the negative half waves, the conducting transistor pair is P2 and N1. Each transistor is driven by the full input swing, causing the turn-on voltage to be the transistor's threshold voltage, V_{th}. The transistor pairs start conducting only after the differential input, $|(PZT+) - (PZT-)|$ according to the nomenclature in Figure 3.11, is greater than V_{th}. The voltage drop across each conducting switch is its drain-source voltage, V_{DS}, which is considerably lower than the voltage drop across a diode. For this reason, the DC output voltage can be higher with the switched structure, for the same input swing.

Ignoring the charge leakage associated to this rectifier, the power output equations of the full-bridge cross-coupled rectifier follow the same principles of

those associated to the full-bridge passive rectifier, with the difference that the voltage drop in the rectifier is no longer the diode voltage drop, V_D, but rather the drain-source voltage drop of the conducting switches, V_{DS}. Equation (3.19) gives the power output of the rectifier and Equation (3.20) presents its maximum power output, which is achieved for $V_{rect} = V_{OC}/2$, like for the full-bridge passive rectifier.

$$P_{rect} = 4.C_i.V_{rect}.f.(V_{OC} - V_{rect} - 2.V_{DS}) \tag{3.19}$$

$$P_{rect\,MAX} = 4.C_i.V_{OC}.f.\left(\frac{V_{OC}}{2} - 2.V_{DS}\right) \tag{3.20}$$

3.4 – DC-DC Converters

3.4.1 – Linear Regulators

Linear voltage regulators vary their resistance in order to deliver a constant output voltage, dissipating excess power as heat. By monitoring the output voltage, they regulate their variable resistor so that the current coming from the input may be controlled and the output voltage maintained at a constant value. Linear regulators are simple regulator circuits, commonly integrated, whose regulating device may be placed between the source and the output, in a series configuration, or parallel to the output load. These regulators can only deliver output voltage values that are lower than the input voltage values, meaning that if the output is required to be higher than the input, a different kind of regulator must be used, for example a charge pump or a boost regulator, which will be explored later in this section.

Low-dropout Regulator

The dropout voltage in a linear regulator is the minimum voltage value by which the regulator's input voltage must surpass the regulator's desired output voltage, so that the regulator can operate. If this dropout voltage is required to be as low as possible for a certain application, a low-dropout (LDO) regulator is a good solution to consider. Figure 3.12 presents an LDO regulator making use of a MOS switch as its variable resistance device, [29, 30].

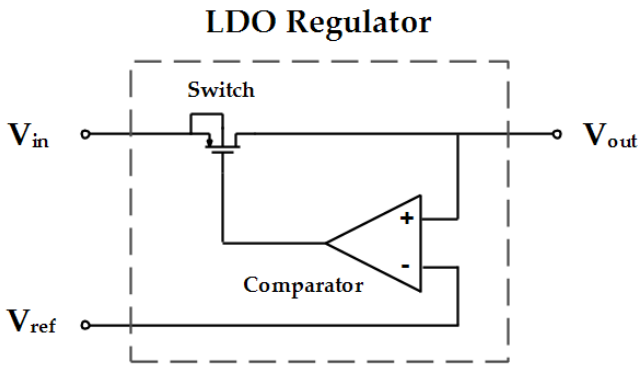

Figure 3.12: Low-dropout Regulator

The comparator has its non-inverting input connected to the output and its inverting input connected to an externally generated voltage reference, with the desired output voltage value. By comparing the regulator's output with its desired voltage, the comparator changes its output terminal value, either turning the MOS switch on for low output values or turning the MOS switch off for high output values. This guarantees that just enough current is flowing to the output to maintain the desired output voltage. If this value exceeds the desired one, the switch is turned off, stopping the input-to-output current flow. If the output is below the desired value, the switch is turned on, allowing the output to receive charge and increase its voltage value.

The efficiency of a voltage regulator can be given by the ratio between the output power and the input power. For the LDO regulator, the difference between input and output power is the sum of the power losses in the switch device and the power consumption of the control circuit, the comparator. Ignoring the control circuit's power consumption, which is commonly very low in comparison to the other quantities, the total power loss is given by $P_{loss} = (V_{in} - V_{out}) * I$, where I is the current in the input and output, flowing through the switch when it is turned on. Since this current is the same for the input and output, the efficiency of the LDO regulator can be approximated by Equation (3.22), which is a result of the considerations made for Equation (3.21).

$$\eta_{LDO} = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} \approx \frac{V_{in} * I - (V_{in} - V_{out}) * I}{P_{in}} = \frac{V_{out} * I}{V_{in} * I} \tag{3.21}$$

$$\eta_{LDO} \approx \frac{V_{out}}{V_{in}} \tag{3.22}$$

Equation (3.22) is an approximation that leads to the conclusion that the LDO regulator's power efficiency is directly related to the difference between the output and input voltage values. In order to have high power efficiencies, this difference should be minimised, ideally to the actual dropout value, the minimum difference with which the correct operation of the regulator is assured.

Given its design simplicity and low dropout voltage value, the LDO regulator may be a good option to consider as a DC-DC converter intended to work in a low-power and low-voltage application, where a down-conversion is needed and the output voltage ripple must be low. The thermal dissipation in the switch device should be considered for the design, especially for higher intended differences between the output and input voltage values. In order to keep power efficiencies high, however, this voltage difference should be as low as possible.

3.4.2 – Switched Capacitor Converters

Switched capacitor DC-DC converters, also called charge pumps, are used to convert a *DC* voltage input to a *DC* output with a different voltage level, which can be higher or lower. They can also be used to change the input's polarity. These converters use capacitors to store energy and switches to periodically change the circuit's configuration, in a way that allows the stored energy to be delivered to the output at a different voltage level.

For a step-up switched capacitor converter, in which the output voltage is higher than the input value, the capacitors are commonly charged and discharged in two distinct stages of a cycle. In the first stage, the charging process is usually done with a parallel configuration of the capacitors, which are charged up to the input's voltage value. In the second stage, the switches change the circuit's configuration, connecting those same capacitors in series with each other and the input, delivering an output voltage that is the input voltage value multiplied by an integer that is related to the number of capacitors involved.

Switched Capacitor Voltage Doubler

There are several different topologies for both step-up and step-down switched capacitor converters, depending on the desired voltage outputs or efficiency levels. Figure 3.13 presents a simple step-up topology, a switched capacitor voltage doubler, [31, 32].

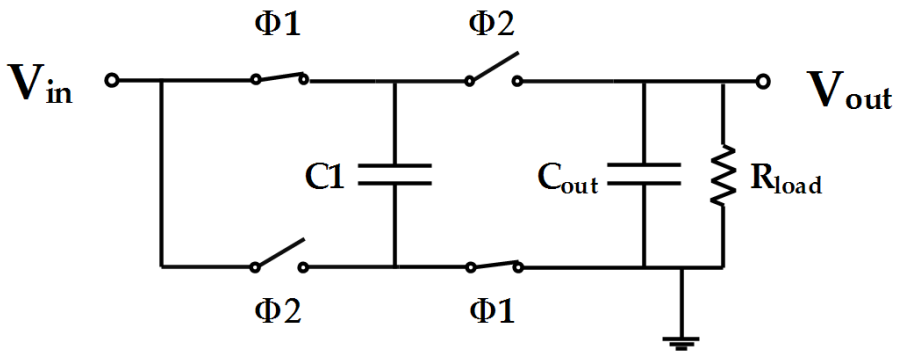

Figure 3.13: Switched Capacitor Voltage Doubler

Phase one and two (Φ_1 and Φ_2) are non-overlapping clock signals. For this topology, the converter charges capacitor C_1 during Φ_1 up to the input voltage value, V_{in}. The charge stored in this capacitor remains the same during the phase transition, $Q = C_1.V_{in}$. During Φ_2, the capacitor is connected in series with the input terminal, which makes its voltage value, V_{in}, stack with the input's voltage value, V_{in}. This causes the doubling effect, making $V_{out} = 2.V_{in}$.

The high efficiency levels of this type of converters (90% to 95%), allied to the fact that they can be fully integrated, makes them a good choice in some low-power applications. A disadvantage of these circuits is the added complexity brought by the need to design and dimension the circuits that drive the switches with the non-overlapping clocks.

3.4.3 – Magnetic Converters

Magnetic DC-DC converters make use of the voltage induced in an inductor by changes in its magnetic flux. The changing magnetic flux is created by changes in the current flowing through the inductor, and these changing currents are caused by the operation of switches, in this kind of converter. The switches are carefully timed so that the alterations in configuration of the converter circuit make use of successive increasing and decreasing of the current values through the inductor, which cause the inductor's voltage polarity to change periodically. The induced voltage in an inductor is given by

$$v = \frac{d(L.i)}{dt} = L\frac{di}{dt}. \tag{3.23}$$

Equation (3.23) supports the previous statement regarding the polarity of the voltage across an inductor. The change in the inductor's voltage polarity is explained by Lenz's Law. If the current flowing through an inductor is increasing, the terminal through which the current is entering the inductor (in the conventional current flow direction) has a higher potential than the terminal through which the current is leaving the inductor. If, in the other hand, the current is decreasing, the inductor's polarity is reversed.

A magnetic converter that delivers a lower voltage value, in relation to its input, is a step-down or buck converter. When the input voltage value is increased, the magnetic converter is called a step-up or boost converter.

Buck Converter

Figure 3.14 presents the topology of a buck converter, including the load, [33].

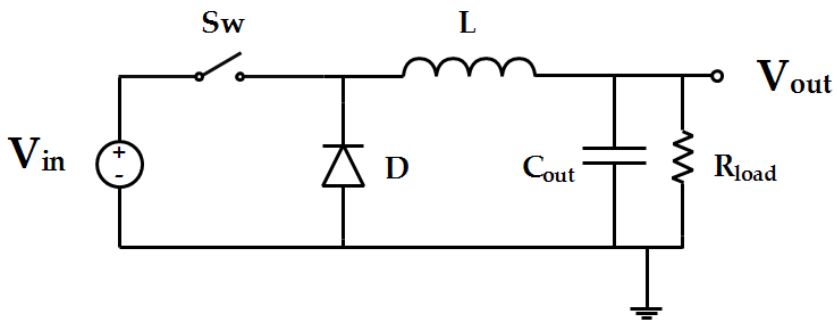

Figure 3.14: Topology of a Buck Converter

Having this figure as a reference, the operating principles of the converter are the following. When the switch is turned on, or closed, current will start flowing from the source to the load, through the inductor. Since this current is increasing in value, the inductor will have a voltage induced at its terminals that counters the source's polarity, since the positive terminal of the inductor will be the one on the left. This way, the voltage drop across the inductor will guarantee that the load will have a lower voltage value, in relation to the input. After the switch has been on for some time, the increase in current will slow down, meaning that the voltage across the inductor will be reduced, making the output voltage rise. The switch is then opened, while the current is still rising, so that there is still some voltage drop at the inductor. After the switch is opened, the voltage source is temporarily removed from the circuit, resulting in a decrease in current. The inductor, however, manages to keep the decreasing current flowing to the load, in the same direction, by using the energy stored in its magnetic field and the closed circuit created by the diode. The inductor's po-

larity is now reversed, and it acts as a temporary source to the load, making sure the output voltage does not decrease too much. The cycle is then repeated when the switch is turned on again, before the inductor discharges completely.

Depending on the amount of energy requested by the load, the converter can either work in continuous or discontinuous mode. The first mode operates in a way that does not let the current through the inductor reach zero, as described above. In the second mode, this current can reach zero. The alternation between modes is regulated by the duration of the on and off time intervals of the switch.

Boost Converter

For the boost converter, the output voltage is superior to the input voltage. This is made possible once again by charging and discharging an inductor, this time using a different circuit configuration, presented in Figure 3.15, [34].

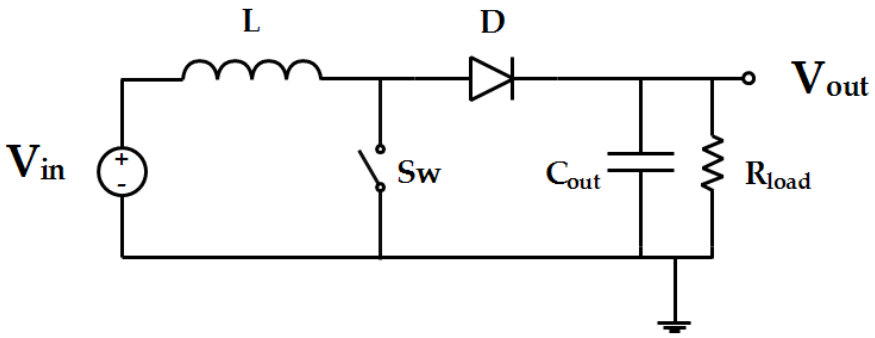

Figure 3.15: Topology of a Boost Converter

When the switch is closed, an increasing current leaves the source and flows through the inductor, charging it. The circuit can be considered as closing through the conducting switch and back to the source, since the impedance of the rest of the circuit is much higher. During this first stage, the inductor increases its magnetic field as a consequence of the increasing current, and energy is stored. The left terminal of the inductor is the positive one. After some charging time, the switch is opened. When this happens, the inductor will discharge

the energy contained in its magnetic field to try to maintain the current flowing. The new configuration of the circuit presents higher impedance to the source and inductor, forcing the current to decrease. This decrease in current changes the polarity of the discharging inductor, which starts to behave as an additional source in series with the original one, making the source and inductor voltage values stack to a higher voltage value, delivered to the output. Before the inductor is fully discharged, the switch is turned on so that the cycle returns to the first stage.

The boost converter also features continuous and discontinuous modes, which can be chosen depending on the load's energy requirements.

4

Proposed System and Circuit Design

The proposed piezoelectric energy harvesting system is presented in this chapter, including the dimensioning considerations and design discussion for each module.

A system overview is given in section 4.1, including the system's structure, the considered load requirements and transducer specifications, and the dimensioning of the external components.

The schematic and dimensioning of the full-bridge cross-coupled rectifier are presented in section 4.2. The principles and requirements that are taken into account in order to reach the proposed dimensions are explained and justified in this section.

Section 4.3 deals with the sizing process that was followed for the proposed LDO regulator. This section is divided into three subsections, each of them focusing in a different block that is part of the DC-DC converter. The first part focuses on the PMOS switch and correspondent dimensioning, the second on the comparator block, and the third part presents the implementation of the clock generator.

4.1 – Piezoelectric Energy Harvesting System Overview

System Modules

The designed piezoelectric energy harvesting system consist of two CMOS integrated modules, which are the rectifier and the DC-DC converter, and two external capacitors, one at the rectifier's output, acting as an intermediate storage device and smoothing capacitor, and the other at the DC-DC converter's output, the system output, serving as the power system's energy storage device. Similar energy harvesting system structures were used in [29, 33]. This chapter's following sections describe each designed module in detail, including schematics and dimensioning. Figure 4.1 presents a block diagram of the proposed piezoelectric energy harvesting system, with the load as the RF receiver presented in subsection 2.3.2. The greyed out blocks were not included in the design.

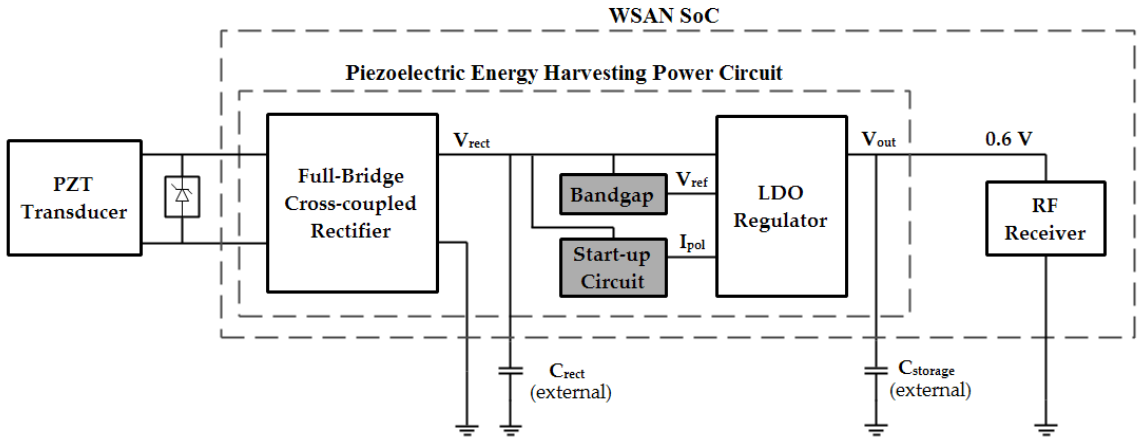

Figure 4.1: Block Diagram of the Proposed Piezoelectric Energy Harvesting Power Circuit, greyed out blocks are not included in the proposed design

The chosen rectifier and DC-DC converter designs were the full-bridge cross-coupled rectifier and the LDO regulator, as presented in Figure 4.1. A presentation of these blocks is done in the previous chapter, and the reasons that motivated the choice will be clarified in the next sections.

Load Requirements and Piezoelectric Transducer Specifications

A presentation of the load's power requirements was given in the second chapter. Table 4.1 summarizes the power requirements of the complete receiver circuit, regarding its requested *DC* current and supply voltage value, [17].

Table 4.1: Summary of the RF Receiver's Power Requirements

DC current	10 mA
V_{DD}	0.6 V

The Midé Volture™ piezoelectric transducers family, [19], was used as a reference for the proposed design, as previously stated. The transducer datasheet contains information regarding the typical outputs of the several different transducers for different vibration conditions, as well as their internal resistance and capacitance values, essential for simulations and power output predictions. Two particular harvesters were chosen from the referred family: the Midé Volture™ V21BL and the Midé Volture™ V25W harvesters. Their internal resistance and capacitance values are presented in Table 4.2, for the reference vibration frequencies of 100 Hz and 120 Hz.

Table 4.2: Summary of the Transducers' Electrical Characteristics, [19]

Transducer	**Single Wafer Capacitance @ 100 Hz**	**Single Wafer Resistance @ 100 Hz**	**Single Wafer Capacitance @ 120 Hz**	**Single Wafer Resistance @ 120 Hz**
V21BL	26 nF	950 Ω	26 nF	770 Ω
V25W	130 nF	210 Ω	130 nF	175 Ω

Depending on the vibration conditions, the electrical output of the piezoelectric transducers varies inside a range of certain values that are available in the datasheet. The chosen natural frequency is 120 Hz for the V25W harvester

and 110 Hz for the V21BL harvester. These frequencies were chosen as a reference because they represent the natural frequency of each transducer without any added tip mass. Table 4.3 presents the open circuit voltage values at each transducer's output, depending on the vibration's acceleration value, in g. The given open circuit voltage refers to a series configuration of the two wafers.

Table 4.3: Summary of the Transducers' Open Circuit Voltage values for different vibration amplitudes, [19]

Transducer	Natural Frequency (Hz)	Amplitude (g)	Open Circuit Voltage (V)
V21BL	110	0.25	3.95
		0.5	6.6
		1	12.1
V25W	120	0.25	3.2
		0.5	5.5
		1	10.1

External Components

The smoothing capacitor at the rectifier's output, C_{rect} , and the storage capacitor at the system's output, $C_{storage}$, were dimensioned having several factors in consideration, more importantly the transducer's internal capacitance and the system's output voltage ripple.

In order to guarantee a relatively stable rectifier voltage output, the C_{rect} capacitor must have a capacitance value that surpasses the transducer's internal capacitance value by a substantial difference. The internal capacitance values presented in Table 4.2 refer to a single wafer, which means that the order of magnitude of the internal capacitance of a piezoelectric transducer connected in a series or parallel configuration of its wafers is between tens of nanofarads to a few hundred nanofarads. To have a satisfactory ratio of one to a thousand, the C_{rect} capacitor should have a capacitance value with an order of magnitude that ranges from tens of microfarads to a few hundred microfarads.

Equation (4.1) defines the current in a capacitor, which is the rate of flow of charge through it, Q(t), with v(t) as the voltage across the capacitor at each instant.

$$i_c(t) = \frac{\mathrm{dQ(t)}}{\mathrm{dt}} = C.\frac{\mathrm{dv(t)}}{\mathrm{dt}} \tag{4.1}$$

From this equation, the peak-to-peak voltage ripple at the rectifier's output can be calculated by

$$V_r = \frac{\bar{I}.T}{2.C_{rect}}\ , \tag{4.2}$$

where V_r is the peak-to-peak voltage ripple at the rectifier's output, $\bar{I}$ is the average rectifier load current and T the rectifier input signal's period. Having an average load current of 10 mA and a vibration frequency of 120 Hz, the C_{rect} capacitance value can be chosen in order to define a maximum predicted voltage ripple. Using Equation (4.2), a capacitance value of 83 µF is reached in order to guarantee a peak-to-peak voltage ripple that is inferior to 500 mV. This calculation is given by

$$C_{rect} = \frac{\bar{I}.T}{2.V_r} = \frac{10\ mA * \frac{1}{120\ Hz}}{2 * 500\ mV} = 83\ \mu F\ . \tag{4.3}$$

A final capacitance value of 100 µF is chosen for the C_{rect} capacitor, thus guaranteeing the referred maximum rectifier output ripple.

In its turn, the $C_{storage}$ capacitance value directly influences the output voltage ripple of the energy harvesting system, since this capacitor is constantly being charged by the system and discharged by the load. The amount of output voltage ripple depends on the frequency at which the LDO's comparator oper-

ates (which is a direct measure of the system's response time), the current requested by the load, and the $C_{storage}$ capacitance value. A simplified visualisation of the system's output voltage ripple is given in the graph presented in Figure 4.2, in which it is considered that the transient time (or initial charging time of the storage capacitor up to the desired voltage) is surpassed and the system has reached stable operation. V_{out} is the voltage across the $C_{storage}$ capacitor, which is the system output voltage, ΔV is the total amount of voltage ripple, T_1 the capacitor's charging time and T_2 the capacitor's discharging time.

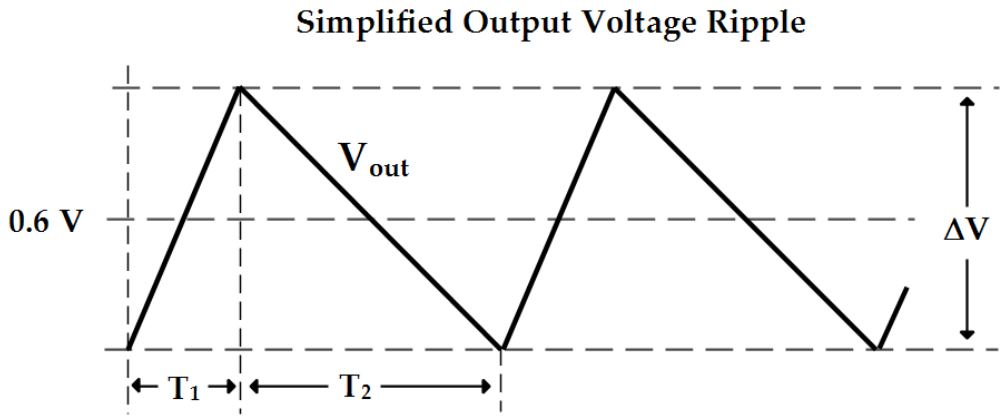

Figure 4.2: Simplified visualisation of the system's output voltage ripple

During T_1, the $C_{storage}$ capacitor is charged by the system, since the LDO's switch is turned on. In the T_2 time interval the switch is turned off, meaning that the capacitor is supplying the load with a current that is the requested load current of 10 mA. The capacitor must be dimensioned in a way that guarantees that the voltage drop that results from this discharging process is not too high, for the expected discharging time interval. This time interval is related to the LDO's comparator frequency of operation.

The relation between the discharging current I_{load} , the discharging time interval T_2, the voltage drop ΔV, and the capacitance value $C_{storage}$, is given by

$$I_{load} \cdot T_2 = \Delta V \cdot C_{storage} \cdot \tag{4.4}$$

The capacitance value is derived from this equation with the following considerations. As an ideal maximum for the output voltage drop, the value of 1 mV was chosen. The system's ability to guarantee very low output voltage ripple depends on the system's time response to the changes in its output. The comparator in this module operates at a frequency that sets the minimum time response value. Considering a typical comparator operation frequency of 100 kHz, the resulting period is 0.01 ms. With a discharging time interval, T_2, with this order of magnitude, and the maximum voltage drop stated above, the capacitance value is given by

$$C_{storage} = \frac{I_{load} \, . T_2}{\Delta \, V} = \frac{10 \, mA * \, 0.01 \, ms}{1 \, mV} = 100 \, \mu F \, . \tag{4.5}$$

Given the high capacitance values, the capacitors must be external components, not included in the integrated system. The considerations made in this section and the electrical simulations run for the system's power circuit resulted in the choice of capacitance values for the C_{rect} and $C_{storage}$ capacitors that is presented in Table 4.4.

Table 4.4: Chosen capacitance values for the system's external capacitors

Capacitor	Capacitance value (µF)
C_{rect}	100
$C_{storage}$	100

4.2 – Active Full-Bridge Cross-coupled Rectifier

The operation principles of the active full-bridge cross-coupled rectifier are presented in subsection 3.3.2.

The full-bridge cross-coupled rectifier is a good solution for a low-voltage application since the voltage drop across its switches can be significantly lower than the diode voltage drop. This full-wave rectifier can be implemented using only four MOSFET transistors. It has better performance in relation to passive rectifiers and is easier to implement than other active rectifiers, saving circuit area, which is an important factor for the application. Another advantage is the autonomous operation it is capable of, since it does not require external switch driving or any kind of external control or power supply. This is essential because the piezoelectric transducer is intended to be the only power source in the application, meaning that no other external power supply is available to guarantee the rectifier's operation.

Schematic and Sizing

The rectifier's schematic is presented in Figure 4.3, [35, 36], which includes the transistor dimensions in µm.

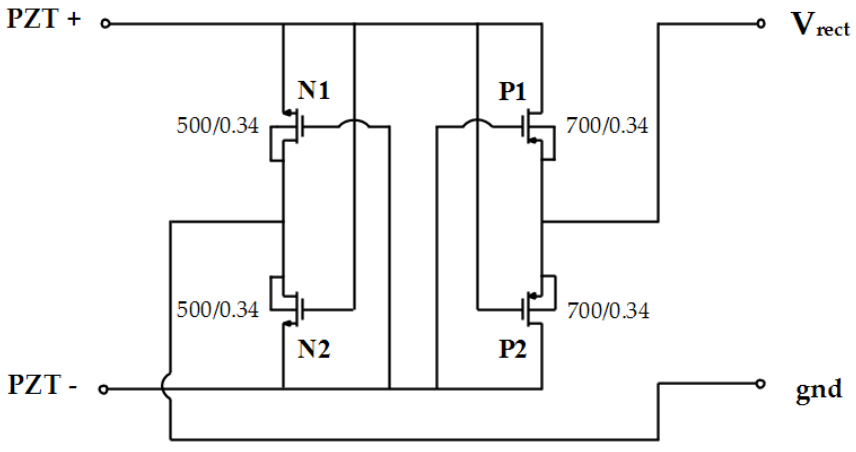

Figure 4.3: Full-Bridge Cross-coupled Rectifier Schematic, including transistor dimensions in µm (W/L)

The bulk terminals for the NMOS devices are connected to ground while for the PMOS devices they are connected to V_{rect}. These two nodes present a relatively stable voltage potential throughout the system's operation cycle, and are the highest (V_{rect}) and lowest (gnd) stable voltage potentials for the power circuit, ensuring the correct operation of the switch devices by avoiding undesirable leakage currents through the bulk terminals.

In order to maximise the total power efficiency of the rectifier, the transistors should present a low voltage drop, V_{DS}. While conducting, the devices are in the triode region. The current flowing through each device in the triode region is modelled by

$$I_D = \frac{1}{2}.\mu C_{ox}.\frac{W}{L}.\left[2.(V_{GS} - V_{th}).V_{DS} - {V_{DS}}^2\right], \tag{4.6}$$

where W and L are the transistor's width and length, respectively, V_{GS} the gate to source voltage, V_{th} the threshold voltage, C_{ox} the gate oxide capacitance per unit area and μ the charge-carrier effective mobility.

Solving (4.6) for V_{DS} results in

$$V_{DS} = \frac{-\left[\mu C_{ox}.\frac{W}{L}.(V_{GS} - V_{th})\right] \pm \sqrt{\left[\mu C_{ox}.\frac{W}{L}.(V_{GS} - V_{th})\right]^2 - 4.\left(-\frac{1}{2}.\mu C_{ox}.\frac{W}{L}\right).(-I_D)}}{2.\left(-\frac{1}{2}.\mu C_{ox}.\frac{W}{L}\right)}. \tag{4.7}$$

Considering a peak current value of 30 mA flowing through the rectifier's switches, for a default piezoelectric transducer output, and a V_{GS} voltage value of 2 V, corresponding to the full transducer output swing, the voltage drop at each device can be plotted using Equation (4.7), for different transistor aspect ratio (W/L) values. Figure 4.4 presents the variation of the voltage drop at each of the PMOS devices, depending on the device's aspect ratio.

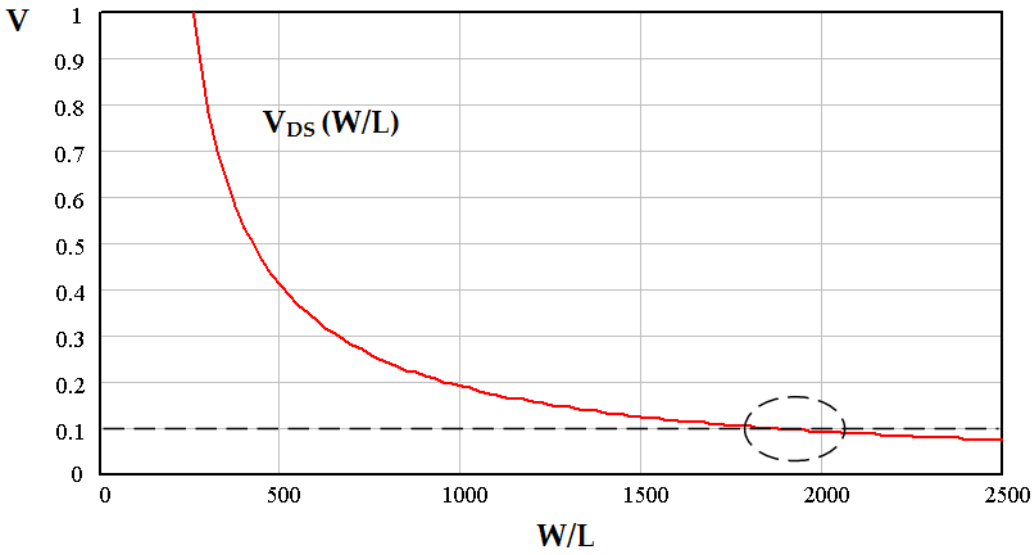

Figure 4.4: Variation of the PMOS device voltage drop for different aspect ratio values

In order to have a voltage drop at the conducting PMOS device that is close to 100 mV, given the previously stated conditions that are taken into account for the plot shown in Figure 4.4, the device's aspect ratio should be close to 2000. For a length value of 0.34 µm, which corresponds to the minimum length for the 3.3 V device models that were chosen for the design, a width value of 700 µm was chosen for the PMOS device (700/0.34 ≈ 2059). The same procedure was followed to determine the dimensions of the NMOS devices.

For each half wave of the transducer's input signal, the conjunction of the rectifier and the C_{rect} capacitor will present an impedance to the piezoelectric transducer that is equal to the capacitor's impedance at the input signal's frequency in series with one PMOS device and one NMOS. The conducting switch resistance value, rds_{on}, is given by Equation (4.8), in the linear or triode region.

$$rds_{on} \approx \frac{1}{\mu C_{ox}.\frac{W}{L}.(V_{GS} - V_{th})} \tag{4.8}$$

The chosen transistor models have a maximum voltage value of 3.3 V and a low V_{th}, with a minimum channel length of 340 nm. The final dimensions of the rectifier transistors are given in Table 4.5, along with their calculated rds_{on} resistance values and V_{DS} voltage drop values, for the conditions used to determine the transistor dimensions.

Table 4.5: Full-Bridge Cross-coupled rectifier transistor dimensions and characteristics

Transistor	W (µm)	L (µm)	multiplier	rds_{on} (Ω)	V_{DS}(mV)
N1	500	0.34	5	1.4	43
N2	500	0.34	5	1.4	43
P1	700	0.34	7	2.9	90
P2	700	0.34	7	2.9	90

Table 4.6 presents the considered values used for the dimensioning of the rectifier and the dimensioning of the rest of the proposed circuit. These values are based on a 130 nm CMOS technology.

Table 4.6: Important technology-related values considered in the dimensioning of the proposed circuit

$\mu_N . C_{ox}$	$\mu_P . C_{ox}$	C_{ox}	V_{thN}	V_{thP}
300 µA.V^{-2}	100 µA.V^{-2}	12.3 fF. µm^{-2}	0.38 V	0.33 V

4.3 – Low-dropout Regulator

The LDO regulator was presented in the third chapter, along with its approximate power efficiency equation. The chosen configuration for this system's LDO regulator is presented in Figure 4.5, with the V_{DD} and V_{SS} terminals of the comparator connected to V_{rect} and ground, respectively.

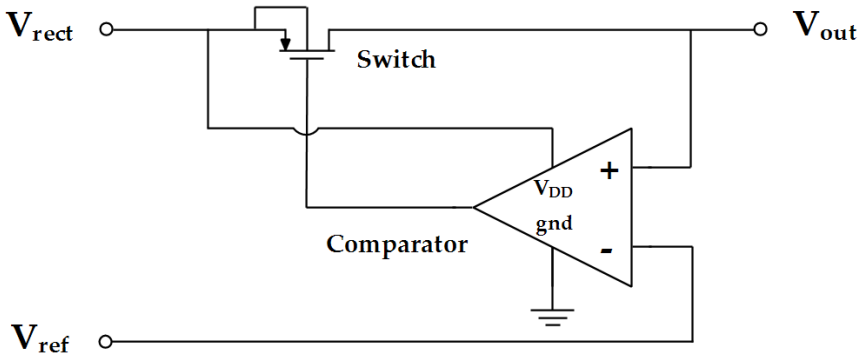

Figure 4.5: Low-dropout Regulator

This type of linear regulator is a good choice for the proposed system because the application requires a step-down DC-DC converter that is able to operate at low voltage inputs, which are the outcome of occasional low vibration levels of the piezoelectric transducer. The simplicity and inductorless characteristics of this converter guarantee reduced circuit area and cost, with the possibility of full integration. At the cost of some efficiency loss for relatively big discrepancy between the input and output values, this converter is capable of delivering an output with reduced voltage ripple, regardless of the voltage input values originated at the rectifier's output. This is very important when the load circuit is an RF receiver with a low PSRR, making it susceptible to variations at its voltage supply rail, which can compromise its operation.

The following subsections will present the LDO regulator with greater detail, including the considerations and dimensioning of the PMOS switch, the

comparator and its main constituents, and finally the clock generator circuit, which was included in the designed regulator module.

4.3.1 – PMOS Switch

Choice of device

The switch was implemented making use of a PMOS device. To turn on a MOS switch, its gate-to-source (or source-to-gate for PMOS) voltage must surpass its threshold voltage, $|V_{GS}| > |V_{th}|$. Having in mind that the source voltage is V_{rect}, the highest potential in the circuit, the following explanation justifies the PMOS choice.

For the PMOS device, the gate can be successfully driven by either the highest (turned off) or the lowest (turned on) voltage potentials in the circuit, which are made available by the rectifier. If an NMOS device was to be used, however, a voltage value that is superior to V_{rect} would have to be generated to drive the device's gate and turn it on. This means that the V_{GS} voltage would have to surpass the V_{rect} voltage by an amount of at least the V_{th} voltage value, which is less desirable.

Switch power losses

The equation for the approximate total conversion efficiency of the LDO regulator, (3.21), was presented in subsection 3.4.1. This equation contains a total power loss variable that includes the switch power loss. This switch-related power loss is the sum of the power dissipated by thermal effect in the conducting switch and the dynamic power at the switch's gate.

The power dissipated in the switch by Joule heating is given by

$$P_{DJ} = \bar{I}^2.rds_{on} = \frac{\bar{I}^2}{\mu.C_{ox}.\left(\frac{W}{L}\right).(V_{GS} - V_{th})}, \tag{4.9}$$

where $\bar{I}$ is the average current flowing through the conducting switch. The dynamic power at the device's gate is given by

$$P_{Dgate} = {V_{rect}}^2 . f . C_{gate} = {V_{rect}}^2 . f . C_{ox} . W . L , \quad (4.10)$$

with C_{gate} as the device's gate capacitance, f the frequency of the gate signal transitions, and V_{rect} the voltage correspondent to the charging or discharging process of the gate capacitance, for each transition.

Sizing

The average current value flowing through the switch is the system's output requested DC current, 10 mA. With this current value and a V_{GS} voltage for the conducting switch that is the V_{rect} voltage, with an average value of 1.8 V for default transducer outputs, the relation between the power dissipated in the switch by heating effect (while conducting) and the transistor's aspect ratio is given in Figure 4.6, using Equation (4.9).

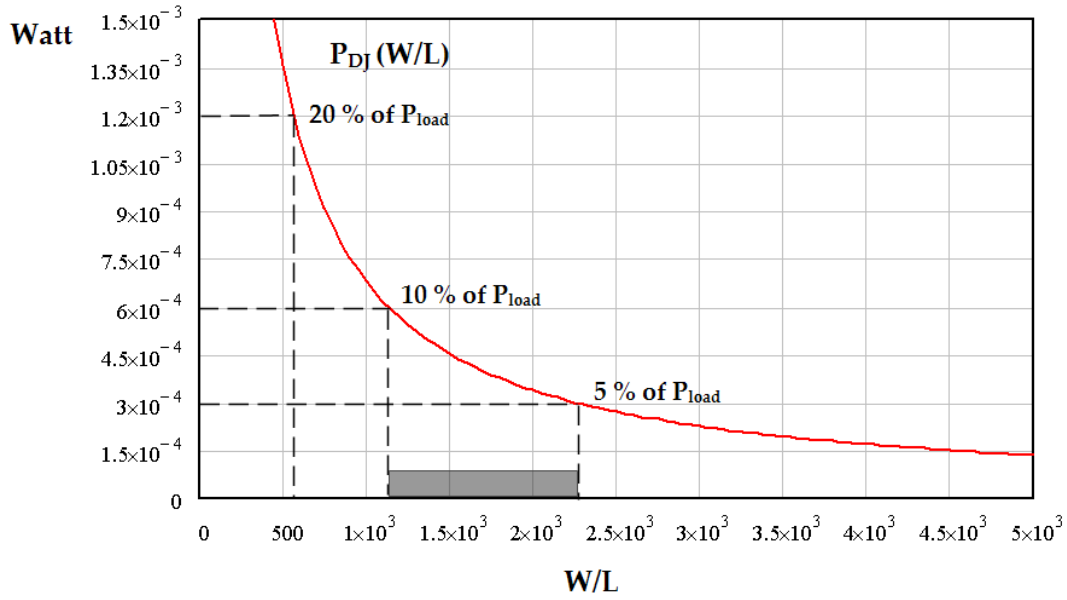

Figure 4.6: Variation of the power dissipated at the conducting switch by heating effect, with the transistor's aspect ratio as a variable (Pload=6mW)

The switch dimensions were chosen having in consideration the power requested by the load, $P_{load} = 0.6\,V * 10\,mA = 6\,mW$. It was decided that the switch should not dissipate an amount of power by heating effect (while conducting) that surpassed 10% of the load requested power. The aspect ratio was chosen in order to guarantee that this power dissipation would be between 5% and 10% of the referred load requested power. A minimum length value of 0.34 µm was defined, and the width was set at 600 µm, in order to have an aspect ratio that complies with the previously mentioned considerations ($600/0.34 \approx 1765$, see Figure 4.6). The LDO regulator's switch dimensions are presented in Table 4.7.

Table 4.7: PMOS Switch dimensions and conducting characteristics

Device	**W (µm)**	**L (µm)**	**m**	**fingers**	$\boldsymbol{rds_{on}}$ **(Ω)**	$\boldsymbol{P_{DJ}}$ **(µW)**
PMOS Switch	600	0.34	6	2	3.8	385

4.3.2 – Comparator

The simplified schematic of the designed comparator is presented in Figure 4.7.

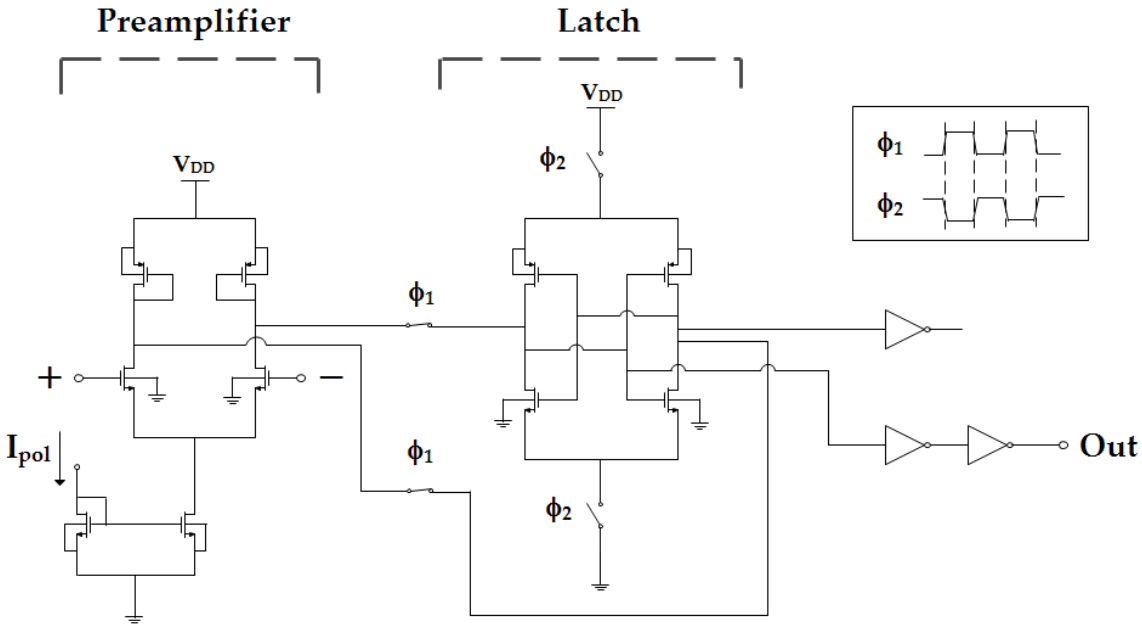

Figure 4.7: Latch Comparator's Simplified Schematic

The preamplifier stage is responsible for amplifying the differential input, which is then applied to the latch stage, where the output is set according to the input's polarity. The output of the latch circuit is set to the V_{DD} supply voltage value (V_{rect}) when the non-inverting input of the comparator (+, V_{out}) has a higher voltage value than the inverting input (-, V_{ref}). This situation corresponds to the case when $V_{out} > V_{ref}$, and in this situation the switch must be turned off, meaning that the output of the comparator must be set to V_{rect}. When $V_{out} < V_{ref}$, the non-inverting input has a lower voltage value than the inverting input, and the switch is turned on by the 0 V voltage value at the comparator's output. This correspondence is summarised in Table 4.8.

Table 4.8: Summary of the Comparator's output-input correspondence

Input	Output	Switch
$V_{out} < V_{ref}$ $(+< -)$	0 V	ON
$V_{out} > V_{ref}$ $(+> -)$	V_{rect}	OFF

Two pairs of switches, presented in Figure 4.7, are driven by two non-overlapping clocks, Φ1 and Φ2, so that the comparator may function properly. These switches guarantee that the two stages of the comparator's operation take place separately. The first one is the amplification stage, occurring during phase one, when the switches driven by Φ1 are turned on. During this stage, the output of the preamplifier is delivered to the latch circuit. During the decision stage, the second one, the switches driven by Φ1 are opened and the ones driven by Φ2 are turned on, connecting the latch circuit to the V_{DD} supply voltage and ground. During this stage the comparator's output is set by the latch circuit to V_{DD} or ground depending on the latch circuit's input. The inverters at the comparator's output serve as output buffers, allowing the comparator to drive the power switch's gate with either V_{rect} or 0 V. By feeding the comparator with V_{rect} as its V_{DD} supply voltage, the power switch of the LDO regulator can be correctly switched off by the comparator, when its output is set at that same voltage, which is the voltage value at the switch's source, making $V_{SG} = 0\,V$.

The design does not include the generation of the voltage reference of 0.6 V, V_{ref}, which is considered as being generated by a bandgap voltage reference circuit and applied to the inverting input of the comparator.

This subsection includes important considerations regarding the preamplifier and latch circuits and presents the dimensioning of each of these stages.

Preamplifier

The preamplifier consists in a CMOS differential pair with PMOS active loads. Figure 4.8 presents the preamplifier's schematic, with P1 and P2 as the PMOS active load, N1 and N2 the NMOS transistors of the differential pair and N_{CM1} and N_{CM2} the transistors that constitute the current mirror.

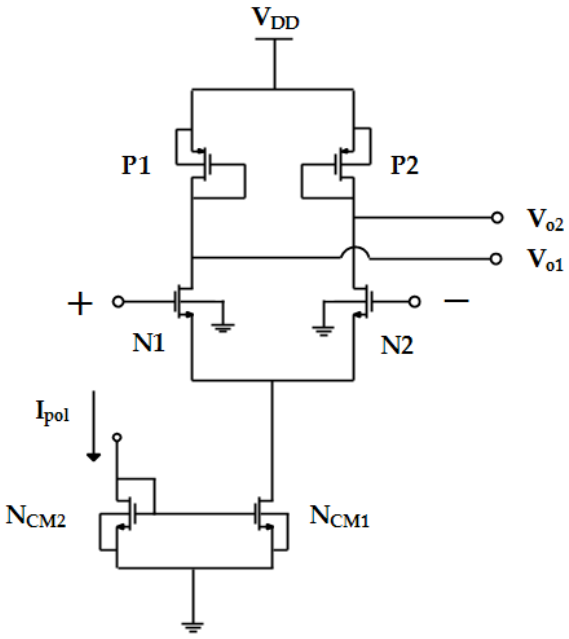

Figure 4.8: Preamplifier Stage of the Comparator

The current reference I_{pol} is intended to be generated by a start-up circuit, not included in this design, and its current value will be presented after some sizing considerations.

The differential gain expression for the CMOS differential pair in a common-source configuration is given by Equation (4.11), [37], where V_{IN+} and V_{IN-} are the voltages at the two inputs, gm_{N1} is the transconductance for the N1 NMOS device (or N2), and R_{load} is the impedance presented by the PMOS device serving as the active load.

$$AV_{diff} = \frac{V_{O1} - V_{O2}}{V_{IN+} - V_{IN-}} = -gm_{N1} \,.\, R_{load} \tag{4.11}$$

Given the PMOS active load configuration, with its gate terminal connected to its drain, the preamplifier's active load can be approximated to a resistor, for AC signals, with a correspondent expression given by Equation (4.12), for which gm_{P1} is the PMOS device's transconductance and gds_{P1} the device's conductance (the approximation was made considering $gm_{P1} \gg gds_{P1}$).

$$R_{load} = \frac{1}{gm_{P1} + gds_{P1}} \approx \frac{1}{gm_{P1}} \tag{4.12}$$

Substituting this last expression in Equation (4.11), the differential gain can be given by

$$AV_{diff} = -\frac{gm_{N1}}{gm_{P1}}. \tag{4.13}$$

The transistor's transconductance in saturation is given by

$$gm = 2.\sqrt{K.I_D} = 2.\sqrt{\frac{1}{2}.\mu.C_{ox}.\left(\frac{W}{L}\right).I_D} = \sqrt{2.\mu.C_{ox}.\left(\frac{W}{L}\right).I_D}. \tag{4.14}$$

Substituting Equation (4.14) in Equation (4.13) leads to the approximated differential gain expression given by Equation (4.15), in which the relation between the NMOS and PMOS transistor dimensions is already featured.

$$AV_{diff} = -\frac{\sqrt{2.\mu_N.C_{ox}.\left(\frac{W}{L}\right)_{N1}.I_D}}{\sqrt{2.\mu_P.C_{ox}.\left(\frac{W}{L}\right)_{P1}.I_D}} = -\sqrt{\frac{\mu_N.C_{ox}.\left(\frac{W}{L}\right)_{N1}}{\mu_P.C_{ox}.\left(\frac{W}{L}\right)_{P1}}} \approx -\sqrt{3.\frac{\left(\frac{W}{L}\right)_{N1}}{\left(\frac{W}{L}\right)_{P1}}} \tag{4.15}$$

The sizing of the preamplifier transistors was done by choosing a differential gain of 15 V/V. Substituting this value in Equation (4.15), and considering an absolute gain value, the relation between the dimensions of the NMOS and PMOS transistors of the preamplifier stage is given by

$$AV_{diff} = 15 = \sqrt{3.\frac{\left(\frac{W}{L}\right)_{N1}}{\left(\frac{W}{L}\right)_{P1}}} \leftrightarrow \frac{\left(\frac{W}{L}\right)_{N1}}{\left(\frac{W}{L}\right)_{P1}} = 75\,. \tag{4.16}$$

In order to meet the gain requirements, the dimensions presented in Table 4.9 were used for the preamplifier transistors. The I_{pol} *DC* current value was set at 10 µA.

Table 4.9: Preamplifier transistor dimensions

Transistor	W (µm)	L (µm)	multiplier	fingers
N1	11.25	1	2	1
N2	11.25	1	2	1
P1	1.5	10	2	1
P2	1.5	10	2	1
N_{CM}1	10	0.34	1	5
N_{CM}2	10	0.34	1	5

Latch Circuit

The schematic for the comparator's latch circuit, including the switches and output inverters, is given in Figure 4.9.

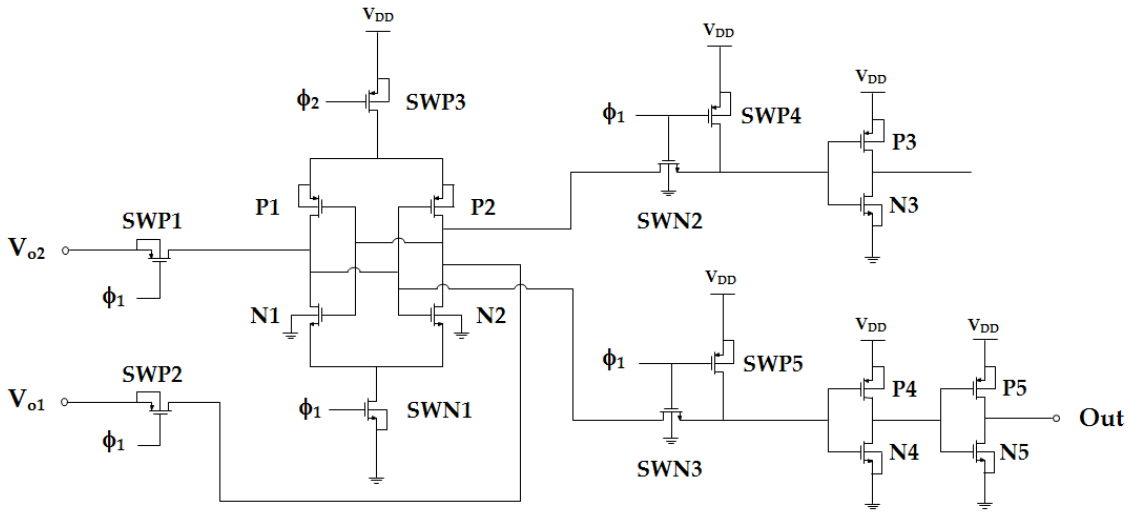

Figure 4.9: Latch Circuit of the Comparator, including switches and output inverters

Switches SWP1, SWP2, SWP3 and SWN1 are the ones previously presented in Figure 4.7. Device SWN1 is driven by phase one, Φ1, instead of phase two like in Figure 4.7, because it was decided that it should be an NMOS switch, given its connection to ground, and phase two could only drive its gate directly if it were a PMOS device. Since the two phases are non-overlapping clocks, phase one drives the SWN1 switch in order to guarantee proper operation results. Devices P3, P4, P5 and N3, N4 and N5 constitute the output inverters also presented in Figure 4.7. It should be noted that the inverter composed of devices N3 and P3 serves the purpose of matching the output loads of the two nodes of the latch circuit's outputs. It is therefore included to assure the circuit's symmetry up to the first stage of inverters.

Given the latch circuit's simplified architecture shown in Figure 4.7, a problem related to the circuit's operation arises, for a specific period of time during the operation cycle. When Φ1 is at a low level, meaning that switches SWP1 and SWP2 are turned on and SWP3 and SWN1 are turned off, the gates

of the devices at the first stage of inverters, devices P3, N3, P4 and N4, are short-circuited to the latch circuit input terminals, V_{O1} and V_{O2}. When this happens, the signal path bypasses the decision stage, meaning that the output of the latch circuit is not guaranteed to be either close to ground or V_{DD}, with the possibility of being in an intermediate level. When these intermediate level voltages are applied to the gates of the transistors belonging to the first stage of inverters, it is not possible to assure that one of each inverter's devices (either the NMOS or the PMOS device) will be cutoff and the other one in the triode region, as it is supposed to happen for an inverter's normal operation. What is likely to occur is that both of the devices will be in saturation, [37], resulting in a path from V_{DD} to ground with moderate levels of current, which increases power consumption and compromises the output voltage, which will also be an intermediate voltage level instead of either ground or V_{DD}.

In order to solve this intermediate voltage level problem, the structures comprised of devices SWN2, SWP4, SWN3 and SWP5 were added to the design. Since this problem arises during low voltage levels of Φ1, the NMOS switches SWN2 and SWN3, driven by Φ1, were included to isolate the inverters from the input during those periods. The PMOS switches SWP4 and SWP5, also driven by Φ1, serve as pull-up devices, setting the voltage at the inverters' inputs at a default level of V_{DD}, during those same periods. This means that the comparator turns the power switch off by default, during low level voltages of Φ1. The added structure assures that either a voltage level that is close to ground or V_{DD} will be at each inverter's input, guaranteeing the correct operation of these output inverters.

The sizing of the latch circuit transistors followed some common considerations for all the devices. The length presents the minimum value of 0.34 μm for all the transistors. The ratio between the width of NMOS and PMOS devices was considered as approximately one third, given the inverse ratio between the charge-carrier effective mobility values of the NMOS and PMOS devices, $\mu_N \approx 3 * \mu_P$. Table 4.10 presents the dimensions of the latch circuit transistors.

Table 4.10: Latch Circuit transistor dimensions

Transistors	W (µm)	L (µm)	multiplier	fingers
P1, P2, P3, P4, P5, SWP1, SWP2, SWP3, SWP4, SWP5	1	0.34	1	1
N1, N2, N3, N4, N5, SWN1, SWN2, SWN3	0.33	0.34	1	1

4.3.3 – Clock Generator

The clock generator is the circuit responsible for generating the clocks previously named as phase one and two, which are responsible for driving the switches of the comparator circuit. The chosen architecture for the clock generator was an inverter ring of five inverters followed by a NOR gate based structure that delivers two non-overlapping clocks (Φ1 and Φ2) with the same frequency as the signal generated by the inverter ring oscillator (Φ0). Figure 4.10 presents the architecture of the clock generator.

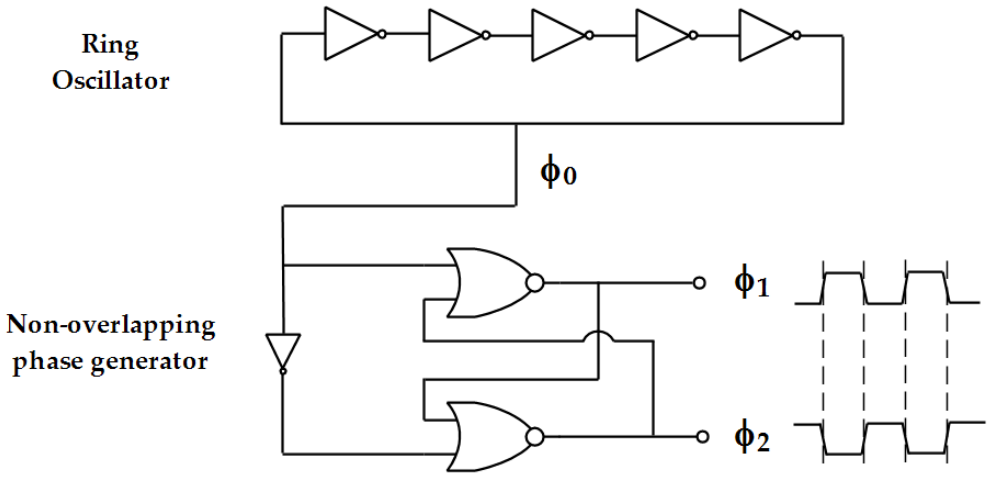

Figure 4.10: Clock Generator's Architecture

With an odd number of inverters in the ring, in this case five inverters, it is possible to create an oscillator with a frequency that depends on the propagation delay of each inverter. The resulting oscillation frequency of an inverter ring oscillator is given by Equation (4.17), in which N is the number of inverters in the ring and t_{PD} the average propagation delay of each of them.

$$f_{osc} = \frac{1}{2.N.t_{PD}} \tag{4.17}$$

Since rise and fall times have different values, the average propagation delay is given by

$$t_{PD} = \frac{t_{rise} + t_{fall}}{2}. \tag{4.18}$$

The transition of the output level from a high level to a low one, or the other way around, has a time constant that is defined by the RC circuit that is formed by the PMOS device of the inverter (in the rising case) or the NMOS device (in the falling case) and the load capacitance at the inverter's output. When the inverter's input has a high level, the PMOS is in the triode region and the NMOS is cutoff, meaning that the load capacitance will charge from the V_{DD} supply rail, through the PMOS device, whose rds_{on} value (Equation (4.8)) will define the resistance value of the RC circuit. On the other hand, when the inverter's input has a low value, the NMOS device will be conducting, discharging the load capacitance to ground.

Figure 4.11 gives a representation of the described transitions.

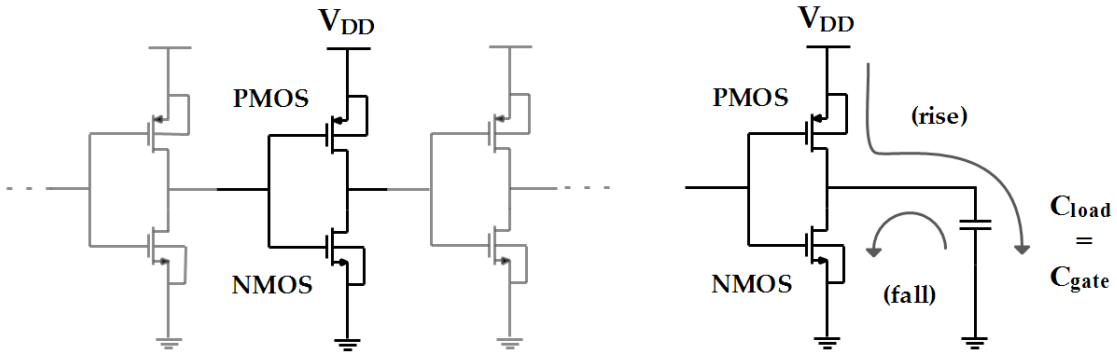

Figure 4.11: Visualisation of the operation of the oscillator ring inverters

Equations (4.19) and (4.20) define these distinct time delays, if parasitic depletion capacitances and parasitic capacitances of the wires are ignored.

$$t_{rise} = \frac{C_{load}.\left(\frac{V_{DD}}{2}\right)}{\frac{1}{2}.\mu_P.C_{ox}.\left(\frac{W}{L}\right)_P.(V_{DD} - V_{thP})^2} \quad (4.19)$$

$$t_{fall} = \frac{C_{load}.\left(\frac{V_{DD}}{2}\right)}{\frac{1}{2}.\mu_N.C_{ox}.\left(\frac{W}{L}\right)_N.(V_{DD} - V_{thN})^2} \quad (4.20)$$

In the two previous equations, μ_P and μ_N are the charge-carrier effective mobilities of the PMOS and NMOS devices, respectively. V_{thP} and V_{thN} are the threshold voltages of the two types of devices and C_{load} is the load capacitance for the inverter, which corresponds to the input gate capacitance of the next inverter in the ring (which has the same transistor dimensions), given by

$$C_{load} = C_{gate} = C_{ox}.(W.L)_P + C_{ox}.(W.L)_N\,. \quad (4.21)$$

The sizing of the transistors that constitute the inverters of the inverter ring was done using these equations. The desired oscillation frequency was set as 100 kHz, since it roughly represents a frequency that is one thousand times greater than the typical vibration frequencies of the piezoelectric transducer. With an initial rough estimation, the five inverters number was set as the lowest odd number of inverters that could guarantee the order of magnitude of the desired frequency. Since the V_{DD} voltage is in fact the V_{rect} voltage at the rectifier's output, an average typical value of 1.8 V was considered for the calculations. The widths of the transistors were set at minimum values, W_N =0.16 μm and W_P =0.48 μm, in order to minimise the transistors' aspect ratios, so that the delay times can be increased, according to (4.19) and (4.20). Having $L_N = L_P = L$, Equation (4.22) can be used to determine the length values of the transistors. Using (4.20) and (4.21), t_{fall} is given by

$$t_{fall} = \frac{C_{ox}.(L.(W_P + W_N)).\left(\frac{V_{DD}}{2}\right)}{\frac{1}{2}.\mu_N.C_{ox}.\left(\frac{W_N}{L}\right)_N.(V_{DD} - V_{thN})^2}. \quad (4.22)$$

Having Equation (4.17) in mind, an oscillation frequency of 100 kHz corresponds to t_{PD}= 1 µs. Considering $t_{rise} = t_{fall}$, Equation (4.18) leads to $t_{fall} = t_{PD} = 1\ \mu s$. Using Equation (4.22), the length value was defined as 50 µm.

The chosen dimensions of the inverter transistors are presented in Table 4.11.

Table 4.11: Dimensions for the Inverter Ring transistors of the Clock Generator

Transistor	W (µm)	L (µm)	multiplier	fingers
PMOS	0.48	50	1	1
NMOS	0.16	50	1	1

The inverter connected to the NOR gates in Figure 4.10 was dimensioned to present a very reduced time propagation delay, contrary to what was done for the inverters in the inverter ring. The dimensions of this inverter's transistors are the same as the dimensions of the transistors of the dimensioned NOR gates, given in Table 4.12. The ratio of three between the PMOS and NMOS widths was not considered in these devices.

Table 4.12: Clock Generator's small delay inverter and NOR gate transistor dimensions

Transistor	W (µm)	L (µm)	multiplier	fingers
PMOS	0.16	0.34	1	1
NMOS	0.16	0.34	1	1

The NOR gates included in the design have a standard architecture, presented in Figure 4.12.

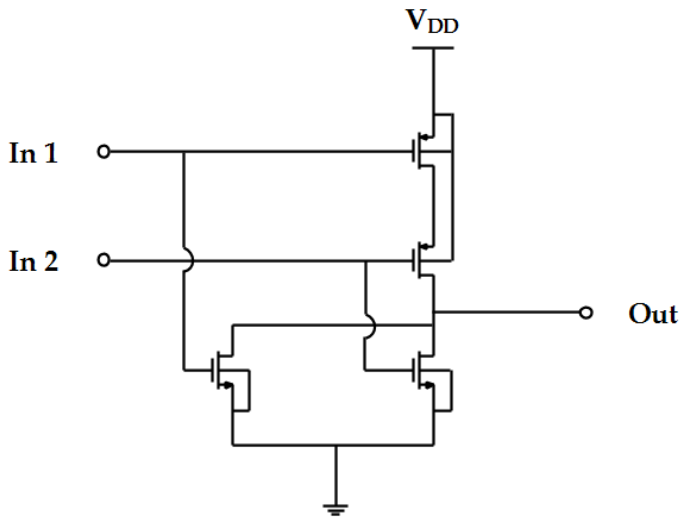

Figure 4.12: NOR gate Schematic

The whole presented clock generator circuit delivers two non-overlapping clocks, Φ1 and Φ2, with a theoretically dimensioned oscillation frequency of 100 kHz. Chapter five presents some simulations of the clock generator circuit, allowing the visualisation of the clock signals and the calculation of the actual oscillation frequency of the dimensioned circuit.

5

Electrical Simulations and Layout

This chapter presents the electrical simulations that were run for the proposed circuit and briefly introduces the most important considerations made for the complete circuit layout.

Section 5.1 is divided into three subsections. In the first subsection, the circuit used as the piezoelectric transducer is revisited, and the circuit that was designed to serve as the system's load, for simulation purposes, is introduced. The second subsection presents the simulations that were run for the rectifier module. The third subsection offers the simulations regarding the complete proposed system. In this subsection, both the system input characteristics and output requirements are varied, in order to test the system's limits of operation and promote its versatility.

The complete circuit layout is briefly addressed in section 5.2. It includes the most relevant considerations that were taken into account for the layout of the power circuit and the control circuit.

5.1 – Electrical Simulations

This system was designed for a 130 nm CMOS technology and it was simulated using BSIM3v3 models with a maximum voltage value of 3.3 V.

5.1.1 – Piezoelectric transducer and Load circuits used for the simulations

Piezoelectric Transducer Equivalent Circuit

Given the transducer output levels presented in Table 4.3, a Thevenin equivalent for the transducer equivalent circuit was chosen for simulations, so that the open circuit voltage could be directly used at the transducer's source. The transducer chosen for the default system input situation was the Midé Volture™ V25W harvester, vibrating at 120 Hz with an amplitude of 1 g. This situation corresponds to an open circuit voltage amplitude of 10.1 V for a series configuration of the two wafers, as is presented in the referred table. Since the desired configuration is a parallel of the two wafers, in order to maximise current output, the considered open circuit voltage amplitude is approximated to 5 V, $V_{pk} = 5\,V$. Figure 5.1 presents the circuit used to simulate the piezoelectric transducer for the chosen default system input.

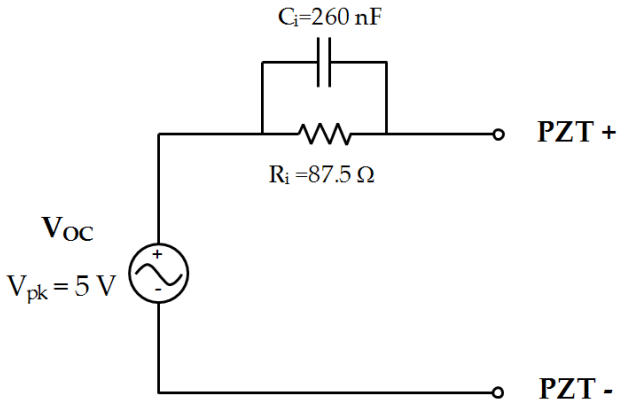

Figure 5.1: Piezoelectric Transducer's Equivalent Circuit with the chosen default system input values

Load Circuit used for simulations

For reasons concerning the very distinct frequency values involved in each circuit's signals, the RF receiver and energy harvesting system were not simulated in conjunction. To simulate the system's load, the circuit presented in Figure 5.2 was used, in which the transistor dimensions are in µm (W/L). This circuit consists in a current mirror driving an approximate *DC* current of 10 mA from the energy harvesting system's output, in order to emulate that previously presented load requirement. With the current mirror structure, it is guaranteed that the load current starts flowing only after the storage capacitor has accumulated some voltage across its terminals, in this case the saturation voltage, V_{DSAT}, that allows the current mirror transistor connected to the storage capacitor to be saturated. This load response is more appropriate to emulate the RF receiver operation than an ideal *DC* current or a resistor.

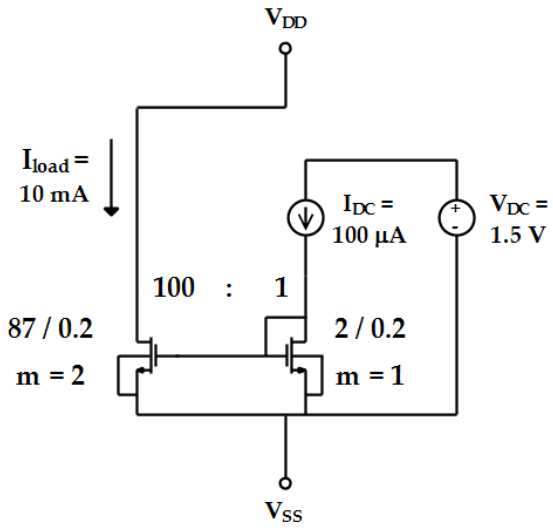

Figure 5.2: Load Circuit used for the simulations

5.1.2 – Simulations regarding the Rectifier

For the following simulations of the rectifier module, the schematic chosen for the test setup is the one presented in Figure 5.3.

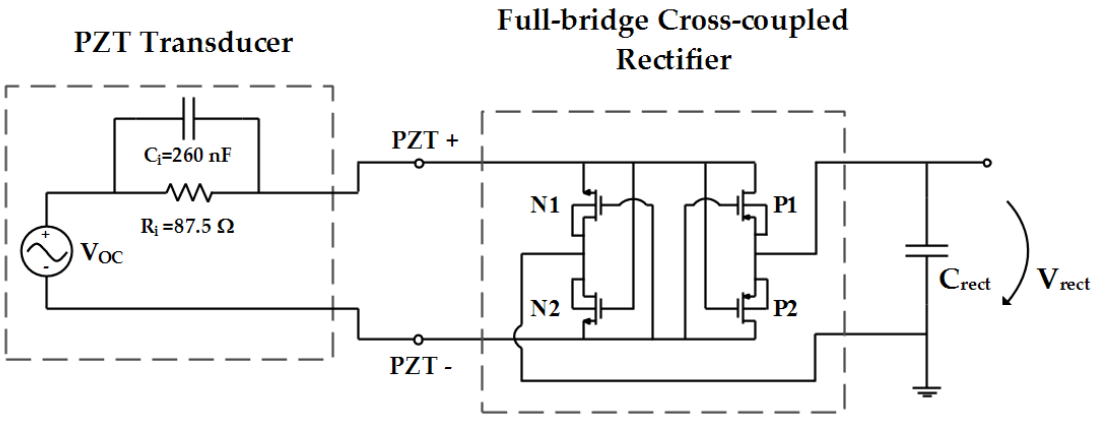

Figure 5.3: Schematic used for the simulations of the Rectifier module

Simulations for the Default System Input

The following simulation of the rectifier module, presented in Figure 5.4, was done for the default system input situation, which corresponds to a 5 V amplitude of the transducer's AC voltage source, $V_{pk} = 5\,V$.

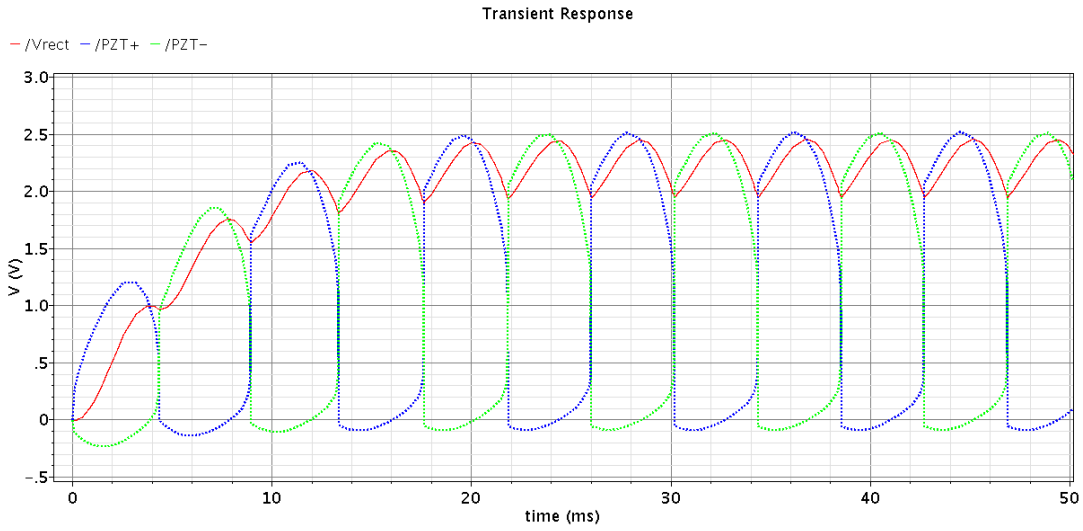

Figure 5.4: Simulations of the Rectifier module for the default system input, $V_{pk} = 5\ V$

The PZT+ and PZT- voltage signals (green and blue dotted signals in the figure) present a peak voltage that is approximately half the peak voltage of the transducer's source. This is due to the voltage drop at the transducer's internal resistance.

The rectifier's output voltage ripple is related to the capacitance value of the C_{rect} capacitor, and it is a negative consequence of a trade-off problem associated to it. The voltage ripple can be reduced by substantially increasing the capacitance value. However, this solution results in an increased initial charging time of the C_{rect} capacitor, which may be undesirable for the application. Moreover, the capacitance value of $100\ \mu F$ represents a considerably large capacitor, and larger capacitors should be avoided. Figure 5.5 presents a simulation done for the same transducer output, but with $C_{rect} = 1\ mF$. The PZT+ and PZT- voltage signals are not included for the graph to be easily interpreted.

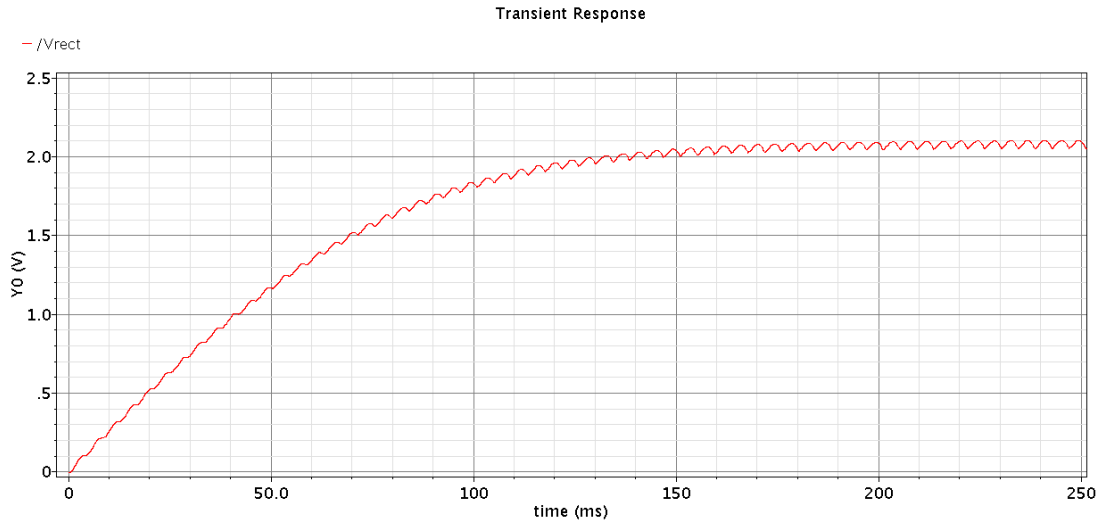

Figure 5.5: Simulation of the Rectifier module for the default system input, with $C_{rect} = 1\ mF$

Simulations for different outputs of the piezoelectric transducer

In order to test the limits of operation of the rectifier, in terms of voltage amplitude at the rectifier's input, several different peak voltage values at the transducer's AC voltage source were used. The reduction in this input value, in relation to the default system input situation, emulates the reduction in the transducer vibration amplitude.

The rectifier is able to operate with low amplitude inputs. It is able to perform rectification with a transducer's peak voltage as low as 200 mV, for example, although the V_{rect} signal only stabilizes after a transient time that is superior to one second, at an approximate voltage level of 150 mV. For transient time intervals in the same order of magnitude as those achieved for the default system input, with an approximate transient period of 20 ms, peak voltage values of a few hundred millivolts should be considered. Figure 5.6 presents the simulation results for $V_{pk} = 0.6\ V$.

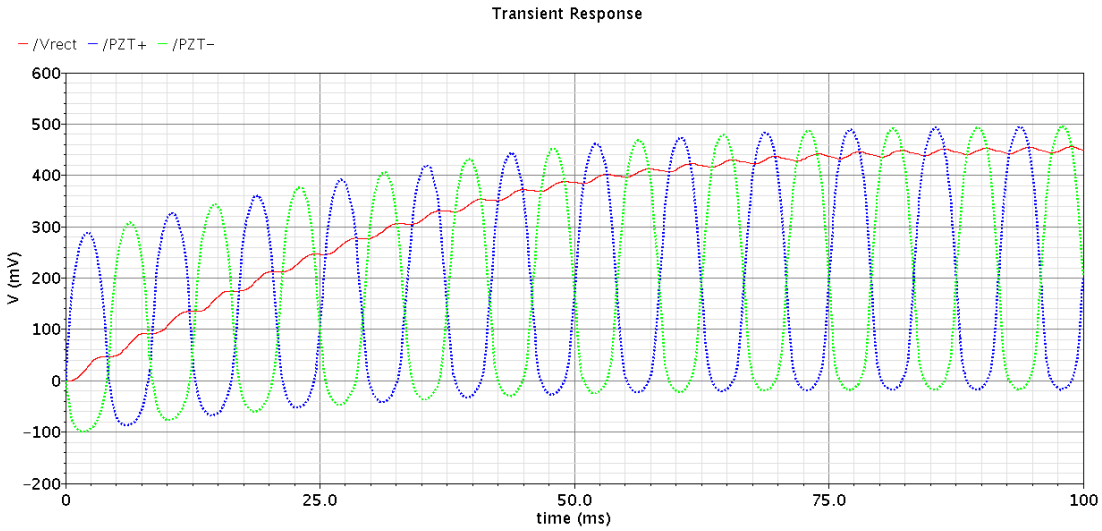

Figure 5.6: Simulation of the Rectifier module with $V_{pk} = 0.6\,V$

Since the system's designed DC-DC converter is a step-down converter, the V_{rect} voltage must be higher than the desired system output voltage, 0.6 V. Although the rectifier is able to operate for much lower input amplitudes, the minimum input amplitudes for the rectifier, operating in the proposed system, are set by the system's requirements. Due to the fact that there is an internal voltage drop at the transducer and that the actual rectifier also presents some voltage drop associated to its switches, the minimum voltage amplitude at the transducer's voltage source must be high enough to guarantee sufficient levels for V_{rect}. Additionally, it must be noted that the system's load drives a considerably high *DC* current of 10 mA, and in order to guarantee the load requirements, the power demands must be met, and not only the voltage related requirements. Subsection 5.1.3 presents the minimum transducer voltage amplitude that guarantees that the load power requirements are achieved.

5.1.3 – Simulations regarding the Complete Proposed System

For the simulations regarding the complete energy harvesting system, the schematic presented in Figure 5.7 was used, in which the transducer, designed rectifier, designed LDO regulator and load were used.

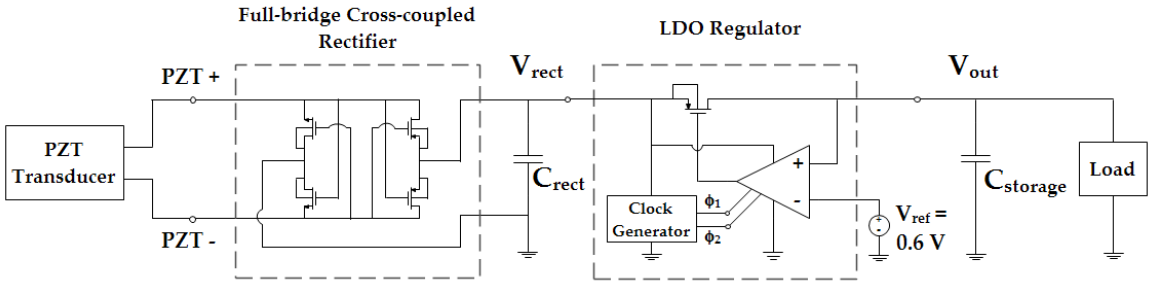

Figure 5.7: Schematic used for the simulations of the Complete Proposed Energy Harvesting System

Simulations regarding the Comparator's operation

Subsection 4.3.2 presented the comparator's operation. Table 4.7 of that subsection gave a correspondence between the comparator's output voltage and the relation between its two input voltages. That correspondence can be observed in the next simulation, presented in Figure 5.8. In this figure it can be seen that the comparator sets its output, P_{gate}, to 0 V when $V_{out} < V_{ref}$ (turns the switch on) and to V_{rect} when $V_{out} > V_{ref}$ (turns the switch off). The simulation also includes the V_{rect} signal and phases one and two. The two phases were added in this simulation so that the asymmetric characteristic of the V_{out} signal could be explained. Given the latch circuit design, presented in the previous chapter, P_{gate} is set at the V_{rect} voltage value whenever phase one is at a low level of 0 V, regardless of the relation between the two comparator inputs. This behaviour explains the V_{out} asymmetry in relation to the V_{ref} voltage value, and it can be observed in Figure 5.8.

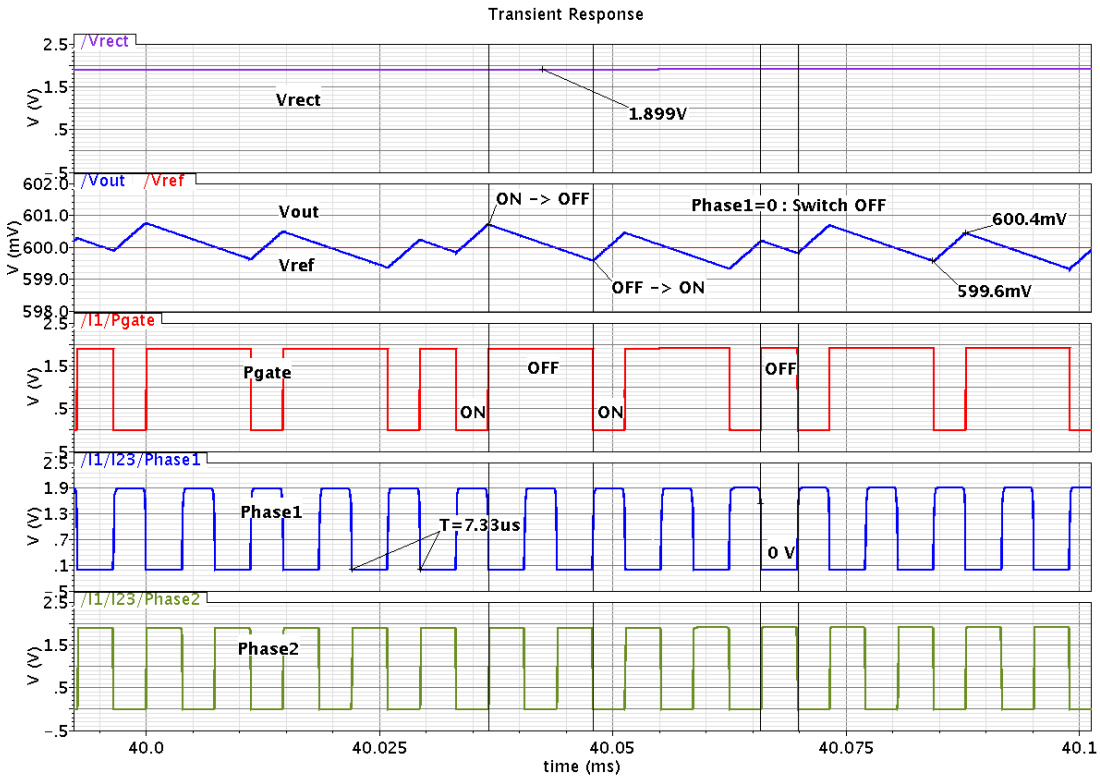

Figure 5.8: Simulation showing the Comparator's output signal, P_{gate}, and input signals, V_{out} and V_{ref}

Simulations regarding the Clock Generator

The clock generator circuit that was presented in the previous chapter generates two non-overlapping clocks that alternate between the low level of 0 V to the high level that corresponds to the V_{DD} supply voltage of the clock generator circuit, V_{rect}. Figure 5.9 presents the clock signals Φ1 and Φ2, and the signal at the inverter ring oscillator's output, Φ0 (introduced in Figure 4.10). The period of these signals is 7.33 μs, which corresponds to a frequency of approximately 136 kHz. This is the actual frequency of the clock signals, and it is close to the theoretically dimensioned 100 kHz desired frequency for the clocks.

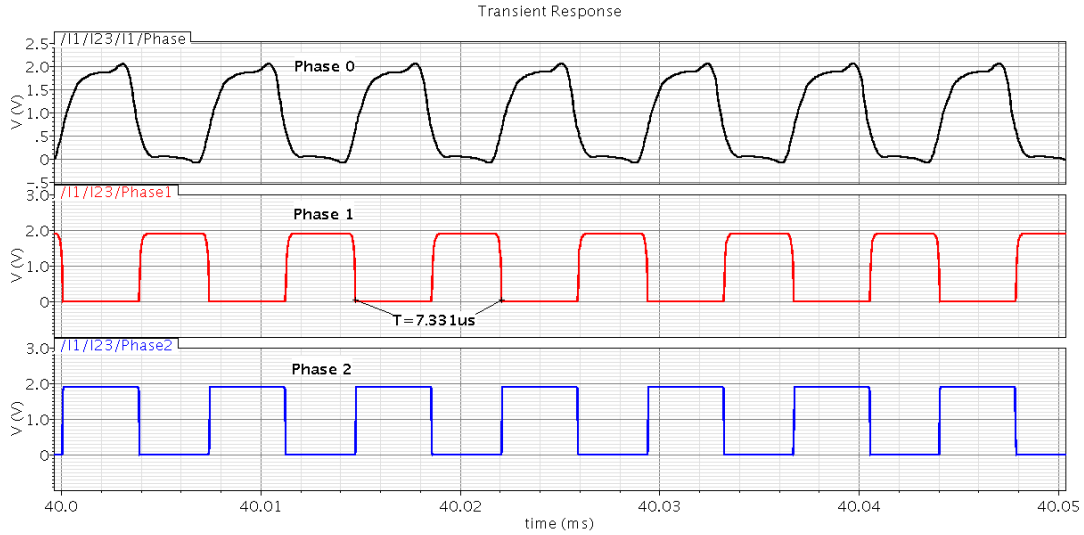

Figure 5.9: Simulation showing the clock signals Φ1 and Φ2, generated by the Clock Generator Circuit

Simulations for the default system input and load requirements

The simulation results regarding the V_{rect} and V_{out} signals for the default system input situation are presented in Figure 5.10, where the current flowing through the load, the requested 10 mA *DC* current, I_{load}, is also included.

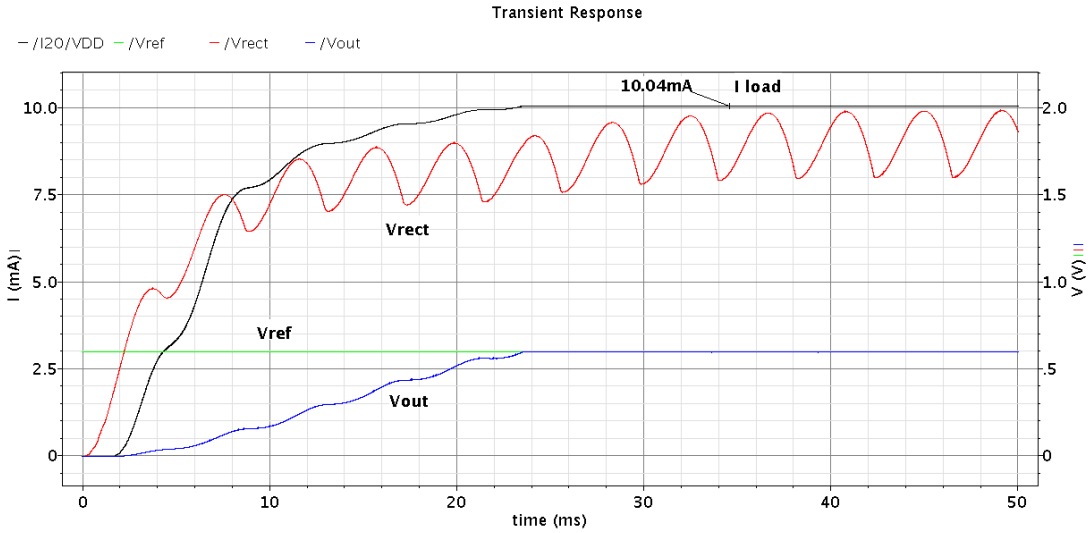

Figure 5.10: Simulation of the Complete Proposed System for the default system input, $V_{pk} = 5\,V$, and the default load requirements, $V_{out} = 0.6\,V$ and $I_{load} = 10\,mA$

Figure 5.11 presents a zoomed in version of the previous simulation, to allow the visualisation of the system's output voltage ripple.

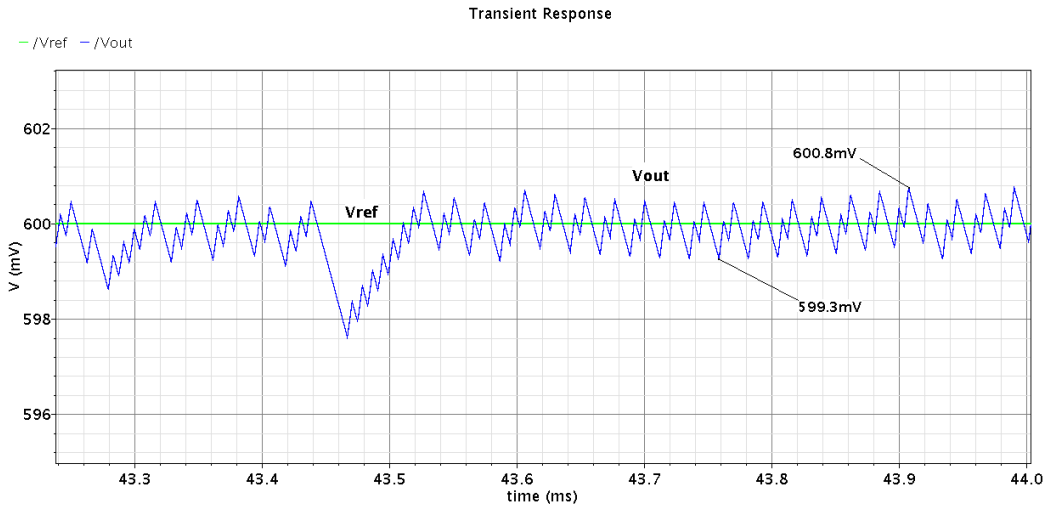

Figure 5.11: Simulation of the Complete Proposed System for the default system input, zoomed in V_{out} signal

This simulation leads to the conclusion that the system is able to successfully regulate its output to a 0.6 V voltage value with a relatively low voltage ripple, in the order of magnitude of a few millivolts, which represents a voltage ripple that is inferior to 1 % of the desired voltage output value. This is true when considering the default system input situation and the desired load requirements, namely the 0.6 V regulated supply voltage and the 10 mA *DC* current that is constantly driven by the load.

Simulations for different outputs of the piezoelectric transducer and different load requirements

To test the system's versatility and minimum input requirements, the following simulations were run using different load requirements and transducer output levels. The colours used for each signal are the same as the ones used for the simulation presented in Figure 5.10.

The following simulation, presented in Figure 5.12, presents the situation with the minimum transducer output levels that allow the system to be able to meet the previously presented RF receiver load requirements.

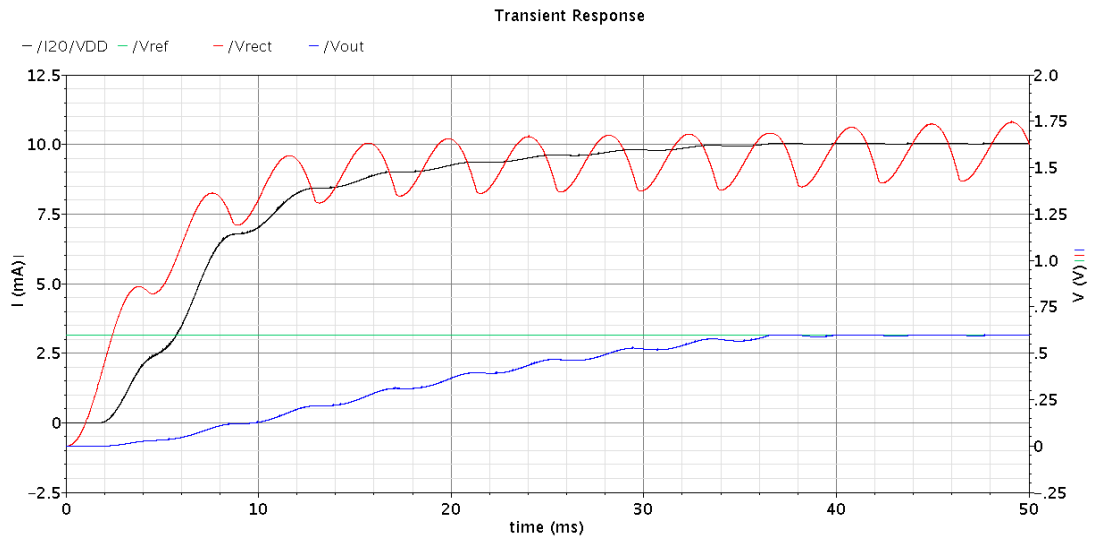

Figure 5.12: Simulation of the Complete Proposed System for the minimum transducer output levels that guarantee the application's power requirements, $V_{pk} = 4.5\ V$

The minimum voltage amplitude at the transducer's *AC* voltage source that guarantees that the system's load requirements are met is approximately 4.5 V, $V_{pk} = 4.5\,V$. This open circuit voltage corresponds to a vibration amplitude, or acceleration, that is slightly inferior to 1 g, according to Table 4.3. This vibration requirement is included in a predicted range of corresponding output values for the considered transducer, which leads to the conclusion that this transducer represents a plausible energy harvesting solution to power the RF receiver, in conjunction with the proposed energy harvesting system.

In order to test the system's versatility, the two following simulations were run. For the first one, whose results are presented in Figure 5.13, the voltage reference was set to 1.2 V and the load's *DC* current requirements were maintained. In order to meet the load requirements, the transducer's voltage amplitude had to be increased to 6 V, $V_{pk} = 6\,V$. Having Table 4.3 in mind, in which the correspondence between vibration amplitude and open circuit voltage levels is made, the following simulation leads to an interesting conclusion: if the RF receiver were to operate with a 1.2 V supply voltage, driving the same *DC* current of 10 mA, a single Midé Volture™ V25W harvester would probably be insufficient to power that circuit, in conjunction with the energy harvesting system, for reasonable levels of vibration amplitudes like the levels predicted in the transducer's datasheet, [19].

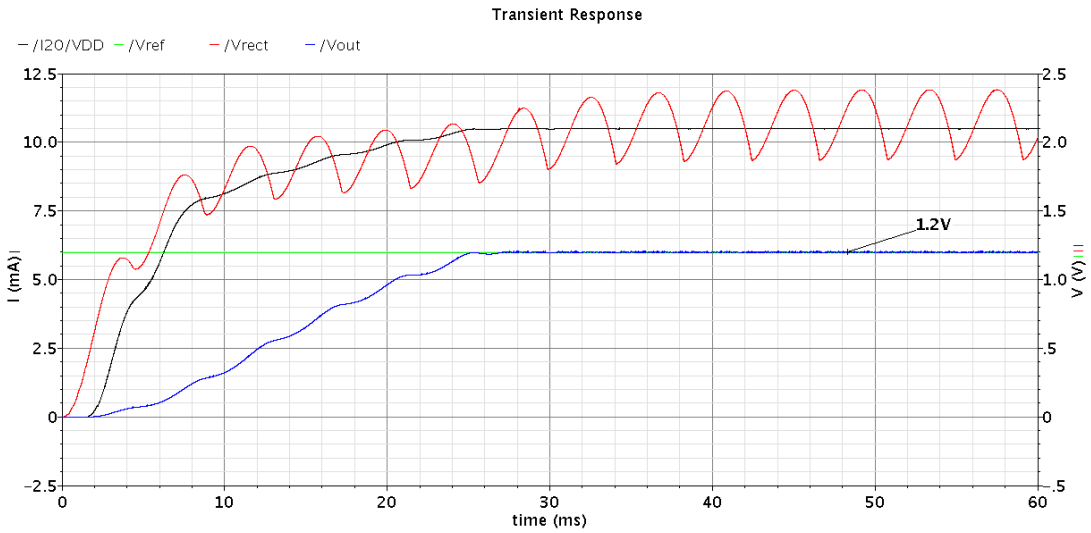

Figure 5.13: Simulation of the Complete Proposed System for $V_{out} = 1.2\,V$ and $I_{load} = 10\,mA$, with $V_{pk} = 6\,V$

For the second simulation, the 0.6 V output voltage level was once again considered, although for this time the *DC* current was set to 5 mA, approximately. Figure 5.14 presents the results for this second case, with the transducer's voltage amplitude set to the approximate minimum value that allows the energy harvesting system to satisfy the described load requirements, $V_{pk} = 3.5\,V$.

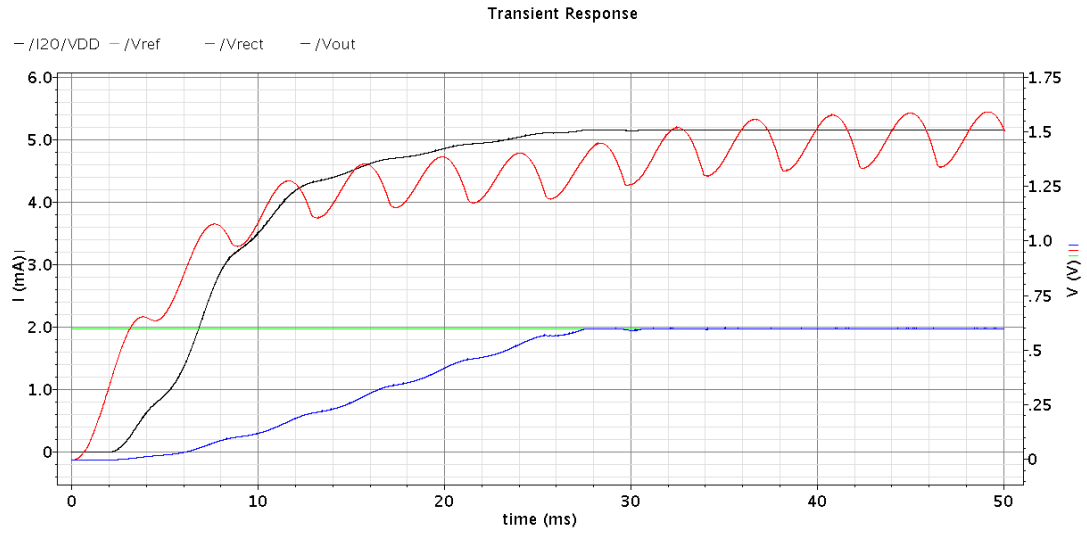

Figure 5.14: Simulations of the complete proposed system for $V_{out} = 0.6\,V$ and $I_{load} = 5\,mA$, with $V_{pk} = 3.5\,V$

Table 5.1 summarises the presented minimum voltage amplitudes of the transducer's voltage source that satisfies each set of different load requirements.

Table 5.1: Summary of the minimum transducer output values for different sets of load requirements

Load Requirements		**Transducer's minimum voltage amplitude (V_{pk})**
V_{DD}	**I_{load}**	
0.6 V	10 mA	4.5 V
1.2 V	10 mA	6 V
0.6 V	5 mA	3.5 V

5.1.4 – Simulations regarding the Complete Proposed System and the RF receiver's LNA

An approach to the simulation of the WSAN SoC is presented in this subsection. The load that is used for the previous simulations is substituted by the RF receiver's LNA circuit, presented in subsection 2.3.2, since this is the receiver's most critical block regarding the supply voltage. Figure 5.15 presents the circuit used for this simulation, with special focus on the LNA's schematic.

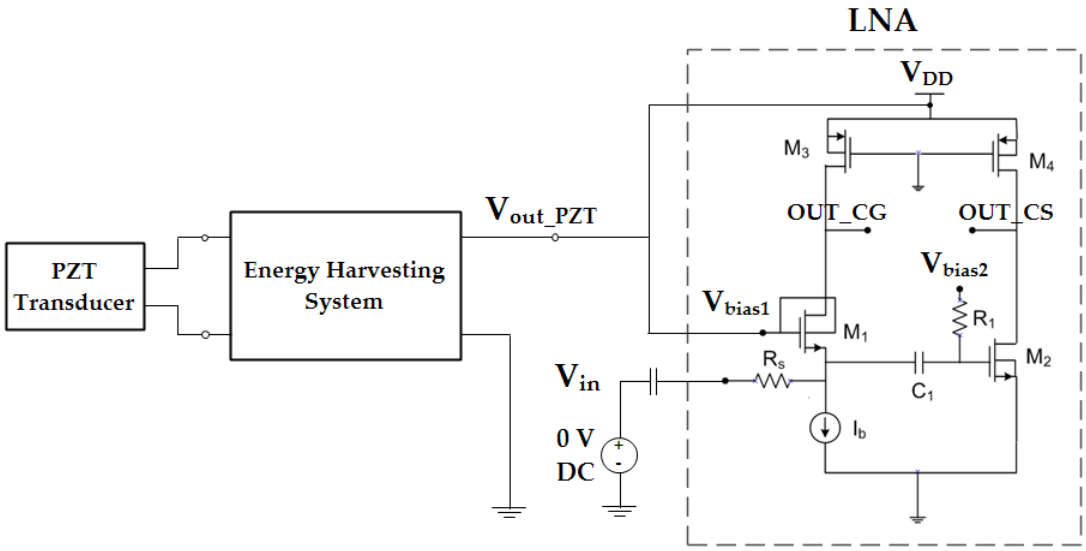

Figure 5.15: Circuit configuration for the simulation of the energy harvesting system and the RF receiver's LNA

The energy harvesting system's output was connected to the LNA's voltage supply rail, V_{DD}, and to the V_{bias1} terminal. The LNA's input was connected to a 0 V *DC* voltage source, so that the influence of the variations of the LNA's supply voltage could be seen at the LNA's outputs. The result of the simulation that was run for the conditions stated above is presented in Figure 5.16 and 5.17.

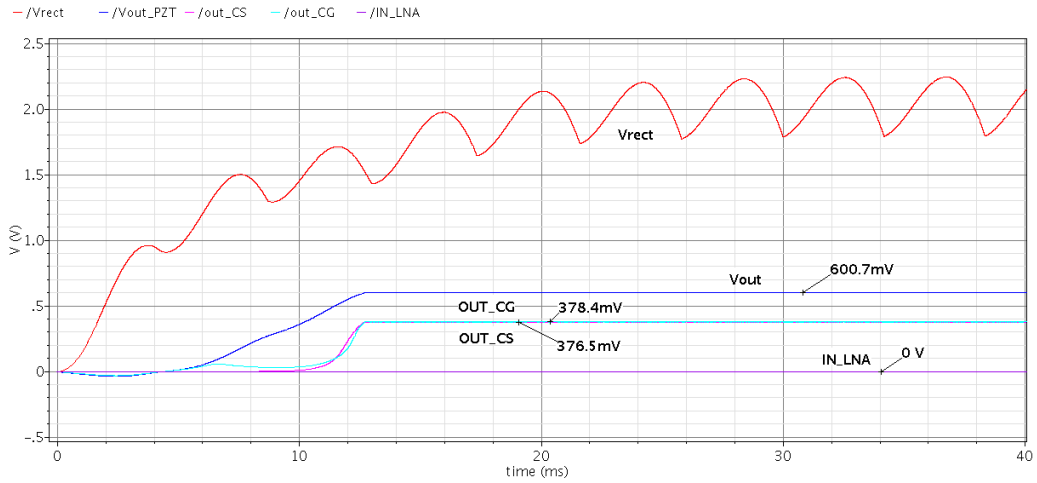

Figure 5.16: Simulation of the complete proposed system and the RF receiver's LNA, with a 0 V DC input

Signals OUT_CG and OUT_CS presented in the simulation relate to the common-gate and common-source LNA output signals (see Figure 5.15). This simulation suggests a normal operation of the energy harvesting system, and it leads to the conclusion that the LNA stabilizes its outputs at apparently matched voltage levels after the output of the energy harvesting system, V_{out}, reaches the 0.6 V desired value. In order to see the influence of the proposed system's output variations in the output of the LNA, a zoomed in view of this simulation is presented in Figure 5.17.

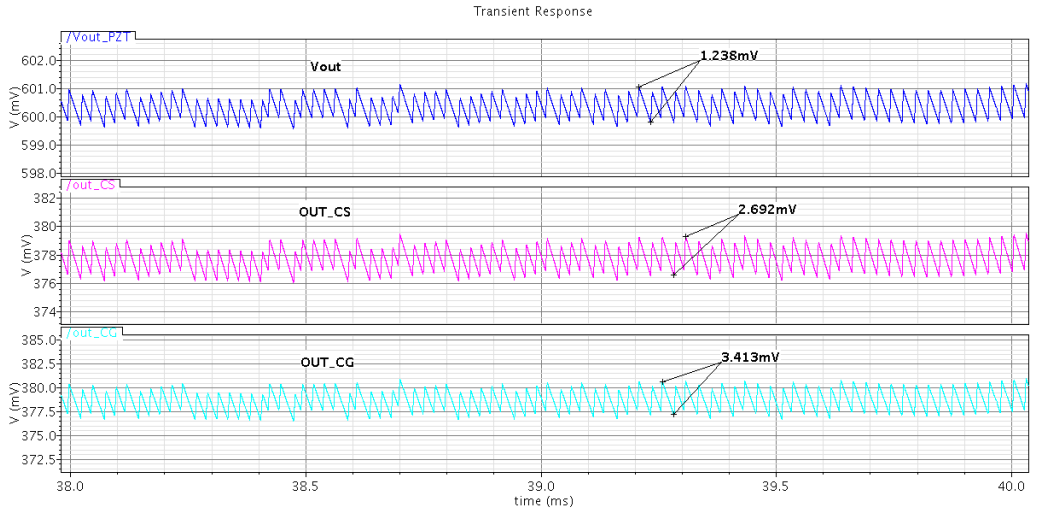

Figure 5.17: Zoomed in view of the simulation of the complete proposed system and the RF receiver's LNA

This view of the simulation presents the OUT_CG and OUT_CS signals, as well as the V_{out} signal, corresponding to the energy harvesting system's output.

The simulation shows peak-to-peak voltage ripples in the three signals, which are a measure of the unintended variation caused by the energy harvesting system's output voltage ripple. This undesirable variation at the LNA's outputs reaches a few mV peak-to-peak, proving that the LNA has a low Power Supply Rejection Ratio (PSRR).

In order to avoid these variations, there are two approaches that can be made in two different fronts: the reduction of the output voltage ripple in the power supply's side and the increase of the PSRR in the receiver's side, particularly in the LNA.

In order to reduce the energy harvesting system's output voltage ripple, the frequency at which the LDO regulator's comparator operates can be increased. Increasing the $C_{storage}$ capacitance value is also a possible solution.

To increase the LNA's PSRR, the PMOS active loads at both the LNA's stages (M3 and M4 in Figure 5.15, originally intended to operate between triode and saturation) should be adjusted to operate in saturation, as much as possible, so that small variations in the drain-to-source voltage do not influence each stage's current in a significant amount. This is an interesting solution having in mind that the receiver's mixer, which is the block at the LNA's output, is intended to operate in current mode, [17]. With this kind of operation, the reduction in the voltage output swing at the LNA's output, caused by the increase of the drain-to-source voltage at the PMOS devices, does not degrade the LNA's output, since it is intended to be in current.

The tuning of each of the constituents of the WSAN SoC to the other parts of the system is a very important step towards the joint implementation of the whole system. In this case, the approach suggested above serves that exact purpose.

5.2 – Layout

The design of the proposed energy harvesting system included the circuit layout. Figure 5.18 presents the complete circuit layout of the energy harvesting system, with the distinction between power circuit, which includes the rectifier and PMOS switch, and control circuit, composed of two main circuits, the comparator and the clock generator. The physical verification process included the design rule checking (DRC) and the layout versus schematic (LVS) for each module of the system and for the complete system block. A general rule used for the whole circuit layout was the adjacent positioning of devices that are connected, whenever possible.

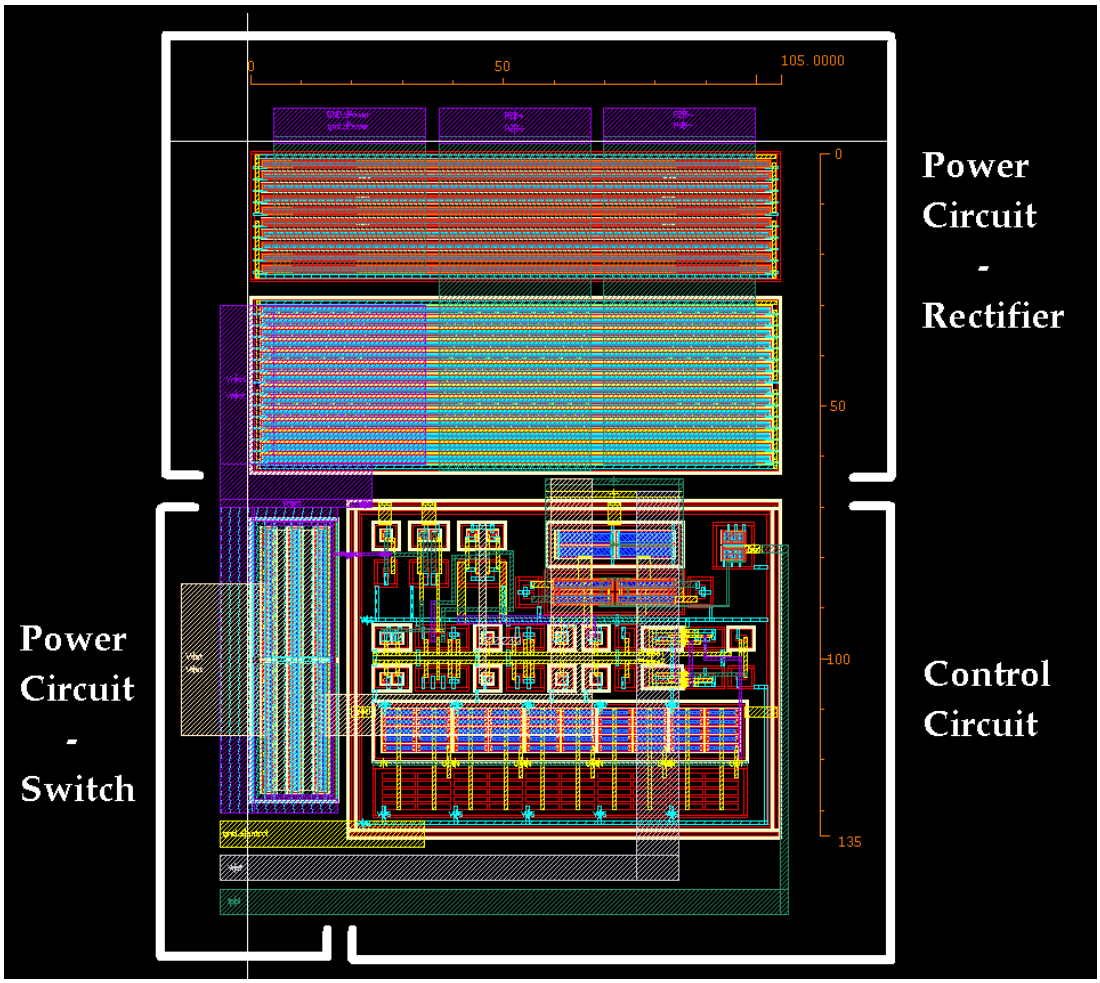

Figure 5.18: Complete Circuit Layout

5.2.1 – Layout considerations for the Power Circuit

The main concern for the layout of the power circuit was the relatively high current flowing through the circuit, in the order of magnitude of a few dozen milliamps. In order to guarantee the power circuit's proper operation, the maximum current density values defined for the technology were taken into account for the dimensioning of the widths of the metal connections and the number of contacts and vias. For both the rectifier and switch, the limited available area forced the connections to be made with multilayered metals connected in parallel, often three or more metal layers for each connection, so that the required width could be distributed by the several stacking levels.

Once again due to the high currents involved, the power circuit ground terminal was not directly connected to the control circuit's ground. This terminal is intended to be available as a pin that is externally connected to the corresponding control circuit ground pin. By connecting the power and control ground terminals externally, the control circuit is protected from the power circuit's high current levels. The power circuit's layout included the use of guard rings for all the transistors.

5.2.2 – Layout considerations for the Control Circuit

The control circuit layout included some important considerations that demanded the inclusion of some additional transistors connected as dummies and in diode configuration. The dummy transistors were connected to the metal paths that form the clock nodes (phase one and phase two), so that the two metal paths could have a symmetrical load in relation to one another. This inclusion of the dummy transistors was necessary to even out the two phases because each one of them drives a different number of switches. This compensation is important to assure the clock generator successfully delivers two non-overlapping clocks. The diode connected transistors that were added to the comparator serve the purpose of cancelling the possible antenna effect that can

be a problem for some transistors. The antenna effect relates to the problem that may occur at the gates of some transistors, when the metal connections at those transistors' gates accumulate charge that may interfere with the proper operation of the device. The diode connected transistors are therefore added to some transistors' gates to discharge that eventual and undesirable charge accumulation.

Given the considerable length value of the transistors that constitute the inverters in the clock generator's inverter ring, each of those NMOS and PMOS transistors was split into ten transistors connected in series, with one tenth of the total length. This allowed a more flexible placing of the transistors in the circuit layout. Another particular case is the comparator's preamplifier transistors. These two NMOS and two PMOS transistors were placed in a common centroid configuration, so that they could be better matched. The control circuit was isolated from the power circuit with a double guard ring, consisting of an interior PTAP ring encased in an exterior NTAP ring, to which the ground potential and the V_{DD} supply voltage were applied, respectively. Figure 5.19 presents the layout of the control circuit.

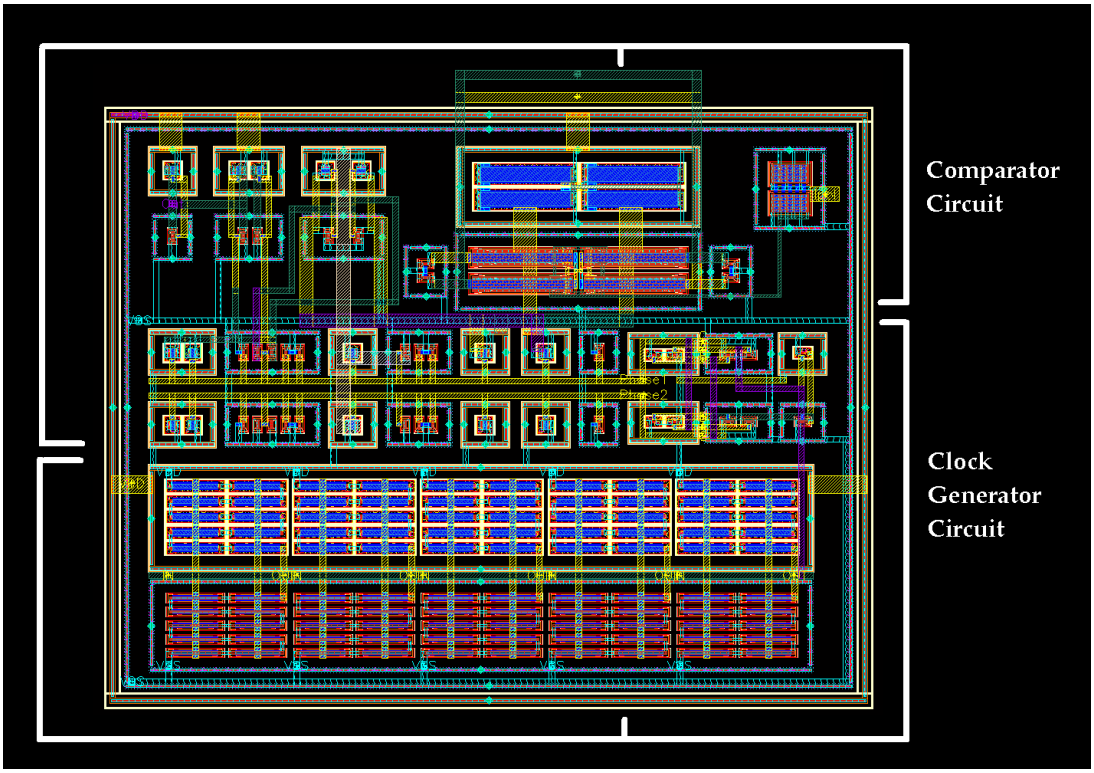

Figure 5.19: Control Circuit Layout

6

Conclusions

6.1 – Conclusions

A theoretical approach was made for piezoelectric energy harvesting as a plausible power source for a wireless sensor node whose surroundings contained moderate levels of vibration. In order to successfully design the piezoelectric energy harvesting system, the power requirements of the system's load and the predictable outputs of the chosen piezoelectric transducer were presented. The system's load was identified as a particular RF receiver, briefly introduced in this thesis.

With the power output requirements and typical predicted input values properly presented, the system design was proposed. Connected to the piezoelectric transducer, a full-bridge cross-coupled rectifier is used to rectify the *AC* output of the transducer. A smoothing capacitor is placed at the rectifier's output to help stabilise it. A DC-DC converter is responsible for stepping down the relatively high voltage level at the rectifier's output to the desired system output voltage, requested by the load. A low-dropout regulator is used for this purpose, with a performance that guarantees a low voltage ripple at the system's output, an essential requirement having in mind the RF circuit's low

PSRR. A storage capacitor is added to the system's output, serving as the system's energy storage device.

Electrical simulations were run for the designed circuit in order to test its performance for the typical transducer outputs and under the load's power requirements. The chosen transducer's equivalent circuit was used for simulations, with its output levels defined according to the appropriate information contained in its datasheet. The simulations lead to the conclusion that the designed energy harvesting system is able to power the RF receiver for moderate levels of vibration of the piezoelectric transducer, presenting low levels of output voltage ripple. It is able to do so requiring only one piezoelectric transducer of the chosen type, for the defined load power requirements. This positive result is strengthened by the system's versatility, tested with simulations for which the system power inputs and output requirements were adjusted to different values.

The designed system presents an inductorless architecture that can be fully integrated, with the exception of the dimensioned external capacitors. The only essential blocks that were excluded from the design were the bandgap voltage reference generator to define the desired output voltage and the start-up circuit, responsible for generating the polarisation current for the comparator's preamplifier stage. Aside from these two external inputs, the system is fully autonomous, presenting an interesting approach for an energy harvesting system prototype. The circuit layout included a wide range of considerations, since the power circuit and control circuit have different concerns that must be addressed, namely the high currents flowing through the power circuit and the potential mismatch of the clock signals generated in the control circuit.

6.2 – Future work

A very interesting analysis could be done with some extended electrical simulations regarding the joint operation of the energy harvesting system and the RF receiver circuit. These extended simulations would support the viability of the WSAN SoC. The implementation of the suggested approaches to the decrease in the output ripple of the energy harvesting system and the increase in the PSRR of the RF receiver is the next obvious step in the development of the WSAN SoC concept.

The fabrication of the designed circuit is also proposed, in order to experimentally validate the simulations' positive results, using the actual piezoelectric transducer while subjecting it to different vibration levels. Regarding the fabrication, a careful heat dissipation analysis should be done for the LDO regulator's switch, since it is expected to dissipate considerable amounts of heat for substantial voltage level differences between the regulator's input and the system's output.

In order to have a fully autonomous piezoelectric energy harvesting system, the implementation of the missing blocks should be considered. These are the bandgap voltage reference circuit and the LDO regulator's start-up circuit. A possible improvement of the system could be the replacement of the designed rectifier by an active rectifier that could compensate the negative influence of the transducer's internal capacitance. This kind of active rectifier would, however, require a start-up circuit (dedicated to the rectifier), which could substantially increase the system's complexity. A careful trade-off analysis should be done in order to weigh the possible increase in complexity and potential improvements in the overall performance of the system.

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