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Development of Electrochromic Thin-Film Transistors on Flexible Substrate

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ABSTRACT

This work documents the fabrication and characterization of electrochromic thin-film transistors (ECTFTs) based on tungsten oxide (WO_3). The ECTFTs exhibit double functionality (optical and electrical modulation) and were deposited on Corning glass and polyethylene naphthalate (PEN) by radio-frequency (RF) magnetron sputtering in an argon-oxygen atmosphere with no intentional substrate heating. The resulting amorphous WO_3 film connects source and drain in a planar configuration with three different architectures (conventional, interdigital and back-electrode) and is gated by a drop-casted lithium-based polymer electrolyte ($LiClO_4$:PC). EC films were characterized using X-ray diffraction (XRD), atomic force microscopy (AFM) and opto-electrochemical measurements, the electrolyte by electrochemical impedance spectroscopy (EIS) and the ECTFTs by static and dynamic electrical characterization. Thinner EC films (75 nm) evidenced lower optical density (ΔOD) and color efficiency (CE) of 0,26 and 21,85 cm^2C^{-1}, respectively, but faster EC reaction kinetics, with bleaching and coloration times (t_b and t_c) of 1,8 and 3,8 seconds, respectively. In terms of electrical properties the best performing ECTFT architecture (interdigital) showed an I_{ON}/I_{OFF} of $2,81x10^5$ and a transconductance of 2,24 mS. The back-electrode architecture however showed better ionic movement control in the channel (adjustable V_{ON}) with enhanced colorations, making it a better candidate for a two-in-one (pixel + transistor) solution for display applications.

Keywords: tungsten oxide (VI); electrochromism; electrochromic thin-film transistors; physical vapour deposition; thin-films; polymer electrolytes.

RESUMO

Este trabalho documenta a fabricação e caracterização de transístores electrocrómicos de filme-fino (ECTFTs) baseados em óxido de tungsténio (WO_3). Os ECTFTs exibem dupla funcionalidade (modulação óptica e eléctrica) e foram depositados em substrato de vidro Corning e polietileno naftalato (PEN) utilizando pulverização catódica de rádio-frequências (RF) assistida por magnetrão numa atmosfera de árgon e oxigénio, sem aquecimento intencional do substrato. O resultante filme amorfo de WO_3 liga a fonte e o dreno numa configuração planar com três arquitecturas diferentes (convencional, interdigital e *back-electrode*) e é conduzido por um electrólito polimérico à base de lítio ($LiClO_4$:PC). Os filmes EC foram caracterizados por difracção de raios-X (DRX), microscopia de força atómica (AFM), medidas electroquímicas e electro-ópticas, o electrólito através de espectroscopia de impedância electroquímica (EIS) e os ECTFTs por caracterização eléctrica estática e dinâmica. Os filmes EC mais finos (75 nm) apresentam menor densidade óptica (ΔOD) e eficiência de coloração (CE) de 0,26 e 21,85 cm^2C^{-1}, respectivamente, mas cinéticas de reacção EC mais rápidas, com tempos de descoloração e coloração (t_b e t_c) de 1,8 e 3,8 segundos, respectivamente. Em termos de propriedades eléctricas a arquitectura de ECTFT com melhor desempenho (interdigital) mostrou uma I_{ON}/I_{OFF} de $2{,}81 \times 10^5$ e uma transcondutância de 2,24 mS. No entanto a arquitectura de *back-electrode* mostrou um melhor controlo da movimentação iónica no canal (V_{ON} ajustável) com melhor coloração, resultando num melhor candidato para uma solução dois em um (pixel + transístor) para a sua aplicação em displays.

Palavras-chave: deposição física de vapores; electrocromismo; electrólitos poliméricos; filmes finos; óxido de tungsténio (VI); transístores electrocrómicos de filme-fino.

LIST OF ABBREVIATIONS

AFM – Atomic force microscopy

AC – Alternating current

AM – Active matrix

a.u. – Arbitrary units

BE – Back-electrode

CAD – Computer aided design

CC – Characteristic curves

CEMOP – Center of Excellence in Microelectronics Optoelectronics and Processes

CENIMAT│I3N – *Centro de Investigação de Materiais*│*Instituto de Nanoestruturas, Nanomodelação e Nanofabricação*

CV – Cyclic voltammetry

CVD –Chemical vapor deposition

CPE – Constant phase element

DC – Direct current

DCM – *Departamento de Ciências e Materiais*

EC – Electrochromic

ECD – Electrochromic device

ECM - Equivalent circuit model

ECT – Electrochemical transistor

ECTFT – Electrochromic thin-film transistor

EDL – Electric double layer

EDLT – Electric double layer transistor

EGT – Electrolyte-gated transistor

EIS – Electrochemical impedance spectroscopy

FET – Field-effect transistor

FPD – Flat panel display

FPP – Four-point-probe

IC – Integrated circuit

ITO –Indium tin oxide

IZO – Indium zinc oxide

MIF – Metal ion free

MOSFET – Metal-oxide-semiconductor field-effect transistor

PC – Polycarbonate

PEN – Polyethylene naphtalate

PM – Passive matrix

PMMA – Poly(methyl methacrylate)

PVD - Physical vapor deposition

RF – Radio-frequency

RT – Room temperature

RC – Resistor Capacitor equivalent circuit

rms – Root mean square

rpm – Revolutions per minute

SCM – Super Conductor Materials

TCO –Transparent conductive oxide

TFT –Thin-film transistor

TMO – Transition metal oxide

UV – Ultra-violet

XRD – X-ray diffraction

LIST OF SYMBOLS

2θ – Incidence angle for XRD measurements

A – Ampere

Ag – Silver

AgCl – Silver chloride

Al – Aluminium

Ar – Argon

Bi_2Te_3 – Bismuth telluride

CE –Coloration efficiency

Cl^- - Chlor ion

Cu – Copper

C_b – Electrolyte bulk capacitance

C_{DL} – Capacitance of electric double layer

C_{eff} – Effective capacitance of electrochemical cell

C_i – Dielectric capacitance per unit area

e^- – Electron

F – Farad

f – Frequency

f_{co} – Cut-off frequency

g_m – Transconductance

Hz - Hertz

H^+ - Hydrogen ion

H_2 – Hydrogen

h – Hour

Im(Z) – Imaginary part of impedance

I_D – Current between soruce and drain

I_G – Leakage current between gate and source

I_{GB} – Current between gate and back-electrode

I_{OFF} – Drain current in the OFF state

I_{ON} – Drain current in the ON state

K^+ - Potassium ion

L – Channel length

Li^+ - Lithium ion

Li – Lithium

Li_2O – Lithium oxide

$LiClO_4$:PC – Lithium perchlorate in a polycarbonate matrix

M – Molar concentration

M_xWO_3 – Tungsten bronze (where M = H, Li, Na, ... with $x \leq 1$)

m - Metre

min – Minute

Na^+ - Sodium ion

NiO – Nickel oxide

O_2 – Oxygen

P_{O2} – Partial oxygen pressure

pH – Acidity or basicity of an aqueous solution

Q_{ext} – Extracted charge

Q_{in} – Inserted charge

Re(Z) – Real part of impedance

R_b – Electrolyte bulk resistance

R_{ext} – Exterior contact resistance

R_s – Sheet resistance

r - Radius

S – Siemens

S_s – Subthreshold swing

s - Second

Ti – Titanium

t_c – Coloration time

T_c – Transmittance in the colored state

t_b – Bleaching time

T_b – Transmittance in the bleached state

t_{dep} – Tempo de deposição

V - Volt

V_B – Voltage between back-electrode and source

V_D – Voltage between drain and source

V_G – Voltage between gate and source

V_{GB} – Voltage between gate and back-electrode

V_{GD} – Voltage between gate and drain

V_{ON} – Transistor ON voltage

V_T – Threshold voltage

W – Channel width

WO_3 – Tungsten oxide (VI)

WO_6 – Corner-sharing tungsten oxide octhaedra

x – Insertion coefficient

Y_0 – Capacitance of a constant phase element

Z – Impedance

ZnO – Zinc oxide

Å - Angstrom

α – Fractal surface character

ΔOD – Optical density

ΔT – Transmittance difference

σ – Electrical conductivity

σ_i – Ionic conductivity

θ – Phase shift

κ - Curvature

λ – Wavelength of electromagnetic waves

μ_{FE} –Electron mobility due to field-effect

μ_{lin} – Electron mobility in the linear regime

ρ – Electrical bulk resistivity

π – Ratio of a circle's circumference to its diameter

Ω - Ohm

ω – Angular frequency

^oC – Degrees Celsius

$|Z|$ - Magnitude of impedance

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MOTIVATION AND OBJECTIVES

Motivation

Nowadays, in an evolving society the urge to push boundaries and the drive to break into ever greater fields of science is more important than ever. Especially the field of display applications together with flexible and transparent technologies has received great attention in the last couple of years.[1] The aim for always lower power consumption, transparency and flexibility in display electronics are only a few of the driving forces behind recent developments in this evolving area,[2] which also presents one of the main motivations for the present work. Another field of interest regards the exploration of new semiconducting materials for their integration into transistor devices since their first investigation in 1948 by Bardeen et al.[3] In particular the widely-known and implemented thin-film transistor (TFT) [4-6] has drawn a considerable amount of attention,[7] especially over the last decade,[8-11] due to its increasing simplicity in fabrication,[12] substrate possibilities [13] and diversification.[14] The combination of these two technologies (Displays and TFTs) has culminated in groundbreaking fields like Flat-Panel Displays (FPDs) and Transparent Displays.[15] A Market analysis by Displaybank from 2011 predicts a gross market revenue of $87,2 billion by the year 2025 (see Annex A) for transparent display applications; a new emerging technology with substantial future potential.[16]

Logically the combination of those two areas (FPDs and TFTs) presented a conisderable opportunity for a new and exciting field of research and applicability. The present work fits right into these two areas, having its main interest based on the field of electrochromism. This field originates from the discovery of the electrochromic (EC) properties of tungsten oxide (VI) (WO_3) [17, 18] and its subsequent integration into EC devices (ECD) with specific application fields, such as high contrast displays, energy-saving smart windows, antiglare mirrors, active camouflage, or reduced visibility windshields,[19, 20] solely based on the color changing properties of the material.

The main scientific interest lays in the optimization of these ECDs and their EC properties, including response time, optical density (ΔOD), color efficiency (CE), durability and cyclability. Investigations are predominantly based on the works of two of the most influential authors in this field of research; Granqvist [21] and Monk.[22] Their literature shows an enormous insight into the underlying theoretical properties of different EC materials as well as their fabrication techniques for ECDs.

One main property of EC materials is the reversible and persistent change of their optical properties, triggered by an electrochemical redox reaction through the application of an electric potential. An ECD is therefore based on the encapsulation of an EC material (inorganic or organic) into an EC cell, also known as an EC battery. An EC cell presents a multilayered architecture, where the EC material (electrode) is separated from the counter-electrode by an electrolyte, as represented in **Figure 1.3 a)**. The electrolyte, which will receive further attention in section 3.2, can take several forms, including electrolyte solution, ionic liquid, ion gel, polyelectrolyte or polymer electrolyte, [23] depending on its desired properties. The application of a difference in potential [24] between the two electrodes triggers the electrochemical reaction, resulting in a change of the material's optical transmittance. This process and its underlying properties, such as the redox reaction and its kinetics will be investigated in section 3.1.2. In this work, the inorganic EC material WO_3 will be in focus, as it is the most studied and understood inorganic EC material to date. Its properties and fundamentals will be discussed in greater detail in section 1.1.

There have been many case studies and a variety of experimental approaches of how WO_3 can be used in thin-films and their application in ECDs. These approaches have been reviewed throughout the twentieth century by Granqvist *et al.*[25-27] In this literature Granqvist assembles and describes different methodologies used for WO_3 fabrication and thin-film preparation techniques and their influences on its intrinsic and extrinsic properties. Regarding process parameters, another key motivation for this work lies in the fabrication of amorphous WO_3 films (section 2.1) relying on low-temperature processes with no intentional substrate heating so that it can be used for temperature sensible substrates such as polyethylene naphthalate (PEN) or even paper.

Another important aspect of electrochromism is that during the electrochemical reaction, WO_3 not only undergoes a change in its optical but also in its electrical properties.[28] The reversible change of its electrical conductivity leads right to the second field of application for WO_3 and EC materials, which is connected to its integration into transistor devices as the semiconducting layer. This integration results in an electrochemical transistor (ECT), which is situated in the group of electrolyte-gated transistors

(EGTs).[29] The group of EGTs show promises in different areas, such as biosensors,[30-32] microelectronics [33] or low-voltage appliactions,[34] mostly due to the high dielectric capacitance of the electrolyte [35] and low source and drain contact resistances.[36] In the area of ECTs several organic transistors were implemented in the field of display,[37] biosensors [38, 39] and microelectronics applications.[40-42] Only a few approaches using inorganics were shown.[43, 44] They all however are limiting their field of application to those that are based on the change of the materials conductivity. However, the one based on WO_3 [44] does take coloration and bleaching processes into account but is centered on its application as a pH biosensor. The only work until to date to implement an EC material into a TFT was elaborated by Li *et al.* [45] but limiting its fabrication process to an all organic EC material (EDOT).

Consequently another motivation throughout this work is to investigate and explore not only the optical but also the electrical modulation of the WO_3 and to combine this behavior into one device. This device, designated as an electrochromic thin-film transistor (ECTFT), posseses double functionality (optical and electrical modulation), arising from the EC properties, suitable for a two-in-one (transistor + pixel) solution in active matrix (AM) display appliactions. Using ECTFTs in such applications would, not only secure less cross-talk for better contrast, but also lower power consumption as a great alternative to, for example, electrophoretic displays.

Objectives

The whole master thesis situates itself around EC WO_3-based TFTs (ECTFTs), devices that exhibit optical and electrical modulation (double functionality) and their final fabrication on a flexible substrate. Plainly put, the main objective is to design, fabricate and characterize WO_3-based ECTFTs based on three specific selected architectures (conventional, interdigital and back-electrode) in order to determine the best performing device, which then will be fabricated on a flexible and transparent polyethylene naphthalate (PEN) substrate.

Logically this main objective will be divided into three sub-objectives, which will evaluate each constitute of the ECTFT individually.

- Study and characterization of the sputtered WO_3 films' properties
- Study of the lithium-based polymer electrolyte
- Electrical characterization of the contact (electrode) materials

The last step hereafter will be the electrical and dynamic characaterization of the complete devices (ECTFTs) in order to understand the underlying mechanisms during these characterizations and to explore their weaknesses and strengths, regarding electrical, electrochemical and electro-optical performances.

The finalizing step will be the transition to fully transparent ECTFTs on a flexible substrate as the proof of concept described above. The resulting devices will be subjected to yet another electrical static characterization under mechanical stress to evaluate their potential application in transparent flexible electronics.

To fully complete this line of investigation, a glimpse into a possible application of an ECTFT in an 8x8 AM EC display will be given, which has been recently developed in CENIMAT│I3N. The present work therefore shows a complete and successful way from the design of a new transistor technology over its characterization until its implementation into a possible field of application.

1.INTRODUCTION

For theoretical comprehension and consulting purposes of the following chapters, an introduction will be given on relevant topics. The following sections throughout this chapter will be concerned with the explanation of the involved phenomena of the material in study, which is based on electrochromism. Then followed by a tutorial about existing thin-film transistor architectures, their operation principle and the associated underlying properties. In order to fully comprehend the conjugation of EC films and TFTs, the final section of this chapter is dedicated to transistor fundamentals and the ECTFT's classification.

1.1. Electrocromism: Fundamentals and Applications

Optically active materials have received great attention throughout the last decades due to their possible applications in modern technology. These materials, also designated as chromogenic materials,[46] are capable of undergoing controlled reversible changes in their optical response (absorption, transmission and reflection), triggered by an external stimulus that promotes a change of the material's chemical or physical state. Depending on the type of the external stimulus a further classification into subclasses of chromogenic materials is possible; for example electrochromism (electrical current), photochromism (light) or thermochromism (heat) to exemplify just a few. Since the motivation of this thesis is the fabrication and characterization of ECTFTs based on tungsten trioxide (WO_3) the focus will be on electrochromism.

After Deb's first publication [17] and patent,[47] scientific and industrial research into the domain of EC materials has gained a great deal of attention over the last decades.[48, 49] There are several reports devoted to this phenomena, which have been inspired by the publications made by high impact scientists dedicated to this specific area, where the ones from Granqvist [21] and Mortimer *et al.* [22, 50] stand out as the most complete.

According to Granqvist *et al.* [27] electrochromism is the persistent and reversible change of a material's optical properties induced by an electrical potential. The optical absorption can be modified through double insertion of electrons and charge-balancing ions,[51] thus having the principle based on a redox reaction. Being a reversible process gives an EC material the capability of transiting between two distinct oxidation states: the colored and the bleached state.[52]

Numerous organic and inorganic materials show EC properties. However since the early stages of the discovery of EC materials,[17] there has been considerable interest in inorganic EC materials, presenting, in some aspects, like chemical stability (photodegradation) superior properties to organic alternatives.[53] Among the group of inorganic EC materials, greater importance has been given towards EC transition metal oxides (TMOs) films.[54] Essentially, these EC materials can be divided into two subgroups depending on the coloration phenomenon: cathodic (coloration under ion insertion) and anodic (coloration under ion extraction). For example, oxides based on tungsten undergo cathodic coloration whilst oxides based on nickel undergo anodic coloration. Oxides based on vanadium can be viewed as a "hybrid" and are capable of both coloration types.[55]

The standard EC device (ECD) incorporates two EC films with complementary coloration (for example, WO_3 and NiO).[51] Shuttling ions between the two EC films one way, colors both of the layers, while shuttling ions the other way, results in their bleaching. Consequently, by combining cathodic and anodic oxides, it is possible to fabricate a more efficient and visually appealing ECD, than with a single EC film [55].

Figure 1.1 illustrates a standard ECD and the underlying schematic.[56] The device has five superimposed layers in a laminate configuration on a transparent substrate, typically of glass or flexible material (such as plastic or paper). The substrates are coated with a transparent conductive oxide (TCO), like indium tin oxide (ITO) or indium zinc oxide (IZO). One of these layers is coated with an EC film, whereas the other with an ion storage film, with or without EC properties. These two layers are separated by an ion-conducting electrolyte. Lithium-based electrolytes have been proposed for application in devices due to the long-term stability for solid-state smart window application and because the diffusion coefficient of the lithium ion is higher than that of other metallic cations.[57] A voltage pulse, of the order of 1 - 2 V, applied between the TCOs leads to optical modulation, following the process described above.[55]

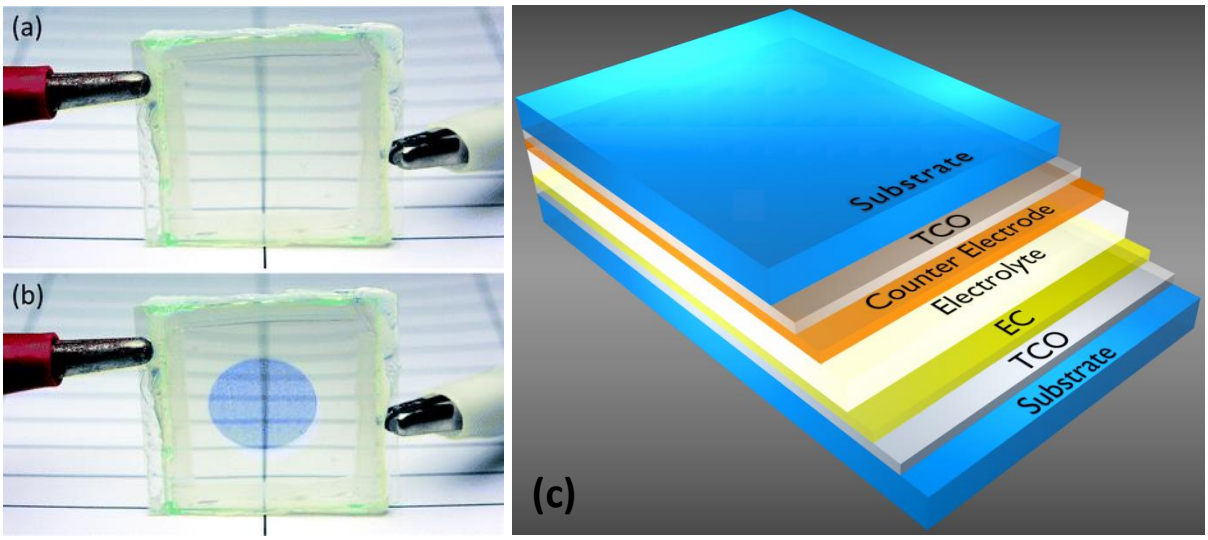

Figure 1.1 - Lab-testing EC device in **(a)** bleached and **(b)** colored state.[58] **c)** Illustration of a typical ECD configuration.

Among the TMOs that exhibit EC properties, WO_3 is by far the most extensively studied due to properties like fast response times, coloration efficiencies or long lifetimes [54, 59] and is also the most widely implemented commercially.[60] However, there are many efforts to improve its coloration performance (lower coloration time, higher color intensity and reversibility) for practical applications.[54]

It is convenient to introduce electrochromism in WO_3 by reference to the simple redox reaction:[27]

$$WO_3\ (transparent) + xM^+ + xe^- \ \leftrightarrows\ M_xWO_3\ (dark\ blue) \tag{1.1}$$

where M^+ is an ion of the alkali metal group (e.g. H^+, Li^+, Na^+ or K^+), e^- represents electrons and parameter x, designated as the insertion coefficient, represents the proportion of electro-reduced tungsten sites.[61] Thus, when WO_3, which is transparent and insulating as a thin-film, incorporates electrons and charge-balancing ions it can be reversibly transformed to a material with radically different properties.[27] This material is known as tungsten bronze (M_xWO_3, M = H, Li, Na or K), which is less insulating and exhibits a dark blue coloration.

The ion intercalation can occur due to the structure of WO_3 which is based on a pervoskite defective one. This structure consists of a three-dimensional network of corner-sharing WO_6 octhaedra, as shown in Annex B, giving rise to a considerable interstitial space, where ion intercalation can occur.[62]

The changes in optical and electrical properties arising from this reaction are evaluated in respect to specific qualitative and quantitative parameters. Some of the main parameters for EC films include response time (time required to transit between the colored and the bleached state), write-erase efficiency (maintaining initial color properties for subsequent electro-bleaching), optical memory (color persistence at open-circuit potential), cycle life (experimental measure of the ECD durability) and coloration efficiency (CE) [63]. Coloration efficiency (CE) is perhaps the most important metric for selecting an EC material and is defined as the change in optical density (ΔOD) per unit of inserted charge (Q):[60]

$$CE(\lambda) = \frac{\Delta OD(\lambda)}{Q} = log\left(\frac{T_b(\lambda)}{T_c(\lambda)}\right)\frac{1}{Q} \tag{1.2}$$

where T_b and T_c represent the transmittance in the bleached and colored state at a specific wavelength λ and Q the charge density. A high CE provides large optical modulation with small charge insertion or extraction. Broadly speaking, a high CE oxide device will be more durable and switch faster. Substoichiometric amorphous WO_3 films have been shown to have the highest oxide CE over the visible region, typically greater than 50 cm^2C^{-1}.[64-66] Evidently the deposition technique and subsequent heat treatments play an important role in the resulting WO_3 film and especially its EC properties.[67] There are several reports devoted to the study of WO_3 thin-films for EC applications obtained by diverse techniques like sputtering, spray pyrolysis, thermal evaporation, chemical vapor deposition (CVD), sol-gel via dipping, spraying, and spinning, etc.[55] For the proposed objective,

which is the fabrication and improvement of ECTFTs, sputtering appears to be a versatile technology to deposit amorphous WO_3 thin-films.[68] In terms of scalability and controllability, sputtering emerged as one of the preferred industrial thin-film technologies for the fabrication of amorphous EC films [55]. It was found that a simple but not unexceptionable surmise would impute faster electronic motion to predominant crystallinity, but ionic rapidity to predominant amorphism (for the same material),[58, 69] which results in two counteracting parts in EC materials.

Regarding the EC films characterization, there are several techniques that can be used in order to study the structural, morphological, electrical, optical, electrochemical and EC properties,[70] being just a few described in this work.

Current applications for ECDs range from flat panel displays over smart windows to antiglare mirrors [20, 24, 60, 71, 72] as illustrated in **Figure 1.2**. However in the area of flat panel displays, passive matrix (PM) EC displays are still an issue, as limiting factors, such as, slow response time,[19] image diffusion or cross-talk [73] still present challenges to be overcome.[74] An active matrix display (AM) with ECTFTs constituting transistors and pixels at the same time could improve the above mentioned limiting factors associated with EC displays, showing a field of possible application for the present work.[75]

Figure 1.2 - Three main applications for EC materials in ECDs: **a)** smart windows,[76] **b)** rear mirrors [77] and **c)** PM displays.[77]

1.2. From Field-Effect to Electrolyte-Gated and Electrochemical Transistors

As described before, in section 1.1, the EC effect not only influences the optical but also the electrical properties of the EC material,[78] enabling these materials to be applied in transistors as the semiconducting layer. The following chapter is therefore designed to give an overview of existing technologies in this field and explain the underlying properties.

A transistor is a three-terminal semiconductor device, which revolutionized modern information technology since its discovery by John Bardeen and Walter Brattain.[3] The basic working principle of a transistor is the modulation of a drain current (I_D) between two electrodes (source and drain) with an applied voltage (V_G) at a third electrode (gate). This current modulation is referred to as field-effect and is the essential property of the field-effect transistors (FETs). [1] In extreme cases the drain current can commute between a small and a relatively large value, resulting in a behavior comparable to an electric ON/OFF switch [79]. Further investigation into the field of transistors culminated in the widely known metal-oxide-semiconductor field-effect transistor (MOSFET) by Atalla and Kahng,[80] which, nowadays, is the most critical device component in modern integrated circuits (ICs). However, with Weimer's publication of "The TFT – A new thin-film transistor" [81] attention shifted to this new family of transistors. MOSFETs are typically fabricated on a silicon wafer, acting also as the semiconductor, whereas TFTs are usually deposited on an insulating substrate such as glass [82], paper [83] or plastic foil.[84] TFTs show promises in terms of fabrication (low-cost materials, temperature, processability, etc.) [82] and their application in displays,[85] which is one of the reasons why this is the transistor type of interest in this work.

[1] Throughout this thesis V_B, V_D, V_G, I_D and I_G will be used, if not stated otherwise, interchangeably with V_{BS}, V_{DS}, V_{GS}, I_{DS} and I_{GS} as the source represents the reference electrode and is usually grounded.

The TFTs basic components are an insulating substrate, conducting electrodes (source, drain and gate), a semiconducting material between source and drain, and a dielectric material sandwiched between semiconductor and gate electrode (Annex C). In general four basic architectures have been described and successfully implemented since the discovery of the TFTs as can be seen in Annex D. The used ECTFT structure in this work though comprises a planar structure, where all three electrodes are on the same plane, separated horizontally and in contact solely through a lithium-based polymer electrolyte, as depicted in **Figure 1.3 a)**. This type of structure is promising due to its easy fabrication, as it is a layered structure, and has already been successfully implemented with organic EC materials [37, 41] as well as the closely related interdigital solutions.[42] All of the described structures were shown to be promising in their application as TFTs and will therefore be in focus. Architectures with a conductive layer under the channel (back-electrode) to control ion movement and enhance EC reactions are a novelty in this area and will receive extra attention in this work.

Having its dielectric layer based on an electrolyte situates the ECTFTs in the group of electrolyte gated transistors (EGTs).[35] The key feature of electronic interest in this material is that it is electrically insulating yet ionically conductive. In a transistor, an electrolyte gate dielectric is used to bridge the gap between a metal gate electrode and the channel. A gate voltage applied to the electrode drives ion migration in the electrolyte. This results in ion accumulation at the electrode and channel surface, which effectively transfers the gate charge into the channel [86].

One main motivation for EGTs is their substantial dielectric capacitance, reaching values in the order of 1 - 10 μFcm^{-2}, outperforming even transistors based on high-k dielectrics.[87-89] The outcome is a considerable reduction in the voltages required for transistor operation as well as an increase in drive currents, as the drain current is directly proportional to the dielectric capacitance (equation E.1 Annex E). Furthermore electrolyte-gating allows low source and drain contact resistances,[36] which still present a major issue in conventional transistors, and it opens route to novel devices, with new architectures, due to the solution processability (printed electronics) of many solid electrolytes.[90-92] A downside of EGTs is their considerable DC leakage current compared to polymers or high-k oxides dielectrics, due to arising Faradaic currents.[93] Consequently the decision to employ EGTs will depend on understanding which figure of merit is most crucial for a given application.[94]

As illustrated in **Figure 1.3 b)**, the group of EGTs is divided into electric double layer transistors (EDLTs), if the semiconducting layer is impermeable to ions, causing a field-effect mode due to the electric field of the electric double layer (EDL), and electrochemical transistors (ECTs), if ions can migrate into the semiconductor, causing electrochemical reactions.[95] The latter is the group of interest, as WO_3 is permeable to ions. ECT operation proceeds by the reversible electrochemical doping and de-doping of the semiconductor channel (i.e. reversible reduction and oxidation of WO_3) upon application and inversion of a positive gate bias, respectively. In contrast to EDLTs, where the channel, induced by the EDL, is seldom over 100 Å and usually much less,[96] in ECTs the channel becomes in fact three-dimensional, permitting much higher drain currents,[97] which can be advantageous, especially for high current applications.[98] However, the ON/OFF switching of an ECT involves ion transport in and out of the semiconductor bulk resulting in slower switching speed and considerable hysteretic behavior,[99] whereas EDLTs rely only on ion migration in the electrolyte.[33] It was shown that EDL formation in ECTs also occurs and a gradual transition from field-effect to an electrochemical mode is possible with polymer electrolytes,[100, 101] which will also be one of the principal involved processes during ECTFT electrical charcaterization. To date little is known about this transition,[34] as most EGTs aim for a field-effect mode based on EDL formation, due to its faster switching, compared to electrochemical doping. This leaves a considerable field for research and possible insight into this rather complex topic. However, the ECTFTs in this work will be characterized from the point of view of a FET (transfer curves), as this is a well-established technique to determine the most important quantitative parameters of the devices (see Annex E).

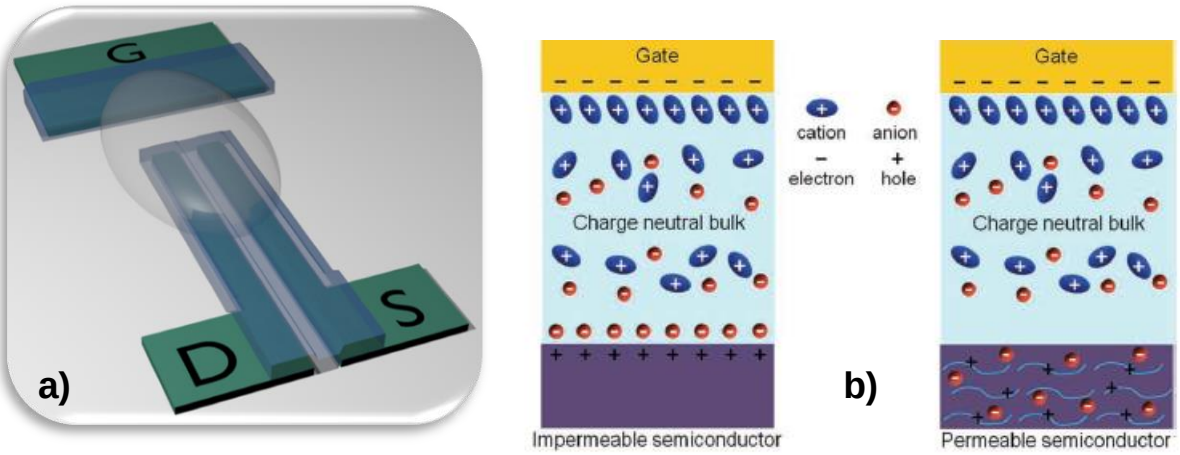

Figure 1.3 - **(a)** Example of one of the basic planar ECTFT structures fabricated and characterized throughout this work. Gate (G), Source (S) and Drain (D) are indicated. The blue transparent layers are the EC films and a transparent droplet between gate and channel represents the electrolyte. **(b)** Working principle of EDLT and ECT with impermeable and permeable semiconductor (example for p-type), respectively. Adapted from [29].

FETs are evaluated based on their characteristic curves (CCs), which are obtained by sweeping either V_D (output) or V_G (transfer) while measuring the response in drain current. Qualitative assessments can be made from the output curves, such as saturation in the post pinch-off regime or contact resistance information from the linear region. Crucial quantitative electrical parameters can be extracted from the transfer characteristics,[102] such as ON/OFF ratio (ratio of maximum to minimum I_D), threshold voltage V_T (voltage for accumulation layer), ON voltage or V_{ON} (voltage for which I_D starts to increase or voltage to fully turn OFF the transistor), subthreshold swing S_s (necessary V_G to increase I_D by one decade), field-effect mobility μ_{FE} (charge carrier mobility) or transconductance g_m (drain current variation to gate voltage variation). Throughout this work the notation of V_{ON} rather than V_T will be used as the determination of V_T has associated sources of error. Essential equations regarding these parameters and the working principle of a FET are remitted to Annex E.

Recently most of the research on ECTs has been focused on the incorporation of organic materials into TFTs,[38, 39, 41, 42, 45] due to a sudden interest in printed electronics. But inorganic ECTs show promises for increased carrier mobilities, faster switching speeds, enhanced chemical stability [103] and their application in biosensors.[44] Nevertheless only a few publications have been made in the field of inorganic ECTs,[43, 104] and the few using EC materials don't consider the EC double functionality, a systematical switching delay study [103] or dynamic behaviors, leaving a wide field for investigation for the proposed ECTFTs.

2. MATERIALS AND METHODS: FABRICATION, OPTIMIZATION AND CHARACTERIZATION PROCESS OF THE ECTFTs

The transistor's architecture plays a crucial role in the device's final performance. Having this in mind, this work was devoted to the fabrication, optimization and characterization of three different kinds of transistor architectures based on WO_3, in order to obtain a device that exhibits optical and electrical modulation. The two former topics were achieved using photolithographic and lift-off processes for sequential layer deposition and pattern definition. The fabricated ECTFTs consist of a planar configuration based on three sequential layers, as it is a commonly used architecture in the area of ECTs:

1. Electrical contacts (gate, source, drain, back-electrode): IZO deposited by radio-frequency (RF) magnetron sputtering or titanium (Ti) deposited by electron-beam evaporation;
2. Semiconductor layer: WO_3 deposited by RF magnetron sputtering;
3. Dielectric layer: solid-state lithium-based polymer electrolyte, developed by other ongoing projects in CENIMAT | I3N in the area of ECDs,[58] deposited by drop-casting.

The final topic is one of the main concerns of this work, consisting of a structural and opto-electrochemical study of WO_3 and an electrical characterization focused on the electrical contact materials and the static and dynamic responses (output and transfer characteristics) of the developed ECTFTs. Furthermore, stability tests of the ECTFTs were conducted aiming for a better understanding of the used encapsulation techniques (Poly(methyl methacrylate) - PMMA). As these procedures present a considerable part of this work, they will be described briefly in the following sections, giving additional insight into device development procedures.

2.1. Fabrication and optimization of the ECTFTs

The different transistor architectures were previously designed using the Computer Aided Design (CAD) software corelDRAW X5. The first and most common of the three TFT architectures is the conventional structure (**Figure 2.1 A**), the second an interdigital configuration (**Figure 2.1 B**) and the third and final architecture is an innovative one that introduces a back-electrode (BE) beneath the channel, between source and drain (**Figure 2.1 C**).

As the mask offers space for more than one possible structure, a statistical approach for the mask definition was taken, in order to alter specific geometric properties of the structures while maintaining the basic architecture. Therefore, the most crucial geometric parameters, including gate to channel separations (b), channel lengths (b, c) and the BE dimensions (d) were varied, as shown **Figure 2.1**, in order to detect their influences on the devices' performances.

Table 2.1 lists a summary of the used spacing for the different parameters. A simple nomenclature will be introduced for device identification, where the uppercase letters represent the device architecture and the lowercase letters the corresponding device dimensions (for example, device Aa2b1 stands for the conventional structure with 50 µm channel length and 170 µm gate to channel distance or Ca2c3d3 would be the BE structure with 170 µm gate to channel distance, 500 µm of channel length and 300 µm of BE width). As for parameters a and b, all permutations are possible in contrast to parameters c and d, where only c1d1, c2d2, c3d3 or c4d4 are possible.

Table 2.1 - Dimensions of the different parameters used for ECTFT fabrication, where a is the gate-to-channel distance, b and c are the channel lengths and d the BE widths.

Parameters	a	b	c	d
Dimensions (µm)	a1 = 120 a2 = 170	b1 = 50 b2 = 100	c1 = 250 c2 = 350 c3 = 500 c4 = 800	d1 = 150 d2 = 200 d3 = 300 d4 = 500

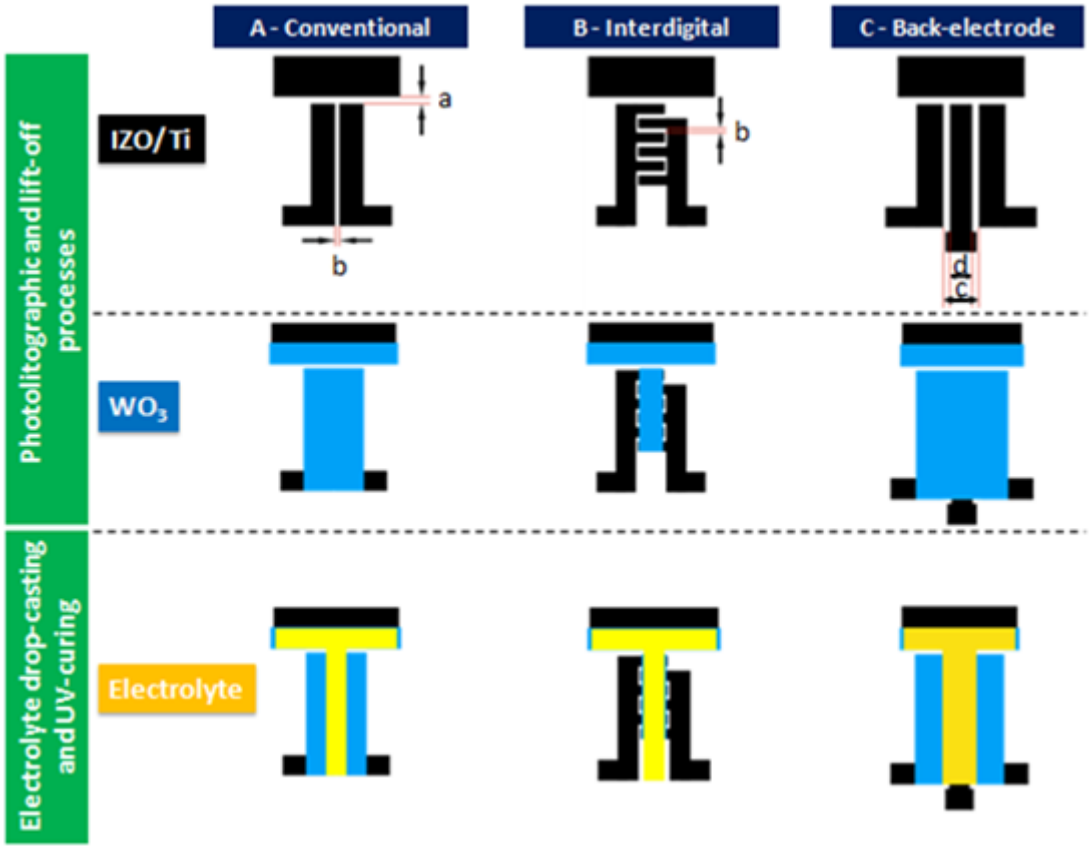

Figure 2.1 - Exemplification of the three implemented transistor architectures (A, B and C) with respective dimensional parameters (a, b, c and d) and their distinct layers. A – Conventional architecture; B – Interdigital architecture; C **–** BE architecture; a – Distances between gate and channel; b and c – Channel lengths; d – BE widths.

The ECTFTs were fabricated with no intentional substrate heating on Corning glass (Eagle XG) and PEN (supported on silicon wafer). The latter one was used in order to produce a flexible and completely transparent device as a proof-of-concept. One initial concern of the fabrication process is the substrate cleaning carried out in an ultrasonic bath for 10 minutes, first in acetone and then in isopropanol, after that, rinsed off in ultra-pure Millipore water and finally dried using nitrogen. Two minutes on a hot plate at 100 ^{o}C eliminated residual water. Regarding the photolithographic process, illustrated in Annex F, the whole procedure was conducted in a yellow room environment, located in the clean/yellow room of *Departamento de Ciência dos Materiais* (DCM). Throughout this work a positive photoresist (AZ1518) and a negative mask were used. To apply the photoresist on the substrate a spin coater system Karl Suss SM 240 was used, firstly at lower velocities of about 1000 rpm for 10 seconds for film uniformization, followed by 3500 rpm for 20 seconds for excessive photoresist removal and thickness definition. In order to reduce the solvent content in the photoresist and enhance adhesion, the substrate was heated at roughly 115-120 ^{o}C for 1 minute and 20 seconds in a process designated as softbake. Mask alignment and UV exposure, was conducted with a mask-aligner (Kark Suss MA 45). The alignment procedure was carried out under proximity mode, while the 30 seconds exposure was done under contact mode. Subsequently the photoresist was developed using a metal-ion-free tetramethyl-ammonium-hydroxide developer (AZ 726 MIF), followed by a cleaning and drying step with ultra-pure water and nitrogen, respectively. Concluding this sequence of steps, the windows opened in the photoresist are destined for film deposition. Development was then followed by the functional layer deposition, after which a lift-off was conducted, using 3 minute ultra-sonic acetone and isopropanol baths.

This whole procedure was repeated two times, in order to firstly define the pattern of the electrical contacts (IZO or Ti) and then of the semiconducting layer (WO_3). The deposition of these two layers was carried out in the clean room of CEMOP│UNINOVA, using the deposition parameters indicated in in Annex G. During WO_3 deposition for the ECTFTs, ITO pre-coated glass (Xin Yan Technology, 155 ± 20 nm of ITO, 15 Ω/□, T ≥ 85% at 550 nm) was also introduced into the chamber for subsequent electrochemical and EC characterization of the obtained WO_3 thin-films.

Concluding the ECTFTs fabrication process, electrolyte was drop-casted onto the EC layers, as depicted in **Figure 1.3 a)**, and subsequently UV-cured for 3 minutes in the yellow room of CENIMAT│I3N. For some specific devices an additional passivation step with PMMA spray, for electrolyte encapsulation, was performed.

2.2. Characterization Techniques

2.2.1 Electrical Contacts, EC Films and Electrolyte Characterization

The films thicknesses were measured with an Ambios XP-200 Profilometer. The structural properties of the EC films deposited onto Corning glass substrates were examined by X-ray diffraction (XRD) using a PANalytical X'Pert Pro in Bragg-Brentano geometry with Cu-Kα radiation (λ = 1,5406 Å) and atomic force microscopy (AFM) using a MFP-3D by AsylumReserach Oxford Instruments.

The electrochemical response of the WO_3 films was evaluated by cyclic voltammetry (CV) with a Gamry Reference 600 potentiostat in a conventional three-electrode cell. The EC film deposited on an ITO/glass electrode was the working electrode, a platinum wire was used as the counter electrode, an Ag/AgCl electrode was the reference electrode and the supporting electrolyte was 0,5 M $LiClO_4$:PC. The contact area between electrolyte and EC film was 0,833 cm^2. All films were electrochemically cycled from 1 to -1 V (vs. Ag/AgCl), at a scan rate of 20 mVs^{-1}, for specific coloration/bleaching cycles.

Optical measurements were performed on the same electrochemical cell in a three-electrode arrangement, using a spectrometer set-up consisting of an HR4000 high-resolution spectrometer (Ocean Optics), halogen light source HL-2000-FHSA (Mikropack) and QP600-2-SR/BX optical fibers (type, SR; fiber core diameter, 600 µm; connector, QSMA; jacketting, BX) and the applied voltage was controlled by a Gamry Reference 600 potentiostat. The EC behavior of the WO_3 films was investigated by measuring the *in-situ* transmittance changes at λ = 633 nm as well as their stabilities. The films were colored and bleached for 30 seconds at operating voltage values of -1 and 1 V, respectively. For calibration, the measurements were performed, considering the electrochemical cell with glass/ITO/EC immersed in a 0,5 M $LiClO_4$:PC electrolyte as 100 % transmittance.

Electrochemical impedance spectroscopy (EIS) was conducted to determine the electrical properties of the used electrolyte. Using a Gamry Reference 600 potentiostat an AC potential of 25 mV rms, at different frequencies, was applied to an electrochemical cell composed of glass/ITO/Electrolyte/ITO/Glass with dimensions indicated in (**Figure 3.4**). The cell thickness was measured using a Mitotyo Micrometer. The fittings for the equivalent circuit models (ECMs) were carried out using Gamry Echem Analyst.

Sheet resistance measurements of the Ti and IZO contacts were performed using four-point-probe (FPP) technique (Jandel Engineering) with forward bias and a forced current of 1 mA and Hall-effect measurements (BIO-RAD/ Nitrogen Stage), respectively.

2.2.2 Static and Dynamic Electrical ECTFT Characterization

Static and dynamic electrical characterizations were conducted at room temperature (RT) using a Semiconductor Characterization System (Keithley 4200-SCS) with a Cryogenic Equipment by JANIS Probe Station. It is also equipped with an Illumination and Microscope system by eo Edmund Optics Worldwide MI-150 HIGH-INTENSITY ILLUMINATOR for image acquisition. In all tests (static and dynamic) V_D was kept at a constant voltage of 1 V. Initially a static gate voltage of 4 and -4 V for up to 40 seconds, respectively, was applied to assess the transistors I_D in the ON and OFF state, respectively. For the transfer curves V_G was initially held at -4 V for 20 seconds for stabilization and then swept in 0,2 V steps, from -4 to 4 V and back with sweep delays (time interval between gate voltage points) of 0,5, 1, 2, 5 and 10 seconds. V_B was always kept at -1 V, except for the 1 s sweep delay, applying progressively -2, -1 and 0 V, in order to investigate V_{ON} shifts.

For symmetric dynamic electrical characterizations V_G was commuted between -4 and 4 V at frequencies of 2, 1, 0,5, 0,2, 0,1, 0,05, 0,025 and 0,0125 Hz. Asymmetric dynamic electrical characterizations were carried out at the same frequencies but for V_G between -6 and 4 V.

Transfer curves during substrate bending (mechanical stress) for the transistors fabricated on PEN were conducted using convex iron supports, as examplified in Annex H, with curvatures of 0,67, 0,44 and 0,31 cm^{-1} (r={1,5; 2,25; 3,25} cm).

3.RESULTS AND DISCUSSION

3.1 Characterization and Properties of the Sputtered EC films

3.1.1 Structural Analysis

As described beforehand in section 2.1, during WO_3 deposition no intentional substrate heating was carried out, as the final objective is the ECTFT fabrication on a flexible PEN substrate, which is not suited for high temperature annealing. Therefore, it was of interest characterizing the ECTFTs' electrical performances with highly amorphous WO_3 films. A structural analysis of a sputtered WO_3 film on corning glass was conducted using XRD and complementary AFM to evidence its amorphous nature.

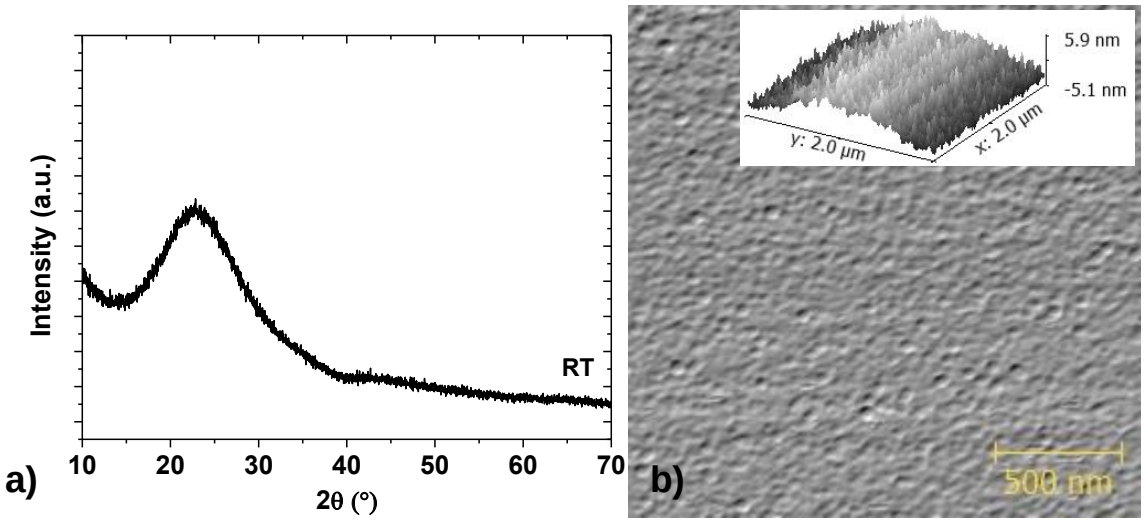

Figure 3.1 – **a)** Diffractogram of a sputtered WO_3 film on glass without substrate heating or *in-situ* annealing, as indicated by RT and **b)** the corresponding topographical and 3D view of the surface obtained by AFM.

Analyzing the obtained diffractogram (see **Figure 3.1 a**) it is clearly observable that no preferred crystallographic orientations are present in the film. A lump is observed situated at about 2θ = 24°, which is associated with the disordered nature of the film.[105] The topography of the film (see **Figure 3.1 b**) shows a relatively smooth surface with peaks of merely a few nanometre. Additionally no grains are observabe. Raman spectroscopy could give further insight into the materials characteristics and would therefore be suggested for a more profound investigation. Knowing the crystallographic nature of the fabricated WO_3 films helps with the interpretation of the results from the following section, as such properties heavily influence the films electrochemical and electro-optical capabilities.[19]

3.1.2 Electrochromic and Electrochemical Properties

One of the most important characteristics of an EC film is its optical modulation (coloration and bleaching) with external electric stimuli. Therefore electrochemical and electro-optical characterizations are fundamental in order to not only determine the basic EC properties mentioned in section 1.1 (color efficiency, optical memory, write erase efficiency, response time, durability and cyclability), but also to correlate these characteristics to the ECTFTs' performances, which are directly influenced by the properties of the EC films, as they constitute the semiconducting layer of the transistors. For the EC film preparation the same thicknesses and WO_3 deposition parameters were used as for the ECTFT fabrication, making it possible to directly connect conclusions from this chapter with the static and dynamic electrical characterization conducted in section 3.3. Using the techniques and process conditions described in chapter 2, transparent WO_3 thin-films deposited on ITO coated glass were obtained and this section will therefore evaluate their electro-optical characteristics.

The capability of an EC film to switch between the colored and the bleached state depends on a number of factors.[25] This includes most importantly the film thickness, as this ultimately determines the necessary charge insertion or extraction for full coloration or bleaching (stable transmissions). The focus will therefore be on three distinct WO_3 thicknesses of 75, 200 and 320 nm. For a thicker film consequently follows an increased number of electro-reducible sites. As ion diffusion and consequent EC redox-reactions are time dependent, thicker films of the same EC material logically exhibit longer

coloration and bleaching times. To characterize the stability, durability and reaction kinetics of the EC films in respect to their consistency of achieved transmittances several cycles were run for each of the three specimens. The whole data spectrum of the conducted chronocoulometry experiments can be accessed in Annex I. The first 20 cycles can be observed in **Figure 3.2 a)**, where the following 21st was used for a full bleaching-coloration-bleaching cycle, each state amounting to 30 seconds (see **Figure 3.2 b)**. From this cycle it is possible to extract vital EC parameters (see Annex J), such as coloration and bleaching times (t_c and t_b, respectively) as well as the associated optical density (ΔOD) at a specific wavelength of 633 nm. The variation of these parameters with the film thickness is represented in **Figure 3.3 a)**.

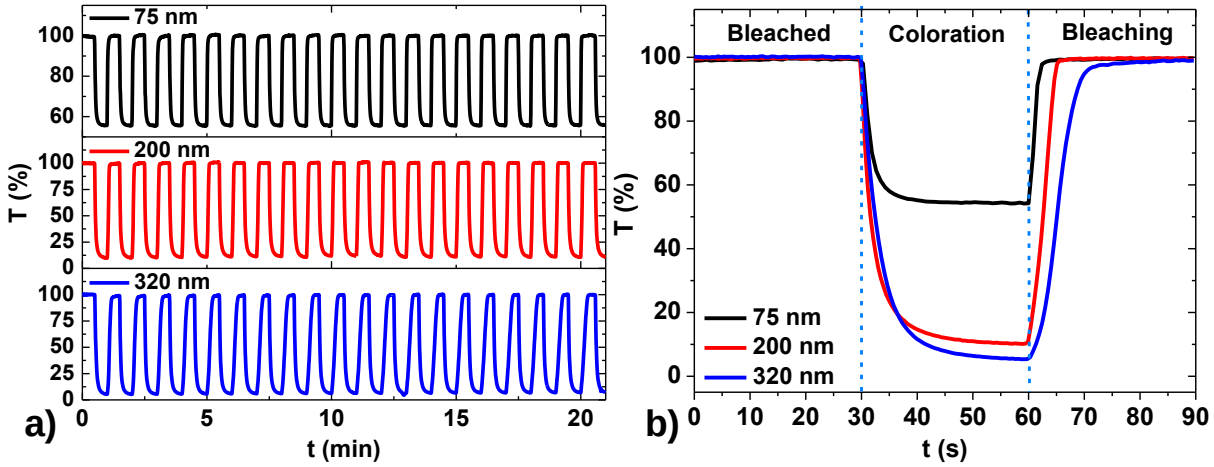

Figure 3.2 - Transmittance versus time for voltages of 1 V (bleaching) and -1 V (coloring) during 30 seconds each. Where **a)** shows the first 20 cycles and **b)** the 21st cycle used for EC parameter calculations.

Considering the first 20 cycles it becomes evident that all three films initially exhibit great stability, transiting between their colored and bleached state, as the films reduce and oxidate. This stability however was observed to level off for progressively higher cycles, where the colored state experienced more degradation than the bleached, eventually reaching a situation where the total transmittance difference (ΔT) falls below 15 %. From this point on the films are considered to exhibit no more significant EC behavior. The attenuation of ΔT is associated to mainly two factors: trapped charges (Li^+) unable to exit the film and a continuos electrolyte degradation. Trapped charges are a direct consequence of the films behavior observed in Annex K, where the inserted charges after 30 seconds of coloring never equal the extracted charges after a subsequent bleaching cycle. Put differently the charge balance is less than 1 ($Q_{in}/Q_{ext} < 1$, where Q_{in} and Q_{ext} represent inserted and extracted charges, respectively). Ideally and for a highly durable film this quotient should be equal or close to unity. Electrolyte degradation is the second influencing factor on the films stability over time. Being an organic electrolyte and in contact with the environment (due to experimental setup) it experiences degradation, loosing its ability to effectively provide lithium ions for EC reactions. However, both of these problems can be counteracted with the integration of a counter electrode (better charge balance) and their encapsulation into a closed device (minimal to no electrolyte degradation).[106]

The 21st cycle, shown in **Figure 3.2 b)**, produces some interesting results in respect to film thickness variations. To begin with, all specimens show close to 100 % transmittance in the bleached state. Logically, when moving to thicker films the transmittance for the colored states showed a considerable decrease from about 55 % (75 nm) to roughly 5 % (320 nm). For each 30 seconds coloration and bleaching a good stabilization of the measured transmittance was reached, evidencing that additional charge insertion or extraction leads to no further considerable color variation. A rise in film thickness was verified to lead in general to increased ΔOD and CE, nontheless reaction kinetics are hindered as charge insertion is higher, leading to increased t_c and t_b (see **Figure 3.3 a**). The former two are of high interest for the ECTFT switching speeds as these times ultimately dictate the transistor's rapidity to commute between the ON and OFF state. Factors that influence t_c and t_b include: film thickness, structure and conductivity of the EC film, interface between EC film and electrolite and the ionic conductivity of the electrolite. For all three films bleaching took place more rapidly than coloration ($t_b < t_c$). This can be explained by considering the films electrical conductivity in each state. The EC film in the bleached state is an insulator with a conductivity of 10^{-9} Scm^{-1},[71] hence this state complicates effective electron conduction, resulting in a hinderence of the EC reaction for its transition to the

colored state. When the film is in the colored state it possesses a far greater conductivity, thus the electrons can quickly leave the film when bleaching takes place. The limiting factor for this transition is consequently the ion migration out of the film, which is facilitated due to its amorphous structure.[69] It is noteworthy that a highly permeable film further accelerates EC kinetics due to enhanced ion intercalation and deintercalation.[53]

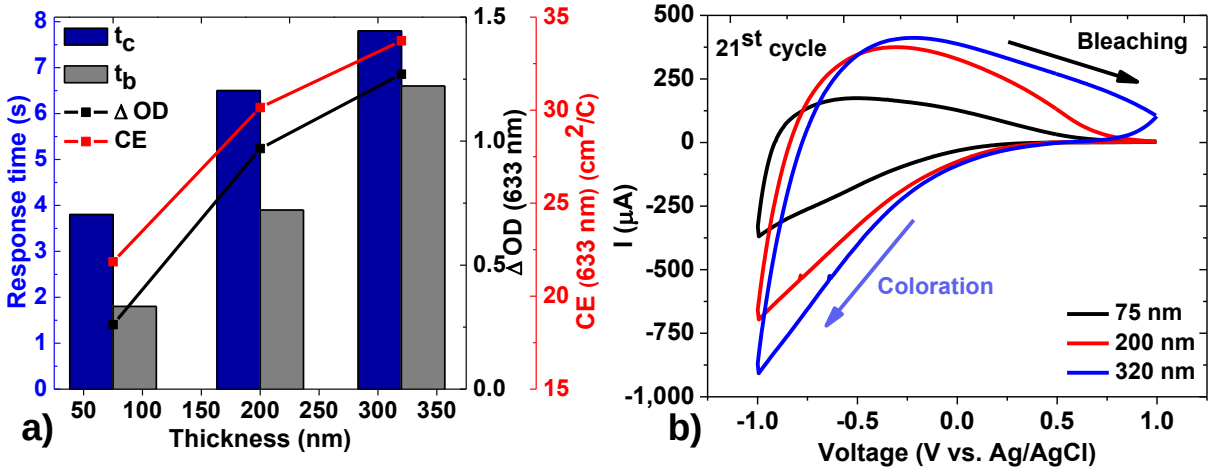

Figure 3.3 - **a)** Crucial EC parameters, including coloration and bleaching times t_c and t_b, respectively, optical density (ΔOD) and color efficiency (CE) and **b)** 21st cycle of CV from -1 to 1 V and back with a scan rate of 20 mVs^{-1} for respective bleaching and coloration, each for 75, 200 and 320 nm of WO_3 films.

In **Figure 3.3 b)** three CV curves are represented for each film thickness, where an applied voltage was swept from -1 to 1 V (vs. Ag/AgCl) and back and the resulting current going in and out of the film was measured. The whole data spectrum of the conducted CV can be accessed in Annex L. As mentioned in section 1.1 WO_3 is a material that undergoes cathodic coloration, which is connected to the insertion of electrons and charge compensating ions for coloration (sweeping to negative voltages) and the opposite mechanism for bleaching (sweeping to positive voltages). Having this process in mind it is only logical that a negative current (in respect to the reference electrode) is measured going into the film for negative voltages and a positive one coming out of the film for positive voltages,[107] which was found to be exactly the case for the investigated films. Furthermore, increased film thicknesses produced higher currents and also increased areas between the curves, which is based on the fact that thicker films offer more electro-reducible sites, thus experiencing higher charge insertion. This observation is likewise proven by charge insertion and extraction measurements during chronocoulometry (see Annex K) and current still exiting the film when already sweeping back from 1 V for the 320 nm film in **Figure 3.3 b)**.

The investigated films showed reproducible results, as can also be verified by comparing with existing research on electrochemical and electro-optical characterizations for WO_3 films.[68] The obtained results, especially ΔOD and transition times (t_c and t_b), give valuable insight into their possible use in PM or AM matrix display applications. Further, as stated beforehand and being the main interest throughout this work, they are suitable for transistor applications as a two-in-one solution due to their double functionality (change in coloration and conductivity). The obtained results in this section will be taken into consideration later in this work for investigations on the static and dynamic electrical characterization of the ECTFTs.

Another important constituent is the used electrolyte, and its performance under different frequencies, as it constitutes the dielectric layer and the ion source for EC reactions. Therefore the next section will investigate the used lithium-based polymer electrolyte using electricochemical impedance spectroscopy (EIS).

3.2 Electrochemical Impedance Spectroscopy of the Lithium-Based Polymer Electrolyte

EIS is a well-known technique to determine the electrical properties of ionic materials,[108] where an AC potential at different frequencies (f) is applied to an electrochemical cell, so the total capacitor impedance (Z) can be measured as a function of the frequency. This gives valuable information about ion migration, EDL formation and the dielectric capacitance (C_i), which ultimately leads to an approximate determination of the ECTFTs' charge carrier mobility. The electrochemical cell prepared for EIS is, as shown in **Figure 3.4**, composed of 3 distinct layers. Explicitly two ITO coated glass substrates and, sandwiched in between, the solid-state lithium-based polymer electrolyte. The comportment of this cell can be described by a number of equivalent circuits for parameter determination. A closer look will be taken on two specific circuits that presented a reasonable fit for the investigated frequencies.

3.2.1 Equivalent Circuit Models and Parameter Fitting

In order to determine important parameters such as bulk resistivity (ρ) and ionic conductivity (σ_i), bulk capacitance (C_b) and EDL capacitance (C_{DL}), associated to the used electrolyte, the obtained data needs to be described by an equivalent circuit model (ECM). The first ECM, also known as the simplified Randels cell,[109] is composed of a resistance (R_{ext}), associated to contact resistances (ITO), in series with a parallel RC circuit (see **Figure 3.4 a**). The components of this RC circuit are solely associated to the electrolyte, where R_b represents the bulk resistance and CPE is a so-called constant phase element. The CPE mimics a non-ideal capacitive behavior, associated to interface inhomogeneities,[110] resulting in a line with less than 90° on the complex plane representation of the impedance (see Annex M). Its physical basis to date is only poorly understood [111, 112] and efforts are made towards its interpretation,[113] thus its application in this context relies on empirical models and is justified by its practicability for the proposed ECMs. It should be noted, that in the Randels cell model (ECM 1) the CPE not only accounts for the capacitance caused by dipole orientation for higher frequencies but also for the EDL formation and its associated capacitance at lower frequencies. This assumption however seems to be incompatible with the obtained data. As can be observed in **Figure 3.5 a)** at progressively higher frequencies, the behavior proposed by the ECM 1 becomes errorneous. A considerable phase (θ) drop and a stabilizing capacitance for higher frequencies suggest additional components or a modification to the ECM 1, that should be considered for that range of frequencies. In fact this has already been investigated by Dasgupta *et. al*. [84] and it was found that by a slight modification of ECM 1 the fitting for higher frequencies can be improved. The modification results in ECM 2 (see **Figure 3.4 b**), where the CPE is substituted by an electrolyte bulk capacitance C_b, accounting solely for dipolar relaxation of the electrolyte solvent molecules,[114] and connecting a CPE in series with the remaining components. However the value of C_b is often negligible, when compared to C_{DL}, and lies in the order of 10^{-10} Fcm^{-2} (see Annex N).

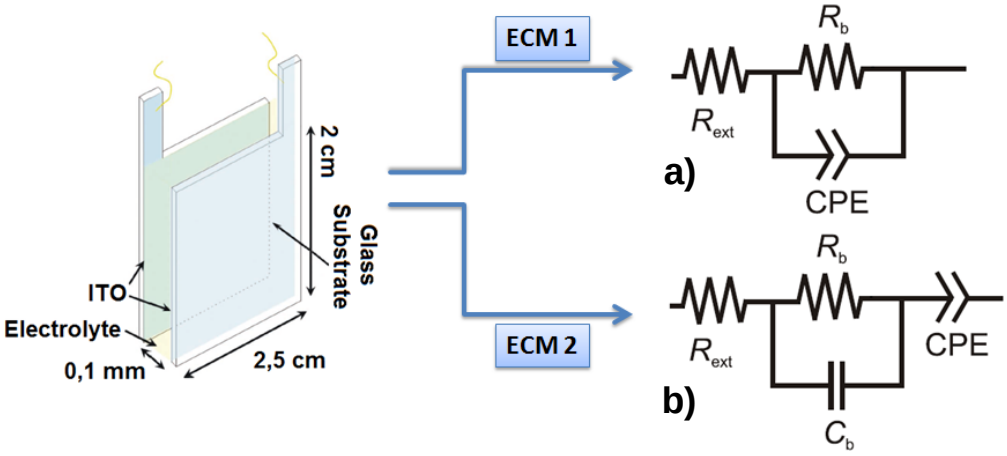

Figure 3.4 - Electrochemical cell setup and corresponding ECMs with **a)** ECM 1 (simplified Randels cell) and **b)** ECM 2 (modified simplified Randels cell). Adapted from [84].

The measured values (red circles) and the fitted curves (blue lines) for each model are depicted in **Figure 3.5** and evidence the improvements for higher frequencies when passing from ECM 1 to ECM 2. Considering the measured capacitance and phase values an electrochemical cell can, in general,

be classified, based on its phase into either predominantly capacitive (θ < -45°) or predominantly resistive (θ > -45°). On behalf of the phase, here mainly two regions can be identified. A capacitive behavior for f < 30 Hz, characterized by a high capacitance from the EDL formation and a resistive behavior from ionic relaxation for the remaining frequencies (30 Hz < f < 10^6 Hz), characterized by a falling capacitance. A third region is developing, as a falling phase for f > 10^4 Hz indicates a capacitive component deriving from dipolar relaxation for higher frequencies.[115] The found ECM 2 works great throughout the whole frequency spectrum as can also be verified by the total impedance graph (Annex O) and the associated Nyquist plot (Annex M). Especially in the Nyquist plot discrepancies between ECM 1 and ECM 2 become clear. Whereas ECM 1 does not take any charge transfers (dipole relaxation) for higher frequencies into account, ECM 2 shows a clear semicircle, matching the measured data points. This semicircle is likewise proven by a decreasing total impedance for f > 10^5 Hz for ECM 2, where ECM 1 continues with a straight line. Both however predict reasonably well the occurring mass transfers across the EDL due to possible ion diffusion into the ITO film, hence the non-ideal capacitor with resistive characteristics (line with less than 90°).

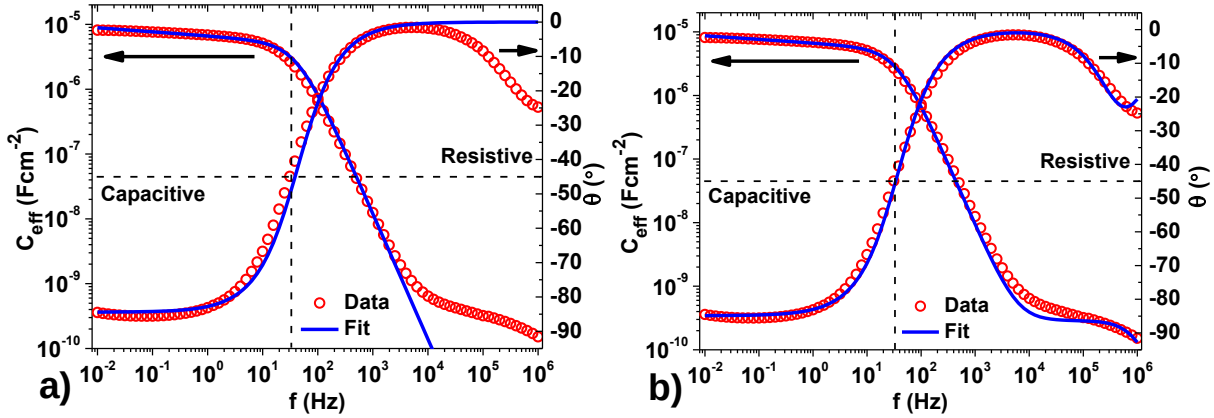

Figure 3.5 – The measured effective capacitance and phases (red circles) and fitted curves (blue lines) for **a)** ECM 1 and **b)** ECM 2. For **a)** diverging behaviors become clear for higher frequencies, whereas for **b)** the fitting approximates the measured data. Dashed lines indicate frequency and phase, where transition from capacitive to resistive and vice-versa occurs.

At this point it is essential to give some contemplation about the dynamic electrical characterization that will be undertaken to test the ECTFTs' performances at different frequencies. As was verified by electrochemical characterization and as will be seen in section 3.3.2 ion diffusion and EC reactions need time and the applied frequency at the gate must be relatively small in order to efficiently color the channel region and promote the transistors to effectively enter the saturation regime (stable drain current). This observation limits the frequencies of interest, which will be seen to situate below 10 Hz. It can be truthfully reasoned that for this range of frequencies both ECM models present satisfying fittings and could be used to determine the following parameters. Nonetheless ECM 2 was chosen, producing a higher fit goodness to the obtained data.

The highest investigated frequency during dynamic electrical characterization was in fact 2 Hz, as this frequency was found to produce close to unity current gain for some ECTFTs, presenting the cut-off frequency (see f_{co} in section 3.3.5.2). At these frequencies complete ionic relaxation takes place and the developed capacitance at the electrolyte/electrode interface is solely due to the EDL. Additionally the frequencies are low enough to reasonably neglect C_b, as this capacitor only plays a role at very high frequencies. Therefore the model proposed by Jović *et al.* [116] for C_{DL} calculation can be used as follows:

$$C_{DL} = \left[Y_0 {R_{ext}}^{-(\alpha-1)}\right]^{1/\alpha} \tag{3.3}$$

Where Y_0 is the capacitance associated to the CPE. Regarding parameter α opinions are diverging. Whereas some [116] treat it as a fractal surface character associated to surface roughness, which gives the CPE a leaky capacitor behavior with non-uniform current distribution. Others [109] think it is best to treat it as an empirical constant with no sound physical basis. However, this factor determines how non-ideal the capacitor behaves, being mostly less than unity. For a value of 0.5 the CPE behaves like a Warburg impedance accounting for considerable ion diffusion into the film.[112] For the present case α was found to be 0.94, giving the CPE an over 90% capacitive behavior. With an Y_0 of 3.73x10^{-5} Ss^{α}, R_{ext} equal to 68 Ω and the cells area of 5 cm^2, C_{DL} yields 5.10 μFcm^{-2}. This value is in

approximate concordance with the measured effective capacitance (C_{eff}) for low frequencies (see **Figure 3.5**) and the main contributor for C_i (C_b is negligible). Using the dimensions indicated in **Figure 3.4** and the resistance of the bulk electrolyte from the fitting of ECM 2 (R_b = 87.34 in Annex N) the ionic conductivity (σ_i) of the electrolyte was determined as 2.29×10^{-5} Scm^{-1}, using the accepted equation from the literature.[117]

The calculated values for C_{DL} and σ_i highly depend on the taken approach, cell setup and dimensions, fitting parameters and considered resistances, where diverging opinions on this subject often produce quite different results.[84, 113, 116] As criticized by Abouzari *et al.* it is evident that performing impedance analysis at frequencies below some MHz is a straightforward procedure, but the physical interpretation of the experimental data is often rather complex. Nevertheless, the found value for C_{DL} for the approach taken in this work shows concordance with existing literature, laying in the typical order of 1 - 10 μFcm^{-2}, described by Kim *et al.* for EGTs.[35] The ionic conductivity also showed to be comparable with existing research on a similar polymer electrolyte, laying in the same order of magnitude.[118-120]

With the obtained value of C_{DL} it will be possible, during electrical characterization, to estimate charge carrier mobilities and to compare the fabricated ECTFTs based on these parameters to existing technologies.

3.3 Electrical Characterization

Taking advantage of the influences of the EC reaction on the tungsten oxide's electrical properties and their potential application in transistors as the semiconducting layer has been outlined in section 1.2. The key part of this work was to explore and describe this specific property and possibly harness the arising double functionality for practical applications. This section is therefore dedicated to the electrical characterization of the fabricated ECTFTs. The aim is to explain the basic working principle of the studied architectures based on their static and dynamic electrical performances. This study also serves to narrow down the field of all the fabricated ECTFTs to the best combination of the studied dimension parameters. Later the best performing architectures of A, B and C will be compared to each other, with static and dynamic electrical characterization, in order to determine their possible fields of application. Special emphasis will be given on their use in either display or electric circuit/ biosensor applications, as the device's final application dictates its necessary performance (switching speed, stability, coloration of EC material etc.).

Essentially two different parameters, consisting of the architecture type (A, B and C) and the EC film thickness, are going to be examined, as these have been proven to be decisive in the transistors' electrical behaviors. As shown in previous work [121] and studied beforehand (section 3.1.2) the EC film thickness strongly influences the EC properties. For thicker films greater optical density and color efficiency is achieved, but on the other hand, higher coloration and bleaching times were observed (see **Figure 3.3 a**), which could effect the ECTFTs' response times (complete channel reduction and oxidation). The architecture type is an extrinsic parameter to the EC film, it could however show influences on the transistors' performances, as miniaturization or differing structures from the normal approaches (B or C) could play a crucial role in this type of device, by for example facilitating EC reactions. To exclude any possible errors associated to contact resistances by TCOs and to investigate the pure EC behavior of WO_3 as the semiconducting layer, first considerations will be taken by analyzing ECTFTs with titanium contacts. Thereafter, a transition to fully transparent transistors, using IZO contacts on flexible substrate (PEN), will be undertaken to investigate contact and substrate factors.

3.3.1 Electrical Contacts

The sputtered IZO films were electrically characterized with Hall-effect measurements to determine parameters, such as bulk and sheet resistivity, electron mobility and carrier concentration. A low resistivity and high mobilities are desired in order to facilitate electron migration through the contacts into the EC film for reduction reactions and through the transistor channel. The initial parameters used for IZO thin-film deposition lead to films with relatively high resistivity, however acceptable electron mobilities.[122] An increase of the partial oxygen pressure (P_{O2}) from 1.3×10^{-5} mbar to 1.5×10^{-5} mbar shows a decrease in resistivity and higher carrier concentration for a slightly lower film thickness, normally suggesting higher resistivity. This trend was shown to be valid, due to oxygen deficiency compensation,[123] until an excessive amount of P_{O2} (3% of total chamber pressure upwards) reduces the insertion of sufficient oxygen vacancies, which constitute donor sites of two free electrons.[124]

Therefore an intermediate value of P_{O2} needs to be found in order to obtain lowest resistivity. The two films showed similar mobilities, suggesting a comparable distribution of ionized scattering centers of carrier sites, such as electrically active oxygen vacancies.[125] For IZO films with enhanced electrical properties an extended study on the above mentioned parameters would be necessary. However, the obtained films with increased P_{O2} (see Sample 2 in Annex P) presented satisfying properties, with a sheet resistance (R_s) and bulk resistivity (ρ) of 37.8 Ω/□ and 3.02×10^{-4} Ωcm, for their use as electrodes in ECTFTs, hence no further optimization was required.

The titanium films, being more conductive than the IZO films, were electrically characterized by the FPP, a simpler and faster technique than Hall-effect measurements, suitable for materials with high conductivities. The obtained 100 nm thick titanium films presented a sheet resistance and bulk resistivity of 8.2 Ω/□ and 8.2×10^{-5} Ωcm, respectively, yielding, as expected, one order of magnitude lower than the IZO films.

3.3.2 Properties and Fundamental Working Principle of the Fabricated ECTFTs

The fabricated ECTFTs rely on ion migration in an electrolyte, charge build-ups at interfaces and consequent electrochemical doping and de-doping (reversible redox reactions: Faradaic processes) of the channel region. This enables the transistor to switch between the ON and OFF state depending on the applied potential to the gate electrode. WO_3 behaves similar to an n-type semiconductor, logically a negative gate voltage turns the transistor OFF and a positive one turns it ON. A simple yet illustrative way to show this behavior is depicted in **Figure 3.6**, where the normalized channel resistance varies over time with a constant gate voltage of 4 or -4 V applied for respective reduction and oxidation of the channel region.

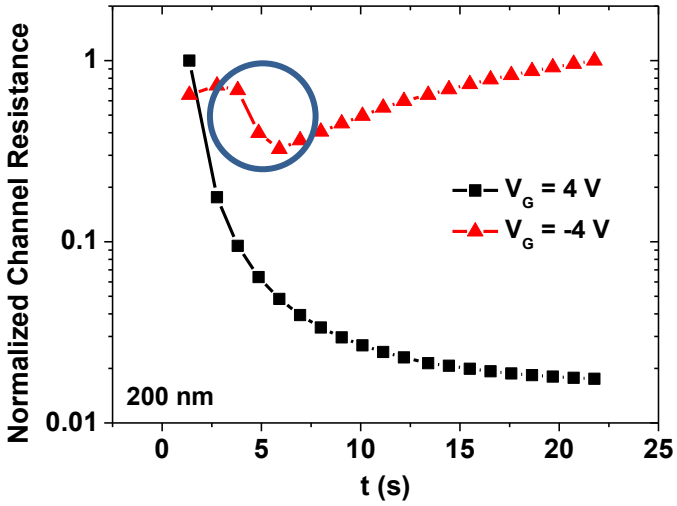

Figure 3.6 – Time dependence of the normalized channel resistance of a Aa2b2 architecture with 200 nm WO_3 and V_G of 4 and -4 V. The blue circle indicates an apparent channel resistance drop due to WO_3 oxidation and consequent electron release.

For V_G = 4 V a continuous reduction of the channel region leads to an increasingly lower channel resistance. After roughly 20 seconds the channel resistance stabilizes at approximately 2% of the initial channel resistance. On the other hand, applying V_G = -4 V the channel seems to close fast, reaching a high resistance after a few seconds. This observation is supported by chronoamperommetry, where bleaching (oxidation) is also faster than coloring (reduction), following the process described in section 3.1.2. Nevertheless, a drop of channel resistance is observed at about 5 seconds (see blue circle in **Figure 3.6**). This behavior can be associated to oxidation processes in the WO_3 layer, which are accompanied by electron releases leading to an apparent current flow through the channel. A similar behavior can be observed during CV, where current peaks are caused by redox reactions.

With this channel resistance behavior it is expected, that the drain current will comute between I_{OFF} and I_{ON} when sweeping the gate voltage from negative to positive values. Due to the electric potential drop from drain (1 V) to source (ground) it becomes evident that the lithium ions (necessary for reduction) in the electrolyte firstly migrate to the source end, when V_G reaches 0 V and V_{GS} turns positive. But V_{GD} continues negative, inhibiting ion migration to the drain end of the channel. This

observation is valid for both architecture types A and B. It is, however, slightly different for the case of architecture C; the involved ion movement for this type is dissimilar and will receive further explanation in section 3.3.4. For type A and B the intermediate situation, where $V_S < V_G < V_D$, results in an EC coloration front moving from the source to the drain end of the channel as V_G increases until 1 V; the point where V_{GD} also turns positive. This front is also visible through the characteristic blue color of the continuously reducing WO_3 (see channel coloration in Annex Q). This simple but effective point of view suggests an enhancement working mode of the fabricated ECTFTs, as only positive gate voltages are capable of complete channel induction at the drain end. However, for higher sweep delays it was possible to pull V_{ON} extremely close to 0 V (see **Figure 3.9**). This implies that for a sufficiently long time at zero gate voltage the drain current eventually starts to rise due to inevitable sporadic channel reduction. Nonetheless, this situation would never completely turn the transistor ON, leaving it in an intermediate state. So to fully turn the transistor ON it is mandatory to effectively pull the gate towards the drain voltage.

However, there is more to this apparently simple working mode. As described in section 1.2 ECTs operate in two fundamental different modes that nevertheless occur at the same time, while sweeping the gate voltage from negative to positive and back. It was found that this holds also truth for the ECTFTs fabricated throughout this work. The two modes are field-effect, owing to charge carrier induction by ion accumulation at the channel/electrolyte interface, forming an EDL, and electrochemical doping, owing to the ion permeability and subsequent reduction of the WO_3 in the channel region. Therefore both of the working modes contribute to an increase of the transistor's drain current. The interaction of these two processes, during static and dynamic electrical characterization, are rather complex and have not yet been described to an extent.[34]

For simplification purposes the gate electrode/electrolyte/channel region can be seen as an electrolytic capacitor (see Annex R), where the gate and the channel region constitute the two electrodes and the electrolyte functions as the dielectric. When applying a voltage at the gate electrode an electric field develops throughout the electrolyte (see Annex R **b**). This causes ion movement, where cations and anions migrate to the negative and positive sides of the potential, respectively. This process and the formation of EDLs at the interfaces are designated as ionic relaxation (see Annex R **c**). Effectively, the entire applied voltage drops across the two EDLs and the electric field becomes very high at the interfaces, but negligible in the charge-neutral electrolyte bulk, as can be observed in Annex R **d)**.[115]

Comparing the time of ionic relaxation from EIS with that determined of reducing WO_3 from electrochemical measurements, it is evident that EDL formation at the channel/electrolyte interface occurs faster than ion diffusion into the WO_3 film. Additionally, for effective net ion diffusion into the WO_3 to occur, a relatively steep ion gradient at the channel/electrolyte interface is advantageous, which in turn constitutes the EDL. With low V_G the EDL is rapidly developed consisting of merely a monolayer of ions (Helmholtz layer),[126] forming an approximate parallel plate capacitor with only a few Angstroms of distance, sufficient for channel induction but not enough for an effective net diffusion of ions into the EC film. Consecutive higher gate voltages then accumulate more and more ions in the diffusion layer, which provides successively higher ion concentration gradients at the interface. This process enables effective electrochemical doping, where ions that diffuse from the Helmholtz layer into the EC film are quickly compensated from the electrolyte, maintaining the EDL.

Consequently a simple surmise would impute a predominantly field-effect mode, due to the EDL charge transfer into the channel, in the subthreshold region, which continuously transitions to a predominantly electrochemical mode in the saturation region, due to the electrochemical reaction of WO_3. The term 'predominantly' is used as electrochemical doping takes place since the EDL is formed, which is from V_{ON} upwards resulting in an overlapping of both processes. The exact determination of this behavior can only be fully assessed with *in-situ* absorption spectroscopy during electrical characterization as proposed by Frisbie *et al.*[127] With this technique it would be possible to effectively monitor the channel's absorbance at λ = 633 nm to determine at what point the transistor fully enters electrochemical mode.

Once the transistor fully enters electrochemical mode and the channel is mostly due to the conductivity of the reduced WO_3, the drain current keeps rising until the whole channel is reduced, reaching saturation (see continuous increase in I_D in **Figure 3.7**). The fact that this process turns the channel three-dimensional allows considerably higher drain currents, than those observed solely due to field-effect.[98] When sweeping V_G back little or no further WO_3 reduction takes place. This results in an approximately constant drain current, maintaining its value in the same order of magnitude, for gate voltages above V_D.

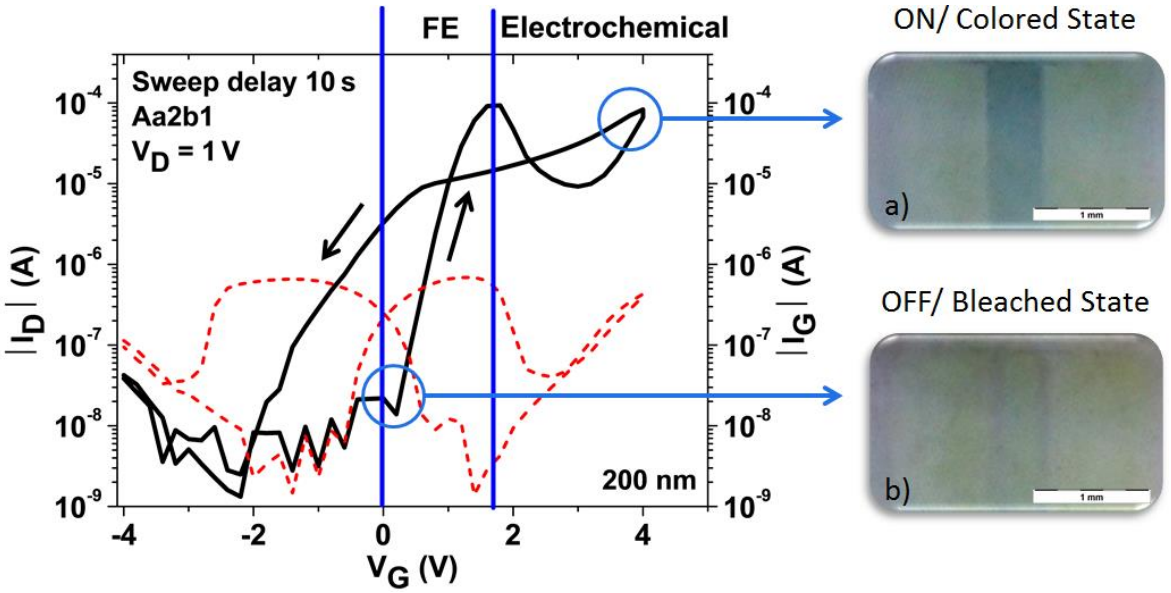

Figure 3.7 – A conventional ECTFT (architecture A) transfer curve with drain and gate (leakage) current. The field-effect to electrochemical doping transition can be observed at about 1,9 V. The two insets **a)** and **b)** show the channel region respectively in the ON (reduced) and OFF (bleached) state for an architecture C with 75 nm of WO_3 layer. Continuous and dashed line represent drain and leakage currents, respectively.

By pulling V_G below V_D the induced channel by EDL pinches off and the channel region starts to oxidize. Once again, as electrochemical reactions take time, the channel is kept open even without any field-effect. This fact together with the aparent current flow through the channel due to oxidation processes translates itself into a considerable counter clockwise hysteric behavior, as observed for every ECTFT in this work.

3.3.3 Influencing Factors on Field-effect to Electrochemical Doping Transition

The field-effect to electrochemical doping transition was observed for all three of the architecture types in study (A, B and C), as this transition is valid as long as there is electrochemical doping in the channel region. However, a clear visualization of this behavior, in the transfer curves, manifested as dependent on fundamentally three factors: EC film thickness, channel length (L) and the used sweep delay.

The EC film thickness and L define the volume of the EC material that needs to be reduced, not only to completely turn ON the transistor but also to obtain a good coloration. The more EC material is available for reduction, the more evident becomes the field-effect to electrochemical doping transition.

To investigate influences of the WO_3 layer thickness let us consider the two transfer curves depicted in **Figure 3.8 a)** from transistors of architecture type C with 75 (black curve) and 200 nm (blue curve). Both transistors show similar OFF currents in the subthreshold regime and comparable ON/OFF current ratios (≈10^5), which suggests analogous performances throughout the transfer curve. However for the transistor with 75 nm of WO_3 thickness the transition between the two modes occurs more continuous than for the transistor with 200 nm, which shows a current peak in the post-pinch off regime. This could be explained by considering the fundamental EC redox reaction of WO_3 (equation 1.1). This reaction requires charge compensating ion intercalation, as well as, electrons. Firstly ions are provided by the Helmholtz layer. A loss of ions from the EDL deteriorates the induced charge carriers by field-effect in the channel. The consumed ions will eventually be replaced by new ones from the electrolyte; however shielding effects from counterions (Cl^-) in the electrolyte could complicate this process. Secondly electrons are needed for the reduction reaction of the WO_3 in the channel. It is reasonable to assume, that the electrons coming from the source will not directly contribute to the drain current, but are rather used for the electrochemical reaction, which in turn could lead to a drop of the drain current. Only when enough WO_3 in the channel is reduced, so that conductivity is high enough and sufficient electrons pass through the channel to sustain EC reaction and to be collected by the drain electrode, a rise of drain current will be measured. The transition is best observed when the induced channel by field-effect reaches the pinch-off point at the drain end; the shallowest part of the channel region due to its tapered shape resulting from the voltage drop

across the channel (from V_{GS} to V_{GD}). The pinch-off happens for gate voltages equal to the applied drain voltage plus the threshold voltage ($V_{Dsat} = V_D + V_t$). It is assumed that at this specific point reduction reaction starts to take place even in the relatively small pinch-off volume. All of the drain current passes through that volume, thus, to reduce WO_3 in this region, a significant amount of the electrons are taken advantage of for the electrochemical reaction. Consequently thicker semiconducting layers mean higher quantities of WO_3 to be reduced at the drain end. Both of these processes could lead, in extreme cases, to severe drain current drops, as it is observable in **Figure 3.7** and **Figure 3.9 b)**. WO_3 layers of 75 nm have shown to bring sufficient coloration and best performances for electrical characterization so, if not stated otherwise, this will be the used thickness for further investigations.

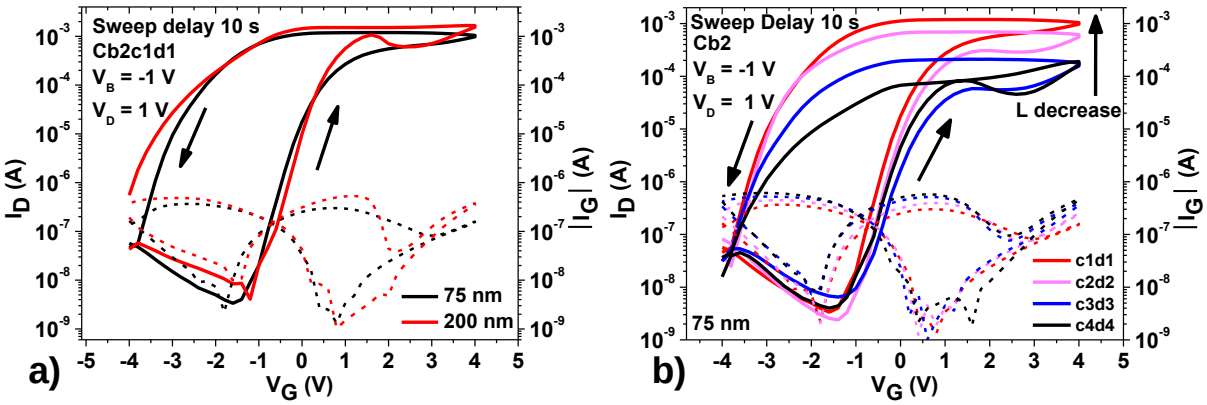

Figure 3.8 - Transfer characteristics for Cb2 structures. Evidencing the influence of **a)** WO3 film thickness and **b)** increasing channel length on the field-effect to electrochemical transition. Continuous and dashed lines represent drain and leakage currents, respectively. The extracted characteristic parameters for **a)** and **b)** are summarized in Annex S and Annex T, respectively.

Another parameter influencing the above described transition was found to be the channel length. For an increase in channel length for the same ECTFT architecture, gate leakage currents showed similar behaviors, whereas the associated drain currents behaved completely different (see **Figure 3.8 b**). It was found that an increase in channel length produced a more visible transition from field-effect to electrochemical doping. Apart from offsets in the measured ON currents, longer channel lengths also imply greater resistance to the drain current. Therefore effective electron transport to this part of the film, where they are needed for WO_3 reduction, is hindered. So the electrons that eventually make it that far do not necessarily contribute to the drain current but are used for electrochemical reactions instead.

Finally, it was found that the used sweep delay comprises another influencing factor on the field-effect to electrochemical doping transition, as this ultimately determines the ionic relaxation in the electrolyte. To investigate the transition's time dependence five different measurements were conducted with 0.5, 1, 2, 5 and 10 seconds. Some fundamental observations were made for increasing sweep delays. Firstly, it becomes evident that higher sweep delays produce steeper subthreshold slopes, which is reasonable, as there is more time for ionic relaxation and consequent charge build-up at the electrolyte/channel interface. Also, with more time provided, ions can penetrate deeper into the channel, resulting in more WO_3 reduction and higher channel conductivity. Secondly, a shift of V_{ON} towards 0 V was observed as the sweep delay was increased. A plausible explanation could be that independently what sweep delays are used, as V_G passes 0 V, ions start to migrate to the source end of the channel. The induced channel shortens the rest of the insulating channel, which then is subjected to an increased electrical field, capable of producing small drain currents. Consequently, the higher the sweep delay the more channel can be induced at the source end and an earlier rise of the drain current is observed (see **Figure 3.9**). Thirdly, the transfer curves showed an increasingly visible field-effect to electrochemical doping transition for higher sweep delays. This is mostly due to the velocity characteristics of EDL formation and ion diffusion, as described above. For low sweep delays (0.5 s) it is observed that I_{ON} at V_G = 4 V tends to be lower than when V_G sweeps back, where an increase in drain current is observed due to the time needed for effective electrochemical doping (see black curves in **Figure 3.9 a)**, **c)** and **d**). But, when increasing the sweep delay this happens earlier, as there is more time for ion intercalation (blue curves in same Figure). Eventually a critical sweep delay (pink to red curves in same Figure) is reached, when I_{ON} levels off (at about 2 – 3 V) and enters saturation. However, after that, electrochemical doping continues and I_D eventually keeps rising. For a

75 nm layer of WO_3 an increase in ON currents was verified, as the sweep delay was raised, on the contrary to the same transistor with a 200 nm thick WO_3 layer (compare **Figure 3.9 a)** and **b)** with sweep delay increase directions indicated by blue arrows). It is assumed that with a thinner layer, fewer electrons are needed for WO_3 reduction and the majority contributes to the drain current. For thicker layers more electrons are consumed by the electrochemical reaction and less contribute to the drain current. This is also evidenced by a difference of one order of magnitude of the ON currents between the two. Nonetheless for even higher sweep delays the transistor with a 200 nm layer will eventually produce higher drain currents than with a 75 nm layer, as the effective channel becomes thicker.

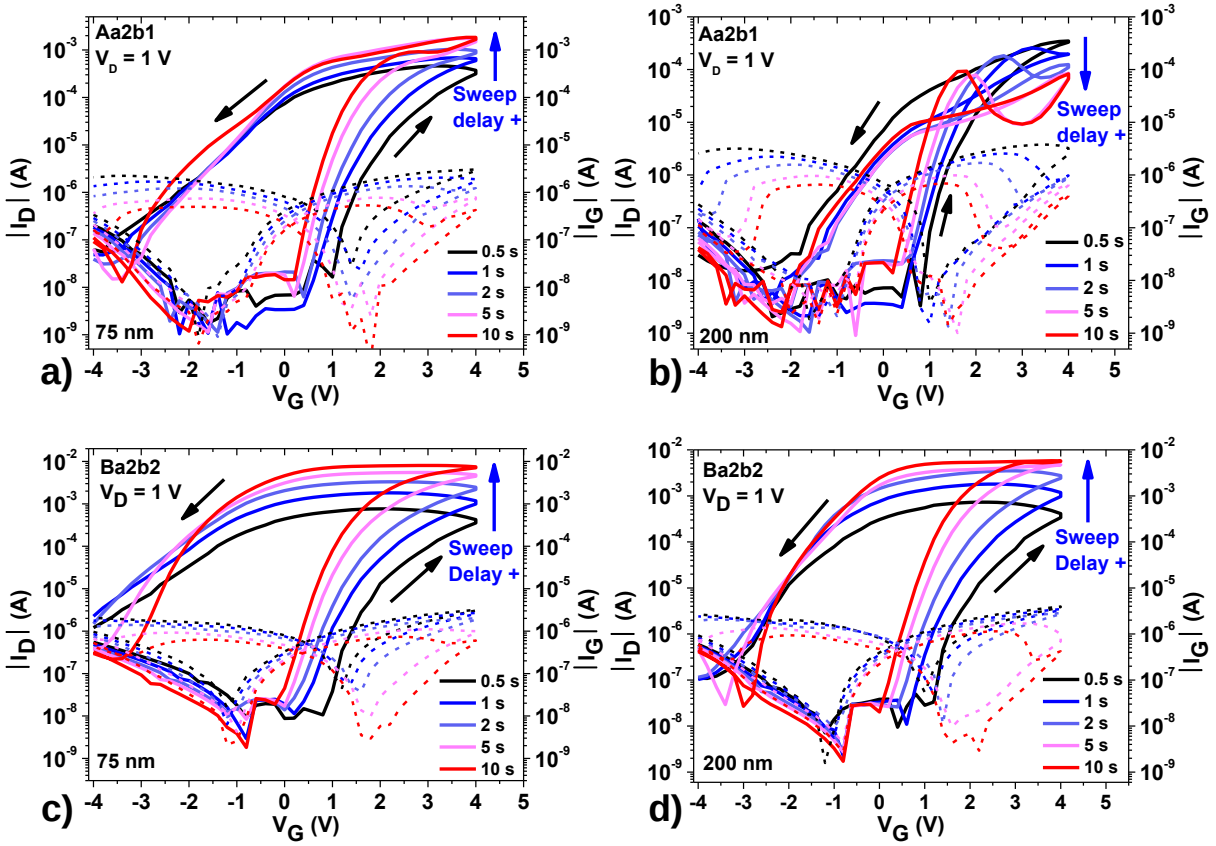

Figure 3.9 - Transfer curves for five different sweep delays of the Aa2b1 and Ba2b2 architectures with **a)** and **c)** 75 nm and **b)** and **d)** 200 nm layer of WO_3. Blue arrows indicate ON current shifts with increased sweep delays. Continuous and dashed lines represent drain and leakage currents, respectively. The extracted characteristic parameters for **a)**, **b)** and **c), d)** are summarized in Annex U and Annex V, respectively.

For architecture type B the current drops in the ON state were not as pronounced to non-existent, compared to the type A structure (see **Figure 3.9 c)** and **d**). Type B, being an interdigital architecture, is capable of creating a higher amount of possible pathways for electrons. This ensures sufficient electrons to reach the WO_3 film for reduction and the drain electrode for stable ON currents.

In terms of coloration qualities a sweep delay of 0.5 seconds did not produce any good colorations of the channel region, as it is too fast for effective channel reduction. For sweep delays of 1 second and higher, coloration of the respective channel regions was observed implying full transitions to electrochemical mode. Consequently further investigations will be focused on sweep delays of 1 second or higher. However, the observed coloration for architecture types A and B showed to be of non-uniform nature, as can be verified by the channel coloration in Annex Q or complementary in **Figure 3.11**.

This type of coloration would be less suited for a two-in-one solution (ECTFT as transistor and pixel) but still applicable in AM displays for cross-talk reduction. Finally, hysteresis effects were observed for all sweep delays due to inevitable intercalation of some ions into the WO_3 film, even for low sweep delays.

The initial study, to examine the fundamental working principle and the field-effect to electrochemical doping transition, already brought up some interesting features of the fabricated ECTFTs, foremost for the structures A and B. To begin with, hysteresis effects and subthreshold swings in the order of 0.22 to 0.78 $Vdec^{-1}$ and I_{ON}/I_{OFF} of 10^4 to 10^5 are common (see Annex S to Annex V). Secondly ON voltages were found to be dependent on the used sweep delay, giving rise to unpredictable switching between the ON and OFF state. The colorations were non-uniform throughout the channel and extended over the source electrode, complicating their use in display applications. Finally and most significantly, unstable drain currents, not only in the subthreshold regime but also in the ON state, were registered, due to leakage currents and electrochemical reactions in the WO_3 layer. These current drops can be critical for the use of this type of transistors in logic gates, as too high variations in the ON current could produce non-stable and even false outputs. However this does not apply for their use in display applications as the ON current does not play a critical factor. The overall performance gives the impression that architecture type A produces unsteady transistor characteristics, limiting its application to fields where switching speed, precise outputs or hysteresis effects are of minor importance. On the other hand architecture type B showed more stable drain currents, showing promises for selected electronic appliactions, such as biosensors.

As already mentioned beforehand in section 3.3.2, a new architecture type, namely type C, was developed and fabricated throughout this work in order to counteract some of the limitations mentioned for structures A and B. Therefore, the next chapter is dedicated to the examination of this new architecture and its comparison with the previous ones, based on the conducted static and dynamic characterizations.

3.3.4 Working Principle of Architecture Type C

It was found that most of the conventional architectures (A and B), and especially the ones with higher film thicknesses, present highly unstable and sometimes even negative drain currents (not visible, as I_D representation is in absolute values) in the subthreshold regime, and more specific in the interval prior to their respective ON voltages. Unstable currents could be associated to leakage currents, as the drain currents are following them until approximately V_G = -1 V (see **Figure 3.9**). However negative drain currents were solely observed after this gate voltage, but still in the subthreshold regime. It is assumed that the developed electric field from the EDL at the electrolyte/channel interface could be strong enough to pull electrons into the WO_3 film for reduction purposes or channel formation. When coloration is occurring at the drain end and the source is not capable of providing sufficient electrons for the EC reaction, it is possible that the drain electrode could, for a short amount of time, function as an electron source to sustain WO_3 reduction in the channel. This current was found to be in the order of nanoamperes. This overall behavior in the subthreshold regime, with negative or unstable outputs, could have impacts on the transistors application in electronic circuits. Not only these negative currents, but also the severe current drops during field-effect to electrochemical doping transition explained in sections 3.3.2 and 3.3.3, clearly show a deficit of electrons in the channel region during EC reaction. A possible method to avoid electron deficiencies and drain current fluctuations is to create a clearly defined potential in the channel region and a way to provide sufficient electrons for conduction and EC reaction. An electron channeling into the channel region is possible by integrating a fourth electrode behind the channel, resulting in architecture type C (see **Figure 2.1 C**).

The process involved in the electron channeling by architecture type C is simple and was found to be quite effective. The introduced fourth electrode is in direct electrical contact with the WO_3 layer, thus, if held at a negative voltage, capable of providing electrons in almost the entire extent of the channel region. So instead of having a reducing front, as it is the case for architecture type A and B, coloration occurs uniformly and solely throughout the whole channel (see inset **a)** in **Figure 3.7**). The applied voltage to this electrode hereafter denoted as BE voltage or V_B, directly influences the ion movement in the electrolyte, as they respond to the electric potential difference between the gate and the channel region ($V_{GB} = V_G - V_B$). Considering sweeping V_G from negative to positive, once V_{GB} inverts from negative to positive, that is V_G reaches the same voltage as V_B, the cations are suddenly attracted to the more negative back-electrode, where they start reducing the EC film. From this point on ($V_{GB} \geq 0$ V), further ion migration, from the gate to the channel region, takes place, turning it more conductive as the reduction process continues for consecutive higher gate voltages. In this context, it is worthwhile to consider that depending on the applied V_B it is possible to effectively control V_{ON} of the transistor, given the premise that this voltage denotes the point where ions start to migrate to the channel region. For the fabricated ECTFTs a negative V_B delivers best performances, as this enhances ion intercalation and at the same time provides electrons, creating a more stable environment, which is why, if not stated otherwise, the default voltage applied to the back-electrode

will be -1 V. However, for other EGTs positive values are also possible for positive ON voltages. With consecutive higher negative potentials applied to the back-electrode, V_{ON} shifts to more negative voltages. This way it is possible, depending on the applied V_B, to effectively change the transistors working mode (see **Figure 3.10 a**) from enhancement ($V_B > 0$ V) to depletion mode ($V_B < 0$ V).

This could bring great advantages, not only for pseudo-NMOS logic circuit architectures, where transistor sizing issues still persist,[128] but also for display applications, where AM displays composed of enhancement mode transistors are advantageous for a more stable performance and less cross-talk. Similar approaches to tune V_{ON} have been published,[129-131] however never with ECTFTs, providing a novelty in this area.

Several characteristics are observed for the depicted transfer curves in **Figure 3.10 a)**, where three distinct BE voltages were applied. To begin with it is evident that for more negative BE voltages earlier saturation is achieved, as the reduction process initiates earlier. Further, the drain currents present a comparable behavior, however with a certain offset in both states. Since the measured I_D current is not exactly the real electron current between source and drain, but more a contribution of several currents exiting the drain electrode, it is plausible that in this setup, with an additional BE, an offset in the measured I_D is created. This offset is due to the BE being an additional electron source, which, with higher negative voltages creates higher currents. So for the total I_D current one must consider a contribution of three distinct currents exiting the drain electrode:

$$I_D = I_{DS} + I_{DB} + I_{DG} \tag{3.4}$$

Here I_{DS} and I_{DB} are the effective electron currents deriving from the source and the BE, respectively (I_{DG} is the leakage current and negligible). Therefore one can observe, that in the OFF state, the three different drain currents vary over one order of magnitude from 2.25 nA to 75.89 nA for $V_B = 0$ V to $V_B = -2$ V, respectively. In transistor device modulation a current between source and drain can occur even with the transistor operating in the OFF state (for $V_G < V_{ON}$).[132] This current, also considered as part of the total leakage current, is known as subthreshold conduction and can, if not low enough, contribute to significant power consumption.[133]

This offset in the OFF state results from a substantial increase in subthreshold conduction between the back and the drain electrode. With higher difference in potential between the two of them, ranging from 1 to 3 V ($V_{DB} = V_D - V_B$, for $V_B = \{0; -1; -2\}$ and $V_D = 1$ V) higher subthreshold currents will arise. In the OFF state the EC film behaves as an insulator (oxidized state), however leakage currents still persist throughout the film and the channel length is a decisive factor. Shorter channels result in higher subthreshold conduction, which is one of the biggest problems in transistor miniaturization.[134] Analyzing **Figure 2.1** and complementary **Table 2.1** the distance between drain and back-electrode for this transistor (Ca2d1e1) amounts to 75 µm and the total channel length to 250 µm. Therefore the main I_{OFF} contributor is the subthreshold current deriving from the back-electrode.

As the conductivity of the EC film increases in the transition to the ON state a similar offset between the curves is observed, deriving from the same underlying process. Here I_{ON} also varies over one order of magnitude, reaching from 0.4 to 4.5 mA (see **Figure 3.10 a**).

Hysteresis was shown to increase with higher negative BE voltages. To explain this behavior one must consider two processes that take place. Firstly, higher negative BE voltages result in higher quantites of intercalated ions into the WO_3 as there is a stronger electrical field. This also means that to fully close the channel again more ions need to be deintercalated from the film for full oxidation. Secondly, besides needing a more negative gate voltage to extract the ions, a greater pull, deriving from a stronger electrical field, on the Li^+ is exerted, making them reside longer in the film. Observing **Figure 3.10 b)** the increased stability of this architecture compared to A or B becomes clear. Less I_{ON} fluctuation as well as V_{ON} shifts are observed. Additionally, very stable I_{OFF} currents and subthreshold behaviors with quite similar subthreshold slopes were observed with S_s ranging solely from 0.31 to 0.45 $Vdec^{-1}$; a tremendous improvement compared to A or B. Hysteresis effects are similar, however normal for ECTs and especially in this case as a longer channel provides more electro-reducible sites for WO_3 reduction.

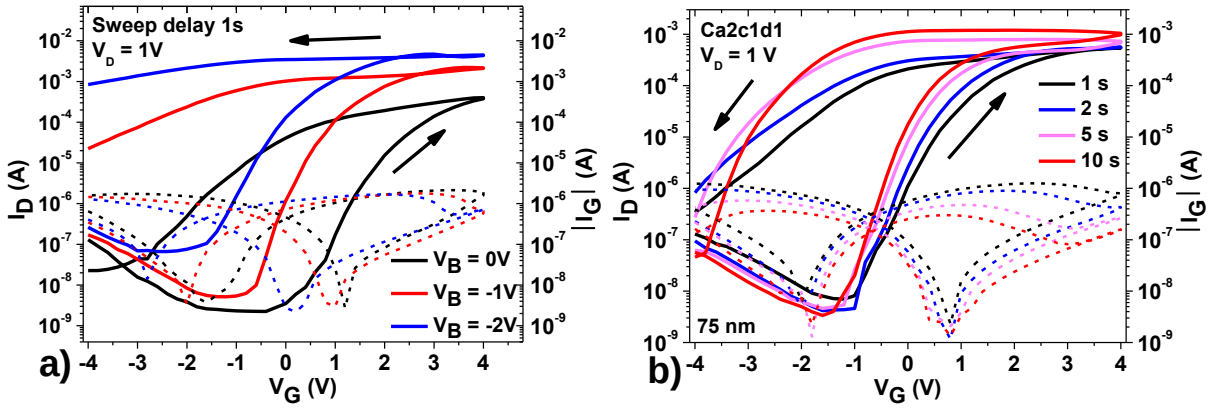

Figure 3.10 – Transfer curves of **a)** architecture Ca2c1d1 with 75 nm WO_3 with different back-electrode voltages applied. A shift of V_{ON} is observable as well as distinct ON and OFF currents and **b)** transfer curves for four different sweep delyas, evidencing increased stability. Continuous and dashed lines represent drain and leakage currents, respectively. The extracted characteristic parameters for **a)** and **b)** are summarized in Annex W and Annex X, respectively.

With the given insight into the underlying working principle it is now possible to directly compare all three architectures with each other, being one of the main concerns in the following section.

3.3.5 Comparison of Architecture Types

As seen beforehand the introduction of an electrode behind the channel region brings some great advantages. However to fully evaluate the resulting performance of the new architecture this section is concerned with a profound comparison between the three architecture types with titanium contacts that showed best performances individually (Aa1b2, Ba2b2 and Ca2c1d1). These best performing devices were determined in respect to static electrical characterization of each architecture with all of the possible permutations arising from Table 2.1. Their comparison with each other in this chapter is based upon their performances during static and dynamic electrical characterizations.

3.3.5.1 Static Electrical Characterization

The presence of the additional electron source for architecture C shows significant improvements in the pre V_{ON} regime, whereas architectures A and B possess irregularities in the drain current, with strong fluctuations and sometimes negative currents. Additionally V_{ON} showed to be less sensitive to sweep delay variations. Where for type A and B the ON voltage shifts up to 1 V (see **Figure 3.9**), type C shows a considerable improvement in V_{ON} stability, where maximum shifts as low as 0.4 V are possible (see **Figure 3.10 b**).

This improvement is due to a precise control of the ion movement in the electrolyte and a homogenous reduction of the channel region, rather than an evolving reduction front, as is the case for A and B. This is further evidenced by considering **Figure 3.11 a)**, where this advantage becomes visibly clear for the implementation of architecture C in display applications. The colored portion of the channel extends with a rather sharp contrast until the drain electrode, making it a possible candidate for a one-in-two (pixel and transistor) application. In comparison to architecture A, where ions are repelled from the drain electrode due to its positive potential, showing a gradual fade of coloration from source to drain. In addition there is ion accumulation in the source electrode region, leading to coloration of the above situated WO_3 (see **Figure 3.11 b**).

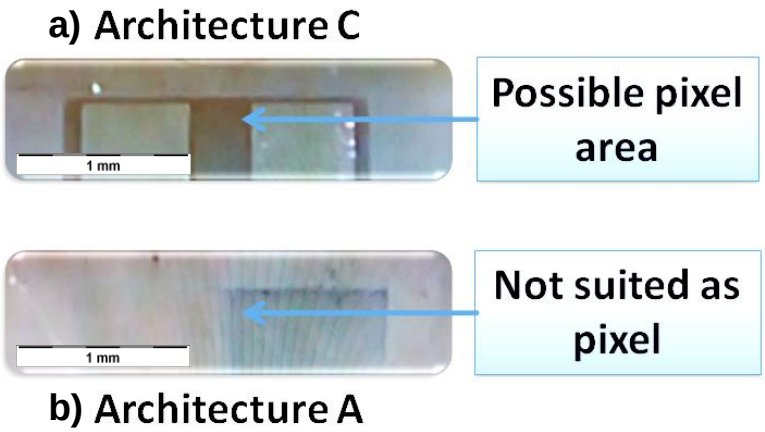

Figure 3.11 – Representation of the channel region of architecture C and A in the ON state for **a)** and **b)**, respectively.

There are, however, some drawbacks associated to the new architecture. As the inserted back-electrode occupies additional space between source and drain, the channel is consequently stretched. This might be advantageous for display applications, as it is possible to define the pixel size by the dimensions of the back-electrode. So the channel length can be assessed, depending on the desired pixel dimensions and resolutions. On the other hand, a longer channel implies also a higher channel resistance, which leads to disadvantages regarding electrical performance.

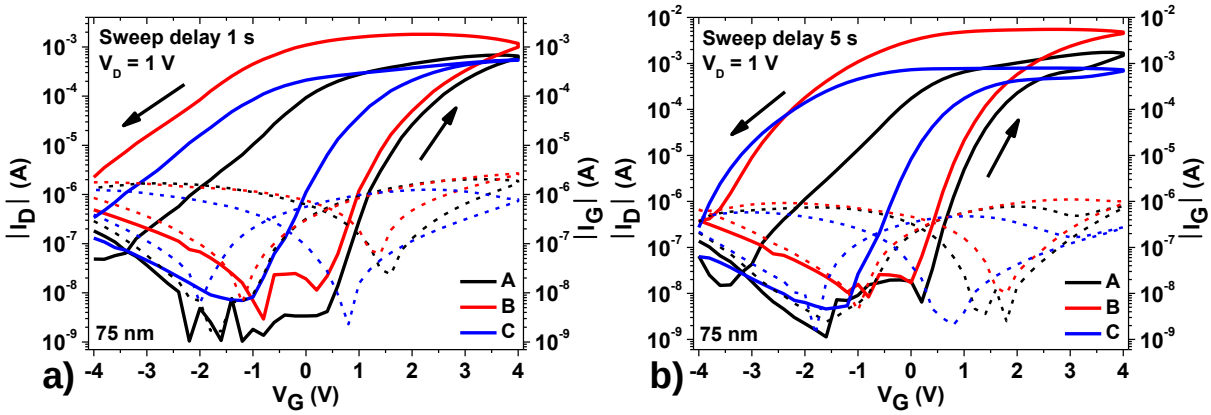

Figure 3.12 - Comparison of the three best performing architectures for **a)** 1 second and **b)** 5 seconds of sweep delay. Continuous and dashed lines represent drain and leakage currents, respectively.

As can be seen by **Figure 3.12** and complementary Table 3.1 a longer channel leads to lower ON currents and therefore diminished ON/OFF ratios. Furthermore, as an increased channel also signifies higher quantities of WO_3 to be reduced, a lower subthreshold slope is observed, leading to a slower transition between the ON and OFF state.

Table 3.1 – Extracted parameters of transfer curves from **Figure 3.12**, for 1 and 5 seconds of sweep delay, respectively.The respective curves can be accessed in Annex Y.

Architecture	V_{ON} (V)		S_s ($Vdec^{-1}$)		I_{ON}/I_{OFF}	
	1 s	5 s	1 s	5 s	1 s	5 s
A	0.40	0.20	0.30	0.25	$1.74x10^5$	$2.60x10^5$
B	0.20	0	0.31	0.28	$1.00x10^5$	$2.81x10^5$
C	-1.00	-1.20	0.43	0.35	$7.71x10^4$	$1.58x10^5$

For all sweep delays highest I_{ON} but also highest hysteresis was observed for architecture B. Being the interdigital structure it offers numerous pathways for electrons from source to drain. This behavior can be useful for biosensor applications as it is less sensitive to non-uniform channel reduction and gives a good response in terms of ON currents, reaching several milliamperes. Hysteresis effects for these applications might be less problematic, if for example it is a disposable single use device or if there is no need for fast cyclability.

Nowadays the mobility determination for ECTs still represents a difficult task and understanding the influences of the ions on the magnitude of the electron (or hole) conductivity remains an important area of research.[98] Some determine the closely related transconductance [135] others use standard transistor mobility equations [136] and most provide both,[29] so there seems to be not yet any real consens about which parameter should be considered. Consequently here, both parameters will be provided for better comparison purposes.

With an applied V_D of 1 V the ECTFTs operate in the linear regime, consequently the following equation to determine the electron mobility will be used:[137]

$$\mu_{lin} = \frac{L}{W}\frac{g_m}{C_i V_D} \tag{3.5}$$

where L and W denote the channel length and width, g_m is the transconductance, C_i is the capacitance of the dielectric, in this case the capacitance deriving from the EDL on the interface (C_{DL}), and V_D is the applied drain voltage. It is rather important to note that the values for C_i obtained by EIS, will merely give an approximation of the calculated channel mobility. This results from the fact that the double layer capacitance only influences charge mobility deriving from the field-effect of the EDL and does not take mobilities arising from effective electrochemical doping into account. Therefore in this case $\mu_{lin} = \mu_{FE}$. This approximation is however acceptable firstly, because there is not yet a reliable method nor is this process yet fully understood for an exact determination of the channel mobility in ECTs, as there are rather complex channel formation mechanisms invloved.

The transconductance on the other hand delivers a direct I_D response for a variance in V_G, representing a parameter with a more valuable physical background. It is defined by:

$$g_m = \frac{\Delta I_D}{\Delta V_G} = \frac{\partial I_D}{\partial V_G} \tag{3.6}$$

So simple differentiation of the transfer curves gives the transconductance for a specific ECTFT, whereas for the mobility, exhausting and not always trivial EIS need to be conducted. The following table (Table 3.2) shows the calculated mobilities and transconductances of the three best performing architectures. To calculate the mobility the respective channel dimensions for L can be accessed in Table 2.1, being equal to parameters a (architecture A and B) and c (architecture C). For architectures A and C the channel width W is equal to 3 mm and for architecture B, W amounts to 4.75 mm.

Table 3.2 – Extracted mobilities and transconductances of transfer curves from **Figure 3.12**, for 1 and 5 seconds of sweep delay, respectively. The respective curves for parameter g_m determination can be accessed in Annex Z.

Architecture	μ_{lin} ($cm^2V^{-1}s^{-1}$)		g_m (mS)	
	1s	5s	1s	5s
A	1.31	4.11	0.40	1.26
B	3.43	9.25	0.83	2.24
C	3.76 (0.38)	5.07 (0.51)	0.23	0.31

It is noteworthy that for architecture C the point of view and the considered values used in equation 3.5 have an impact on the calculated mobility. For instance one could argue that the effective channel length would be in fact the one between the back and the drain electrode (50 µm instead of 250 µm) and that V_D would be V_{DB} (2 V instead of 1 V). These values are included in Table 3.2 in brackets and show mobilities of one order of magnitude lower. Here again the transconductance shows no variation,

giving the real value with no space for interpretation. Consequently this will be the parameter of interest for comparison purposes with other ECTs from the literature. Once more it becomes evident that higher sweep delays produce increased performances, with higher transconductances and consequently higher mobilities as the channel conductivity increases with subsequent reduction.

Architecture A was subjected to a passivation step with PMMA, in order to compare electrolyte degradation with and without a passivation layer. Whereas ECTFTs without any passivation experienced rapid electrolyte degradation, showing no response whatsoever after 24 h, the encapsulated transistor still evidenced some current modulation after that time. In **Figure 3.13** micrographs of the channel regions show two distinct ECTFTs without (**Figure 3.13 a**) and with (**Figure 3.13 b**) a PMMA passivation layer.

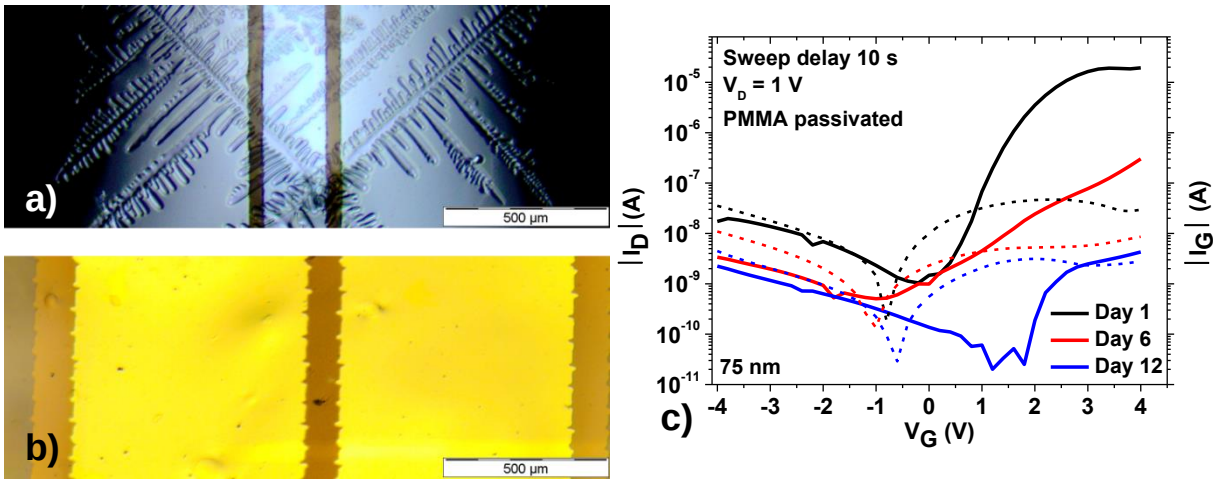

Figure 3.13 – Micrographs of channel region without **a)** and with **b)** PMMA passivation layer. In **c)** the associated transfer curves for encapsulated architecture Aa1b1 are visible after 1, 6 and 12 days of encapsulation. Continuous and dashed lines represent drain and leakage currents, respectively. The extracted characteristic parameters for **c)** are summarized in Annex AA.

Both micrographs were taken after static electrical characterization. The electrolyte in **Figure 3.13 a)** shows severe crystallization, which can also be associated to impurities on the WO_3 surface. This hinders effective ion transport to the channel region, resulting in less current modulation and channel coloration. After solely one day not even a current ratio of one order of magnitude was achievable. With encapsulation however the electrolyte experienced no crystallization (as seen in **Figure 3.13 b**) and the ECTFT was able to maintain some current modulation. But, observing the transfer curves in **Figure 3.13 c)** it is evident that even with a passivation layer the transistor eventually looses its capability of current modulation. I_{ON} degrades over time, falling from 1.94×10^{-5} to 4.29×10^{-8}. Additionally, V_{ON} experiences a shift of up to 2 V, leading to highly unpredictable transistor characteristics. In terms of channel coloration no decisive observations could be made as the WO_3 was deposited on Ti contacts, which made any evaluation difficult. This could be once again determined by *in-situ* absorbtion spectroscopy, as already suggested beforehand.

The obtained results for static characterization show pros and cons for all three architectures, which would dictate their possible field of application. Despite unstable drain currents in the OFF state and V_{ON} shifts, the obtained parameters from Table 3.1 suggest a slight edge for architecture A, yielding better performances throughout the investigation. Not considering the stability issues mentioned beforehand. Although presenting strong hysteresis effects, architecture B shows high drain currents in the ON state, exceptional mobilities and transconductances and subthreshold slopes comparable to A. Architecture C is in disadvantage regarding electrical parameters, but compensates with stable ON voltages and drain currents in the OFF state and a tunable ON voltage, enabling normally-OFF to normally-ON transitions, advantageous for display applications. Moreover C shows channel coloration of a highly uniform nature. It is further expected that for this architecture hysteresis effects could be diminished by inverting V_B from negative to positive when closing the channel, effectively pushing the ions out of the channel region. Even though this results in higher power dissipation the switching speed could be increased dramatically.

The obtained results for the three best performing architectures showed similar behavior, however with slightly distinct parameters. Regarding static characterization ON/OFF ratios in the order of 10^4 -

10^5 were measured. These values are satisfactory as compared to other inorganic EGTs and ECTs such as 10^5 for a ZnO transistor by Bong *et al.* [138] or an ambipolar Bi_2Te_3 transistor with a 10^3 ON/OFF ratio by Yuan *et al.*[139] Nevertheless it is noteworthy that pure EGTs normally possess a non-3D channel and ON and OFF currents are usually lower.

The determined carrier mobilities, which lay in the order of up to 9.25 $cm^2V^{-1}s^{-1}$ (interdigital), are equivalent to existing similar devices. For instance the ZnO EGT by Bong *et al.* with a mobility as high as 13 $cm^2V^{-1}s^{-1}$, but surpassing other inorganic EGTs, such as an ambipolar PbSe nanocrystal thin-film transistors from Kang *et al.* [140] or a nanoink ITO droplet TFT by Dasgupta *et al.* [84] by up to one order of magnitude. However and as mentioned before, these mobilities are calculated on behalf of the field-effect imposed by C_{DL}, which is only partly true for the present ECTFTs, turning this comparison fairly far-fetched. Furthermore different deposition techniques of the inorganic semiconductor yield different performances.

Therefore the most suited comparison to existing devices is based on the calculated transconductance, which lays in the order of up to 2.24 mS. A pH-Sensitive WO_3-Based Microelectrochemical Transistors by Natan *et al.*,[44] with similar characteristics and a transconductance by gate width of 12 $mSmm^{-1}$ can be used for comparison purposes. Dividing the obtained value by the channel width (4.75 mm) yields a transconductance by gate width of 0.47 $mSmm^{-1}$, showing a value of two orders of magnitude lower than the one indicated in the literature. The discrepancy between the two values can be associated to a number of factors, such as experimental setup, used electrolyte and film thickness.

Encapsulated ECTFTs showed current modulation even after a few days, whereas no encapsulated transistors lost this capability completely. The study about encapsulation using PMMA or other organic coatings leaves a wide field of possible research as only a few of the transistors were investigated in regard to this topic. Especially a study on the coloration abilities could turn up some interesting results.

The next section will assess the transistors' performances during dynamic characterization, which helps to make conclusions regarding their behavior under a commuting gate voltage and their rapidity to adapt to these stimuli.

3.3.5.2 Dynamic Electrical Characterization

Dynamic characterizations not only serve to test the transistors stability over a certain time interval but also to determine cut-off frequencies and their response time to certain frequencies. Therefore dynamic electrical characterizations were conducted with the best performing architectures (Aa1b2, Ba2b2 and Ca2c1d1) in order to assess their performance when subjected to an alternating V_G at different frequencies.

Architectures A and B were found to reach a stable dynamic behavior after a few cycles for the investigated frequencies, suggesting constant characteristics until electrolyte degradation eventually starts to have influences on the transistors' responses. In contrast to architecture C, where for higher frequencies the transistor started to show a somewhat peculiar behavior. As can be observed in **Figure 3.14 a)** and complementary Annex BB the transistor experiences a continuous degradation of ON/OFF ratio for higher frequencies. With V_B = -1 V, frequencies above 0.1 Hz seem to deliver insufficient time to fully extract the ions from the WO_3. So with every cycle, more and more ions accumulate in the channel region, leading to a continuous charge build-up. This leads to progressively higher channel conductivities especially in the OFF state. ON currents showed stable values after a few cycles but OFF currents were observed to continuously rise, which lead to ever smaller ON/OFF ratios, eventually leaving the transistor fully ON. Given this scenario the transistor would be deemed useless above these frequencies. Surprisingly there is a simple yet effective solution to this problem. The capability of the BE to hold the ions in the film during the negative gate voltage part of the cycle can be overcome by simply applying an asymmetric gate voltage of 4 and -6 V. This way it is possible not only to rise but also to stabilize the ON/OFF ratios for higher frequencies (see **Figure 3.14 b**)

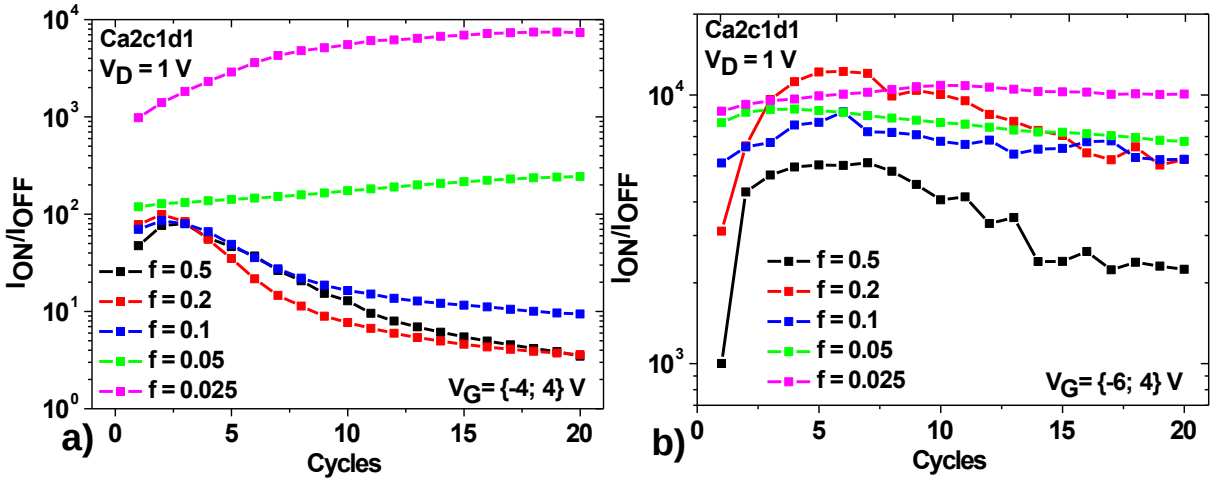

Figure 3.14 – I_{ON}/I_{OFF} versus cycles for different frequencies. With **a)** symmetric gate voltages of -4 and 4 V and **b)** asymmetric gate voltages of -6 and 4 V. For high frequencies a pronounced degradation of ON/OFF ratio for **a)** is observed due to charge built-up in the channel, whereas for **b)** more stable and higher ON/OFF ratios were measured.

This development can be verified by comparing **Figure 3.15 a)** with **b)**, which emphasizes the impact of asymmetric gate voltages, especially for architecture C, where an increase of ON/OFF ratio of up to 4 orders of magnitude is achieved. What showed to have an exceptional positive impact for architecture C was found to be of disadvantage for architectures A and B. A considerable loss of ON/OFF ratio was observed for these devices as the gate voltage nature was switched from symmetric to asymmetric (see **Figure 3.15 b**). Hence these devices would not need an asymmetric gate voltage in order to reach best performance, which is a great advantage, as higher voltages also always imply higher power dissipations. The cut-off frequencies (f_{co}) can be found at the point where the current gain (I_{ON}/I_{OFF}) reaches unity. In **Figure 3.15** it is observable how, with increasing frequencies, the current gains are approximating to unity (10^0), but still situated above this specific current gain, showing still some room for further increase in the working frequencies. It is however expected for the ON/OFF ratios to quickly converge to unity current gain, most likely for frequencies situated below 10 Hz.

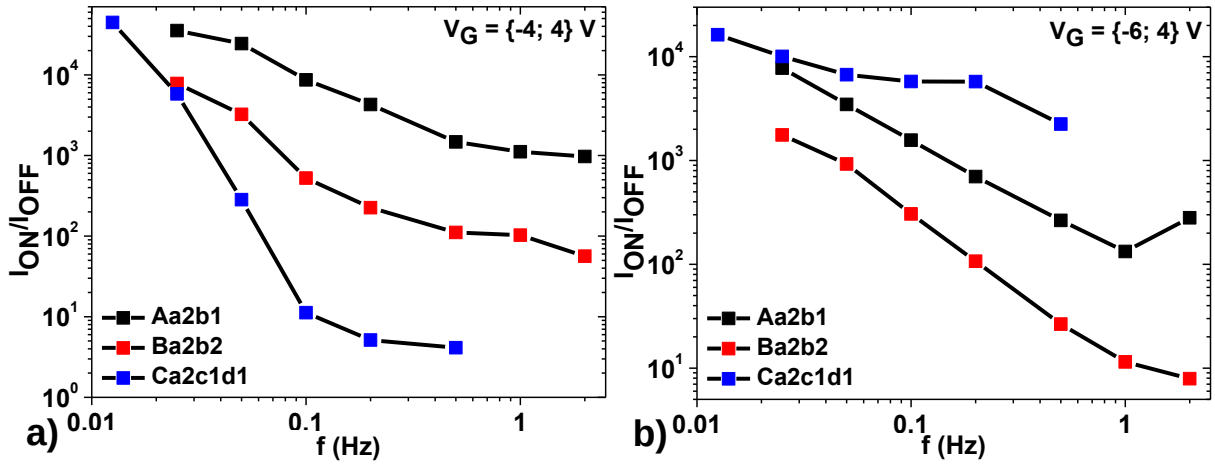

Figure 3.15 – Comparison between the three architectures regarding their ON/OFF ratios for different frequencies. With **a)** showing results for symmetric **b)** for asymmetric gate voltages.

Figure 3.16 a) and **b)** each shows one full cycle for two different frequencies (0.05 and 0.025 Hz) and symmetric gate voltages. It becomes apparent, by observing the behavior of architecture C that even for these relatively low frequencies a stable OFF current cannot be reached, which additionally varies over one order of magnitude moving from 0.05 to 0.025 Hz. This in turn is not observed for architectures A and B that show stabilization and even a slight increase in I_D after reaching a minimum (see black and red curve of **b)** in **Figure 3.16**). Nevertheless architecture C possesses a much quicker ability to transit to the ON state compared to the other two devices. This evidences the accelerated ion

movement to the channel region due to the negative V_B, which however, also plays a decisive role during the charging process described above. Remarkably for the lowest frequency of 0.025 Hz the transition to the ON state for architecture C seems to be almost instantaneous with I_D commuting rapidly between 10^{-7} and 10^{-3} A, whereas the drain currents for the other architectures show a slow and gradual transition. For asymmetric gate voltages (**Figure 3.16 c)** and **d**) all three curves reach a stable I_D in the OFF state with architecture C showing lowest I_{OFF}, advantegous for low power dissipation.

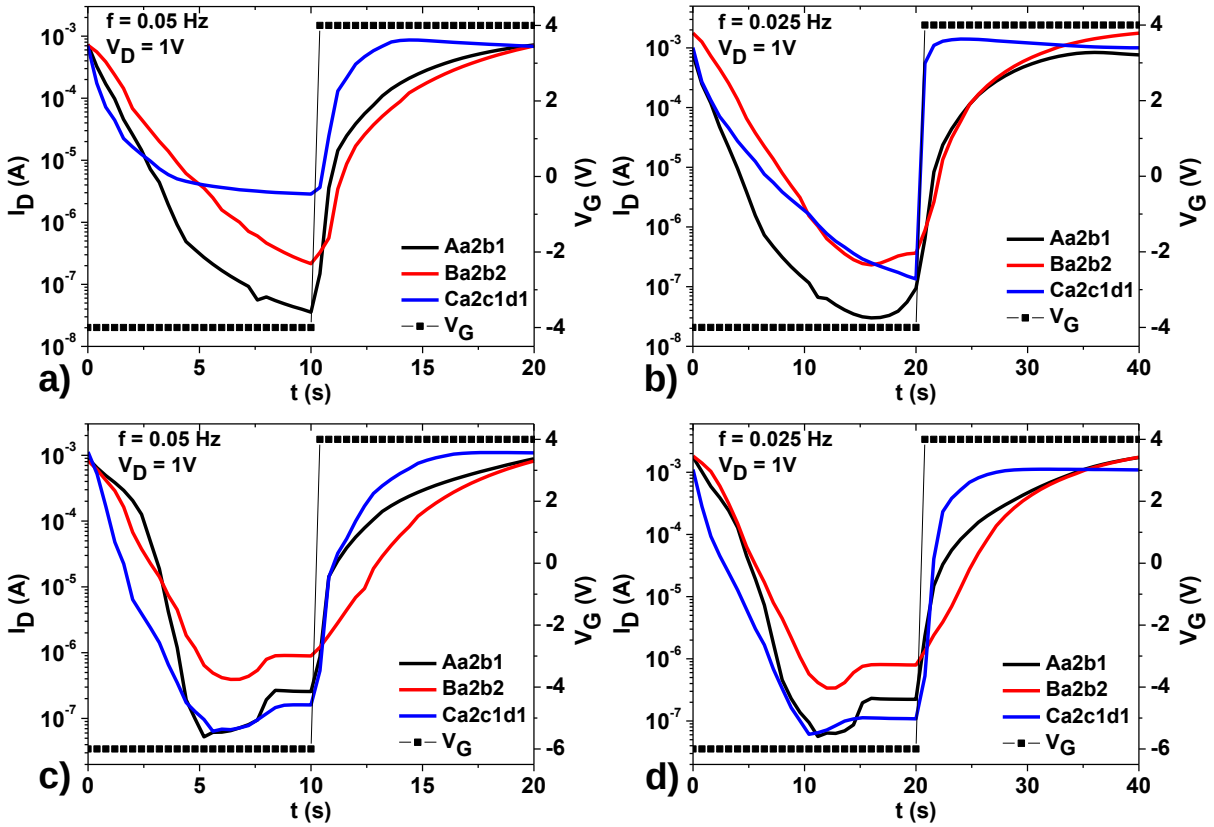

Figure 3.16 – One cycle for each architecture for **a)** 0.05 Hz and **b)** 0.025 Hz with symmetric and **c)** and **d)** with asymmetric gate voltages.

The static and dynamic characterizations for architecture C were carried out with a constant back-electrode voltage held at V_B = -1 V. However, it might be reasonable to attempt static and dynamic characterization with variable back-electrode voltages. To facilitate ion migration in and out of the film, the BE voltage can be inverted from -1 to 1 V when inverting the gate voltage from 4 to -4 V. The resulting increased difference in potential for each half cycle leads to an enhanced ion movement. Consequently the channel would open and close more rapidly and asymmetric gate voltage would become redundant.

The final step was the fabrication and characterization of fully transparent ECTFTs on a flexible substrate (PEN), using IZO instead of Ti as electrode material. The next section is therefore destined to evaluate their static electrical characterization under normal conditions as well as under mechanical stress (curvature).

3.3.6 Towards Fully Transparent and Flexible ECTFTs

The main objective of this work was successful as completely transparent, flexible and functional ECTFTs were obtained. The transistors were characterized by optical microscopy and static electrical characterization before and after delamination of the PEN substrate from the silicon wafer support. This served for an evaluation of possible mechanical stress that could have damaged the deposited thin-films during delamination. However, as both, the IZO and the WO_3 films are of amorphous nature, they seem to be able to adapt to the internal stress during delamination and no danification was observed visually (see **Figure 3.17 a)** and **b**). Nevertheless, the individual electrical characterizations showed slightly different behaviors (Annex CC). With a sweep delay of 5 seconds similar subthreshold swings, ON voltages and transconductances were observed, for ECTFTs before and after

delamination (PEN on Wafer and PEN). When comparing to ECTFTs deposited on glass with Ti contacts, ECTFTs on PEN show in some cases better (S_s) but in other worse (g_m) performances (compare Table 3.1 with the Table from Annex CC). However, in terms of ON/OFF ratio a drastic decrease after delamination was observed, with a difference of one order of magnitude from $6.13x10^4$ to $6.92x10^3$ (see Table from Annex CC). These fluctuations and a low transconductance are however not problematic as the main interest is focused on the coloration ability of the channel during imposed mechanical stress. To determine influences deriving from mechanical deformation (convex bending), transfer curves solely of delaminated PEN were considered for subsequent stress tests with different iron support curvatures.

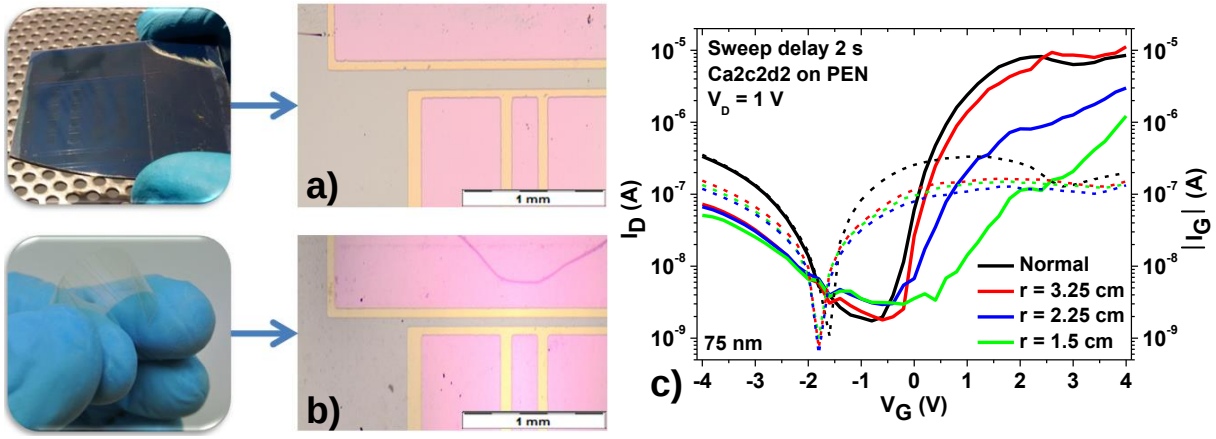

Figure 3.17 – Images and micrographs of ECTFTs with IZO electrodes on PEN substrate before and and after delamination from the silicon wafer support, **a)** and **b)** respectively. The artifact on the gate electrode in micrograph **b)** is not part of the film and did not influence the electrical characterization. **c)** Shows the associated transfer curves from one of the ECTFTs (Ca2c2d2) from the delaminated substrate of **b)** with different curvatures.

Observing **Figure 3.17 c)** the transfer curves without any mechanical stress showed relatively good electrical modulation with an ON/OFF ratio of $4.89x10^3$. Of course, this value is not as high as for the same architecture with a smaller channel length (Ca2c1d1), as channel resistivity is increased. A continuous decrease in subthreshold slope and consequently lower ON/OFF ratios are observed when increasing the internal mechanical stress, that is increasing curvatures with lower iron support radi ($\kappa = 1/r$). As the ON current is merely in the order of µA and the channel width is slightly increased, all three curves evidence the field-effect to electrochemical doping transistion at about V_G = 1.9 V. This also indicates effective channel coloration, which was observed for all three curvatures during charcaterization. Furthermore normal mechanical conditions present a smooth curve with continuous currents (see black curve in **Figure 3.17 c**); this seems to worsen as substrate bending is increased, producing somewhat unsteady drain currents (see red, blue and green curves in **Figure 3.17 c**).

The amorphous nature of the deposited films on PEN showed a good compensation of the stress concentration during delamination, preventing complete device failure. The differences in electrical performances of the ECTFTs before and after delamination are even favorable, with lower drain currents for the delaminated ECTFTs, good for lower power consumption. The unsteady drain currents and decreased electrical performances can be associated to stretched or dangling bonds within the WO_3 or IZO matrix difficulting electron conduction.[141] As a consequence thereof the switching speed for ECTFTs under mechanical stress is expected to be lower. Even with increased bending, channel colorations were verified to be still of good quality, presenting advantages towards practical applications in flexible display electronics.

4.CONCLUSIONS AND FUTURE PERSPECTIVES

The present work was centered on the fabrication, characterization and improvement of TFTs based on the EC material WO_3, in order to obtain devices with double functionality (optical and electrical modulation). The work was in fact successful and the final objective, which consisted of the fabrication of a completely transparent ECTFT on flexible substrate, was achieved. Apart from two existing architectures (A - conventional and B – interdigital approach), a new transistor architecture (C – back-electrode) was designed and implemented, consisting of a modification of architecture A by adding an additional electrode behind the channel. The developed ECTFTs and their EC films were mainly characterized in respect to their optical, electrochemical and electrical properties. This final chapter is therefore focused on giving some final remarks about the work as well as some perspectives for possible future investigations on this specific topic.

4.1 Final Conclusions

The used fabrication techniques, such as patterning (lithography and lift-off), layer deposition (sputtering and electron-beam) and drop casting proved to be of a relatively straight forward nature and perfectly suited for these devices, which are based on a layered and planar configuration. Nonetheless it would be preferable to distance oneself from sophisticated high-cost thin-film deposition techniques like sputtering that still involve undesired process parameters like vacuum or plasma and try to focus on low-cost alternatives like screen or inkjet-printing with solution based EC materials.

Regarding the deposited EC films no annealing was carried out leading to a purely amorphous WO_3 film with good ion permeability. The main investigated property of the EC films was the film thickness. Being merely an extrinsic property of the EC material, it showed a strong influence on EC reaction kinetics and achieved optical density and color efficiency. Thinner films exhibited shorter coloration and bleaching times (t_c and t_b of 1.8 and 3.8), on the other hand however lower ΔOD and CE (0.26 and 21.85 cm^2C^{-1}, respectively), showing less appealing colorations.

Using EIS measurements an estimation of the lithium-based polymer electrolyte's electrical parameters was conducted, showing comparable results with existing research on the same electrolyte. Modifying and improving the existing ECM 1 (simplified Randels cell) to ECM 2 and analyzing its respective fitting made it possible to determine the capacitance due to EDL as C_{DL} = 5.10 μFcm^{-2} and the electrolyte's ionic conductivity amounting to $2.29x10^{-5}$ Scm^{-1}. The determination of these parameters was vital before entering ECTFT characterization as the electrolyte constitutes the dielectric layer of the transistors and plays a crucial role in the devices' performance.

It was possible to link the obtained results from electro-optical and electrochemical characterizations to the static and dynamic electrical characterizations, especially for the interpretation of the underlying process during field-effect to electrochemical doping transition. Regarding this transition it is highly recommended to further investigate into this direction with *in-situ* optical spectroscopy during static electrical characterization. This would give insight into channel coloration during ON to OFF transitions for a better understanding of the involved phenomena.

Architectures A and B produced good but somewhat unpredictable transfer curves, where process parameters like the sweep delay showed to have a strong impact on properties like V_{ON}, S, I_{ON} and hysteresis. Moreover the channel region coloration of these architectures in the ON state was of non-uniform nature, making their application in displays as a pixel problematic. However they are still suitable for applications, where unsteady electrical characteristics are no problem; for instance in selected biosensors applications. Architecture C on the other hand produced stable transfer curves for different sweep delays, in terms of absolute parameters values even with a longer channel almost matching electrical characteristics observed for the two former architectures. The implementation of a fourth electrode behind the channel is promising as it brings advantages like uniform channel coloration and adjustable V_{ON} (possible normally-ON to normally-OFF transitions) due to improved ionic movement control in the channel. The improved channel coloration is favorable for their possible application in displays as a two-in-one (pixel + transistor) solution. The positive side-effect of an adjustable V_{ON} brings advantages regarding cross-talk issues, which could be reduced owing to a greater security margin in an enhancement working mode transistor. The downside however is associated to increased power dissipation due to extra voltages that need to be applied.

Overall for the static electrical characterization architecture B produced unstable (sweep delay dependent) however best characteristics with an I_{ON}/I_{OFF} of $2.81x10^5$ and a transconductance of 2.24 mS. Surprisingly when moving to flexible substrates architecture Ca2c2d2 on delaminated PEN substrate showed a remarkable subthreshold swing of S_s = 0.18 $Vdec^{-1}$ however lower ION/IOFF of $6.92x10^3$. Regarding dynamic electrical characterization a continuous charge built up in the channel with symmetric gate voltages for architecture C was observed, which however was easily counteracted with asymmetric gate voltages between -6 and 4 V. With this process condition, architecture C showed best performances with almost instantaneous transition from the OFF to the ON state, lowest I_{OFF} in the order of 10^{-7} A and highest ON/OFF ratios for the investigated frequency range.

4.2 Future Perspectives

As was seen throughout this work the area of ECTFTs still presents a novelty with only a handful of implemented applications. Consequently when thinking about possible future projects for this specific area several aspects come to mind worth taking into consideration.

Firstly architectures A and B on PEN were not investigated as only the new architecture (C), which showed incredible channel coloration and characteristics stability, was implemented on a flexible substrate in order to investigate its integration into flexible and transparent display applications as a two-in-one solution. The two former architectures however showed promises during static characterization and therefore an extended study of these two architectures on PEN is highly recommended. Furthermore, and this regards all implemented ECTFTs, a more profound study of passivation and encapsulation methods (vertical structure with gate electrode over channel) and their influence on the static and dynamic electrical behavior as well as coloration should be undertaken as it is expected to bring increased performances and better device stability and durability. Another field of research would be the integration of anodic EC materials, such as NiO (p-type), to achieve enhanced colorations or even CMOS architectures. Additionally and already stated before, the field-effect to electrochemical doping transition still presents a poorly understood field and unfortunately most conclusions are based on assumptions. A method to further explore this field would be the integration of an *in-situ* absorption spectroscopy during electrical characterization. This could be used to indirectly quantify charge carrier concentration in the WO_3 layer for colored and bleached states as well as injected ions from the electrolyte into the semiconductor as a function of the gate voltage.

Electrochemical characterization evidenced rather slow transitions between the colored and the bleached state, even for the thinnest WO_3 film under investigation (75 nm), laying in the order of seconds. The use of a nanostructured WO_3 layer surface could lead to a drastic decrease in response time, owing to an increased contact area between electrolyte and WO_3 film. This could have considerable impact on both the optical and the electrical response of the device, facilitating aspects like ion diffusion and electron conduction.

Last but not least the electrolyte represents an important factor for the devices' proper performances and should receive further attention in future projects. An extended study is recommended on parameters like its adherence to the used thin-films (WO_3, Ti, IZO), wettability properties or arising discrepancies during drop-casting. EIS measurements of the electrolyte showed promising results and ECM fittings, yet the underlying fundamentals for CPEs are not well explored and still present a wide area for future research. For instance the integration of a Warburg-impedance in the proposed ECM in combination with an electrochemical cell composed of WO_3 layers could lead to further insight into diffusion properties and also a more profound understanding of the field-effect to electrochemical doping transition. Furthermore, emerging technologies like microfluidics for the used electrolyte could present themselves as useful aspects to be explored, in order to improve device performances or open paths to enhanced device encapsulation and passivation methods.

All in all the present work shows a complete and successful way from designing and developing a new transistor architecture for an exciting emerging technology, leaving also space for future fields of research. The process went through design, fabrication, characterization and understanding, until an implementation into a possible field of application. This last step was recently confirmed by a running project in CENIMAT | I3N, where an EC display based on an active 8x8 matrix, consisting of EC pixels and transistors of the new architecture type C, was developed (Annex DD). With the right focus and dedication this technology could reach the open market within a few years with applications ranging from biosensors to transparent and flexible displays.

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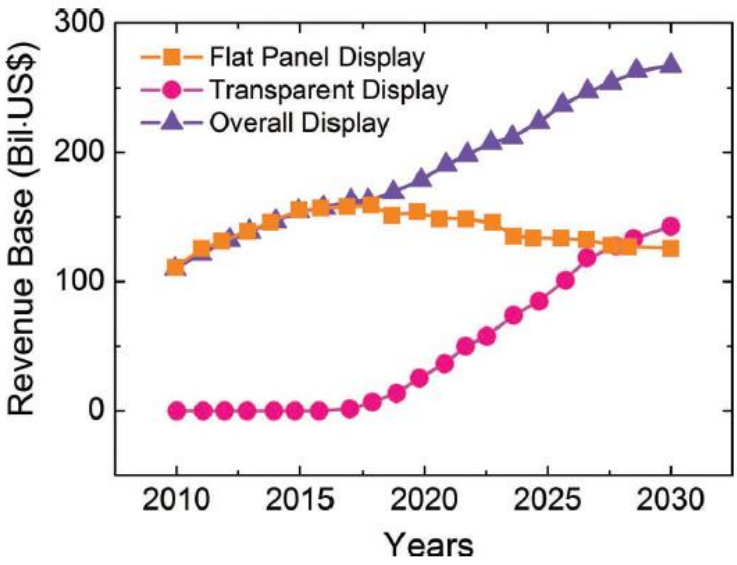
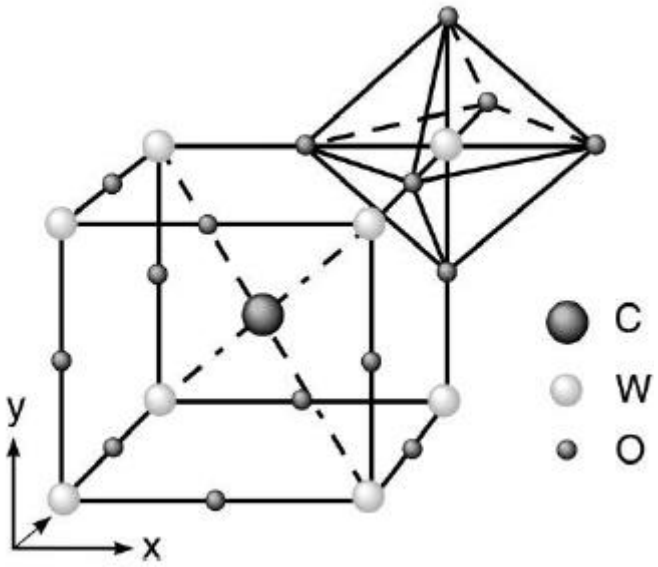
6.ANNEX

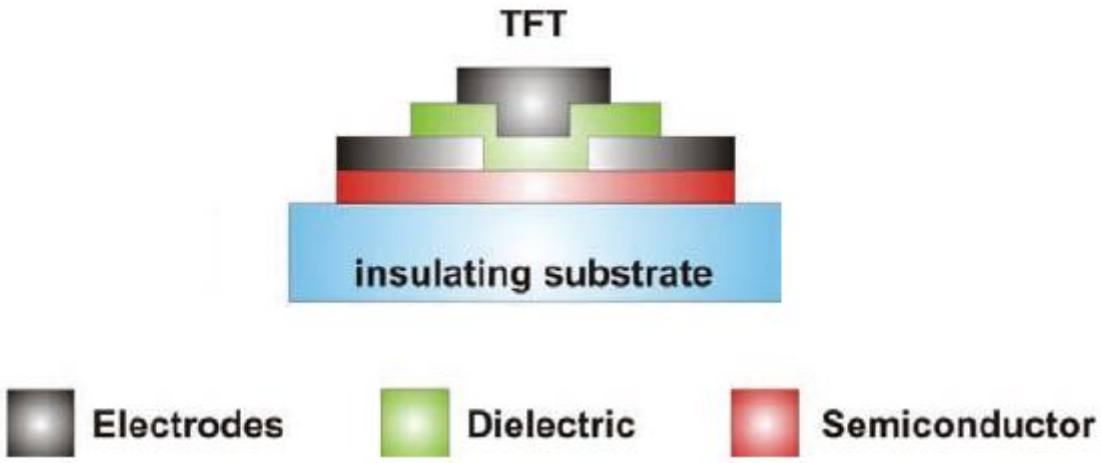
Annex A – Gross market revenue of FPDs, Transparent displyas and overall displays until the year 2030, predicted by Displaybank in 2011.



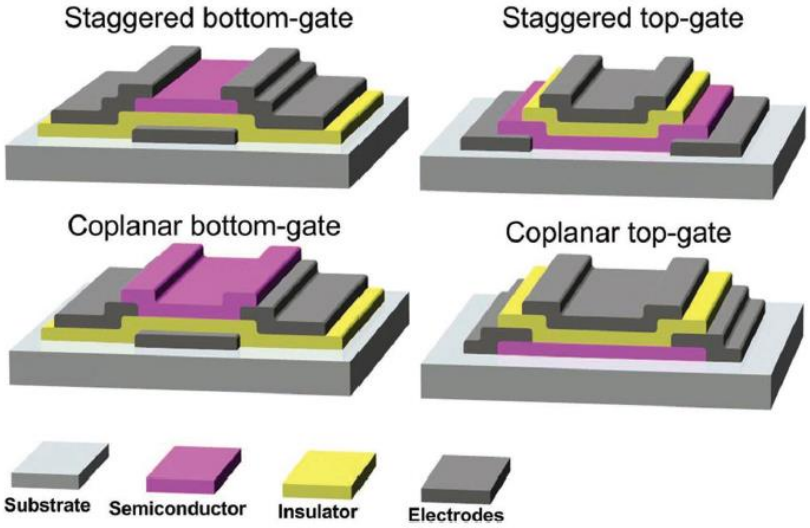
Annex B – Unit cell of tungsten trioxide perovskite defect structure with W and O representing tungsten and oxygen atoms and C showing the position of the intersticial space for ion intercalation.[142]



Annex C – Common TFT device structure in an coplanar top gate architecture. Adapted from [143].



Annex D - Schematic presentation of the four most common TFT architectures with material identification. Adapted from [85].



Annex E – Working principle and essential equations for a field-effect transistor. Adapted from [144].

The term field-effect refers to the I_D current modulation by an electrical field V_G as described above. The electric field directly influences the shape and therefore the conductivity of the channel between source and drain. In the case of the widely used metal-oxide-semiconductor field-effect transistor (MOSFET) this channel region relies on inversion, a process, where minority carriers accumulate close to the dielectric/semiconductor interface to form the channel. However, in the case of a TFT charge accumulation rather than inversion is responsible for the channel formation. For the case of an n-type semiconductor the applied gate voltage must be positive in order to accumulate electrons in the channel region, reversibly a p-type semiconductor requires a negative gate voltage to function in its ON state.

If a small yet sufficient gate voltage to accumulate enough charges for channel formation, also denoted as threshold voltage (V_t), is applied, an I_D current can flow between the source and drain contacts.

With a small V_D applied, the channel is approximately uniform and the transistor responds with a linear ohmic behavior (**Figure E.1 b**). As the channel depth depends on the voltage drop (relative to the source) across the channel, which decreases from V_G at the source end to $V_G - V_D$ at the drain end, it is evident, that for gradually increased V_D the channel takes a tapered shape, being deepest at the source and shallowest at the drain end. This results in an increase in resistance along the channel,

thus bending the I_D curve for higher V_D (**Figure E.1 b**). As long as $V_D < V_G - V_T$ the i_D curve is in the triode or linear region and can be described by:

$$I_D = C_i \mu_{FE} \frac{W}{L} \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right] \quad \text{(E.1)}$$

Where C_i is the dielectric capacitance per unit area, μ_{FE} the field effect mobility and W and L are the channel width and length, respectively. For sufficiently low V_D the quadratic term can be neglected, making it the linear relation (ohmic) between I_D and V_D, as explained before.

For increasingly higher V_D the channel depth at the drain end decreases, increasing the total channel resistance, which is evidenced by a bending of the I_D output curve when approximating $V_{DS\ sat}$ (**Figure E.1 b**). For $V_D = V_{Dsat} = V_G - V_T$ the channel depth reduces to zero and eventually pinches-off as can be observed in **Figure E.1 a)**. Increase in V_{DS} after the channel pinched-off has little or no effect on the I_D current (constant I_D in the saturation region). From this point on (for $V_D \geq V_G - V_T$) the transistor operates in the saturation or pinch-off regime and the drain current is described by:

$$I_D = C_i \mu_{sat} \frac{W}{2L} (V_G - V_T)^2 \quad \text{(E.2)}$$

where μ_{sat} represents the carrier mobility in the saturation regime.

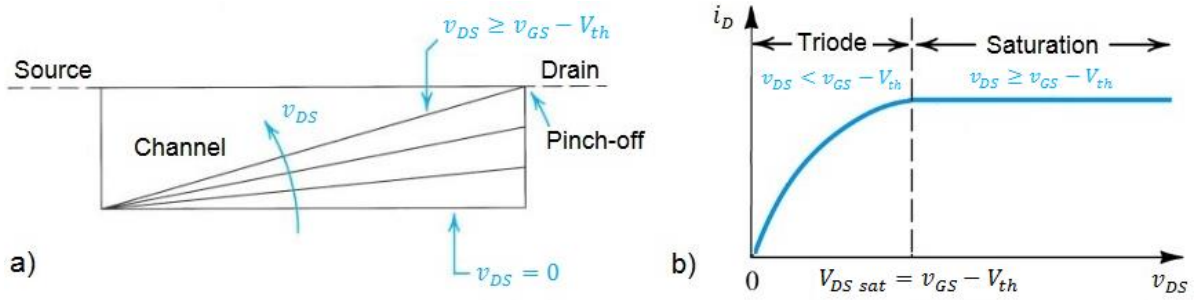


Figure E.1 – **a)** Channel shape and influence of applied drain voltage; (b) I_D current in function of applied drain voltage with regime indication; for both schematics $V_G > V_{ON}$ is fulfilled.

However, increasing V_G will attract more and more charge carriers to the channel resulting in progressively higher pinch-off voltages and consequently higher drain currents. This behavior is best described by the output **a)** and transfer **b)** characteristic curves (CCs) of a TFT (**Figure E.2**).

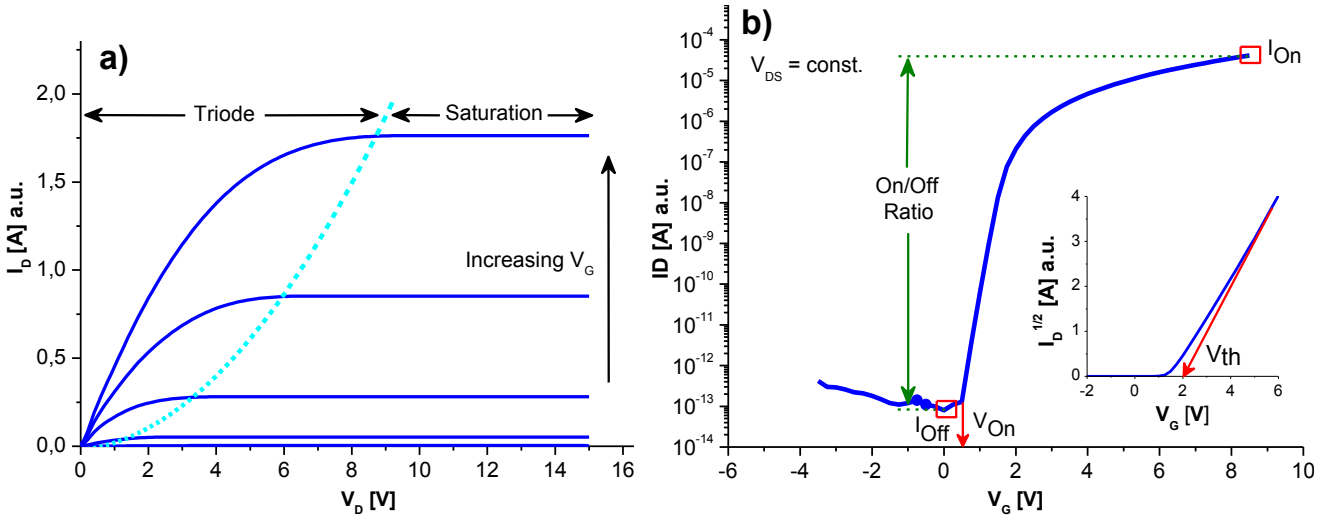
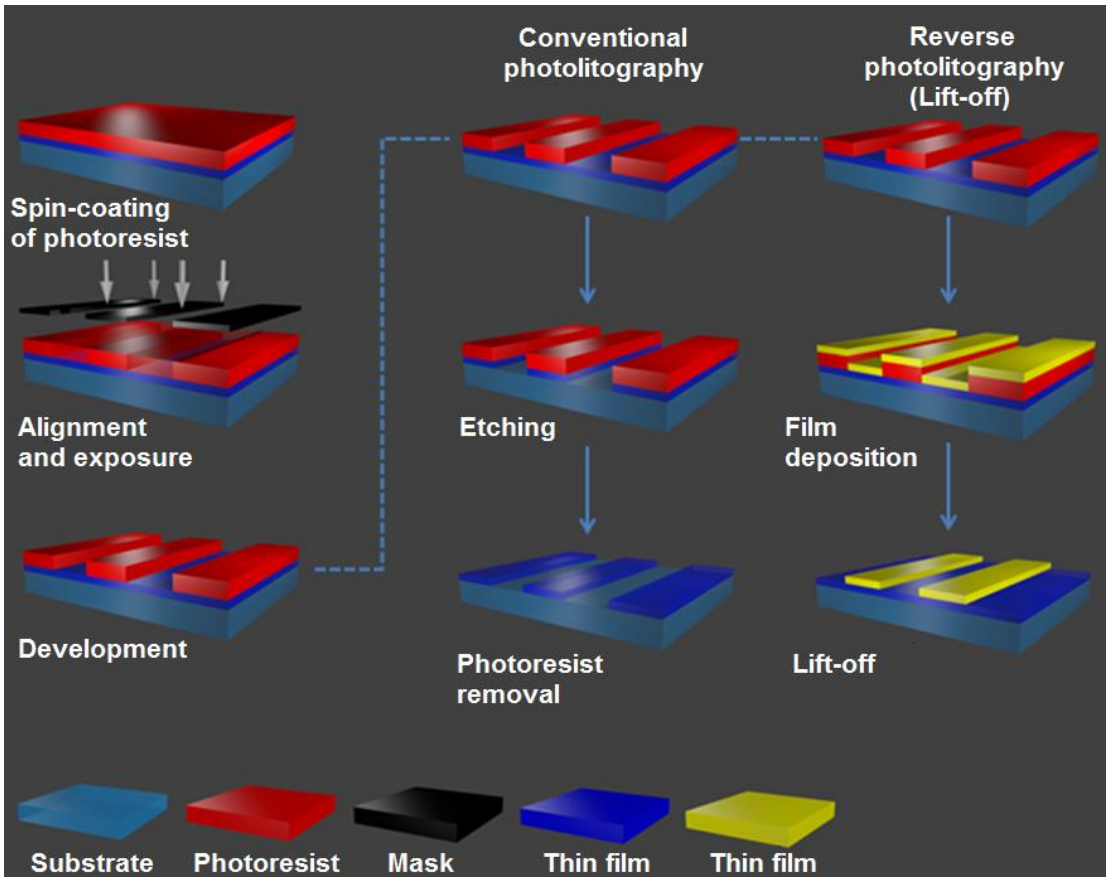


Figure E.2 – CC curves of a conventional FET. With **a)** showing the output characteristics and **b)** the transfer characteristics (obtained for $V_{DS} >> V_{DSsat}$). Some specific parameters, such as I_{ON}, I_{OFF}, ON/OFF ratio, V_{ON} and V_T, are indicated.

Thin-film transistors are evaluated based on these CCs, which are obtained by sweeping either V_D (output) or V_G (transfer) and measuring the drain current, and their respective characteristic parameters. Different application fields require distinct parameters and are not always confined to a certain performance, such as TFTs for PM or AM in displays. The ECTFTs in this were evaluated using the transfer curves depicted in **Figure E.2 b)**.

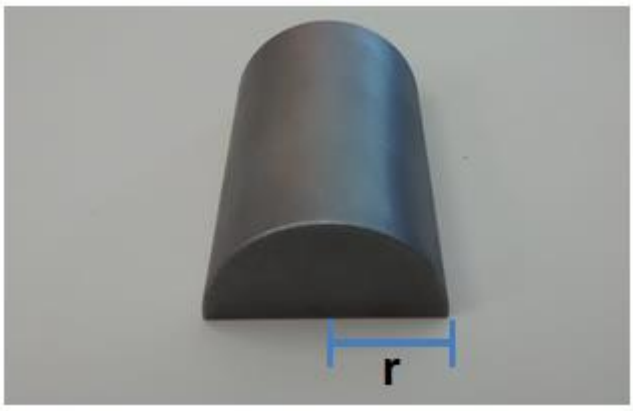
Annex F – Schematic of two basic phtolithographic processes. Comparison between the conventional (on the left) and reverse (or lift-off) photolithographic (on the right) procedures, exemplified by a positive photoresist.



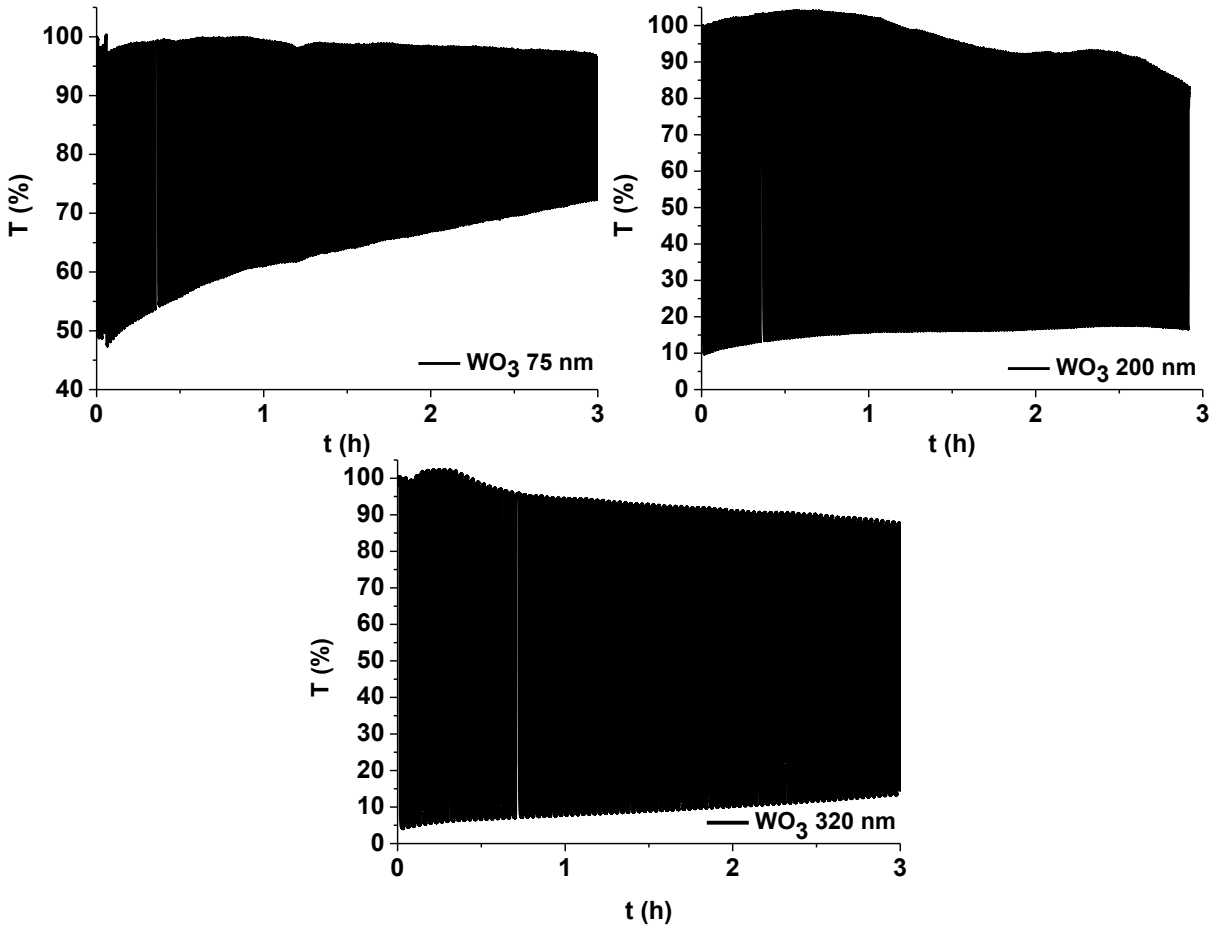
Annex G – Depposition parameters for IZO and WO3 sputtering and for Ti electron-beam evaporation.

Material	Deposition Technique	Deposition System	Deposition Conditions
IZO	RF magnetron sputtering	Home-made	• Target: In_2O_3:ZnO (Super Conductor Materials, diameter of 3 in, 99.99% purity) • Target-substrate distance: 15 cm • Forward power: 75 W • Reflex power: 0 W • DC-Bias: -300 V • Base pressure: $1x10^{-6}$ mbar • O_2 pressure (pO_2): $1.5x10^{-5}$ mbar • Total pressure (pO_2+Ar): $2x10^{-3}$ mbar • Pre-sputtering: 5 min • Deposition time: 40 min • Temperature: RT
WO_3	RF magnetron sputtering	Pfeiffer Classic 500	• Target: WO_3 (Plasmaterials, diameter of 3 in, 99.9% purity) • Target-substrate distance: 15 cm • Forward power: 200 W • Reflex power: 0 W • DC-Bias: -200 V • Base pressure: $1.5x10^{-6}$ mbar • O_2 pressure (pO_2): $1.2x10^{-3}$ mbar • Total pressure (pO_2+Ar): $1.5x10^{-2}$ mbar • Pre-sputtering: 10 min • Deposition time: 10, 30 and 40 min • Temperature: RT
Ti	Electron-beam evaporation	Home-made	• Pellets: Ti (SCM,Inc. random pieces 3-6 mm, 99,99% purity) • Base pressure: $4.5x10^{-6}$ mbar • Deposition time: 5 min 30 s • Temperature: RT

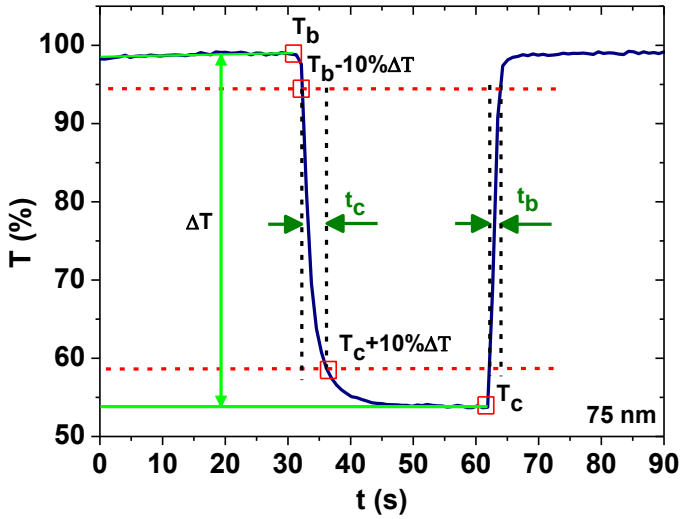
Annex H - Iron support examplification with curvature for mechanical stress during electrical characterization. The used radii were: r= {1.5; 2.25; 3.25} cm.



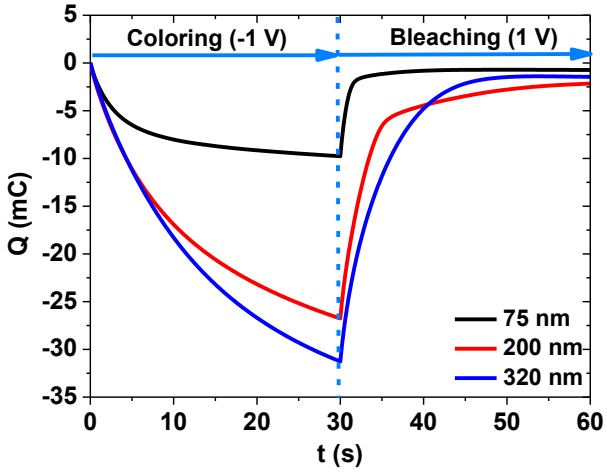
Annex I – Full data spectrum of Chronocoulometry measurements for up to 3 hours with transmittance versus time for voltages of 1 V (bleaching) and -1 V (coloring) during 30 seconds each. Transmittance decrease due to trapped charges and electrolyte degradation becomes clear for this time range.



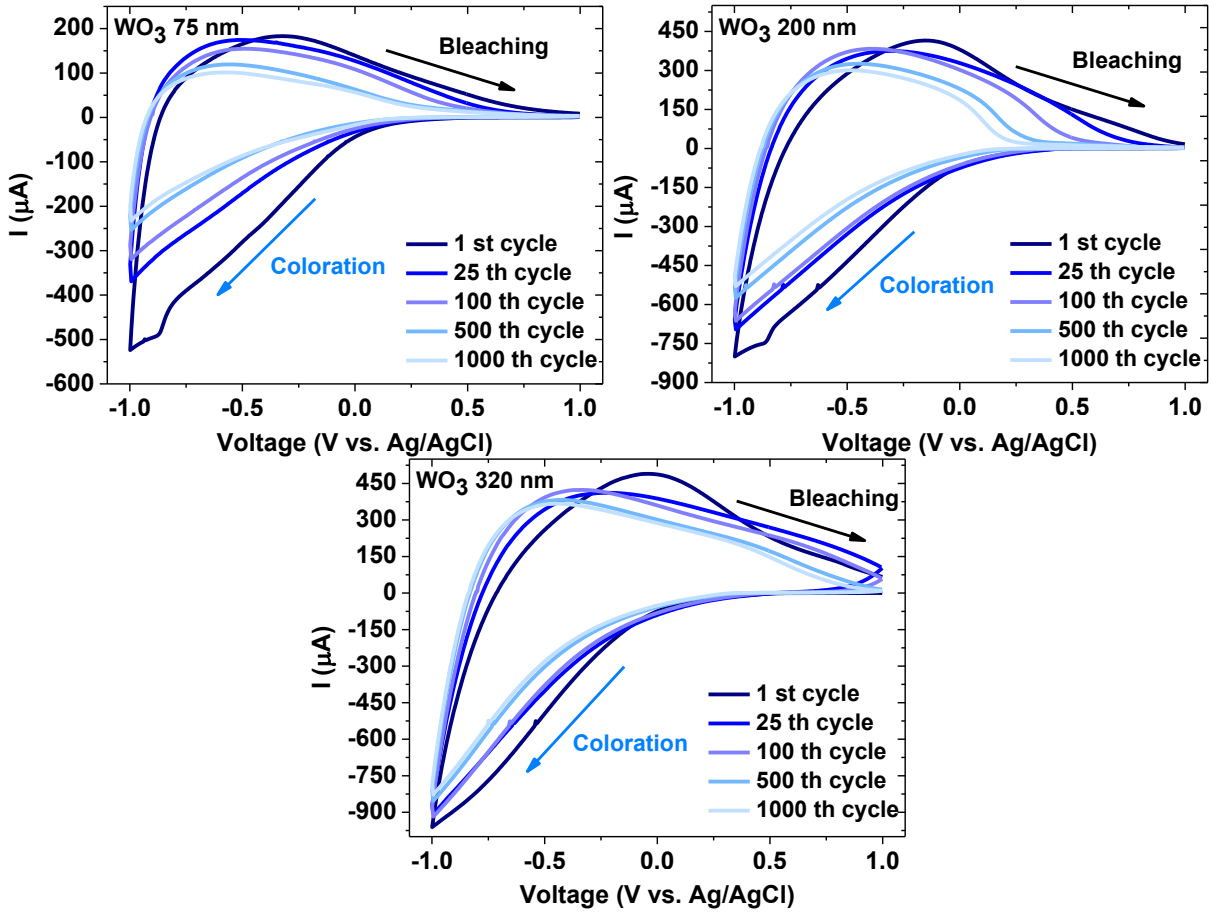
Annex J – Exemplaification of 21st cycle of chronocoulometry measurements with transmittance versus time for voltages of 1 V (bleaching) and -1 V (coloring) during 30 seconds each. Indicated are some vital extractable EC parameters.



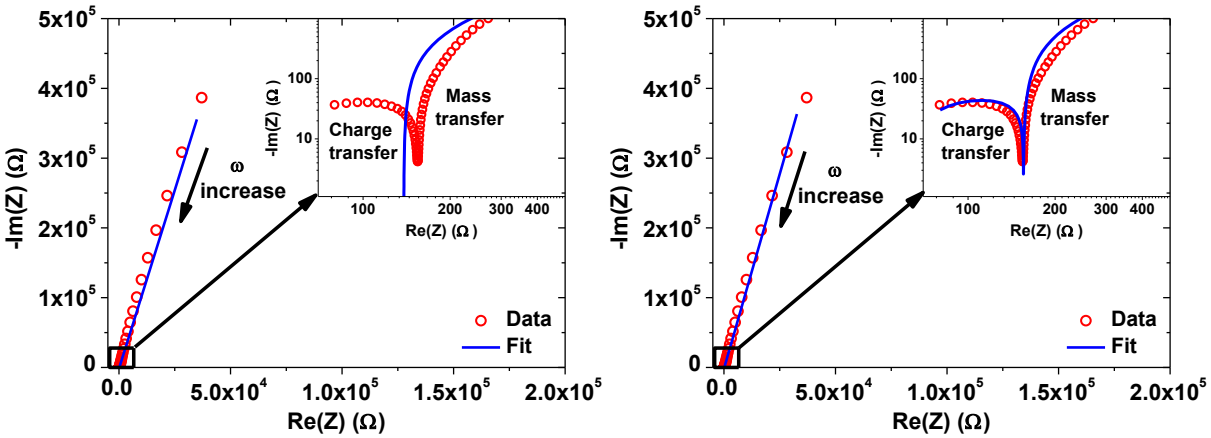
Annex K – Charge insertion and extraction during consecutive 30 seconds coloration (-1 V) and bleaching (1 V) during 21st cycle for three distinct film thicknesses of 75, 200 and 320 nm.



Annex L - Full data spectrum of CV measurements between -1 V (coloration) and 1 V (bleaching) for up to 1000 cycles.



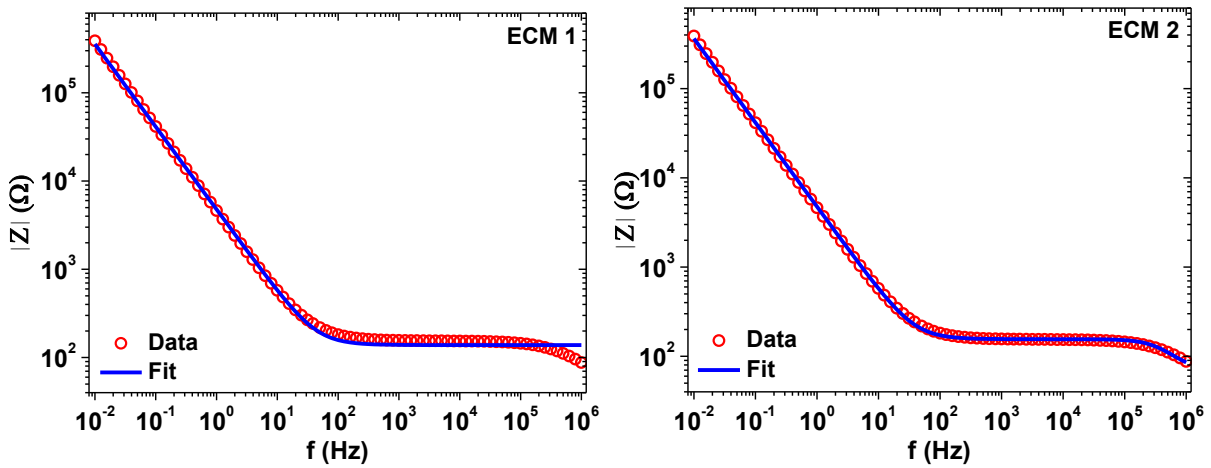
Annex M – Nyquist plots for **a)** ECM 1 and **b)** ECM 2, where red circles indicate the measured data and the blue lines the fittings for each ECM with indication of increasing ω (2πf). Indicated in the insets are also the regions responsible for charge and mass transfer.



Annex N – Extracted parameters for each component comprising ECM 1 and 2. Apart from R_b all parameters show similar values. The value for R_b in ECM 1 is exaggerated and makes no sense to take into considerations for ionic conductivity calculations, being another reason why ECM 2 was selected for the involved calculations.

Parameters	ECM 1	ECM 2
R_b (Ω)	1.18×10^{11}	87.34
R_{ext} (Ω)	138.3	68.00
Y_0 (Ss^{α})	3.75×10^{-5}	3.37×10^{-5}
α	9.38×10^{-1}	9.43×10^{-1}
C_b		4.54×10^{-9}

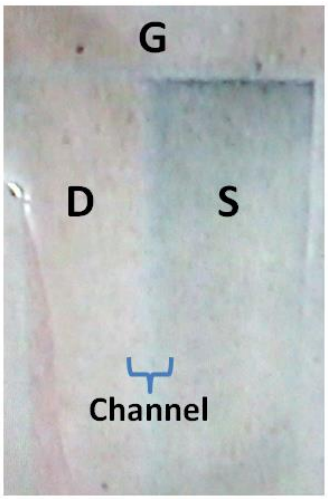
Annex O – Total impedance (|Z|) variation with different frequencies. Better fitting is observed for ECM 2 for the whole frequency spectrum.



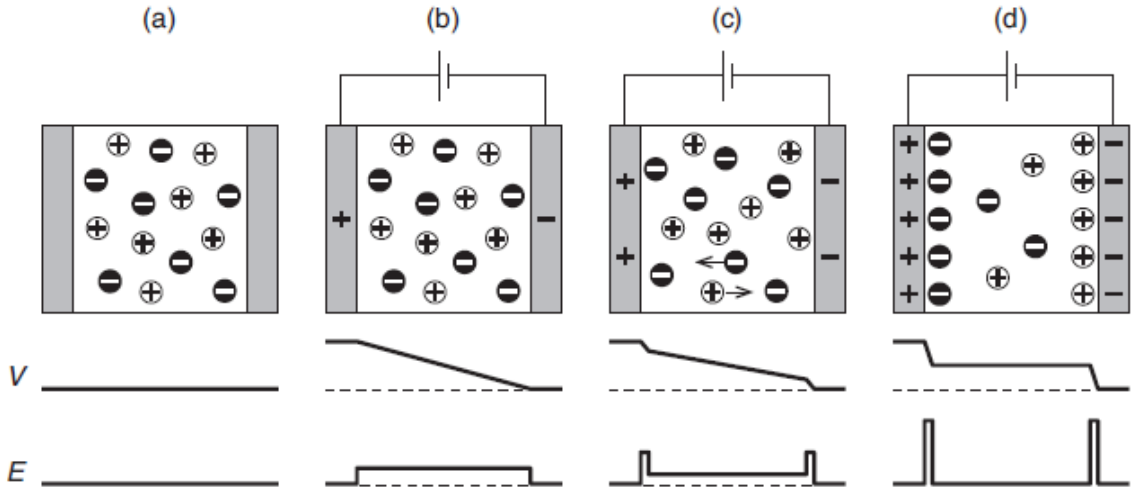
Annex P – Electrical parameters extracted from Hall-measurements for two IZO films deposited at two different values of P_{O2}.

Sample	P_{O2} (mbar)	Film Thickness (nm)	Resistivity		μ ($cm^2V^{-1}s^{-1}$)	Carrier concentration (cm^3)
			R_s (Ω/□)	ρ (Ωcm)		
1	$1.3x10^{-5}$	120	50.2	$6.02x10^{-4}$	49.2	$1.26x10^{20}$
2	$1.5x10^{-5}$	80	37.8	$3.02x10^{-4}$	48.3	$1.71x10^{20}$

Annex Q – Image of an architecture type A ECTFT in the ON (colored) state. Indicated are gate (G), source (S) and drain (D) electrodes as well as the channel region. A light blue non-uniform coloration of the source and channel region is visible, being most intense close to the gate. The drain electrode shows no coloration whatsoever as it is at 1 V, repulsing the Li^+ ions. Similar colorations were observed for architecture type B.

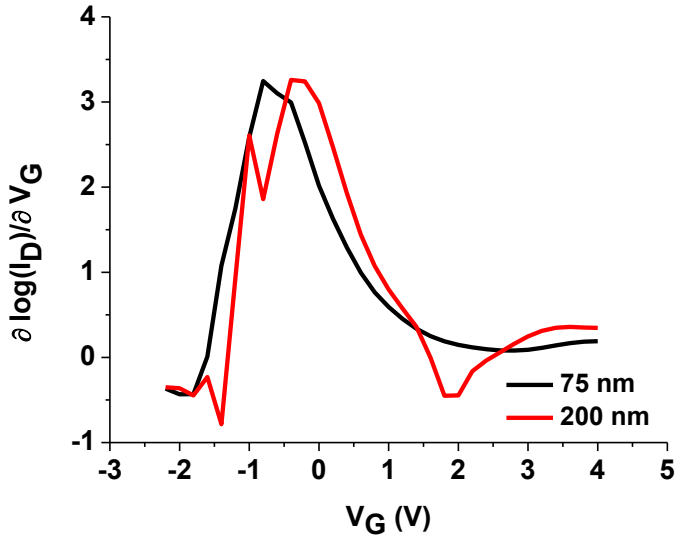


Annex R – Schematic of an electrolytic parallel plate capacitor, where a) shows the steady state with no applied voltage, b) with an applied voltage, c) the ionic relaxation process of the ions in the electrolyte and d) the EDL formation on both interfaces. Also indicated are the potential drop across the electrolyte and the electric field distribution. Adapted from [115].



Annex S – Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.8 a)**, which compares two distinct WO_3 thicknesses (75 and 200 nm) for the same architecture. The used sweep delay was 10 seconds. To determine the subthreshold swing S_s one must take the reciprocal of the maximum value as shown in equation S.1.

Thickness (nm)	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
75	-1.50	0.31	$2.98x10^5$
200	-1.20	0.31	$3.69x10^5$



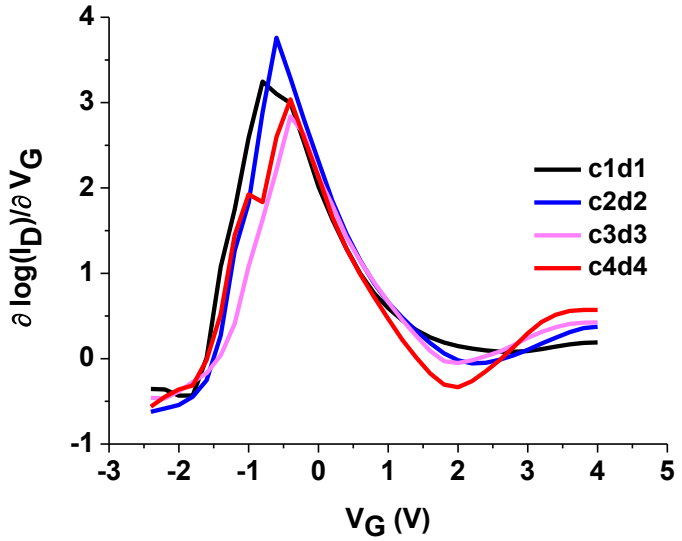
The subthreshold swing S_s is calculated by:

$$S_s = \left(\frac{\partial \log(I_D)}{\partial V_G}\right)^{-1}_{max} \qquad \text{(S.1)}$$

where $\frac{\partial \log(I_D)}{\partial V_G}$ is the subthreshold slope.

Annex T - Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.8 b)**, which compares tansfer curves with increasing W for the same architecture. The used sweep delay was 10 seconds.

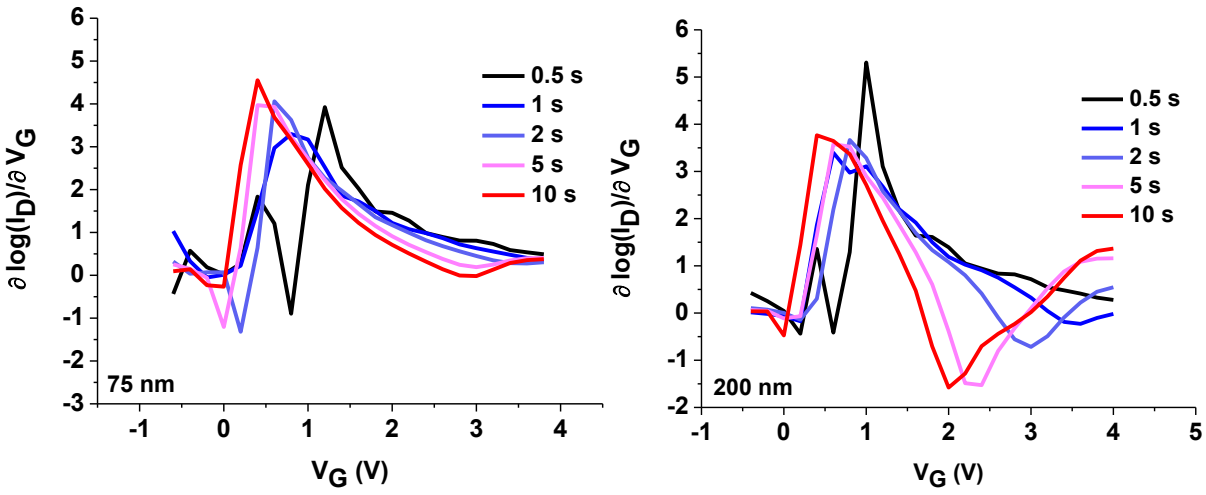
W (µm)	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
250 (c1d1)	-1.60	0.31	$2.98x10^5$
350 (c2d2)	-1.40	0.27	$2.32x10^5$
500 (c3d3)	-1.40	0.35	$2.40x10^4$
800 (c4d4)	-1.50	0.33	$4.19x10^4$



Annex U - Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.9 a)** and **b)**, which compare tansfer curves for two distinct thicknesses (75 and 200 nm) with increasing sweep delays for the same architecture (Aa2b1). The first table shows values corresponding to WO_3 thickness of 75 nm and the second to 200 nm. S_s was calculated at V_{ON}.

Sweep delay (s)	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
0.5	1.00	0.54	$4.55x10^4$
1	0.40	0.30	$1.75x10^5$
2	0.40	0.25	$1.38x10^5$
5	0.20	0.25	$2.32x10^5$
10	0.20	0.22	$1.18x10^5$

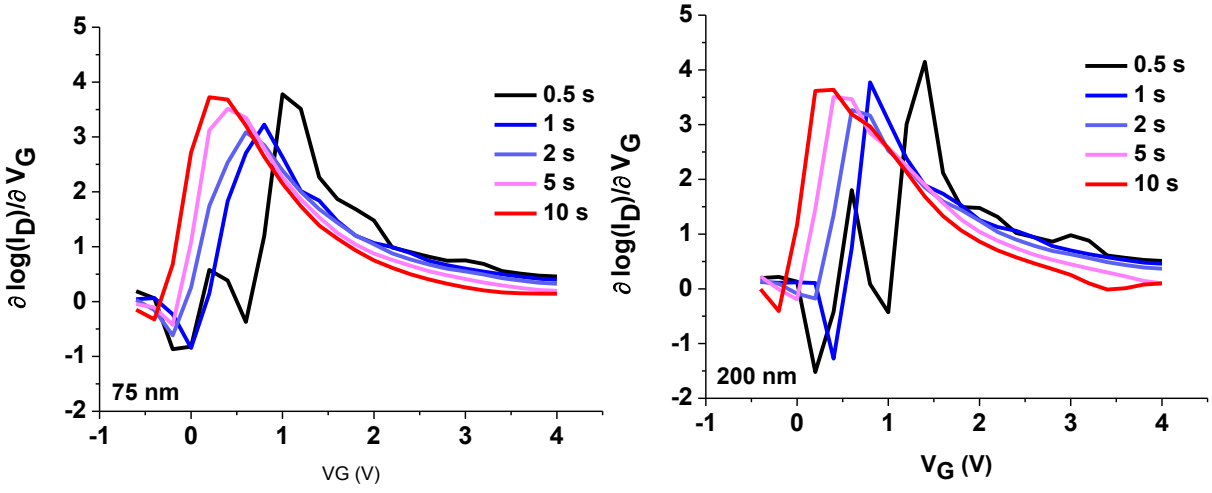
Sweep delay (s)	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
0.5	0.80	0.78	$1.05x10^5$
1	0.40	0.29	$6.30x10^4$
2	0.40	0.27	$5.29x10^3$
5	0.40	0.28	$3.31x10^3$
10	0.20	0.27	$4.78x10^3$



Annex V - Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.9 c)** and **d)**, which compare tansfer curves for two distinct thicknesses (75 and 200 nm) with increasing sweep delays for the same architecture (Ba2b2). The first table shows values corresponding to WO_3 thickness of 75 nm and the second to 200 nm.

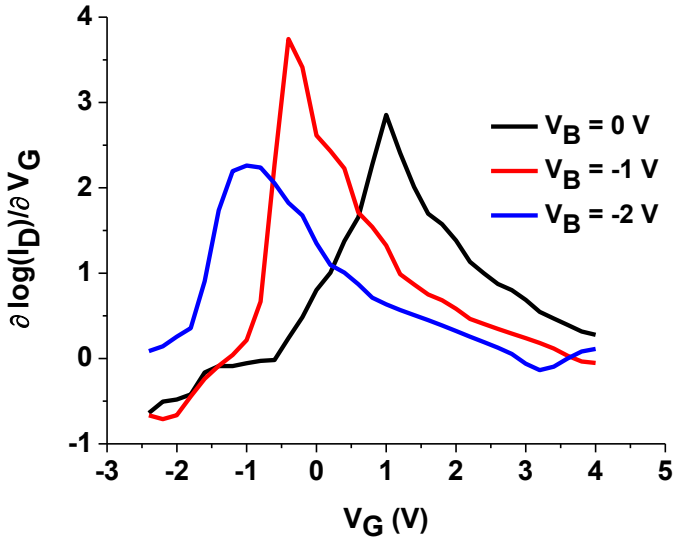
Sweep delay (s)	V_{ON} (V)	S_s (Vdec^{-1})	I_{ON}/I_{OFF}
0.5	0.80	0.26	4.01×10^4
1	0.20	0.31	8.73×10^4
2	0	0.32	1.80×10^5
5	0	0.28	2.63×10^5
10	-0.20	0.27	3.74×10^5

Sweep delay (s)	V_{ON} (V)	S_s (Vdec^{-1})	I_{ON}/I_{OFF}
0.5	1.20	0.24	1.01×10^4
1	0.60	0.27	8.91×10^4
2	0.40	0.31	9.23×10^4
5	0.20	0.28	1.77×10^5
10	0	0.27	2.77×10^5



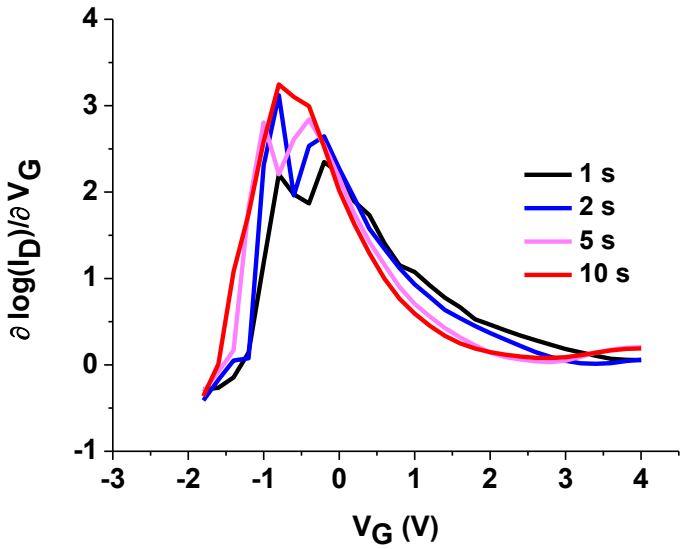
Annex W - Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.10 a)**, which compares tansfer curves with distinct V_B applied (-2, -1 and 0 V) for the same architecture (Ca2c1d1). The used sweep delay was 1 seconds.

V_B (V)	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
-2	-2.00	0.35	$6.21x10^4$
-1	-1.00	0.27	$3.92x10^5$
0	-0.20	0.44	$1.68x10^5$

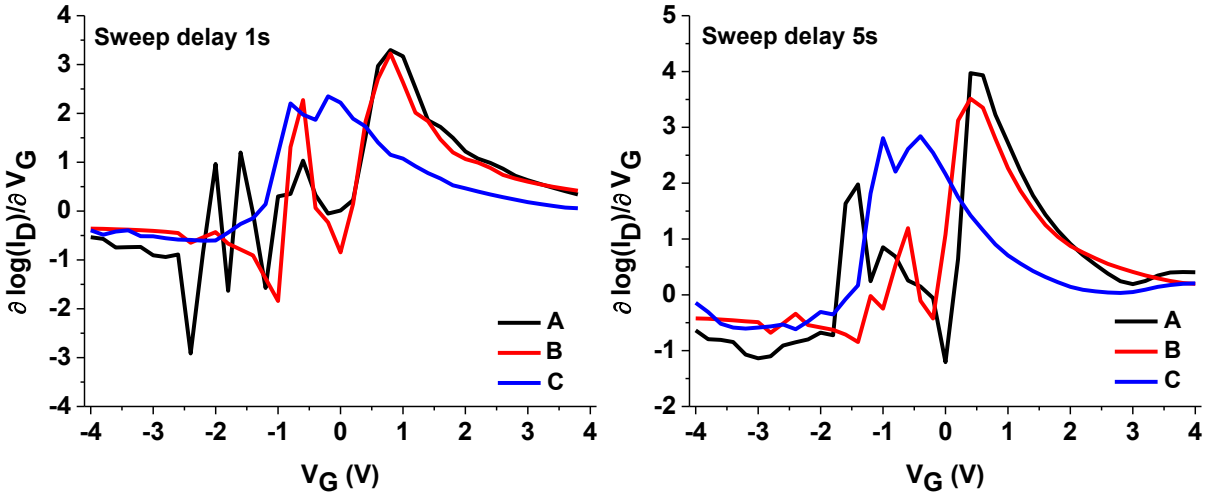


Annex X - Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.10 b)**, which compares tansfer curves with different sweep delays for the same architecture (Ca2c1d1).

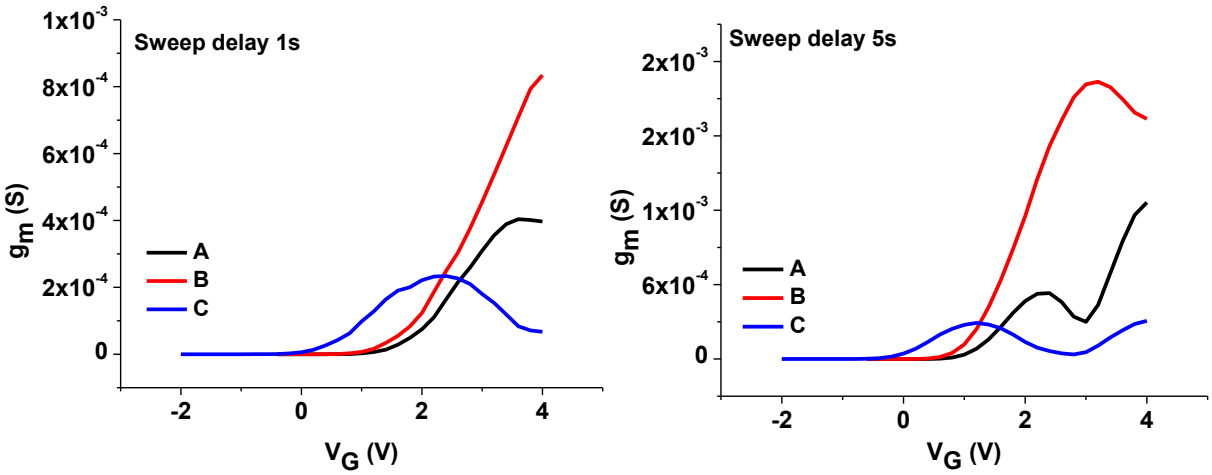
Sweep delay (s)	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
1	-1.00	0.45	$7.71x10^4$
2	-1.00	0.32	$1.20x10^5$
5	-1.20	0.36	$1.48x10^5$
10	-1.40	0.31	$2.44x10^5$



Annex Y – Subthreshold slopes for the best performing architectures in study with 75 nm WO_3 layer for 1 and 5 seconds, respectively. Subthreshold slopes obtained from **Figure 3.12**.

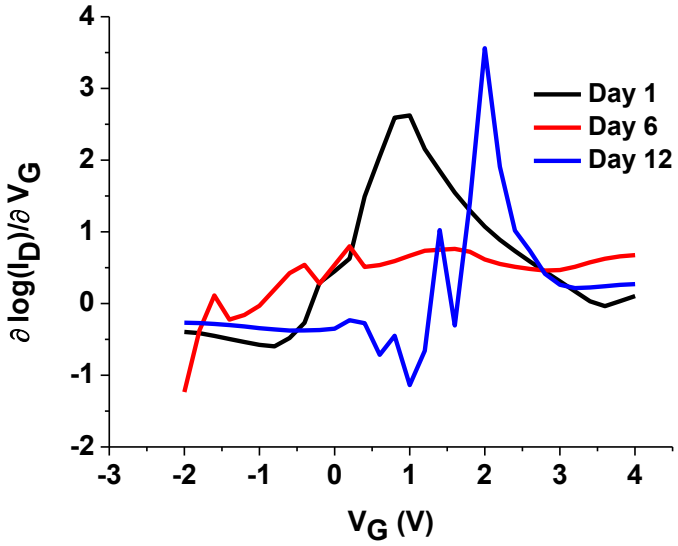


Annex Z - Transconductances for the best performing architectures in study with 75 nm WO_3 layer for 1 and 5 seconds, respectively. Transconductances obtained from **Figure 3.12**.

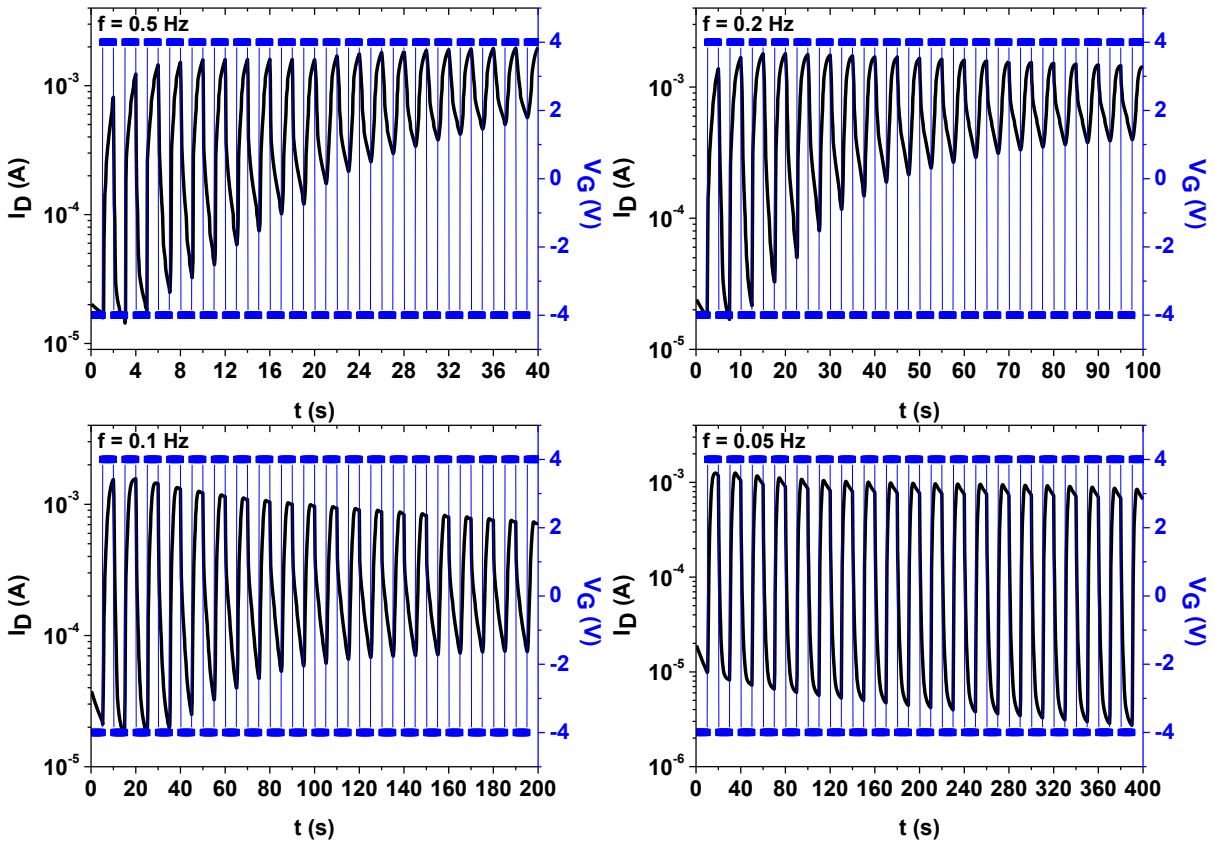


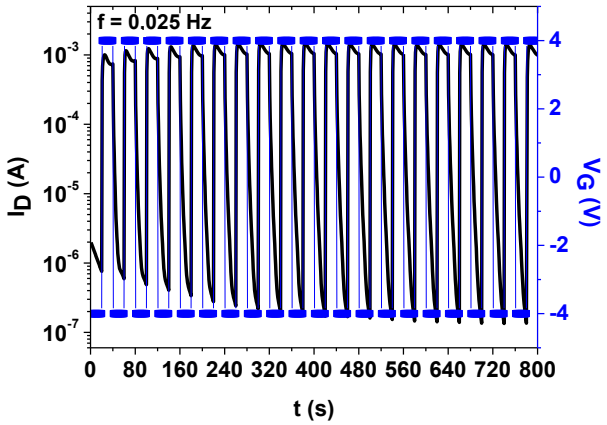
Annex AA - Characteristic parameters and subthreshold slope graphs extracted from transfer curves of **Figure 3.13 c)**, which compares tansfer curves with different sweep delays for the same architecture (Ca2c1d1).

Day after passivation	V_{ON} (V)	S_s ($Vdec^{-1}$)	I_{ON}/I_{OFF}
1	-0.20	0.28	$1.87x10^4$
6	-0.80	1.25	$5.98x10^2$
12	1.80	0.28	$1.7x10^2$

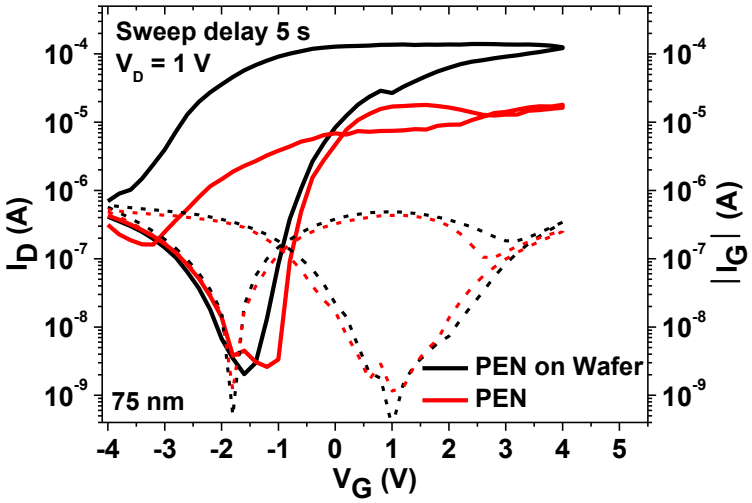


Annex BB – Full data spectrum of symmetric dynamic electrical characterization for architecture C. For higher frequencies degradation of I_{ON}/I_{OFF} is observable due to continuous charge build-up in the channel.





Annex CC – Transfer curves and extracted electrical parameters for best performing ECTFT architecture C for PEN on Wafer vs. delaminated PEN.



Substrate type	I_{ON}/I_{OFF}	V_{ON} (V)	S (V/dec)	g_m (mS)
PEN on Wafer	6.13×10^4	-1.60	0.27	0.039
PEN	6.92×10^3	-1.20	0.18	0.015

Annex DD – Photo of an AM EC display comprised of an 8x8 pixel matrix driven by transistors based on architecture type C developed in CENIMAT│I3N.