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Mestre em Engenharia Microelectrónica e Nanotecnologias

Development of p-type oxide semiconductors based on tin oxide and its alloys: application to thin film transistors

Dissertação para obtenção do Grau de Doutor
em Nanotecnologias e Nanociências

Orientador: Doutora Elvira Maria Correia Fortunato, Professora Catedrática, Faculdade de Ciências e Tecnologia da Universidade Nova de Lisboa

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Novembro de 2014

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ABSTRACT

In spite of the recent p-type oxide TFTs developments based on SnO_x and Cu_xO, the results achieved so far refer to devices processed at high temperatures and are limited by a low hole mobility and a low On-Off ratio and still there is no report on p-type oxide TFTs with performance similar to n-type, especially when comparing their field-effect mobility values, which are at least one order of magnitude higher on n-type oxide TFTs. Achieving high performance p-type oxide TFTs will definitely promote a new era for electronics in rigid and flexible substrates, away from silicon. None of the few reported p-channel oxide TFTs is suitable for practical applications, which demand significant improvements in the device engineering to meet the real-world electronic requirements, where low processing temperatures together with high mobility and high On-Off ratio are required for TFT and CMOS applications.

The present thesis focuses on the study and optimization of p-type thin film transistors based on oxide semiconductors deposited by r.f. magnetron sputtering without intentional substrate heating. In this work several p-type oxide semiconductors were studied and optimized based on undoped tin oxide, Cu-doped SnO_x and In-doped SnO_2.

The influence of the deposition parameters, such as the percentage of oxygen and the deposition pressure and post deposition annealing treatments (up to 200 °C) parameters was investigated in order to optimize the properties of the p-type thin films. The detailed study of the material was accomplished through various techniques of characterization of their electrical and optical properties, crystal structure, chemical composition, topology and morphology.

The obtained undoped SnO_x thin films showed p-type conduction for a narrow percentage of oxygen, between 2.5% and 4%, after an annealing treatment at 150 °C and 200 °C. The thin films have a mixture of both tetragonal β-Sn and α-SnO phases, mobilities between1.6 cm^2/Vs and 2.6 cm^2/Vs and a carrier concentration between 10^{16} and 10^{17} cm^{-3}. TFTs produced with this material were optimized presenting very good electrical performances, with On-Off ratio ~10^4, μ_{FE} up to 3.5 cm^2/Vs and V_{th} between -0.41 V and 15 V. The influence of the dielectric was also studied and leading to new results. Depending on the gate dielectric used, n-, p-type and ambipolar devices were obtained for the same semiconductor deposition conditions.

Doping SnO_x with Cu also results in transparent p-type oxide semiconductors with mobilities between 1.6 cm^2/Vs and 2.6 cm^2/Vs and a carrier concentration between 10^{16} and 10^{17} cm^{-3}. When applied as active layer, resulted in poor performance thin film transistors, with lower On-Off ratio and the higher V_{th}, despite μ_{FE} increased.

When doping the SnO_2 films with In, p-type conduction was achieved without the need of the annealing treatment. The obtained as deposited thin films are amorphous and show mobilities up

to 27 cm^2/Vs and very low resistivities ~10^{-3} Ω cm, obtaining in this way the a p-type oxide transparent conductor with the lowest electrical resistivity so far reported in the literature.

RESUMO

Apesar dos recentes desenvolvimentos em TFTs tipo-p, baseados em SnO_x e Cu_xO, os resultados obtidos até agora referem-se a dispositivos produzidos a temperaturas elevadas, cuja principal limitação é a baixa mobilidade dos portadores de carga maioritários, buracos, e baixa razão On-Off. Sendo que ainda não se encontra na literatura aritogs de TFTs tipo-p com desempenho semelhante a TFTs tipo-n, produzir TFTs tipo-p a baixa temperatura com elevado desempenho, vai certamente iniciar uma nova era para a electrónica em substratos rígidos e flexíveis onde temperaturas de processo baixas, elevada mobilidade e elevado rácio On-Off são necessários para aplicações em TFTs e CMOS.

Esta tese, foca-se no estudo e optimização de TFTs baseados em óxidos semicondutores tipo-p depositados por pulverização catódica reactiva de rádio frequência assistida por magnetrão sem aquecimento intencional do substrato. Neste trabalho foram estudados e otimizados vários óxidos semicondutores tipo-p de SnO_x não dopado, SnO_x dopado com Cu, e SnO_2 dopado com In. A influência dos parâmetros de deposição, tais como a quantidade de oxigénio na câmara de deposição, a pressão de deposição e o recozimento efectuado após a deposição (até 200 °C), foi estudada de forma a optimizar as propriedades dos óxidos semicondutores transparentes. O estudo detalhado do material foi realizado através de várias técnicas de caracterização, tendo inferido as propriedades eléctricas, ópticas, estruturais, composição química, e morfologia.

Os filmes de SnO_x obtidos apresentam condução tipo-p para uma percentagem de oxigénio entre 2.5% e 4%, após um tratamento térmico de 150 °C – 200 °C. Os filmes apresentam uma mistura de fases de β-Sn e α-SnO, apresentando mobilidades entre 1,6 cm^2/Vs e 2,6 cm^2/Vs, e uma concentração de portadores entre 10^{16} e 10^{17} cm^{-3}.

Após a obtenção do óxido semicondutor tipo-p, produziram-se os TFTs. Obtiveram-se TFTs a funcionar nos diferentes modos, de depleção e enriquecimento, com V_{th} de -0,41 V a 15 V, rácio On-Off ratio ~10^4 e μ_{FE} até 3.5 cm^2/Vs . A influência do dieléctrico no desempenho do dispositivo também foi estudada, tendo sido obtidos novos e promissores resultados. Dependendo do dieléctrico utilizado, foram obtidos transístores a tipo-n, tipo-p e ambipolares, para a mesma condição de deposição da camada activa.

Dopar SnO_x com Cu também resultou em óxidos semicondutores tipo-p com mobilidades entre 1.6 cm^2/Vs e 2.6 cm^2/Vs e N entre 10^{16} e 10^{17} cm^{-3}. Os transístores com base neste material apresentam, de um forma geral, um pior desempenho, com um rácio On-Off inferior e maior V_{th}, apesar do aumento na μ_{FE}.

Ao dopar SnO_2 com In, obtiveram-se semicondutores tipo-p, sem a necessidade de qualquer tratamento térmico. Os filmes obtidos apresentam um estrutura amorfa e elevada transparência na zona do visível. Em relação às propriedades eléctricas, conseguiu-se obter um óxido tipo-p

com mobilidade de 23 cm^2/Vs e resistividade bastante baixa, ~10^{-3} Ω cm, obtendo-se desta forma um condutor transparente tipo-p com propriedades únicas.

SYMBOLS

%Cu - percentage of copper defined by (Cu/(Cu+Sn))

%In - percentage of copper defined by (In/(In+Sn))

percentage of oxygen content in the $Ar+O_2$ mixture

$\vec{B}$ - *magnetic field vector*

$\vec{E}$ - electric field vector

A – Area

c - Speed of light (= 3.0×10^8 m/s)

C_i - Areal capacitance

D - Crystallite size

d_d - Dielectric thickness

d_{hkl} - Inter-planar spacing

d_s - Oxide semiconductor thickness

E - Electric field

E_a - Thermal activation energy

E_c - Conduction band

E_F - Fermi level

E_G – Bandgap

E_{opt} - Optical band-gap (eV)

g_{d} – Condutance

g_{m} – Transcondutance

h - Planck's constant (= 6.626×10^{-34} J·s)

I - Current

I_{DS} - Drain to source current

I_{GS} - Gate leakage current

I_{off} - I_{DS} at off state

I_{on} - I_{DS} at on state

J - Current density

k - Extinction coefficient

L - Channel length

n - Refractive index

N - Free carrier concentration

N_s - Sheet carrier density

On-Off ratio - TFT I_{DS} on-to-off ratio

p_d - Deposition pressure

P_{rf} - rf power density

q - Elementary charge of a particle ($1.6x10^{-19}$ C)

R_H - Hall coefficient

R_{sheet} - Sheet resistance

SS - Subthreshold gate voltage swing

T – Transmittance

T_A - Annealing temperature

V – Voltage

V_{DS} - Drain to source voltage

V_{GS} - Gate voltage

V_H - Gate voltage

V_{on} - Turn-on voltage

V_{th} - Threshold voltage

W - Channel width

α – Absorption coefficient (/cm)

ε_0 - Vacuum dielectric constant (= 8.85×10^{-12} F/m)

ε_s - Dielectric constant of the semiconductor

ϑ - Bragg angle

Φ - Figure of merit

χ – Electron affinity

χ^2- Error function

φ_B - Barrier height

φ_G - Gate electrode work function

φ_M - Metal work function

φ_S - Semiconductor work function

κ – Dielectric constant

λ – Wavelength of electromagnetic wave

μ – Mobility

μ_{FE} - Field-effect mobility

μ_{SAT} - Saturation mobility

μ_{eff} - Effective mobility

ρ – Electrical resistivity

σ – Electrical conductivity

υ – Frequency of electromagnetic wave

ψ – Differential amplitude angle

ABBREVIATIONS

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ATO	Antimony-doped Tin Oxide
CBM	Conduction band minimum
CEMOP	Centro de Excelência de Microelectrónica e Optoelectrónica de Processos
CENIMAT	Centro de Investigação de Materiais
CVD	Chemical Vapor Deposition
EDS	Energy Dispersive X-ray
FPD	Flat Panel Display
FWHM	Full Width at Half Maximum
GIZO	Gallium Indium Zinc Oxide
I3N	Instituto de Nanoestruturas, Nanomodelação e Nanofabricação
IPA	Isopropilic Alcohol
ITN	Instituto Tecnológico e Nuclear
ITO	Indium Tin Oxide (Sn-doped In_2O_3)
KP	Kelvin Probe
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MIS	Metal-Insulator-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NIR	Near Infrared
OLEDs	Organic Light Emitting Diode
PLD	Pulsed Laser Deposition
PLD	Pulsed Laser Deposition

PVD	Physical Vapor Deposition
r.f.	radio-frequency
RBS	Rutherford Backscattering Spectroscopy
RMS	Root-mean-square
sccm	Standard cubic centimeters per minute
SEM	Scanning Electron Microscopy
SMU	Source Monitor Unit
SPA	Semiconductor Parameter Analyzer
STM	Scanning Tunneling Microscopy
TCLC	Trap Charged Limited Current
TCO	Transparent Conducting Oxide
TFT	Thin-Film Transistor
TSO	Transparent Semiconductor Oxide
UV	Ultra-Violet
VBM	Valence Band Maximum
VRH	Variable Range Hopping
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction

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1. MOTIVATION, OBJECTIVE AND STRUCTURE OF THE DISSERTATION

1.1. Motivation

Transparent Electronics is an emerging field of technology in which the conventional opaque electronic components are expected to be replaced by transparent electronic ones. Even though most of the conventional electronic applications require both n-type and p-type transistors, there appears relatively little effort towards the development of p-type transparent thin-film transistors (TFTs) and p-type transparent conducting oxides (TCOs) [1]–[3]. Developments on this area would enable oxide CMOS circuitry and great improvements on existing optoelectronic devices, such as OLEDs and related applications, such as flat-panel displays.

The enormous success of n-type oxides and the application of transparent conductive oxides (TCOs) as “invisible electrodes” [4], [5] and of transparent semiconductive oxides (TSOs) as active channel layers of thin-film transistors (TFTs) [6]–[9] has motivated the interest in p-type oxides for both types of applications. Indeed, p-type oxides are relevant both for TCO (as low contact resistance material for a large variety of optoelectronic devices, such as solar cells or OLEDs) and TSO (for fully transparent p-n junctions or p-type TFTs) applications. One of the major goals is to have ambipolar devices, enabling Complementary Metal Oxide Semiconductors (CMOS) architectures, for fast and low-power consumption electronics, as required when complex and integrated electronic blocks are thought to be fabricated [10] [11]

However, until now reports on p-type TCOs are scarce, most of them arose in the last 5 years, while no report about p-type oxide TFTs with performance similar to n-type ones is known. As far as TSOs are concerned, we are facing exactly the same problems faced by organic TFTs but now in an opposite way, since most of organic TFTs with good electrical performance are p-type [12], [13]. Organic materials have been studied for more than 50 years and the significant improvements in the semiconducting properties associated to the discovery of electroluminescence in organic diode structures make these materials excellent candidates for low-cost electronic and optoelectronic integrated systems[14], [15]. The main advantage of these materials is their low temperature fabrication, while the main disadvantage is the life time of the devices where they are integrated, concerning both idle shelf life and stability under electrical stress. Moreover, the n-type organic semiconductors have even much lower mobilities than p-type ones (10^{-2} -10^{-1} against 1-2 cm^2 V^{-1} s^{-1}), [16]–[19] limiting the field of applications of these materials, inhibiting important concepts such as reliable CMOS circuitry. All these issues drive the need of searching for alternatives combining stable and good performing electronic devices that

can be processed at low temperatures with low fabrication costs. Oxide materials are seen as one of the most promising routes to achieve this.

At present, almost all reported oxide TCOs and TSOs for TFTs are based on n-type oxides [20]–[23]. For p-type oxides, carrier conduction path (valence band) is mainly formed from the oxygen p asymmetric orbitals, which severely limits the carrier mobility. Thus, p-type oxides have very low carrier mobility compared to their n-type counterparts, which is the main obstacle in obtaining high performance TCOs and p-channel oxide TFTs. Recently much attention has been given to Cu and Sn based semiconductors[1], [3], [24]. By introducing III-family elements in these materials, such as In, doping can theoretically be achieved in order to enhance conductivity and mobility.

1.2. Objectives

The main objective of this dissertation is to produce, study and optimize transparent sputtered p-type oxide semiconductors based on tin oxide and to apply as channel layers in thin film transistors. For this purpose, it was first studied the influence of different deposition and post deposition parameters on the structural, morphological and compositional, electrical and optical properties of the films. After its optimization, the thin films were applied as channel layer in TFTs. Besides that, it was also exploited some of the produced p-type thin films as TCOs

1.3. Structure of the dissertation

The present chapter presents the motivation, objectives, and the organization throughout the dissertation. Chapter 2 is divided into two main themes: first introduces the subject of TOS referring to its main properties with particular focus on oxides based on tin oxide and its alloys. The second where are described the properties and working principle of TFTs. Chapter 3 focuses on the production and characterization techniques used during the research work of this dissertation. At chapter 4 are presented and discussed the the main results obtained within this dissertation to obtain p-type oxide semiconductors and at Chapter 5 is demonstrated the application of the produced TOS in TFTs. Finally, in Chapter 6 are presented the main conclusions of this work as well as future prospects.

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Chapter 2. Transparent oxide semiconductors, thin films transistors

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2. TRANSPARENT OXIDE SEMICONDUCTORS, THIN-FILM TRANSISTORS

2.1. General concepts

We are currently experiencing a fascinating scientific period in the area of thin film transistors using non-conventional materials, like oxide conductors and semiconductors. Conductive transparent oxides (TCOs) are a special class of materials, because they exhibit both high optical transparency to visible light and electrical conductivity, which is not common when one considers conventional materials such as metals, polymers and ceramics. In general, material as metals have a high conductivity, but are opaque and a wide band gap material means a low carrier concentration, which makes the material an insulator, like glass. This can be achieved if the materials has a band gap above 3 eV and the carrier concentration (free electrons or holes) should above 10^{19} – 10^{20} cm^{-3} (Figure 2.1) [1]. These oxide materials are mainly based on SnO_2, ZnO and In_2O_3. Usually dopants are used to supply the carriers needed to make many oxides electrical conductors, such as Al-doped ZnO (AZO), Sn-doped In_2O_3 (ITO) to achieve carrier concentration of the order of 10^{21} cm^{-3}. Transparent oxide semiconductors has been created with the objective to increase the carrier mobility and decrease the carrier concentration, making possible its use for the production of high performance thin film transistors (TFTs).

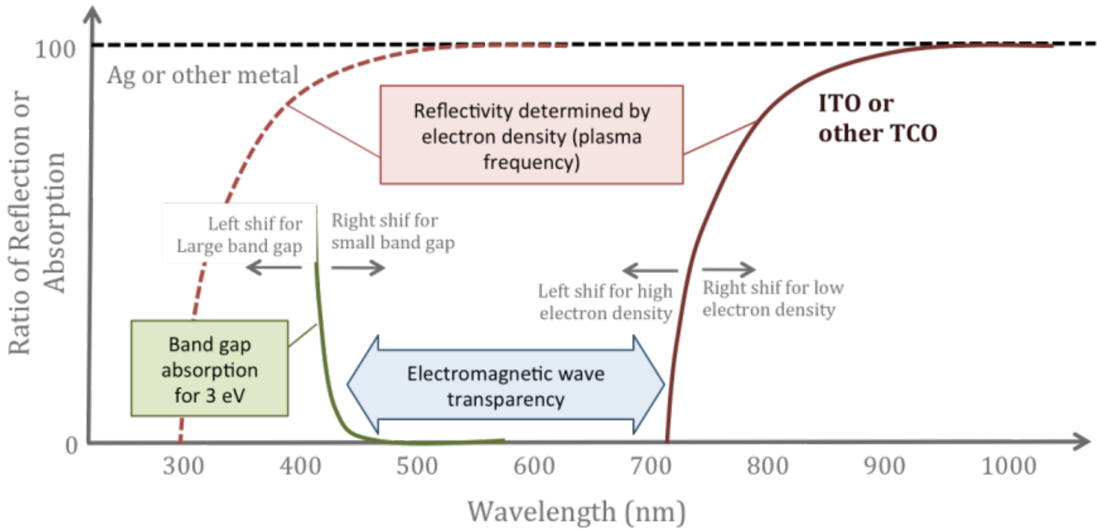

Figure 2.1. Conditions for transparent materials: for a semiconductor, dielectric or other material to be transparent we must follow two conditions: (1) the band gap must be wider than 3 eV; and (2) the carrier concentration must be below 10^{21} cm^{-3}. If both conditions are met simultaneously, visible light will not be reflected or absorbed [2].

Transparent electronics is today one of the most advanced topics for a wide range of device applications, where the key component are wide band gap semiconductors, where oxides of different origin play an important role, not only as passive component but also as an active component similar to what we observe in conventional semiconductors. As passive components they include the use of these materials as dielectrics for a wide range of electronic devices and also as transparent electrical conductors for used in several optoelectronic applications, such as liquid crystal displays, organic light emitting diodes, solar cells, optical sensors [3]–[6]. As active material, they exploit the use of truly electronic semiconductors where the main emphasis is been put on transparent thin film transistors, light emitting diodes, lasers, UV sensors, integrated circuits among others [7]–[10]. The way to achieve these properties is to use wide band gap oxides, in order to favor the transparency, doped with a significant amount of mobile charge carriers, holes (p-type) or electrons (n-type). Oxide electronics or in more generic terms transparent electronics, is emerging as a serious alternative to amorphous silicon (a-Si:H) and organic semiconductors, especially for thin film transistors (TFTs) and more complex electronic circuits. Oxide semiconductors are a promising class of TFT materials that have made an impressive progress especially in display applications in a relatively short time, challenging silicon not only in conventional applications but specially opening doors to completely new and disruptive areas like paper electronics [11].

Within the diverse library of transparent semiconductors, amorphous transparent oxide semiconductors (a-TOSs) possess several distinctive attractions over organics, III/V compounds, and crystalline TOSs, such as substantial carrier mobility, excellent environment stability, low-temperature processability, smooth surface morphology, and great film uniformity [12]–[16]. The ideal choice for n-type a-TOS are a series of metal oxides composed of cations having a $(n-1)d^{10}ns^{0}$ $(n \geq 4)$ electronic configuration and oxygen anions [17]. Under this definition, candidates HMCs to form TOSs can be found from the periodic table. Table 2.1 shows the elements under this definition as well as their electronic configurations.

Table 2.1. Candidates for a-TOS and respective electronic configuration [18].

Cu	Zn	Ga	Ge	As
[Ar]3d¹⁰4s¹ → $[Ar]3d^{10}4s^{1}$	$[Ar]3d^{10}4s^{2}$	$[Ar]3d^{10}4s^{2}4p^{1}$	$[Ar]3d^{10}4s^{2}4p^{2}$	$[Ar]3d^{10}4s^{2}4p^{3}$
Ag	**Cd**	**In**	**Sn**	**Sb**
$[Kr]4d^{10}5s^{1}$	$[Kr]4d^{10}5s^{2}$	$[Kr]4d^{10}5s^{2}5p^{1}$	$[Kr]4d^{10}5s^{2}5p^{2}$	$[Kr]4d^{10}5s^{2}5p^{3}$
Au	**Hg**	**Tl**	**Pb**	**Bi**
$[Xe]4f^{14}5d^{10}6s^{1}$	$[Xe]4f^{14}5d^{10}6s^{2}$	$[Xe]4f^{14}5d^{10}6s^{2}5p^{1}$	$[Xe]4f^{14}5d^{10}6s^{2}5p^{2}$	$[Xe]4f^{14}5d^{10}6s^{2}6p^{3}$

$[Ar]:1s^{2}1s^{2}2s^{2}2p^{6}3s^{2}3p^{6}$;

$[Kr]:1s^{2}2s^{2}2p^{6}3s^{2}3p^{6}3d^{10}4s^{2}4p^{6}$;

$[Xe]:1s^{2}2s^{2}2p^{6}3s^{2}3p^{6}3d^{10}4s^{2}4p^{6}4d^{10}5s^{2}5p^{6}$

The first publication of a partially transparent TFT using an n-type TSO as active layer was presented by Klansens and Koelmans in 1964[1], where the oxide semiconductor material used as active layer was SnO_2. Although the oxide semiconductor used is highly transparent in the visible region, the gate electrode used was Al and a non-specified metal was used as source and drain electrodes. There are no details about the electrical performance of the device. Another publication of a partially transparent TFT n-type appeared in 1997 by Prins et al [19]. The TSO used was SnO_2:Sb and as dielectric a ferroelectric material $PbZr_{0.2}Ti_{0.8}O$, both transparent. The only non-transparent material was the gate electrode, $SrRuO_3$. The structure of the device is co-planar bottom-gate. All these SnO_2 based TFTs are depletion-mode devices, requiring the applications of a gate voltage to turn them off.

The first publications of fully transparent TFTs emerged in 2003 by Hoffman et al, Carcia et al, Masuda et al, Nishii et al, Nomura et al, Norris et al, and Fortunato et al [20]–[25]. Although these devices have zinc oxide (ZnO) as active layer, there are significant differences, in particular regarding the deposition techniques, the structure of the device and the maximum temperature reached in the process. The latter is one of the most important factors in the manufacturing process of a TFT, because it allows the use of a wider range of substrates, for example, low cost polymers such as paper [26] or polyethylene terephthalate (PET) [27]. Both Carcia and Fortunato devices were produced at room temperature.

Others n-type TFTs have been developed based in materials such as indium oxide, zinc oxide and binary and ternary compounds based on these materials such as zinc tin oxide (ZTO), indium zinc oxide (IZO), zinc tin gallium oxide (ZTGO), and gallium indium zinc oxide (GIZO) may be used as channel layer in high performance transparent thin film transistors (TFTs) [28], [29] [9], [30], [31]. This extensive academic and industrial efforts made to enhance the TTFT performance, e.g., to improve the field effect mobility (μ_{FE}) and/or to lower the operating voltages [32]–[37], results in a significant worldwide interest appeared, especially for active matrix for organic light emitting diodes (AMOLED) technology, both in industry and academia.

Samsung has released at the end of 2010 what they boast proudly as one of the world’s finest and largest 3D Ultra Definition (UD) TV [38] with 70” diagonal and a sports resolution of 240 Hz that will meet the demands of 3D capability. Samsung has claimed that, the making of this device is the first of the kind on oxide semiconductor TFT technology that supports high pixel density of resolution of 3840 × 2160, which is equivalent to 8 MP. These transparent LCD panel utilizes ambient light such as sunlight, which consequently reduces the dependency on electricity for generating power. This new class of semiconductor materials, amorphous oxides semiconductors (AOS) represents a revolutionary idea and exhibit a stimulating combination of high optical transparency, high electron mobility, and amorphous microstructures [39], [40].

Besides that, AOSs do not have grain boundaries, thereby obviating the primary limitation of mobility in polycrystalline semiconductors, which is a huge advantage for process integration. Other advantages include low temperature deposition routes and ultra-smooth surfaces for suppressing interface traps and scattering centers. Besides that the materials as well as the technology used are environmental friendly and much less expensive than conventional silicon technology [41]. In Table 2.2 it is presented a summary of some of the most important device properties for the different available technologies; amorphous Si, polycrystalline Si and oxide semiconductors.

Table 2.2. Comparison between transparent n-type based TFTs and the other commercial available technologies; amorphous Si and poly-Si [7].

TFT properties	Oxide semiconductors	Amorphous Si	Low-T poly-Si
μ (cm^2/Vs)	1 to 100	1 max	50 to 100
S (V/dec)	0.1 to 0.6	0.4 to 0.5	0.2 to 0.3
Leakage current (A)	10^{-13}	$\sim 10^{-12}$	$\sim 10^{-12}$
TFT characteristic variation	Low	Low	High
TFT for AMOLEDs	4 to 5 masks	4 to 5 masks	5 to 9 masks
Manufacturing cost	Low	Low	High
Long term TFT reliability	High (forecast)	Low	High
Yield	High	High	Low
Process temperature (°C)	RT to 350	About 250	250
CMOS fabrication	Yes (large areas)	Very low performance	Yes (not large areas)

However, these TFTs are limited to n-type conduction and despite the p-type oxide TFTs developments based on SnO_x [42]–[45] and Cu_xO [46]–[50], the results achieved so far, refer to devices processed at high temperatures limited by a low hole mobility and with a low On-Off ratio. Achieving high performance p-type oxide TFTs (they have the advantage among n-type TFTs since the TFT supply hole current for the anode of the OLED with-out affecting the drain current in the saturation mode) will definitely promote a new era for electronics in rigid and flexible substrates, away from silicon.

None of the few reported p-channel oxide TFTs, is suitable for practical applications, which demand significant improvements in the device engineering to meet the real-world electronic requirements, where low processing temperatures together with high mobility and high On-Off ratio are required for TFT and CMOS applications. Producing and developing p-type oxide TFTs are mainly limited by the low hole mobilities due to hopping conduction, characteristic of the material in which the valence band maxima (VBM) is mainly composed from localized O 2p orbitals with strong directivity and large electronegativity [51].

The development of p-type oxide semiconductors and its application at thin film transistors enables a number of new applications in transparent electronics such as pn junctions and complementary circuits CMOS (complementary metal-oxide-semiconductor).

2.2. P-type oxide semiconductors

The main reason to the difficulty of developing high-mobility p-type TCOs is due to the localized oxygen p nature of the valence band in most oxides that makes those bands very flat and leads to large hole effective masses [52], [53].

Only few transparent p-type semiconductors are known and studied, where the most studied are Cu based materials with the delafossites structure as $CuAlO_2$, $SrCu_2O_2$, Cu_2O, LaCuOS, $CuCrO_2$:Mg, $CuGaO_2$ and $CuInO_2$ [49], [54]–[70]. The low effective mass is due to the hybridization of closed 3d shell of Cu cation with oxygen 2p orbitals.

Cu_2O is a p-type oxide with mobility exceeding 100 cm^2/Vs [71]. However, TFTs based on these materials have lower field-effect mobilities and On-Off current ratio, below 1 cm^2/Vs and 10^2 respectively, due to difficulty in controlling the hole density in channel layer as well as in control the high density of interface defects specially at the channel/semiconductor interface [71]–[75].

Nevertheless recently Zhou [82] demonstrated a Cu_2O based TFT with a mobility and On-Off ratio of 4.3 cm^2/Vs and 3×10^6, respectively which reopens the study on this semiconductor with more than 80 years. A good approach to achieve p-type conduction is to use compounds with $(n-1)d^{10}sn^2$ cations (Sn^{2+}, Pb^{2+}, Tl^{+1}) where the low effective mass originates from the s states with the oxygen 2p orbitals. Studies were also performed with $ZnRh_2O_4$ [76], NiO [77], [78], NiO: Li [79], $AgCoO_2$ [68] and SnO[44], [80], [81]. Despite the extensive list provided of p-type oxide semiconductors, their application in devices is still, however, quite low.

The only $(n-1)d^{10}sn^2$ ion p-type oxide studied until now was SnO and has receiving more attention as a p-type semiconductor because the VBM is made of pseudoclosed ns^2 orbitals, Sn 5s and O 2p to form hybridized orbitals (see Figure 2.3), reducing the location of the valence band edge and resulting in a more effective hole transport path and higher hole mobility semiconductor with a

better performance applied as a channel in TFTs [44], [81]. TFTs based on p-type SnO_x are expected to fulfil these requirements due to the particular nature of band structure [44]. Contributions from Sn 5s states to valence band maxima (VBM) could offer appreciable hole mobility in this material, without using high processes temperature.

SnO has a specific electronic structure associated with the presence of divalent tin (Sn II), in a layered crystal structure. The origin of p-type conductivity in SnO is mainly attributed to the Sn vacancy and the O interstitial where tin is in Sn^{2+} oxidation state [83].

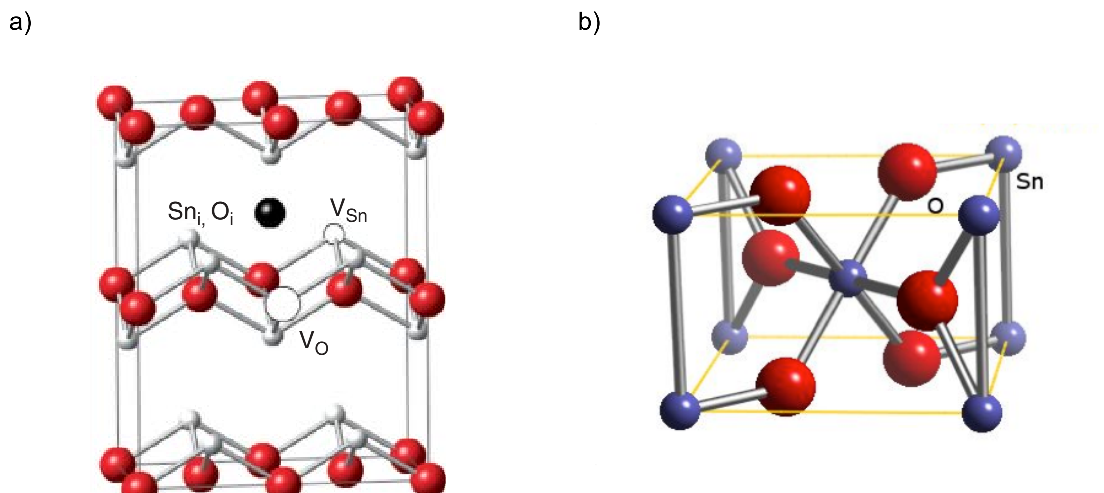

Figure 2.2. Unit cell of a) tin oxide showing the presence of interstitial atoms and vacants of oxygen and tin in the structure and b) tin dioxide structure [84].

Tin oxide is present into two well-known forms: tin monoxide SnO and tin dioxide SnO_2. SnO_2 and doped SnO_2 is a typical functional material with multiple applications, including transparent conducting oxides [85], [86], low emission windows coatings [94] and solid state gas sensing material [87]. The preparation of SnO is relatively difficult, because Sn (II) is readily oxidized to Sn (IV) in the presence of oxygen [84], [88], but due to its technological applications in recent decades, SnO have been used in a variety of applications such as: anode materials for lithium rechargeable batteries [89], [90], coatings [91], catalysts for several acids [92] and precursor for the production of SnO_2 [93]. Several techniques have been adopted in the growth of SnO films on various substrates, including reactive rf magnetron sputtering [44] e-beam evaporation [94], laser ablation [51].

The valence electronic configuration of tin atoms is $4d^{10}5s^25p^2$ and $2s^22p^4$ for oxygen atoms. Oxygen is the most electronegative element, capturing two electrons from tin and giving rise to electronic configuration $2s^22p^6$ for oxygen and $4d^{10}5s^25p^0$ for tin.

Thus, the oxidation state is tin II [25]. In this state, the two 5p electrons are considered to be connected, while the two 5s electrons are a lone pair. SnO has a specific electronic structure associated with the presence of divalent tin, Sn(II), in a layered crystal structure with a Sn-O-Sn sequence and a van der Waals gap between Sn layers of 2.52 Å. Oxygen atoms are tetrahedrally bonded to Sn ones. The Sn atoms are situated at the top of regular square-based pyramids that are based on oxygen atoms with Sn-O distances equal to 2.22 Å [95]. Figure 2.3 a) and b) shows the electronic band structure of SnO_2 and SnO, respectively.

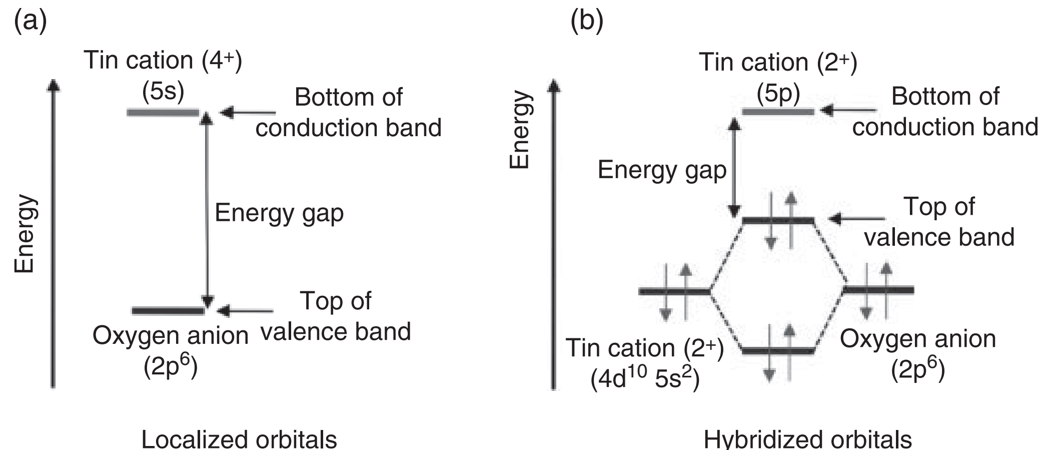

Figure 2.3. Comparison between the band structure of a) SnO2 and b) SnO. [96].

The origin of the p-type conductivity of SnO_x is mainly attributed to Sn vacancies and O interstitials [83], which when fully ionized produces band deformation close to VBM and so, to the formation of acceptor like states, negative charged, located very close to valence band tails. That is, the formation of an energy band level localized close to the top of VBM which, for temperatures above the absolute zero, are partly filled by holes coming from the valence band, according to one of the quasi- chemical stoichiometric reactions [96]:

$$SnO \leftrightarrow Sn^{2+} + 2V_{Sn}^{-} + \frac{1}{2}O_2(1h/V_{Sn}) \tag{2.1}$$

$$SnO \leftrightarrow Sn^{2+} + V_{Sn}^{-} + \frac{1}{2}O_2(2h/V_{Sn}) \tag{2.2}$$

$$SnO \leftrightarrow Sn^{2+} + V_{Sn}^{-} + O_{Sn}^{-} + \frac{1}{2}O_2 + V_O^{+} \tag{2.3}$$

$$SnO \leftrightarrow Sn^{2+} + V_{Sn}^{-} + O_{Sn}^{-}(2h/V_{Sn} + O_{Sn}) \tag{2.4}$$

In general terms, the deviation of stoichiometry, when all possible non-associated native atomic defects are present, can be described by the formula [66]:

$$\Delta x = \frac{[\bar{O}_i] + [\bar{O}_{Sn}] + [\bar{V}_{Sn}] - [\overline{Sn}_i] - [\overline{Sn}_O] - [\bar{V}_O]}{N_O} \quad (2.5)$$

Where

$$\bar{V}_{Sn} = [V_{Sn}^{x}] + [V_{Sn}^{-}] + [V_{Sn}^{2-}] + [V_{Sn}^{3-}] \quad (2.6)$$

and

$$\bar{V}_O = [V_O^{x}] + [V_O^{+}] + [V_O^{2+}] \quad (2.7)$$

are the average total concentration of vacancies in the tin and oxygen sub-lattices, respectively.

N_0 is the number of lattice sites in each sub-lattice per cubic centimeter, which will determine the sub-band gap localization. Here we have to take into account that cation vacancies form more easily than O interstitials in most metal oxides with densely packed structures, where the open spaces surrounded by Sn^{2+} may facilitate the formation of O interstitials [96].

Another approach, is that of acceptor doping the n-type TCOs, has been an ongoing research goal for decades. The advantage of fabricating a p-type SnO_2 is that this material can be easily used to form p–n junctions with their n-type counterparts, increasing the ease of device construction. P-type SnO_2 has become contentious recently with some studies indicating that group 13 dopants will act as shallow acceptors in SnO_2, being In is the most soluble acceptor of the group 15 elements, most probably due to its similar ionic radius to Sn (IV) [97].

Theoretically, the effective substitution of Sn^{4+} by III-family elements (lower valence cations as acceptor impurity) will increase the hole concentration, converting the majority carriers from electrons to holes and, consequently, making SnO_2 p-type conducting [98]–[102]. Experiments were already made in order to obtain p-type SnO_2 by doping with Al, Ga, Li, In, Zn and N for both TCO and gas sensing applications [100], [103]–[109]. Regarding p-type In-doped SnO_2, Ji et al. have achieved a maximum hole concentration of 3.99×10^{18} cm^{-3} with a very low mobility of 3×10^{-3} $cm^2V s^{-1}$ for process temperatures between 600 °C and 800 °C [98].

2.3. Thin-Film Transistors (TFTs)

2.3.1. TFT structure and operation

TFT is a field effect device in which the current is modeled according to the same principle as the MOS transistor [110]. The differences between the two devices are primarily due to the material properties, the thickness of the semiconductor, the conduction mode and the fabrication process. While in MOS transistor, the substrate is an active part of the device, usually monocrystalline silicon, the same does not happen in TFTs, which allows separating elements in an integrated circuit. Despite the advantage mentioned above it is noted that the fabrication process of TFTs is now limited to lower temperatures because the substrate is typically glass or polymeric materials, which allow maximum processing temperatures of around 650 ° C (for glass substrate) whereas the monocrystalline silicon allows much higher process temperatures [110].

This current modulation, known as field effect, relies on the capacitive injection of carriers close to the dielectric/semiconductor interface, which is turned possible due to the parallel plate capacitor structure formed by the gate electrode, dielectric and semiconductor [111].

The basic principle of MOS transistor was proposed and patented in 1930 by Lilienfeld. Due to the lack of vacuum and others technological equipment, the production of this device was not possible and this first report is actually a concept patent.

Figure 2.4 shows a schematic drawing of the transistor, as shown in the patent. The technological limitation of time refers to the lack of control of the high density of surface states and charges the semiconductor. This high density of surface states produced a semiconductor shield, thereby preventing a modulation of carrier density, this is, of the conductance between the source and drain contacts for the gate voltage.

Finally, only in 1960, the first TFT was produced by Weimer at the RCA Laboratories in 1962 [112]. Weimer used a vacuum technique (evaporation) to deposit gold electrodes, a polycrystalline cadmium sulfide (CdS) n-type semiconductor and a silicon monoxide insulator, using shadow masks to define the patterns of these layers.

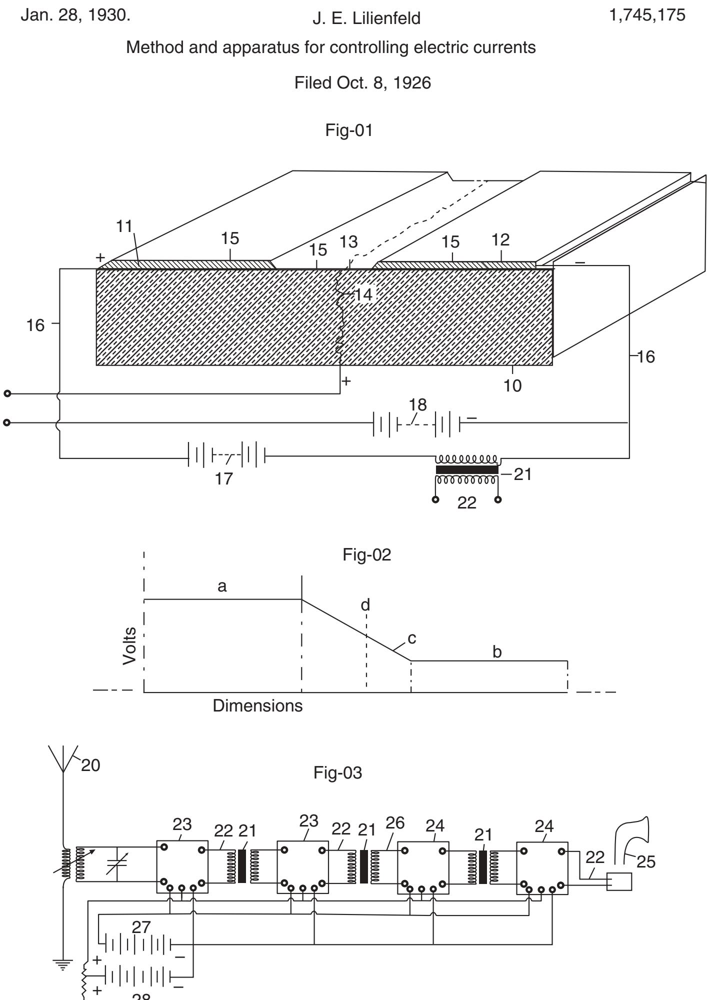

Figure 2.4. Reproduction of the patent nº 1,745,175, granted to the physicist J.E. Lilienfeld by the US Patent Office in January [7]

A TFT consists in an insulator layer, inserted between the gate electrode and the semiconductor, three electrodes, gate, source and drain and one semiconductor placed between the source and drain electrodes, wherein a channel is formed by applying a potential between the source and drain electrodes and at the gate electrode [113], [114].

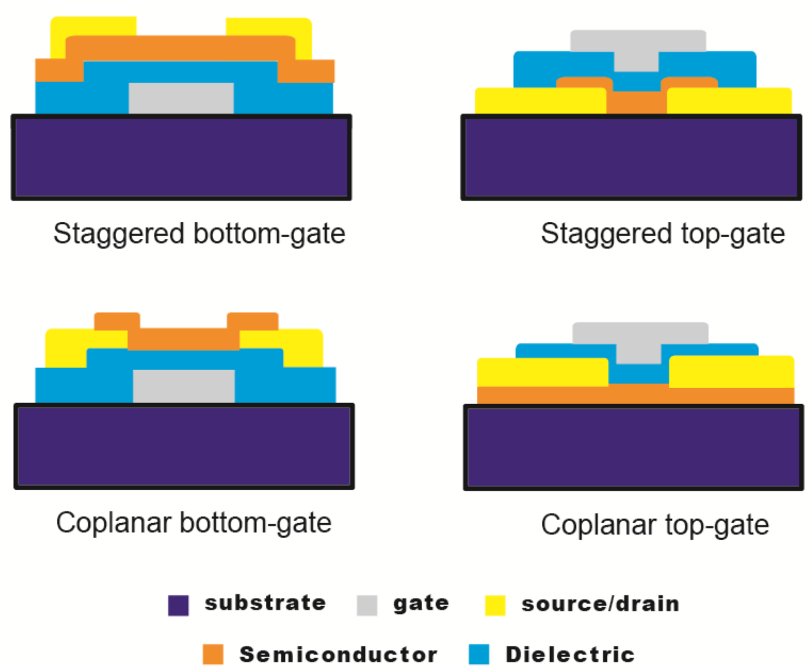

Figure 2.5. Schematics showing some four general TFT structures.

Figure 2.5 shows four possible TFT device structures. The devices can be either staggered or coplanar. In a coplanar configuration, the source and drain contacts and the insulator are on the same side of the semiconductor, the source-drain contacts are in direct contact with the induced channel. In a staggered configuration, the source and drain contacts are on the opposite side of the semiconductor from the insulator, there is no direct connection to the induced channel. Inside staggered and coplanar structures, TFTs can be classified as bottom-gate (inverted) or top-gate (normal) devices. A bottom-gate TFT, has the gate insulator and gate electrode located beneath the semiconductor. A top-gate TFT has the gate and insulator located on top of the semiconductor. In a top-gate device, the semiconductor is covered by a gate insulator, so that the top surface is inherently passivated. Regarding this work, p-type oxide semiconductors were produce and applied as active layer in thin film transistors. The follow explanations about TFT operation will be done considering this fact. The behavior of n-type TFTs is similar, only the sign of the polarizations is the opposite and the majority carriers are electron instead of holes.

If no voltage is applied to the gate electrode (V_{GS}), the free carriers are homogeneously distributed in the semiconductor layer. If the semiconductor has a low density of charge carriers, then the conductivity in the active layer is very low as well as the current between the source and drain electrodes resulting from the application of an electric field between them [110], [115]. This state is called off state and the resulting current is called off current (I_{DSoff}) (Figure 2.6 a).

When a negative voltage is applied to the gate electrode, an excess of majority carriers, holes in this case, is attracted to the surface of the p-type semiconductor, near the interface with the dielectric. The charge density of this thin layer increases, thereby creating a conductive channel between the source and the drain. By applying an electric field between the source and drain electrodes (V_{DS}), results in a flow of current between them. This current is called on current (I_{DSon}) because the device is at on state (Figure 2.6 b) [116].

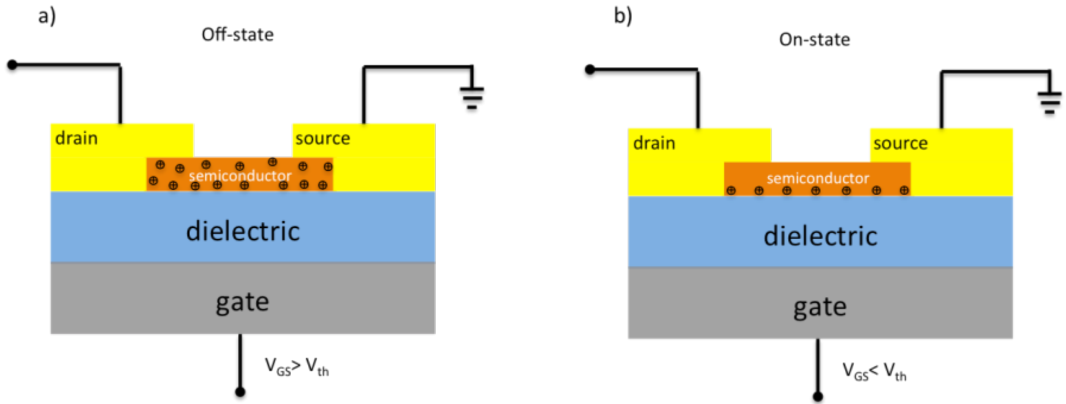

Figure 2.6. Schematics of a TFT in the a) off-sate and b) On-state

Figure 2.7 describes the ideal operation of a TFT (p-type) by analyzing the energy band diagram of the capacitor comprised by the gate electrode, dielectric and semiconductor, upon the application of different voltages in the gate electrode, where the gate material has a work function smaller than the ionization potential of the semiconductor. Basically, three cases may exist at the semiconductor surface when the capacitor is biased with positive or negative voltages. When a negative voltage is applied to the gate electrode (Figure 2.7 a), the valence band edge, E_V, bends upward near the surface and is closer to Fermi level and the semiconductor/insulator interface has an accumulation of holes (a channel has formed), since the carrier density depends exponentially on the energy difference (E_F-E_V). This is called the accumulation case. When a positive voltage is applied (Figure 2.7 b), the bands bend downward, and the majority carriers are depleted (depletion case) and when a larger positive voltage is applied (Figure 2.7 c) the band bends ever more downward so that the intrinsic level E_i at the surface crosses over the Fermi level E_F (inversion state) and the number of electron at the surface is larger that the number of holes.

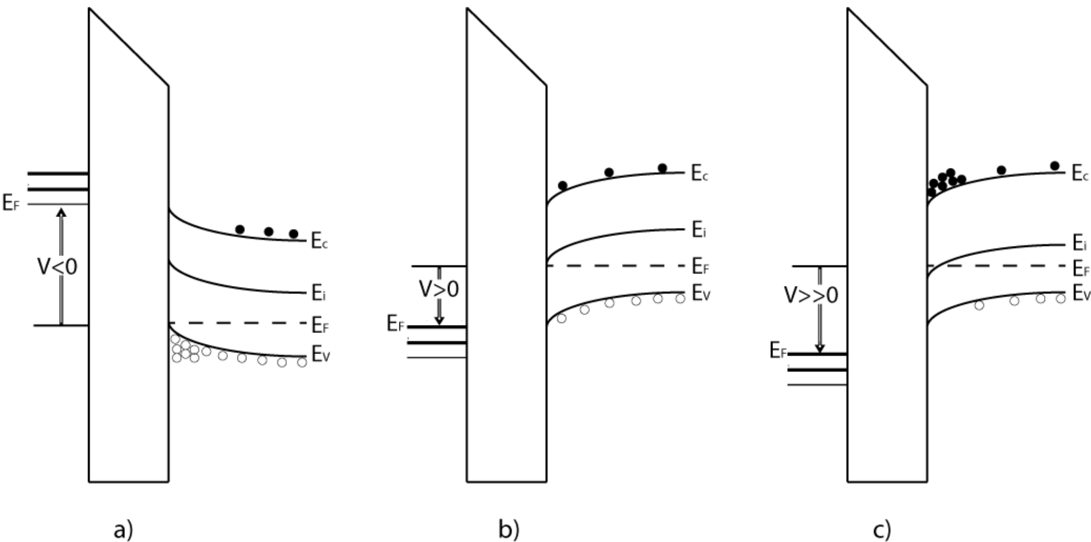

Figure 2.7. Energy band diagrams for TFT gate region where φm < φs: (a) accumulation, (b) depletion and c) inversion modes [115].

P-type TFTs can operate in enhancement or depletion mode, depending V_{th} is negative or positive. For TFTs that operate in enrichment mode, the conductivity of the channel for a zero bias gate voltage is zero (off-state) and it is required a negative gate voltage to put the device at on-state. For a device that operates in depletion mode, the device is already on even without a gate voltage being applied and is necessary to apply a V_{GS} to achieve the off-state. Depletion mode devices are less desirable because they require more energy to keep the device off [110].

2.3.2. TFT operation

As stated above, when applying a negative voltage V_{GS}, the field effect transistors, where the active layer is a p-type material, operate in accumulation mode and the charges accumulated are holes. Depending on the voltage applied between the drain and source electrodes there are two regimes of operation of the transistor: the linear and the saturation regime [110].

When $V_{DS} < V_{GS} - V_{th}$, the current I_{DS} increases linearly with V_{DS} (linear range) and it is calculated by the following equation [114]:

$$I_{DS} = \frac{WC_i}{L} \mu_{FE} \left((V_{GS} - V_{Th})V_{DS} - \frac{{V_{DS}}^2}{2} \right) \quad \textbf{(2.8)}$$

where L is the channel length, W is the channel width, C_i is the areal dielectric capacitance, V_{th} is the threshold voltage and μ_{FE} is the field effect mobility.

When $V_{DS} \geq V_{GS} - V_T$, the free carriers near the drain region decrease leading to the saturation of IDS (pinch-off phenomenon). In the saturation regime, I_{DS} can be expressed by

$$I_{DS} = \frac{WC_i}{L} \mu_{SAT} (V_{GS} - V_T)^2 \quad \textbf{(2.9)}$$

Figure 2.8 a) and b) shows the output and transfer characteristics curves of a typical p-type oxide based TFT, respectively. In output characteristics, I_{DS} is measured as a function of V_{DS} for different V_{GS} values. From the output curves it is possible to obtain qualitative information such as the V_{DS} and V_{GS} range needed so the active layer is fully depleted, observed by the flatness of the I_{DS}-V_{DS} curves at the pos-pinch-off regime and also if there is a degradation of the mobility that can be indicated by a decreasing separation between I_{DS}-V_{DS} curves when increasing V_{GS} [111].

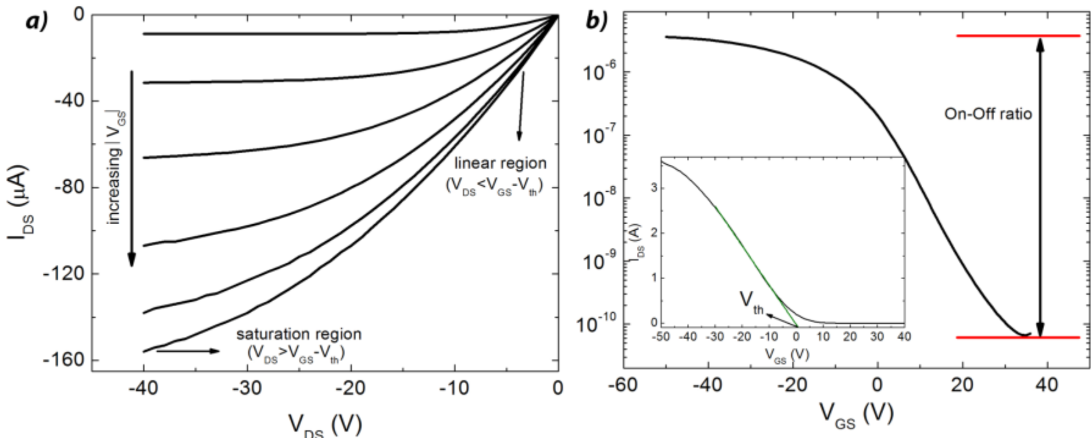

Figure 2.8. Typical (a) transfer and (b) output characteristics of a p-type oxide semiconductor based TFT.

Transfer curve is obtained by measuring I_{DS} as a function of V_{GS} keeping V_{DS} constant. From transfer curve several electrical parameters can be calculated, as following:

- *Threshold voltage (V_{th})*

Threshold voltage corresponds to the V_{GS} for which an accumulation layer or conductive channel is formed close to the dielectric/semiconductor interface. V_{th} can be calculated at low V_{DS} (linear regime) doing a linear extrapolation of the I_{DS}-V_{GS} plot or at high V_{DS} (saturation regime) extrapolated from $I_{DS}^{1/2}$-V_{GS} plot.

- *Effective mobility (μ_{eff})*

Effective mobility can be estimated at low V_{DS} by the conductance of the device, given by [117]

$$g_d = \left(\frac{\partial I_D}{\partial V_{DS}}\right) = \mu_{eff} C_i \frac{W}{L}(V_{GS} - V_T) \quad \textbf{(2.10)}$$

obtaining

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L}(V_{GS} - V_T)} \quad \textbf{(2.11)}$$

- *Field effect mobility (μ_{FE})*

Field effect mobility is obtained at linear regime from the transcondutance (g_m). The transcondutance is defined as

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)\Bigg|_{V_{DS=cte}} \quad \textbf{(2.12)}$$

by differentiating equation (2.1) as a function of V_{GS} comes

$$g_m = \mu_{FE} C_i \frac{W}{L} V_{DS} \quad \textbf{(2.13)}$$

and μ_{FE} is given by

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_{DS}} \quad \textbf{(2.14)}$$

- *Saturation mobility (μ_{SAT})*

At saturation regime, g_m can be obtained by differentiating $\sqrt{I_{DS}}$, from equation (2.2) as a function of V_{GS}

$$g_m = \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}}\right)\Bigg|_{V_{DS=cte}} = \sqrt{\frac{1}{2}\mu_{SAT} C_i \frac{W}{L}} \quad \textbf{(2.15)}$$

where μ_{SAT} is given by

$$\mu_{SAT} = \frac{\left(\frac{\partial\sqrt{I_{DSAT}}}{\partial V_{GS}}\right)^2}{\frac{1}{2}C_i\frac{W}{L}} \quad \textbf{(2.16)}$$

The field effect mobility is usually lower than the effective mobility, because the dependence of mobility on electric field is neglected trough g_m. The major differences can be often observed between the mobilities calculated from linear and saturation regions. μ_{EF} can be affected by problems from source and drain contacts and in such cases there are deviations regarding the linearity of I_{DS}-V_{DS} curve, underestimating the value of μ_{FE}. For saturation regime, when channel width as the same dimension of dielectric thickness, I_{DS}-V_{DS} curve don't show saturation and exhibiting high values leading to incorrectly high values of μ_{SAT}.

- *Subthreshold slope (S)*

Subthreshold slope is defined as the V_{GS} needed to increase I_{DS} by one decade and is given by the inverse of the maximum slope of the transfer characteristic.

$$S = \left(\frac{\partial V_{GS}}{\partial(logI_{DS})}\right) \quad \textbf{(2.17)}$$

While high μ_{FE} affords high saturation current and fast switching speed between on/off states, low *SS* values and high On-Off ratio values indicate efficient and effective modulation of I_{DS} with V_G, and V_{th} close to zero ensures low power consumption.

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Chapter 3.Thin films and devices: Deposition and *Characterization Techniques*

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3. THIN FILMS AND DEVICES: DEPOSITION AND CHARACTERIZATION TECHNIQUES

This chapter summarizes relevant techniques involved for the production and characterization of thin films and devices. In this thesis, sputtering was adopted to produce the oxide semiconductors. Characterization of electrical, optical, morphological, compositional and structural properties was carried out by using a variety of techniques, whose main feature will be outline in the following sections.

3.1. Thin-film and TFT processing

3.1.1. Sputtering

The sputtering technique is a physical vapor deposition (PVD), which involves the condensation of compounds in the gaseous phase to form solid materials, usually in the form of a thin film deposited on a substrate. In this process, the material is a solid target which is progressively removed by bombardment of energetic ions forming a gas plasma at low pressure [1]. This phenomenon was firstly observed by Grove and Plucker in 1852 [2], [3]. These two researchers found that during an electrical discharge between two conductive electrodes, in a gaseous atmosphere at reduced pressure, the cathode surface was sputtered by energetic ions from the gaseous discharge, and the material that the cathode was made of, was deposited on the surface of the anode and of the tube walls in the form of a thin coating.

Only about a hundred years later this phenomenon started to be developed and studied for the production of thin films. In 1938, Berghaus developed the first processes of physical vapor deposition [4], but it was only in the 60s that the ionic deposition began to be developed by Mattox [5], consolidating high expectations around these PVD techniques based on vacuum systems.

With the advancement of technological revolution vacuum systems, power supplies, amongst others, were developed to optimize the quality and low cost production of coatings. Currently there are dozens of variations of this basic process in laboratories around the world. The reactive sputtering technique is one of the most versatile techniques for the production of thin films, since it facilitates the transition of laboratory work to the industry.

When the target is bombarded with energetic particles such as accelerated ions, atoms from the target surface are ejected [6], [7]. This technique for the production of films consists basically of two processes: ejection of atoms or clusters of atoms of the material constituting the target and the deposition (in solid phase) on a substrate (Figure 3.1).

If the energy transferred by the incident ion energy is higher than the normal bonding energy of the material, it is possible to eject surface atoms.

The thin film of the material to be deposited is then obtained by accumulation of the sputtered atoms on a substrate placed in front of or slightly off-center relative to the target. The reactive sputtering is performed inside a high vacuum chamber in which gas is admitted, inert at low pressures (typically argon). The target is connected to the negative voltage source and the substrate holder forms the anode (Figure 3.2) [8]. By applying an electric field or by using a heating filament, electrons are released colliding with gas atoms resulting in the formation of Ar^+ ions and a potential difference is established in this area. Ar^+ ions are accelerated and collide with the target, resulting from this collision the release of several kinds of particles: atoms (or clusters of atoms) of the material constituting the target, secondary electrons and charged atoms. The neutral atoms ejected with high kinetic energy end up being deposited on a substrate placed in front of the target. The secondary electrons are accelerated and may give rise to new Ar^+ ions by collision with argon atoms.

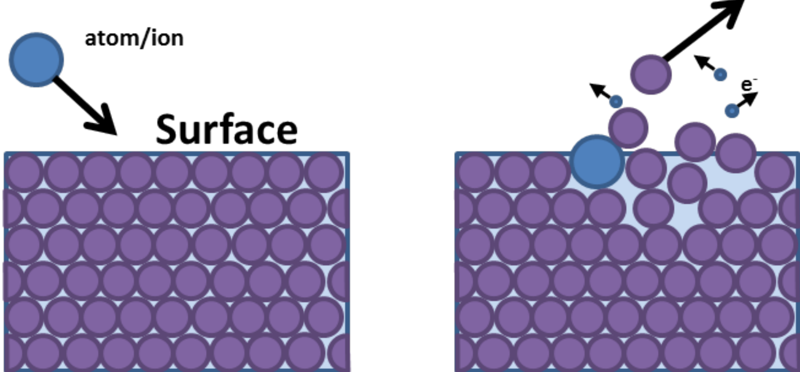

Figure 3.1. Scheme of an atom ejected from the target by an energetic ion [9].

One of the most important parameters to characterize this process is called the sputtering efficiency, defined as the number of atoms ejected from the target surface by incident ion (Figure 3.1). The main issues that influence sputtering efficiency are the material, and its structure and composition the characteristics of the incident ion and the geometry within the deposition chamber.

However, it should be noted that there is a threshold energy of the incident ions, below which no material will be ejected from the target. With the increase of ions energy, the sputtering rate increases linearly reaching a maximum, from which it slowly decreases, showing that the mean free path of the existing species in the plasma have an important role.

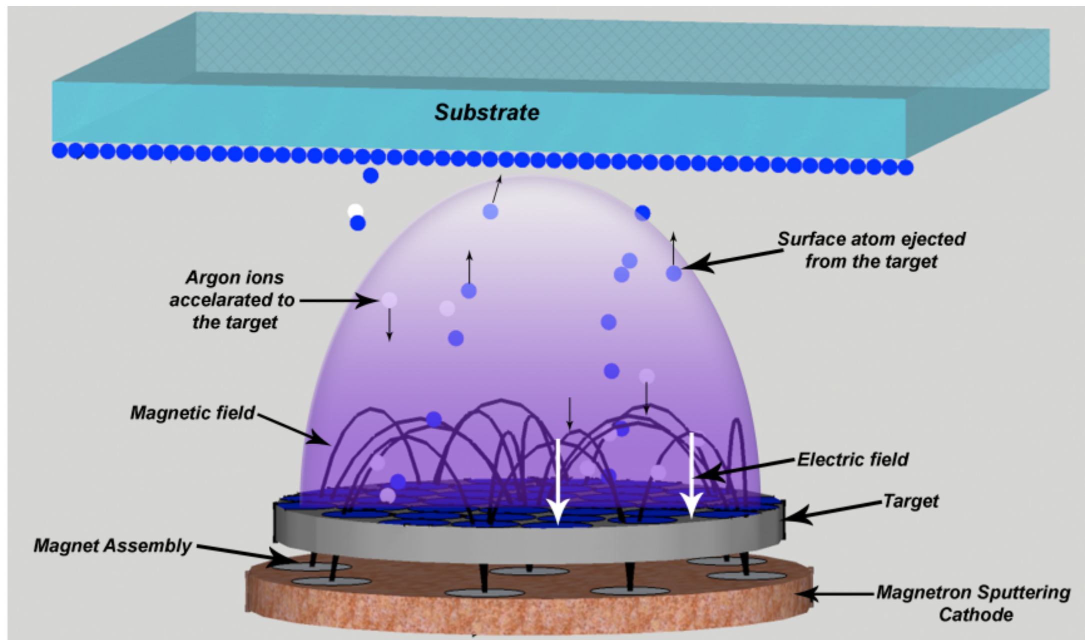

Figure 3.2. Interior of a sputtering deposition chamber. In this scheme an energetic ion energy (Ar^+) collides on the surface of the target, ejecting atoms.

The reactive sputtering efficiency is increased by placing the target over a magnetron with an appropriate geometry (Figure 3.2). C.J. Overbeck reported the deposition of compounds by sputtering in a reactive gas ("reactive sputter deposition") in 1933 for use as optical coating [10] and in 1936 F.M. Penning proposed the "crossed field" (electric and magnetic) electron trap to enhance plasmas in sputtering from cylindrical-hollow (inverted) magnetrons and cylindrical-post magnetrons [11]. One of the problems of the sputtering technique is on the one hand the requirement of very low working pressures within the deposition chamber to minimize the collision process between species and on the other hand, the working pressure must be high enough to allow ion bombardment necessary to maintain the plasma. Reactive magnetron sputtering technique reduces this problem because it leads to a more efficient ionization at low pressures.

For a planar magnetron system, the planar cathode lays on permanent magnets in an appropriate geometry, resulting in a toroidal field with closed field lines over the surface of the target (cathode). The technique is then called magnetron sputtering. The plasma confinement leads to higher deposition rates, allows the system to work at lower gas pressures, as well as the use of lower voltages on the target. Nevertheless, when the target material is isolating the technique of sputtering fails because when the established electric field within the chamber is stationary, it is possible to sputter only materials with high electrical conductivity or an accumulation of charges on the target occurs (the potential grow on the surface of the material) leading zero potential preventing the continuation of the sputtering process.

The application of a high frequency alternating voltage to the target, radiofrequency (rf) sputtering with a typical frequency of 13.6 MHz, allows bombard its surface with electrons with an interval time of half cycle, canceling the charge accumulated in the preceding half cycle. This technique of rf sputtering allows the use of insulating targets, and thus allows with one equipment, to deposit films from conductors, semiconductors and insulating targets.

There are numerous advantages of the technique of reactive sputtering, including:

- *Good adhesion of the film to the substrate due to the plasma ability to preheat the substrate by energetic ions and also due to the neutral bombardment of the substrate surface.*
- *The ability to work at very low pressures allowing the deposition of high purity materials.*
- *The temperature during deposition is relatively low. The direct ionization of the atoms of the material to deposit provides benefits previously achieved only on heated substrates.*
- *Processes such as gas dispersive effects and the ability to rotate or move the samples relatively to the source during deposition allows the thickness uniformity of the films.*
- *Control of the films structure. Sputtering promotes epitaxial growth and increases the atomic mobility.*

To deposit the p-type thin films developed at this work, a radio frequency magnetron sputtering, AJA, Model ATC ORION8 RF magnetron sputtering system (AJA International, Inc., North Scituate, MA), existing at CEMOPs clean room at New University of Lisbon Faculty of Sciences and Technology was used (Figure 3.3).

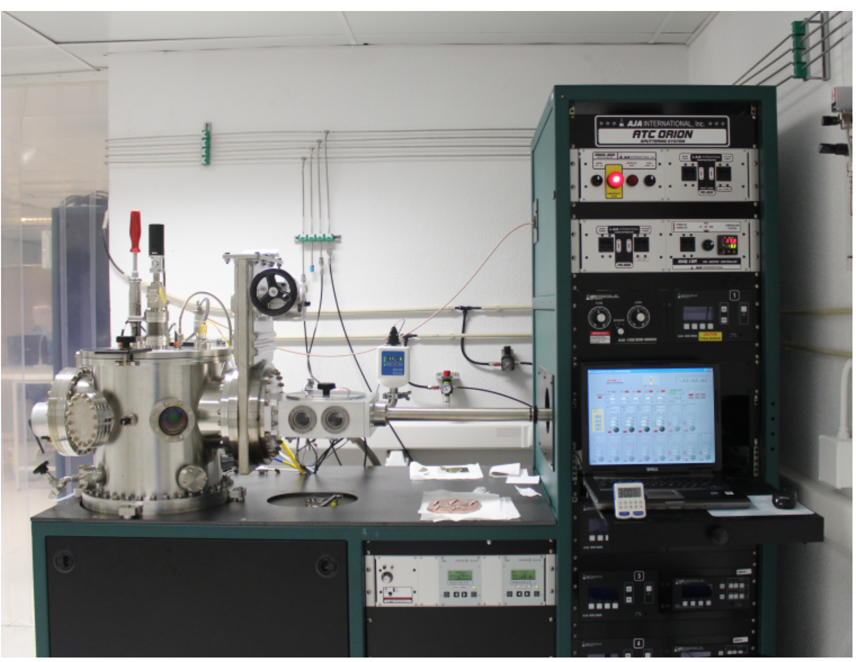

Figure 3.3. Radio frequency magnetron sputtering existing at CEMOPs clean room at New University of Lisbon Faculty of Sciences and Technology.

This system consists of three magnetrons, which enables the deposition of three different materials simultaneously. The substrates holder is on top of the targets and is prepared to support substrates up to 10 × 10 cm^2.

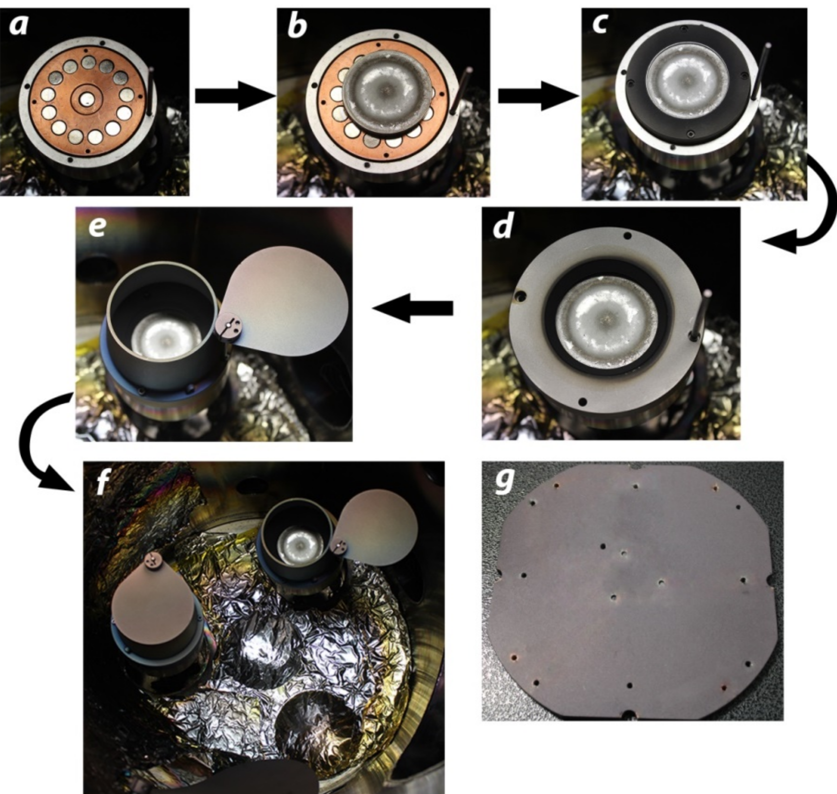

Figure 3.4. Assembly of the target into the magnetron (a to e), f) interior of the deposition chamber and g) substrate holder.

3.1.2. Electron beam physical vapor deposition

The electron beam deposition technique is also a physical vapor deposition technique of thin films. The process is very simple and consists in heating the material to be deposited at a temperature in which its pressure should be high enough, so that the particles diffuse from the source to the remainder of the chamber where they are confined. As in the sputtering technique, the evaporation temperature is very low due the fact that the system has a much lower pressure than the atmospheric, generally about 10^{-4} to 10^{-5} Pa. There is a flow of material from the source to the substrate and it is important that the residual gas inside the chamber is sufficiently low so that the mean free path of the particles is much higher than the source-substrate distance.

It is necessary that the kinetic energy corresponding to the component perpendicular to the surface is higher than the energy required to maintain the intermolecular forces, for a molecule to leave the surface of the material. Since the substrate surface temperature is lower, the particles would condensate and form the film. A good vacuum system is necessary to ensure the purity of the deposited material [12].

Since the film thickness is an essential parameter in the device production, its uniformity study of regarding the characteristics of the sources is of great importance. The growth rate using a flat source is given by [8]:

$$Rc = \frac{m}{\pi \rho r^2} \cos\phi \cos\theta \ \ (cm/s) \tag{3.1}$$

where ϕ is the angle measured from the normal to the source plane, θ is the angle of the substrate relative to the vapor flow, ρ is the density (g/cm^3) and *m* is the weight evaporative rate (g/s) of the deposited material.

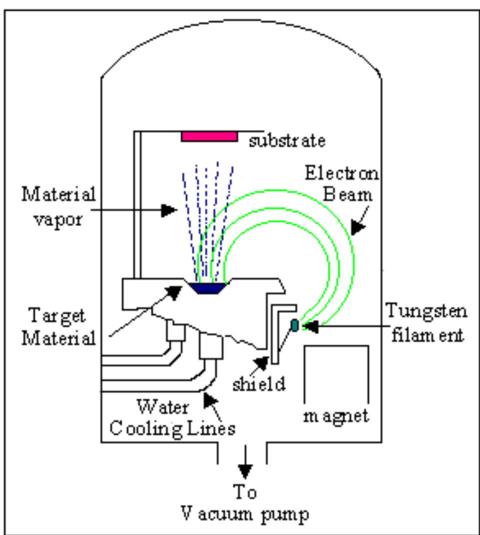

Figure 3.5. Simplified schematic of the process of electron beam evaporation scheme [13].

This type of system was used to deposit the double layer Ni/Au used as source and drain electrodes on the thin film transistors produced and consists on a high vacuum chamber, a vacuum system, a production and electron beam focusing system to heat the material, and a thickness and electron beam current measurers. The vacuum system consists of two types of pumps: a mechanical pump that allows reaching primary vacuum of 10 Pa in the deposition chamber, and a molecular turbo pump, allowing to reach a final pressure of 10^{-3} Pa inside the deposition chamber.

There are also two pressure measures, a Pirani type (which measures the pressure to the lower limit of 10^{-3} Pa) and another of Penning measuring the lower pressures inside the chamber, allowing the control of the pressure inside the deposition chamber. A fully automated process via a quartz sensor controls the deposition rate of the films.

Figure 3.5 shows a simplified schematic of the evaporation process and in Figure 3.6 a picture of the equipment used existing at CEMOPs clean room at New University of Lisbon Faculty of Sciences and Technology.

Figure 3.6. Picture of the electron beam deposition system existing at CEMOPs clean room at New University of Lisbon.

In order to reach the material to evaporate, the electron beam is deflected e focalized by a magnetic field. Is the electron beam is accelerated with an appropriate voltage (usually between 5 and 150 kV), it is capable of heating several materials reaching to its fusion point or causing its sublimation and consequently its evaporation. The pressure inside the chamber should be lower than 10^{-1} Pa so the electron beam could exist and be controlled. Above this value several undesirable effects could occur, such as discharges and electronic captures leading to a strong instability of the electron beam and thus precluding its use.

The main parts that constitute an electron beam evaporator are: a tungsten filament, a cathode heated by electric current passage, a Wehnelt cylinder for focusing the beam, an anode, and

some elements for magnetic deflecting and focusing, a crucible containing the material to evaporate and high-voltage generators of the cathode and anode.

The material to be evaporated is placed in a crucible, usually made of copper or graphite which is cooled with water. This scheme is illustrated in Figure 3.7 and in Figure 3.8 we can see its picture.

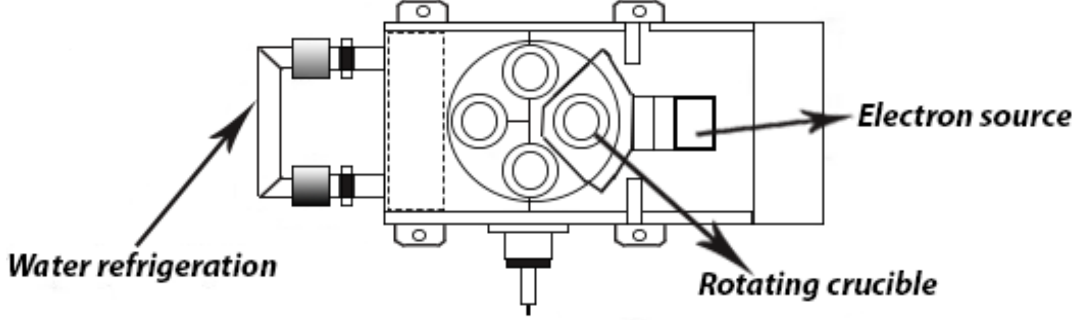

Figure 3.7. Rotating crucible with four compartments of the electron beam evaporator. Adapted from [13].

The main focus of this technique is that only a small portion of the evaporation material melts or sublimates, and thus there is no contamination of the crucible material in the film. This does not occur with other evaporative deposition techniques, such as resistive thermal evaporation, where the main disadvantages are the possible contamination of the crucible material, beside the limitation of working with relatively low evaporation temperatures.

Figure 3.8. Picture of the electron beam evaporation crucible unit.

3.1.3. Post-deposition annealing

Post-deposition annealing plays an important role on the electrical, optical and structural properties of the thin films and devices, since it can promote the concentration of oxygen vacancies and/or the crystallization of initially amorphous structures. In this work, thermal annealing in air atmosphere is selected as the post-deposition technique performed with temperatures ranging from 100 °C to 400 °C with heating ramps of 10 °C min^{-1}, maintaining the desired temperature during 1 h and removing the samples only after cooling down below 60 °C.

The annealing treatments were performed using a hot plate Torrey Pines existent in CEMOP's clean room, at New University of Lisbon.

Figure 3.9. Picture of the hot plate used to perform thermal annealing of thin films and devices.

3.1.4. Photolithography

Photolithography was used as a pattering technique for the fabrication of thin film transistors. Lithography process is widely used in microelectronics for defining patterns or structures on different substrates. In this technique, a photosensitive polymer (photoresist) is sensitized when exposed to ultraviolet radiation.

Since the maximum spectral sensitivity of the photoresist in such processes is in the near ultraviolet and part of the visible blue spectrum (from 320 nm to 460 nm), an environment yellow light has to be used, in order to block the photons with wavelengths shorter than 500 nm. This process has to be done in a controlled environment of humidity, pressure, temperature and inside a clean room whose number and size of particles is reduced not compromising the performance of the final device.

Photoresist is composed by resins, photosensitive compounds and a solvent, being the latter responsible for the mechanical properties of the photoresist such as viscosity. One of the categories in which photoresist can be divided is related to their polarity:

1) *Positive – allows patterning on the substrate the same pattern as in the lithographic mask.*
2) *Negative – allows patterning on the substrate the inverse pattern of the lithographic mask.*

Regardless the type of photoresist to be used, it must exhibit good adhesion to the substrate, high resolution, uniformity over the entire surface, high sensitivity, high chemical purity and proper viscosity.

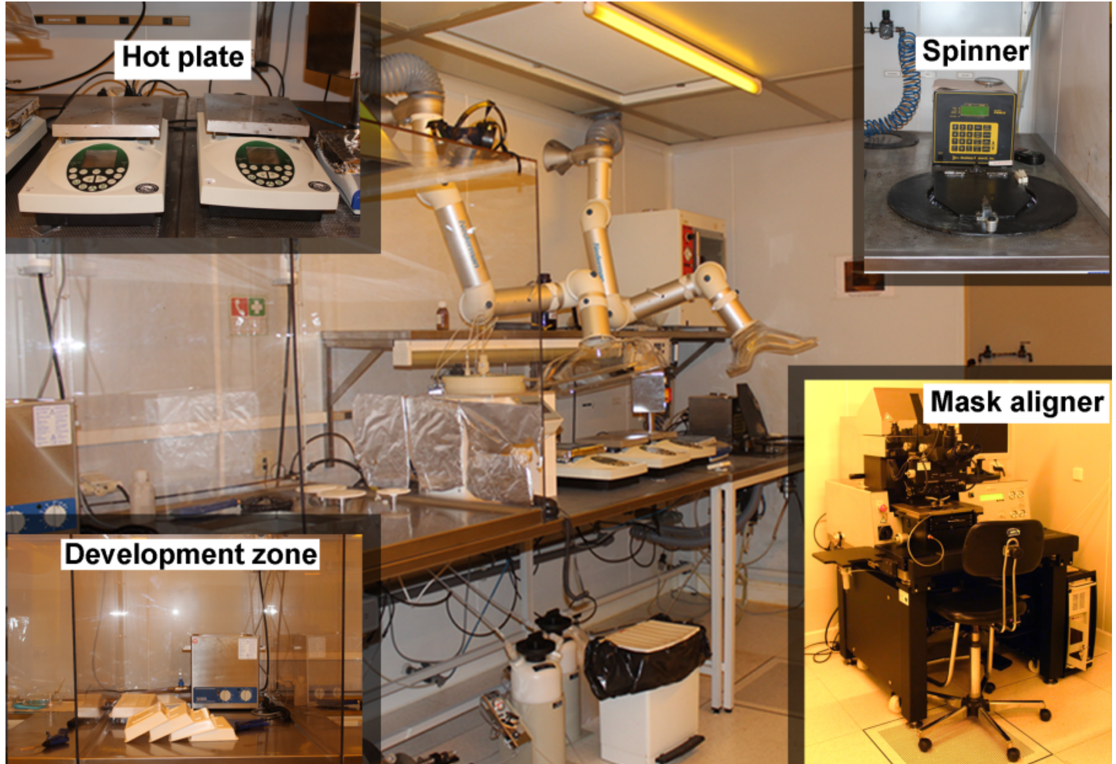

Figure 3.10. Picture of the yellow zone existing at CEMOP's clean room.

Typically, photoresist is applied in liquid form. There are several methods for its application, such as Spraying, Dip coating and Spin coating being the latter the most commonly used and also the process used at this work. The substrate is fixed by vacuum in the center of a rotating disc, spinner, *PWM32* da *Headway Research, Inc* (Figure 3.10)*)*. Then, a few drops of photoresist are applied in the center of the substrate and the disc is set to rotate at high speeds between 2500 and 5000 rpm, in order to promote the spreading of photoresist over the substrate surface. The thickness of photoresist depends on its viscosity, and is inversely proportional to the square root of spinning speed by the equation:

$$d_{ft} = \frac{K \times P^2}{\sqrt{w}} \quad \textbf{(3.2)}$$

d_{ft} – photoresist thickness [μm];

K – spinner/substrate constant [μm min-1/2];

P – percentage of solids on photoresist [%];

ω – spinner rotational velocity [rpm]

The spin-coating process generally comprises two stages, one at lowest speed which serves to spread the photoresist across the substrate and another are used at higher speed to adjust the final thickness of the photoresist.

Figure 3.11 illustrates the main steps of conventional photolithographic process. Within this research work, an AZ6612 positive photoresist was used. After spin-coating the photoresist, the substrate is placed in a hot plate 100-115 °C during 1m15s in order to improve the adhesion of photoresist and reduce its solvent content (*softbake*). This process is extremely important, because if the solvent is not properly removed, some undesirable phenomena can occur such as reduced thermal stability in subsequent process steps or lack of definition of the resist structures [14].

After the spin-coating and softbake processes the substrate is placed in a mask aligner, Karl-Suss MA6 (Figure 3.10), in order to do the mask alignment and UV exposure processes. After the exposure to UV light if, the photoresist is positive, the exposed areas become more soluble, since UV radiation breaks its chemical bonds and subsequent reduces the molecular weight of the polymer. If the photoresist is negative, the exposed areas become less soluble as the UV promotes cross-linking between the polymer chains, increasing the molecular weight. For AZ 6612 photoresist, when it is exposed to UV-light, its photoactive compound, DiazoNaphtoQuinone- (DNQ-) sulfonate, loses a nitrogen molecule, being converted into indene carboxylic acid by incorporating a water molecule. Since the photoresist regions where this photoreaction happens have a much higher alkaline solubility than the unexposed regions, when the substrates are introduced in a suitable developer the desired patterns can be obtained in the photoresist.

For the AZ6612 photoresist, a metal ion free developer, AZ 726 MIF, primarily composed by tetrametil ammonium hydroxide is used. The result is a photoresist structure with the negative of the desired final pattern. After these steps, the thin film is deposited and then a photoresist stripping step is necessary to remove the photoresist and the film deposited on top of it.

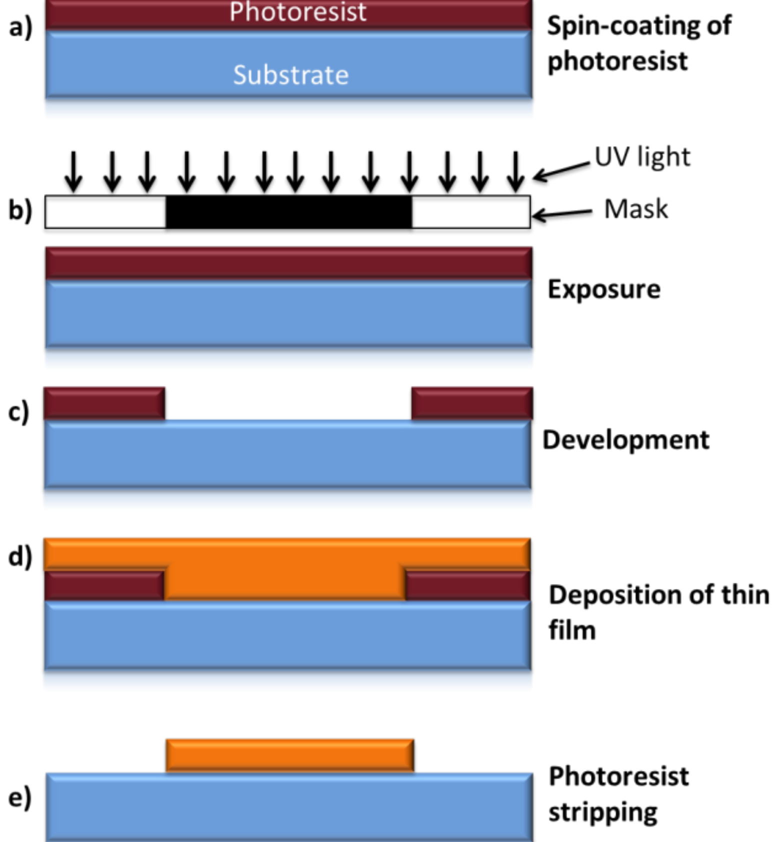

Figure 3.11. Process flows showing the main steps of conventional photolithography.

3.2. Thin film characterization techniques

The thin films produced within this thesis were characterized using optical, structural, morphological and electrical characterization techniques described in this sub chapter.

3.2.1. Profilometry

To make sure that the thin films produced satisfy the specified technological demands a wide field of characterization, measurement and testing methods are available. The physical properties of the thin films and consequently of the devices produced are highly dependent on their thickness. Thus, the determination of the film thickness and of the deposition rate is a fundamental task in thin film technology. The thin films thickness was obtained using Ambios XP-200 profilometer existing at CENIMAT at New University of Lisbon (Figure 3.12).

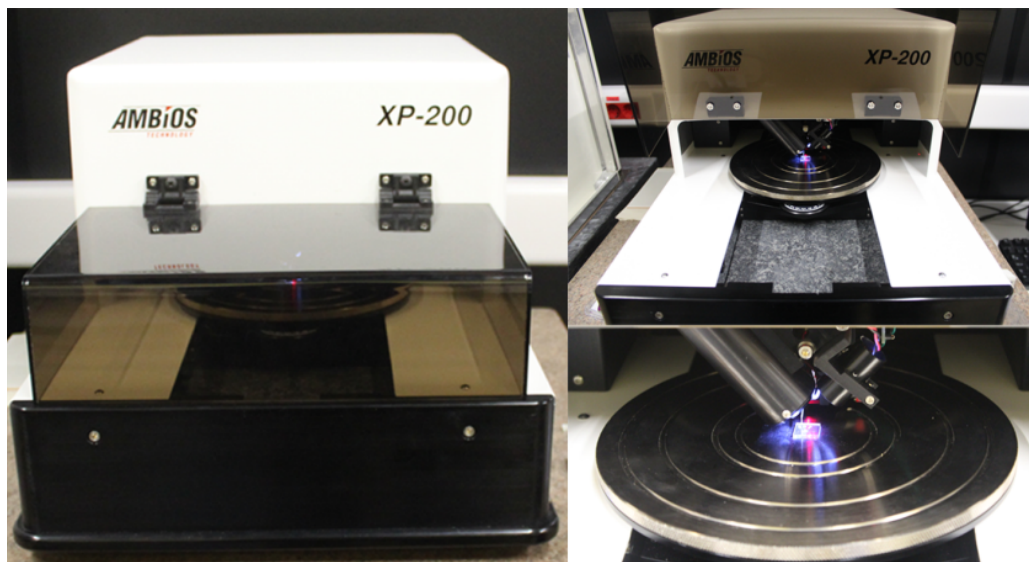

Figure 3.12. Picture of Ambios XP-200 existing at CENIMAT.

In order to measure the thickness, the film has to exhibit a step on a plane substrate. A diamond stylus is pulled along the surface at constant velocity and the step height is measured by a pick-up system. Prerequisite for an exact measurement are a suitable hardness of the film and a plane substrate. A typical measurement is illustrated at Figure 3.13.

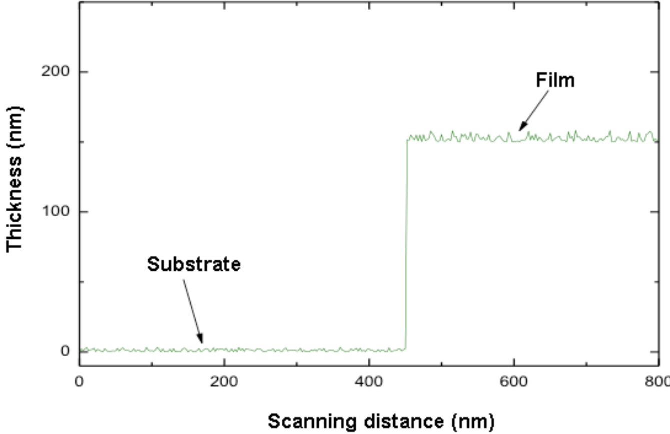

Figure 3.13. Typical step height corresponding to a 150 nm film thickness deposited on a glass substrate.

Knowing the film thickness and the deposition time, it is possible to calculate the growth rate with the formula:

$$Rc = \frac{d}{t} \quad \mathbf{(3.3)}$$

3.2.2. Electrical characterization

3.2.2.1 Hall-effect measurements

Hall effect is usually used to characterize conductor and semiconductor material, since it allows, determining the type of carriers, carrier concentration and mobility of the material. Using the Hall effect system Biorad HL 5500 with a constant magnetic field of 0.5 T, existing at CENIMAT (Figure 3.14) it was possible to determine the electrical resistivity, mobility, and carrier concentration of the films produced and also the majority charge carrier type (n or p-type).

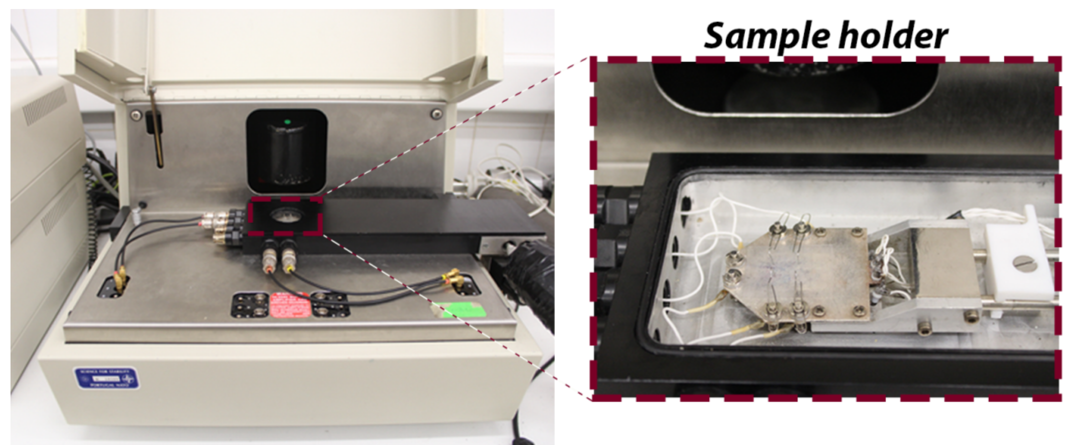

Figure 3.14. Biorad HL 5500 Hall effect system existing at CENIMAT, New University of Lisbon.

The Hall effect was observed for the first time by E. H. Hall in 1880 and consists in the appearance of an electric field called Hall field E_H, due to the deviation of the charge carrier trajectories by an external magnetic field. If a semiconductor with the shape of a rectangular bar in which an electric current circulates, is placed in a magnetic field perpendicular to the current, an electromotive force perpendicular to the current appears - referred to as the Hall voltage V_H (Figure 3.15).

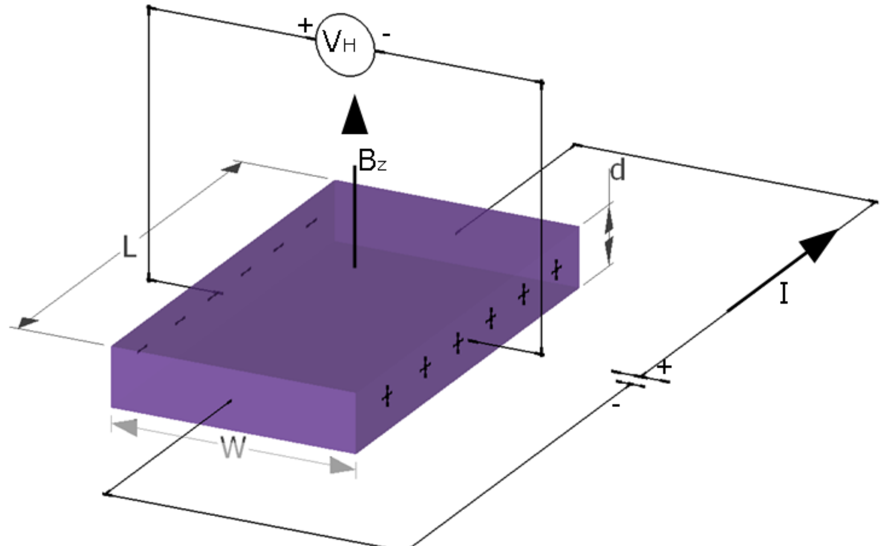

Figure 3.15. Illustration of the experimental setup allowing the observation of Hall effect.

This phenomenon is due to the Lorentz force in which the charge carriers that cause a current flow through the film are bent by the magnetic field depending on their charge signal (type) and mobility. When the magnetic field is moderate, the Hall voltage can be given by:

$$V_y = V_H = \frac{R_H I_x B_z}{d} \quad \textbf{(3.4)}$$

where d is the film thickness, R_H is the Hall constant, I_x is the current and B_z the magnetic field. Hall effect is a conduction phenomenon, which is different for different charge carriers. Since positive and negative charges within the semiconductor move in opposite directions, the Hall voltage has a different polarity for positive and negative charge carriers. Knowing the current and magnetic field directions, the sign of the Hall voltage indicates if the current is predominantly due to electrons or holes. Given the sign convention shown in Figure 3.15, the Hall voltage is positive for holes and negative for electrons. Hall constant in related with mobility and carrier concentration through equation

$$R_H = \frac{r(p\mu_p^2 - n\mu_n^2)}{q(p\mu_p + n\mu_n)^2} \quad \textbf{(3.5)}$$

where *r* is the Hall factor, μ_n and μ_p are the electron and hole mobilities, respectively, and *q, p* e *n* are the carrier charge, hole and electron concentration, respectively. In order to know the electrical characteristics of the semiconductor, we must suppose that if the semiconductor conductivity is due to electrons with charge $q=1.6\times10^{-19}$ C (n-type) and $\mu_n/\mu_p > 1$ the previous expression is reduced to

$$R_H \approx -\frac{1}{en} \quad \textbf{(3.6)}$$

and if the semiconductor conductivity is due to holes is reduced to

$$R_H \approx \frac{1}{ep} \quad \textbf{(3.7)}$$

where Hall constant has opposite signs in agreement with the majority carriers type. The previous equations allows the determination of carrier concentration, and when combined with conductivity equations:

$$\sigma = \frac{1}{\rho} \approx q\mu_p p \quad \text{or} \quad \sigma = \frac{1}{\rho} \approx q\mu_n n \quad \textbf{(3.8)}$$

allow the determination of carriers mobility, μ_n or μ_p .

One of the techniques to measure the electrical resistance of thin films is the so called sheet resistance, expressed in Ω/sq. the resistance of a film in a rectangular section (measured in the parallel direction to the film surface) as shown in Figure 3.16 is given by

$$R = \frac{\rho L}{dW} \quad \textbf{(3.9)}$$

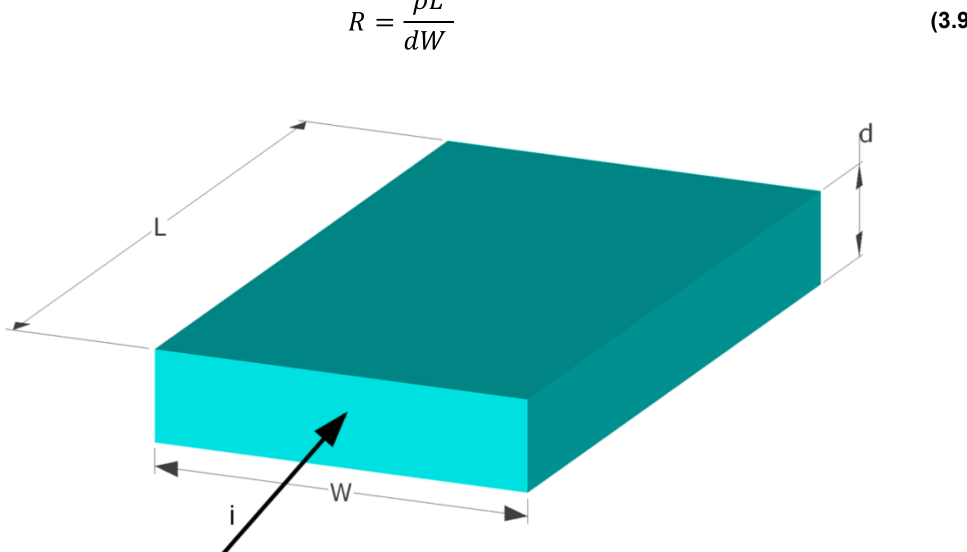

Figure 3.16. Illustration of the definition of sheet resistance.

When L = W,

$$R = \frac{\rho}{d} = R_S \tag{3.10}$$

For several conductors and semiconductors materials, the technique employed to the resistance measurement consists on the utilization of 4 probes disposed at the surface sample. Between two of these probes is applied a known current and between the other two, the voltage is measured [15]. Figure 3.17 shows some of the configurations used to measure the electrical resistivity.

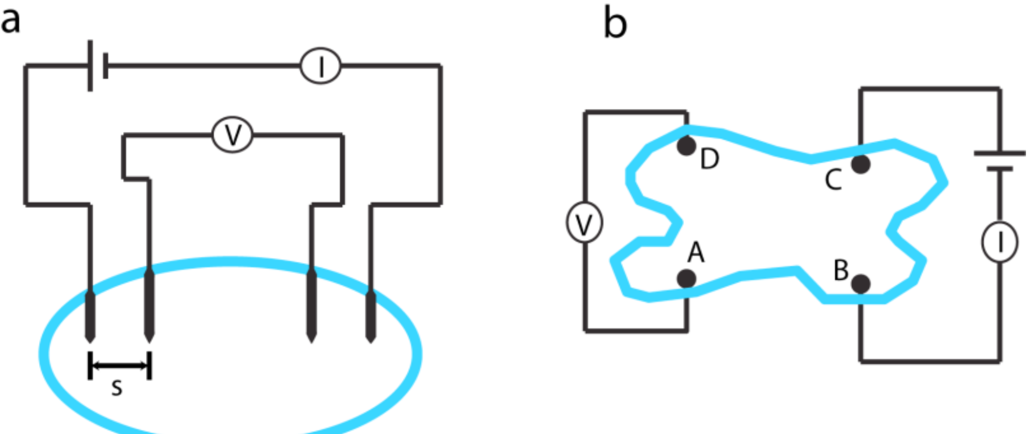

Figure 3.17. Techniques to measure electrical resistance of thin films. a) four point method to measure sheet resistance (b) Van der Pauw method to measure the resistivity with arbitrary geometries.

The Van der Pauw with defined geometry as represented at Figure 3.18 was used to the Hall effect measurements of the thin films produced.

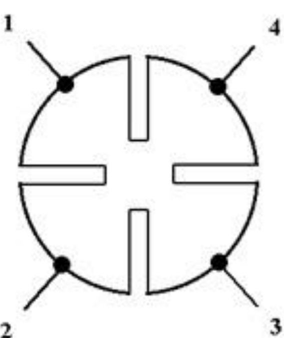

Figure 3.18. Van der Pauw geometry used for the thin films Hall effect measurements.

This method is widely used at semiconductors industry to measure the resistivity of uniform films [16]. By applying a known current between contacts 1 and 2, we can measure the voltage between contact 4 and 3, V_{43}, and by applying a known current between contacts 2 and 3, we measure the voltage between contact 1 and 4, V_{14}.

R_A and R_B can be calculated with the equations:

$$R_A = V_{43}/I_{12} \text{ and } R_B = V_{14}/I_{23} \quad \text{(3.11)}$$

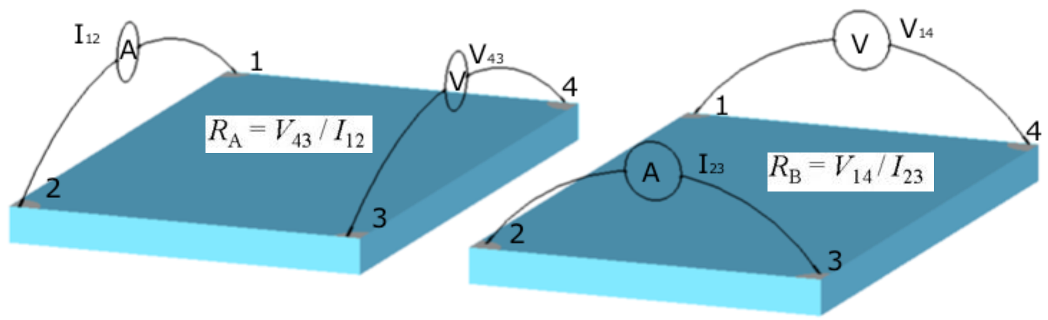

Figure 3.19. Van der Pauw method to measure R_A and R_B.

Between R_A and R_B, there is the relation

$$exp(-\pi R_A/R_S) + exp(-\pi R_B/R_S) = 1 \quad \text{(3.12)}$$

that can be solved to R_s.

Bulk resistivity can be calculated if the sample thickness is known trough

$$\rho = R_S \times d \quad \text{(3.13)}$$

The Hall voltage measurement consists of a series of voltage measurements with a constant current I and a constant magnetic field B applied perpendicular to the plane of the sample as shown at Figure 3.20.

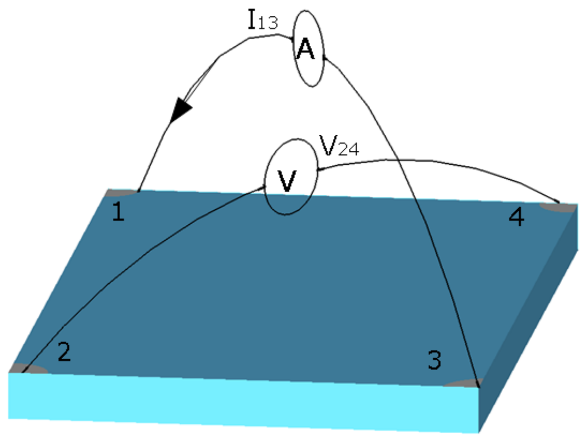

Figure 3.20. Van der Pauw method to measure R_A and R_B.

3.2.2.2 Dark Conductivity measurements

In order to determine the conduction mechanism of the oxide semiconductors produced, it was performed dark conductivity measurements as a function of temperature. The measurements were performed using a cryostat CS8900 (Bio-Rad) and a programmable electrometer Keithley 617 (Figure 3.21).

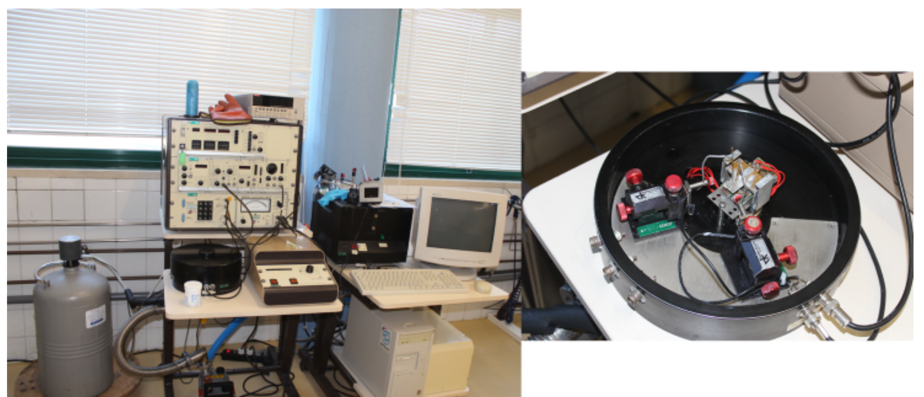

Figure 3.21. DC dark conductivity system, existing at CENIMAT, New University of Lisbon.

Dark conductivity measurements were taken by gradually heating the sample from 100 K to 400 K in a conventional liquid nitrogen cryostat using coplanar Ni/Au electrodes of 4 cm width and 1 mm spacing, as illustrated at Figure 3.22. For each value of temperature, a delay and stabilization time was defined to ensure the perfect control of temperature and also a better statistic of the current measured.

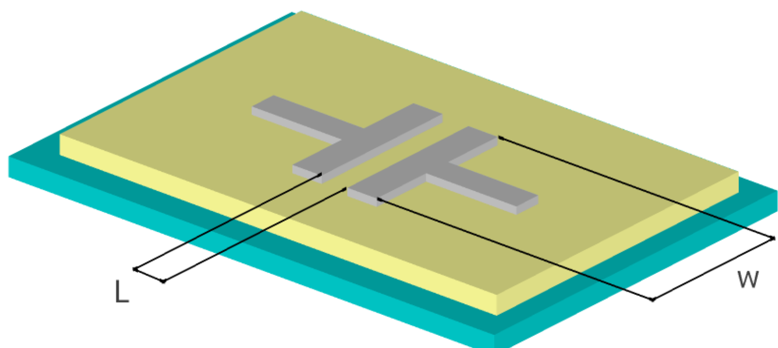

Figure 3.22. Geometry used for DC measurements in dark as a function of temperature.

The current density (**J**) through a generic surface is given by,

$$I = \int J \cdot dS \quad \textbf{(3.14)}$$

where dS is the surface element given by $dS = dx \cdot dz$.

Then, the current density can be written as

$$J = \frac{I}{wx} \quad \textbf{(3.15)}$$

where *x* is the film thickness and *w* is the contacts width. The electrical field *E*, originated by the potential applied between the two contacts, *V*, is given by

$$E = \frac{V}{L} = \rho J \quad \textbf{(3.16)}$$

where ρ is the material resistivity and *L* the distance between the contacts.. Since the resistivity is the inverse of conductivity, we obtain

$$\sigma = \frac{Il}{Vwx} \quad \textbf{(3.17)}$$

3.2.3. Structural and morphological characterization

3.2.3.1 X-ray diffraction (XRD)

X-ray diffraction is an experimental and non-destructive technique, very important for the crystallographic characterization of solids. The structural analysis of thin films using this technique allows us to identify the phases present in the material, to obtain information about the orientation and the amorphous or polycrystalline state of the materials [17]. When the X-rays focus on a crystal, the electromagnetic waves penetrate the crystal structure. Each plane of atoms reflects a part of the waves. Waves of different plans interfere and give rise to the diffracted beam at a 2θ angle of the incident beam [18].

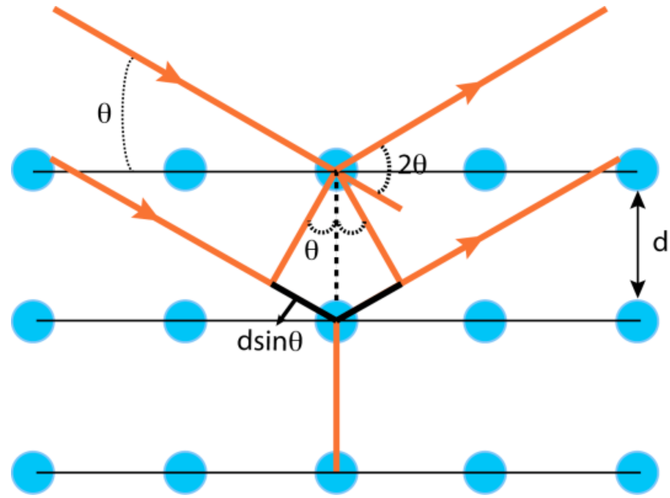

Figure 3.23. Illustration of X-ray diffracting from crystal planes.

Part of the incident beam is not diffracted and the diffracted part by the crystalline structure exists only in well-defined directions: 2θ angles of the incident beam, where the crystal surface does not affect the diffraction process. The diffraction angle 2θ depends on the wavelength of the X-ray, λ, and on the separation between planes, d (Bragg's law):

$$2d\sin\theta = n\lambda;\ n=1, 2, 3, \ldots. \quad \textbf{(3.18)}$$

the crystallite size is calculated trough the Scherrer formula [19],

$$D = \frac{0.94\lambda}{B\cos\theta} \quad \textbf{(3.19)}$$

Where D is the crystallite size, λ is the wavelength of incident X-ray and, θ is the diffraction angle and B is the line broadening at half the maximum intensity (FWHM).

XRD measurements were performed with a diffractometer PANalytical, model X´Pert Pro existing at CENIMAT, New University of Lisbon (Figure 3.24) in grazing incidence geometry with Cu Kα line radiation (λ = 1.5406 Å) at room temperature.

Figure 3.24. Picture of PANalytical, model X´Pert Pro existing at CENIMAT, New University of Lisbon.

3.2.3.2 Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) technique allows to obtain similar images to those obtainable by the reflection optical microscopy, but in a remarkably higher magnification range (from 10x to 100000x) with a depth field of 30 micrometers. To this technique is often associated energy dispersive X-ray spectroscopy (EDS), which allows a semi-quantitative analysis of the elements present in the sample.

The samples are scanned sequentially by an electron beam accelerated by a voltage ranging from 0 to 40 kV finely focused through a system of electromagnetic lenses. The interaction of the electron beam with the sample results in the emission of various types of radiation and electrons including secondary electrons, from which an image of the sample is formed.

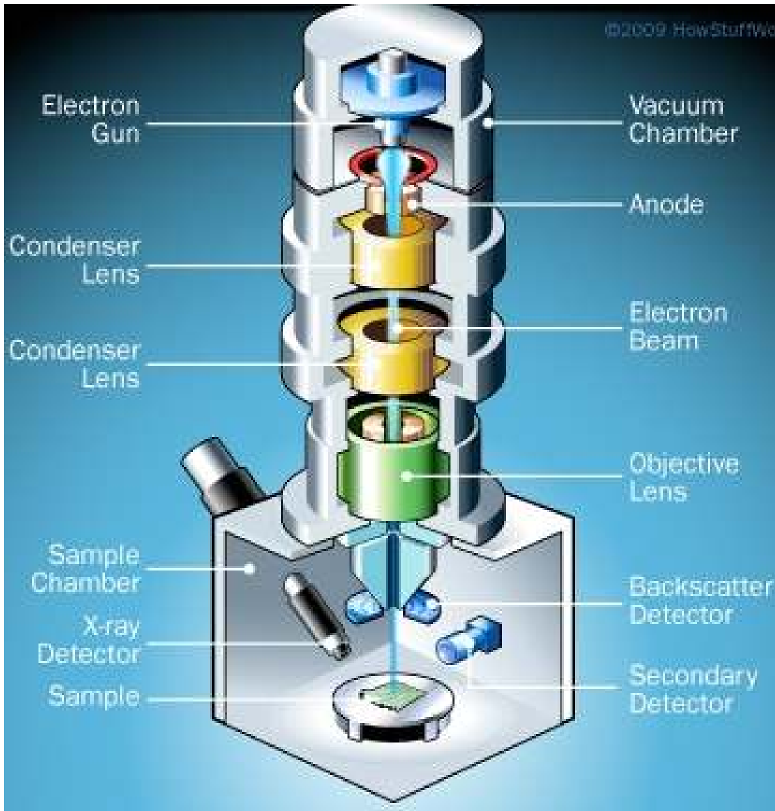

Figure 3.25. Diagram of a scanning electron microscope [20].

Secondary electrons are electrons in the sample that suffer excitement escaping from the surface. Backscattered electrons allow the distinction, within the sample under analysis, of light and heavy elements regions.

SEM observations were carried out using a Carl Zeiss AURIGA CrossBeam (FIB-SEM) workstation, equipped for Energy Dispersive X-Ray Spectroscopy and Energy Backscatter Diffraction measurements. EDS data have been collected and analyzed with the INCA software, existing at CENIMAT, New University of Lisbon (see Figure 3.26).

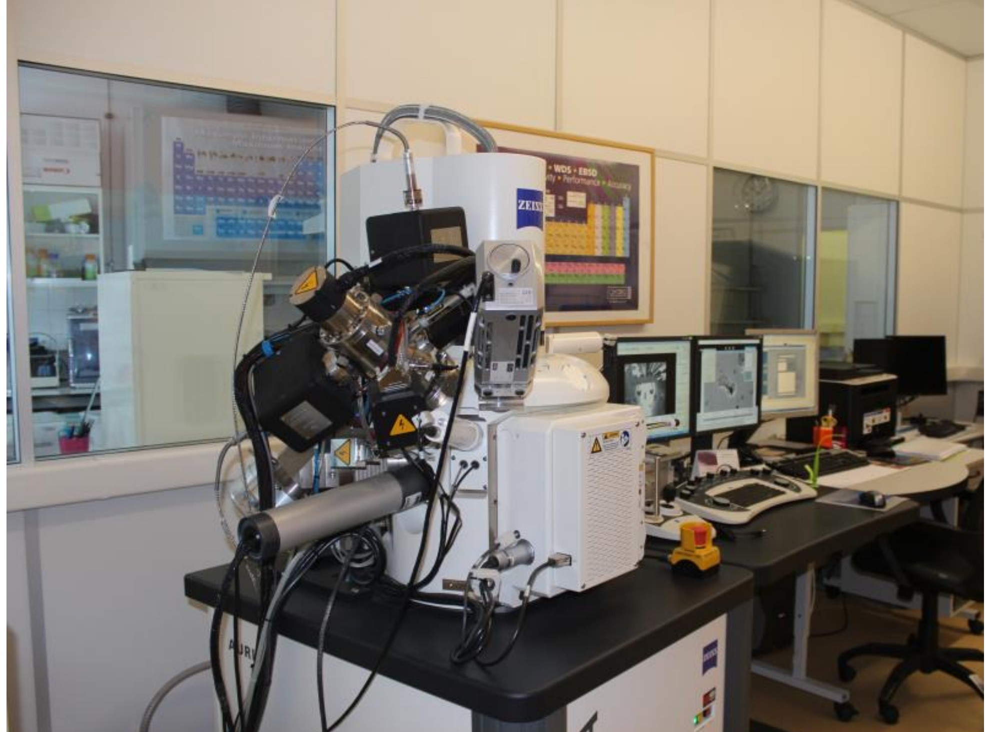

Figure 3.26. Scanning electron microscope existing at CENIMAT, New University of Lisbon.

3.2.3.3 Atomic force microscopy (AFM)

Scanning Probe Microscopes (SPM) are a family of microscopes used to locally observe the various properties of a sample surface. The most used microscopes from this type are the Atomic Force Microscope (AFM) and the Scanning Tunneling Microscope (STM). The basic principle of operation of SPMs is the detection of the interaction between a probe and the sample surface. With these microscopes the sample surface can be characterized with resolution ranging from the atomic to the micrometer scale.

SPMs arose from the observation, made by Gerd Heinrich Binnig and Rohrer in 1981,of electron tunneling effect between a tungsten tip, atomically sharp, and a platinum surface. Motivated by this observation, Binnig and Rohrer developed a device with the ability to simultaneously scan the surface of a sample under a conductive probe, atomically sharp, and measure the tunneling current between the tip and the surface, giving rise to the scanning tunneling microscope (STM).

Since then, several SPMs have been developed, allowing, at least, 20 different types of interactions between the probe and the sample surface. This versatility allows SPMs to be used in several research areas, such as materials science, physics, biology, chemistry, and metrology. Unlike electronic microscopes capable of performing only measures in the plane of the sample surface, the SPMs are also able to perform measurements in the perpendicular direction to the plane of the surface.

The resolution of the images acquired with SPMs, typically ranges from 0.1 to 10 nm in the plane of the surface and can be better than 0.1 nm in the perpendicular direction. In a way, STM is limited because only conductive and semiconductive surfaces can be analyzed, leading G. Binnig, C. F. Quate and Ch. Gerber to develop, in 1986, the Atomic Force Microscope. With AFM the interaction force between the tip and the surface sample is monitored. This force, similar to the interatomic forces on a solid, has a magnitude in the order of 10^{-9} N. With the AFM technique, both conducting, semiconducting and isolating samples can be studied.

Depending on the characteristics of the sample surface and on the properties we are interested in analyzing, AFM can operate in three different modes: contact mode (region of repulsive forces), intermittent contact mode (region of attractive and repulsive forces) and non-contact mode (region of attractive forces). Within this work AFM analysis were performed using a Asylum MFP3D AFM system existent in CENIMAT (Figure 3.27). The images are acquired in AC mode with a Si_3N_4 tip and a scan rate of 1 Hz.

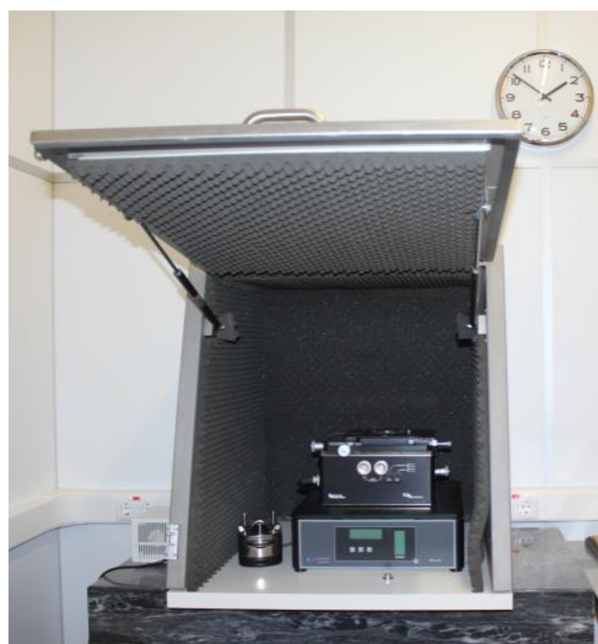

Figure 3.27. Atomic force microscope existing at CENIMAT, New University of Lisbon.

3.2.4. Compositional Characterization

3.2.4.1 X-ray photoelectron spectroscopy (XPS)

XPS technique is the main technique used in surface characterization, providing information on the atomic composition of the surface, chemical and electronic state of the elements existing within the material [21]. In this technique a beam of X-rays of low energy, in this case produced by AlKα lines with energy of 1486.6eV, is used to eject electrons from the sample.

When a surface is excited by photons, the emitted electrons, called photo-electrons, have an energy characteristic of the element from which they were emitted. In this process, the incident photon transfers all its energy to the electron bound and the identification element is given by the measure of each electron ejected from the sample without loss of energy, being the energy of each ejected electron equal to the energy of the incident photon minus the binding energy of that electron in the target atom.

XPS technique allows the identification of elements from by measuring the kinetic energy of the photo-ejected electrons, after the sample has been bombarded with X-ray since this energy is directly related to the binding energy of the element ejected. Handbooks and graphs of binding energies for elements and compounds are available [22]. The method is illustrated with the energy band diagram represented in Figure 3.28. Primary X-rays of 1 to 2 keV energy eject photoelectrons from the sample. The measured energy of the ejected electron at the spectrometer E_{sp} is related to the binding energy E_b , referenced to the Fermi energy E_F , by [23]

$$E_b = h\upsilon - E_{sp} - q\Phi_{sp} \tag{3.20}$$

where hv is the energy of the primary X-rays and φ_{sp} the work function of the spectrometer.

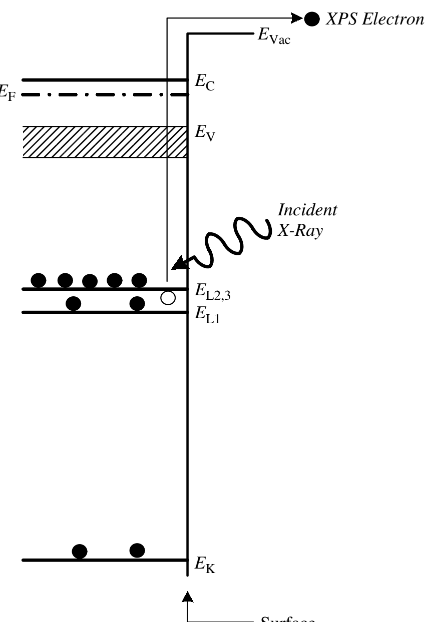

Figure 3.28. Electronic processes in X-ray photoelectron spectroscopy [23]

XPS measurements have been performed using the Darmstadt Integrated System for Materials Research (DAISY-MAT), existing at Technische Universitat Darmstadt, which is schematically shown in Figure 3.29. The system provides a central sample distribution chamber, which combines a Physical Electronics PHI 5700 multitechnique surface analysis system with several preparation chambers, allowing for rapid sample transfer between preparation and analysis

chambers without breaking ultrahigh vacuum (UHV) conditions. The base pressure in the spectrometer and the sample handler is 10^{-9} mbar [24].

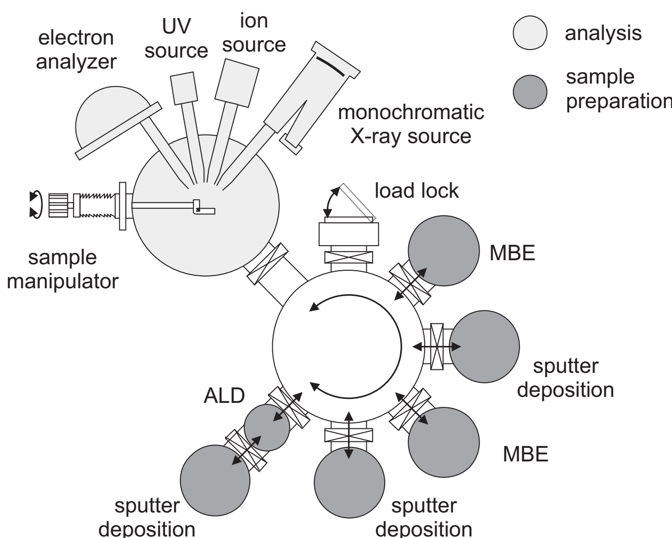

Figure 3.29. Darmstadt Integrated System for Materials Research (DAISY-MAT) existing at Technische Universitat Darmstadt [25].

X-ray photoelectron spectroscopy (XPS) was performed using monochromatic Al Kα radiation with an energy of 1486.6 eV and an overall energy resolution of less than 0.4 eV. Binding energies are reported with respect to the Fermi level, which was calibrated measuring a sputter cleaned metallic silver sample. The integral intensities of the photoelectron emission lines serve for determination of the sample's stoichiometry using atomic sensitivity factors [22].

3.2.4.2 Rutherford Backscattering (RBS)

Rutherford Backscattering Spectroscopy (RBS) is a technique widely used for analyzing materials. This technique was developed in the early twentieth century by Rutherford to determine the composition and atomic concentration profiles (in depth) of the elements present in a given sample. Its principle is based on the detection of particles which are backscattered after the collision with the atoms that constitute the sample [23].

The sample is bombarded with a monoenergetic ion beam (usually as He^+ or H^+) that gradually lose their energy due to inelastic collision with electrons and elastic collision with the atomic nucleus of the sample. The backscattered particles can be detected and its energy is determinated by the energy loss of the entry path, during the elastic collision process and of the out path. In this way, the histogram of the detected energy is a function of the depth at which the collision occurred and the mass of the scattered nucleus. Thus, it is possible to determine the concentration profile of a given element along the thickness of the sample analyzed.

RBS measurements were done at Instituto Tecnológico e Nuclear, ITN, in a 2.5 MV van de Graaff accelerator (Figure 3.30) using a 2.0 MeV He+ beam and silicon solid state detector with 20 KeV

energy resolution located at 165°with respect to the beam direction. The angle of incidence, defined as the angle between the beam and the normal of the sample, was fixed constant at 0°. The current in the sample was kept below 3 nA and the charge accumulated in the spectra was 2 μC.

Figure 3.30. RBS system existing at ITN [25].

3.2.5. Optical characterization

3.2.5.1 UV-Visible-NIR transmittance spectroscopy

Optical characterization technique was used to measure the optical transmittance of the thin films and calculate the respective optical bandap. For this purpose, we used a double beam spectrophotometer SHIMADZU UV-VIS-NIR 3100 PC existing in CEMOP, New University of Lisbon (Figure 3.31) that allows then to obtain the values of absorbance and transmittance of thin films over a range of wavelengths between 190 nm and 3100 nm (the ultraviolet, visible and infrared).

Figure 3.31. *SHIMADZU UV-VIS-NIR 3100 PC system for optical characterization,* existing at CEMOP, New University of Lisbon.

The specular transmittance was measured with a scan range between 250 and 2500 nm using a glass substrate (of the same type as the one of the substrate samples) as reference so that the spectrum obtained in only from the thin film. The spectrophotometer sensor detects the beam that passes through the sample and the beam passing trough the reference, comparing their intensities. The absorption coefficient (α) can be calculated from the optical measurements trough the equation

$$\alpha = \frac{1}{d} ln[1/T] \qquad \textbf{(3.21)}$$

where T is the transmittance and d is the film thickness.

The optical gap is determined in the strong absorption region, using the Tauc law: $\alpha^x = (h\nu - E_{opt})$, extrapolating the linear region of the $(\alpha h\nu)^2$ versus $h\nu$ plot, trough the equation

$$(\alpha h\nu)^m = B(h\nu - E_{op}) \qquad \textbf{(3.22)}$$

where h is Planck's constant, ν the frequency, B is a constant that depends on photon's energy, E_{opt} is the optical bandgap and m is a value related with the transition type. When plotting a graph of $(\alpha h\nu)^m$ as a function of $h\nu$, one can find what is the transition in question through the linearity of the fit. The transition can be 2, 2/3, 1/2 or 1/3 depending if the transition is allowed direct, forbidden direct, allowed indirect or forbidden indirect, respectively. In the case of oxide materials the type of transitions is usually allowed direct.

3.3. Thin-film transistor

3.3.1. Current-voltage measurements

The measurement of output and transfer characteristics of the produced devices were done using an Agilent 4155C SPA and Cascade M150 microprobe station existing at CENIMAT (Figure 3.32). The measurements are made in the dark, at room temperature, with relative humidity being maintained between 35-50 %.

Figure 3.32. Microprobe Cascade MicroTech M150 and Agilent 4155C existing at CENIMAT; New University of Lisbon.

To compare the different devices produced a measure method was followed:

1. Three consecutive transfer characteristics with V_{GS} ranging from 50 to -40 V in saturation regime (V_{DS}= -30 V), performed in single sweep mode in order to evaluate the stability of the TFT;
2. One transfer characteristic with V_{GS} ranging from 50 to -40 V, with V_{DS}= -1 V to assure linear mode operation, performed in double sweep mode;
3. One transfer characteristic with V_{GS} ranging from 50 to -40 V, with V_{DS}= -30 V to assure saturation mode operation, performed in double sweep mode. This plot is used to extract V_{th}, S and On-Off ratio;
4. One output characteristic with V_{DS} ranging from -50 to 0 V, with 9 steps of V_{GS}, from 0 to 40 V.

3.3.2. Stress measurements

In order to study the dominant degradation mechanisms and to see if the devices are suitable for application in present and future electronic circuits stress measurements were performed on a Keithley 4200-SCS with a Janis ST500 microprobe, where a constant V_{GS} is applied during 6 h, while keeping the source and drain electrodes grounded. The stress/recovery periods are shortly interrupted several times to assess the transfer characteristics of the TFTs.

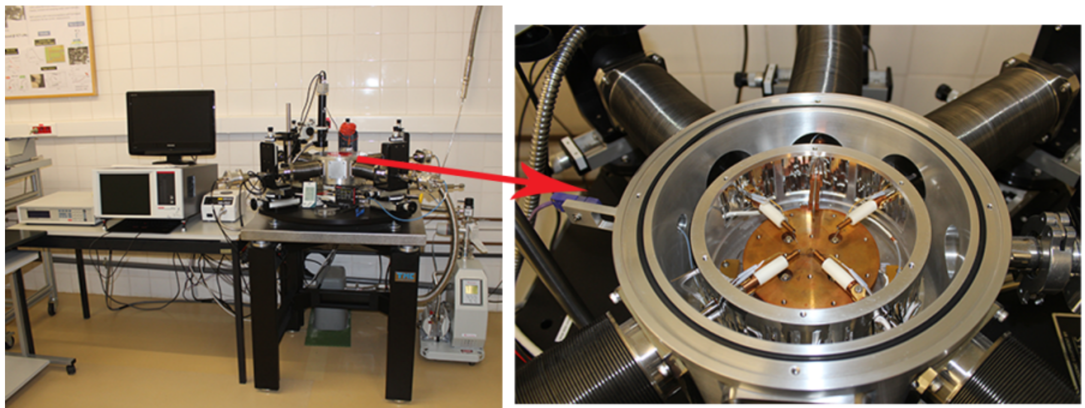

Figure 3.33. Microprobe Cascade MicroTech M150 and Agilent 4155C existing at CENIMAT; New University of Lisbon.

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Chapter 4. *Transparent p-type oxide semiconductor produced by sputtering*

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4. TRANSPARENT P-TYPE OXIDE SEMICONDUCTOR PRODUCED BY SPUTTERING

This chapter describes the characterization and optimization of tin oxide based p-type transparent oxide semiconductors (TOSs) produced at room temperature by r.f. magnetron sputtering technique. Three different p-type TOSs were fabricated; tin oxide, copper-doped tin oxide and indium-doped tin dioxide.

The influence of the deposition and post depositions parameters on the electrical, morphological, structural, morphological and optical properties such as the content of oxygen ($\%O_2$), the deposition pressure (p_d), and the post-annealing temperature (T_A) is discussed in this chapter where the main goal is to select the best conditions to obtain a p-type semiconductor in order to apply in a thin film transistor.

4.1. Oxide semiconductors based on SnO

4.1.1. Deposition Parameters

The tin oxide thin films were obtained from a metallic tin target of 99.99% purity using a radio frequency reactive magnetron sputtering system. In order to obtain p-type oxide semiconductors thin films and to better understand its properties, several parameters were varied during and after the deposition process. During the deposition a mixture of argon and oxygen were present. The control of oxygen content plays a fundamental role to obtain the SnO_x phase.

Its percentage, calculated from $\%O_2= P_{O2}/(P_{O2}+P_{Ar})$, during the deposition was varied between 2.5% and 8 %. Also during the deposition, the deposition pressure was varied between 0.2 Pa and 0.4 Pa, once it can strongly influence the growth rate and the morphology of the thin films. The r.f. power applied was kept constant, 40 W, because the melting point of Sn is to low (232 °C) and above this value of r.f. power, the target would melt. After the deposition, the thin films were annealed at 150 °C and 200 °C in air during one hour. Table 4.1 summarizes the parameters used for this study.

Table 4.1. Conditions used for the deposition of SnO_x thin films.

Target	**Metallic tin, (Plasmaterials, Inc,)** **purity= 99.999%, ϕ = 2”, thickness = 3 mm**
Gases	argon oxygen
Experimental conditions	
Substrate temperature	No intentional heating
Target-substrate distance	18 cm
r.f. Power(W)	40
$\%O_2$ (%)	2.5 – 8-5
Deposition Pressure (Pa)	0.2 – 0.4

4.1.2. Dependence of the growth rate on the deposition parameters

The growth rate (R) of the thin films can be strongly influenced by the deposition parameters, such as the $\%O_2$, and the p_d.

Figure 4.1 shows the influence of $\%O_2$ and p_d on the growth rate of the SnO_x thin films. As observed, the introduction of oxygen results in lower R. Without oxygen, R has a value of 5.4 nm/min and it decreases to 3.65 nm/min for an oxygen content of 8.5%. This reduction with the oxygen content when sputtering metal oxides could be attributed to the re-sputtering of the atoms from the film surface by energetic O^- ions, since that with the increase of oxygen content at the deposition chamber, more O^- ions are available resulting in a higher re-sputtering, decreasing in the deposition rate. Also, O_2 ions have a lower mass compared to Ar, resulting in a lower energy transfer to the target [1][2].

Another explanation is that higher $\%O_2$ means less quantity of Ar and consequently an increase of unionized neutral oxygen atoms. These neutral O_2 atoms collide with the sputtered particles consuming their energy. Consequently, these particles diffuse to low energy positions without enough energy to reach the substrate, resulting in lower deposition rate [3].

Figure 4.1 also shows the dependence of R with the deposition pressure. It is observed a clear decrease on R as p_d increases. The increase of p_d results in the increase of atoms and gas molecules inside the deposition chamber, leading to a lower mean free path (λ_m) and consequently to a lower growth rate of the films [4]. The mean-free path (λ_m) is related to the deposition pressure by the equation [5]

$$\lambda_\mathrm{m}=\frac{k_B\mathrm{T}}{\sqrt{2}\pi \mathrm{d}^2 \mathrm{p_d}} \qquad \textbf{4.1}$$

where k_B is the Boltzmann constant, T the absolute temperature, d is the particle diameter and p_d is the deposition pressure. For higher p_d, λ_m decreases leading to more collisions between the sputtered species during the target-substrate path resulting in a loss of energy of the sputtered species due to the thermalization process and consequently they can't reach the substrate where the thin film is being deposited [6]. For low p_d, λ_m is higher meaning that more sputtered particles reach the substrate and with higher energies

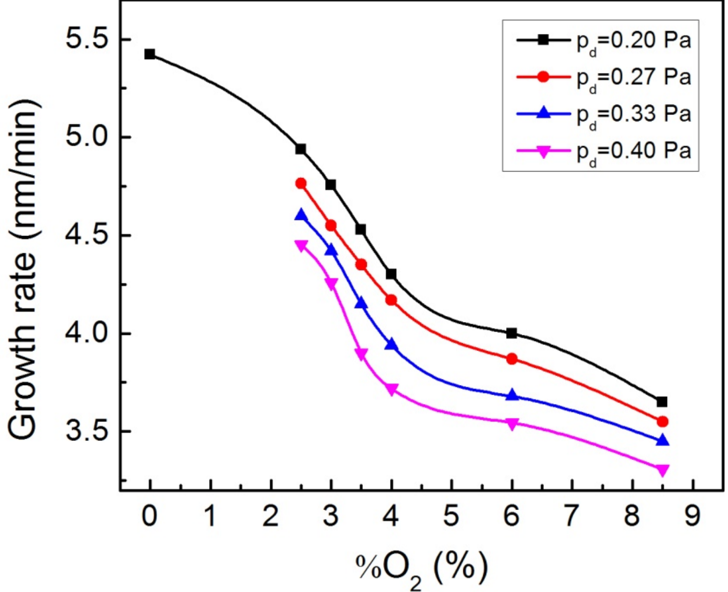

Figure 4.1. Growth rate as function of %O_2 and p_d.

4.1.3. Structural and morphological properties

4.1.3.1 Influence of the deposition parameters

From Figure 4.2, we can observe that an increase on the oxygen content leads to a lower crystallinity of the thin films and consequently to a decrease at the crystallite size (Figure 4.5). For the film deposited with O_2=2.5 %, the diffraction peaks can be addressed to β-Sn and to α-SnO preferentially oriented with (110) plane (ICDD cards No 98-004-0673 and 98-006-0395). As the content of oxygen increase, both the intensity of α-SnO and β-Sn phases decrease, with the latter disappearing for %$O_2 \geq$ 6%. At %O_2=8.5% there were no characteristic peaks for any phases, suggesting the amorphous nature of the films. The decrease of α-SnO phase crystallinity could be justified considering that the incorporation of O_2 results on the oxidation of Sn^{2+} to Sn^{4+} (SnO to SnO_2) and that SnO_2 could be amorphous for T_A=200 °C [7].[8].

This structural behavior, with increasing O_2, is observed regardless the deposition pressure used during the thin film deposition (see Figure 4.3).

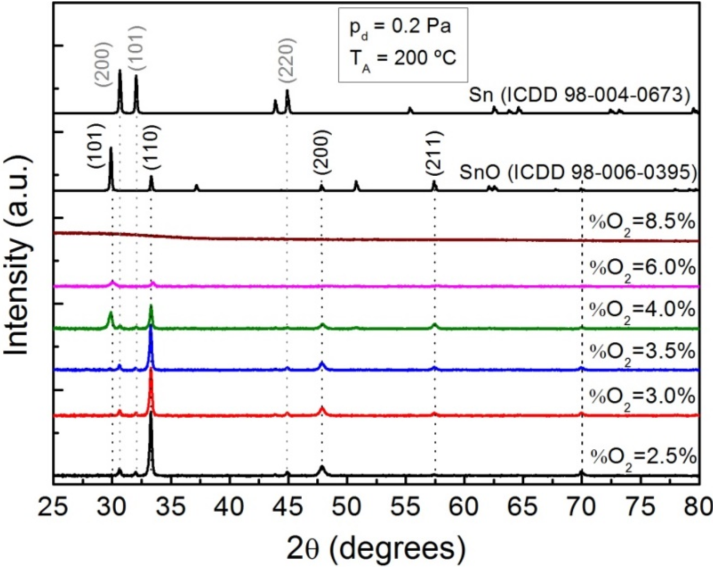

Figure 4.2. XRD diffractograms for the SnO_x films deposited at p_d=0.2 Pa and annealed at 200 °C as a function of $\%O_2$

From Figure 4.3, we observe that for an increase in p_d while keeping constant $\%O_2$, there is a decrease of the thin films crystallinity due to the reduced sputtering particles and to more crystal defects when increasing the deposition pressure. For lower deposition pressure, the mean free paths of the particles within the plasma is higher and fewer collisions occur resulting in a higher adatom mobility of the deposited films and consequently in a better crystalline quality [3][9].

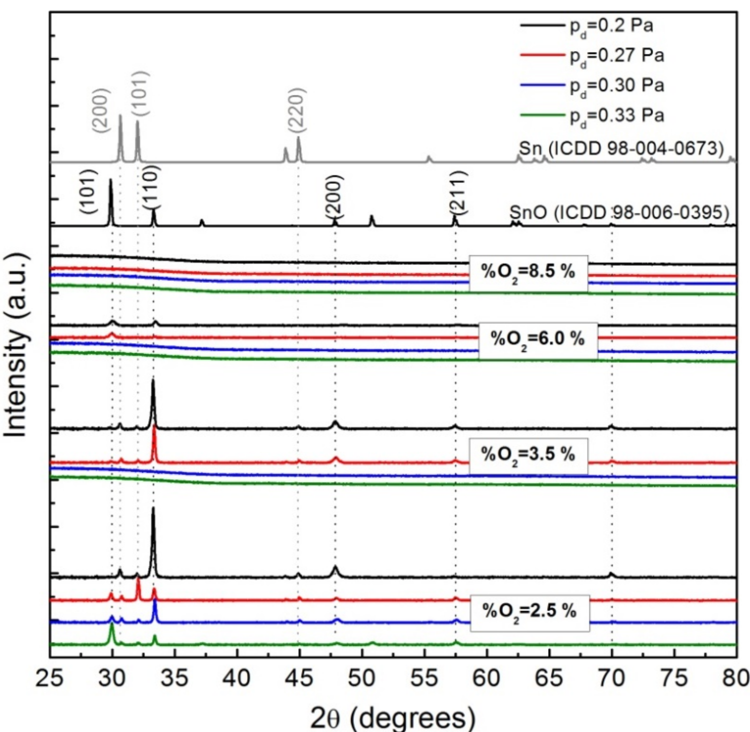

Figure 4.3. XRD diffractograms for the SnO_x films annealed at 200 °C deposited at different deposition pressures and oxygen content.

Figure 4.4 shows the SEM and AFM images of SnO_x films annealed at 200 °C for a p_d= 0.2 Pa, and %O_2 varying between 0 % and 8.5 %, obtained from SEM and AFM techniques and Figure 4.5 presents the crystallite size (*D*) estimated for the high intense peak of α-SnO (110) using the Scherrer's equation (3.19) and the mean roughness obtained from AFM measurement as a function of oxygen content.

With the increase in oxygen content, the lamella like grain morphology showed a transition to equiaxed structure and finally to a very fine and smooth nano structure.

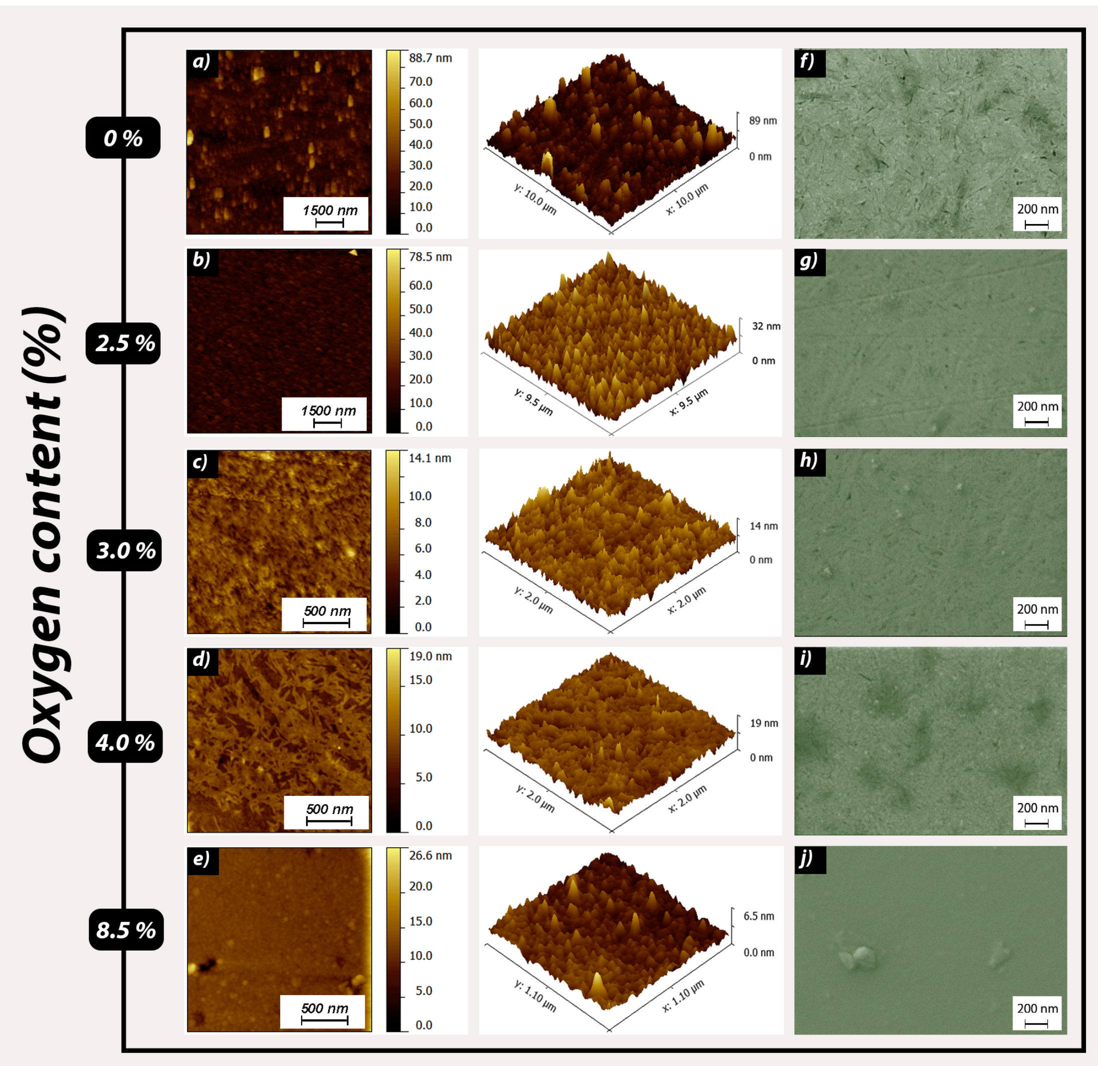

Figure 4.4. AFM, a) to e) and SEM, f) to j) images of the films deposited at p_d= 0.2 Pa, T_A= 200 °C for different %O_2.

As the content of oxygen increases, the mean route square roughness, r_{rms} and the grain size of the films decrease. The films have a more sharper grain structure for lower oxygen content with no well-defined boundaries. As the content of oxygen increases, the films surface becomes smoother and more uniform.

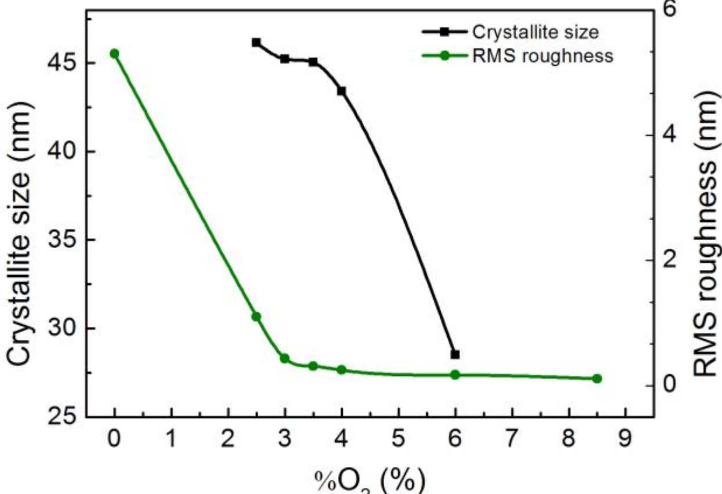

Figure 4.5. Dependence of surface roughness and grain size with oxygen content for the films deposited at pd= 0.2 Pa and annealed at 200 °C.

4.1.3.2 Influence of the annealing temperature

Figure 4.6 shows the X-ray diffraction (XRD) pattern for the p-type SnO_x thin films as deposited and annealed at 150 °C and 200 °C, deposited at p_d = 0.2 Pa and %O_2 varying between 2.5 % and 4 %.

For the as deposited thin films, the diffraction peaks correspond only to metallic tin (β-Sn), except for a %O_2=4 % where no peaks are observed. After the annealing, the metallic tin is partially oxidized to SnO phase (α-SnO) with a tetragonal structure and a preferential orientation along the (110) plan. However, impurities due to metallic Sn still present at the thin films decreasing for higher oxygen contents. We can also observe that the crystallinity of the films increases with the annealing temperature while the metallic β-Sn phase disappears.

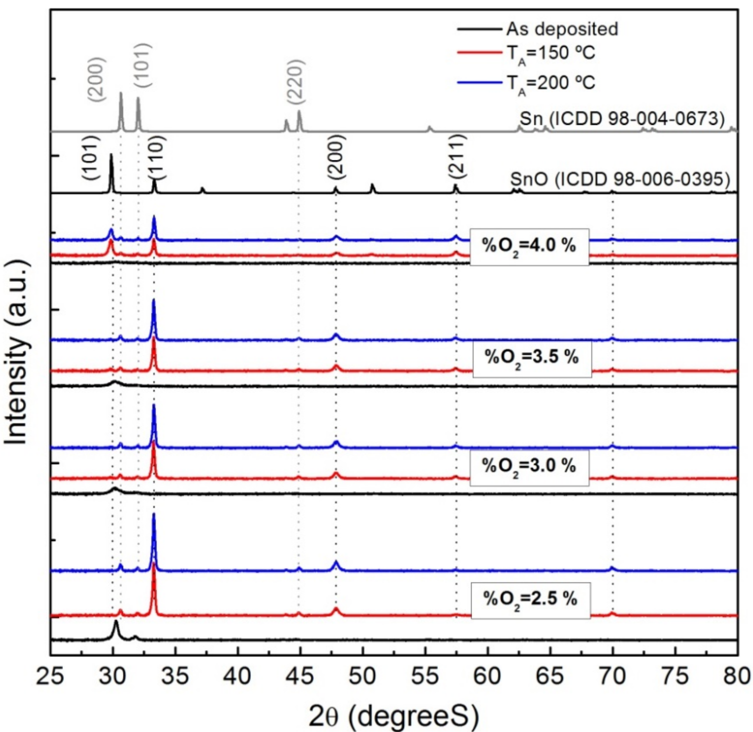

Figure 4.6. XRD diffractograms for the SnO_x films deposited at p_d=0.2 Pa for different annealing temperatures and oxygen content.

The crystallite size of the film was calculated using full width half maximum (FWHM) of (110) peak at Scherrer equation and it is presented at Figure 4.7. The crystallite size of SnO_x thin films slightly increases with annealing temperature. This could be due the annealing coalescence of small grain boundary diffusion resulting in major grain growth. As the substrate temperature is increased, the crystallinity of the films improve, as evidenced by the increase in sharpness and intensity of the XRD peaks.

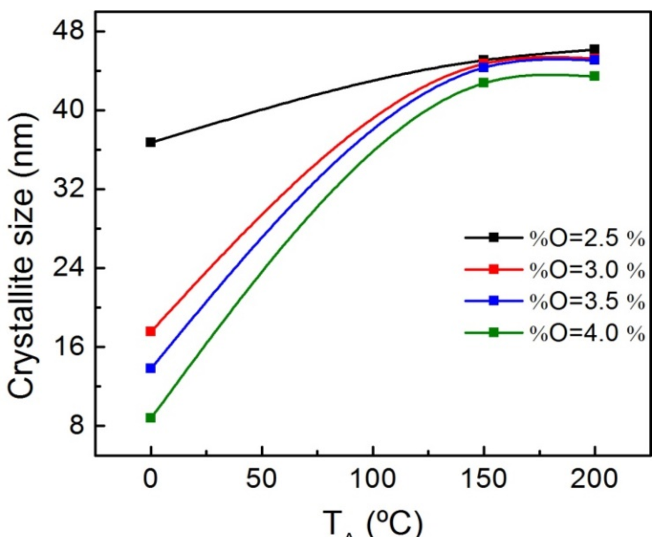

Figure 4.7. Dependence of crystallite size with annealing temperature for the films deposited at p_d= 0.2 Pa different $\%O_2$.

Figure 4.8 shows the surface morphology of the SnO_x thin films, studied by AFM and SEM measurements for different annealing temperatures. The films roughness increases from 0.51 nm for the as deposited film to 1.1 nm for the annealed film, with the increase of annealing temperature, since a major grain growth leads to an increase in the surface roughness [10].

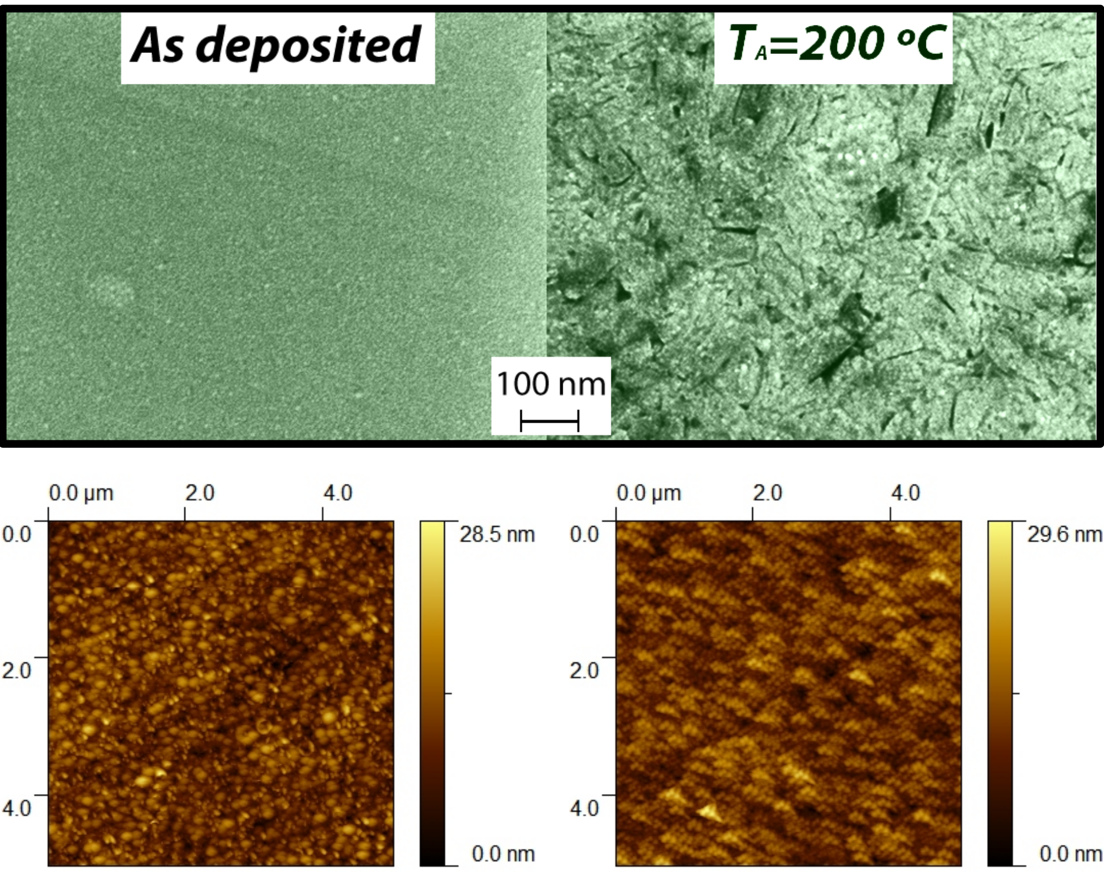

Figure 4.8. SEM and AFM images of the films deposited at p_d= 0.2 Pa, %O_2=2.5 %, as deposited and T_A= 200 °C.

4.1.4. Compositional analysis

Despite the results obtained from XRD, in order to a better understanding of the thin film composition and the ratio between the Sn, SnO and SnO_2 phases, X-ray photoelectron spectroscopy (XPS) was performed to the film deposited at p_d=0.2 Pa and %O_2=4%, as deposited and annealed at T_A=200 °C. XPS was performed using monochromatic Al Kα radiation with energy of 1486.6 eV and an overall energy resolution of less than 0.4 eV. Binding energies are reported with respect to the Fermi level, which was calibrated measuring a sputter cleaned metallic silver sample. No charging of the sample has been observed during measurement. As seen from the survey scan spectra in Figure 4.9, only Sn and O elements were observed except for a small amount of C due to air contact at 285 eV. Figure 4.10 shows the O1s, Sn $3d_{3/2}$ and Sn $3d_{5/2}$ XPS spectra in detail and Figure 4.11 shows the fitting results of Sn $3d_{5/2}$ XPS spectra of the thin film as deposited and annealed at 200 °C. The individual contributions have been fitted by a

convolution of Gauss and Lorentz profiles. For the oxidized species, a Gauss to Lorentz ratio of 0.7-0.8 was chosen, while the metallic tin component was fitted with 0.9. The FWHM for the oxidized components was fixed at 1.2 while the emission of metallic tin was fitted with 0.8.

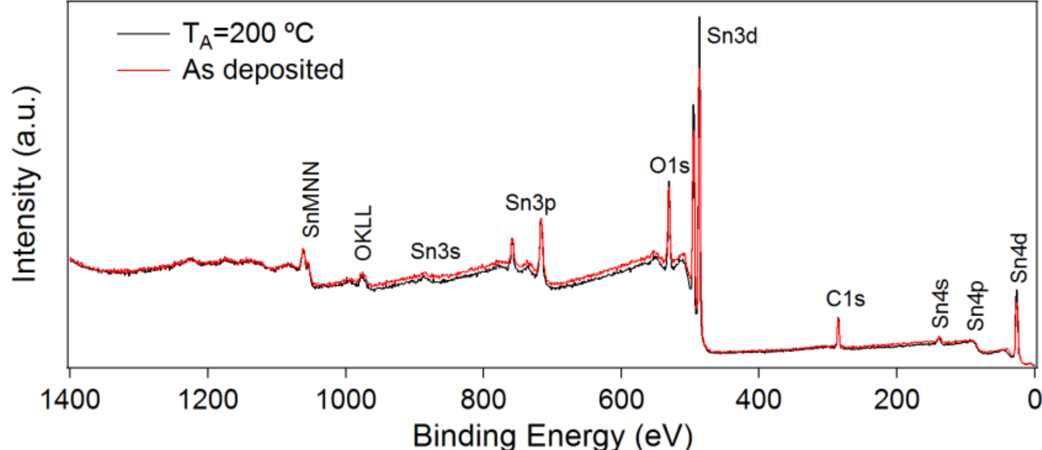

Figure 4.9. XPS survey spectra of tin oxide films as deposited and annealed prepared by reactive magnetron sputtering.

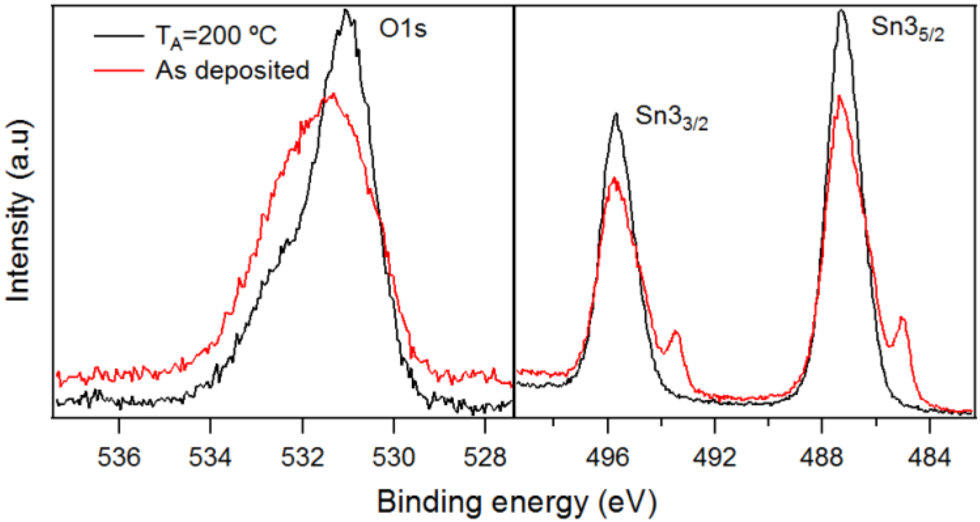

Figure 4.10. O1s, Sn $3d_{3/2}$ and Sn $3d_{5/2}$ XPS spectra of SnO_x thin film as deposited and annealed at 200 °C.

Although the XRD diffractogram of the as deposited film presents only β-Sn, we can observe from Figure 4.11 a) that Sn $3d_{5/2}$ spectrum can be fitted with contributions of Sn^{4+}, Sn^{2+} and Sn^{0}, even though the adjustment is not perfect. The binding energies are reported in TABLE XYZ. The binding energy of Sn^{2+} changes over 0.2 eV when the sample is annealed, which cannot be explained at this point. It is however not reasonable to assume other oxidation states the 2+ and 4+.

Since the probing depth of XPS is in the range of 5-10 nm and XRD doesn't show phases related to oxidized tin, it can be concluded that the oxidation takes place mainly at the surface [reference for surface oxidation of SnO to SnO2]. After the annealing, the shoulder corresponding to Sn^0 disappears and only Sn^{2+} and Sn^{4+} are present in the film whereas their relative intensities change due to the presence of more Sn^{4+}. The Sn $3d_{5/2}$ peaks after annealing are composed of Sn^{2+} and Sn^{4+} contributions, indicating the coexistence of the SnO and SnO_2 phases, without a metallic phase, at least within the probing depth of XPS.

Table 4.2 summarizes the atomic percentages of the elements for the as deposited and annealed film. Oxygen of adsorbed carbon species from air exposure has been subtracted from stoichiometry calculations by fitting the carbon 1s line, as outlined elsewhere [Payne, J. Electron Spectrosc. Relat. Phenom. 2011]. The values obtained by fitting have been compared to the stoichiometry analysis by considering that each Sn^{2+} binds to one oxygen, while Sn^{4+} involves two oxygen anions. The resulting oxygen percentage calculated from the fitting is 60.33% for the as deposited sample and 62.69% after annealing. These values are reasonably close to the results from stoichiometry analysis.

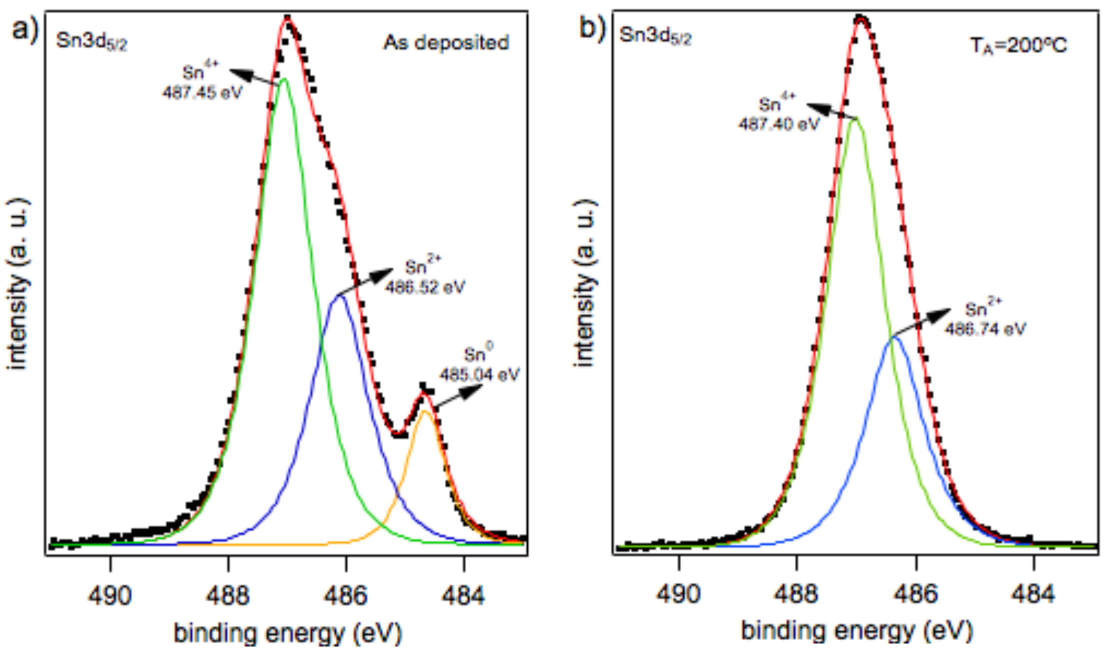

Figure 4.11. XPS spectra of Sn 3d (a) as deposited and (b)annealed for the SnO_x films. Smooth lines are representing fitting data.

Table 4.2. Content of Sn^0, Sn^{2+} and Sn^{4+} in the SnO_x films as deposited and annealed.

	O (%)	Sn (%)		
		39.95		
As deposited	60.05	Sn^0	Sn^{2+}	Sn^{4+}
		11	27	62

	O (%)	Sn (%)		
		37.64		
T_A= 200 °C	62.36	Sn^0	Sn^{2+}	Sn^{4+}
		0	29	71

Figure 4.12 shows the graphical method used to evaluate the VBM position. Due to the metallic states existing on the sample as deposited, it is not precise to perform this procedure on the as deposited sample. For the p-type SnO_x film annealed at 200 °C the value obtained was 1.2 eV, as reported by others and much lower than the one obtained for pure SnO_2 [11].

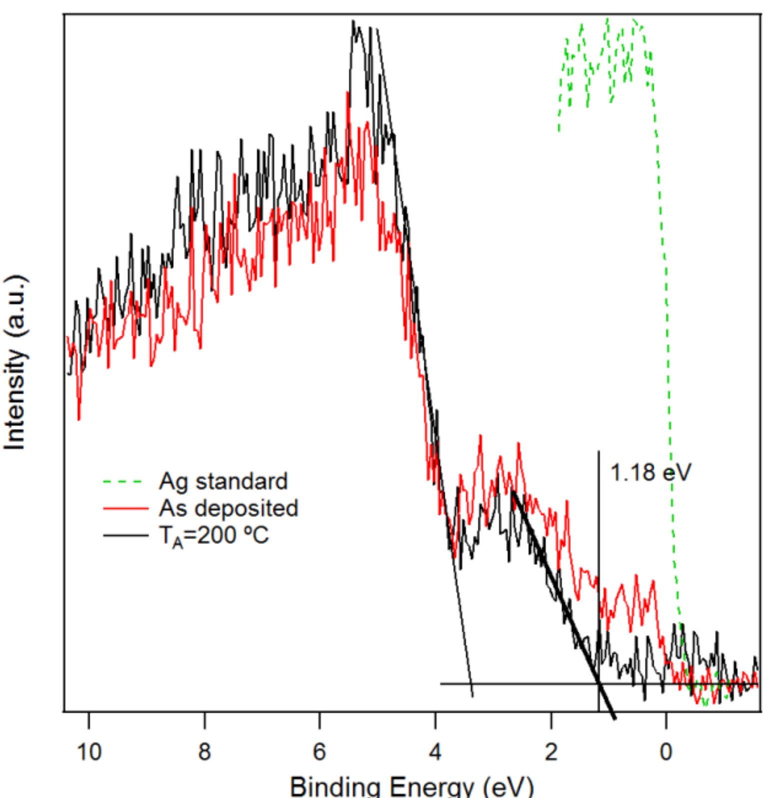

Figure 4.12. Valence band spectra of SnO_x films as deposited and annealed at T_A=200 °C.

4.1.5. Optical properties

4.1.5.1 Influence of the deposition and post-deposition parameters on the optical properties

- *Percentage of oxygen (%O_2) in the Ar+O_2 mixture and annealing temperature*

Figure 4.13 a) and b) shows the transmittance spectra of the thin films as deposited and annealed at T_A=200 °C as a function of the oxygen content. The optical transmittance of the as deposited films is very poor and almost constant with the increase of oxygen content in the visible region due to the presence of metallic tin (Figure 4.13 c)).

After annealing at T_A=200 °C, the optical transmittance of the thin films in the visible region increases considerably. However, for low contents of oxygen, where β-Sn phase is still present, the films still exhibit a lower transmittance because of the intensive light absorption of the metal gradient.

As the content of oxygen increases, the transmittance of the films also increases and the band edges shift gradually to shorter wavelengths, consistent with the blue-shift of the band gaps.

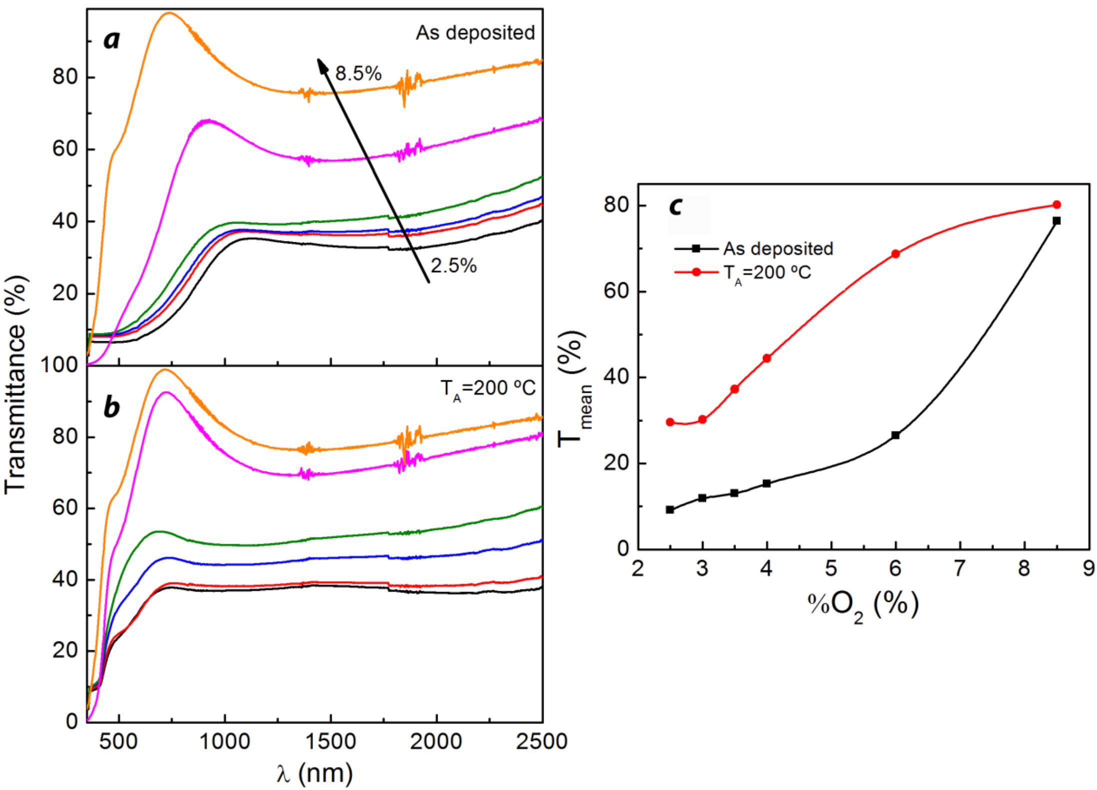

Figure 4.13. Optical transmittance spectra of the SnO_x films with different content of oxygen a) as deposited and b) annealed at 200 °C; c) mean transmittance of the films.

At Figure 4.14 we can observe the pictures of the annealed thin films at T_A=200 °C with ~120nm, for different contents of oxygen and at Figure 4.15 the thin film with $\%O_2$=2.5% as deposited and annealed at T_A=200 °C with ~120 nm and the thin film with the thickness used as a channel in a thin film transistor, with 12 nm thickness annealed at the same temperature. As we can observe, the thin film annealed at T_A=200 °C with 12 nm is very transparent in the visible range.

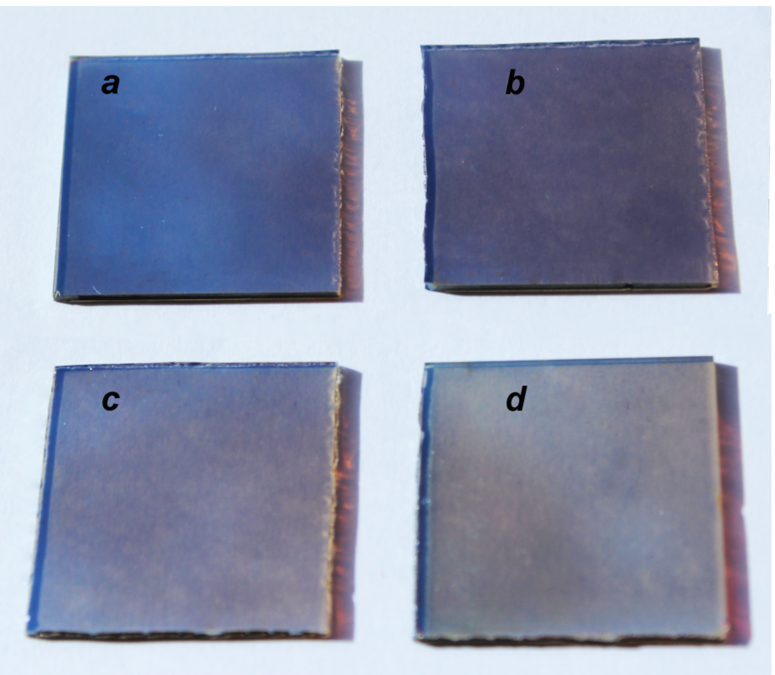

Figure 4.14. Picture of the thin films annealed at T_A=200 °C with a $\%O_2$ of a)2.5%, b)3.0%, c) 3.5% and d) 4%.

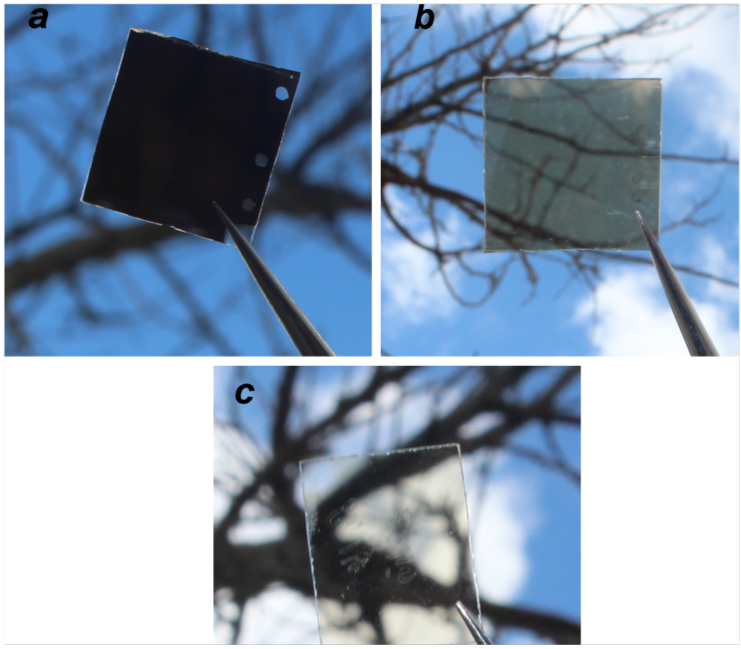

Figure 4.15. Picture of the thin films with 120 nm thickness with a %O_2=2.5% a) As deposited and b) Annealed at T_A=200 °C and c) With 12 nm thickness annealed at T_A=200 °C.

Figure 4.16. c) shows the evolution of optical bandgap (E_{opt}) with %O_2, calculated from the transmittance data using Tauc's plot (Figure 4.16 a) and b)) defined at Chapter 3.

The optical bandgap obtained for the as deposited film at %O_2=2.5 % is 1.36 eV and increases up to 3.3 eV for %O_2= 8.5%. In general E_{opt} for low contents of oxygen of as deposited films, is considerably lower when compared to the annealed films, but as the content of oxygen increases the optical band gap of the as deposited films approaches the ones of the annealed films.

For the annealed films and %O_2 between 2.5 % and 4 % (p-type conductivity), the optical bandgap obtained varies from 2.60 eV to 2.74 eV as the content of oxygen increases, close to the reported band gap of tetragonal SnO (2.5-3.0 eV) [12][13]. The increase of E_{opt} with the increase of oxygen content can be related to the phases present at the thin films. At lower %O_2, β-Sn phase is present, acting as metallic particles that absorbs the light intensively. As %O_2 increases the increase of E_{opt} could be due to the presence of SnO and for higher %O_2 due to the presence of SnO_2, that has higher bandgap (~3.6 eV) than SnO.

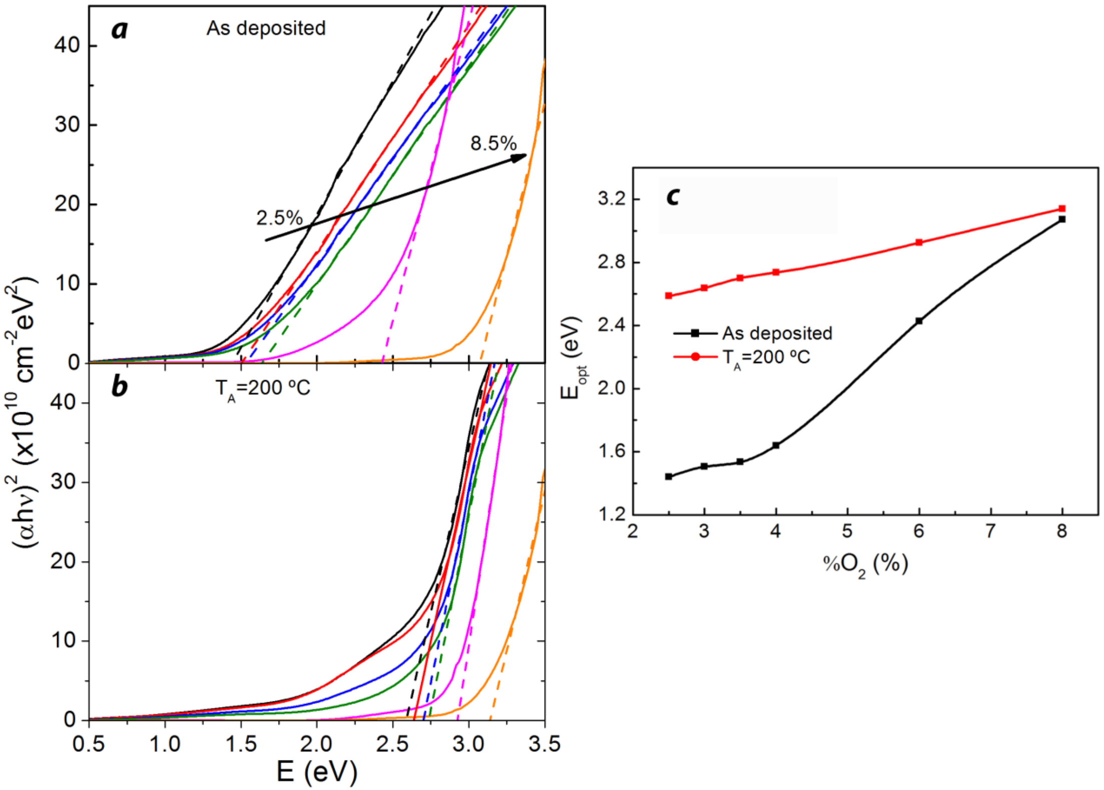

Figure 4.16. $(\alpha h\nu)^2$ vs photon energy ($h\nu$) spectra for the films a) as deposited and b) annealed at 200 °C; c) calculated optical bandgap as a function of oxygen content for the thin films.

4.1.6. Electrical properties

4.1.6.1 Influence of the deposition and post-deposition parameters on the electrical properties

4.1.6.1.1 Percentage of oxygen in the Ar+O_2 mixture (%O_2)

Hall Effect measurement is the most commonly used technique to identify the charge carrier and carrier mobility in the material. It is important to refer that in contrast to n-type oxides, Hall measurement does not give reliable results for p-type oxides, mainly because of very small drift mobility of holes. Some of the films show ambiguous results, particularly the as deposited films, presenting both negative and positive Hall coefficient during the electrical measurements.

Because of the uncertain type of conduction of these films, their electrical properties are not presented here. Due to limitations of the Hall Effect system it was also not possible to measure samples with higher content of oxygen, due to their more resistive nature. The most critical parameter to control, in order to obtain a p-type semiconductor, is the oxygen content (%O_2) in the SnO_x film.

Among the %O_2 studied, p-type conduction was achieved in the films deposited with a %O_2 between 2.5% and 4 %. This could be understand with the tin ion change, upon oxidation, from Sn^{2+} (p-type conduction) to Sn^{4+} (n-type conduction) [14]. Therefore, small amounts of oxygen should be used for obtaining p-type SnO_x and a higher O_2 content should change to n-type SnO_2 even in a poor O_2 atmosphere.

Figure 4.17 shows the variation of resistivity (ρ), mobility (μ) and carrier concentration (n) as a function of the oxygen content (%O_2) between 0% and 6.5% for a deposition pressure of 0.2 Pa, annealed at 200 °C. Below %O_2=2.5 %, the thin films were highly metallic due to the presence of Sn and with a poor adhesion to the corning glass substrate even upon the annealing step. With %O_2 between 2.5% and 4 % p-type conduction is achieved and above 4.0 % favors the films shows n-type conduction.

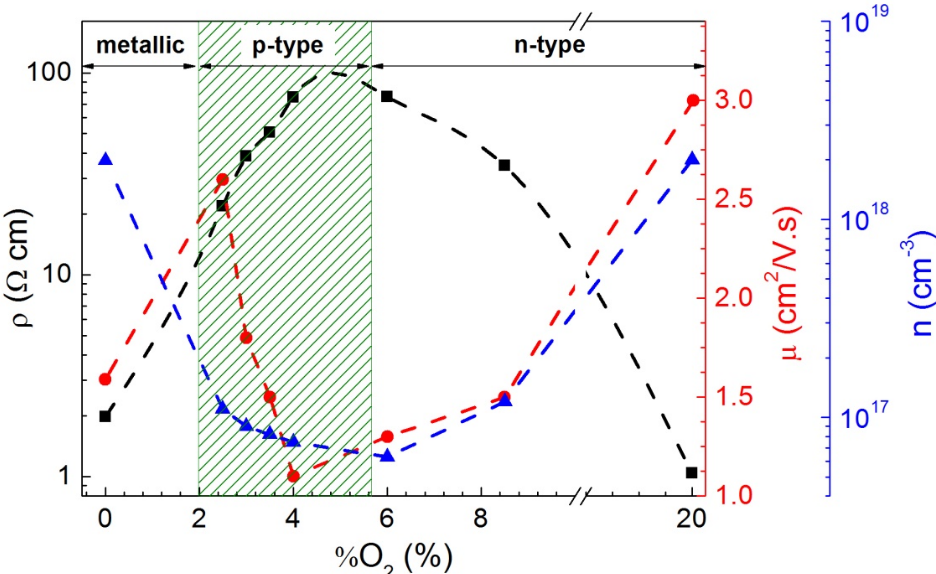

Figure 4.17. Variation of resistivity (ρ), mobility (μ) and carrier concentration (n) as a function of the oxygen content (%O_2).

For %O_2 between 2.5% and 4% the films are structurally composed by α-SnO phase and exhibited p-type conduction behavior with the resistivity, mobility and hole concentration, in the range of 22−76 Ω cm, 2.6−1.1 $cm^2/(V\ s)$ and 1.1×10^{17} to 7.5×10^{16} cm^{-3}, respectively. For this particularly range, as the content of oxygen increases, the resistivity increases, and both the mobility and the carrier concentration decrease.

From previous works it is known that the origin of p-type conductivity in SnO is due to interstitial oxygen, from the excess of oxygen, and tin vacancies (Sn_i). However, we observe that the hole concentration decreases with the increase of oxygen content which can only be explained as if the excess of oxygen is not resulting in interstitial oxygen that ionize to O_2 and work as acceptors

[15], but instead partial oxidation of Sn^{2+} occurs resulting in partial formation of oxygen deficient SnO_2. This result is in agreement with Togo et al, which states that Sn vacancies are the main contributors for the holes generation and not interstitial oxygen [16]. As $\%O_2$ increases the percentage of Sn^{4+} ions also increase and spontaneously act as donors or hole killers thus decreasing the concentration of holes, as observed [17]–[19]. The decrease on mobility could be related with the decrease of the grain size, as observed by the XRD diffractograms (see Figure 4.18). As the content of oxygen increases, the crystallite size decreases, improving the carrier scattering from grain boundary, thereby giving rise to the decrease of carrier mobility and film conductivity.

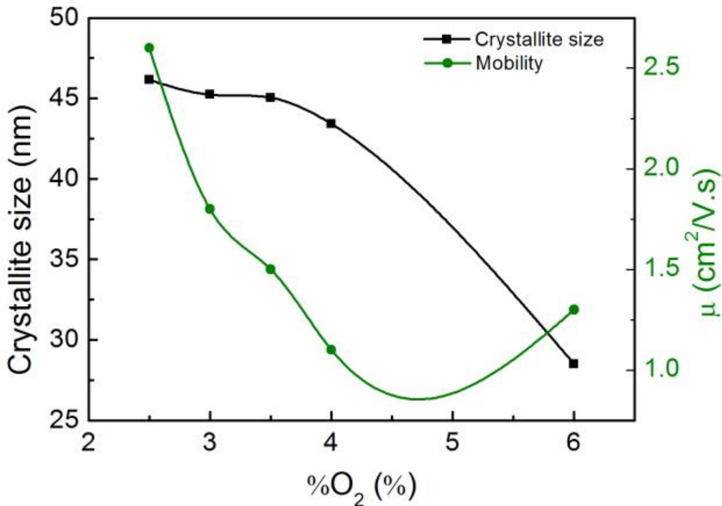

Figure 4.18. Variation of crystallite (D) size and mobility (μ)a function of the oxygen content (%O₂).

4.1.6.1.2 Deposition pressure (p_d)

Figure 4.19 shows the variation of resistivity (ρ), mobility (μ) and carrier concentration (n) as a function of the deposition pressure for an $\%O_2$=2.5%, annealed at 200 °C. as the deposition pressure increases the mobility and the carrier concentration decrease and the resistivity increases. The decrease on mobility is believed to be caused by the deterioration of crystallinity according to the XRD results, while the carrier concentration decrease can be justified by the lower sputtered particles, decreasing in this way, the ratio Sn/O which drive down the formation energy of tin vacancies (V_{Sn}) and drive them to the high density grain boundaries of higher deposition pressure deposited films.

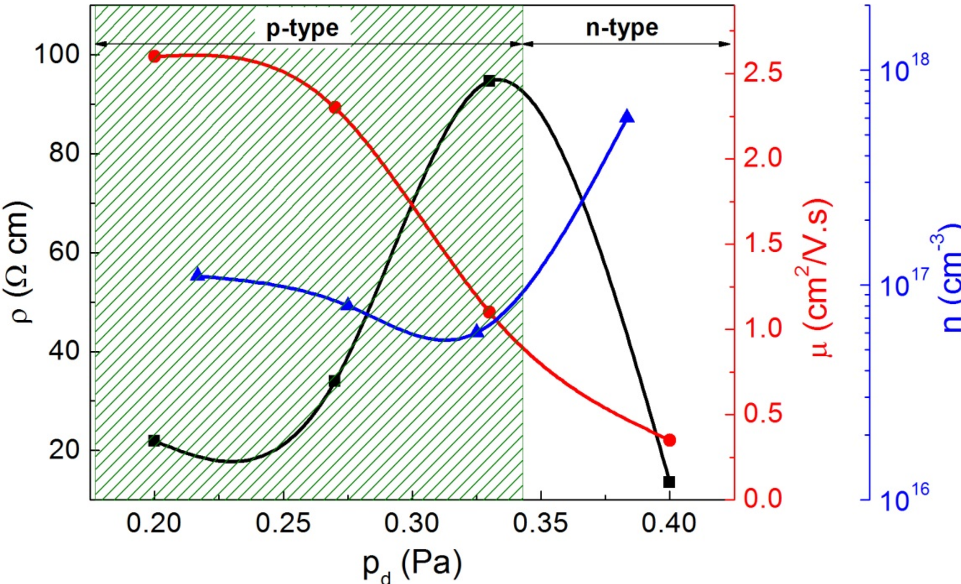

Figure 4.19. Variation of resistivity (ρ), mobility (μ) and carrier concentration (n) as a function of the oxygen content (%O_2).

4.1.6.1.3 Annealing temperature (T_A)

With the increase of the annealing temperature up to 200 °C, we can observe an increase on the resistivity and a decrease on carrier concentration. This is an expected result since the annealing temperature promotes first the crystallization of the film from metallic β-Sn to more resistive p-type α-SnO structure due to the oxidation of Sn to Sn^{2+} and Sn^{4+} ions, as observed from the XPS results shown on Figure 4.11.

For annealing temperatures between above 200 °C and below 400 °C it was not possible to obtain measurements from Hall Effect due to high resistivity nature of the films. For T_A=400 °C, the films shows a n-type behavior with a low resistivity and a higher carrier concentration.

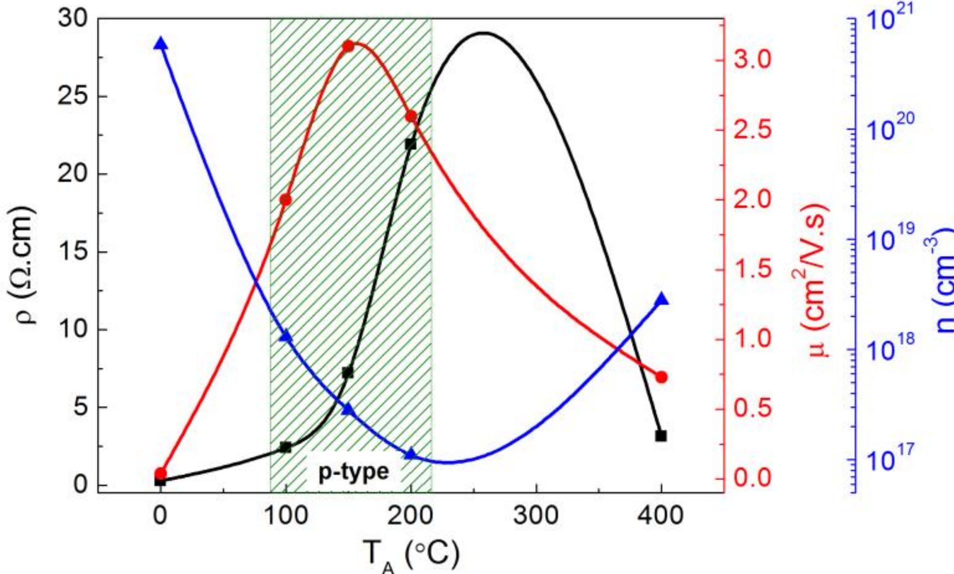

Figure 4.20. Variation of resistivity (ρ), mobility (μ) and carrier concentration (n) as a function of the annealing temperature(T_A).

Figure 4.21 shows the Arrhenius plots for p-type SnO_x samples with different $\%O_2$ annealed at T_A=200 ºC, which do not follow a simple thermally activated transport mechanism. The data could be fitted by a model with two conduction regimes. The first activation energy(E_{a1}) occurs at low temperature while the second is at high temperature. The second activation energy (E_{a2}), at high temperature, is controlled by a broad acceptor band located at energy Ea>VBM and partially assisted by phonons.

The values of the activation energy E_{a1} and E_{a2} are given in Table 4.3 and it was taken the slope of best fit straight line of these curves. The activation energies were determined by using Equation

$$\sigma = \sigma_o \left(exp - \frac{E_a}{K_B T} \right) \quad \textbf{(4.1)}$$

where E_a represent the activation energy, T is the temperature, K_B is Boltzmann`s constant, σ_o is the ideal conductivity of monocrystalline structure, and σ is the electrical conductivity.

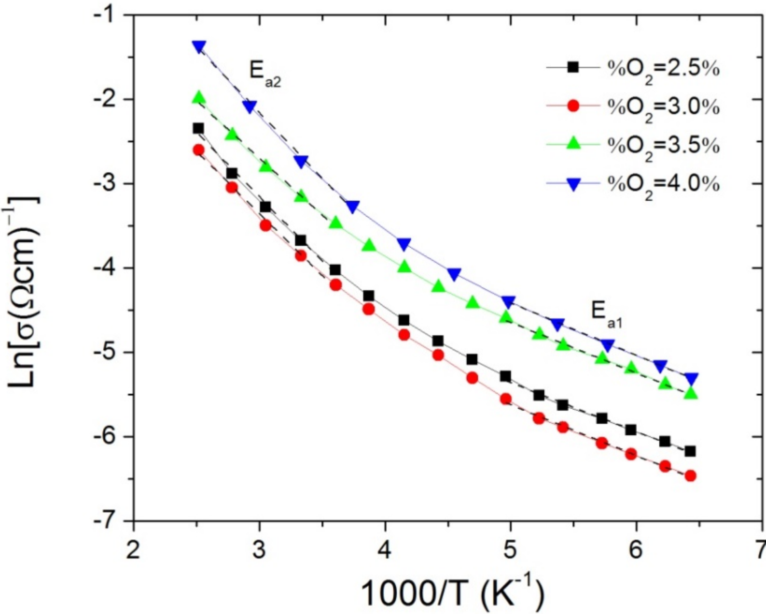

Figure 4.21. Temperature dependent dark conductivity for p-type SnO_x films with different $\%O_2$.

Under this condition we estimate E_{a1} between 0.050–0.053 eV and E_{a2} between 0.117-0.134 eV, which agrees with the Mott model where a localized disorder exists. The conductivity activation energies obtained are much larger than K_BT, which could be an indicative that the dominant transport mechanism is the thermionic emission of charged carriers.

Table 4.3. Activation energy calculated using the Arrhenius equation.

$\%O_2$ (%)	E_{a1} (eV)	E_{a2} (eV)
2.5	0.052	0.127
3.0	0.050	0.131
3.5	0.052	0.117
4	0.053	0.134

4.2. Oxide semiconductors based on Cu-doped SnO_x

4.2.1. Deposition parameters

Cu-doped SnO_x films were grown by reactive r.f magnetron sputtering at room temperature (RT) using an AJA, Model ATC ORION8 system without intentional heating. A 2" diameter Sn and Cu metals targets from Plasmaterials (with 99.999% purity) were used at 15 cm from the substrate. The deposition pressure ($Ar+O_2$) was kept constant as well as the Sn r.f. power (40 W). The r.f power applied to Cu target was varied between 6-40 W.

The film thicknesses were measured with a surface profilometer Sloan Tech Dektak 3. XRD experiments were performed in grazing incidence geometry using Cu *K*α1,2 lines, while optical measurements were performed with a double beam spectrophotometer in the wavelength from 200 nm to 2500 nm. Hall Effect measurements using the Van der Pauw configuration at room temperature were used to determine the resistivity, the carrier concentration and mobility of the majority carriers. Table 4.4 summarizes the parameters used for this study.

Table 4.4. Conditions used for the deposition of Cu-doped SnO_x thin films.

Targets	**Metallic tin and metallic copper (Plasmaterials, Inc,) purity= 99,999%, ϕ = 2", thickness = 3 mm**
Gases	argon oxygen
	Experimental conditions
Substrate temperature	No intentional heating
Target-substrate distance (cm)	15 cm
r.f. Power (W)	5 to 40
%Cu (%)	0 – 9
$\%O_2$ (%)	4.0
Deposition Pressure (Pa)	0.20

4.2.2. Dependence of the growth rate on the deposition parameters

Since the partial pressures of Ar and O_2, as well as the deposition pressure and r.f. power of Sn, while increasing the r.f. power of Cu in order to increase its content at SnO_x films, it is expected that the growth rate increases as the content of Cu increases as shown in Figure 4.22.

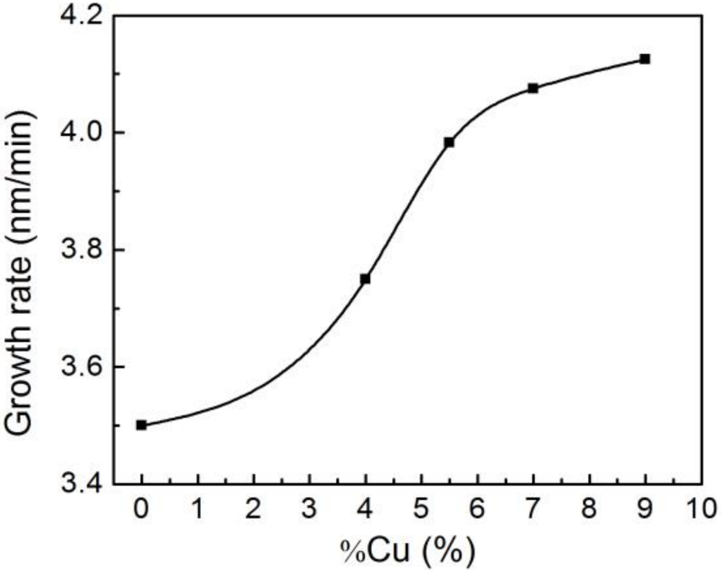

Figure 4.22. Growth rate as function of %Cu.

4.2.3. Compositional analysis

- *Percentage of Cu (%Cu) in the Sn+Cu mixture*

The composition of Cu-doped SnO_x thin films were analyzed by EDS and RBS. The results from EDS are represented at Figure 4.23. As the r.f. power of Cu target is increased the content of Cu also increases on the thin films.

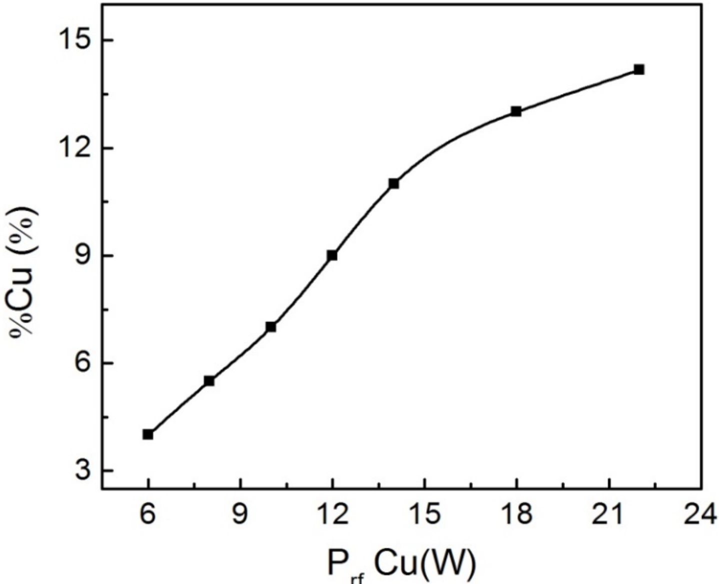

Figure 4.23. Atomic concentrations obtained by EDS of Cu, on Cu doped SnO_x thin films.

Rutherford backscattering (RBS) was used in order to characterize the chemical composition of Cu-doped SnO_x samples. RBS experiments were performed in a 2.5 MV van de Graaff accelerator using a 2.0 MeV He+ beam and silicon solid state detector with 20 KeV energy resolution located at 165° with respect to the beam direction.

The angle of incidence, defined as the angle between the beam and the normal of the sample, was fixed constant at 0°. The current in the sample was kept below 3 nA and the charge accumulated in the spectra was 2 μC.

Figure 4.24 shows the RBS sprectrums, analyzed with the IBA DataFurnace NDF software [20], for the non-doped film and Cu-doped SnO_x films with a content of Cu of 4.0% and 7.0% as deposited and annealed at T_A=200 °C. We can observe from Figure 4.24 that as the P_{rf} (Cu) increases, the %Cu also increases, as expected.

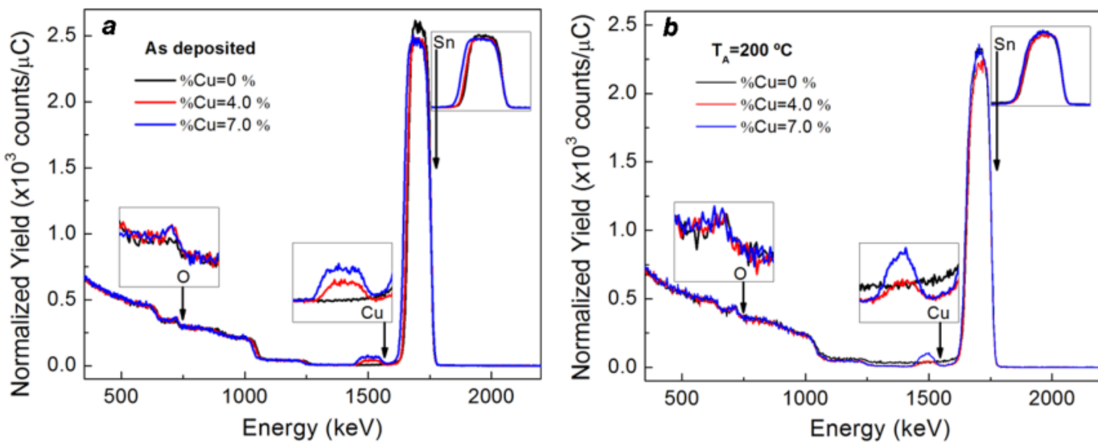

Figure 4.24. RBS spectrum for the Cu-doped SnO_x films deposited at p_d=0.2 Pa as a function of %Cu a) as deposited and b) annealed at 200 °C.

From Figure 4.25, we can observe that Cu-doped SnO_x films annealed at T_A=200 °C, mainly for the film with %Cu=7.0 %, the shape of Cu peak is different and it shifts toward lower energies whereas the tin signal decreases at its surface edge. This could be an indicative of growth and formation of copper free tin oxide and/or some deagglomeration of Cu and metallic Sn, in contrary to what has been observed when doping other elements with Cu in order to produce oxide materials, $Cu_xA_yO_z$ (A=Ta,Va) [21][22].

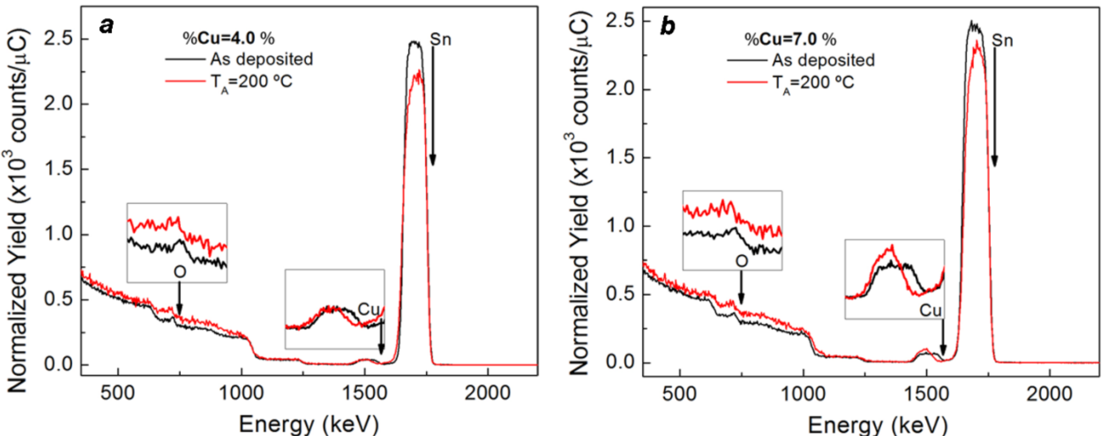

Figure 4.25. RBS diffractograms for the Cu-doped SnO films deposited as deposited and annealed at 200 °C for a) %Cu=4.0 % and b) %Cu=7.0 %.

4.2.4. Structural and morphological properties

4.2.4.1 Influence of the deposition parameters

- *Percentage of Cu (%Cu) in the Sn+Cu mixture*

Figure 4.26 shows the X-ray diffraction (XRD) pattern for the p-type Cu-doped Sn thin films as deposited and annealed at T_A=200 °C, deposited at p_d = 0.20 Pa and $\%O_2$=4.0 % as a function of Cu content. As deposited, non-doped film shows high intensity peaks corresponding to (200) and (101) peaks of metallic β-Sn (ICDD card No 98-004-0673). As the content of Cu increases, we observe a decrease of (101) and (200) peak intensities resulting in a single peak corresponding to the (011) peak of Cu_6Sn_5 alloy (ICDD card No 98-008-1512).

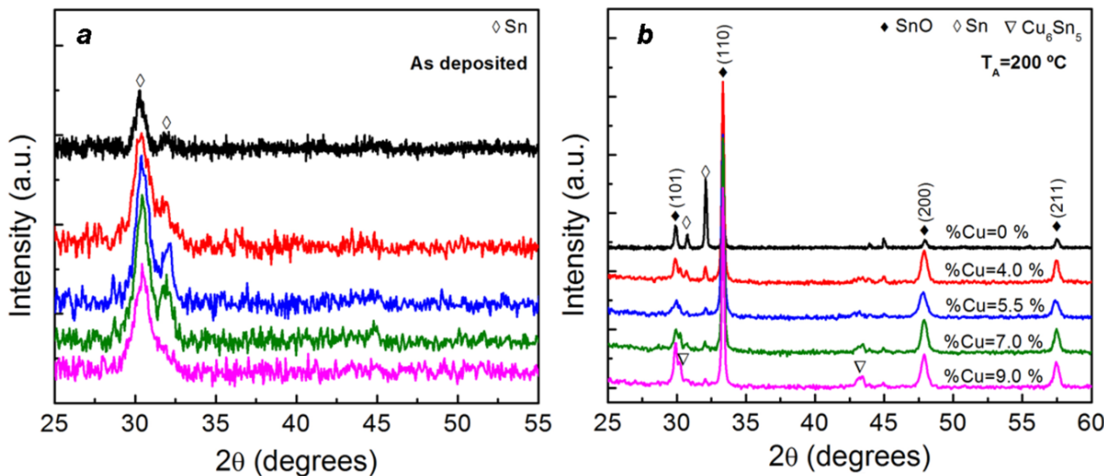

Figure 4.26. XRD diffractograms for the Cu-doped SnO_x films deposited at p_d=0.2 Pa as a function of %Cu a) as deposited and b) annealed at 200 °C.

After annealing at 200 °C and similar to what was observed at (4.1.3) the diffraction peaks of the non-doped film can be addressed to α-SnO preferentially oriented with (110) plane and metallic β-Sn. With Cu increasing, the intensity of α-SnO (110) keeps constant, and, while the metallic Sn phase decreases, a new peak appears at the peak 2θ~ 30.2 corresponding to Cu_6Sn_5 (011) peak (see Figure 4.27).

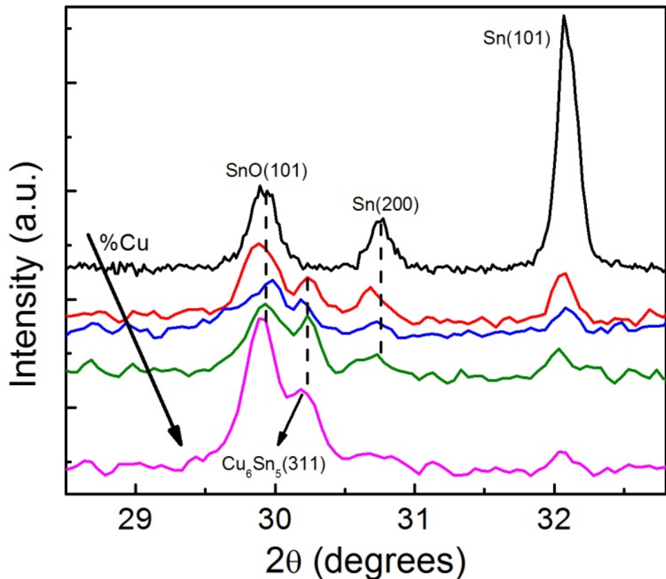

Figure 4.27. XRD diffractogram of the main α−SnO peaks for the Cu-doped SnOx films annealed at 200 °C.

Figure 4.28 a) presents the crystallite size (*D*) estimated using the Scherrer's equation for the peaks (200) and (101) of β-Sn phase and b) the peaks (101) of α-SnO phase for the films annealed at T_A=200 °C. As the content of Cu increases, the grain size corresponding to peak β-SnO decreases, while for the (101) α-SnO, the grain size accomplish the incorporation of Cu into the Sn matrix. First decreases until %Cu=5.5 % due to the disturb caused by Cu (double peak), increasing when adding more Cu (more intense double peak), until the final rearrangement is achieved.

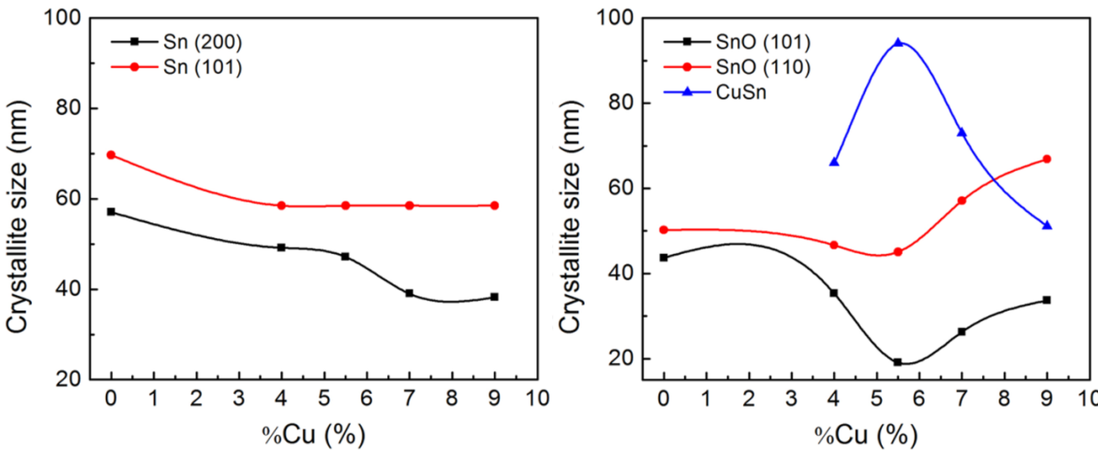

Figure 4.28. Dependence of grain size for β-Sn and α-SnO peaks with %Cu for the films deposited at pd= 0.20 Pa, %O_2=4 % and T_A=200 °C.

Figure 4.29 shows the SEM images of Cu-doped SnO_x films as deposited and annealed at 200 °C for different contents of copper.

The as deposited thin films shows very similar surface and despite the increase on Cu content we can only observe some small grains at the surface. After the annealing, the films surfaces changes considerably, resulting on a grain growth at the SnO_x films. When we had the doping element to SnO_x we can observe bigger grains with 40-45 nm, increasing to 50 nm for %Cu=5.5% and then decreasing again for higher contents of Cu. We can also observe for the doped films smaller grains of 20-25 nm. This could correspond to a mixture of phases of SnO and Cu_2O in the film as discussed from RBS results.

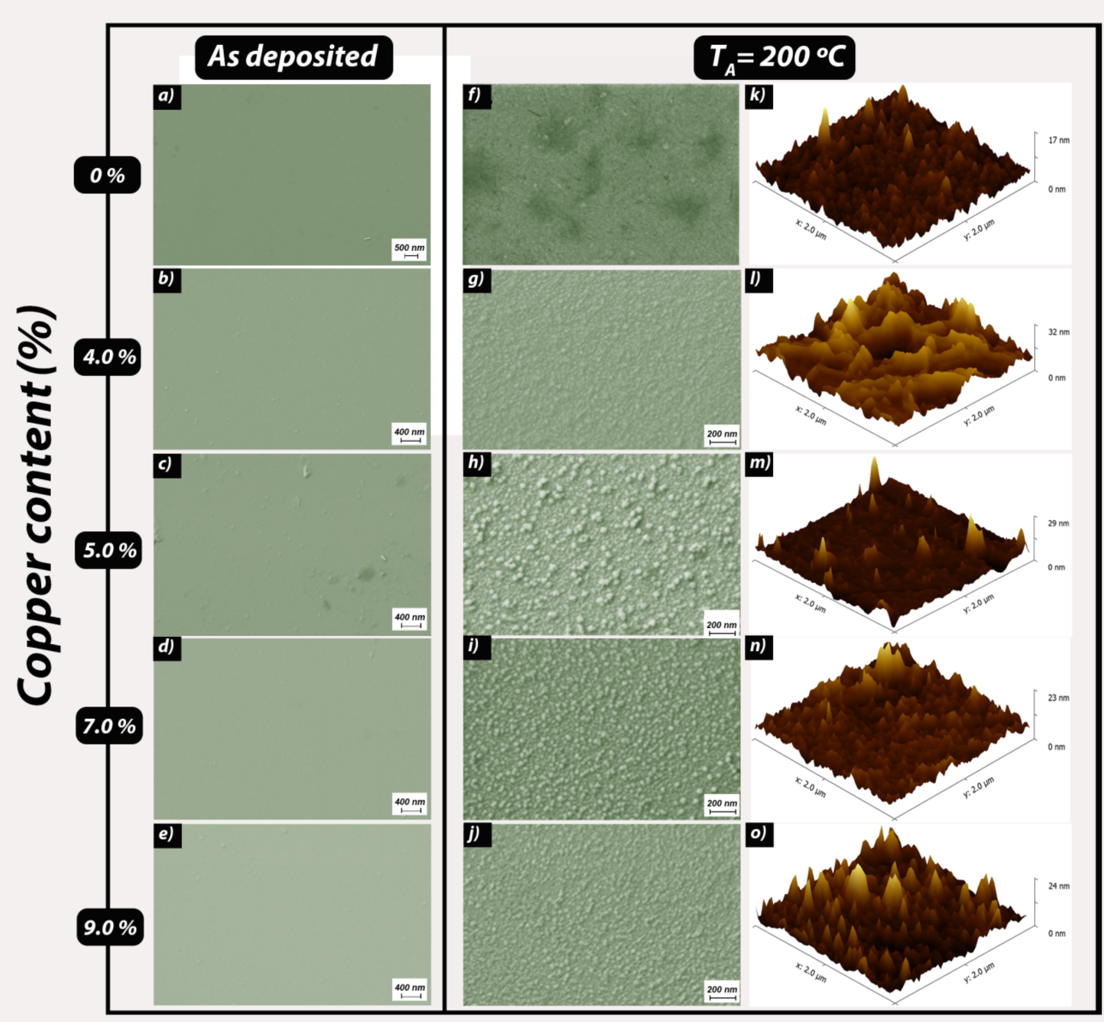

Figure 4.29. SEM images of the films deposited at p_d= 0.2 Pa, %O_2=2.5 %; a) – e) as deposited, f) - j) annealed at T_A= 200 °C; and k) - o) AFM images annealed of the films annealed at T_A= 200 °C

4.2.5. Optical properties

Figure 4.30 a) and b) shows the transmittance spectra between 350 and 2500 nm of the Cu-doped SnO_x thin films as deposited and annealed at T_A=200 °C as a function of Cu content and Figure 4.31 shows the pictures of the same films. Similarly as in the case of undoped films, the optical transmittance of as deposited thin films is very poor with a very low mean transmittance in the visible region; attributed to the presence of metallic tin. After annealing at T_A=200 °C, the optical transmittance of the thin films in the visible region increases considerably.

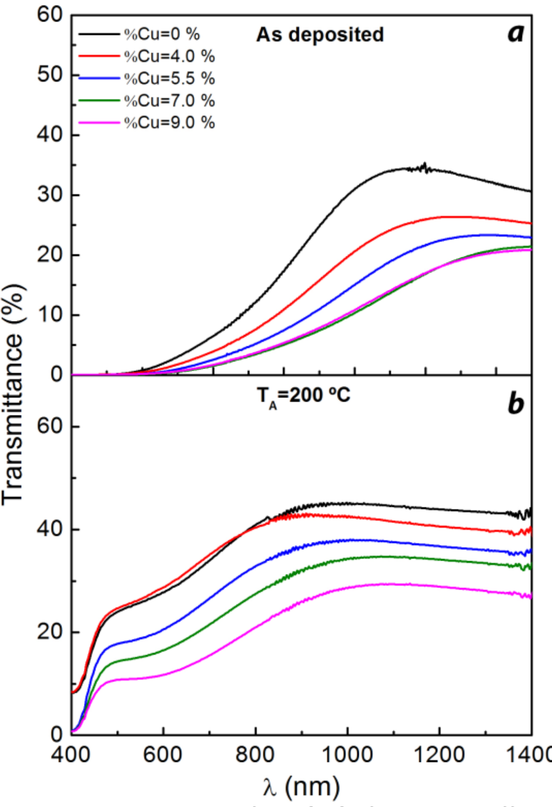

Figure 4.30. Optical transmittance spectra of the SnO_x films with different content of copper a) as deposited and b) annealed at 200 °C.

At Figure 4.31 we can observe the pictures of the films as deposited and at Figure 4.32 the films annealed at T_A=200 °C, with different contents of copper.

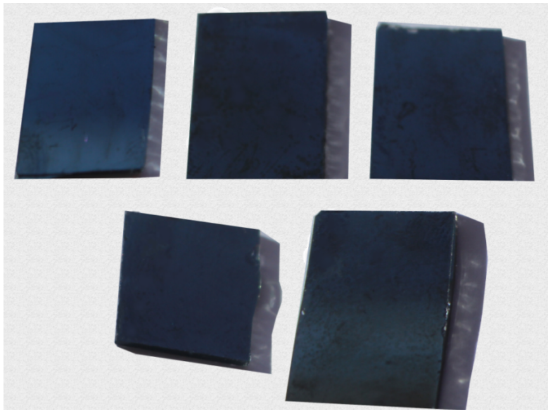

Figure 4.31. Picture of the thin films as deposited with a %Cu of a) 0 %, b)4.0 %, c) 5.5 %, d) 7.0 % and e) 9.0 %

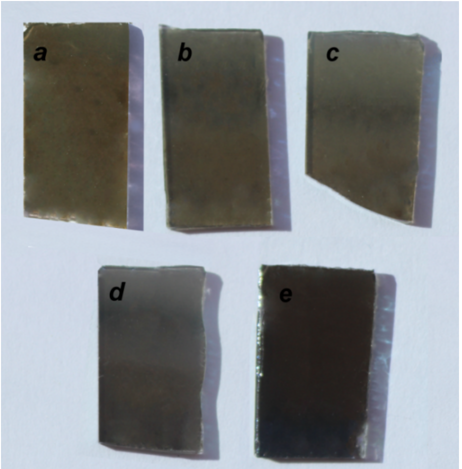

Figure 4.32. Picture of the thin films annealed at T_A=200 °C with a %Cu of a) 0 %, b)4.0 %, c) 5.5 %, d) 7.0 % and e) 9.0 %

The optical band gap (E_{opt}) of Cu-doped SnO_x thin films represented at Figure 4.33 c) was calculated using the Tauc law: $\alpha^x = (h\nu - E_{opt})$ extrapolating the linear region of the $(\alpha h\nu)^2$ versus hν plot, represented at Figure 4.33 a) and b). For the as deposited films, as the %C increases, E_{opt} decreases due to light absorption of Cu. After the annealing, all the films present higher E_{opt}, that can be explained by the oxidation of metallic Sn and Cu. We can also observe that for higher %Cu, E_{opt} slightly decreases due to the Cu oxide nature, which has a lower E_{opt} than SnO_x films [23].

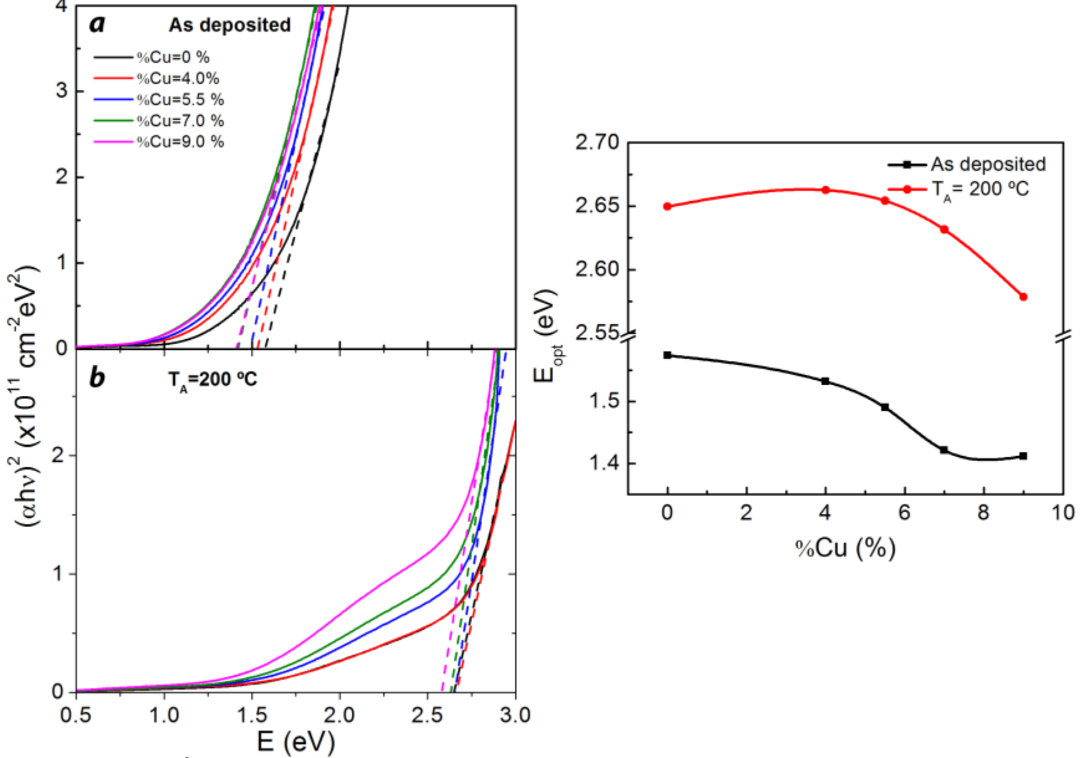

Figure 4.33. $(\alpha h\nu)^2$ vs photon energy (hν) spectra for the films a) as deposited and b) annealed at 200 °C and c) calculated optical bandgap as a function of copper content for the thin films.

4.2.6. Electrical properties

Figure 4.34 shows the resistivity, hall mobility and carrier concentration of the produced thin films as deposited and annealed at 200°C as a function of %Cu. These transparent and conductive oxide films, resulting from doping SnO_x with Cu, have n-type and p-type conductivity depending on the annealing temperature. As deposited, the thin films present a n-type behavior and annealing at T_A=200°C, a p-type behavior is achieved for the undoped thin film and the doped thin films with %Cu between 4.0% and 7.0%. The thin film doped with 9% always shows n-type behavior.

As the content of Cu increases, the mobility in enhanced to 1.91 cm^2/Vs , the resistivity of the p-type SnO_x film drops from 75.7 to 9.35 Ωcm^{-1} and the carrier concentration increases from $7.5x10^{16}$ cm^{-3} to $3.5x10^{17}$ cm^{-3} to %Cu=7.0 %. The enhancement of Hall mobility upon doping is induced by an increase in grain size because the dopants promote the grain growth rate.

Despite is not observed at the XRD diffractograms, and has discussed before, we could have some oxidized Cu after the annealing at T=200 °C, that despite its phase, Cu_2O or CuO will always contribute with holes due to its p-type conduction, resulting on the increase of free carrier concentration.

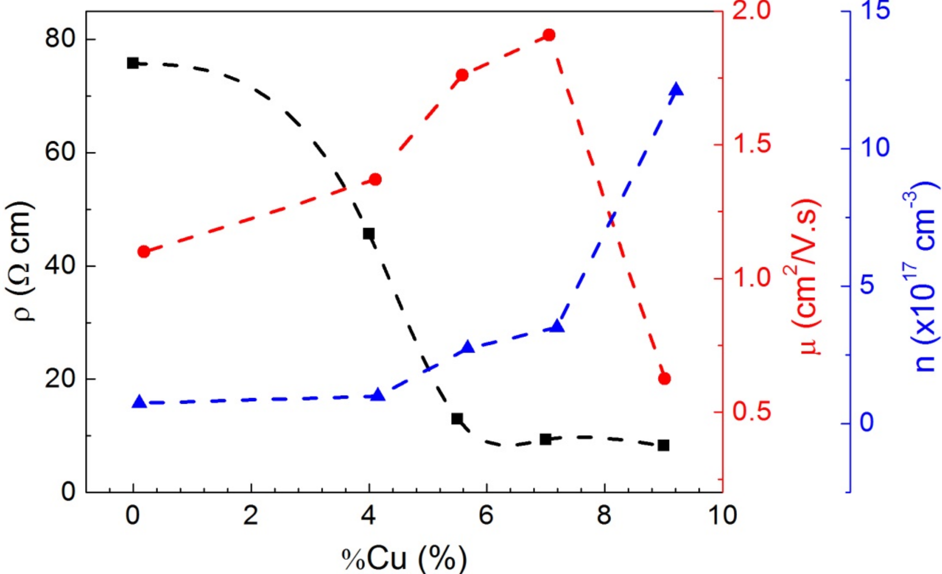

Figure 4.34. Variation of resistivity (ρ), mobility (μ) and carrier concentration (n) as a function of copper content (%Cu).

4.3. Oxide semiconductors based on In-doped SnO_2

4.3.1. Deposition parameters

In-doped SnO_2 films were grown by reactive r.f magnetron sputtering at room temperature (RT) using an AJA, Model ATC ORION8 system without intentional heating. A 2” diameter ceramic SnO_2 and a metallic Sn targets from Plasmaterials (with 99.999% purity) were used at 15 cm from the substrate. For this study, p_d was kept constant and $\%O_2$ and %In was varied. Similarly to Cu-doped SnO_x depositions, the r.f. power applied to the dopant target, In, was varied in order to obtain films with different %In. Table 4.4 summarizes the parameters used for this study.

Table 4.5. Conditions used for the deposition of In-dopedSnO_2 thin films.

Targets	**Tin oxide (SnO_2) and metallic indium, (Plasmaterials, Inc,)** **purity= 99,999%, ϕ = 2”, thickness = 3 mm**
Gases	argon oxygen

Experimental conditions

Substrate temperature	No intentional heating
Target-substrate distance (cm)	15 cm
r.f. Power(W)	SnO_2 – 50 In – 4 to 20
%In (%)	15 – 38
$\%O_2$ (%)	5.0-7.0
Deposition Pressure (Pa)	0.20

4.3.2. Electrical properties

Figure 4.35 shows the resistivity, hall mobility and carrier concentration of the produced thin films as deposited as a function of In content for $\%O_2$=5.0 and 7.0%. As seen in this figure, the conducting types were dependent on In and oxygen contents. For $\%O_2$= 5 %, the films showed p-type conducting at lower doping levels (%In =15 - 21%) and as %In increases, both resistivity and mobility decrease and the carrier concentration increases. The resistivity is between 52.6 and 0.35 Ωcm, mobility between 26.3 and 0.862 $cm^2V s^{-1}$and carrier concentration between 4×10^{15} and 2×10^{19} cm^{-3}, respectively, but the films showed n-type again at higher doping levels. For low %In,

In^{3+} plays as acceptor, which makes the films p-type and further increase of %In ratio should lead to the an excess of indium oxide phase in the films, which became n-type.

When increasing $\%O_2$ to 7%, p-type behavior is observed for the films with higher content of In, which can be explained by considering the co-existence of donors (intrinsic defects such as oxygen vacancies and tin interstitials) and acceptors (substitution of Sn by In) in the films. For higher content of indium and lower $\%O_2$, indium atoms were not activated to behavior as acceptors, so the films were n-type because of the intrinsic defects. But when increasing the content of oxygen the acceptor effect of In^{3+} substituting Sn^{4+} was activated, which resulted in the p-type conducting of the films. In this case, a remarkable performance was achieved for %In=26 % for a p-type oxide material, since the material has a resistivity of 5.1×10^{-3} Ωcm, mobility of 22.8 $cm^2V s^{-1}$ and carrier concentration of 5.4×10^{19} cm^{-3}.

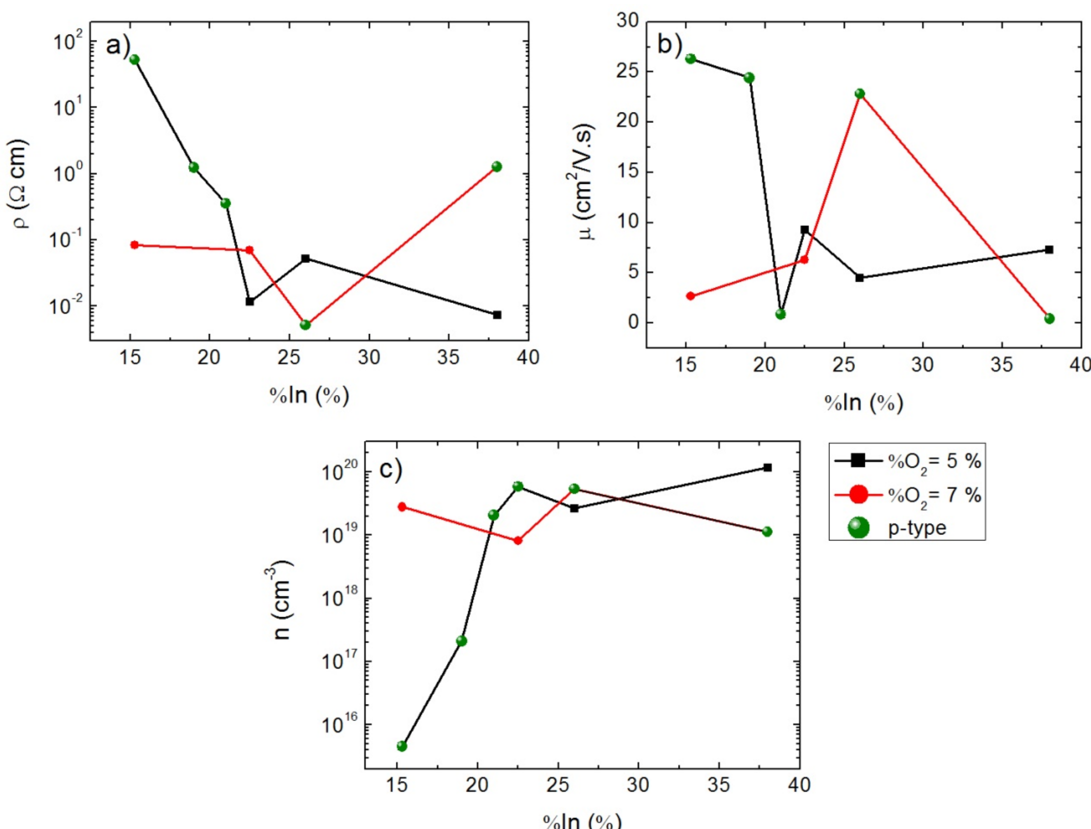

Figure 4.35. Variation of a) resistivity (ρ),b) mobility (μ) and c) carrier concentration (n) as a function %In for different $\%O_2$.

4.3.3. Compositional analysis

- *Percentage of In (%In)*

The composition of Cu-doped SnOx thin films were analyzed by EDS. The results from EDS are represented at Figure 4.36. As the r.f. power of In target is increased the content of In also increases on the thin films.

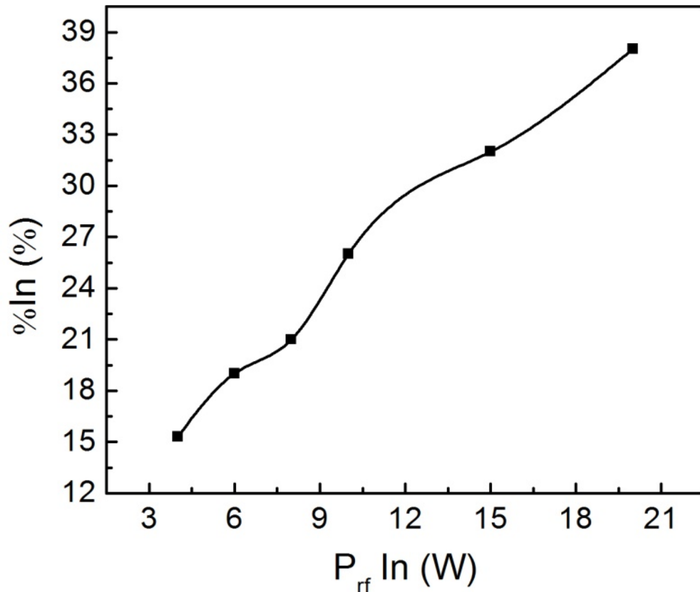

Figure 4.36. Atomic concentrations obtained by EDS of In, on In-doped SnO_2 thin films.

As in (4.1.4) X-ray photoelectron spectroscopy (XPS) was performed using monochromatic Al Kα radiation with energy of 1486.6 eV and an overall energy resolution of less than 0.4 eV. Binding energies are reported with respect to the Fermi level, which was calibrated measuring a sputter cleaned metallic silver sample. In order to compare the content of the elements present, the oxidation states and the VBM position, samples with different conductivity (p-type and n-type) were chosen from this study and were compared with the p-type SnO_x film measured at 4.1.4.

Table 4.6. Electrical properties of the samples chosen to XPS measurements.

	%In (%)	$\%O_2$ (%)	ρ (Ω cm)	μ (cm^2/Vs)	n (cm^{-3})
n-type TIO	26	5	5.22×10^{-2}	4.51	2.66×10^{19}
p-type TIO	15	5	5.26×10^{1}	26.3	4.51×10^{15}
SnO_x	0	4	75.8	1.1	7.50×10^{16}

As seen from the survey scan spectra in Figure 4.37, only Sn, In and O elements were observed except for a small amount of C due to air contact at 285 eV. Figure 4.38 shows the O1s, Sn $3d_{3/2}$, Sn $3d_{5/2}$ and In $3d_{5/2}$ XPS spectra.

Figure 4.38 shows the O1s, Sn $3d_{3/2}$, Sn $3d_{5/2}$ and In $3d_{5/2}$ XPS spectra and Figure 4.39 shows the fitting results of Sn $3d_{5/2}$ XPS spectra of the three films. The n-type TIO film Sn $3d_{5/2}$ XPS spectra could not be fitted with two components, so no SnO is assumed to be present. Even though this films has n-type conductivity, the percentage of the elements is still far from the ones typical of the known TCO tin-doped indium oxide (ITO) [24].

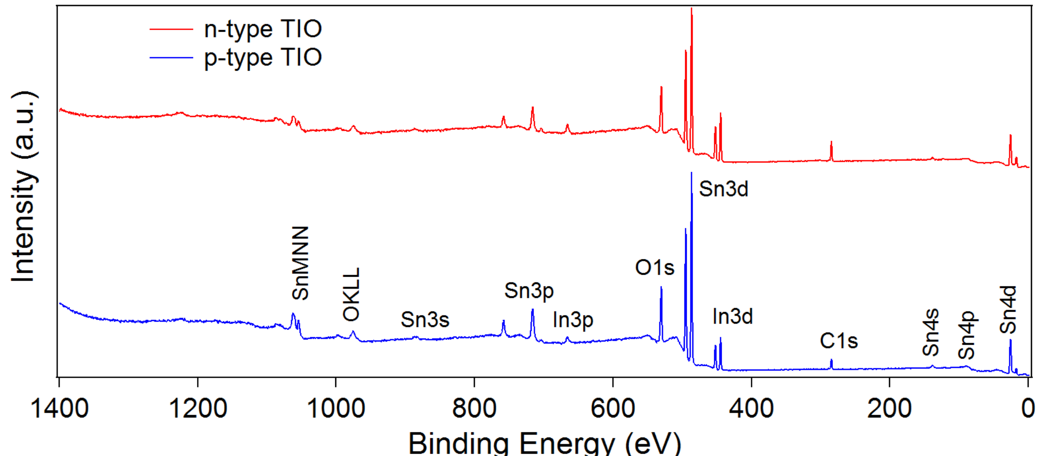

Figure 4.37. XPS survey spectra of tin oxide films as deposited and annealed prepared by reactive magnetron sputtering.

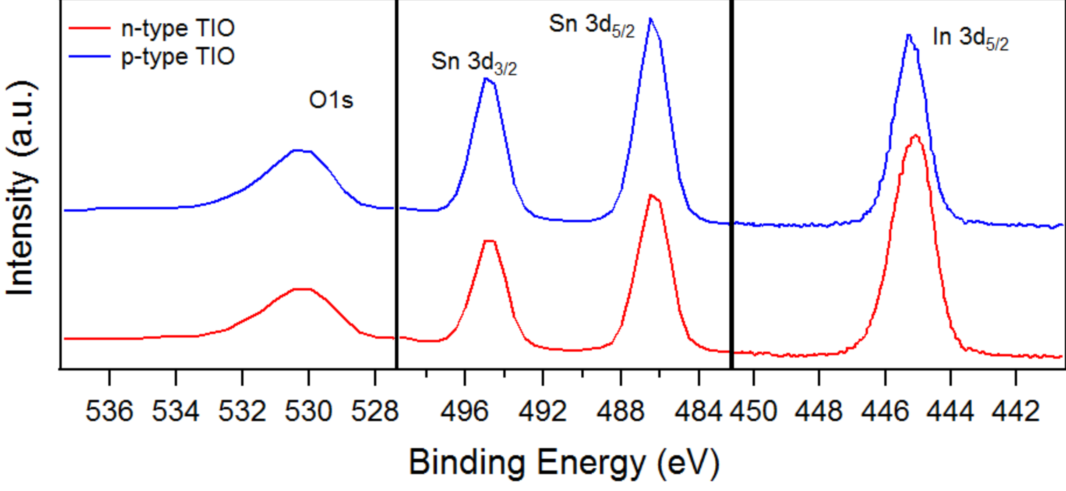

Figure 4.38. O1s, Sn $3d_{3/2}$,Sn $3d_{5/2}$ and In $3d_{5/2}$ XPS spectra of n-type and p-type In-doped SnO_2 films.

For the p-type TIO film, two peaks were clearly resolved. Curve-fitting analysis shows that one peak is located at 486.6 eV and another one at 487.3 eV, corresponding to different oxidation states of Sn^{2+} and Sn^{4+}, like it is observed for the p-type SnO_x. Table 4.7 summarizes the atomic percentages of the elements for the as deposited and annealed film.

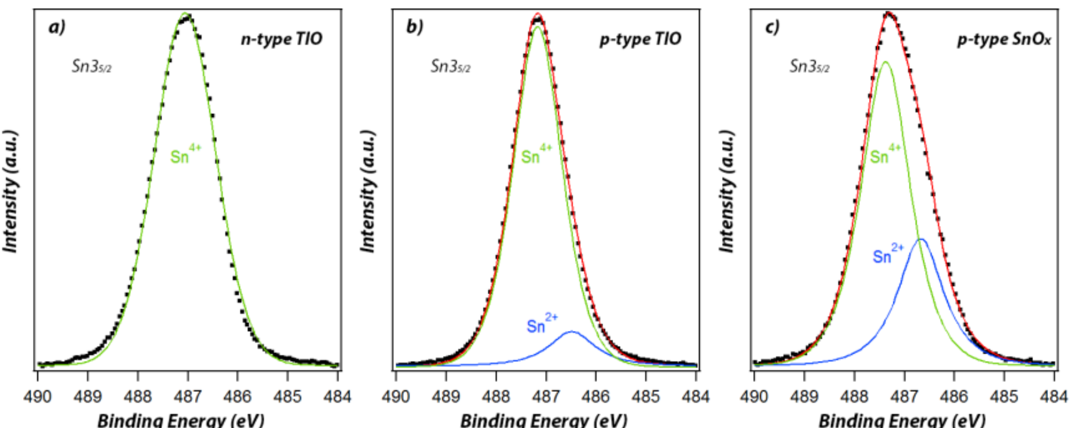

Figure 4.39. XPS spectra of Sn $3d_{5/2}$ for (a) n-type and (b)p-type In-doped SnO_2 and for c) SnO_x p-type. Smooth lines are representing fitting data.

Table 4.7 summarizes the atomic percentages of the elements for the thin films produced and annealed at T_A=200ºC. Even though this films has n-type conductivity, the percentage of the elements is still far from the ones typical of the known TCO tin-doped indium oxide (ITO) [24]. The values O (-In) and O (-Sn) have been calculated by assuming indium to be completely oxidized to In2O3, which appears to be reasonable when considering the line shape of the $In3d_{5/2}$ emission. O% (-Sn) is then equal to O% minus 3/2 In%. Under this assumption, the tin to oxygen ration Sn/O is 0.57 for both n- an p-type TIO samples while p-type SnOx has a slightly higher Sn/O ratio of 0.6.

Table 4.7. Content of O, Sn and In in the n- and p- type In-doped SnO_2 films and in the SnOx films annealed.

	O (%)		Sn (%)	In (%)	Sn/O_Sn
n-type TIO	62.86		27.47	9.67	56.8
	O (-In)	*O (-Sn)*			
	14.50	48.36			

	O (%)		Sn (%)	In (%)	Sn/O_Sn
p-type TIO	63.28		31.10	5.62	56.7
	O (-In)	*O (-Sn)*			
	8.43	54.85			

	O (%)	Sn (%)		Sn/O_Sn
SnO_x	62.36	37.64		60

Figure 4.40 shows the graphical method used to evaluate the VBM position. The VBM for the n-type TIO film is similar to what is reported for n-type SnO_2 on literature [25], [26]. Valence band maxima in p-type TIO and SnO_x are both at ~1.2 eV, the hump at 2-3 eV is less pronounced in p-type TIO than in SnO_x.

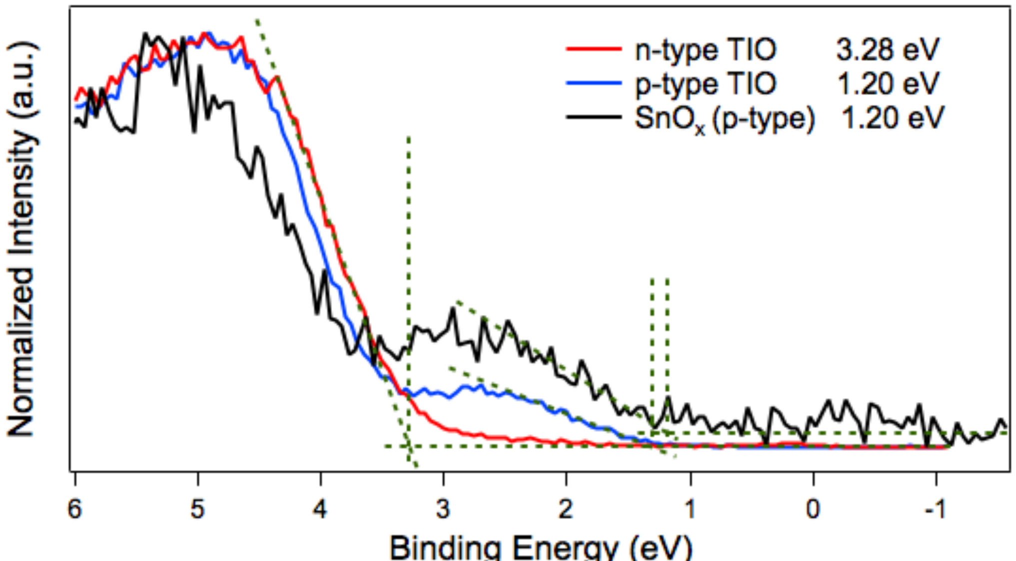

Figure 4.40. Valence band spectra of SnO_x and In-doped SnO_2 films.

4.3.4. Structural and morphological properties

4.3.4.1 Influence of the deposition parameters

Regardless the %In and %O_2, all the In-doped SnO_2 films produced are amorphous, as exemplified in Figure 4.41.

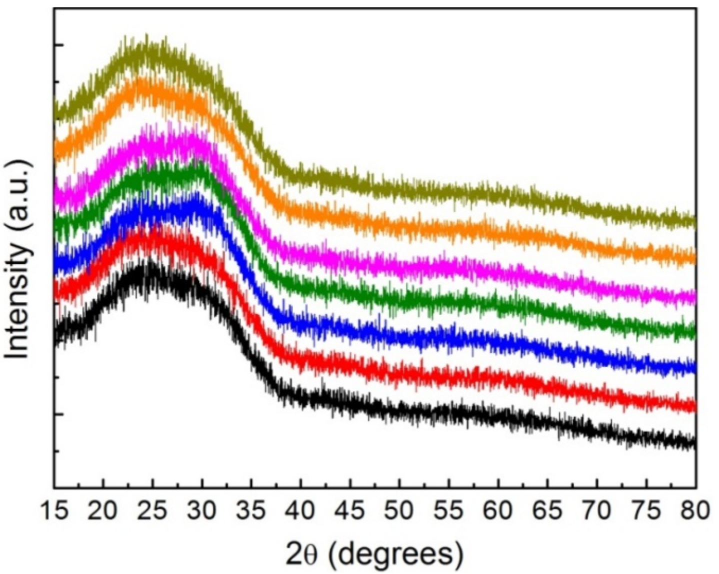

Figure 4.41. XRD diffractograms for the In-doped SnO_2 films deposited at different %O_2 and %In.

Figure 4.42 shows the SEM images of In-doped SnO_2 films for different contents of indium. Due to the amorphous nature of the films, no significant differences are observed,

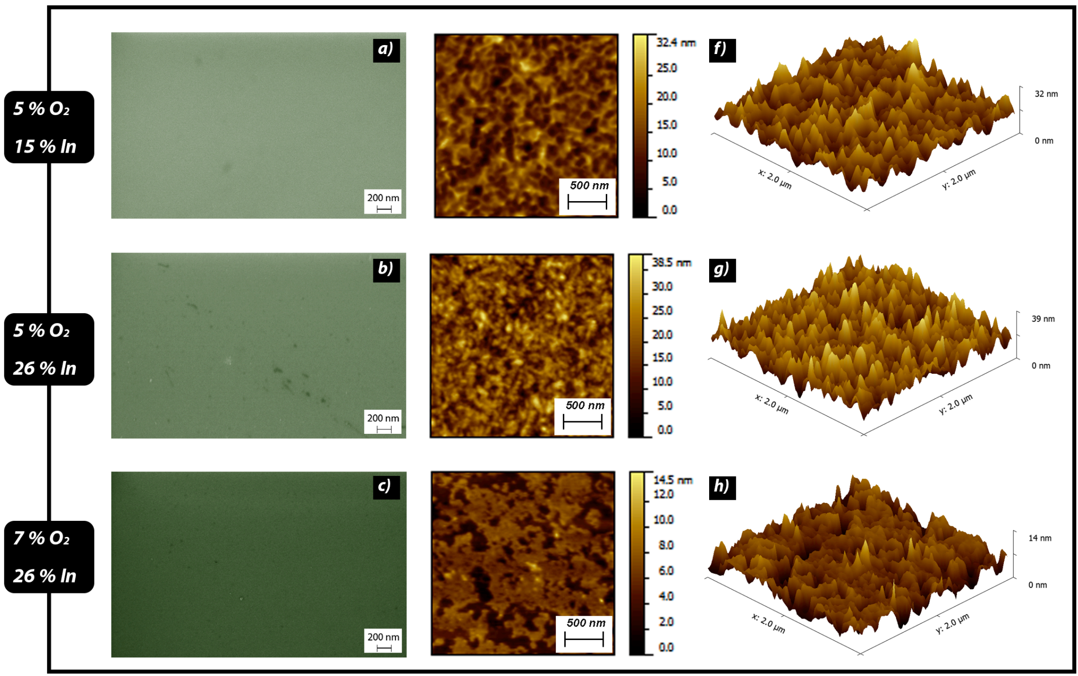

Figure 4.42. a) – c) SEM and f) – h) AFM images of In.doped SnO_2 films with $\%O_2$=5.0 – 7.0 % and %In=15 – 26%.

4.3.5. Optical properties

Optical transmittance spectra between 350 and 2500 nm of In-doped SnO_2 thin films as a function of In content is shown at Figure 4.43. For the films with $\%O_2$=5 %, T_{mean} in the visible range is between 65-70% and increases up to ~80% for $\%O_2$=7 %. Regardless $\%O_2$, as the content of indium increases also the mean transmittance increase.

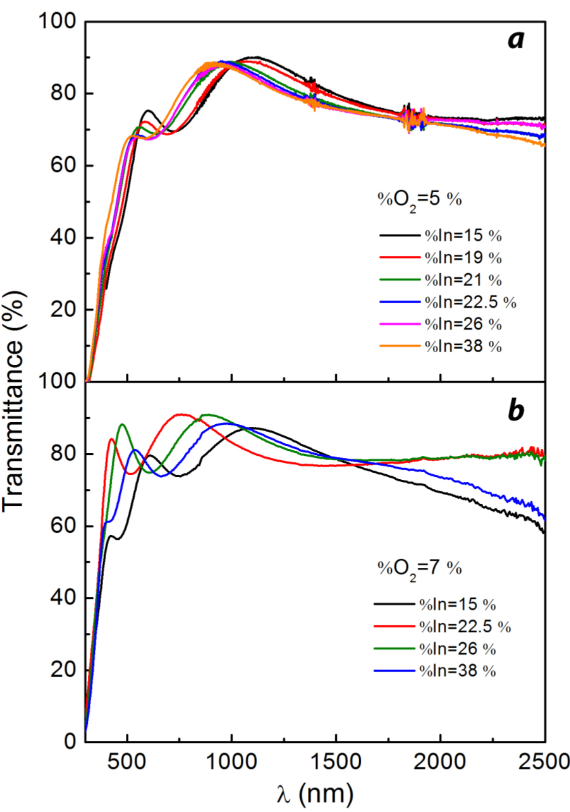

Figure 4.43. Optical transmittance spectra of In-doped SnO_2 films with different content of In for a) $\%O_2$=5 % and b) $\%O_2$=7 %.

At Figure 4.44 we can observe the pictures of the films with $\%O_2$=7% for different contents of In. As we can observe, the films produced with $\%O_2$=7% are more transparent in the visible range.

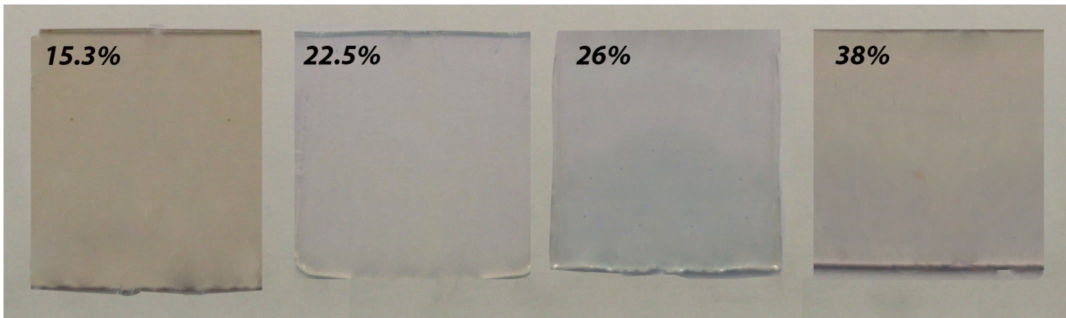

Figure 4.44. Picture of the thin films deposited with $\%O_2$=7%.

Figure 4.45 shows the optical band gap (E_{opt}) of In-doped SnO_2 thin films calculated using the Tauc law: $\alpha^x = (h\nu - E_{opt})$ extrapolating the linear region of the $(\alpha h\nu)^2$ versus $h\nu$ plot. For the films with higher oxygen content, E_{opt} is higher which can be explained by the more oxidation of In.

For both $\%O_2$, as the %In increases, E_{opt} increase due to the presence of more In_2O_3, and the formation of ITO material, presenting a higher E_{opt}.

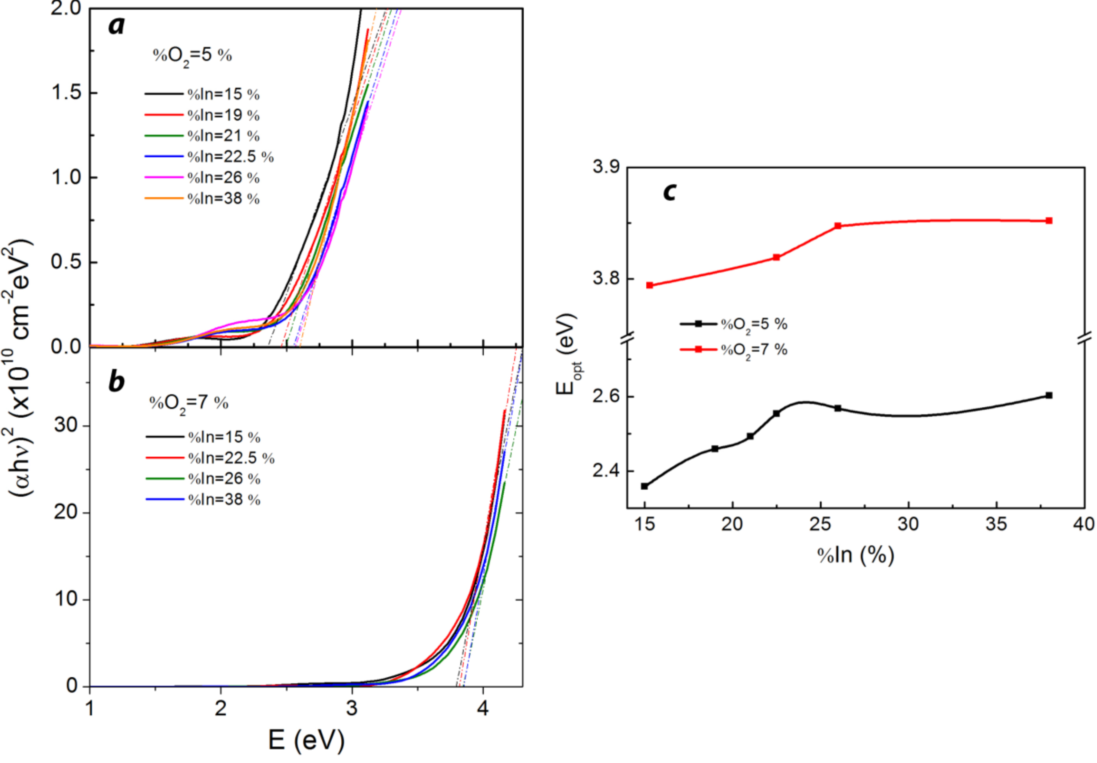

Figure 4.45. **$(\alpha h\nu)^2$ vs photon energy (hν) spectra of In-doped SnO_2 films with different %In for a) $\%O_2$=5 % and b) $\%O_2$=7 %; c) calculated optical bandgap as a function of In content.**

4.4. Conclusions

In this chapter were analyzed the influence of different process and post-process parameters on the properties of SnO_x based films.

<u>SnO$_x$</u>

- The growth rate is strongly influenced by the deposition parameters, since the introduction of oxygen and higher deposition pressures results in a lower growth rate. The reduction with the oxygen content when sputtering metal oxides could be due to the re-sputtering of the atoms from the film surface by energetic O^- ions, since the increase of oxygen content at the deposition chamber, more O^- ions are available leading to a higher re sputtering and a decrease in the deposition rate.. Another explanation is that higher O_2 content means less quantity of Ar and consequently an increase of unionized neutral oxygen atoms. These neutral O_2 atoms collide with the sputtered particles consuming their energy. Consequently, these particles diffuse to low energy positions without enough energy to reach the substrate, resulting in lower deposition rate.

- An increase on the oxygen content also affects the structural properties of the material, leading to a lower crystallinity of the thin films and consequently to a decrease at the crystallite size. For low contents of O_2, the diffraction peaks can be addressed to β-Sn and to α-SnO preferentially oriented with (110) plane As the content of oxygen increase, both the intensity of α-SnO and β-Sn phases decrease until an amorphous structure is observed. The decrease on crystallinity of α-SnO phase could be justified considering that the incorporation of O_2 results on the oxidation of Sn^{2+} to Sn^{4+} (SnO to SnO_2) and that SnO_2 could be amorphous for annealing temperature of 200°C. The increase on p_d also contributes for a decrease on crystallinity of the thin films due to the reduced sputtering particles. For lower deposition pressure, the mean free paths of the particles in plasma is higher and fewer collisions occur within the plasma resulting in a higher adatom mobility of the deposited films and resulting in a better crystalline quality. The crystallinity of the films is strongly affect by the annealing temperature. While for the as deposited thin films, the diffraction peaks correspond only to metallic tin (β-Sn) and after annealing at T_A=200°C, the metallic tin is partially oxidized to α-SnO, where, impurities due to metallic Sn are still present at the thin films decreasing for higher oxygen contents. The crystallite size in the SnO_x thin films increases with annealing temperature justified by the annealing coalescence of small grain boundary diffusion resulting in major grain growth.
- Regarding the morphological properties of the films, we can observe that with the increase in oxygen content, the lamella like grain morphology showed a transition to equiaxed structure and finally to a very fine and smooth nano structure and that the r_{rms} and the grain size of the films decrease. The films have a more sharper grain structure for lower oxygen content with no well-defined boundaries. As the content of oxygen increases, the films surface become more smooth and more uniform. Increasing the annealing temperature results in roughness films with higher grain size.
- XPS measurements were performed in order to analyze the composition and the oxidation state of the elements present in the film. The film as deposited is composed of Sn^0, Sn^{2+} and Sn^{4+} and after the annealing only Sn^{2+} and Sn^{4+} are present, indicating that the mixed oxidation states is responsible for the origin of V_{Sn} and O_i and consequently for the p-type conductivity.
- The optical transmittance in the visible region of as deposited thin films is very poor and almost constant with the increase of oxygen content due to the presence of metallic tin, but after annealing at T_A=200 ℃, the optical transmittance of the thin films in the visible region increases considerably. However, for low contents of oxygen, where β-Sn phase is still present, the films still exhibit a lower transmittance because of the intensive light absorption of the metal gradient. As the content of oxygen increases, the transmittance of the films also increases and the band edges shift gradually to shorter wavelengths,

consistent with the blue-shift of the band gaps. For the annealed films, the optical bandgap for the annealed films varies from 2.6 eV to 3.3 eV as the content of oxygen increases, close to the reported band gap of tetragonal SnO (2.5-3.0 eV). The increase of E_{opt} with the increase of oxygen content can be related to the phases present at the thin films.

- Regarding the electrical properties, the p-type conduction was obtained for films annealed between 150 °C and 200 °C, for a narrow $\%O_2$ between 2.5 % and 4 %. Below $\%O_2$=2.5 %, the thin films were highly metallic due to the presence of Sn, for $\%O_2$ between 2.5% and 4 %.p-type conduction is achieved with resistivity, mobility and hole concentration, in the range of 22−76 Ω cm, 2.6−1.1 cm^2/Vs^{-1} and 1.1×1x10^{17} to 7.5x10^{16} cm^{-3}, respectively. Above 4.0 % the films shows n-type conduction.

<u>Cu-doped SnO_x</u>

- Rutherford backscattering (RBS) was used in order to characterize the chemical composition of Cu-doped SnO_x samples. From these measurements, we observe a shift of Cu edge towards lower energy that could be indicative of growth and formation of copper free tin oxide and/or some deagglomeration of Cu and metallic Sn.
- Regarding the structural and morphological properties, the as deposited films are composed of metallic β-Sn and as the %Cu increases there is a decrease of this phase, and the appearance of CuSn alloy. The annealed films (T_A=200 ℃) have both β-Sn and α-SnO phases and as the %Cu increases β-Sn decreases giving rise to Cu_6Sn_5 phase. The incorporation of Cu into SnO_x is quite visible from the SEM images of the annealed films where grains of different sizes can be seen that could correspond to a mixture of phases..
- Similarly as in the case of undoped films, the optical transmittance of as deposited thin films is very poor with a very low mean transmittance in the visible region; attributed to the presence non oxidized tin. After annealing at T_A=200 ℃, the optical transmittance of the thin films in the visible region increases considerably. As the %Cu increases, the E_{opt} slightly decreases due to the Cu oxide nature, which has a lower E_{op} than SnO_x films.
- P-type conductivity of Cu-doped SnO_x films is achieved for a %Cu between 4.0% and 7.0% after annealing at T_A=200℃. As the content of Cu increases, the mobility in enhanced to 1.91 cm^2/Vs , the resistivity of the p-type SnO_x film drops from 75.7 to 9.35 Ωcm^{-1} and the carrier concentration increases from 7.5x10^{16} to 3.5x10^{17} cm^{-3} for %Cu=7.0 %.

In-doped SnO_2

- Regarding the electrical properties of In-doped SnO_2 films, depending on %in and $\%O_2$ both n- and p-type conductivity were obtained. For lower content of oxygen ($\%O_2$= 5 %), p-type conductivity was obtained for lower %In (15-21%). As %In increases, both resistivity and mobility decrease and the carrier concentration increases with resistivity between 52.6 and 0.35 Ωcm, mobility between 26.3 and 0.862 $cm^2V s^{-1}$and carrier concentration between $4x10^{15}$ and $2x10^{19}$ cm^{-3}, respectively. For higher doping levels, the films showed n-type conductivity. For low %In, In^{3+} plays as acceptor, which makes the films p-type and further increase of %In ratio should lead to the an excess of indium oxide phase in the films, and therefore the films became n-type. With the increase of $\%O_2$, p-type behavior is observed for the films with higher content of In. This can be explained by considering the co-existence of donors (intrinsic defects such as oxygen vacancies and tin interstitials) and acceptors (substitution of Sn by In) in the films. For higher %In and lower $\%O_2$, indium atoms were not activated to behavior as acceptors, so the films were n-type because of the intrinsic defects. The acceptor effect of In^{3+} substituting Sn^{4+} was activated for higher $\%O_2$, resulting in p-type films. For %In=26 % and $\%O_2$= 5 %, it was obtained a highly conductive p-type film, having resistivity of $5.1X10^{-3}$ Ωcm, mobility of 22.8 $cm^2V s^{-1}$ and carrier concentration of $5.4x10^{19}$ cm^{-3}.
- XPS measurements were performed in In-doped SnO_2 films with n- and p-type conductivity in order to analyze the composition and the oxidation state of the elements present in the film. No SnO phase is present for the n-type TIO film, while for the p-type TIO film, two peaks were clearly resolved (XPS Sn $3d_{3/2}$ spectra), indicating the presence of Sn^{2+} (486.6 eV) and Sn^{4+}(487.3 eV), which similarly as in the case of p-type SnO_x film, the mixed oxidation states could be the responsible for the origin of V_{Sn} and O_i and consequently for the p-type conductivity. The VBM for the n-type TIO film is similar to what is reported for n-type SnO_2 for p-type TIO film is ~1.24 eV, the hump at 2-3 eV is less pronounced in p-type TIO than in SnO_x.
- The mean transmittance in the visible region is higher for the films deposited with a higher content of oxygen, but in general the produced films are quite transparent in this region (above 65%). Despite the content of oxygen, as the content of indium increases also the mean transmittance increase. The optical bandgap follows the same behavior, is higher for the films with higher oxygen content, which can be explained by the presence of more oxidized indium. For both $\%O_2$, as the %In increases, E_{opt} increase due to the presence of more In_2O_3, and the formation of ITO material, presenting a higher E_{opt}.

4.5. References

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Chapter 5. *Transparent p-type thin film transistors*

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5. TRANSPARENT P-TYPE THIN-FILM TRANSISTORS

5.1. TFTs with SnO_x channel

5.1.1. Process flow and device structure

P-type SnO_x based TFTs were produced using soda-lime glass substrates coated with indium tin oxide (ITO, 200 nm) and aluminum titanium oxide (ATO, 220 nm), supplied by Planar Systems, corresponding to the gate electrode and the gate insulator respectively. The SnO_x layer was deposited by rf magnetron sputtering from a 2-inch diameter Sn metallic target (provided by Plasmaterials) in a AJA ATC ORION8 system without any intentional substrate heating. Ni/Au contacts (≈6/60 nm respectively) where deposited by e-beam evaporation in a homemade system. The devices were then annealed in air, in a hot-plate at 100 °C, 150 °C and 200 °C for 1 hour (450 °C/h ramp). All necessary patterning was done by photolithography and lift-off. The masks used to the lithographic fabrication are shown on Figure 5.1.

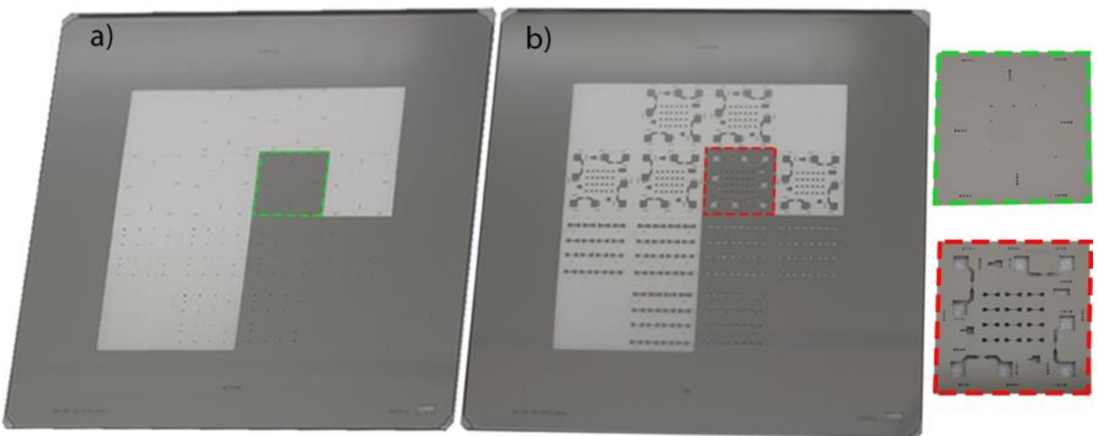

Figure 5.1. Masks used for the fabrication of bottom gate thin film transistors a) channel and b) source and drain patterning.

Electrical characterization of TFTs was performed at room temperature with an Agilent 4155C semiconductor parameter analyzer and a Cascade M150 microprobe station. Devices characterized had a width to length ratio of 50 to 50 µm. Figure 5.2 shows a schematic of the process used to produce the TFTs.

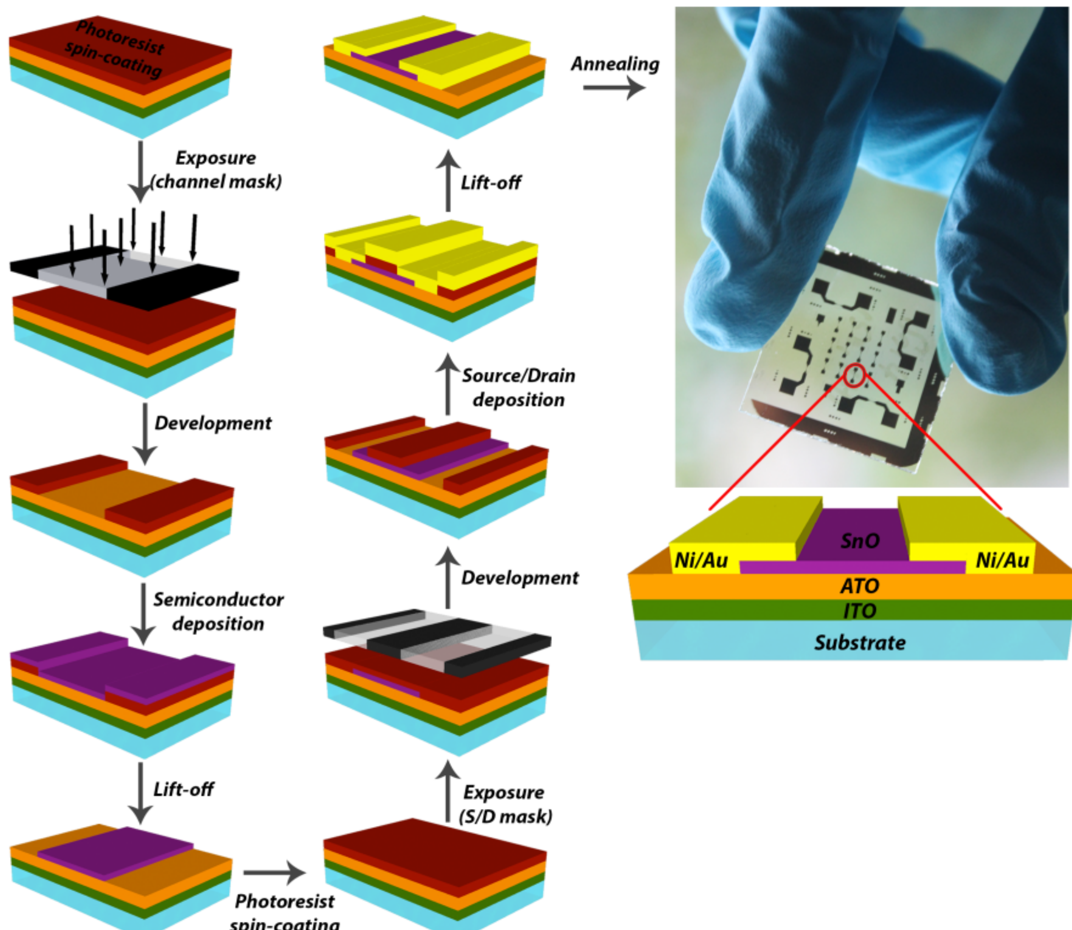

Figure 5.2. Process flow used to produce TFTs based on SnO_x and schematic of the bottom gate device structure.

5.1.2. Influence of the deposition and post-deposition parameters on the electrical properties of TFTs

As explained in Chapter 4, the processing and the post-annealing parameters play an important role in order to obtain p-type oxide semiconductors. In this section the influence of these parameters, such as oxygen content, deposition pressure, channel layer thickness and annealing temperature and the influence of the dielectric layer is showed on the electrical properties of SnO_x based TFTs.

5.1.2.1 Percentage of oxygen in the Ar+O$_2$ mixture (*%O$_2$*)

As seen on Chapter 4, the content of oxygen is crucial to obtain the best characteristics of p-type SnO_x semiconductor and consequently has a great influence on the electrical properties of the TFTs.

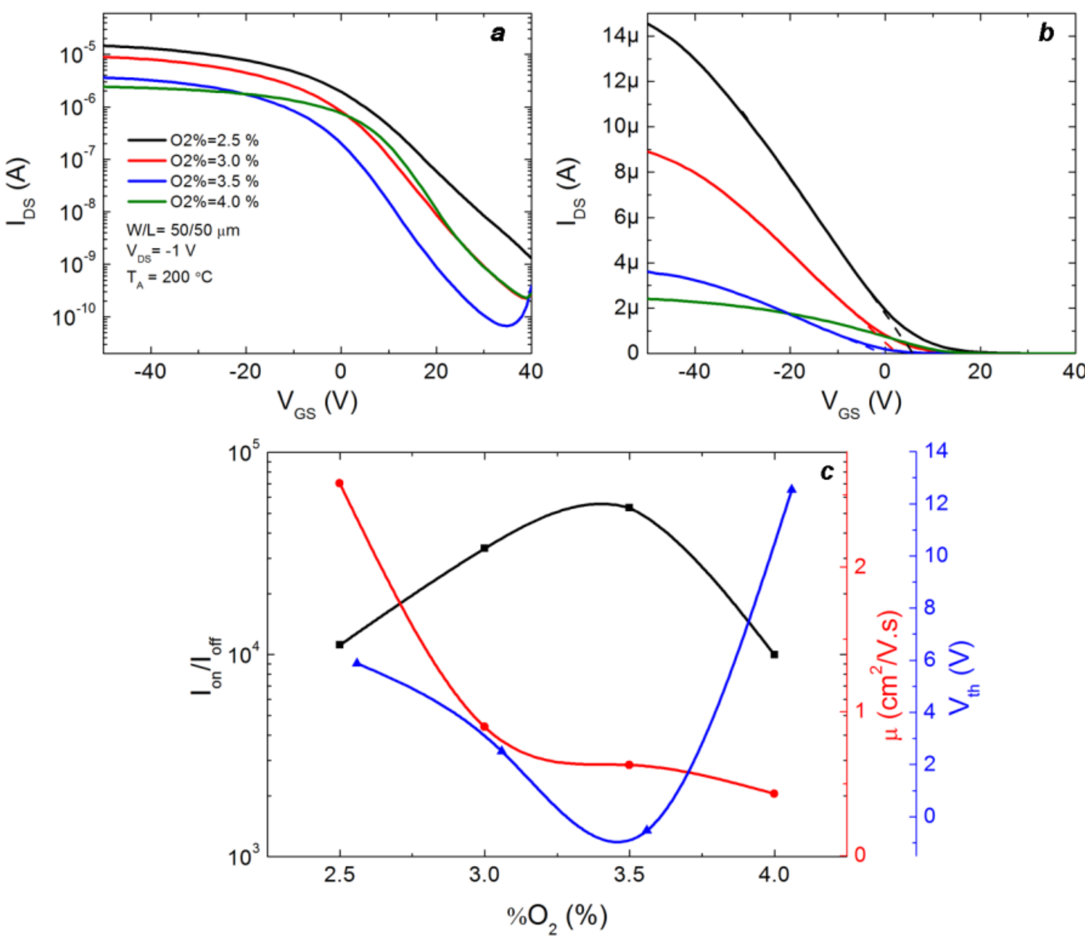

Figure 5.3. a) transfer curves and the c) variation of the main electrical characteristics for TFTs deposited at different percentages of oxygen, a deposition pressure of 0.2 Pa and 12 nm SnO_x channel thickness, annealed at 200 °C. V_{th} was calculated from the linear extrapolation of I_{DS}-V_{GS} curves at b) at the linear regime.

From Figure 5.3 c) we can observe that, as the content of oxygen ($\%O_2$) increases from 2.5% to 3.5%, the On-Off ratio, the field effect mobility and the threshold voltage decrease. We one can also observe that is possible to achieve the turn Off state of the device that could be explained due to the lower N of the semiconductor channel [1], [2]. The higher values of V_{th} for lower $\%O_2$ are related with the higher concentration of holes (N) within the semiconductor and defects at the semiconductor/dielectric interface (see Table 5.1.). For higher N, additional gate voltage is necessary in order to deplete the holes from the bulk portion of the channel. The field effect mobility increases with the decrease of the oxygen content, being in agreement with the electrical results obtained from the Hall effect (Chapter 4), where the mobility and the carrier concentrations are higher for lower $\%O_2$. This phenomenon can be explained by the structural and morphological properties of the SnO_x thin films.

The grain size and RMS roughness increase with decreasing of oxygen content. The large grain size leads to a lower grain boundary density leading to a small grain boundary scattering and thus increasing the mobility [3], [4]. We can observe that for a content of oxygen of 4.0 % V_{th} and I_{off} tends to increase again. This could be due the increase of SnO_2 phase, leading to a higher disorder and an increase of defects within the semiconductor and consequently an increase of V_{th}.

From the output curves showed at Figure 5.4 we can conclude that the devices shows a clear linear and saturation regions of the output characteristics and do not present significant current crowding for low V_{DS}, indicating low series resistance in source-drain contacts with SnO_x channel layer. As the content of O_2 decreases, the drain current increases showing the more metallic behavior of the semiconductor, but still the saturation region is well clear and defined.

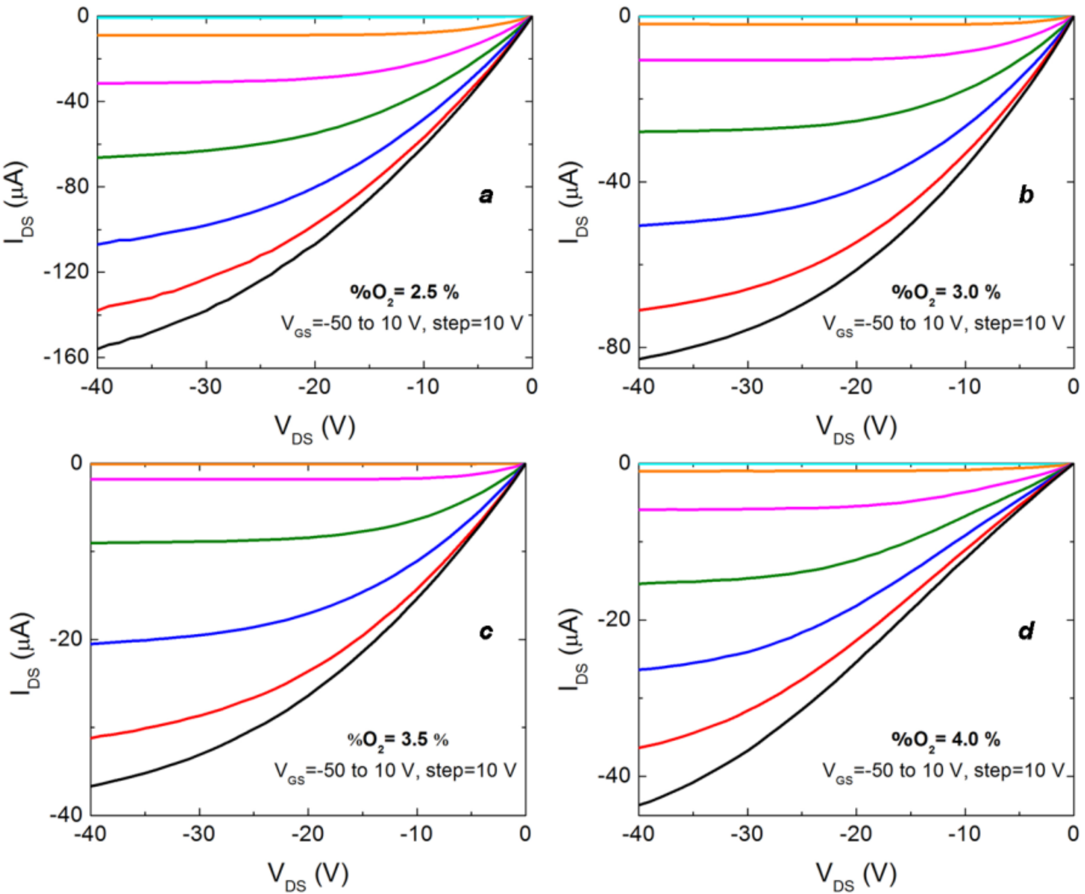

Figure 5.4. Output curves for the TFTs deposited at different percentages of oxygen, a deposition pressure of 0.2 Pa and 12 nm SnO_x channel thickness, annealed at 200 °C.

Table 5.1. Electrical properties of the devices depicted in Figure 5.3 a).

$\%O_2$ (%)	On-Off ratio	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	S ($V dec^{-1}$)	D_{it} (cm^{-2})
2.5	1.11×10^4	2.58	5.88	9.62	6.41×10^{13}
3.0	3.35×10^4	0.89	2.51	8.75	5.84×10^{13}
3.5	5.32×10^4	0.63	-0.54	7.75	5.16×10^{13}
4.0	9.96×10^3	0.43	12.53	5.71	3.80×10^{13}

The electrical measurements were also performed in double sweep mode to access the hysteresis magnitude obtained with the content of oxygen. At Figure 5.5 we observe the increase of hysteresis with the increase of oxygen meaning that more trapping effects occur. We can also conclude that the charge trapping effect occurs at or close to the dielectric/semiconductor interface since the hysteresis direction is always clockwise [5].

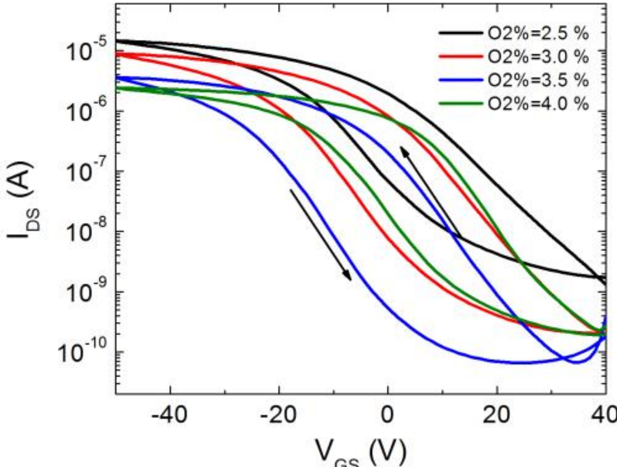

Figure 5.5. Transfer curves measured in double sweep to access the hysteresis magnitude for the TFTs deposited at different percentages of oxygen, a deposition pressure of 0.2 Pa and 12 nm SnO_x channel thickness, annealed at 200 °C.

5.1.2.2 Deposition pressure (p_d)

As previously observed on Chapter 4 the increase on the chamber pressure produces more crystal defects, leading to a decrease on the crystalline quality of the thin films [6]. The decrease at the crystallinity and consequently at the grain size of the films leads to a lower mobility as previous explained. This is also observed on the TFTs characteristics (Figure 5.6 c). As the deposition pressure increases from 0.2 Pa to 0.33 Pa, the field effect mobility decreases from 2.16 $cm^2 V^{-1} s^{-1}$ to 0.99 $cm^2 V^{-1} s^{-1}$. The threshold voltage and the off current increase with the

increase of deposition pressure. This result seems to be contradictory with the electrical results obtained, since the carrier concentration decreases with the increase of the deposition pressure. The increase of the threshold voltage could be due a higher density of interface states which can justify the decrease of mobility. V_{th} depends on the work function difference between the gate electrode and the semiconductor, the fixed charges within the dielectrics and the charges and trap density in the interface states at the semiconductor/dielectric interface and within the semiconductor [7]–[9]. In this study, and since the only variable is the semiconductor channel properties, the change on V_{th} must be due the interface states, leading to the conclusion that a higher deposition pressure and consequently more re-sputtered species results on a higher density of interface states. Their effect is to reduce the slope of the linear region of the characteristic transfer curves (I_{DS} V_{GS}) and the analysis of those curves using Eq. 2.14 will show an apparent reduction in carrier mobility, since in this equation it is assumed that all charge induced by the gate voltage is due to free charge in the channel. In the presence of interface states, the induced charge is partitioned between the free carriers in the channel and carriers trapped up to the Fermi level in the interface states [8].

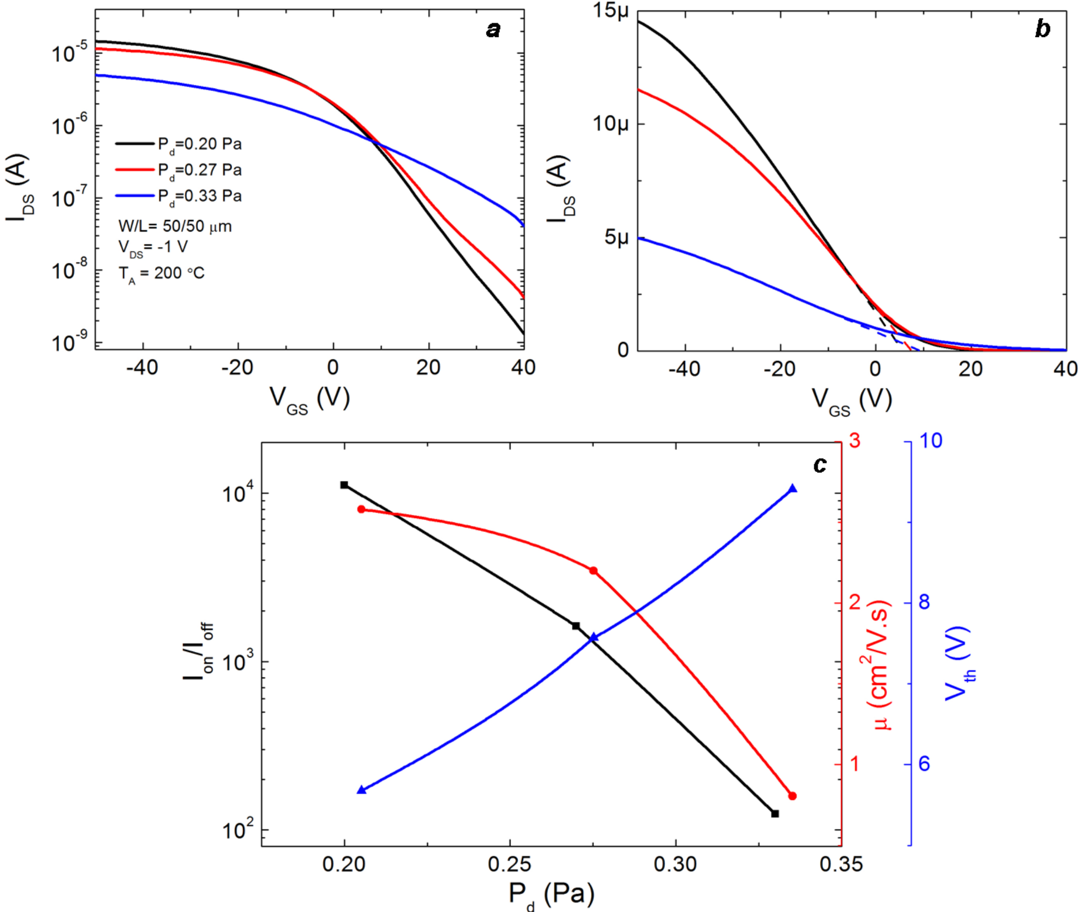

Figure 5.6. a) Transfer curves and the c) variation of the main electrical characteristics for TFTs deposited at different deposition pressures, %O_2= 2.5 % and d_s= 12 nm, annealed at 200 °C.

Similar to what was observed for the influence of oxygen content, the devices shows clear linear and saturation regions of the output characteristics and do not present significant current crowding for low V_{DS}, indicating low series resistance in source-drain contacts with SnO_x (Figure 5.7). For higher deposition pressures, the drain current is lower as a result of the lower conductivity of the channel.

Table 5.2. Electrical properties of the devices depicted in Table 5.7 a).

P_d (Pa)	On-Off ratio	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	S (V dec^{-1})	D_{it}
0.20	$1.11x10^4$	2.58	5.88	9.62	$6.41x10^{13}$
0.27	$1.62x10^3$	2.20	7.57	13.33	$8.91x10^{13}$
0.30	$1.24x10^2$	0.81	9.41	25.0	$1.67x10^{14}$

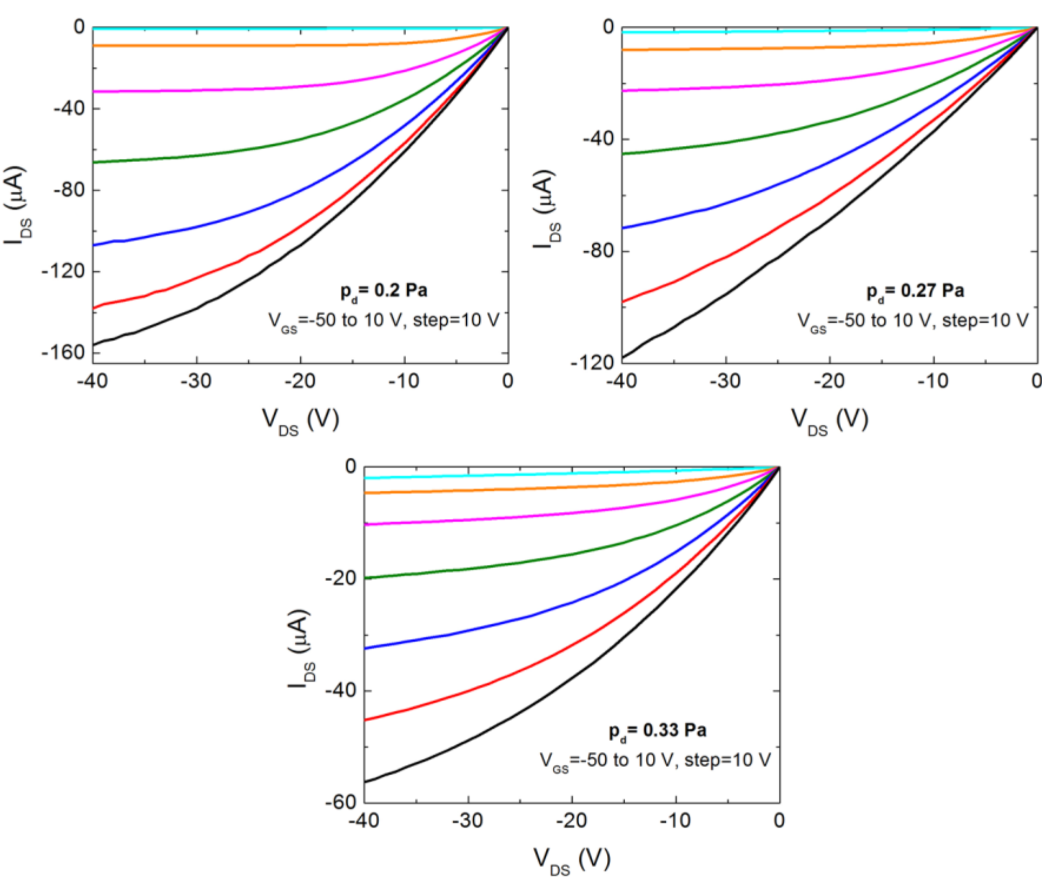

Figure 5.7. Output curves for the TFTs deposited at different depositions pressures, %O2=2.5 % and 12 nm SnOx channel thickness, annealed at 200 °C.

5.1.2.3 Annealing temperature (T_A)

From Figure 5.8 we can observe that for higher annealing temperature, the filed effect mobility and the threshold voltage decrease. With the increase of temperature a phase transformation from SnO_x to SnO_2 occurs, leading to the formation of p-n junctions depleted of electrical carriers at the interfaces between the SnO_2 crystallites and the SnO_x matrix [10]. With the formation of these p-n junctions both the concentration and the mobility of electrical carriers in the film will be reduced. This reduction of carrier concentration results in a decrease on the threshold voltage and on the off current. The formation of these p-n junctions, subsequently leads to the decrease of the conductivity with the increase of temperature, resulting in a lower off current.

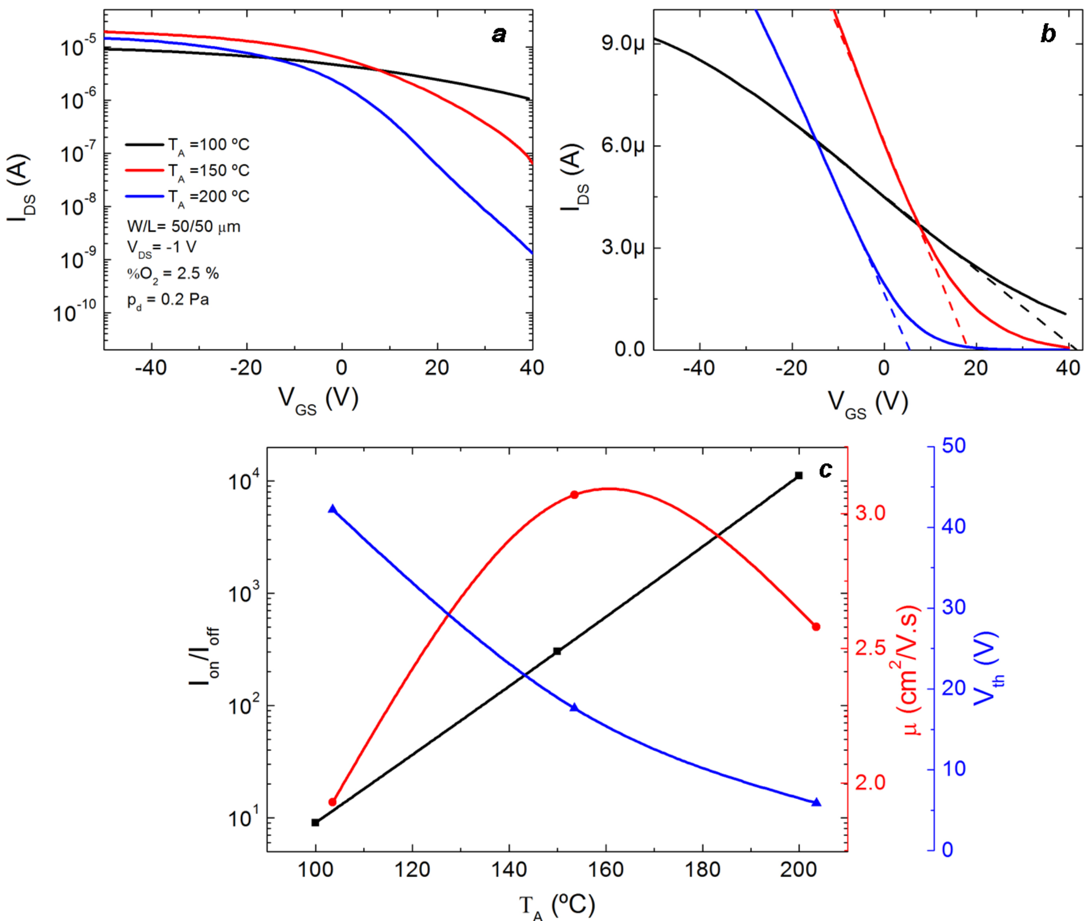

Figure 5.8. a) transfer curves and the b) variation of the main electrical characteristics for TFTs deposited at $\%O_2$= 2.5 %, p_d= 0.2 Pa and d_s= 12 nm, annealed at 100, 150 and 200 °C.

From the output curves of Figure 5.9 we can observe that for T_A= 100 °C, the drain current has a linear behavior with the drain voltage and the device does not achieve the saturation regime. This is attributed to high Sn metallic phase still present at the channel semiconductor for low annealing temperature. As the temperature increases, the devices shows clear linear and saturation regions

not presenting current crowding for low V_{DS}, indicating low series resistance in source-drain contacts with SnO_x.

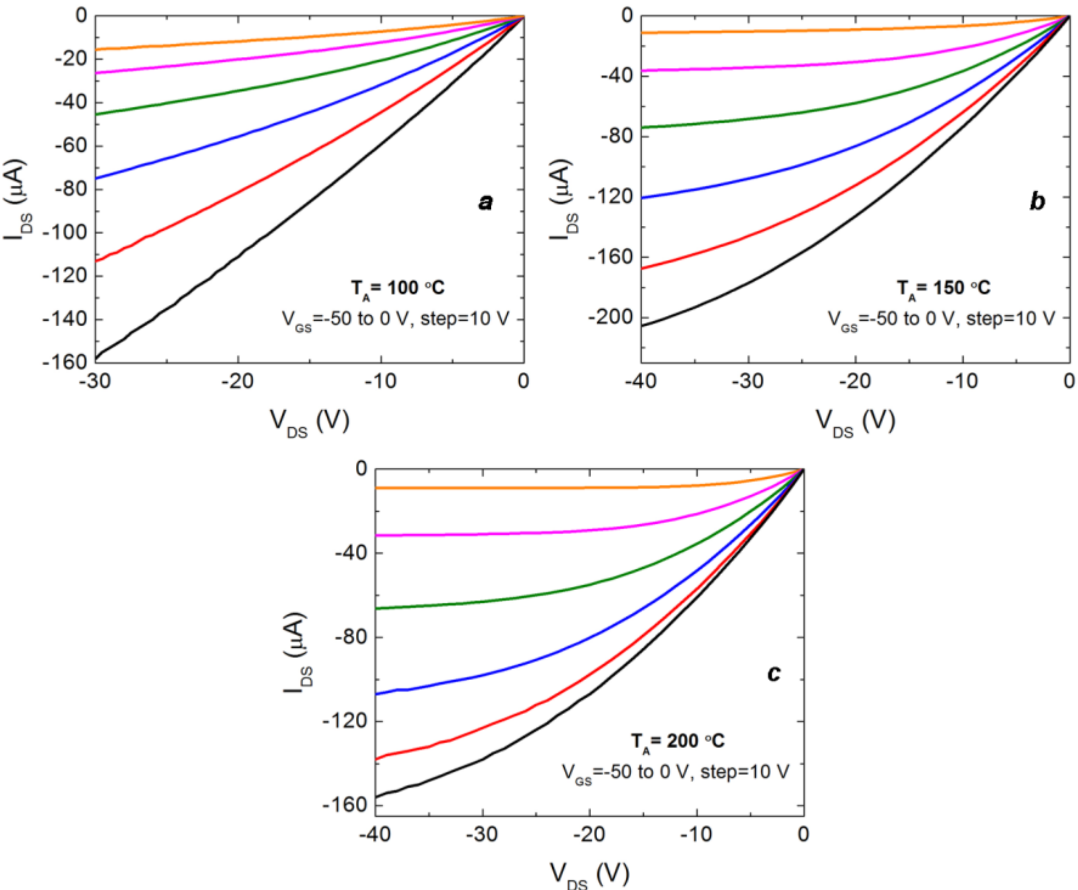

Figure 5.9. Output curves for the TFTs deposited at $\%O_2$= 2.5%, p_d=0.2 Pa, t_s=12 nm annealead at a)100 °C, b) 150 °C and c) 200 °C.

5.1.2.4 Influence of SnO_x channel thickness on the electrical performance of TFTs

For the study of the thickness (d_s) influence on the device performance, SnO_x TFTs with four different channel layer thicknesses were fabricated with W/L= 50/50 μm using $\%O_2$= 3.5 %, p_d=0.2 Pa and annealed in air at 200 ºC during 1 hour.

It can be seen from the plots in Figure 5.10, that with the increase in the thickness of the SnO_x film, the field-effect mobility increases, the threshold voltage is shifted from negative to positive values, the off drain current is increased and that is not possible to achieve the turn Off state of the device [1]. In Figure 5.11 (a)-(d) is presented their output characteristics and in Table 5.3 is summarized the device performance of SnO_x TFTs with different channel layer.

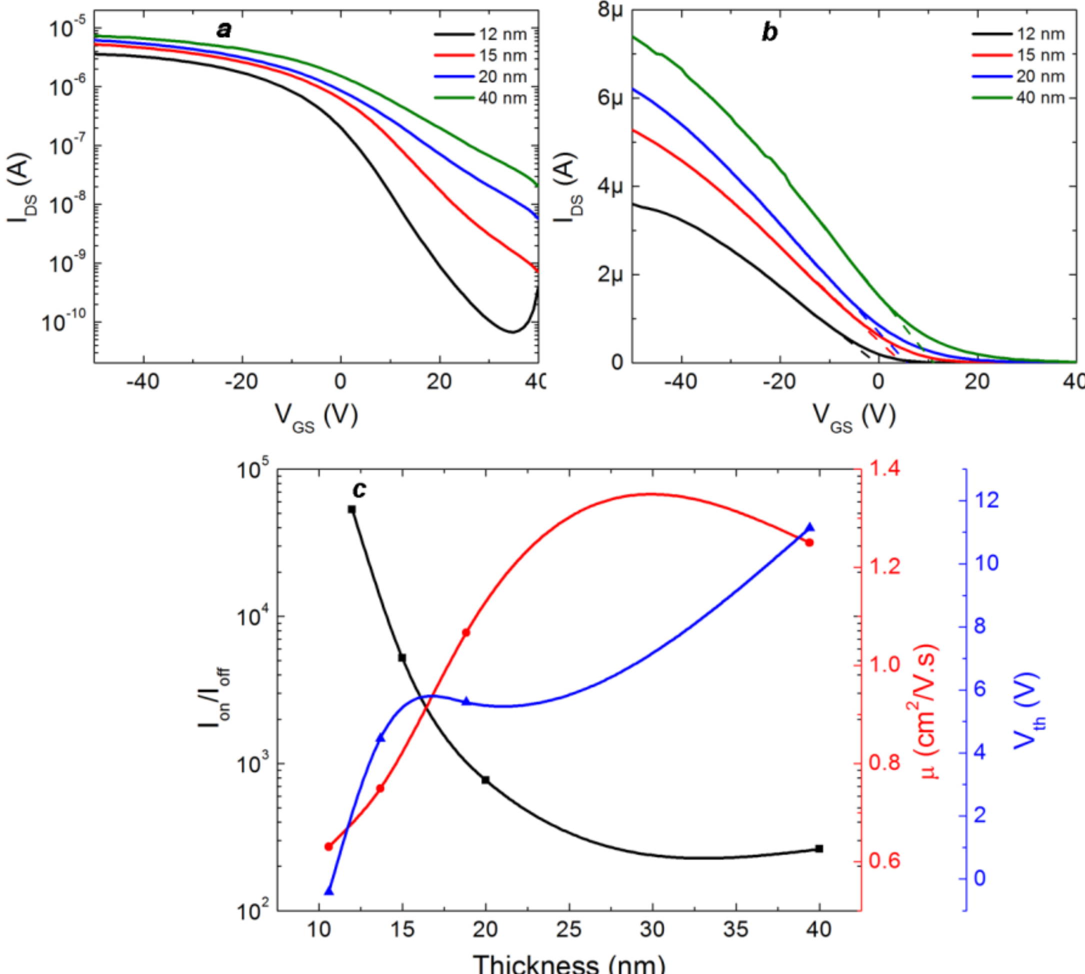

Figure 5.10. Transfer characteristics curves a) semi log and b) liner scale for the TFTs deposited with %O_2= 3.5 %, p_d= 0.2 Pa with different SnO_x channel layer thicknesses, annealed at 200 °C.

With the increase of thickness, the operation mode changes from enhancement (negative V_{th}) to depletion mode (positive V_{th}) suggesting that the active layer is not fully depleted for higher d_s. This could be explained by the higher numbers of free charges present in the bulk of the thicker active layer which require a higher gate voltage, V_{GS}, to deplete the semiconductor channel. [11] Thus, for thicknesses lower that 15 nm, V_{th} is negative meaning that the TFT is completely depleted under zero gate bias. When the d_s increases, the threshold voltage is positive because the TFT is partially depleted under zero gate bias.

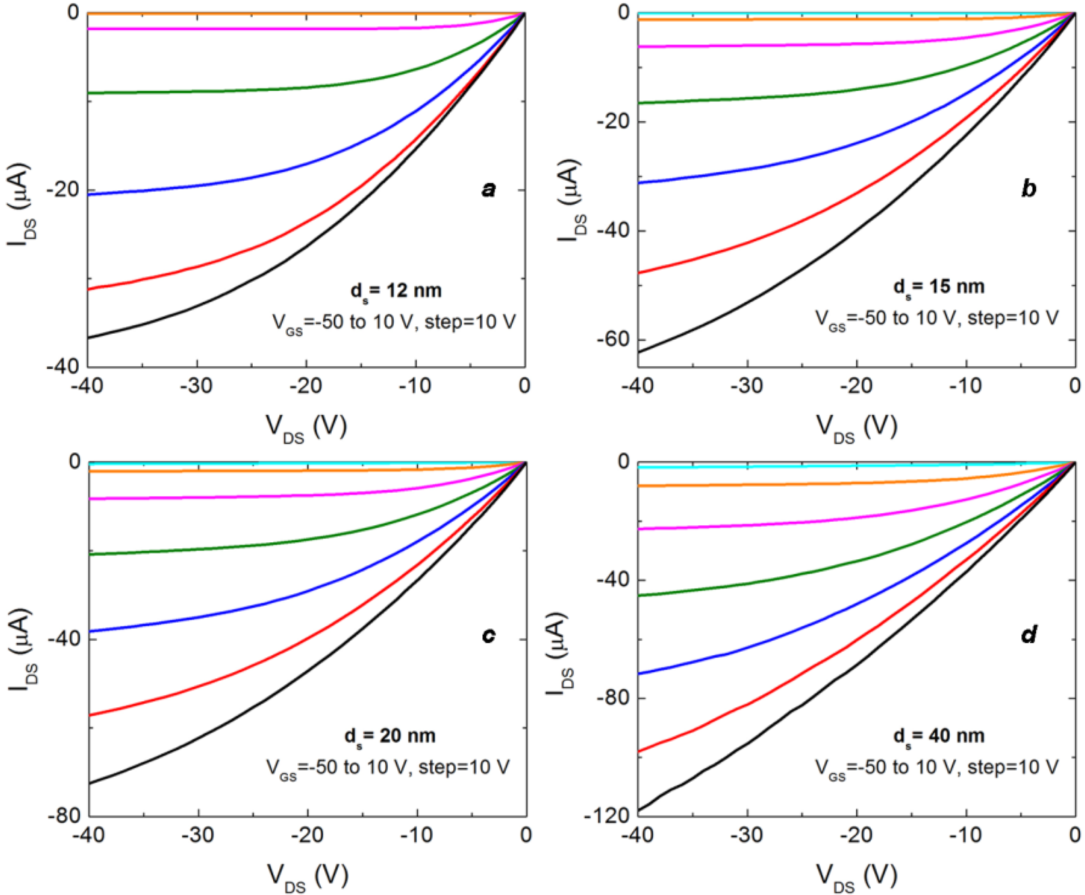

Figure 5.11. Output curves for the TFTs deposited with %O_2= 3.5 %, p_d= 0.2 Pa with a $SnOx_x$ channel layer thickness of a) 12nm, b) 15 nm, c) 20 nm and d) 40 nm, annealed at 200 °C.

A considerable decrease of μ_{FE} is observed as the d_s decreases. This is due to the fact that d_s becomes comparable to the surface roughness and the morphological defects create discontinuities in the film, leading to a decrease in the mean free path of holes within the channel, and consequently decreasing μ_{FE}. This does not necessary mean that the interface trap density increases, since the subthreshold voltage decreases with the decrease in thickness. This decrease can be justified by the fact that as the film get thicker, it can take more time to accumulate the charge ate the semiconductor/dielectric interface [1], [12]. We can also observe from Table 5.3 the deterioration of S (increase) with the increasing of d_s. This deterioration can be due a combination of effects (depicted in Figure 5.12) due to the increase thickness [13]:

- *Increase of I_{off} current*
- *Movement of the charge centroid of the induced accumulation layer away from the insulator-semiconductor*
- *Increase in the sheet trap density, Nt*

The first mechanism of *S* degradation, as identified in Fig. 4.18, is an increase in the off current (I_{off}) with increasing of d_s. Neglecting the effect of band bending at the back surface of the semiconductor, I_{off} is approximated as

$$I_{off} \sim \frac{\sigma_D d_s W V_{DS}}{L} \quad \textbf{(5.1)}$$

where σ_D is the dark conductivity of the semiconductor layer, d_s is the thickness of the semiconductor, V_{DS} is the drain to source voltage, and W and L are the width and length of the semiconductor channel, respectively .

An increase in I_{off} obscures the effect of gate-induced current since a larger fraction of the total drain current arises from I_{off}, since the total drain current is the sum of the off current and gate-induced current. A modified subthreshold swing equation including I_{off} is given as

$$S = \frac{V_{GS2} - V_{GS1}}{log10(I_{off} + I_D(V_{GS2}) - log10(I_{off} + I_D(V_{GS1})} \quad \textbf{(5.2)}$$

Using this relation, we obtain a subthreshold voltage swing of 12.1 $Vdec^{-1}$ and 22.8 $Vdec^{-1}$ for the TFTs with channel semiconductor thicknesses of 15 and 40 nm, respectively. In this way, we can conclude that for higher values of I_{off}, the S increases.

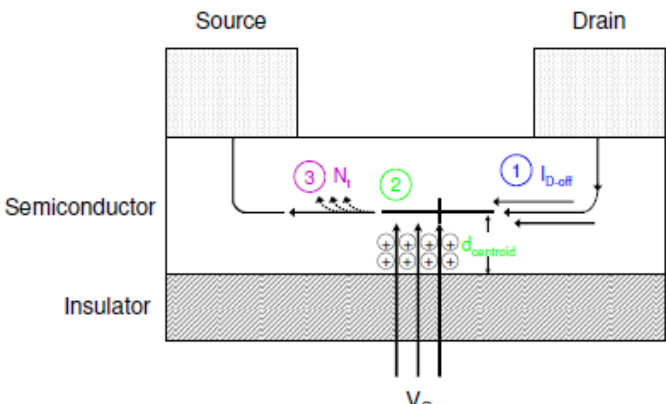

Figure 5.12. Possible mechanisms for degradation of the subthreshold swing, *S*, with increasing semiconductor thickness: (1) an increase in I_{off}, (2) movement of $d_{centroid}$ away from the insulator-semiconductor interface and (3) increase in the sheet trap density, *Nt*. Adapted from [13]

With the increase of d_s, the distance between the charge centroid and the semiconductor/dielectric interface increases, inserting a semiconductor capacitance in series with the gate insulator capacitance, reducing the effective capacitance and leading to an increase in subthreshold swing (represented with 2 in Figure 5.12).

Finally, considering that the channel layer trap density, n_t, is constant across the film, the sheet trap density, N_t, increases with the increase of thickness. This results in more traps that induce more free carriers, resulting in the subthreshold swing degradation in the TFTs.

Table 5.3. Electrical properties of the devices produced with different semiconductor channel layer thicknesses.

Thickness (nm)	On-Off ratio	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	V_{th} (V)	S ($V\ dec^{-1}$)	D_{it} (cm^{-2})
12	5.32×10^4	0.63	-0.54	7.75	5.16×10^{13}
15	5.21×10^3	0.75	4.46	12.35	8.25×10^{13}
20	7.71×10^2	1.07	5.60	17.38	1.16×10^{14}
40	2.58×10^2	1.25	9.37	17.24	1.15×10^{14}

We observe, from the transfer characteristics curves performed in double sweep (Figure 5.13), that the hysteresis reduces as d_s increases. For a thinner semiconductor layer, the conduction is confined near the insulator-semiconductor interface, where interface states and/or a higher concentration of defects are expected.

As the thickness increases, the influence of the interface region is reduced while the influence of the “bulk” region increases, leading to a decrease in hysteresis in thicker films. Also, the thinner the semiconductor layer is, more discontinuities and inhomogeneous it can be result of the nucleation and island formation mechanism associated with the growth of a thin film, leading to increased hysteresis for thinner films[13].

Once again, the hysteresis direction is clockwise, meaning that the charge trapping effect occurs at or close to the dielectric/semiconductor interface.

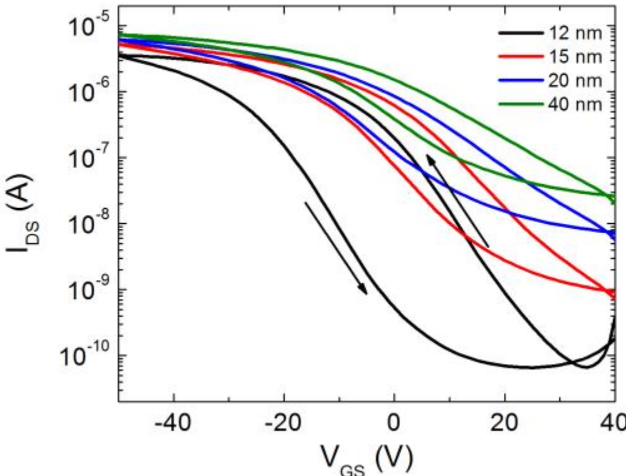

Figure 5.13. Transfer curves measured in double sweep to access the hysteresis magnitude for the TFTs deposited with different semiconductor channel thicknesses, a deposition pressure of 0.2 Pa and 12 nm SnOx channel thickness, annealed at 200 °C.

5.1.3. Influence of gate dielectric on the electrical properties of TFTs

The interface between the semiconductor and the dielectric in a thin film transistor plays a crucial role in the electrical performance of the device. It is known that the free carriers flow through the channel in the first nanometers of the channel (front surface), specifically at the interface between the semiconductor and the dielectric layer. The dielectric properties determine the charge accumulation at the dielectric/semiconductor interface and the existence of defects at this interface as well as within the dielectric, strongly influence the TFT main characteristics, such as field effect mobility, leakage current and operating voltage [14], [15].

Complementary-Metal-Oxide-Semiconductor (CMOS) has been the most widely used technology for decades, being the successful Si/SiO_2 combination the main responsible for the extraordinary performance exhibited by MOSFETs [15]. However, the demand for higher performance and lower manufacturing costs leads to the scaling of the thin film transistors with channel dimensions below 45 nm which implies that the thickness of the SiO_2 dielectric layer should be lower than 1 nm [16] due to the low-k of SiO_2 . This is a critical issue causing the increase of gate leakage current due to quantum tunneling effects [17].

The way to solve this issue is to use materials with a higher permittivity, called high-k dielectrics, so the thickness of the films can be increased and the capacitance per unit area can be maintained. For these reasons, the gate dielectric has receiving great attention, especially multicomponent high-κ dielectrics and its application mainly in n-type TFTs and in organic n and p type TFTs [14], [18]–[21]. The most promising high-k materials, due to their larger dielectric constant, incorporate hafnium, titanium, tantalum, strontium, aluminum and its oxides [22]–[27].

The dielectrics must satisfy some criteria in order to be used in transparent TFTs: high bang gap (E_G), preferentially higher than the semiconductor and, favorable conduction band offset, to avoid high gate leakage and also a good interface that is mostly achieved using amorphous dielectrics [28]. As can be seen in Figure 5.14a, E_G is inversely proportional to κ, meaning that the required high-k materials should have low bandgap. This issue is a disadvantage for these materials, since for low bandgap materials, the gate leakage is higher due to excitation of electrons or holes by Schottky emission into the dielectric conduction or valence bands, or due to other defect-assisted transport mechanisms, such as Poole-Frenkel effect or hopping conduction [29], [30]. Figure 5.14b shows the calculated band offsets of oxide dielectrics on silicon. In order to achieve good reliability, the offsets of the dielectric's VBM, in case of p-type transistor, and CBM, for a n-type transistor, should be at least 1 eV relatively to the ones of the semiconductor [7].

A very important aspect is the structure of the dielectric to assure an interface with a high electrical quality, low interface state density and absence of interface defects. A bad interface leads to high fixed charge density reducing the performance of the thin film transistor. In order to improve the interface quality, amorphous oxide dielectrics should be used.

The amorphous oxides present some advantages over the crystalline ones such as the lower number of interface defects, the isotropy of the dielectric constant, such that fluctuations in polarization from differently oriented oxide grains will not cause scattering of carriers.

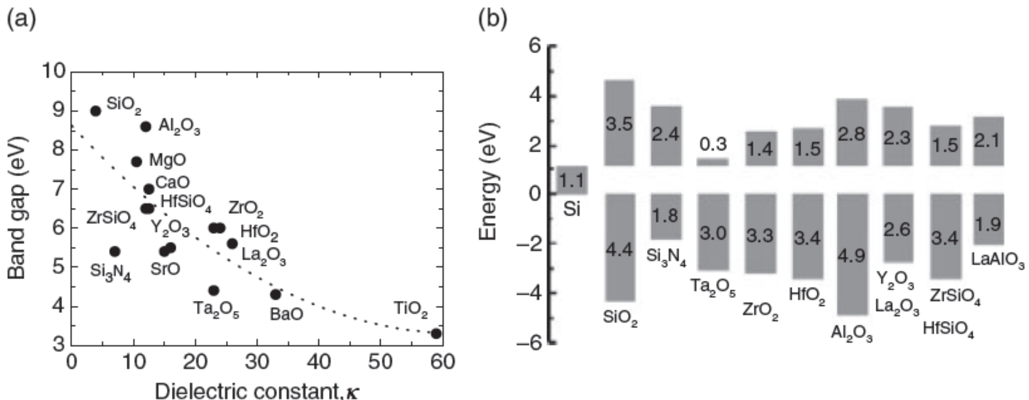

Figure 5.14. (a) Relation between E_G and κ for for some dielectrics; (b) calculated band offsets of oxide dielectrics on silicon.[15]

Several techniques have been used to produce high-κ dielectrics, such as sputtering [26], [31], [32], sol-gel process [33], [34], ion-assisted e-beam evaporation [35], [36], Atomic Layer Deposition (ALD) [37]–[41], pulsed laser deposition (PLD) [42]–[44] and metal-organic chemical vapor deposition (MOCVD) [45]–[47].

ALD is considered one of the most promising solution for the growth of ultra-thin and conformal films such as oxides, nitride and metal films [7] since this process deposits one atomic layer in each cycle, allowing the control of film growth at the nanometer scale leading to a conformal coating even in high aspect ratio and complex structures.

Nowadays, ALD is already and successfully employed for the growth of thin films in several industrial applications such as high-k gate oxides, storage capacitor dielectrics, adhesion layers, organic semiconductors, nanoporous structures coating, Bio Mems, electroluminescent displays [37], [48]–[51].

In order to understand the influence of the dielectric in p-type TFTs, several SnO_x based TFTs were produced in a bottom gate configuration using different dielectrics produced in collaboration with Beneq, Inc., in Finland. SnOx films were grown by reactive r.f magnetron sputtering using an AJA, Model ATC ORION8 system without intentional heating, as described at (5.1.1). The deposition pressure (p_d) was kept constant at 0.20 Pa, the r.f power (P_{rf}) at 40 W, the oxygen content ($\%O_2$) of 3.0% and 12 nm thickness (d_s). The multicomponent dielectrics were produced by Atomic Layer Deposition technique using a P400A model, from Beneq. The dielectric used during this thesis work, AlTiO (ATO), deposited by Atomic Layer Deposition (ALD) has been widely used as a gate dielectric in oxide TFTs [52]–[54], consisting of alternate layers of aluminum oxide (Al_2O_3) and titanium oxide (TiO_2) and its successful application in p-type oxide TFTs was already demonstrated [55], [56].

Thus, the first approach used in this study was to produce dielectrics films (see Table 5.4) based on AlTiO. Process 1, consists of a multicomponent layer of AlTiO plus 250Å of Al_2O_3 on the top. In order to understand the influence of the Al_2O_3 top layer on the dielectric/semiconductor interface, at process 2 we deposited an extra layer of this material (process 2) at the top of ATO and at process 3, a layer of HfO_2, was deposited instead of Al_2O_3.

The second approach was to substitute the multicomponent layer AlTiO, with a multicomponent dielectric consisting on Al_2O_3 and HfO_2 ($HfAlO_x$). At process 4 it was deposited only a multicomponent layer of $HfAlO_x$ and at processes 5 and 6, an Al_2O_3 layer was added at the top of the multicomponent layer and also the quantity of Al_2O_3 at the multicomponent layer was different.

Table 5.4. Multilayer dielectrics produced by ALD

	Dielectric Process			
1 Al_2O_3 AlTiO Al_2O_3	Al_2O_3(250Å)	17x[Al_2O_3(50 Å) + TiO_2(50 Å)]	Al_2O_3(250Å)	
2 Al_2O_3 Al_2O_3 AlTiO Al_2O_3	Al_2O_3(250Å)	17x[Al_2O_3(50 Å) + TiO_2(50 Å)]	Al_2O_3(250Å)	Al_2O_3(250 Å)
3 HfO_2 Al_2O_3 AlTiO Al_2O_3	Al_2O_3(250Å)	17x[Al_2O_3(50 Å) + TiO_2(50 Å)]	Al_2O_3(250Å)	HfO_2(50 Å)
4 Al_2O_3 + HfO_2 Al_2O_3	Al_2O_3(200 Å)	13x[Al_2O_3(50 Å) + HfO_2(50 Å)]		
5 Al_2O_3 Al_2O_3 + HfO_2 Al_2O_3	Al_2O_3(200 Å)	14x[Al_2O_3(25 Å) + HfO_2(50 Å)]	Al_2O_3(250 Å)	
6 Al_2O_3 Al_2O_3 + HfO_2 Al_2O_3	Al_2O_3(200 Å)	11x[Al_2O_3 (50 Å) + HfO_2(50 Å)]	Al_2O_3(250 Å)	

All the dielectrics were deposited on top of with Indium Tin Oxide, ITO, (used as gate electrode at the TFT) in order to continue the production of bottom gate TFTs, where the active layer is a 12 nm SnO_x thin film p-type semiconductor, as previously explained and for the source-drain electrodes, double layer Ni/Au (8/50 nm thick) were e-beam evaporated using a home-made evaporation system. Both the semiconductor and the source-drain electrodes were patterned by lift-off, being obtained TFTs with a width-to-length ratio (W/L) of 50/50 μm.

The final devices were annealed at 200 °C for 1 hour in air using a using a hot-plate with controllable heating ramp. The electrical characterization was performed with a relative humidity of 35-40%, with an Agilent 4155C semiconductor parameter analyzer and a Cascade Microtech M150 microprobe station.

All the electric measurements were done inside a dark box and at ambient atmosphere. The capacitance of each dielectric was obtained from Capacitance-Voltage measurements at 100 kHz on Metal/Insulator/Metal (MIM). The structure and morphological properties of the dielectrics, investigated by XRD, AFM and SEM, are shown in Figures 5.15 and 5.16 and at Table 5.5 is shown the distinct capacitance, dielectric constant and roughness for the dielectrics produced.

At the processes based on ATO we one can observe some differences due to the top layer. For the dielectrics layers produced in processes 1 and 2 we can observe grains coalescence that could probably be the responsible for the high roughness of these films. The process 3, in which the top layer is HfO_2 has a more pronounced structure that could be justified by the crystalline nature of HfO_2 at lower temperatures. Nevertheless, it has a smooth surface when comparing to processes 1 and 2. The processes based on HfO_2 shows very similar smooth morphology and the roughness is drastically reduced (until a maximum of 32%) when compared with the other processes produced in this work.

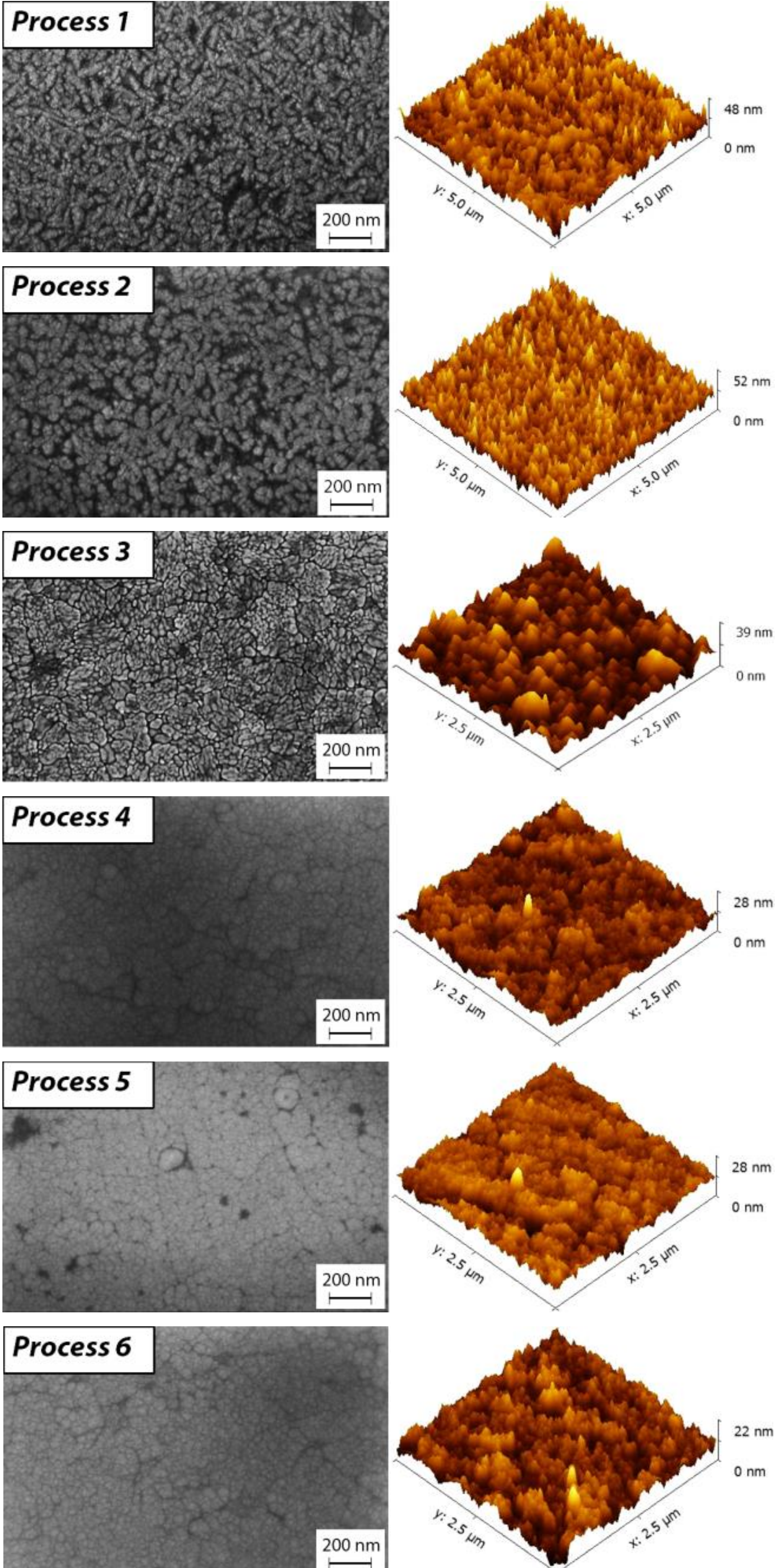

Figure 5.15. SEM and AFM images of the dielectrics produced.

In Figure 5.16 is shown the XRD diffractograms of the different dielectrics layers. All the peaks correspond to the ITO layer, meaning that the dielectrics layers are amorphous, which is an advantage over the crystalline dielectrics in which the grain boundaries act as paths for impurity diffusion and leakage current and consequently deteriorate the dielectric properties [15].

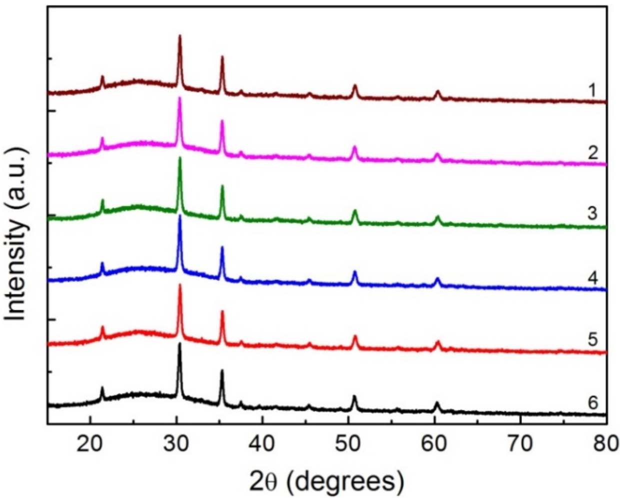

Figure 5.16. XRD diffractograms for multicomponent dielectrics produced with different materials.

As it is shown on Table 5.5, the capacitance density of the different gate dielectrics, depends not only on the multicomponent layer material, but also on the top layer. The dielectrics based on ATO show a lower capacitance density when compared with the processes using a multicomponent layer based on HfO_2. The capacitance density is reduced when adding a Al_2O_3 or HfO_2 layer. For the processes based on $HfAlO_x$ multicomponent layer, the capacitance is substantially higher. However, adding a Al_2O_3 layer at the top of the multicomponent or increasing the content of Al_2O_3 within the multicomponent layer, the capacitance decreases.

Table 5.5. Electrical and morphological properties of the produced dielectrics.

Process	Capacitance density (nF/cm^2)	k	Roughness (nm)
1	50.4	12.5	1.6
2	42.7	11.8	1.8
3	44.1	11.2	0.8
4	76.2	12.9	0.47
5	73.1	12.3	0.5
6	66.1	11.5	0.51

When applied as gate dielectric in SnOx p-type TFTs, the dielectrics characteristics strongly influences the V_{GS} range necessary to the working mode as well the on-off ratio and field effect mobility of the devices. Figure 5.17 a) shows the transfer characteristics of the devices produced using the dielectrics described at processes 1 to 6.

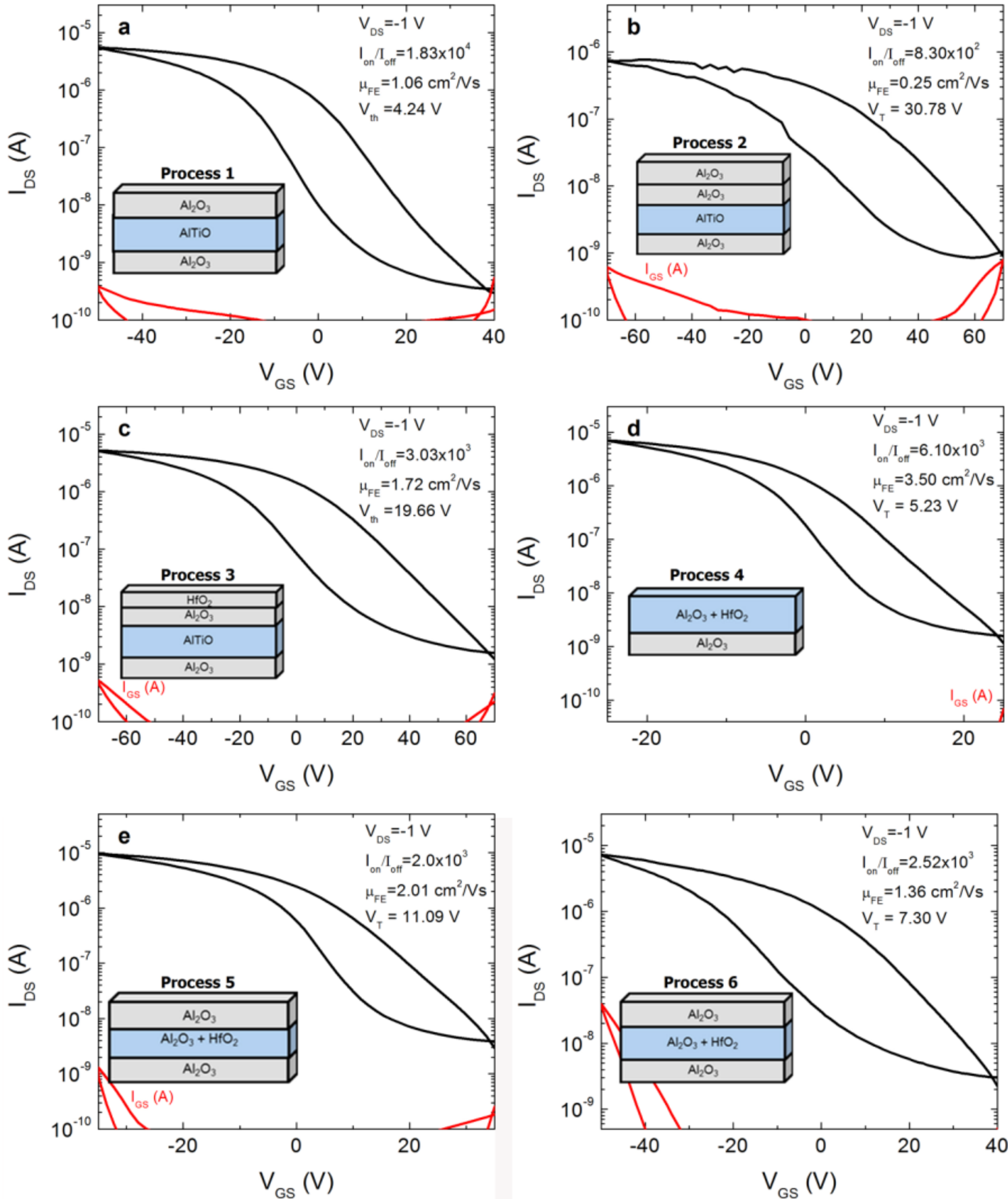

Figure 5.17. Influence of the dielectrics(a-c) based on ALTiO and (d-f) HfO_2 in the transfer characteristic of SnO_x TFTs annealed at T_A=200 °C.

When comparing to the device produced with the ATO dielectric produced at process 1, the addition of an Al_2O_3 layer at the top of ATO (process 2) results in a higher threshold voltage, lower filed effect mobility and lower On-Off ratio of the device due to the higher roughness and lower capacitance of the dielectric.

Despite the dielectric produced in process 3 has a lower roughness and similar capacitance to the one produced at process 1, we can observe an increase at the threshold voltage. This increase could be justified by a poor interface between the ATO and HfO_2 layers, leading to a higher trap density. The lower roughness of the dielectric obtained from the process 2 could be responsible for the higher On-Off ratio and field effect mobility. The TFT produced with the dielectric 4, HfO_2 based and without the addition of Al_2O_3 layer, shows better performance. The I_{GS} is lower, meaning that the interface quality was improved due to the superior bulk isolating property and also the μ_{FE} is higher due to less interface states and lower roughness of the gate dielectric. The lower threshold voltage indicates enhanced control capability of gate voltage on channel conduction reducing the power consumption [57].

Table 5.6. Electrical properties of the devices depicted in

Process	On-Off ratio	**μ_{FE} ($cm^2 V^{-1} s^{-1}$)**	**V_{th} (V)**	**S ($V dec^{-1}$)**	**D_{it} (cm^{-2})**
1	$1.83x10^4$	1.06	4.24	8.26	$5.51x10^{13}$
2	$8.3x10^2$	0.25	30.78	9.09	$6.06x10^{13}$
3	$3.0x10^3$	1.72	19.66	5.99	$3.98x10^{13}$
4	$6.1x10^3$	3.50	5.23	5.56	$3.69x10^{13}$
5	$2.0x10^3$	2.01	11.09	5.58	$3.69x10^{13}$
6	$2.52x10^3$	1.36	7.30	10.75	$3.01x10^{13}$

Since the channel semiconductor properties were kept constant, we could state that the improvement on the electrical behavior is due to the dielectric characteristics. We one could conclude that the gate dielectric strongly influences the TFTs performance mainly due to the electrical and morphological properties of the material. The interface quality can be improved, decreasing the interface states and also the V_{GS} range necessary for the TFT to works is lower.

5.1.3.1 SnO_x ambipolar TFTs

Figure 5.18 shows the transfer characteristics of the devices produced with the dielectrics form processes 1 and 5 annealed at 150 °C, 200 °C and 250 °C. From the transfer curves obtained for the TFTs annealed at 250 °C, we can observe that the device produced with ATO has a typical characteristic transfer curve of a n-type device, while the one produced with $HfAlO_x$ shows an ambipolar behavior, transporting both holes and electrons in one device. A clear inversion characteristic is observed in the transfer curve by applying a positive V_{GS}. The different performance of the devices should be due the higher capacitance provided by the $HfAlO_x$ based dielectric resulting on the collection of holes for negative drain voltages.

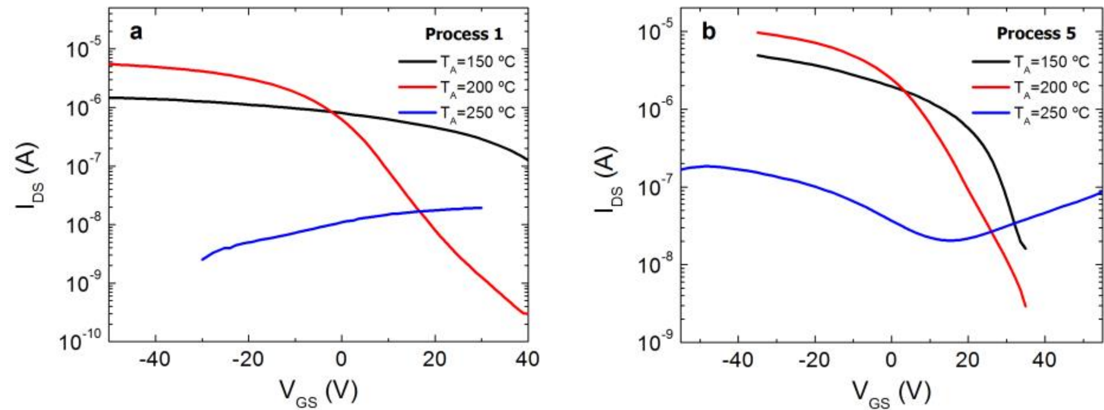

Figure 5.18. Influence of the annealing temperature on the TFTs with gate dielectric based on a) ATO and b) HfO_2

SnO_x ambipolar behavior was already achieved by Liang et al and Nomura et al [58], [59], where a post deposition annealing temperature of 400 °C was needed to achieve this behavior. To construct ambipolar thin film transistors is necessary to balance the injection of holes and electrons, as well as their transport. The injection of both carriers from the source/drain electrodes to the channel layer depends on the band alignment between source/drain electrodes and the semiconductor layer. When applying a negative V_{DS}, the charge injection takes place as the Fermi level of the source electrode lines up with the valence band maximum (VBM) of the semiconductor for hole injection or as the Fermi level of the drain electrode matches with the conduction band minimum (CBM) for electron injection. For positive V_{DS}, is necessary a band alignment between drain electrode and VBM and source electrode and CBM, for holes and electrons injection, respectively. SnO_x is a good candidate to achieve this, since it has a small fundamental bandgap (0.5-0.7 eV) facilitating the band alignment to reduce the injection barriers [60], [61].

Both for negative and positive V_{DS} regions (Figure 5.19 a) and b)) the output characteristics exhibit current enhancement when V_{GS} is negative and positive respectively, but the pinch-off and current saturation are not clear due to the high off currents.

It is observed a standard saturated behavior for holes (electrons) and a significant superlinear increase in I_{DS} at low V_{GS} and high V_{DS}, that can be explained by the injection of electrons (holes) from the source (drain) electrode, being a typical output characteristic for an ambipolar TFT [59], [62].

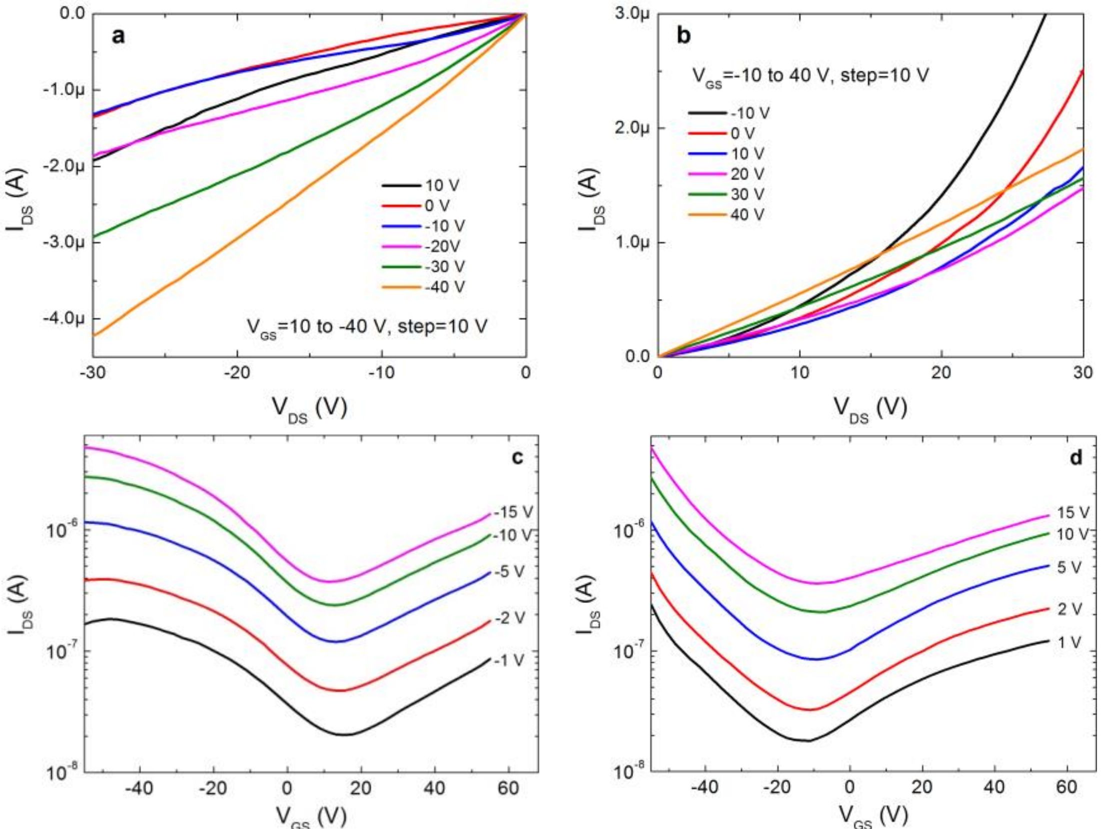

Figure 5.19. Output characteristics under a) p-channel and b) n-channel operation. Transfer characteristics under a c) negative and a d) positive V_{DS}

As seen on Figure 5.19 c) and d), the transfer curves of the ambipolar transistor exhibit a characteristic V-shape, where one arm indicate electron transport and the other indicate hole transport. We can also observe that the transfer curve for the opposite carrier channel shift with the applied V_{DS} of one carrier are dependent. For positive (negative) applied voltages, the effective gate voltage for holes (electrons) depends on the applied source-drain voltage, which gives rise to the characteristic dependence of the transfer characteristics on the source-drain voltage.

The p and n-channel operations show a linear field effect mobility of $2x10^{-2}$ $cm^2V^{-1}s^{-1}$ and $2.6x10^{-3}$ $cm^2V^{-1}s^{-1}$ respectively. This result indicates that the injection of holes is higher than the injection of electron for the ambipolar TFT.

5.1.4. Electrical stability

5.1.4.1 Constant drain current and constant gate bias stress

Bias stress effect is a phenomenon known by the change on the threshold voltage of a transistor over time, when a gate-source voltage is applied to create a channel in a field effect transistor. This effect has been widely investigated in a-Si:H TFTs, where it has been studied as a dispersive phenomenon [23–25] and also in oxide based transparent electronics, being the most studied the thin film transistors based on ZnO, GIZO, ZTO,[54], [63]–[66]. The current instability effects play an important role in defining the overall TFTs electrical performances, since the main characteristic variations of TFTs, such as threshold voltage, field effect mobility and sub threshold variations, occurred from the bias stress and can limit or make possible their practical application in complex electronic circuitry such as active matrix organic light emitting diodes (AMOLED) [67].

The bias stress effect is attributed to the trapping of carriers from the gate bias induced conduction channel into localized electronic sates [67]. These states could be located within the semiconductor or dielectric, or at the semiconductor/dielectric interface. The number of trap carriers increase as longer as the gate bias is applied. Although the trapped carriers still contribute to the charge balance in the TFT, they do not contribute to the drain current resulting in a larger shift in threshold voltage, V_{th}. After the gate bias is removed, the trapped carriers either return to mobile states, or they remain trapped until the trap states are physically removed with thermal annealing, for example, depending on the physical characteristics of the trap states.

From Figure 5.20 we can observe that as the stress times increases, the transfer characteristic is gradually negatively shifted and the slope of the curves does not show large variation indicating that there is no degradation of the field effect mobility, μ_{EF}, (less than 9% from the t=0 s to $t=2.3x10^4$ s) and of the sub-threshold swing, S. This result agrees with the reported in literature both for organic or inorganic n and p-type thin film transistors [68]–[73] and indicates that the creation of additional interface states induced by the gate bias could be negligible, being the dominant mechanism for the threshold shift the hole trapping at the semiconductor/dielectric interface [68], [71].

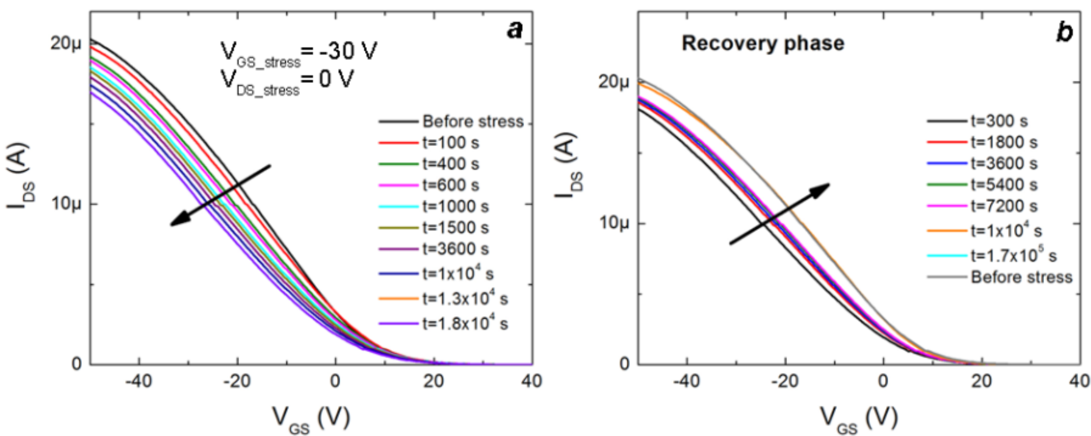

Figure 5.20. Stress (a) and recovery (b) experiments regarding device deposited with a %O_2 = 2.5%, pd = 0.2 Pa and ts = 12 nm annealed at 200 °C (VD=-2 V, VGS_stress=-30 V).

Figure 5.21 shows the absolute value of the threshold voltage shift, ΔV_{th}, under an application of a constant gate bias of -30 V during $1.9x10^4$ s. The threshold voltage time evolution is well fitted with the stretched exponential time dependence equation defined by [72]:

$$\Delta V_{th} = V_0 \left\{ 1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta} \right] \right\} \quad \textbf{5.3}$$

where V_0 is ΔV_{th} at infinite time (threshold voltage when equilibrium has been reached at t→∞) , β is the stretched-exponential exponent, and τ is the characteristic trapping time of carriers. V_0 depends on the bias stress voltage and is determinate by

$$|V_0| = |(V_{ST} - V_{thi})|^{\alpha} \quad \textbf{5.4}$$

where V_{ST} is the bias stress voltage applied, V_{thi} is the initial threshold voltage and α is a parameter associated with the interface qualities. For the device shown in Figure 5.21, measured in air at room temperature, the fitted parameter values were $\tau=5x10^3$ s, β=0.65 and V_0=3.8 V.

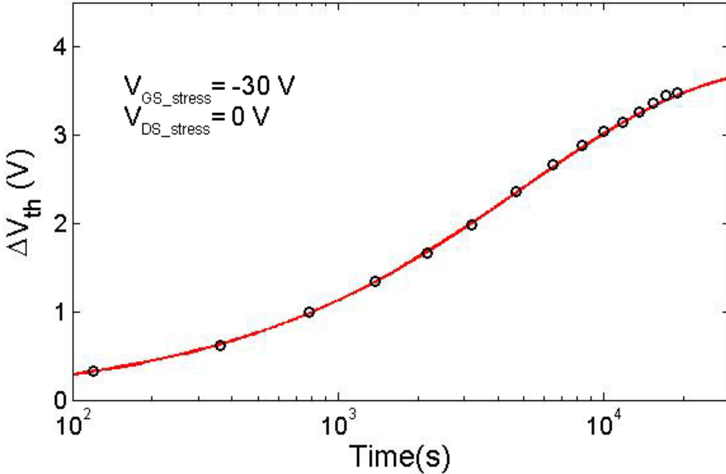

Figure 5.21. Bias stress induced threshold voltage shift as a function of time on a logarithmic scale. (V_{DS}=-1 V).

- *Constant gate bias stress and drain variation*

Figure 5.22 shows the threshold voltage variation, ΔV_{th}, as a function of the gate-bias stress time under various drain-bias stress voltages.

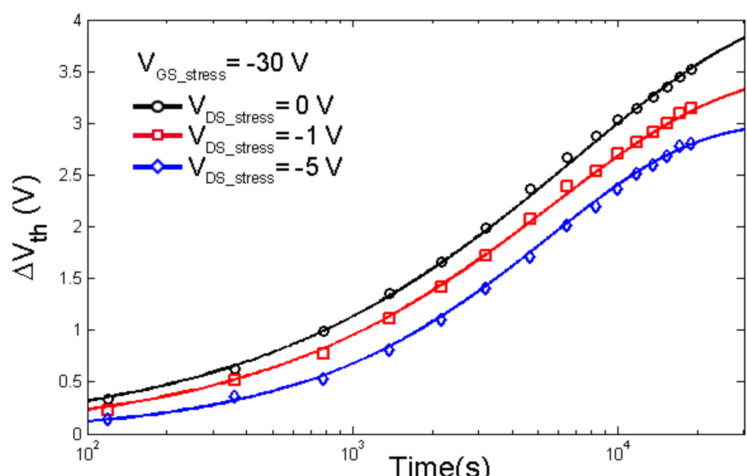

Figure 5.22. Shift of threshold voltage as a function of stress time for different drain biases (V_{DS}=0 , -1 and -5 V), constant V_{GS}=-30 V and V_{DS}=-1 V.

Table 5.7 summarizes the results of the bias stress measurements. We can observe that larger drain-source voltage leads to a slower bias stress-induced threshold voltage shift and reduces the time constant τ.

This is due to the fact that a larger drain-source voltage neutralizes the electrical field generated by the gate-source voltage near the drain contact, resulting on the decrease of the carrier density in the channel close to the drain contact and reducing the number of carriers trapped per time and area [67], [74]. The stretched-exponential exponent β increases as the drain-source voltage becomes larger, meaning that the trap distribution becomes more uniform and thus the response becomes less stretched when the drain-source voltage is increased.

Table 5.7. Electrical properties of the devices depicted in Figure 5.22

VDS (V)	β	τ (s)	V_0 (V)	α
0	0.6	6900	4.2	0.46
-1	0.66	5700	3.5	0.39
-5	0.8	5500	3	0.34

5.2. TFTs with Cu-doped SnO_x channel

5.2.1. Process flow and device structure

P-type Cu-doped SnO_x based TFTs were produced in the same way as described at 5.1.1., using soda-lime glass substrates coated with indium tin oxide (ITO, 200 nm) and aluminum titanium oxide (ATO, 220 nm), supplied by Planar Systems, corresponding to the gate electrode and the gate insulator respectively. The channel layer based on Cu and Sn was deposited by r.f magnetron sputtering using two different targets metallic Sn and metallic Cu of 2-inch diameter (provided by Plasmaterials) in a AJA ATC ORION8 system without any intentional substrate heating. Ni/Au contacts (≈6/60 nm respectively) where deposited by e-beam evaporation in a homemade system. The devices were then annealed in air, in a hot-plate at 150 ^{o}C and 200 ^{o}C for 1 hour (450 ^{o}C/h ramp). All necessary patterning was done by photolithography and lift-off using the same lithographic masks as in Figure 5.1.

Electrical characterization of TFTs was performed at room temperature with an Agilent 4155C semiconductor parameter analyzer and a Cascade M150 microprobe station. Devices characterized had a width to length ratio of 50 to 50 μm. Figure 5.23 shows a schematic of the process used to produce the TFTs.

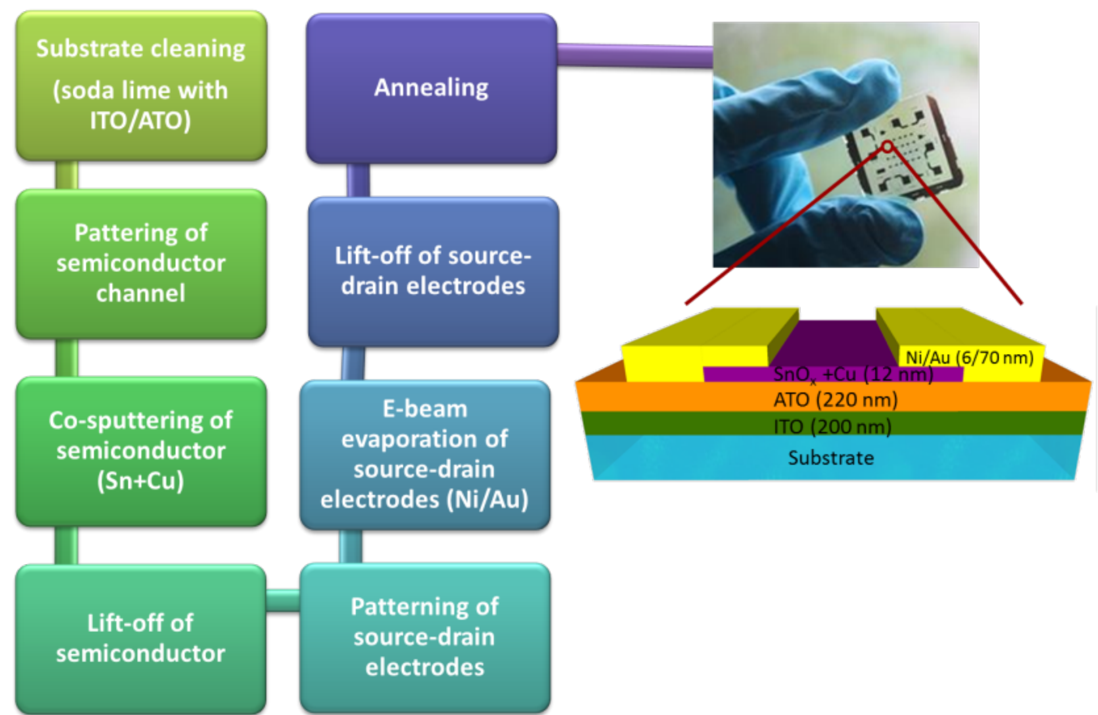

Figure 5.23. Process flow used to produce TFTs based on Cu-doped SnO_x and schematic of the bottom gate device structure.

5.2.2. Influence of the deposition and post-deposition parameters on the electrical properties of Cu doped SnO_x TFTs

The main goal of doping SnO_x with Cu was to produce a p-type transparent semiconductor oxide with improved electrical properties. In this sub chapter is evaluated the electrical properties and performance of the doped semiconductor as a channel in a TFT.

5.2.2.1 Percentage of Cu in the (Sn+Cu) mixture

Figure 5.24 shows the I_{DS}-V_{DS} characteristics of Cu-doped SnO_x TFTs with %Cu varying between 0% and 7% after annealing in air at 200 °C with W/L=1 µm. The drain voltage (V_{DS}) is swept from +0 to -30 V and the gate voltage (V_{GS}) is stepped between +10 and -30 V. The device based on undoped SnO_x shows a clear linear and saturation regions of the output characteristics and do not present significant current crowding for low V_{DS}, indicating low series resistance in source-drain contacts with SnO_x. As the content of Cu increases we can observe that the drain current increases and the saturation region is no longer clear and well defined showing the more metallic behavior of the semiconductor.

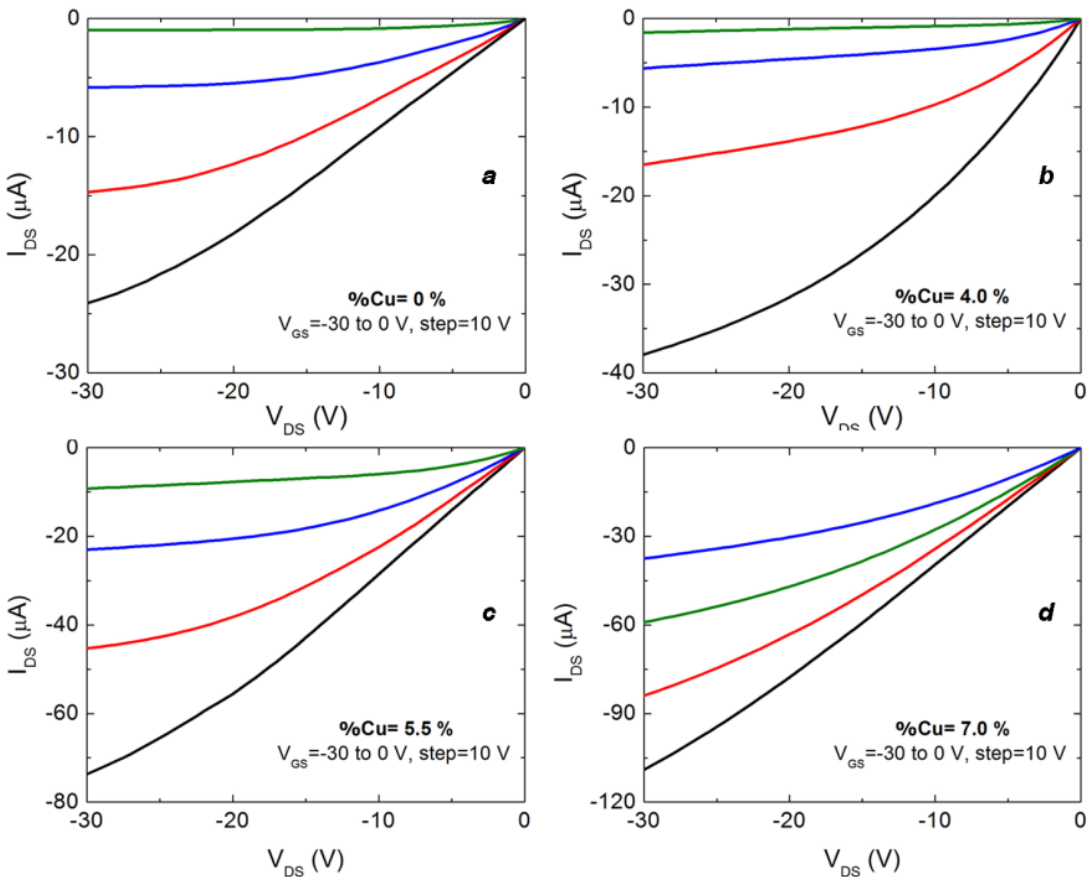

Figure 5.24. Output curves for the TFTs deposited with %O_2= 4.0 %, p_d= 0.2 Pa and a Cu content of a) 0 %, b) 4.0 %, c) 5.5 %and d) 7.0 %, annealed at 200 °C.

Figure 5.25 shows the I_{DS}-V_{GS} transfer characteristic of the devices with V_{DS}=-2 V. For all the devices the leakage current (I_{GS}) value is quite low, (10^{-11}-10^{-13} A), for the swept voltage used showing that ATO provides good insulating properties even for large negative bias.

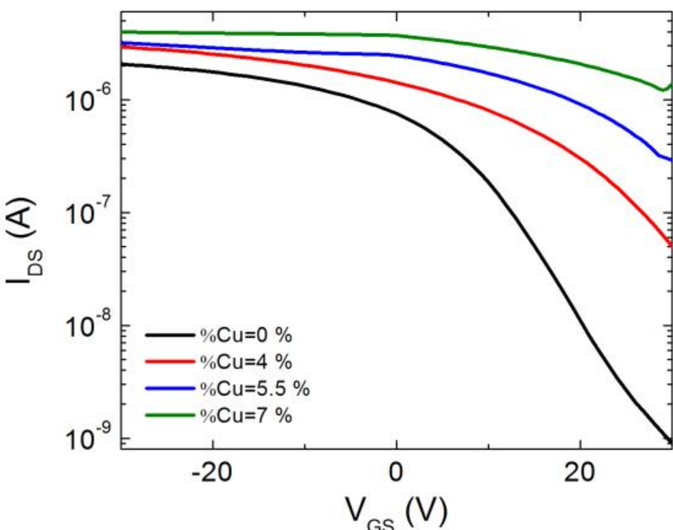

Figure 5.25. Transfer characteristics curves of the TFTs with %O_2= 4 %, p_d= 0.2 Pa as a function of the Cu content, annealed at 200 °C.

Table 5.8 summarizes the devices performance of Cu-doped SnO_x Doping SnOx with Cu leads to an increase of the filed effect mobility which is consistent with the electrical results obtained from Hall effect measurements and discussed on Chapter 4.

As the content of Cu increases, the carrier concentration of free charges in the bulk of the semiconductor also increases. This is reflected at the performance of the device in two ways; as an increase of the threshold voltage due to the higher voltage required to deplete the semiconductor channel and the subthreshold swing degradation because of the higher content of traps present at the semiconductor layer and at the semiconductor/dielectric interface as confirmed by the increase of D_{it}.

Table 5.8. Electrical properties of the devices depicted in Figure 5.25.

%Cu (nm)	On-Off ratio	μ_{FE} (cm^2 V^{-1} s^{-1})	V_{th} (V)	S (V dec^{-1})	D_{it}
0	9.96X10^3	0.43	12.53	5.71	3.80X10^{13}
4	5.78X10^1	1.07	23.41	5.75	3.82X10^{13}
5.5	1.08X10^1	1.35	32.07	13.33	8.91X10^{13}
7	3.29	1.48	46.77	25.54	1.72X10^{14}

5.3. Conclusions

Controlling the deposition parameters and the post annealing conditions resulted in different electrical performance of the TFTs due to the electrical and morphological properties changes of the channel semiconductor.

- *Dependence on oxygen content and deposition pressure*

For higher oxygen content and lower deposition pressure, we achieved a TFT working in accumulation mode. This achievement is very important since the application of this type of TFTs in complementary circuits requires lower power consumption due to the lower voltage necessary to turn on the device. In order to obtain faster devices and still with a higher On-Off ratio, the oxygen content and the deposition pressure must be lower, as it is seen for the device produced with $\%O_2$= 2.5 % and p_d= 0.2 Pa. Increasing the deposition pressure results in worst devices, in a general way, because V_{th} increases, while μ_{FE} and On-Off ratio decrease.

- *Dependence on semiconductor layer thickness*

The semiconductor layer thickness also plays an important role on the devices performance. In one way, with lower thickness semiconductor the device works on enhancement mode and has a lower V_{th}, which reduces the power consumption of the device, and has less interface defects (lower S). On another way, the field effect mobility is improved for higher semiconductor thicknesses.

- *Dependence on annealing temperature*

The as-deposited SnO_x films produced at room temperature are composed of β-Sn phase or are amorphous, requiring an annealing step to crystallize the films to SnO_x in order to obtain p-type conduction. Annealing the devices up to 200 °C decreased the threshold voltage and on the off current and improved the On-Off ratio.

- *Influence of gate dielectric*

Despite we have observed that the properties of the semiconductor are very important for the performance of the TFT, also the properties of the gate dielectric results in a change of the device properties. Due to the condition of SnO_x semiconductor channel layer, although different dielectrics were used to fabricate p-type TFTs, a common feature between them is the large off-current and the depletion mode operation. Such characteristics were ascribed to the high hole density of the SnO_x films, which, has shown, strongly depends on the deposition parameters and post annealing conditions. However it was possible to improve the electrical characteristics of the

devices, by using $HfAlO_x$ dielectric produced by ALD. Using gate dielectrics with higher capacitance and lower roughness, based on a multicomponent layer of Al_2O_3 and HfO_2, resulted in a lower V_{GS} range for to the working mode of the device as well as an increase of the On-Off ratio and of the field effect mobility of the SnO_x based TFTs.

Ambipolar SnO_x TFTs were demonstrated by annealing the devices with $HfAlO_x$ gate dielectric at 250°C. While the devices with ATO gate dielectric showed an inversion of the operation mode, the devices where the gate dielectric is based on $HfAlO_x$ showed ambipolar operation. This behavior could be attributed to the large capacitance of the latter.

- *Cu-doped SnO_x TFTs*

Doping SnO_x semiconductor with Cu also results in transparent p-type thin film transistors. Despite the lower On-Off ratio and the higher threshold voltage, the field effect mobility increased as the Cu content increases. Although it was not totally possible to describe and understand in detail the role of Cu in the SnO_x matrix, it was demonstrated that is possible to produce p-type TFTs doping SnO_x.

5.4. References

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6. FINAL CONCLUSIONS AND FUTURE PERSPECTIVES

6.1. Conclusions

The research work presented in this dissertation was divided into two main areas. The first objective was to study, produce and optimize sputtered p-type oxide semiconductors based on SnO_x and the second objective was to study the influence of these oxide semiconductors prepared under different processing and post processing conditions when applied as channel layer on TFTs.

In this chapter are presented general conclusions about these topics, as well as some future perspectives for further development of this research area, based on the results of this dissertation and on recent reports in literature.

6.1.1. p-type oxide semiconductors

This work focused on the production of p-type oxide semiconductors through three different tin oxide based systems; tin oxide, copper-doped tin oxide and indium-doped tin dioxide. In order to obtain these materials, sputtering technique was used without intentional substrate heating. Several variables, such as, content of oxygen, deposition pressure and post-annealing temperature strongly influence the conductivity type of these materials as well as it's structural and morphological properties. These materials exhibit p-type conductivity for a very limited range of these variables.

- *SnO_x*

During this dissertation transparent oxide semiconductors based on SnO_x were developed using reactive magnetron sputtering technique without intentional substrate heating, exhibiting p-type conductivity after a low temperature annealing at 150 °C and 200 °C.

The as deposited SnO_x films are crystalline, presenting only β-Sn phase, and after the annealing they present a mixture of both tetragonal β-Sn and α-SnO phases and an increase of crystallite size. With the increase of oxygen content within the deposition chamber, Sn^{2+} oxidizes to Sn^{4+}, resulting in a decrease on the crystallinity of α-SnO phase, and consequently an amorphous structure for higher contents. With the increase of oxygen content, the films structure changed from a lamella like grain morphology to an equiaxed structure and finally to a very fine and smooth nano structure, with lower grain size and surface roughness.

Concerning the optical properties, the p-type SnO_x films present E_{opt} ≈2.8 eV and for 30 nm thick films the optical average transmittance is around 85 %, between 400 and 800 nm, decreasing to about 50 % when the film thickness is enlarged by a factor of 4.

The p-type conductivity is obtained for a narrow content of oxygen, between 2.5 % and 4 % highly dependent on the post deposition annealing temperature, between 150 °C and 200 °C. Within these ranges the hole carrier concentration obtained was in the range of $\approx 10^{16}$-10^{18} cm^{-3}, resistivity between 7 and 76 Ωcm and mobility reaching a maximum of 3.1 $cm^2 V^{-1} s^{-1}$.

From XPS measurements it was possible to analyze the composition and the oxidation state of the elements present in the SnO_x p-type film with $\%O_2$=4% deposited at p_d=0.2 Pa. While the as deposited film is composed of Sn^0, Sn^{2+} and Sn^{4+}, after annealing at 200 °C Sn^{2+} and Sn^{4+} are present, indicating that the mixed oxidation states is responsible for the origin of V_{Sn} and O_i and consequently for the p-type conductivity.

- *Cu-doped SnO_x*

P-type Cu-doped SnO_x were produced using the same deposition technique, sputtering, from metallic Sn and Cu targets. Depending on %Cu, both n-type and p-type semiconductive films can be obtained with distinct optical and structural properties. Also for this system, the post-deposition annealing plays an important role in order to obtain p-type conductivity.

P-type conductivity was achieved for a %Cu between 4.0% and 7.0% after annealing at T_A=200°C. with the increase of Cu content, both mobility and carrier concentration increase and the resistivity decreases.

As observed for SnO_x, the as deposited films presented metallic β-Sn phase and, as the %Cu increases, CuSn phase appears. After annealing at T_A=200 °C, both both β-Sn and α-SnO phases were present and the films with higher %Cu also have the main characteristic peak of Cu_6Sn_5.

From SEM images it was possible to observe grain with different sizes and morphology, that should correspond to different materials with different oxidation states.

Regarding the optical measurements, we can observe that the as deposited films, due to the presence of metallic tin, presents a low transmittance in the visible region, that increases significantly after annealing at T_A=200 °C. E_{opt} decreases, as %Cu increases, due to the Cu oxide nature, which has a lower E_{op} than SnO_x films.

P-type conductivity of Cu-doped SnO_x films was achieved for the films annealed at 200 °C and a %Cu between 4.0% and 7.0%. The mobility in enhanced to 1.91 cm^2/Vs , the resistivity of the p-type SnO_x film drops from 75.7 to 9.35 Ωcm^{-1} and the carrier concentration increases from $7.5x10^{16}$ to $3.5x10^{17}$ cm^{-3} as the content of Cu increases.

- *In-doped SnO_2*

As for the two others SnO_x based system, depending on the content of the dopant (%In) and on $\%O_2$ both n- and p-type conductivity were obtained. While for lower $\%O_2$, lower %In had to be used, for higher $\%O_2$, it was necessary to doped with more In, in order to obtain p-type conductivity.

For low $\%O_2$ and low %In, In^{3+} plays as acceptor, which makes the films p-type, with lower resistivities (0.35-52.6 Ωcm), μ_{FE} between 26.3 and 0.862 $cm^2Vs^{-1}$and N between $4x10^{15}$ and $2x10^{19}$ cm^{-3}. Further increase of %In ratio should lead to the an excess of indium oxide phase in the films, and therefore the films became n-type.

When increasing $\%O_2$, p-type behavior is observed for the films with higher content of In the activation of the acceptor effect of In^{3+} substituting Sn^{4+}. For lower $\%O_2$ and higher %In, indium atoms were not activated to behavior as acceptors, so the films were n-type because of the intrinsic defects.

It was achieved a p-type oxide conductor, with resistivity of $5.1X10^{-3}$ Ωcm, mobility of 22.8 cm^2Vs^{-1} and carrier concentration of $5.4x10^{19}$ cm^{-3} for %In=26 % and $\%O_2$= 5 %.

From XPS measurements performed in both n- and p-type In-doped SnO_2 films, we observed that, while no Sn^{2+} is present for the n-type film, the p-type film had a mixture of Sn^{2+} and Sn^{4+}, as observed for SnO_x p-type film, that could be the responsible for the origin of V_{Sn} and O_i and consequently for the p-type conductivity.

The VBM for the n-type TIO film is similar to what is reported for n-type SnO_2 for p-type TIO film is ~1.24 eV, the hump at 2-3 eV is less pronounced in p-type TIO than in SnO_x.

The mean transmittance in the visible region of In-doped SnO_2 films is ~65% for the films deposited with lower $\%O_2$ and increases to ~80% for higher $\%O_2$. When increasing the content of In, the optical bandgap increases, due to the presence of In_2O_3.

6.1.2. P-type oxide semiconductor based thin-film-transistor

Despite the deposition conditions of the semiconductor channel layer, i.e., percentage of oxygen, deposition pressure, thickness and of the gate dielectric used, the, post-annealing has a strong influence on the electrical properties of the resulting devices. The best TFTs performance was achieved annealing the TFTs at 200 °C, since improves the electrical properties of the TFTs, higher field effect mobility and On-Off ratio and lower threshold voltage. The best properties were achieved with SnO_x films deposited at $\%O_2$=2.5-4.0 %, p_d=0.2-0.3 Pa and T_A=200 °C.

Even within this limited range of conditions, several non-ideal effects occur, such as, highly conductive channel layers, with higher N and consequently always-on devices with high $V_{th.}$ Still, for higher N p-type oxide semiconductors, for lower p_d and d_s it was possible to obtain good performing transistors with high μ_{FE} and low V_{th}.

As stated before, T_A has a strong influence on the device performance. This is because first is necessary an annealing step to obtain p-type conductivity and then, as T_A increases, V_{th} decreases and the On-Off ratio increases.

When the processing conditions deviate from this, the main issue is that the device will no longer work as p-type, since the conductivity of the semiconductor changes to n-type.

Also the gate dielectric had a strong influence on the devices performance. Despite the large off-current and the depletion mode of the SnO_x p-type transistors, using $HfAlO_x$ dielectric produced by ALD, it was possible to improve the electrical characteristics, such as, a lower V_{GS} range for to the working mode of the device, an increase of the On-Off ratio and the improvement of μ_{FE}. This was observed for T_A=200 °C, but when annealing at T_A=250 °C, it was observed an ambipolar behavior, while for the devices with ATO gate dielectric, the TFTs showed n-type conductivity. This means, that with the appropriate gate dielectric, it is possible to have n- and p-type TFTs, with the same material deposited with the same conditions.

Doping SnO_x with Cu also results in transparent p-type thin film transistors, despite the general performance of the device was poor. A lower On-Off ratio and the higher threshold voltage were obtained, while the μ_{FE} increased as the Cu content increases.

6.2. Future perspectives

During this PhD thesis, different paths were covered that allowing to achieve several conclusions and also gave the appearance of new ways to explore and many questions to answer.

P-type SnO_x based films were extensively explored during this dissertation, where unique properties having been obtained. However, since some issues remained unclear, the study of this type of material should be continued. It is essential a better understanding of the band structure of the undoped and doped material, particularly the function and influence of the dopant. The analysis by XPS could be very useful for the compositional analysis, mainly for the detection of the dopant and O_2 in the films.

Despite r.f. sputtering is a technique where high quality and uniform films can be obtained without intentional substrate heating, it uses vacuum systems limiting the cost reduction. Other alternatives are based on solution processes systems, such as spin-coating, Ink-jet and spray pyrolysis. From these techniques, ink-jet has been the most promising, since it allows the deposition of materials with predefined patterns.