Pedro Daniel Manta de Almeida

Licenciado em Ciências da Engenharia Electrotécnica e de Computadores

An RF LC Q-enhanced CMOS filter using Integrated Inductors with layout optimization

Dissertação apresentada para obtenção do Grau de Mestre em Engenharia Electrotécnica e de Computadores, pela Universidade Nova de Lisboa, Faculdade de Ciências e Tecnologia.

Orientador : Maria Helena Silva Fino, FCT-UNL

Júri:

Presidente: Prof. Fernando José Vieira do Coito

Arguentes: Prof. Luis Bica de Oliveira

Vogais: Prof. Maria Helena Silva Fino

Prof.

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

Abril, 2013

RF LC Q-enhanced CMOS filter using Integrated Inductors with layout optimization

To my parents and my girlfriend

Acknowledgements

I am deeply grateful to my advisor Prof. Helena Fino for her expert guidance, stimulating suggestions, patience, constant encouragement and never-ending supports.

I must to thank all my colleagues and friends that I have interacted with in the past few years. They exposed me to a variety of challenging, invigorating and enjoyable experiences.

I want to give a special thanks to a very important person in my life, Carlota Faria, for the encouragement and motivation in the long journey of my research and for helping me stay focused and stabilized.

Finally, a special thanks to my parents, Isabel e Daniel Almeida, for their love and support. My parents have always believed in and encouraged me in all my endeavors and without their support I would never have been able to accomplish what I have now.

You all deserve the best.

Abstract

The advancement of CMOS technology led to the integration of more complex functions in a single chip. In the particular of wireless transceivers, integrated LC tanks are becoming popular both for VCOs and integrated filters. The design of a 2^{nd} order CMOS 0.13 μm Q-enhanced integrated LC filter for a frequency of 2.44 GHz is presented. The intent of this filter is to create a circuit for integrated wireless receiver and minimize the requirement for off-chip passive filter components, reducing the overall component count and size of wireless devices and systems. For RF applications the main challenge is still the design of integrated inductors with the maximum quality factor. For that purpose, tapered, i.e, variable width inductors have been introduced in the literature. In this work, a characterization of variable width integrated inductors is proposed. This inductor model is then integrated into an optimization procedure where inductors with a quality factor improvement are obtained.

Keywords: Inductor layout optimization, variable metal width, integrated RF inductor, Q-enhanced RF LC filter.

Resumo

Com o avanço da tecnologia CMOS surgiram funcionalidades mais complexas num único circuito integrado. No caso particular de emissores-receptores sem fios, tanques integrados LC estão a tornar-se populares, tanto para VCOs (Osciladores controlados por tensão) como para filtros integrados. O projecto de um filtro LC integrado de segunda ordem com melhoramento de factor de qualidade é apresentado neste trabalho. A intenção deste filtro é a de criar um circuito integrado para a recepção sem fios minimizando o requisito de componentes passivos não integrados, reduzindo o número de componentes e tamanho global de dispositivos sem fios e sistemas. Para aplicações de RF (Frequência de rádio) o principal desafio ainda é o projecto de bobines integradas com elevado factor de qualidade. Para este efeito, bobines de espessura variável têm sido propostas por vários autores. Nesta tese é proposta uma caracterização de bobines integradas de espessura variável. Este modelo de bobine é então integrado num processo de optimização, onde são obtidas bobines com uma melhoria de factor de qualidade

Palavras Chave: Optimização geométrica da bobibe, espessura variável, bobine integrada, Filtro LC com melhoramento do factor de qualidade

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The radio frequency (RF) and wireless market has suddenly expanded to unimaginable dimensions. With the emergence of cellular phone, wireless local-area network (WLAN) and Bluetooth technology, we are standing on the threshold of a new radio frequency epoch. In the field of communication circuit design, the realization of the complete integration of RF transceivers and digital signal processing blocks onto a single integrated circuit (IC) is a logical area in which to develop system-on-chip (SoC) solutions [3]-[4]. By doing this, the cost and the difficulty of assembly and tuning are reduced drastically. Presently, the growing demand for multi-functional wireless communications systems is becoming increasingly evident. Meanwhile, the lower cost and faster advance of CMOS processes has motivated extensive efforts in designing RF CMOS circuits. CMOS technologies exhibit properties and limitations that directly impact the design of a receiver from the architecture level to the device level and from the RF front end to the baseband processor.

In the long term, traditionally analog functions of a radio receiver (see figure 1.1 will be replaced with software or digital hardware. The final goal of a radio receiver would be to digitalize the radio frequency (RF) signal at the out put of the antenna, allowing the implementation of all receiver funtions in either digital hardware or software [5].

Achieving this would be very interesting for many reasons. It would reduce product development time and costs. It would also allow to implement new functions that are impossible to implement in analog hardware. Another great advantage would be the

possibility of creating receivers designed to allow reception of different modulation types.

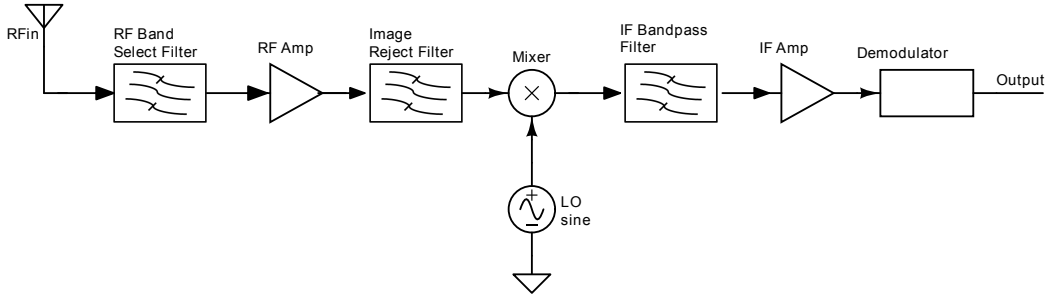


Figure 1.1: Typical radio receiver [1]

The ever increasing demand for wireless communications motivates in reducing complexity, cost, power dissipation, and the number of external components in selecting receiver architecture (figure 1.1). The integrated inductors spiral plays an important role in the development of Si RF ICs. The spiral inductor has a great influence on the performance of many RF circuits. The obvious example is the LC tank, in which the quality factor Q of the spiral inductor determines the bandwidth and the resonance impedance of the LC tank. Another example is the bandpass filter built with inductor and capacitors, in which the quality factor of the spiral inductor determines the insertion loss [6]. Following the success in fabrication, intensive research has been conducted in the modeling of spiral inductors on silicon. One approach is to use a compact circuit model. In other way, a lot of work has been done in the synthesis and optimizations of spiral inductors in silicon. The purpose of this thesis is to present an optimization method for the design of spiral inductors. The focus for this optimization is on the geometric layout of the spiral inductor. We develop a theory based on fundamental electronic principles that yields simple, accurate inductance expression for on-chip spiral inductors of various geometries.

Besides the introduction, this thesis contains 4 chapters. In Chapter 2 an introduction to integrated spiral inductors is presented, and the well known pi-model is introduced. Analytical physics-based expressions for the model elements are givel, and finally working examples proving the validity of the model are shown. In Chapter 3 the adequation of the previously described model to variable width integrated indutors is described. After

validating this model, optimization methodologies are applied to the design of variable width inductors, leading to final designs with quality factor improvement (for the same area) in the order of 20%. In Chapter 4 the variable with integrated inductors are used for designing LC-filters. Examples considering the application for 2.44 GHz are presented. Finally, in Chapter 5, conclusions are offered.

Chapter 2

Integrated inductors

The growth of wireless applications in the low GHz frequency range has been a catalyst in numerous research activities to develop wireless applications. CMOS is considered a technology of choice in the integration of radio frequency systems in the low frequency range (up to a maximum of 10 GHz) because of the relatively lower costs in developing single chip solutions over other semiconductor processes. For RFIC in CMOS, planar inductors will have a dominant role in defining the achievable performance of the system as a whole. Depending on the technology possibilities, several metal layers may be used and different geometries can be adopted. In this work a 0.13μm CMOS technology is used for implementing spiral inductors. In this chapter we review on-chip inductor realization and see how they can be modeled.

2.1 Introduction

Inductors are components used to store energy in the form of magnetic field. However integrated inductors are not easy to implement because of their non-ideal behaviour that entail a myriad of trade-offs. Parasitic effects, such as coupling capacitance and losses related to the integration substrate, affect these devices, degrading their performance [7]. In order to understand these trade-offs, both vertical and lateral of the layout have to be considered.

Figure 2.1 shows a typical implementation of an integrated spiral inductor where the important physical dimensions of the spiral inductor are identified: inner diameter (d_{in}),

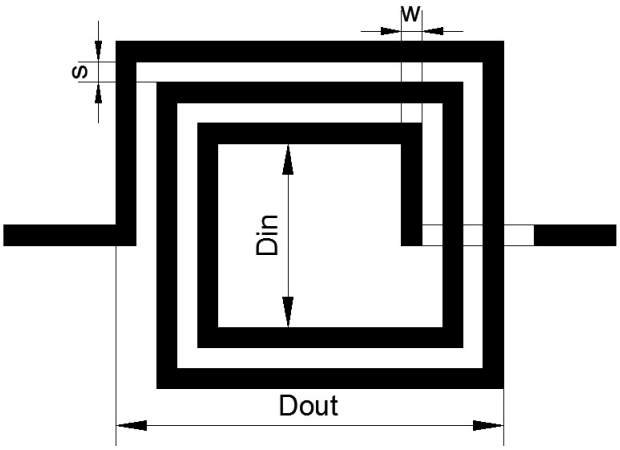


Figure 2.1: Typical layout of an integrated spiral inductor

outer diameter (d_{out}), space between turns (s) and width of metal trace (w). Since we have chosen to fill in the spiral down to the inner diameter,

$$d_{out} = d_{in} + 2nw + 2(n-1)s \tag{2.1}$$

.

The top and outermost end of the inductor are directly connected to a port while the inner end is connected to the metal strip or air bridge from beneath. Generally, the uppermost layer of metal is used for construction as it offers a low resistance to the current.

2.2 Inductor model

Quality factor (Q) of inductors in RFIC applications is poor. For achieving high Q geometrical parameters of the inductors should be carefully determined so that the highest Q for the given technology may be obtained. Since inductor design parameters are highly correlated, optimization based design metodology are usually adopted. Since electromagnetical simulation is a time consuming process, designers usually adopt inductor models as a way of increasing the efficiency of the design task. Regarding integrated inductor models the approach can be found accurate with literature.

While many simulation techniques focus on determining the complete network behavior of an integrated inductor such as its 1- or 2-port s-parameters, this information is not always in the most useful format for designers. The behavior of a device, such as the

inductors, may in fact be understood from the s-parameters, but designers are generally interested in including one inductor device within a larger circuit or system. In this case, it is necessary to have a more compact representation of the device for its inclusion in a larger system. For this purpose, various models of integrated circuits represent compact inductors have been developed [8].

The simplest model available for representing inductors, showed in figure 2.2, is useful for characterizing the device's behavior at low frequencies and is composed of an inductor in series with a resistor that represents the ohmic losses along the length of the inductor.

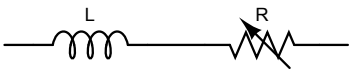


Figure 2.2: Simple 1-port model

This representation can be easily extracted directly from the 1-port complex impedance of the device, $Z_{in} = R + j\omega L$. However, at higher frequencies parasitic capacitors must be taken into account and this model becomes insufficient.

In order to take into account the losses over a range of frequencies, circuits models of spiral inductors on silicon, such as the simple π-model proposed in [9] and represented in figures 2.3 and 2.4.

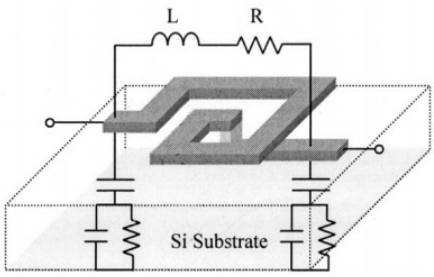


Figure 2.3: On-chip implementation of a spiral inductor

However and notwithstanding the fact that more accurate models have been proposed and developed, the simple π-model of spiral inductor on silicon is the most common model used by the designers due to its simplicity. Its parameters are easy to adjust to empirical data and they have a clear physical meaning. As a trade-off, this is a narrow band model because it is only valid for modeling the behavior of an inductor in a small range of

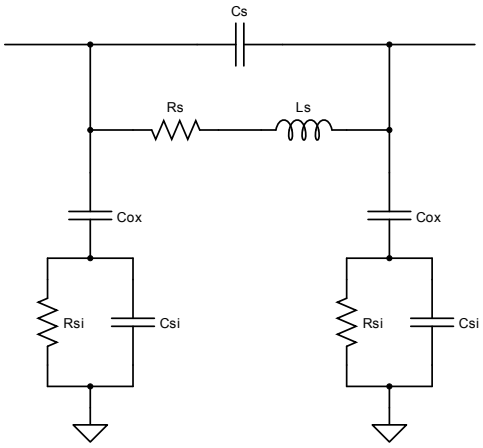


Figure 2.4: π circuit equivalent model of a spiral inductor

frequencies. For this reason it is normally used only to model the spiral at frequencies under few GHz.

So, in this circuit model, the inductor L_s models the inductance of the spiral inductor and the resistor R_s models the resistance of the metal trace. The capacitor C_s represent the direct coupling through the overlap between the spiral and the underpass. The oxide capacitance C_{ox} is the capacitive coupling between the inductor and the substrate through the oxide layer and the resistance and capacitance of the substrate, referred to ground, are modeled by R_{si} and C_{si}, respectively. The characteristics of each in this equivalent circuit model elements are strongly dependent on the inductor shape and on the technological parameters of the CMOS process used. In the next subsections, the analytical expressions for the evaluation of the π-model element values is presented.

2.2.1 Metal length

For the accurate calculation the length of the inductor be performed accurately a decomposition of the inductor in its elementary segments was accomplished. Our formula is derived in an inductor provided with a hollow center of an arbitrary inner diameter d_{in} that affects linearly the total length, l:

$$l = 4n(d_{in} + w) + n(w + s) + 4n(n - 1)(w + s). \tag{2.2}$$

In this work we also consider the half turns of the spiral inductor. Therefore, if the

spiral have an half turn it is necessary to add the length of that half turn,

$$\textbf{length of half inductor} = 2(d_{in} + w) + n_i(w + s) \tag{2.3}$$

where n_i corresponds to the integer part of the number of turns.

2.2.2 Series Inductance

The knowledge of series inductance is a critical point to engineers who develop and use on-chip inductors for RFICs. The inductance represents the magnetic energy stored in the device, although parasitic components may store energy as well. For the evaluation of the inductance, several approaches have been proposed, based either on fitting process to experimental values [4] or through physics-based equations (modified Wheeler formula) [10], where

$$L_S = K_1 \mu_0 \frac{n^2 d_{avg}}{(1 + K_2 \rho)}. \tag{2.4}$$

Given that, K_1 and K_2 are coefficients allowing the model to be adopted to several inductors shapes and are seen in Table 2.1,

Table 2.1: Modified Wheeler Expression's coefficients

Inductor shape	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

n is the number of turns, d_{avg} is the average diameter given by,

$$d_{avg} = \frac{1}{2}(d_{in} + d_{out}) \tag{2.5}$$

and ρ is the fill ratio defined as

$$\rho = \frac{(d_{out} - d_{in})}{(d_{out} + d_{in})} \tag{2.6}$$

.

From 2.6 two spiral inductors with the same average diameter but different fill ratios

will have different inductance values. The fuller one has a smaller inductance because its inner turns are closer to the center, thus contributing less positive mutual inductance and more negative mutual inductance [4].

2.2.3 Series Resistance

Series resistance R_S arises from the metal resistivity in the inductor and is closely related to the quality factor. As such, the series resistance is an important key parameter for inductor modeling. The electric resistance in a metal trace conductor is given by,

$$R_{Sdc} = \frac{l}{\sigma w t} \tag{2.7}$$

where the resistance dependence on the metal conductivity, σ, is explicit and the metal dimension is reflected by w, w and t (track thickness). The previous equation is valid for a conductor where the current density is uniform, typically at DC and low frequency circuits. On the other hand, when the inductor operates at high frequencies Eddy currents are induced on the conductor, leading to a non-uniform current distribution, formerly know as the skin effect [11]. This means that for hight frequencies, the useful conducting area in a conductor is reduced. The most critical parameter presenting in the skin effect is the skin depth and can be determined by [12],

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.8}$$

where f is the frequency and μ is the magnetic permeability of free space and σ the conductivity of the conductor.

Due to skin effect, for high frequencies R_S becomes a function of frequency given by

$$R_S = \frac{l}{\sigma w \delta (1 - e^{-t/\delta})} \tag{2.9}$$

For a planar conductor the previous equation just takes into account the top and the bottom walls of the conductor. This approximation is not a problem if the conductor width is greater than thickness. If not, neglecting the conductor side walls, can introduce a huge error in resistance estimation. To overcome this gap the following equations to evaluate

the conductor resistance were proposed where k is a correction factor that depends on w and t [11], [13].

$$\lim_{f\to 0} R_{ac} = R_{dc} = \frac{l}{\sigma w t} \tag{2.10}$$

$$\lim_{f\to \infty} R_{ac} = k\frac{l}{2\sigma\delta(w+t)} \tag{2.11}$$

$$R_S = \sqrt{R_{dc}^2 + R_{ac}^2} \tag{2.12}$$

2.2.4 Crossover Capacitance

The capacitance, C_S, appears between the spiral and the underpass necessary to connect the inner turn to the outside of the spiral inductor. For the evaluation of this capacitance, all overlap capacitances are considered [14] and it is calculated by

$$C_S = n_c w^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{2.13}$$

where ε_{ox} is the oxide permittivity, n_c is the number of overlaps and $t_{oxM1-M2}$ is the oxide thickness between the spiral upper and lower metal.

2.2.5 Oxide Capacitance

Between the spiral metal and the silicon substrate, the parasitic capacitance, C_{ox} is formed. An usually adopted equation to estimate this capacitance is

$$C_{ox} = \frac{1}{2}\frac{\varepsilon_{ox}}{t_{ox}} lw \tag{2.14}$$

where t_{ox} is the thickness of the SiO_2 between the inductor and the substrate and lw defines the area of the spiral.

2.2.6 Substrate Resistance and Capacitance

The substrate parasitic elements are a consequence of the time-varying magnetic field that penetrates into the silicon substrate, leading to power loss as well as a reduction in the spiral inductance. The substrate capacitance and resistance are given by

$$C_{si} = \frac{1}{2} C_{sub} lw \tag{2.15}$$

$$R_{si} = \frac{2}{G_{si} lw} \tag{2.16}$$

where G_{sub} is the substrate conductance per unit area and C_{sub} is the substrate capacitance per unit area, where,

$$G_{sub} = \frac{\sigma_{si}}{h_{si}} \tag{2.17}$$

and

$$C_{sub} = \frac{\varepsilon_0 \varepsilon_r}{h_{si}} \tag{2.18}$$

given that σ_{si} and h_{si} are the substrate height and conductivity [14].

2.3 Quality Factor of an Inductor

The quality factor (Q) of an inductor gives a measure of the goodness of the inductor and is usually adopted as the characteristic to be used when comparing inductors performance. The general expression for the quality factor is [6]:

$$Q = 2\pi \frac{energy\, stored}{energy\, loss\, in\, one\, oscillation\, cycle} \tag{2.19}$$

.

For inductors, the only desirable source of storing energy is magnetic field and hence any source of storing electric energy such as capacitances is considered as a parasitic. This electric energy has to be calculated and the equation 2.19 can be rewritten as

$$Q = 2\pi \frac{peak\,magnetic\,energy\ -\ peak\,electric\,energy}{energy\,loss\,in\,one\,oscillation\,cycle} \tag{2.20}$$

.

From equation 2.20 it is possible to realize that Q is zero for the frequency at which the peak magnetic energy is the same as the electric energy. That frequency is called the self-resonance frequency (SRF). This means that an inductor maintains is behaviour for operating frequencies below the self-resonance frequency, but for higher frequencies the component does not behave as an inductor and presents capacitive performances.

The π-model presented in figure 2.4 takes into account a set of various parasitic and loss elements, allowing to rewrite equation 2.20 as function of the passive elements. To do this, the circuit model is first transformed into its equivalent circuit with one port connected to the ground (Figure 2.5).

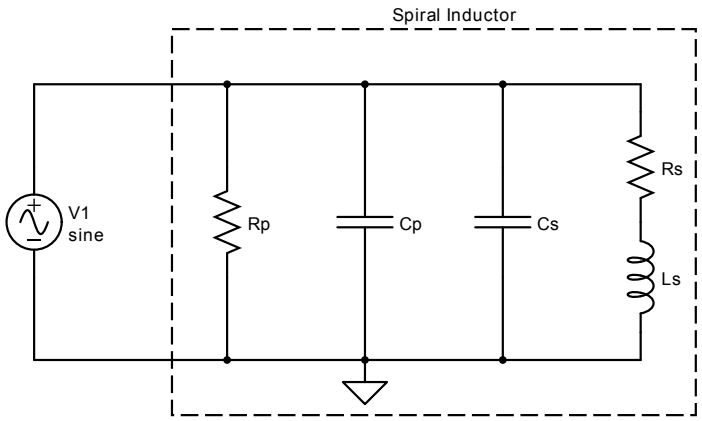


Figure 2.5: One port equivalent model of π model

This configuration aims to simplify the analysis of the Q behavior. The parasitic elements C_{ox}, R_{si} and C_{si} are replaced by its parallel equivalents C_p and R_p. These elements continue to be frequency dependent and are calculated as [6].

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \tag{2.21}$$

$$C_p = C_{ox} \frac{1 + \omega^2 (C_{ox} + C_{si}) C_{si} R_{si}^2}{1 + \omega^2 (C_{ox} + C_{si})^2 R_{si}^2} \tag{2.22}$$

Then, in order to obtain Q, we can calculate the energy associated to each of the passive elements in the equivalent circuit. The peak magnetic energy is related with the inductance L_s and given by

$$E_{peak\,magnetic} = \frac{1}{2}L_s V_0^2 = \frac{V_0^2 L_s}{2 \cdot [(\omega L_s^2) + R_s^2]} \tag{2.23}$$

where V_0 is the peak voltage at the inductor branch. The peak electric energy store in parasitic capacitances is

$$E_{peak\,electric} = \frac{1}{2}CV_0^2 = \frac{V_0^2(C_s + C_p)}{2} \tag{2.24}$$

and for last the energy loss in one oscillation cycle is

$$E_{loss\,in\,one\,oscillation\,cycle} = \frac{2\pi}{\omega} \cdot \frac{V_0^2}{2} \cdot \left[\frac{1}{R_p} + \frac{R_s}{(\omega L_s)^2 + R_s^2}\right] \tag{2.25}$$

According to definition (2.20) and replacing equations (2.23)-(2.25), the quality factor can be calculated as

$$\begin{aligned} Q &= 2\pi \frac{peak\,magnetic\,energy\ -\ peak\,electric\,energy}{energy\,loss\,in\,one\,oscillation\,cycle} \\ &= \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + \left[(\omega L_s/R_s)^+ 1\right] R_s} \\ &\quad \cdot \left[1 - \frac{R_s^2(C_s + C_p)}{L_s} - \omega^2 L_s(C_s + C_p)\right] \end{aligned} \tag{2.26}$$

Note that Q increases with increasing L_S and with decreasing R_S. Moreover, it appears form 2.26 should increase monotonically with the frequency. However, this is not the case. At higher frequencies the substrate losses becomes a dominant factor for Q. We can see three different terms in previous equation. The first one represents an almost ideal inductor, where just the magnetic field stored and the ohmic losses are considered. The last two terms on the right-hand side of 2.26 denote the substrate loss factor and self-resonant factor. On-chip inductors are normally built on a conductive Si substrate, and the substrate loss is due mainly to the capacitive and inductive coupling. The capacitive coupling, C_p (see Figure 2.5) from the metal layer to the substrate has two negative

consequences: changes the substrate potential and induces the displacement current. The inductive coupling is formed due to time-varying magnetic field penetrating the substrate and such a coupling induces the eddy current flow in the substrate. Both the displacement and currents give rise to the substrate loss and thereby degrade the inductor performance. An important conclusion we can take from the equation 2.26. If R_p approaches to infinity, the substrate loss factor approaches the unity. Since R_p approaches infinity when R_{si} goes to zero of infinity (see equation 2.21), the quality factor can be improved by making the silicon substrate either a short or a open [15].

A more expedite process to calculate Q could be achieved by measuring the input impedance of the circuit with one port grounded. The energy stored in the inductor, is linked to the imaginary part of the input impedance Z_{in}; whereas the real part of Z_{in} is proportional to the energy dissipated in resistances. With this approach, the equation 2.26 for the quality factor is reduced to

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})}. \tag{2.27}$$

2.4 Working Examples

In order to verify the accuracy of the model (π-model) described, simulations for inductor of 1, 2 and 3 nH were performed. The inductors were implemented using the top metal level of a 0.13 μm digital CMOS process. The technological parameters shown in Table 2.2 were used.

Table 2.2: UMC130 - Technological Parameters

Parameter	Value	Parameter	Value
ε_0	8.85e-12	t_{ox} (μm)	600
ε_r	1	C_{sub} (F/m^2)	4.0e-6
σ (Ωm)	1/2.65e-8	G_{sub}	2.43e5

For the metal spacing, a minimum space between tracks of 1.5 μm is always assumed.

In table 2.3 the dimensions of the inductors implemented are summarized. In this example a working frequency of 710 MHz was considered.

The validity of these results was checked against simulation with ASITIC (Analysis

Table 2.3: Spiral inductor design constraints

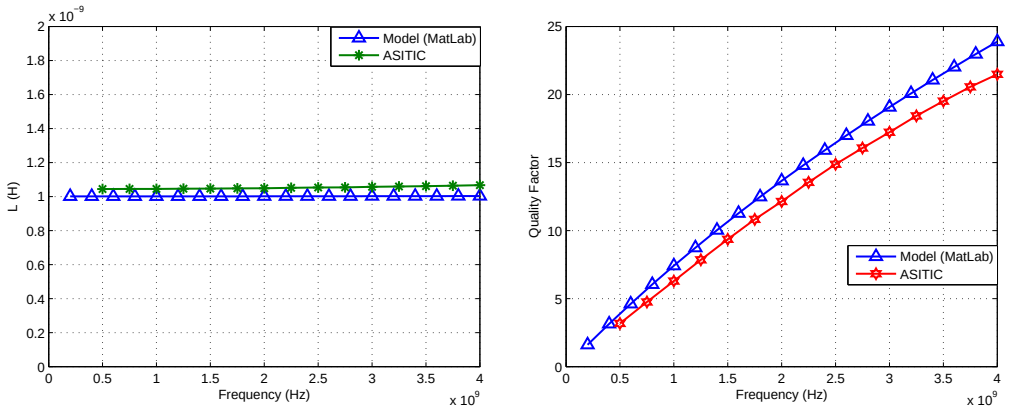
Inductor	w (μm)	d_{in} (μm)	n	d_{out} (μm)
1 nH	13.8	69.5	2.5	143
2 nH	14.5	137	2.5	214
3 nH	22.3	204	2.5	320

and Simulations of Spiral Inductors and Transformers for Integrated Circuits) yielding results shown in Table 2.4.

Table 2.4: Results comparison with ASITIC - 710 MHz

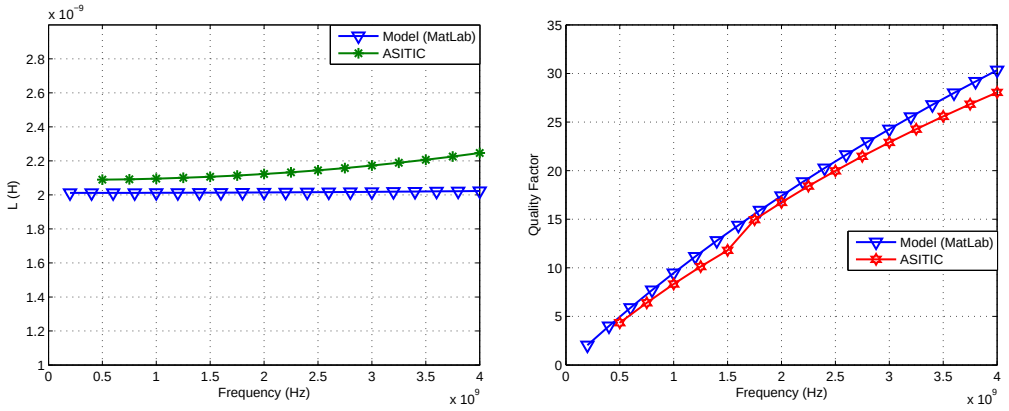
L			Q		
Model	ASITIC	ε_L (%)	Model	ASITIC	ε_Q (%)
1.00 nH	1.05 nH	4.5	5.38	4.63	13.9
2.00 nH	2.09 nH	4.6	6.89	6.23	6.23
3.00 nH	3.14 nH	4.8	10.5	9.35	11.0

Analyzing the results for these three working examples we observe close agreement between our formulas and the measured data from ASITIC, with a maximum relative error in order of 10 %. A major limitation in the design, modeling and simulation of spiral is the difference between our circuit model of the spirals inductor and the ASITIC. Then we can conclude that the results are quite acceptable to the chosen frequency of test. For the model to be more accurately validate it will be necessary to prove it to various frequencies. The figures 2.6, 2.7 and 2.8 shows the results of these three inductors for a range of frequencies and comparing likewise with ASITIC.



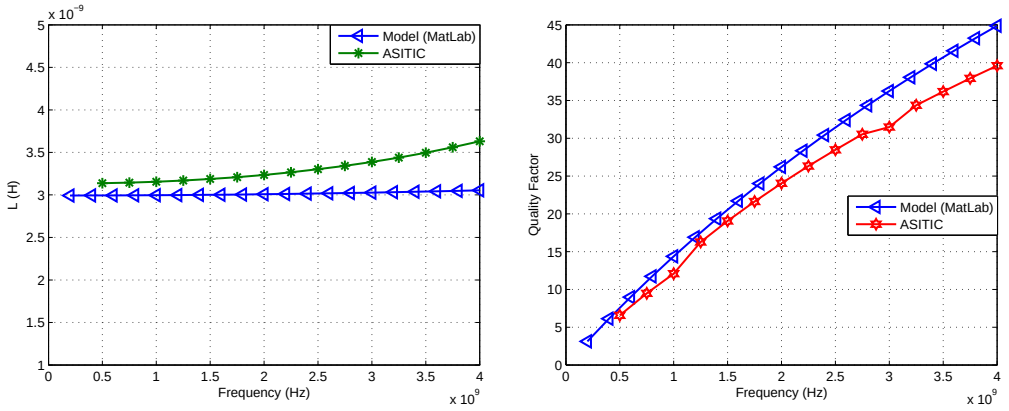
(a) (b)

Figure 2.6: Frequency dependence of 2.6(a) inductance and 2.6(b) the quality factor of spiral inductor



(a) (b)

Figure 2.7: Frequency dependence of 2.7(a) inductance and 2.7(b) the quality factor of spiral inductor



(a) (b)

Figure 2.8: Frequency dependence of 2.8(a) inductance and 2.8(b) the quality factor of spiral inductor

2.4.1 Conclusion

The figures reveals the excellent match between the values calculated and ASITIC. For high frequencies, the magnetic field effect seems to be a dominant factor. The Q increases with the frequency up to the peak value and then drops at higher frequencies due to the parasitic capacitance. Despite of this limitations we can conclude that the model we have achieved is quite adequate to be used.

Chapter 3

Integrated inductors with variable width

3.1 Introduction

The main goals for the design of an integrated inductors consist of:

- high quality factor (Q factor) in order to obtain low-power loss and high-storage energy inductor,
- self-resonance frequency well above the frequency of operation in order to guarantee minimum inductance,
- high inductance per unit area in order to obtain highly integrated efficiency,
- high robustness in order to minimize the process derivation [16]

In this work, we try to improve the spiral inductor's Q for frequency range behind the self-resonance frequency, which can be easily installed into present CMOS technology without a special process change. The degradation of the Q-factor of monolithic inductors was attributed to substrate and metal loss, especially for silicon based technology. Using highly resistive substrate and a high level metal layer can prevent substrate losses. The metal loss was attributed to Ohm loss and eddy-current loss. Technologies such as using copper metal, a thick metal layer, and a multilevel metal layer have been employed in order

to prevent the metal loss. One of the goal of this work is to reduce the series resistance R_s, arising from the resistivity of the metal, reducing the eddy current loss and consequently improving the Q factor. This is helpful for the design of low-power consumption and high-performance RFICs. So, a variable metal width of the spiral inductor was proposed. The basic idea is to increase the line width by arithmetic-progression.

Although this method can operate at low frequencies where the current density in a wire is uniform, as the frequency increases the skin effect pulls more current to the outer cross section of the metal wire and the so-called skin depth (i.e., the depth in which the current flows) is reduced with increasing frequency (see equation (2.8)). Thus, the skin effect increases the series resistance at high frequencies, and the approach of increasing the line width would not be effective. According to an earlier study, the larger the cross section, the lower the onset frequency at which the skin effect dominates the series resistance. Furthermore, a wider metal line would occupy more area, which increases the fabrication cost [17]. In this chapter we present one possible solution to this problem.

3.2 Variable width inductors

For a conventional spiral inductor with uniform metal width the influence of magnetically induces losses is much more important in the inner turn of the coil, where the magnetic field reaches its maximum. To avoid this effect, some authors proposed an optimization by maximizing the internal diameter [7],[17]. However this is not the best procedure to improve the quality factor of the integrated inductor, since increasing the inner diameter increases the occupied area which goes against one of the designers goals.

One method is to employ the so-called tapered inductor, in which the line width increases toward the outer turn of the spiral. In this way a reduced series resistance leads to an improve of the quality factor. In this work, square inductors, where each segment shows a width increment of Δw, as illustrated in figure 3.1, are considered.

Since each segment will show an increment of both width and length new equations will be proposed, relying on the dimensions of each segment of the inductor. The width of a segment may be evaluated with

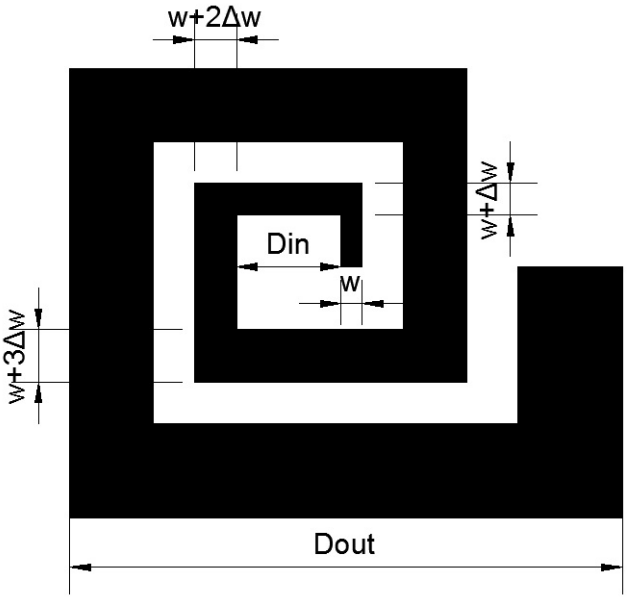


Figure 3.1: Variable width square inductor [2]

$$w_i = w + n_i \Delta w \tag{3.1}$$

where n_i is the number of the segment, and w is the initial metal width. So, the starting point for the derivation of our formulas is a common point with the precise analytical algorithm: decomposition of an inductor into segments as shown in figures 3.2 and 3.3.

Taking that into account that the basic structure for supporting all the inductor segments characterization is a matrix of four columns (one for each segment per turn) and n line (one per inductor turn). Initially, a matrix l_{ij} containing every segment length

$$l_{ij} = \begin{bmatrix} l_{11} & l_{12} & l_{13} & l_{14} \\ l_{21} & l_{22} & l_{23} & l_{24} \\ l_{31} & l_{32} & l_{33} & l_{34} \\ \vdots & \vdots & \vdots & \vdots \\ l_{n1} & l_{n2} & l_{n3} & l_{n4} \end{bmatrix} \tag{3.2}$$

and a matrix containing every segment width, w_{ij}

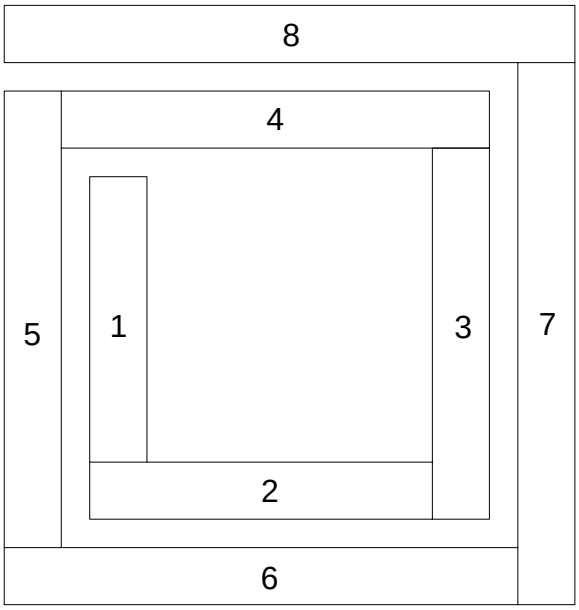


Figure 3.2: A regular spiral inductor divided by segments

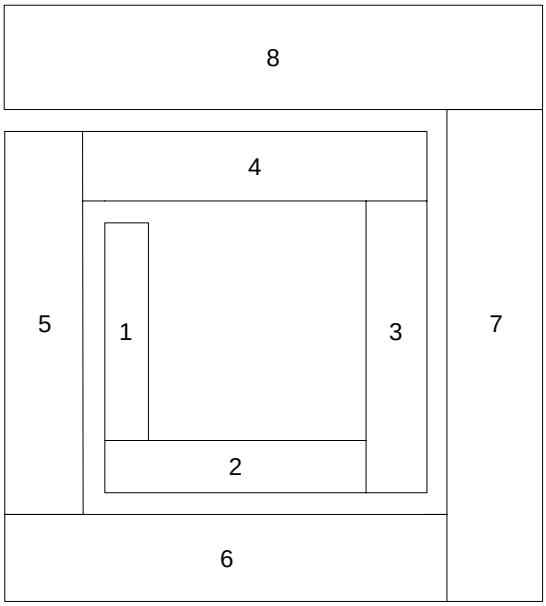


Figure 3.3: A non-uniform width spiral inductor divided by segments

$$w_{ij} = \begin{bmatrix} w_{11} & w_{12} & w_{13} & w_{14} \\ w_{21} & w_{22} & w_{23} & w_{24} \\ w_{31} & w_{32} & w_{33} & w_{34} \\ \vdots & \vdots & \vdots & \vdots \\ w_{n1} & w_{n2} & w_{n3} & w_{n4} \end{bmatrix} \tag{3.3}$$

are generated.

In chapter 2 we see that the model components of the integrated inductors are based on their geometrical parameters. So, given that these parameters are modified by the introduction of the increase in the metal width, new expressions for the π-model are needed.

3.2.1 Modeling variable inductors

For determining the analytical expressions for the calculation of the component values of the π-model is necessary to characterize the width, w_i, and the length, l_i for each segment of the spiral inductor. The new expression for each component are presented below, based upon the expressions used to model a regular inductor.

a) Series Inductance, L_S

Regarding the π-model inductance, L_s analytical equation 2.2.2 we see that a new way for evaluating d_{out} must be adopt because of the change in geometry parameters of the metal strip and expression, and it is given by

$$d_{out} = d_{in} + (2n+1)w + (2n-1)s + (2n(2n+1))\Delta w \tag{3.4}$$

But, at this point there is a easier way to calculate the d_{out} of the inductor. Considering the basic matrices in (3.2) and (3.3), the outer diameter is obtained by

$$d_{out} = l_{n3} + w_{n4} \tag{3.5}$$

where l_{n3} is the third segment's length and w_{n4} is the last segment's width of the last turn. The resulting equation of series inductance for a non-uniform inductor width takes the same form of the expression for a regular width spiral inductor, replacing the outer diameter. Thus

$$L_S = K_1 \mu_0 \frac{n^2 d_{avg}}{(1 + K_2 \rho)}. \tag{3.6}$$

where the average diameter (d_{avg}) depends on the new d_{out}.

b) Series Resistance, R_S

For the evaluation of the series resistance, R_S, is necessary to be more careful, since the maths inherent is a little more complex. As we see in 2.2.3 the expressions that are used to calculate R_S, 2.10 and 2.11, depends on the dimensions of the inductor.

For this purpose two new matrix (3.7) and (3.8) based on the matrices containing the lengths and widths of each segment are generated (3.2 and 3.3).

$$\frac{l_{ij}}{w_{ij}} = \begin{bmatrix} \frac{l_{11}}{w_{11}} & \frac{l_{12}}{w_{12}} & \frac{l_{13}}{w_{13}} & \frac{l_{14}}{w_{14}} \\ \frac{l_{21}}{w_{21}} & \frac{l_{22}}{w_{22}} & \frac{l_{23}}{w_{23}} & \frac{l_{24}}{w_{24}} \\ \frac{l_{31}}{w_{31}} & \frac{l_{32}}{w_{32}} & \frac{l_{33}}{w_{33}} & \frac{l_{34}}{w_{34}} \\ \vdots & \vdots & \vdots & \vdots \\ \frac{l_{n1}}{w_{n1}} & \frac{l_{n2}}{w_{n2}} & \frac{l_{n3}}{w_{n3}} & \frac{l_{n4}}{w_{n4}} \end{bmatrix} \tag{3.7}$$

$$\frac{l_{ij}}{w_{ij}+t} = \begin{bmatrix} \frac{l_{11}}{w_{11}+t} & \frac{l_{12}}{w_{12}+t} & \frac{l_{13}}{w_{13}+t} & \frac{l_{14}}{w_{14}+t} \\ \frac{l_{21}}{w_{21}+t} & \frac{l_{22}}{w_{22}+t} & \frac{l_{23}}{w_{23}+t} & \frac{l_{24}}{w_{24}+t} \\ \frac{l_{31}}{w_{31}+t} & \frac{l_{32}}{w_{32}+t} & \frac{l_{33}}{w_{33}+t} & \frac{l_{34}}{w_{34}+t} \\ \vdots & \vdots & \vdots & \vdots \\ \frac{l_{n1}}{w_{n1}+t} & \frac{l_{n2}}{w_{n2}+t} & \frac{l_{n3}}{w_{n3}+t} & \frac{l_{n4}}{w_{n4}+t} \end{bmatrix} \tag{3.8}$$

Following our line of thinking, the resultant series resistance is a sum of the resistance of all segments in particular. In other words, each segment will have a different resistance because of their different dimensions. Thus,

$$R_{dc} = \frac{1}{\sigma t} \sum_{i=1}^{n} \sum_{j=1}^{4} \frac{l_{ij}}{w_{ij}} \tag{3.9a}$$

$$R_{ac} = \frac{k}{2\sigma\delta} \sum_{i=1}^{n} \sum_{j=1}^{4} \frac{l_{ij}}{w_{ij}+t} \tag{3.9b}$$

c) Crossover Capacitance, C_S

As we discussed in 2.2.4 the crossover capacitance, C_S, connect the inner turn to

the outside of the spiral inductor. As the width of the metal strip is increased for each segment, the final metal width is larger than the initial one. The capacity is formed by two plates with different areas. Assuming that the plates are relatively close that there is low leakage flux, the capacitance is formed by the lower plate area. Thus, only the initial width of the metal is considered and this element can be calculated by,

$$C_S = n_c w^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{3.10}$$

d) Oxide Capacitance, C_{ox}

As already discussed in 2.2.5 this capacity is formed between the metal strip and the silicon substrate. Analyzing the expression we see that this component also depends on the dimensions of each segment of the coil. Picturing the 3d-image of the spiral inductor and keeping in mind that we are considering a π-model for each segment we came to the conclusion that the oxide capacitances of all the segments are in parallel. So the total *Cox* is the sum of them all and is given by,

$$C_{ox} = \frac{1}{2} \frac{\varepsilon_{ox}}{t_{ox}} \sum_{i=1}^{n} \sum_{j=1}^{4} l_{ij} w_{ij}. \tag{3.11}$$

e) Substrate Capacitance, C_{si} and Resistance, R_{si}

The mindset for the evaluation of the new expressions of substrate resistance and capacitance is similar. From the sectional view we can see that the substrate capacitances of all segments of the inductor are in parallel resulting in the total substrate capacitance,

$$C_{si} = \frac{1}{2} C_{sub} \sum_{i=1}^{n} \sum_{j=1}^{4} l_{ij} w_{ij}. \tag{3.12}$$

For the substrate resistance, the only different is in the parallel of resistances. But treating these as conductances, we can sum them and invert the result. Thus,

$$R_{si} = \frac{2}{G_{sub}} \sum_{i=1}^{n} \sum_{j=1}^{4} \frac{1}{l_{ij} w_{ij}}. \tag{3.13}$$

In section 3.3 a validation of the proposed model by comparasion with ASITIC is performed.

3.3 Validation of the model

To prove the validity of the proposed model was carried out the following test. Maintaining constant the geometric parameters of the Table 3.1 and varying the increment value of width (Δw) the results shown in Table 3.2 were obtained.

Table 3.1: Validity of the optimization model

w (μm)	d_{in} (μm)	n
10.5	134	2.5

Table 3.2: Results comparison with ASITIC

Inductor	Δw (μm)	d_{out} (μm)	L			Q		
			Model	ASITIC	ε_L (%)	Model	ASITIC	ε_Q (%)
1	0.0	191	2.01	2.14	6.5	16.30	15	8.0
2	0.1	194	2.01	2.07	2.9	16.91	17.7	4.7
3	0.25	199	2.00	2.07	3.5	17.71	18.21	2.8
4	0.5	205	1.98	2.04	3.1	18.95	19.32	1.9
5	1.0	220	1.96	2.04	4.3	21.19	20.87	1.5
6	2.5	257	1.93	1.97	2.0	26.85	23.33	13.1

By the results in Table 3.2 it is quickly to realize that the quality factor increases with the variation of the width (Δw) and hence the total area of the inductor. Note also a maximum relative error of around 10% in value compared with ASITIC, from which we can conclude that our model is a valid layout optimization. In Table 3.3 a ratio between the increase of the area occupied by the integrated inductor and the increase of the quality factor is presented.

Table 3.3: Validity of the optimization model

Inductor	Increased Area (%)	Improvement Q (%)	Imp.Q/Inc.Area
2	1.8	3.6	2
3	4.3	7.9	1.84
4	7.1	14.0	1.97
5	13.4	23.1	1.73
6	25.9	39.3	1.52

These results are particularly interesting because we can see a greater increase in the

quality factor in relation to the occupied area. Following this line of reasoning is to be expected that we can get a higher quality factor for the same area using variable metal width spiral inductors.

3.4 Optimization

In order to confirm this theory, a set of square spiral inductors has been designed using an optimization based tool for the automatic design of spiral inductors [18]. The efficiency of the tool is accomplished by the inductor π-model. The proposed tool offers the designer the possibility for obtaining the layout parameters for the desired inductance value. The solution is obtained considering constraints in the design variables which are defined by the designer (see Table 3.4).

Table 3.4: Spiral inductor design constraints

Parameter	Min	Step	Max
w (μm)	5.0	0.5	100.0
Δw (μm)	1	0.25	-
s (μm)	1.5	-	-
d_{in} (μm)	20.0	0.5	200.0
n	1.5	0.5	15.5
d_{out}	-	-	700

These constraints consider not only upper/lower bounds on the variable values, but also a discretization of the values according to the technology. The technological parameters shown in Table 3.5 were used.

Table 3.5: UMC130 - Technological Parameters

Parameter	Value	Parameter	Value
ε_0	8.85e-12	t_{ox} (μm)	600
ε_r	1	C_{sub} (F/m^2)	4.0e-6
σ (Ωm)	1/2.65e-8	G_{sub}	2.43e5

The designer may also choose which performance parameter is to be optimized, such as maximizing the quality factor, Q, at a predefined operation frequency, or the minimization of the area occupied. This tool was developed in Matlab [19] and the validity of the solution obtained was checked against results from simulation with ASITIC simulator.

For the model validation a comparison between results obtained with variable width

design fixed width designs, for a approximately equal area, is presented. A set of examples for a spiral inductors at a working frequency of 2.44 GHz was considered.

3.4.1 Example 1

In this example a spiral inductor of 1 nH was considered. The spiral inductor constraints design obtained for a fixed width layout as well as for Δw of 1.5 μm are represented in Table 2.3. In the Table 3.7, the simulation results obtained with ASITIC for each case are represented.

Table 3.6: Spiral inductor design constraints for inductance of 1nH

Inductor	w (μm)	d_{in} (μm)	n	d_{out} (μm)	Δw (μm)
1	13.0	69	2.5	153	0.0
2	5.75	42.3	3	153	1.5

Table 3.7: Results comparison with ASITIC

Inductor	L			Q			Improvement (%)
	Model	ASITIC	ε_L (%)	Model	ASITIC	ε_Q (%)	
1	1.00	1.06	7	6.86	6.04	12	
2	1.01	1.03	2	8.13	7.76	5	18

In the last columns the relative improvement in the quality factor from using incremental width is given.

3.4.2 Example 2

In this example a spiral inductor of 2 nH was considered. The spiral inductor constraints design obtained for a fixed width layout as well as for Δw of 0.5, 0.75, 1 and 2 μm are represented in Table 3.8. In the Table 3.9, the simulation results obtained with ASITIC for each case are represented.

Table 3.8: Spiral inductor design constraints for inductance of 2 nH

Inductor	w (μm)	d_{in} (μm)	n	d_{out} (μm)	Δw (μm)
1	10.5	134	2.5	191	0.0
2	10.0	97	3.0	190	0.75
3	11.8	67.8	3.5	182	0.5
4	5.75	96.3	3.0	173	1.0
5	4.50	96.3	3.0	201	2.0

Table 3.9: Results comparison with ASITIC

Inductor	L			Q			Improvement (%)
	Model	ASITIC	ε_L (%)	Model	ASITIC	ε_Q (%)	
1	2.00	2.14	6.5	16.3	15.0	8.0	
2	2.01	1.92	4.6	21.3	20.4	4.2	24
3	2.00	1.91	4.6	22.4	21.3	4.8	27
4	2.00	1.90	4.8	17.7	17.5	1.0	8
5	2.00	1.86	7.0	20.7	19.2	7.7	21

In the last columns the relative improvement in the quality factor from using incremental width is given.

3.4.3 Conclusion

The validity of the model was shown through two working examples considering the design of 1.0nH and 2.0nH inductors at a working frequency of 2.44 GHz. From the examples presented a quality factor improvement in the order of 10% to 30% may be obtained, by using variable width for the same chip area.

Chapter 4

An RF LC Q-Enhanced CMOS filter

4.1 Introduction

Surface acoustic wave (SAW) filters are applied extensively in today's communication equipment. These high performance components have reached a key position in current communication technology assisting the efforts to increase the spectral efficiency of limited frequency bands for higher bit rates. During the last decades, driven by the boom of the wireless technology business, great and important progress in SAW device performance was made, and a variety of innovative applications were developed. The developments are based on technological improvements. The reduced size and weight of the complete system will be an advantage in all kinds of portable electronic products. Moreover, receiver architectures in telecommunication systems use higher IF frequencies to improve the interfering signal rejection. The allocations of radio frequency spectrum has led to the development of small and low-cost wireless products. The commercial sector has responded with increasing levels of integration. Researchers have attempted to design high Q bandpass filters by enhancing lossy integrated inductors. Shunt mounted resonator, composed of an inductor and capacitor in parallel is presented to realize RF bandpass filter. The design of the integrated on-chip 1.2V 2.44 GHz Q-enhanced LC filter using silicon CMOS process is presented in this chapter.

4.2 Tuned Amplifiers

Highly selective bandpass filters have long been implemented with tuned amplifiers. In figure 4.1 the amplitude response of a tuned amplifier is represented, which may be characterized by the central frequency, ω_0, and the 3-dB bandwidth, B. In many applications, the 3-dB bandwidth is less than 5% of ω_0 [20]

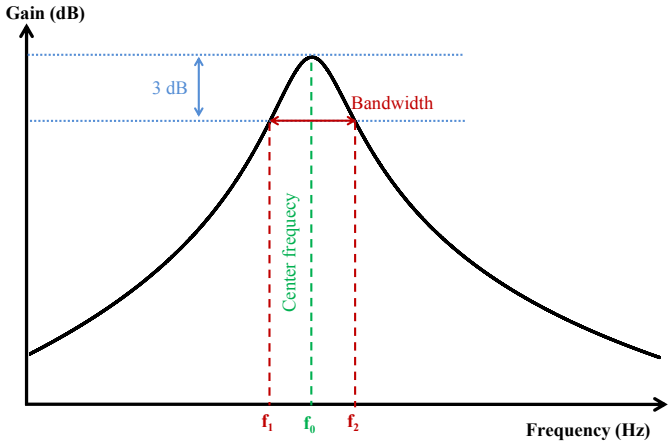


Figure 4.1: Frequency response of a tuned amplifier

The basic principle in the design of tuned amplifiers is the use of parallel RLC circuit as the load, or at the input, of a BJT or a FET amplifier. In figure 4.2 a MOSFET class A amplifier, having a tuned-circuit load is illustrated. For the sake of simplicity, the bias details are not included. Since this circuit uses a single tuned circuit, it is known as a single-tuned amplifier [20].

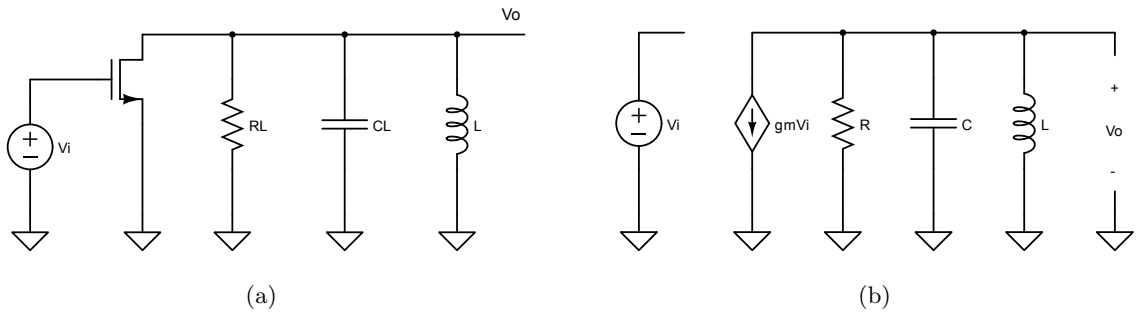


Figure 4.2: The basic principle of tuned amplifier is illustrated using a MOSFET with a tuned circuit load. Bias details are not shown.

The amplifier small signal equivalent circuit is represented in figure 4.2 where R de-

notes the parallel equivalent of R_L and the MOSFET output resistance r_o, and C is the parallel equivalent of C_L and the FET output capacitance (usually very small). From the equivalent circuit we may write,

$$V_o = -\frac{g_m V_i}{Y_L} = -\frac{g_m V_i}{sC + \frac{1}{R} + \frac{1}{sL}} \tag{4.1}$$

The voltage gain is a second-order bandpass function and can be expressed as

$$\frac{V_o}{V_i} = -\frac{gm}{C}\frac{s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{4.2}$$

We may thus conclude that the tuned amplifier has a center frequency of

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.3}$$

a 3-dB bandwidth of

$$B = \frac{1}{RC} \tag{4.4}$$

a quality factor of

$$Q \equiv \frac{\omega_0}{B} = \omega_0 RC \tag{4.5}$$

and a center-frequency gain of

$$\frac{V_o(j\omega_0)}{V_i(j\omega_0)} = -\frac{g_m}{C}\frac{j\omega_0}{(j\omega_0)^2 + Bj\omega_0 + \omega_0^2} = -\frac{g_m}{C}\frac{j\omega_0}{(-\omega_0)^2 + Bj\omega_0 + \omega_0^2} = -g_m R \tag{4.6}$$

In the case of wireless transmitters it is necessary to implement filters of very high selectivity. In these cases LC filters may be employed. The use of integrated inductors in CMOS technology raises problems for the implementation of high selectivity LC filters selectivity due to the difficulty of designing coils with high quality factor operating at RF frequencies. For wireless applications fully integrated highly selective bandpass filters are needed with quality factor in the order of 30. In this cases a Q-enhanced LC topology

must be adopted. In the next section a brief description of a Q-enhancement technique using a negative active resistance g_m will be presented.

4.3 Principles of Q enhancement

Q enhancement has long been used in LC circuits for signal amplification, signal selection and for generating stable oscillation [21]. In this section, our discussion is focused on the Q-enhancement in integrated LC filters. If a high selectivity LC resonator is desired some form of Q-enhancement is needed to increase the quality factor of resonators designed with lossy on-chip resonator.

Regardless of the coupling mechanism between the resonators, losses associated with the on-chip reactive components change the center frequency and the loaded quality factor of the filter. Having estimated and modeled the total resistive loss of the resonator, a active device to create a negative resistance, ($-1/G_{neg}$), exactly the opposite caused by the losses of reactive components can be added to compensate its effect as shown in figure 4.3.

Although methods that include phase-shifted current feedback via coupled inductors have been investigated, the direct use of active devices as negative resistors is the prevalent Q-enhancement technique [3]. This way, combining the reactive component with a negative resistance, the real part of the total impedance is reduced, eliminated or even made negative, depending on the value of the negative resistance used. We can say that the quality factor of the original lossy component can be improved (enhanced) by the negative resistance and resulting component can replace the original used in the LC filter.

This Q-enhancement technique is shown in figure 4.4.

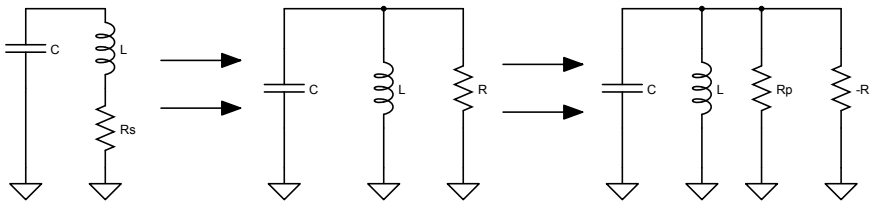


Figure 4.3: Active Q-enhancement using negative resistance

Assuming that a lossy inductor with a quality factor of Q_0 can be simplistically modelled (4.3) by an inductor L with an series resistance R_S, we may consider,

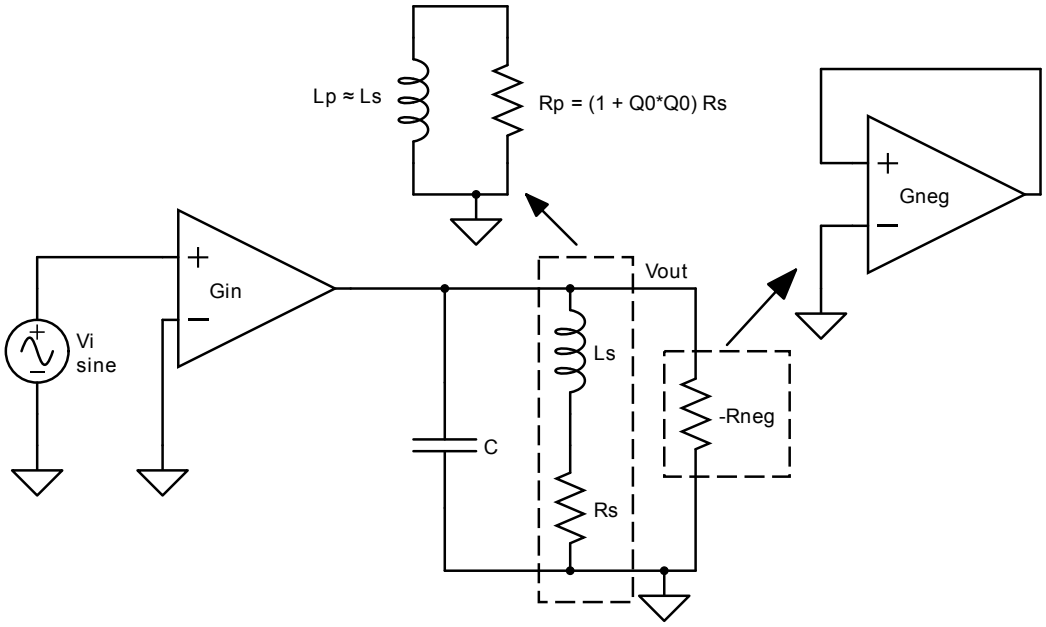


Figure 4.4: Q-enhancement technique applied to a RLC filter

$$R_S = \frac{\omega L}{Q_0} \tag{4.7}$$

These losses can be compensated by connecting the negative resistance in parallel with the LC tank. Assuming that the quality factor of the tank capacitance is much larger than the inductor, the series combination of the inductor (L_S) and its loss R_S can be modeled as a parallel combination of an inductance L_P and resistance R_P given by

$$L_P = L_S(1 + \frac{1}{Q_0^2}) \approx L_S = \omega L Q_0 \tag{4.8}$$

and

$$R_P = R_S(1 + Q_0^2) = \omega L Q_0 \tag{4.9}$$

If the inductor quality factor Q_0 is large enough then, $L_P \cong L$. The frequency response of the filter in the figure 4.5 can be approximated as

$$H(s) = \frac{V_o(s)}{V_{in}(s)} \cong \frac{G_m}{G_P - G_{neg} + \frac{1}{sL_P} + sC} \tag{4.10}$$

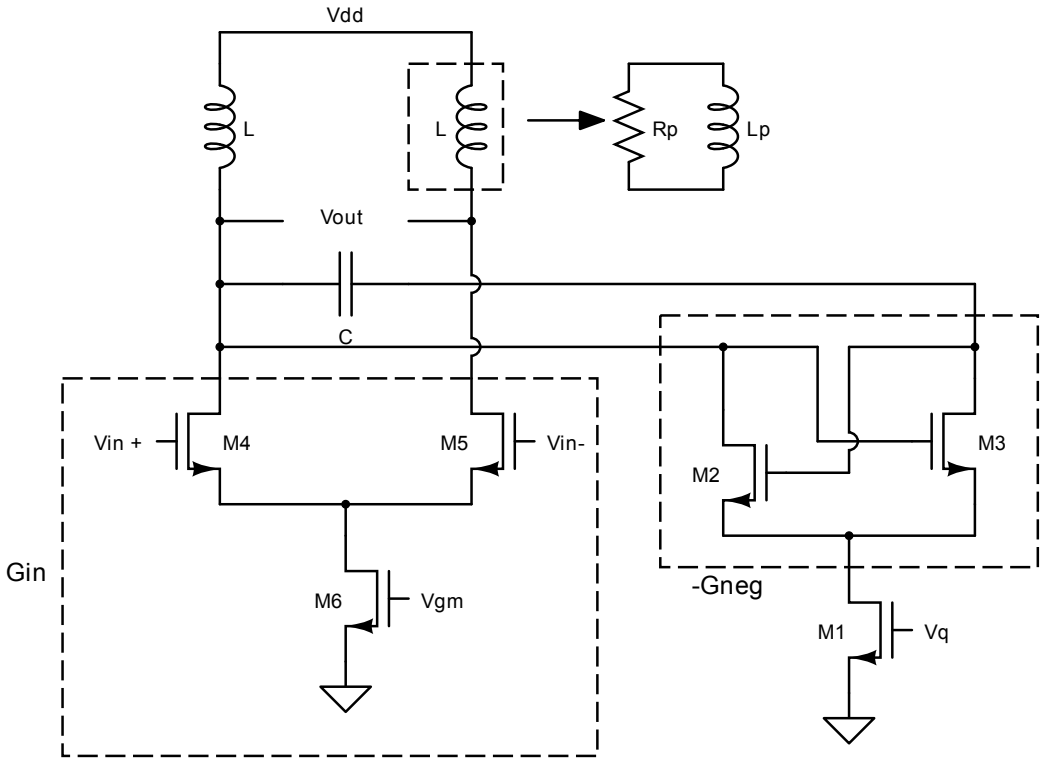


Figure 4.5: Q-enhanced LC bandpass filter

or

$$H(s) = \frac{V_o(s)}{V_{in}(s)} \cong \frac{\frac{-G_m}{C}s}{s^2 + \frac{G_P - G_{neg}}{C} + \frac{1}{LC}} = \frac{-A_0\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.11}$$

From which we may conclude that the central frequency will be given by

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.12}$$

Also from equation 4.11 we may conclude that the filter quality factor will be given by

$$Q = \frac{C\frac{1}{\sqrt{LC}}}{G_P - G_{neg}} = \frac{\sqrt{\frac{C}{L}}}{(G_P - G_{neg})} \tag{4.13}$$

The filter central gain, A_0 will be given by

$$A_0 = \frac{G_m}{C}\frac{Q}{\omega_0} = \frac{G_m}{G_P - G_{neg}} \tag{4.14}$$

and the bandwidth, B can be described as:

$$B = \frac{\omega_0}{Q} = \frac{\sqrt{\frac{1}{LC}}(G_P - G_{neg})}{\sqrt{\frac{C}{L}}} \tag{4.15}$$

As 4.12 shows, the quality factor of the inductor (Q_0) does not modify the center frequency but increases the Q of the resonator. Thus at high frequencies, due to the higher losses, a larger G_{neg} is required which results in changing both Q. Note that the equation 4.13 is valid only around the LC tank's resonant frequency, due to the fact that the equivalent parallel conductance from the inductor loss varies with frequency.

Considering the circuit implementation of a second-order Q-enhanced LC filter in 4.5, the center frequency tuning is achieved through varactors which are PMOS transistors implemented in separate wells (in an n-well technology) and with their drain/source terminals connected together to the well terminal. The capacitance seen by the gate is adjusted by changing the voltage V_f and exploiting the variation of the gate capacitance when the transistor goes from weak inversion to the accumulation region.

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. In the saturation or active mode the switch is turned on when $V_{gs} > V_T$ and $V_{gs} > V_{ds} - V_T$ and a channel is created which allows current to flow between the drain and the source. The drain current is weakly dependent upon drain voltage and controlled primarily by the gate-source voltage, and modeled approximately as:

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_T)^2 \tag{4.16}$$

A key design parameter, the MOSFET transconductance g_m is:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}}\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_T)^2\right) = \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_T) \tag{4.17}$$

The cross coupled transistor M_2-M_3 form the negative transconductance -G_{neg} which based on equation 4.13 changes the quality factor of the filter. The transconductance G_{neg}

is dependent on the control voltage, V_q. Considering that the transistors M_2 and M_3 are equal, we know that,

$$\begin{aligned} I_{D_{2,3}} = \frac{1}{2} I_{D_1} \Leftrightarrow & \\ & \Leftrightarrow \quad \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{2,3}(V_{gs}-V_T)^2 = \frac{1}{2}\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_q - V_T)^2 \\ & \Leftrightarrow \quad (V_q - V_T)^2 = \frac{1}{2}\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{2,3}}(V_q - V_T)^2 \end{aligned} \tag{4.18}$$

Using the equation 4.16 results in,

$$G_{neg} = \mu_n C_{ox}\sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_1\left(\frac{W}{L}\right)_{2,3}}(V_q - V_T) \tag{4.19}$$

where $(W/L)_{2,3}$ and $(W/L)_1$ refer to the (W/L) ratios of $M_{2,3}$ and M_1 in figure 4.5, respectively. To simplify the formulas we consider that

$$\beta_q = 0.5\mu C_{ox}\sqrt{0.5\left(\frac{W}{L}\right)_{2,3}\left(\frac{W}{L}\right)_1} \tag{4.20}$$

so,

$$G_{neg} = \beta_q(V_q - V_T) \tag{4.21}$$

Following the same reasoning, the control voltage V_{gm} changes the transconductance G_m of the input differential pair M_4-M_5 thus, changing the peak amplitude gain A_0 of the filter while keeping the Q invariant. Note that G_m as a function of V_{gm} can be expressed as

$$G_m = \beta_m(V_{gm} - V_T) \tag{4.22}$$

where

$$\beta_m = 0.5\mu C_{ox}\sqrt{0.5\left(\frac{W}{L}\right)_{4,5}\left(\frac{W}{L}\right)_6} \tag{4.23}$$

and $(W/L)_{4,5}$ and $(W/L)_6$ refer to the (W/L) ratios of $M_{4,5}$ and M_6 in figure 4.5, respec-

tively.

Thus using 4.19 and 4.22 the peak amplitude gain A_0 defined in equation 4.10, can be expressed as,

$$A_0 = \frac{G_m}{G_P - G_{neg}} = \frac{2\beta_m(V_{gm} - V_T)}{G_P - \beta_q(V_q - V_T)}. \tag{4.24}$$

In similar way the quality factor Q can be expressed as,

$$Q = \frac{\sqrt{\frac{C}{L}}}{G_P - \beta_q(V_q - V_T)}. \tag{4.25}$$

4.4 Integrated Filters design

Like analog circuit in general, radio-frequency integrated circuit (RFIC) designs suffer from required trade-offs that include linearity, noise, power, frequency, gain and supply voltage [1].

The circuit design investigated in this work introduces a loss-compensated second-order RF filter that is to be implemented in a standard 0.13μm CMOS process. This filter uses an on-chip resonant tank comprised of an spiral integrated inductor and a capacitance that is a combination of the1 circuit parasitics as well as specifically incorporated passive elements. Loss compensation is achieved by using a transconductor that emulates negative resistance. This particular topology is a circuit solution for the Q-enhancement as explained in the section 4.3.

An operational objective of this work is to implement a Q-enhanced LC filter with center frequency of 2.44 GHz and 3-dB bandwidth of 84 MHz and a maximum gain of 15 dB. One of the trade-offs suffered when incorporating active on-chip filters to replace the passive off-chip counterparts is in the required power consumption. In wireless devices circuit topologies that maximize the time of operation are a primary concern.

This section provide details regarding the Q-enhanced LC filter including circuit operational characteristic, design methodology, physical layout considerations and simulation results.

Components values for the inductors and capacitors of the resonant tank were chosen

to realize the specifications of the filter. In this case, we have,

$$\omega_0 = 2\pi \cdot 2.44 \cdot 10^9 = 1.5331 \cdot 10^{10} rad/s \tag{4.26}$$

and

$$B = 2\pi \cdot 84 \cdot 10^6 rad/s \tag{4.27}$$

In order to prove the advantage of using optimized integrated spiral inductors two designs of the LC filter were performed. So, a comparison between the non-optimized (fixed width) and the optimized integrated inductor (variable width) is performed. An inductor of 1 nH was considered to implement this filter since it is a reasonable value for the envisaged central frequency. In table 4.1 the layout dimensions as well as the values of the inductance and resistance of the inductors used to implement the filter is presented.

Table 4.1: Inductor of 1 nH used in filter

w (μm)	d_{in} (μm)	n	d_{out} (μm)	Δw (μm)	L(nH)	R(Ω)	Q
7.75	68.8	2.5	112	0.0	1.00	1.4	11.0
5.5	47.5	3.0	114	0.75	1.00	1.133	13.55

Its possible to size the values of the transconductance, G_{neg}, and of the capacitance solving the following system of equations given by 4.12 and 4.15. Thus,

$$\begin{cases} \omega_0 = \sqrt{\frac{1}{LC}} \\ B = \frac{G_P - G_{neg}}{C} \end{cases} \tag{4.28}$$

results in

Table 4.2: Values of the G_{neg} and C

	Regular inductor	Optimized inductor
G_{neg} (mS)	3.7	2.6
C (pF)	4.25	4.25

In order to obtain this values of the G_{neg} we have to size the dimensions of the transistor MOS. By equation 4.19 demonstrated in the previous section we have that,

$$G_{neg} = \mu C_{ox} \sqrt{0.5 \left(\frac{W}{L}\right)_1 \left(\frac{W}{L}\right)_{2,3}} (V_q - V_T) \tag{4.29}$$

To simplify the sizing of transistors to obtain the desired G_{neg}, it was decided to design the three transistors with the same size and $L = L_1 = L_2 = L_3 = 600$ μm since the length should be greater than three times the minimum allowed by the technology ($3 \times 130\mu$m). Substituting in the above equation, the width of transistor MOS in order to obtain the value of the G_{neg} is given by,

$$W = \frac{G_{neg} L}{\mu_n C_{ox} \sqrt{0.5} (V_q - V_T)} \tag{4.30}$$

For the technological parameters we have considered $\mu_n C_{ox}$ equals to $309 \cdot 10^{-6}$ μm and a V_T is 0.27 V. These values were obtained from simulations in Cadence. The value of V_q is 0.8 V as a way of having the transistors working in moderate inversion. Given that we are now able to determine the exact value for the width of the transistor. The table 4.3 shows the value of the W for both regular and optimized inductor.

Table 4.3: Value of the Width of the transistors MOS

	Regular inductor	Optimized inductor
MOS Width (μm)	18.7	13.14

Now we must design the size of the transistors M_4, M_5 and M_6 in order to obtain the desired gain, A_0. Assuming we want a gain of 15dB, by equation 4.24 we know that,

$$G_m = (G_p - G_{neg}) A_0 \tag{4.31}$$

In the previous section we demonstrated in equation 4.22 that,

$$G_m = \mu_n C_{ox} \sqrt{0.5 \left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{4,5}} (V_{gm} - V_T) \tag{4.32}$$

Again, to simplify the sizing of transistors to obtain the desired g_m, it was decided to design the three transistors with the same size and $L = L_4 = L_5 = L_6 = 600$ μm, μC_{ox}

equals to $309 \cdot 10^{-6}$, V_T is 0.27 V and V_{gm} is 0.8 V.

Substituting in the above equation, the width of transistor MOS in order to obtain the value of the G_{neg} is given by,

$$W = \frac{g_m L}{\mu_n C_{ox} \sqrt{0.5}(V_{gm} - V_T)} \tag{4.33}$$

The table 4.3 shows the value of the W extracted from equation 4.33 for both regular and optimized inductor.

Table 4.4: Value of the Width of the transistors MOS (4,5,6)

	Regular inductor	Optimized inductor
G_m (mS)	12.1	12.3
MOS Width (μm)	62.8	63.6

To verify the design of the Q-enhanced RF bandpass filter, the filter was simulated in a UMC130 standard CMOS process using the Cadence design environment.

4.4.1 Simulation results

In this section the results of the simulations, namely the passband response are presented. Two implementations of the filter were performed. The first implementation using a regular integrated inductor, ie, with fixed width. In the second implementation an optimized integrated inductor with non-uniform metal width was used proving that the filter maintain the good performance with this type of inductor.

As illustrated in figure 4.6, for the simulation of the inductor the corresponding pi-model was used. As previously explained, the value of the π-model resistance R_S is frequency dependent. Yet, since we are considering its inclusion in a highly selective filter, using a fixed R_S value obtained for the center frequency is a good approach.

4.4.2 g_mLC filter with regular integrated inductor

The figure 4.6 shows the schematic of a second order Q-enhanced LC filter using a regular integrated inductor. Using the input values of the table 4.1 presented in the previous section for the case of Δw= 0 we obtained the following values of the model-π components.

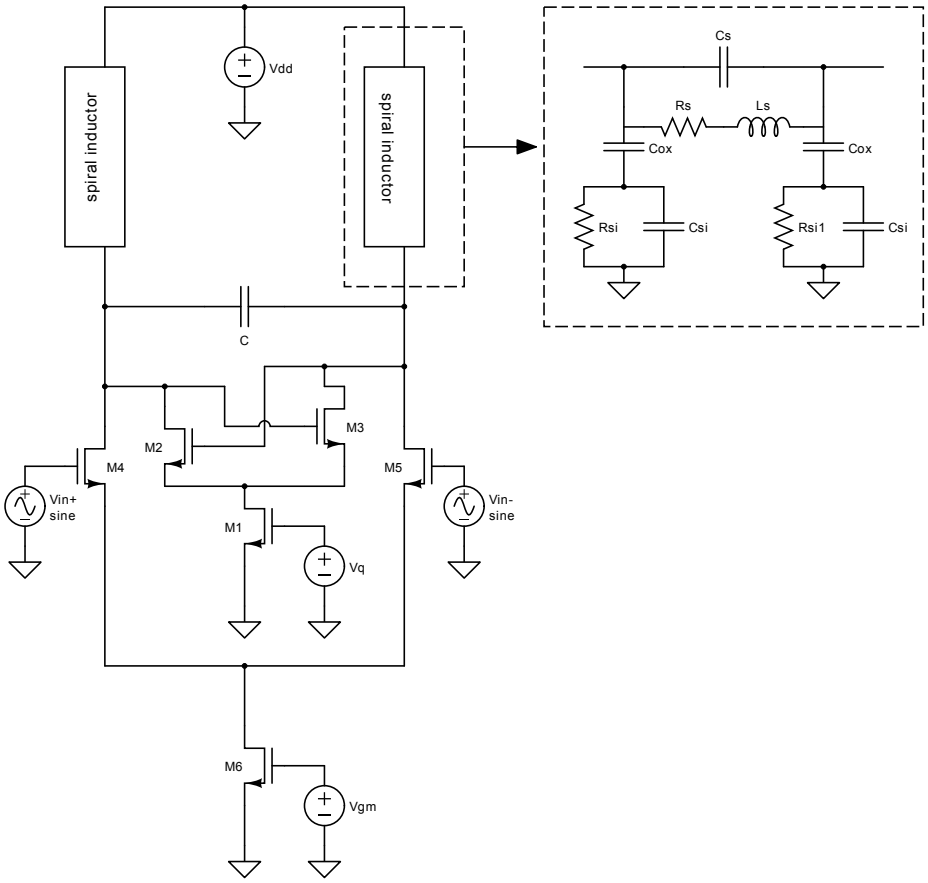


Figure 4.6: A 2^{nd} Q-enhanced on-chip LC bandpass filter

Table 4.5: Model π components values

L_S (H)	R_S (Ω)	C_S (F)	C_{ox} (F)	C_{si} (F)	R_{si} (Ω)
1e-9	1.4	0.751e-15	22.8e-15	0.526e-15	5.61e8

The filter passband response measurements performed using AC analysis in the Cadence simulator is shown in figure 4.7.

The measured gain of 12.65 dB at the center frequency of 2.405 GHz is lower than the originally designed filter gain in approximately 2.5 dB. Figure 4.7 also illustrates that the filter center frequency is shifted slightly lower than the required f_0 of 2.44 GHz specified for the targeted Bluetooth application, falling within 1.43% of the design goal. The table 4.6 compares the predicted and the simulated results.

Analysing the results presented in the table 4.6 it could be concluded that the method used to design the filter is quite acceptable since the results are close to the desired results.

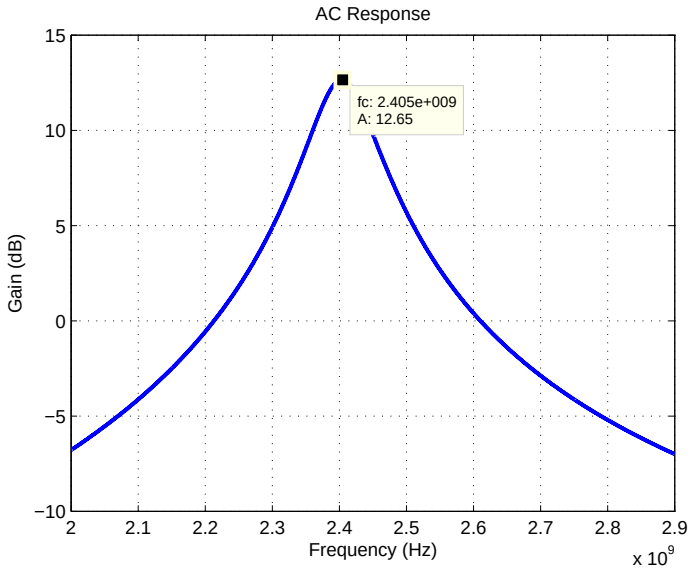


Figure 4.7: Frequency response of the RF LC Q-enhanced filter using a regular spiral inductor

Table 4.6: Simulation results

	Targeted values	Achieved values	$\varepsilon_r(\%)$
G_{neg} (mS)	3.7	3.87	4.59
G_m (mS)	12.1	11.14	7.93
f_c (GHz)	2.44	2.405	1.43
BW (MHz)	84	90	7.14
Quality factor	29	26.72	8
Output Gain (dB)	15	12.65	15.67

The largest relative error was obtained in the output gain of approximately 16%. This errors were already expected since the parasitic capacities of the transistors are not taken into account and the quadratic model of MOS transistors is not the most appropriate for the technology used.

4.4.3 g_mLC filter with optimized integrated inductor

For the implementation of the second order Q-enhanced LC filter using a optimized integrated inductor studied in chapter 3 the filter design used was the same (see figure 4.6, but now using the input values of the table 4.1 for the case of Δw= 0.75. The table 4.7 shows the value of the model-π components obtained.

The frequency response of the filter is shown in figure 4.8.

The measured gain of 13.07 dB at the center frequency of 2.417 GHz is lower than the

Table 4.7: Model π components values

L_S (H)	R_S (Ω)	C_S (F)	C_{ox} (F)	C_{si} (F)	R_{si} (Ω)
1e-9	1.13	0.504e-15	30.1e-15	0.691e-15	4.28e8

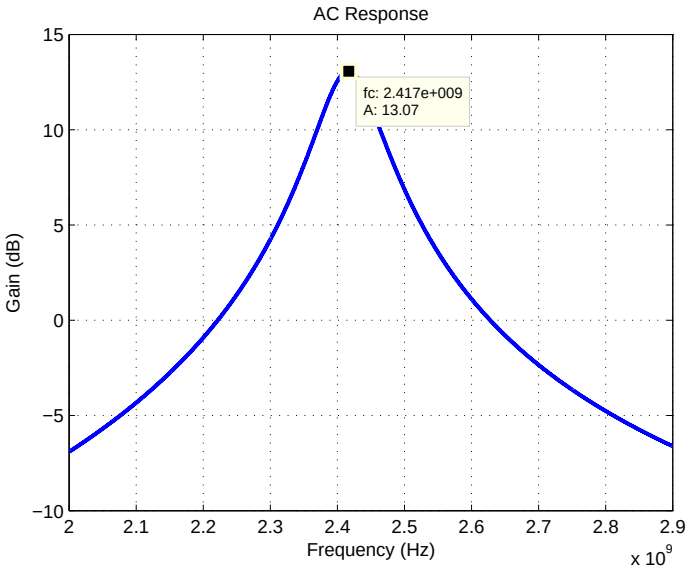


Figure 4.8: Frequency response of the RF LC Q-enhanced filter using an optimized spiral inductor

originally designed filter gain of approximately 2 dB. Figure 4.7 also illustrates that the filter center frequency is shifted slightly lower than the required f_0 of 2.44 GHz specified for the targeted Bluetooth application, falling within 0.94% of the design goal.

The table 4.8 compares the predicted and the simulated results

Table 4.8: Simulation results

	Targeted values	Achieved values	$\varepsilon_r(\%)$
G_{neg} (mS)	2.6	2.72	4.62
G_m (mS)	12.3	11.28	8.2
f_c (GHz)	2.44	2.417	0.94
BW (MHz)	84	88	4.76
Quality factor	29	27.5	5
Output Gain (dB)	15	13.12	12.53

By the results in table 4.8 we can see a close agreement between the target and the achieved values. The largest relative error was obtained in the output gain of approximately 12.5%.

In the following subsection a comparison of the performance of the filter using the two types of integrated inductors is performed.

4.4.4 Conclusions

In order to get a more appropriate comparison between the two implementations of the filters, a fine tuning was carried out with the purpose of the frequency response of the filters became identical and in order to meet the desired specifications. The inverse proportional relation between G_m of the input and G_{neg} of loss compensation negative resistance must be taken into account. For example, suppose that G_{neg} is decreased for lower Q, then G_m should be increased to keep the gain constant. The center frequency shifting is mainly due to the parasitic capacitances of the transistors. This can be compensated by reducing the value of the capacitance C. In this way, we can achieve the synchronized coarse tuning of f_0, gain, the -3 dB bandwidth and the corresponding Q. The fine tuning can be done in the following steps by considering the weak interaction between f_0, gain and Q, and the control variables such as G_m and G_{neg}:

1. Tune C for f_0 fine tuning.

2. Tune G_{neg} for fine bandwidth tuning and the consequent fine filter Q tuning.

3. Tune G_m for fine gain tuning.

The table 4.9 presents the values of the parameters changed to the fine tuning.

Table 4.9: Fine tuning resulting values

Parameter	Regular inductor		Optimized inductor	
	Before	After	Before	After
C (pF)	4.25	4.06	4.25	4.10
$W_{1,2,3}$ (μm)	18.7	19.7	13.14	14.1
$W_{4,5,6}$ (μm)	62.8	71.5	63.6	71.5

In figures 4.9 and 4.10 the AC desired response of the filter is presented.

The table 4.10 shows the performance comparison of RF integrated LC filter for the two types of integrated inductors.

The comparison table demonstrates that the proposed RF filter has lower power-consumption when using the optimized (variable width) inductors in order of 10%. This reduction is due to decreased resistance of the optimized inductor. A smaller resistance requires a G_{neg} smaller reducing the size of the transistors.

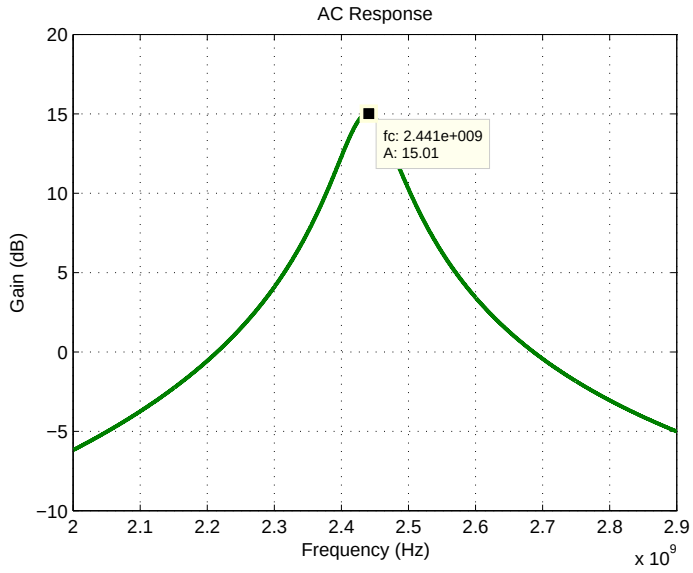


Figure 4.9: Frequency response of the RF LC Q-enhanced filter using a regular spiral inductor

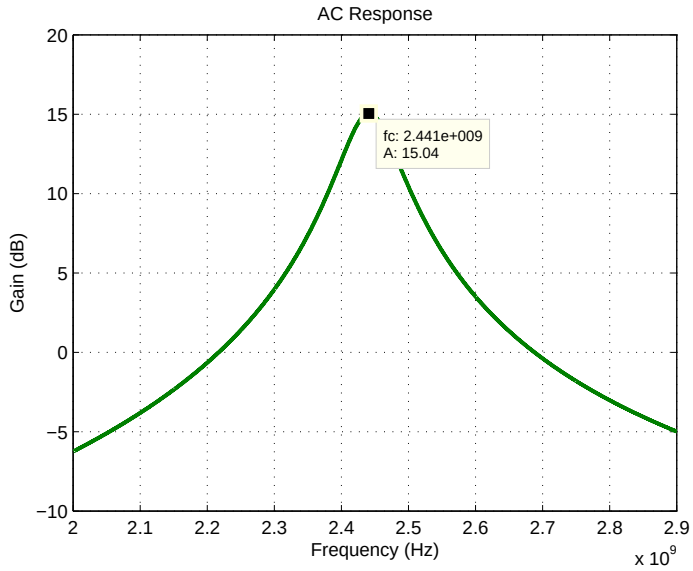


Figure 4.10: Frequency response of the RF LC Q-enhanced filter using a regular spiral inductor

Table 4.10: Simulation results

Performance Parameters	Regular Inductor	Optimized Inductor
Center frequency (GHz)	2.441	2.441
3 dB Bandwidth (MHz)	84	84
Maximum Gain in passband (dB)	15.01	15.04
Supply Voltage (V)	1.2	1.2
DC Current (mA)	5.66	5.09
DC consumption (mW)	6.79	6.11

Chapter 5

Conclusions

The design and simulation of a 2.44 GHz in standard 0.13μm CMOS fully integrated second-order Q-enhanced LC bandpass filter have been introduced and verified, which demonstrate that the RF bandpass filter can achieve a high selectivity.

In a fully integrated LC bandpass filter the integrated spiral inductor is an important performance-limiting component in RF circuits. This work is devoted to the study of RF integrated inductors as planar square spirals in silicon-based technology. The degradation of the Q-factor presents great challenge for the designers. The inductor series resistance is analysed taking into account both ohmic losses, due to conduction currents and magnetically induced losses, due to eddy currents.

A method to improve the Q factor of the inductor is presented. The method is based on the layout optimization being the width of the metal strip used to perform the main variable of the optimization process. For a given frequency of operation, the application of the proposed method minimizes the series resistance of each segment of the inductor coil, leading to a multistrip-width layout.

The proposed method is used to optimize the layout of square spiral inductors for the 0.13μm CMOS technology. The comparison of the results obtained for the optimized layout with those of other non-optimized (occupying the same chip's area) reveals that the application of the proposed model leads to a significant increase in the inductor Q factor. From the examples presented a quality factor of 20% to 30% to may be obtained by using variable metal width.

A 2^{nd} order filter with center frequency ate 2.44 GHz was designed using integrated spiral inductors. The quality of on-chip reactive components is a challenge in the design of such filter, since the losses and the parasitics in those components can result in frequency response distortion and need for active components like negative resistors to compensate the losses. In order to validate the performance of the optimized inductor a comparison as performed between inductors with and without layout optimization. The results shows that with a power supply of 1.8 V the filter using the optimized inductor has a lower power consume in order of 10%.

With this work it has been verified through simulation that the design of a Q-enhanced LC filter in a new systematic way to achieve gain, center frequency, and filter Q tuning capability.

Bibliography

[1] W. A. Gee, *CMOS Integrated LC Q-Enhanced RF Filters for wireless receivers.* PhD thesis, Georgia Institute of Technology, 2005.

[2] P. Almeida, P. Pereira, and M. H. Fino, "Using variable width rf integrated inductors for quality factor optimization," in *Technological Innovation for the Internet of Things*, vol. 394, pp. 619–627, Springer Berlin Heidelberg, 2013.

[3] F. Bahmani, *High Performance RF and baseband building blocks for wireless receivers.* PhD thesis, Texas A and M University, 2006.

[4] S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *Solid-State Circuits, IEEE Journal of*, vol. 34, pp. 1419 –1424, oct 1999.

[5] G. Zardo, "A 4th order cmos 0,13 μm integrated lc filter for rf receivers," Master's thesis, Ecole Polytechnique, 2006.

[6] W. Yu, "Optimization of spiral inductors and lc resonators exploiting space mapping technology," Master's thesis, McMaster University, 2006.

[7] J. Lopez-Villegas, J. Samitier, C. Cane, P. Losantos, and J. Bausells, "Improvement of the quality factor of rf integrated inductors by layout optimization," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 48, pp. 76 –83, jan 2000.

[8] J. Peters, "Design of high quality factor spiral inductors in rf mcm-d," Master's thesis, Massachusetts Institute of Technology, 2004.

[9] C. Yue, C. Ryu, J. Lau, T. Lee, and S. Wong, "A physical model for planar spiral inductors on silicon," in *Electron Devices Meeting, 1996. IEDM '96., International*, pp. 155 –158, dec. 1996.

[10] S. Jenei, B. Nauwelaers, and S. Decoutere, "Physics-based closed-form inductance expression for compact modeling of integrated spiral inductors," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 77 –80, jan 2002.

[11] M. Raieszadeh, "High-q integrated inductors on trenched silicon islands," Master's thesis, Georgia Institute of Technology, 2005.

[12] M. Park, C.-H. Kim, C. S. Kim, M.-Y. Park, S.-D. Kim, Y.-S. Youn, and H. K. Yu, "Frequency-dependent series resistance of monolithic spiral inductors," *Microwave and Guided Wave Letters, IEEE*, vol. 9, pp. 514 –516, dec 1999.

[13] Y.-S. Choi and J.-B. Yoon, "Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for rf ics," *Electron Device Letters, IEEE*, vol. 25, pp. 76 – 79, feb. 2004.

[14] J. Aguilera and R. Berenguer, *Design and Test of Integrated Inductors for RF Applications*. Kluwer Academic Publishers, 2004.

[15] J. Chen and J. J. Liou, "On-chip spiral inductors for rf applications: An overview," *Journal of Semiconductor Technology and Science*, vol. 4, no. 3, pp. 149–167, 2004.

[16] H. Heng-Ming, "Improving the quality factor of a broadened spiral inductor with arithmetic-progress step width," *Microwave and Optical Technology Letters*, vol. 45, no. 2, pp. 118–120, 2004.

[17] J. Liu, Y. Shi, X. Wen, D. Chen, T.-X. Luo, H. Huang, H. Ye, and Y. Wang, "On-chip spiral inductor with novel gradually changed structure," *Microwave and Optical Technology Letters*, vol. 50, no. 8, pp. 2210–2213, 2008.

[18] P. Pereira, M. H. Fino, F. Coito, and M. Ventim-Neves, "Gadisi – genetic algorithms applied to the automatic design of integrated spiral inductors.," (Caparica, Pt), pp. 515–522, Springer, 2010.

[19] P. Pereira, H. Fino, F. Coito, and M. Ventim-Neves, "Adisi- an efficient tool for the automatic design of integrated spiral inductors," in *Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on*, pp. 799 –802, dec. 2009.

[20] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. Cambridge, MA, USA: Oxford University Press, 1991.

[21] Y. Sun, ed., *Active filters using integrated inductors*, vol. 14 of *Circuits, Devices and Systems*, The Institution of Engineering and TechnologySpringer, 2002.

Appendix A

Publications

In this appendix the article made throughout this thesis are presented. The article "Using Variable Width RF Integrated Inductors for Quality Factor Optimization", was submitted in the 4th IFIP WG 5.5/SOCOLNET Doctoral Conference on Computing, Electrical and Industrial Systems, DoCEIS 2013. This article is based on all the work done throughout the project of this master thesis.

Using Variable Width RF Integrated Inductors for Quality Factor Optimization

Pedro Almeida[1], Pedro Pereira[1], Helena Fino[1]

[1] Departamento de Engenharia Electrotécnica, Faculdade de Ciências e Tecnologia, FCT, Universidade Nova de Lisboa, 2829-516 Caparica, Portugal.

pedrodalmeida77@gmail.com, {hfino, pmrp}@ieee.org

Abstract. The advancement of CMOS technology led to the integration of more complex functions. In the particular of wireless transceivers, integrated LC tanks are becoming popular both for VCOs and integrated filters [1]. For RF applications the main challenge is still the design of integrated inductors with the maximum quality factor. For that purpose, tapered, i.e., variable width inductors have been proposed in the literature. In this paper, analytical expressions for the determination the pi-model parameters, for the characterization of variable width integrated inductors are proposed. The expressions rely exclusively on geometrical and technological parameters, thus granting the rapid adaptation of the model to different technologies. The results obtained with the model are compared against simulation with *ASITIC*, showing errors below 10%. The model is then integrated into an optimization procedure where inductors with a quality factor improvement in the order of 20-30% are obtained, when compared with fixed width inductors.

Keywords: Inductor layout optimization, variable metal width, integrated RF inductor

1 Introduction

During the last years the worldwide market on communications has experienced an ever-growing demand for integrated systems with scaling down dimensions and increased functionality. In the particular case for RF communication circuits, integrated spiral inductors are widely used, notwithstanding their poor performance and their subsequent negative impact on the circuit efficiency at high frequencies. This poor performance is due to the large effect the technology parasitics have on the small value of inductance usually required. As a result, significant effort has been employed in investigating silicon planar inductors, their associated models and methods of improving their performance [1-3].

Regarding layout optimization, non-uniform metal width is proposed, as a way of increasing the inductor quality factor [4, 5]. The main objective of this methodology is to reduce the influence of magnetically induced losses in the inner turns of the

spiral where the magnetic field reaches its maximum. By reducing the line width toward the center of the spiral a minimization of the series resistance of the inductor coil, taking into account both Ohmic losses due to conduction currents, and magnetically induced losses due to Eddy currents, is obtained. Although several promising results have been reported, a fully analytical characterisation of the inductor, leading to perfect understanding of the device performance limitations, is needed so that optimized designs may be obtained.

In this paper analytical expressions for the evaluation of the inductor model parameters are proposed. These expressions rely exclusively on technological parameters and on the geometrical characterization of each inductor segment. The proposed model is used for the optimization-based design of several inductors, where the advantage of using tapered topologies is well pointed out.

The remain of the paper is organized as follows. The novelty introduced by this paper, is highlighted in Section 2. In this section the basic inductor model is introduced and then, the adaptation of the model for variable width inductors is carefully described. Section 3 is dedicated to the description of several working examples. Finally, conclusions are offered in Section 4.

2 Relationship to Internet of Things

Internet of things relies on the interconnections of a large number of heterogeneous cooperating devices. The development of these devices has been made possible due to the rapid evolution of electronic technologies, enabling the implementation complex functions, in smaller and more rapid circuits. To cope with the necessity of minimizing the power consumption of such systems, new design methodologies must be adopted. In the particular case of communications services, RF integrated inductors are becoming popular elements. Yet, designing integrated inductors for RF applications is a challenging process where a set of correlated geometrical parameters must be obtained, leading to the need of using optimization-based design methodologies.

The main objective of the work described is the optimization of the spiral inductors quality factor, by using variable width inductors

The novel contributions of this paper are as follows:

- It proposes a set of analytical expressions for the evaluation of the pi-model parameters, for variable width integrated inductors. The proposed expressions depend exclusively on the technological parameters and on the geometric characterization of each segment of the inductor.
- It proposes an efficient optimization-based design for nano-CMOS planar spiral inductor, based in analytical models, instead of using an electromagnetic simulation based approach;

Since the proposed equations are an extension of the model used for fixed width inductors, next sub-section gives a brief description of this model. In subsection 2.2 the adequacy of the model to variable width inductors is carefully described.

2.1 Planar Spiral Inductor Pi-Model

Several integrated inductor models have been introduced in the last years, as illustrated in Fig.1 [6]

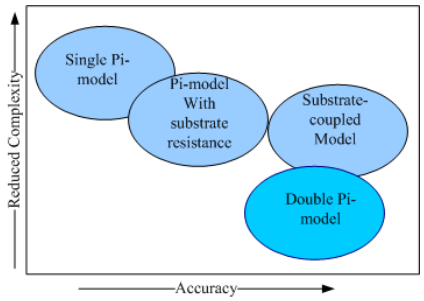


Fig. 1. Planar inductor lumped element models complexity versus accuracy trade-off

The simplest one is the pi-model, which is widely used for inductors operating in a frequency range up to a few GHz. For the sake of simplicity, the pi-model, illustrated in Fig. 2.a., is adopted, where L_s, and R_s. account for the inductance and resistance of the spiral. The overlap between the spiral and the underpass allows direct capacitive coupling between the two terminals of the inductor. The feed-through part is modelled by C_s. Capacitor C_{ox} represents the capacitance between the spiral and the substrate. Finally, C_{si} and R_{si} account for the silicon substrate capacitance and resistance, respectively.

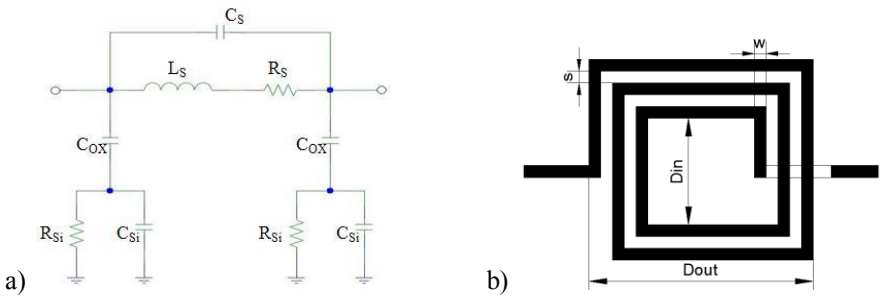


Fig. 2. a) Planar inductor pi-model; b) Geometric parameters for a square inductor.

For the evaluation of the inductance, L_S, several approaches have been proposed, based either on fitting processes to experimental values [7] or through physics-based equations [8], where

$$L_s = k_1 \mu_0 n^2 d_{avg} / (1 + k_2 \rho). \quad (1)$$

Given that,

$$\rho = (d_{out} - d_{in})/(d_{out} + d_{in}). \quad (2.a)$$

$$d_{avg} = 0.5(d_{out} + d_{int}). \quad (2.a)$$

$$d_{out} = d_{in} + 2nw + 2(n-1)s. \quad (2.b)$$

Where n is the number of turns, s is the track-to-track distance, and w is the track width. Finally, k_1 and k_2, are coefficients allowing the model to be adapted to several inductor shapes.

The evaluation of the spiral resistance, R_s, is obtained by [9]

$$R_s = \sqrt{{R_{dc}}^2 + {R_{ac}}^2}. \quad (3)$$

Where,

$$R_{dc} = l/\ (\sigma w t). \quad (4.a)$$

$$R_{ac} = kl/[2\sigma\delta(w+t)]. \quad (4.b)$$

And σ and t are the metal conductivity and thickness, respectively. The metal length, l, is obtained with [10]

$$l = N_{sides} d_{avg} n\ tan(\pi/N_{sides}). \quad (5)$$

And the skin depth, δ, may be determined by [11]

$$\delta = 1/\sqrt{\sigma\mu\pi f}. \quad (6)$$

For the evaluation of the capacitance, C_s, all overlap capacitances are considered and given by [12].

$$C_s = n_c w^2\, \varepsilon_{ox}/t_{oxM1-M2}. \quad (7)$$

Where ε_{ox} is the oxide permittivity, n_c is the number of overlaps and $t_{oxM1-M2}$ is the oxide thickness between the spiral upper and lower metal. The parasitic capacitance, C_{ox}, between the spiral metal and the silicon substrate, is estimated with [12]

$$C_{ox} = 0.5lw\, \varepsilon_{ox}/t_{ox}. \quad (8)$$

Where t_{ox} is the thickness of the SiO_2 between the inductor and the substrate and lw defines the area of the spiral. Finally the Substrate resistance, R_{si}, and capacitance C_{si}, are obtained with 11

$$R_{si} = 2h_{si}/(l\, w\, \sigma_{si}). \quad (9)$$

$$C_{si} = 0.5lw\, \varepsilon_o \varepsilon_r/h_{si}. \quad (10)$$

where σ_{si} and h_{si} are the substrate conductivity and height, respectively.

This model has been extensively used in an optimization-based tool for inductor design [13] yielding solutions with very good accuracy when compared with results obtained with ASITIC.

2.2- Variable Width Inductor Model

Variable width inductor layout has been proposed as a way of maximizing the quality factor of integrated inductors. In this work, square inductors, where each segment shows a width increment of Δw, as illustrated in Fig.3. , are considered.

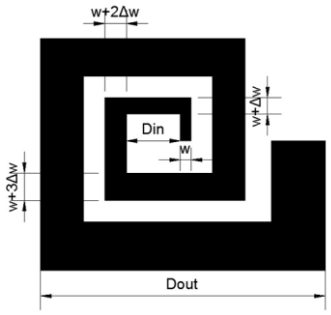


Fig. 3. Variable width square inductor

Since each segment will show an increment on both width and length new equations will be proposed, relying on the dimensions of each segment of the inductor. The width of a segment may be evaluated with

$$w_i = w + n_i \Delta w. \tag{11}$$

Where n_i is the number of the segment, and w is the initial metal width.

In this work, the basic structure for supporting all the inductor segments characterization is a matrix of five columns (one for each segment per turn) and n lines (one per inductor turn). Initially, a matrix containing every segment length, l_{ij} as

$$l_{ij} = \begin{bmatrix} l_{11} & l_{12} & l_{13} & l_{14} & l_{15} \\ l_{21} & l_{22} & l_{23} & l_{24} & l_{24} \\ \dots & \dots & \dots & \dots & \dots \\ l_{n1} & l_{n2} & l_{n3} & l_{n4} & l_{n5} \end{bmatrix}. \tag{12}$$

Is generated. Then a matrix containing every segment width, w_{ij}

$$w_{ij} = \begin{bmatrix} w_{11} & w_{12} & w_{13} & w_{14} & w_{15} \\ w_{21} & w_{22} & w_{23} & w_{24} & w_{24} \\ \dots & \dots & \dots & \dots & \dots \\ w_{n1} & w_{n2} & w_{n3} & w_{n4} & w_{n5} \end{bmatrix}. \quad (13)$$

is generated.

Regarding the pi-model inductance, L_S, a new way for evaluating d_{out} must be adopted. Considering the basic matrixes in (12), (13), d_{out} may be obtained by

$$d_{out} = l_{n4} + w_{n5}. \quad (14)$$

For the evaluation of R_S, (4.a) and (4.b) are replaced by

$$R_{dc} = \frac{1}{\sigma t} \sum_{i=1}^{n} \sum_{j=1}^{5} \frac{l_{ij}}{w_{ij}}. \quad (15.a)$$

$$R_{ac} = \frac{k}{2\sigma\delta} \sum_{i=1}^{n} \sum_{j=1}^{5} \frac{l_{ij}}{w_{ij} + t}. \quad (15.b)$$

For this purpose the two new matrix (15.a) and (15.b) are generated containing each segment geometrical information for R_{dc} and R_{ac}

$$\frac{l_{ij}}{w_{ij}} = \begin{bmatrix} \frac{l_{11}}{w_{11}} & \frac{l_{12}}{w_{12}} & \frac{l_{13}}{w_{13}} & \frac{l_{14}}{w_{14}} & \frac{l_{15}}{w_{15}} \\ \frac{l_{21}}{w_{21}} & \frac{l_{22}}{w_{22}} & \frac{l_{23}}{w_{23}} & \frac{l_{24}}{w_{24}} & \frac{l_{25}}{w_{25}} \\ \dots & \dots & \dots & \dots & \dots \\ \frac{l_{n1}}{w_{n1}} & \frac{l_{n2}}{w_{n2}} & \frac{l_{n3}}{w_{n3}} & \frac{l_{n4}}{w_{n4}} & \frac{l_{n5}}{w_{n5}} \end{bmatrix}. \quad (16)$$

$$\frac{l_{ij}}{w_{ij} + t} = \begin{bmatrix} \frac{l_{11}}{w_{11} + t} & \frac{l_{12}}{w_{12} + t} & \frac{l_{13}}{w_{13} + t} & \frac{l_{14}}{w_{14} + t} & \frac{l_{15}}{w_{15} + t} \\ \frac{l_{21}}{w_{21} + t} & \frac{l_{22}}{w_{22} + t} & \frac{l_{23}}{w_{23} + t} & \frac{l_{24}}{w_{24} + t} & \frac{l_{25}}{w_{25} + t} \\ \dots & \dots & \dots & \dots & \dots \\ \frac{l_{n1}}{w_{n1} + t} & \frac{l_{n2}}{w_{n2} + t} & \frac{l_{n3}}{w_{n3} + t} & \frac{l_{n4}}{w_{n4} + t} & \frac{l_{n5}}{w_{n5} + t} \end{bmatrix}. \quad (17)$$

Finally (8) , (9) and (10) are replaced by

$$C_{ox} = \frac{1}{2} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \sum_{i=1}^{n} \sum_{j=1}^{5} l_{ij} w_{ij} \,. \tag{18}$$

$$R_{si} = \frac{2}{G_{sub}} \sum_{i=1}^{n} \sum_{j=1}^{5} \frac{1}{l_{ij} w_{ij}} \,. \tag{19}$$

$$C_{si} = \frac{1}{2} \cdot C_{sub} \sum_{i=1}^{n} \sum_{j=1}^{5} l_{ij} w_{ij} \,. \tag{20}$$

For which an auxiliary matrix containing the area of each segment is considered.

4 Variable Inductor Working Example

In order to confirm the validity of the proposed layout optimization method, a set of square spiral inductors has been designed. Three examples, considering the design of 1nH, 1.5nH and 2nH inductors at a working frequency of 1GHz will be presented. In all examples the technological parameters shown in Table I were used

TABLE I
UMC130 – TECHNOLOGICAL PARAMETERS

Parameter	Value	Parameter	Value
ε_o	8.85e-12	t_{ox}(μm)	600
ε_r	1.0	C_{sub} (F/m^2)	4.0e-6
σ (Ωm)	1/2.65e-8	G_{sub} (S/m^2)	2.43e5

For the model validation a comparison between results obtained with variable width design, against fixed width designs, for an approximately equal area, is presented. The layout parameters were evaluated according to the constraints in Table II

TABLE III
SPIRAL INDUCTOR DESIGN CONSTRAINTS

Parameter	Min	Step	Max
w (μm)	5.0	0.5	100.0
Δw (μm)	1	0.25	-
s(μm)	1.5	-	-
d_{in} (μm)	20.0	0.5	200.0
n	1.5	1.0	15.5
d_{out}	-	-	500

A. *Example 1 – Inductor with 1 nH*

In this example a spiral inductor of 1nH was considered. The results obtained for a fixed width layout as well as for Δw of 1.25µm, 1.5µm and 1.75µm are represented in Table II. Also in the same table, the simulation results obtained with ASITIC for each case are represented.

TABLE IIII
OPTIMIZATION RESULTS FOR 1nH INDUCTOR WITH SEVERAL Δw

Ind	Δw (µm)	w (µm)	d_{in} (µm)	n	d_{out} (µm)	L (nH)			Q			Q.
						Model	Asitic	ε_L	Model	Asitic	ε_Q	Impr.
1	0	13.8	68.8	2.5	157	1	1.07	6.3%	**6.94**	6.28	10.5%	
2	1.25	7.5	41.3	3	154	0.998	1.06	5.4%	8.07	8.24	1.7%	16%
3	1.5	7.25	39.8	3	161	0.999	1.04	4.3%	8.57	8.53	0.5%	23%
4	1.75	5.75	40.3	3	162	1.01	1.04	2.5%	**8.52**	8.16	4.4%	**23%**

In the last column the relative improvement in the quality factor from using incremental width is given.

B. *Example 2 – Inductor with 1.5nH*

In this example a spiral inductor of 1.5nH was considered. The results obtained for a fixed width layout as well as for Δw of 2µm, 2.5µm and 3.0 µm are represented in Table II. Also in the same table, the simulation results obtained with ASITIC for each case are represented.

TABLE IVI
OPTIMIZATION RESULTS FOR 1.5 nH INDUCTOR WITH SEVERAL Δw

Ind	Δw (µm)	w (µm)	d_{in} (µm)	n	d_{out} (µm)	L (nH)			Q			Q
						Model	Asitic	ε_L	Model	Asitic	ε_Q	impr
1	0	20.3	10.3	2.5	231	1.5	1.62	7.6%	**10.1**	9.27	9.0%	
2	2	11.5	61.3	3	233	1.5	1.58	5.2%	12.29	12.61	2.6%	22%
3	2.5	6.25	64.3	3	221	1.5	1.52	1.6%	11.07	10.59	4.6%	9%
4	3	8.75	58	3	253	1.51	1.54	1.8%	**13.44**	12.74	5.5%	**33%**

C. *Example 3 – Inductor with 2nH*

In the last example a spiral inductor of 2.0nH was considered. The results obtained for a fixed width layout as well as for Δw of 2µm, 2.5µm and 3.0µm are represented in Table II. Also in the same table, the simulation results obtained with ASITIC for each case are represented.

TABLE V
OPTIMIZATION RESULTS FOR 1.5 nH INDUCTOR WITH SEVERAL Δw

Ind	Δw (µm)	w (µm)	d_{in} (µm)	n	d_{out} (µm)	L (nH)			Q			Q
						Model	Asitic	ε_L	Model	Asitic	ε_Q	impr
1	0	25.8	137	2.5	297	2	2.16	7.6%	**12.72**	11.62	9.4%	
2	2.75	12.5	85	3	296	2	2.1	4.8%	15.03	15.21	1.2%	18%
3	3	9.75	86.3	3	288	2	2.05	2.6%	14.39	14.19	1.4%	13%
4	3.75	10.3	80.5	3	317	2	2.05	2.6%	**16.14**	15.34	5.2%	**27%**

5 Conclusions

In this paper the analytical expressions for the evaluation of integrated inductor pi-model parameters was proposed. This expressions consider variable width square inductors, were each segment shows a constant increment of width. The validity of the model was shown through three working examples considering the design of 1.0nH, 1.5nH and 2.0nH inductors at a working frequency of 1GHz. From the examples presented a quality factor improvement in the order of 20% to 30% may be obtained, by using variable width.

Should higher frequency of operation be envisaged, a more accurate inductor, such as 2-pi-model should be used. The adaptation of the proposed equations to the 2-pi-model is under test.

References

1. I Krout, H. Mnif, M. Fakhfakh, and M. Loulou, "Optimizing LC VCO Performances Through a Heuristic", Wseas Transactions on Electronics, vol. 5, pp.274-281, 2008.
2. P-W. Lai, L. Dobos, S. Long, "A 2.4GHz SiGe low phase noise VCO using on chip Tapped inductor", Solid-State Circuits Conference - ESSCIRC,pp. 505–508, 2003.
3. L. L. K. Leung, and H. C. Luong, "A 1V9.7mW CMOS frequency synthesizer for IEEE 802.11a transceivers", IEEE Trans. Microw. Theory Tech., vol. 56, pp. 39–48, Jan. 2008.
4. Wesley A. Gee, "CMOS Integrated LC **Q**-enhanced RF Filters for wireless Receivers", PhD. Thesis, Georgia Institute of Technology, 2005.
5. C. Patrick Yue and S. Simon Wong, "Physical modeling of spiral inductors on silicon", IEEE Transactions on Electron Devices, Vol. 47 560-568, 2000.
6. Lai,I., Fujishima, M., "Design and Modeling of Millimeter-Wave CMOS Circuits for Wireless Transceivers - Era of Sub-100nm Technology", Springer, 2008.
7. Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances", IEEE Journal of Solid-State Circuits, Vol. 34, Nº 10, October 1999.
8. S. Jenei, B. K. J. C. Nauwelaers, and S. Decoutere, "Physics-Based Closed-Form Inductance Expression for Compact Modelling of Integrated Spiral Inductors," IEEE J. Solid-State Circuits, vol. 37, no. 1, pp. 77–80, January 2002.
9. Y. S. Choi and J. B. Yoon, "Experimental Analysis of the Effect of Metal Thickness on the Quality Factor in Integrated Spiral Inductors for RF ICs," IEEE Electron Device Lett., vol. 25, no. 2, pp. 76–79, February 2004.
10. D. J. Allstot, K. Choi, J. Park, "Parasitic-Aware Optimization of CMOS RF Circuits", *Kluwer Academic Publishers*, ISBN 1-4020- 7399-2, 2003.
11. M. Park, C. H. Kim, C. S. Kim, et. al, "Frequency-Dependent Series Resistance of Monolithic Spiral Inductors," IEEEMicrowave Guided Lett., vol. 9, no. 12, pp. 514–516, December 1999.
12. Olive H. Murphy, "Advanced Physical Modelling of Multilayer Inductors for CMOS RF Front-End Applications", PhD Thesis, University College Cork - National University of Ireland, October, 2005.
13. Pereira, P., Fino, M. H., Coito, F. & Ventim-Neves,M. "ADISI- An efficient tool for the automatic design of integrated spiral inductors" The 16th IEEE International Conference on Electronics, Circuits, and Systems (ICECS'09), 799–802, 2009.