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Transimpedance Amplifier for Integrated SpO2 Optic Sensor

Dissertação para obtenção do Grau de Mestre em
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Resumo

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestre em Engenharia Electrotécnica e de Computadores

por José Alberto Martins de Carvalho

O nível de oxigenação do sangue, ou SpO2 (saturação de hemoglobina arterial como é medida pelo oxímetro de pulso) é um sinal vital essencial para o diagnostico médico e a sua medição por métodos não invasivos é uma das grandes inovações da medicina moderna. Esta medição pode ser efectuada pelo processamento da luz vermelha e infravermelha reflectida no dedo do paciente e recebida num fotorreceptor. Antes deste sinal ser aplicado a um conversor analógico-digital (ADC), a corrente gerada no fotorreceptor tem de ser convertida para um sinal em tensão, e a sua amplitude ajustada por forma a usar totalmente a gama dinâmica do ADC. Uma vez que o fotorreceptor gera um sinal em corrente de amplitude variável, é necessário um amplificador de transimpedância (TIA) de ganho controlável. O TIA de dois andares proposto nesta tese utiliza um andar de porta comum com regulação (RCG) no primeiro andar, ao mesmo tempo que utiliza técnicas de cancelamento de ruído e de conversão de sinal single-end para diferencial, com recurso a um andar fonte comum adicional. Um segundo andar de ganho regulável é implementado, baseado no amplificador MOS paramétrico (MPA), idealmente sem ruído. O MPA é um amplificador em tempo discreto, eliminando portanto a necessidade de um circuito de amostragem (S & H), na entrada do ADC. O circuito proposto foi dimensionado em tecnologia CMOS standard de 130 nm com 1.2 V de tensão de alimentação e o consumo total do circuito é inferior a 350 μW.

Palavras Chave: SpO2; Amplificador de Transimpedância; Cancelamento de Ruído; Amplificador Parametrico; Baixa Potência

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Abstract

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The oxygen level in blood, usually referred as SpO2 (Saturation of hemoglobin with oxygen as measured by pulse oximetry) is an essential medical information. Measuring the oxygen level of the human blood using non- intrusive techniques is a vital achievement in modern medicine. This can be performed by processing the infrared and red light transmitted through the patient's finger and received by a photoreceptor. Before being applied to an analog-to-digital converter (ADC), the incoming light has to be converted to a voltage and the range should be dynamically adjusted in order to use the full input range of the ADC. Since the photoreceptor generates an output current, a transimpedance amplifier (TIA) with gain control is required. The two-stage TIA proposed in this paper, uses a regulated common-gate (RCG), in the first stage, employing noise cancellation and balun operation using an additional common-source (CS) stage, while the adjustable gain is implemented in the second-stage, which is based on an intrinsically noiseless MOS parametric amplifier (MPA). This MPA operates in the discrete-time domain, thus, eliminating the need of an input sample-and-hold (S&H) block in the ADC. The proposed circuit has been designed in a 130 nm digital 1.2 V CMOS technology with a power consumption lower than 350 μW.

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Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog to **D**igital **C**onverter
CG	**C**ommon **G**ate
CMOS	**C**omplementary **M**etal-**O**xide **S**emiconductor
CS	**C**ommon **S**ource
DC	**D**irect **C**urrent
DTPA	**D**iscrete **T**ime **P**arametric **A**mplifier
IC	**I**ntegrated **C**ircuits
IR	**I**nfra**R**ed
KCL	**K**irchhoff's **C**urrent **L**aw
LED	**L**ight **E**mitting **D**iode
LNA	**L**ow **N**oise **A**mplifier
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
NEF	**N**oise **E**xcess **F**actor
PCB	**P**rinted **C**ircuit **B**oard
PSD	**P**ower **S**pectral **D**ensity
RCG	**R**egulated **C**ommon **G**ate
RGC	**R**e**G**ulated **C**ascode
RF	**R**adio **F**requency
S&H	**S**ample and **H**old
SoC	**S**ystem **o**n **C**hip
TIA	**T**rans**I**mpedance **A**mplifier
VCCS	**V**oltage **C**ontrolled **C**urrent **S**ource

Chapter 1

Introduction

1.1 Background and Motivation

Nowadays, with the increased population demand, there is a need for better and more economic health care. It's in this context that the need for economical and reliable devices to continuously and remotely monitor the health of a patient arises, in order for actions to be taken as soon as a change in a patients status is observed, and thus, improving the health care quality and saving costs, on the long run, by dealing with illnesses and critical conditions on it's early stages. In modern medicine the blood oxygen level is considered to be one of the important vital signs (alongside blood pressure, heart rate, breathing rate and body temperature) and its constant monitoring can give early insight on problems in the circulatory and respiratory system.

Pulse oximeters are a non-invasive method to measure the percentage of oxygenated hemoglobin in a patients blood, and as such are ubiquitous in modern medicine, as such pulse oximeters are widely used in intensive care, operating rooms, emergency care, birth and delivery, neonatal and pediatric care, sleep studies, among others.

In traditional pulse oxymeters the transducer is usually clipped or taped to a translucent area of the patient, such as an earlobe or a finger, and wires extend from the transducer to the central processing unit, making this system not very practical for portable and wearable applications and limiting it's usefulness.

Besides the traditional applications, there is a growing demand for a new type of devices, which focus on the remote monitoring of the patients, and so the need for novel architectures built around cheap and portable solutions arises. This new devices will make possible applications, such as, home care monitoring for the elderly or chronically ill, wireless medical sensing, remote monitoring of the health status of military personnel in the battlefield as well as fire-fighters engaging in fire control, and rescue missions. It's in this context that reducing size and power consumption is critical. Power consumption is directly related to price and size, because it directly influences battery life. More compact approaches comprising the whole transducer and analog front-end could potentially lead to cheaper and easier to use disposable systems, boosting even further the applications of this systems.

In this work a CMOS differential transimpedance amplifier (TIA) with adjustable gain that also doubles as a sample and hold (S&H) is proposed in order to be implemented in the same die as a photo-detector and ADC (Analog-To-Digital Converter) in order to build a full SoC pulse oximeter analog front end. To accommodate for different photo-sensor's, variations in light sources and transducer positioning a controllable gain is desirable. The goal is to design a TIA that is both low power, and has a high dynamic range with controllable gain.

1.2 Thesis Organization

This thesis has been organized in six chapters, including this introductory chapter.

Chapter 2 consists of a brief overview of the pulse oximetry principles. This includes a brief explanation of the phisical aspects of the pulse oximetri measurment as well as a breif explanation of the basic blocks in the architecture. A basic overview of noise in CMOS circuits is then presented, as well as an introduction to two of the most common TIA topologies, and the principles of parametric amplification.

In Chapter 3, a more in depth analysis is given for the RCG TIA. Starting with a very simple and intuitive explanation of the working principle of the RCG circuit we start from the CG and then introduce the gm boosting mechanism characteristic of this topology. After having some insight into the basics of the RCG, teoretical equations for input impedance, transimpedance function and noise are presented as well as some considerations regarding the stability of the RCG.

Chapter 4 presents a noise cancelling and balun operation principle. First, the known equations for the LNA CG/CS circuit are shown, and then a parallelism between the LNA and the TIA is demonstrated, and equations to guarantee simultaneous noise cancelling and balun operation are presented. From the analysis of the RCG, the proposed RCG/CS circuit is then presented with the matching conditions to assure noise cancelling and balun operation.

Chapter 5 is dedicated to the DTPA, which is the second stage of the proposed architecture. First a brief analysis of the working principle of the DTPA is made. The MOS varactor that constitutes the heart of the DTPA is then presented, as well as a technique that enables the gain to be varied. The proposed DTPA is then presented with simulation results the corroborate the proposed variable gain aspect of the circuit.

Chapter 6 starts with implementation considerations for the proposed circuit. Simulation results are provided for the TIA and the complete architecture. It's shown that the TIA has a good performance compared to other circuits with similar purposes in the literature. The DPTA is shown to work as expected in simultaneous with the TIA.

Chapter 7 comprises the overall conclusions on the work developed, as well as suggestions for further research work.

1.3 Contributions

The main contributions of this thesis are:

A novel integrated architecture for a front end amplifier for application in SpO_2 sensors is presented. The presented architecture aims at being booth low power, and low noise. The architecture comprises two main blocks, namely a transimpedance amplifier and a discrete time parametric amplifier with gain control.

A new topology is proposed for the transimpedance amplifier based on the regulated common gate, and the well known common-gate/common-source topologies. The proposed circuit exploits booth thermal and flicker noise cancelling, while offering balun operation.

A new controllable gain amplifier is proposed based on the discrete time MOS parametric amplifier. A circuit is designed and validated by simulation.

This work also originated a paper accepted for oral presentation at the 2012 IEEE International Conference Mixed Design of Integrated Circuits Systems (MIXDES)[4].

Chapter 2

State of the art

In the following sections, the physics behind the working principles of a pulse oximeter are presented in order to give a better insight on the challenges of the its design. Then the proposed pulse oximeter architecture is presented, as well as its constituting blocks.

2.1 Principles of Pulse Oximetry

The percentage of oxygen in blood as measured by the pulse oximeter(SpO_2)is given by the ratio between oxygenated hemoglobin and the total hemoglobin, as given by 2.1, where HbO_2 is refers to the oxygenated hemoblogin, and Hb refers to hemoglobin with reduced oxygen.

$$SpO_2 = \frac{HbO_2}{Hb + HbO_2} \tag{2.1}$$

Oxygenated hemoblogin(HbO_2), which is bright red absorbs more IR light, and let's more red light pass through it than its de-oxygenated counter part, the dark red hemoglobin(Hb), as can be observed in Fig.2.1. It's this different absorption characteristics for red light (660 nm) and infra-red light (940 nm) that make possible to measure the blood oxygenation by measuring the ratio of absorption of red and IR light.

The light sources, usually light-emitting diodes (LED's) shine red and IR light through a translucent part of patients body such as an earlobe or a finger or toe. The light passes through the patients tissue, and is then measured with a photo-sensor, usually a

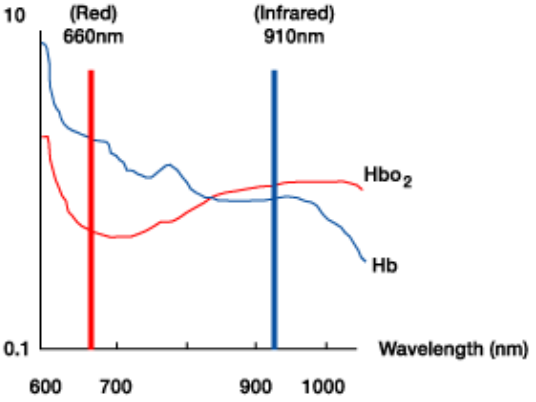


FIGURE 2.1: Absorption spectra of Hb and HbO_2.

photo-diode. Light has to travel through other tissues, such as skin, bones and muscle, but fortunately blood vessels expand and contract with the heart beat so the oximeter signal appears modulated, making it possible to effectively separate the blood transmission characteristics, an AC signal, from the transmission characteristics of the unmodulated tissue in the background, a DC signal.

The physics behind the working principle of the pulse oximeter are based on the Beer-Lambert law. Beer's law relates the transmitted and incident light through a medium that contains an absorving substance of concentration C and lenght l acording to 2.2, where I_{TRANS} and I_{INC} are the intensity of the transmitted and incident light respectively.

$$I_{TRANS}(t) = I_{INC}e^{-\varepsilon(\lambda)CL} \tag{2.2}$$

We can define the transmittance T as I_{TRANS}/I_{INC} and the absorbance A as $-ln(T)$, and we obtain the total light absorbance of blood that is given by

$$A_{bld}(t) = [\varepsilon_{HbO2}(\lambda_R)C_{HbO2} + \varepsilon_{Hb}(\lambda_R)C_{Hb}]L \tag{2.3}$$

We have stated before that the blood vessels expand and contract, so it can be established that their thickness varies, and so does the observance of the blood in them with L in 2.3. If we define R to be the ratio of relative absorbances at the red and IR wavelenghts we get,

$$\begin{aligned} R &= \frac{\ln(i_{H,R}/i_{L,R})}{\ln(i_{H,R}/i_{L,R})} \approx \frac{i_{ac}^R/i_{DC}^R}{i_{ac}^{IR}/I_{DC}^{IR}} \\ &= \frac{\varepsilon_{HbO2}(\lambda_R)C_{HbO2} + \varepsilon_{Hb}(\lambda_R)C_{Hb}}{\varepsilon_{HbO2}(\lambda_{IR})C_{HbO2} + \varepsilon_{Hb}(\lambda_{IR})C_{Hb}} \end{aligned} \tag{2.4}$$

It's known that the right-hand side of equation 2.4 is a good aproximation of the left-hand side, considering that the ac signals are very small when compared to the dc component. Whe can then combinine equations 2.1 and 2.4 to obtain

$$SpO_2 = \frac{\varepsilon_{Hb}(\lambda_R) - \varepsilon_{Hb}(\lambda_{IR})R}{\varepsilon_{Hb}(\lambda_R) - \varepsilon_{HbO2}(\lambda_R) + [\varepsilon_{HbO_2}\lambda(_{IR}) - \varepsilon_{Hb}(\lambda_{IR})]R} \times 100\% \tag{2.5}$$

The absorbances for Hb and HbO_2 are know for the red and IR wavelenghts, so it's now clear that the value that the pulse oxymeter measures is the ratio R, wich relates to SpO_2 by means of equation 2.5.

2.2 Pulse Oxymeters

Pulse oxymeters usually are comprised of two parts, a sensing probe, and a control unit. Usually the sensing probe consists of the transducer and the light sources, while the control unit takes care of the signal conditioning, data acquisition, signal processing and data display. A typical system level architecture is depicted in Fig. 2.2[1].

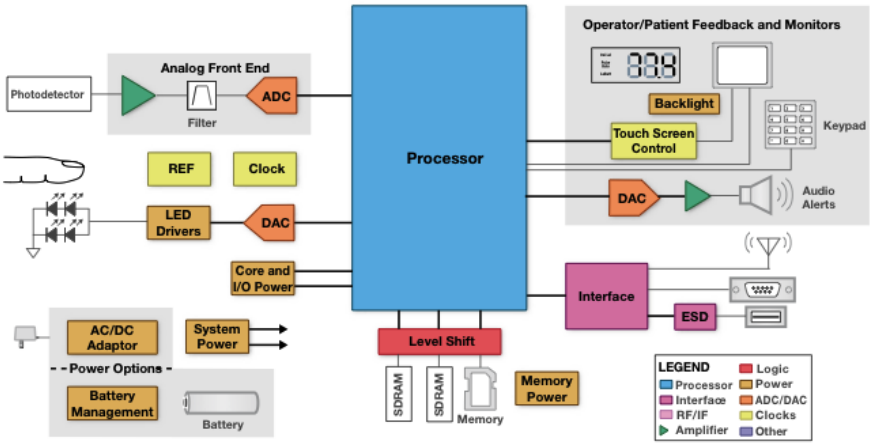


FIGURE 2.2: Pulse oximeter system block diagram from [1].

The LED's are pulsed in order to save power, while the signal of interest (the light absorbed by the patients tissue), is measured at the photodector. It's then conditioned in the analog front end, where the current signal coming from the photodetector is converted into a voltage signal, which is then filtered and converted into the digital domain in the analog to digital converter (ADC). After converted into the digital domain, discrete time

digital processing clears the signal, and computes the SpO_2 by computing the ratios of absorbance acording to the principles explained in the previous section. Note that most of the power consumption can be traced back to the the user interface and signal processing.

One big inconvenience of this type of traditional systems is that the sensing probe has to be connected via a wire to the main unit. Albeit being perfectly useful in a situation where a patient is in a hospital bed, for applications such as home care monitoring for the elderly or chronically ill, wireless medical sensing, remote monitoring of the health status of military personnel in the battlefield as well as fire-fighters engaging in fire control, and rescue missions among others, proves to be a severe constraint.

2.3 Proposed Pulse Oximeter Architecture

In contrast to the traditional pulse oxymeter architectures, the proposed work is based on an architecture where the photodetector and analog front end are separated from the data display and signal processing. This way, we can have a low power probe, that uses a small battery attached to the patient, while a device such as a smart phone is connected wirelessly to the probe and handles the power consuming signal processing and data display. The architecture for the proposed pulse oxymeter front-end is depicted on Fig. 2.3. By decoupling the analog front end from the rest of the circuit, a low power solution can be obtained, while it's expected that by integrating the photodetector with the analog front end might lead to reduced cost's, and greater usability. This comes from the fact that no wires are needed for the sensor itself.

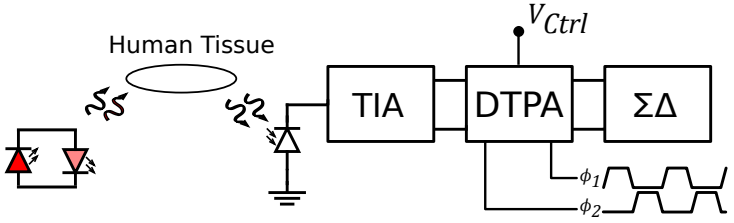


FIGURE 2.3: Pulse oximeter architecture.

The light sources to be used are two LED's, one IR and one red, in anti-parallel so that they can be easily switched on one at a time. The transducer is a photodiode that converts the incident red an IR lights into a current. This current is then amplified and converted into a voltage in the TIA, and then further amplified while being sampled and held in the discrete time parametric amplifier (DTPA). The output of the DPTA is then fed to

the ADC, and once the signal is in the digital domain it can finally be sent wirelessly to a remote device for signal processing. This device can be a bluetooth capable smart phone, that can easily log the patients status for a long time. By using this architecture, several other sensors can be used to create wearable integrated remote monitoring device for medical applications by using time division multiplexing in order for the ADC and wireless module to be shared with the rest of the sensors.

2.3.1 Integrated Photodiode

In order to convert light signal into an electrical signal some sort of transducer must be used. The photodiode is a type of photodetector that converts a light signal into a current signal. Like a normal diode a photodiode consists of a p-n junction. When a photon of sufficient energy is absorbed in the photodiodes p and n regions an electron-hole pair is generated. Although in the bulk region these electron hole pairs have a high chance of recombining, in the depletion region and a a diffusion width on either side of it, the existing electric field quickly sweeps the electrons to the n side and the holes to the p side. This creates a photocurrent, which is proportional to the incident light. Any p-n junction is a potential photodiode, this is the reason why devices containing p-n junctions are encapsulated in opaque packages in order to prevent any photocurrent induced malfunctions. With careful design, one can implement a photodiode in the same die as the rest of the circuit, resulting in a more compact and cheaper monolithic approach. In the past several work has been done in the area of integrated photodiodes in standard CMOS technologies, namely for CMOS image sensors [5], optic communications [2], and others. One example of an integrated photodiode can be seen in Fig. 2.4 [2], where a photiode for optical comunications is integrated in the same die as the TIA.

Typically a photodiode can be modelled as a current source in parallel with a capacitance [6]. This capacitance is usually high, and is biasing dependent. Typical values for capacitances are in the order of pF for a device of $50\,\mu m \times 50\,\mu m$ [7]. Although this capacitance is dependent on the technology used, PD size and biasing [7], for this work a input capacitance of 1 pF is assumed for design and simulation, knowing that although this it is not an accurate value, is of the expected order of magnitude of the real capacitance according to the literature [7][8] . The current output of the photodiode is also highly dependent on its surface area [7]. For this work it's assumed that the photodiode outputs a current between $0.1 - 10\,\mu A$. The sizing of the photodiode is outside the scope of this work, and it should be done according to this output current specification.

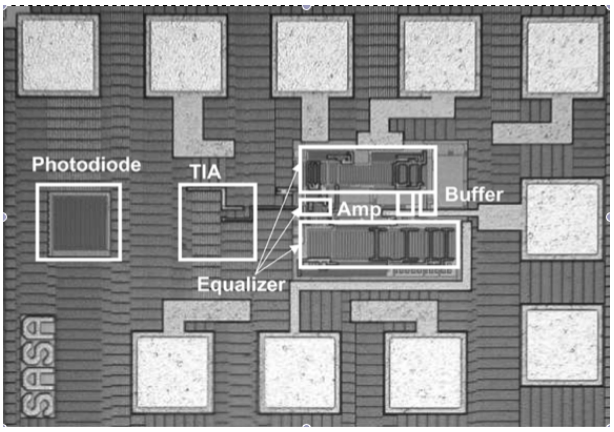


FIGURE 2.4: Chip microphotograph of integrated photodiode and preamplifier in standard CMOS [2].

2.3.2 Transimpedance Amplifiers

Traditionally amplifiers sense voltages at their input and amplify them in their output. Other types of amplifiers also exist, namely amplifiers that sense currents and output voltages. This "current-voltage" amplifiers are effectively a current controlled voltage source (CCVS) and are commonly know as transimpedance (TIA) amplifiers. Ideally the input impedance should be zero much like an ideal current meter. Likewise the output impedance should also be zero as in a ideal voltage source. The transimpedance gain is then defined as $R_o = v_{out}/i_{in}$.

2.3.3 Discrete Time Parametric Amplifier

Parametric amplifiers work by the change of a parameter within the amplifier. In this particular case, amplification is made through the variation of a sampling capacitor. This can be simply described by taking the equation for the charge in a capacitor, given by $Q = C \cdot V$. If we can vary the capacitance from an initial value C_1, to a lower value C_2 while conserving the charge in the capacitor we can obtain a gain expressed as:

$$A_v = \frac{V_o}{V_{in}} = \frac{C_1}{C_2} \tag{2.6}$$

In [3] an aproach is proposed, where the capacitor can be replaced by MOS transistor connected to work as a varactor. Note that besides the noise involved in the sampling process the amplification itself is ideally noiseless [9]. Theoretically, if the value of the

initial or final capacitance could be varied, one could obtain a variable gain. In the proposed circuit presented in the next chapters this possibility is pursued further.

2.4 Noise

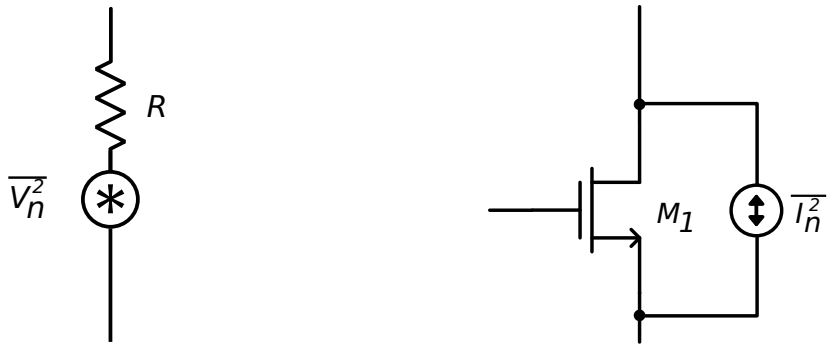
In electronic circuits, we consider noise to be a random unwanted signals. This signals are generated in electronic devices due to different physical phenomena. Noise in electronic circuits comes from the fact that charge is carried in discrete amounts equal to an electrons charge [10][11]. These small fluctuations of charge create small fluctuations in the current and voltage at the macroscopic level that are perceived as noise. Although the presence of noise in electronic circuits can be desired and useful, such as in some oscillators, usually noise limits the circuits performance. When dealing with low power signals, it's crucial that the noise is not of the same order of magnitude as the signal itself, otherwise that would make the two signals indistinct. Noise also limits the upper limit of an amplifiers gain to V_{dd}/v_n where V_{dd} is the supply voltage and v_n is the noise floor at the input of the amplifier [11]. A gain larger then V_{dd}/v_n would simply saturate the transistor, leaving no output dynamic range for the input signal. Although noise is by definition a random signal in the time domain, its average power and frequency spectrum can be quantified. In this section two of the most common noise sources in CMOS transistors are described.

2.4.1 Thermal Noise

In every conductor at a temperature different then 0 K there is a random motion of electrons. This random motion creates what is usually referred to as thermal noise. In a resistor the noise generated by thermal noise can be expressed as [12][10]

$$\overline{v_{nRes}^2} = 4kTR\Delta f \tag{2.7}$$

where T is the absolute temperature in Kelvin, k is the Boltzmann constant and Δf is the bandwidth of the system. Note that noise power is usually referred to a normalize 1 Hz bandwidth, so the Δf term is sometimes omitted. The thermal noise power is frequency invariant, so the thermal noise has a flat power spectral density (PSD). It's because of this flat PSD that thermal noise is also referred to as white noise. As shown in Fig.2.5(a) (a) thermal noise in a resistor can be modelled by a voltage source in series with the resistor.



(a) (b)

FIGURE 2.5: Models of the thermal noise in a resistor (a) and a MOS transistor (b).

The same phenomena that occurs in resistors, also occurs in a MOS transistor conducting channel. Usually thermal noise in a MOS transistor is modelled with a current source between drain and source as can be seen inf Fig.2.5(b) (b). It can be proved that for long channel MOS devices in the saturation region the thermal noise in the transistor channel can be expressed as [12],

$$\overline{v_{nMOS}^2} = 4kTgm\gamma\Delta f \tag{2.8}$$

where T and k are the absolute temperature and Boltzmann constant respectively, Δf is the bandwidth of the system, gm is the transistors transconductance and γ is the noise excess factor (NEF). For long channel devices the NEF can be derived to be equal to 2/3 but it's higher for submicron transistors [12].

2.4.2 Flicker Noise

Another type of noise is also present in MOS transistors. Flicker noise is thought to be caused by the impurities in the interface between the gate oxide and the silicon substrate. Unlike the thermal noise flicker noise power can't be predicted easily [12], and it's quantification is still largely based on empirical considerations [11]. Flicker noise has a PSD of $1/f^n$ with $n \approx 1$. In Fig.2.6 the total noise power (flicker and thermal noise) of a MOS transistor is presented. One can see that until the corner frequency f_c the flicker noise is dominant, but for higher frequencies it can be neglected.

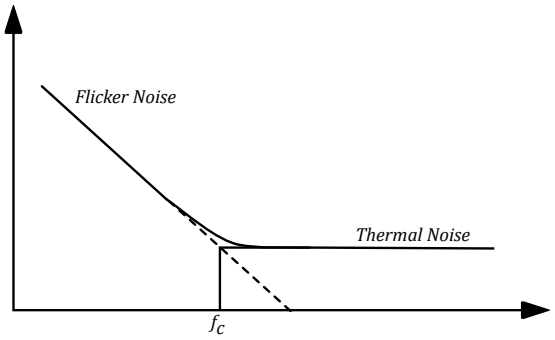


FIGURE 2.6: PSD of the total noise in a transistor (flicker noise and thermal noise)

Flicker noise is modelled by a voltage source in series with the transistor gate with a power roughly given by [12]

$$\overline{v_{nf}^2}_{MOS} = \frac{K}{C_{ox}WL}\frac{1}{f^n} \tag{2.9}$$

where K is a process dependent constant, C_{ox} is the gate oxide capacitance per unity area, and W and L are the transistors width and length respectively. Cleaner fabrication processes result in lower values for K, and thus in lower flicker noise values. Also PMOS transistors have lower K values then NMOS transistors, and thus have less flicker noise.

2.5 Transimpedance Amplifier Topologies

In this section, a brief analysis of three common TIA's is presented. Simple equations for the transimpedance gain, input impedance are derived, as well as equations relating to the noise performance of the TIA's.

2.5.1 Feedback Transimpedance Amplifier

The feedback TIA is commonly used in optoelectronic integrated circuits [13]. It consists of an operational amplifier (OA) with feedback shunt-shunt feedback topology as illustrated in Fig. 2.7.

If we assume the op-amp in Fig. 2.7 to be ideal, we know that it's negative input voltages tends to zero. This translates into a very low input impedance (ideally zero). Considering

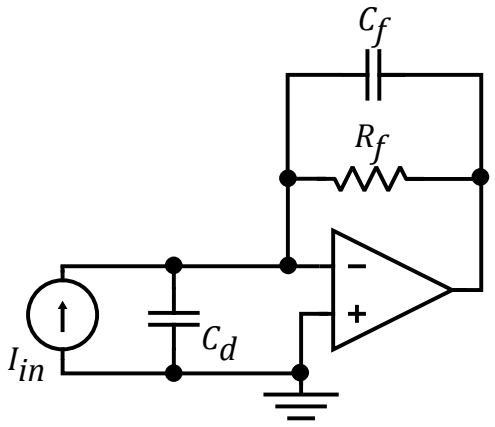


FIGURE 2.7: Shunt feedback transimpedance amplifier.

that the gain of the opamp is very high and frequency independent we can write

$$\frac{V_o}{Z_f} = I_{in} \tag{2.10}$$

where Z_f is the feedback impedance given by $R_f//\frac{1}{sC_f}$. By this means we can achieve a high tranimpedance gain, while maintaining a very low input impedance. Considering that the OA has a dominant pole as in [14] it's transfer function is given by equation 2.11. and it's GBW is given by equation 2.12

$$A(s) = \frac{A_0}{1 + s\tau_a} \tag{2.11}$$

$$B = A_0\omega_a = \frac{A_0}{\tau_a} \tag{2.12}$$

We know that the voltage in the negative input of the op-amp is given by $V_o(s)/A(s)$ we can write the Kirchhoff current law (KCL) to the input node thus obtaining

$$\frac{V_o(s) - \frac{V_o(s)}{A(s)}}{Z_f} + I_{in}(s) - \frac{\frac{V_o(s)}{A(s)}}{s}C_d = 0 \tag{2.13}$$

Rearranging equation 2.13 and rewriting the op-amp transfer function $A_(s)$ with equations 2.11 and 2.12 we can then obtain the transimpedance function of the feedback TIA.

$$\frac{V_o(s)}{I_{in}(s)} = -\frac{R_f}{s^2R_fC_dB^{-}1 + sR_f(C_f + \frac{C_d}{A_0}) + 1} \tag{2.14}$$

Since we know that the voltage at the input node is given by $\frac{V_o(s)}{A(s)}$ we can derive the input impedance.

$$\frac{V_o(s)}{V_{in}(s)} = A(s) \Leftrightarrow \frac{V_o(s)}{I_{in}(s)Z_{in}(s)} = A(s) \Leftrightarrow Z_{in} = \frac{V_o(s)}{I_{in}(s)}\frac{1}{A(s)} \tag{2.15}$$

$$Z_{in}(s) = -\frac{R_f}{s^2 R_f C_d B^{-}1 + sR_f(C_f + \frac{C_d}{A_0}) + 1} \cdot \frac{1}{A_0} + sB^{-1} \tag{2.16}$$

While studying the feedback TIA it's also important to have some insight into it's noise performance. For this study we will assume that the noise generated in the opamp can be modelled by a voltage source in series with the input of the amplifier. Note that the opamp can be designed in a way that dominant noise contribution is originated in the input transistor and that it's contribution to the total noise can be shown to be dominant over the feedback resistors noise [14]. Thermal noise in a MOS transistor can be modelled by a current source between source and drain and flicker noise by a voltage source in series with the gate [12]. In order to simplify the analysis we can transform the thermal noise current into a equivalent voltage in series with the gate. Taking the equations for thermal and flicker noise already presented in the previous section, we get the equivalent input noise voltage of the opamp to be,

$$\overline{v_{na}^2} = 4kT\gamma gm^{-}1 + \frac{K}{C_{ox}WL} \cdot \frac{1}{f}, \tag{2.17}$$

where k is the Boltzmann constant,γ is a channel length dependant coefficient, K is a process dependent constant, and $C_{ox}WL$ is the gate capacitance [12].

The noise transfer function for the feedback is derived in [14] and is given by

$$N(s) = \frac{V_{no}}{V_{na}} = -\frac{1 + sR_f C_d}{s^2 R_f C_d B^{-1} + sR_f(C_f + \frac{C_d}{A_o}) + 1} \tag{2.18}$$

In order to minimize the thermal noise high values of gm are required acording to equation 2.17. This can be obtained at the cost of either die area, using very wide transistors (high W/L) or high currents. Note that high area transistors also lower the flicker noise. Since the application devised in this work is battery operated, a low current design is preferred.

Note that the complexity and area needed for a good performance opamp could lead to an increased cost.

2.5.2 Common-gate Trasimpedance amplifier

Another basic TIA topology commonly used is the common-gate (CG) stage presented in Fig. 2.8, where I_{B1} and V_{Bias} are a bias current and voltage, respectively. This topology is know for it's low input impedance and broadband [6]. Since the input current at the transistors source equals the output current at the transistors drain, ideally the transimpedance gain would be equal to R_x. Intuitively the common-gate stage acts as a current buffer, while the I-V conversion is performed at the output by the load resistor R_x. It's then important to know it's input impedance.

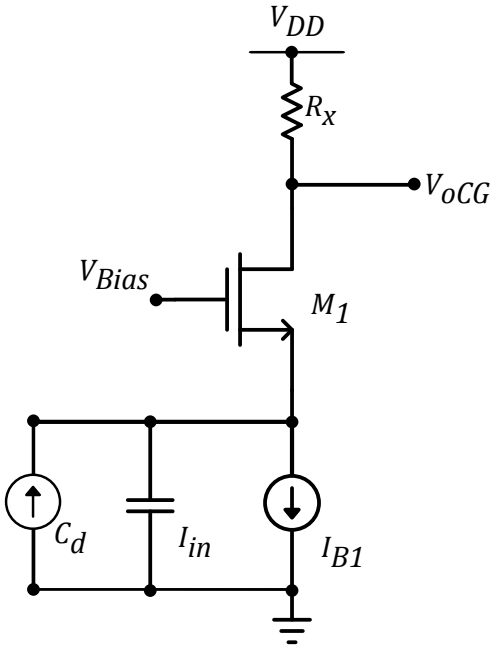


FIGURE 2.8: CG transimpedance amplifier stage.

By observing the small signal equivalent in Fig. 2.9 and disregarding the parasitic capacitances, noting that the bulk and gate are tied to ground we can write

$$V_{in} = -v_{gs} = v_{sb} = v_s \tag{2.19}$$

$$I_{in} = \frac{V_{in} - I_{out}R_x}{r_o} - (gm + gm_b)v_{gs} \tag{2.20}$$

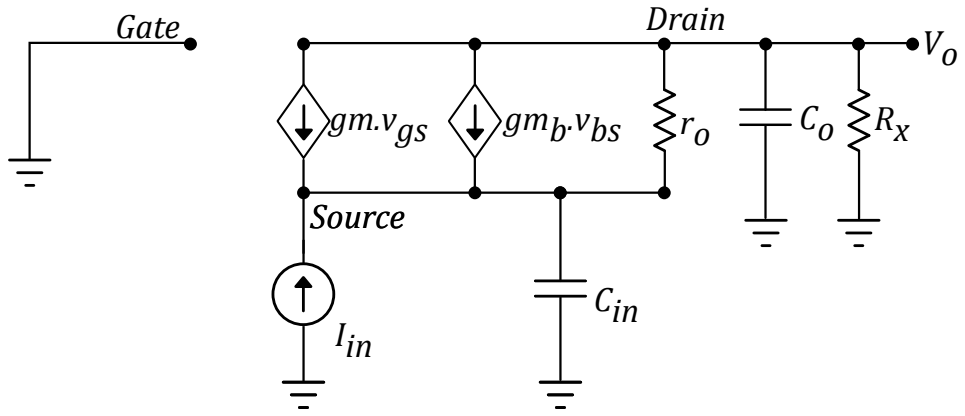


FIGURE 2.9: CG transimpedance amplifier stage small signal model.

By combining equations 2.19 and 2.20 and having $Z_{in} = V_{in}/I_{in}$ we obtain the input impedance for low frequencies to be given by

$$Z_{in} = \frac{r_o + R_x}{1 + (gm + gm_b)r_o} = \frac{1}{\frac{1}{r_o} + gm + gm_b}\left(1 + \frac{R_x}{r_o}\right) \tag{2.21}$$

From equation 2.21 some considerations can be made. First, note that input impedance depends on the load R_x, divided by r_o. Since r_o is usually very high, for low gain amplifiers where R_x is relatively small we can approximate $Z_{in} = 1/(gm + gm_B)$ as in [14]. For high gain amplifiers and sub-micron technologies, where r_o and R_X can be of the same order of magnitude this relation between gain and input impedance must be taken into account. The body effect effectively lowers the input impedance. Also note that the output impedance of the biasing current source wasn't considered because it's high compared with the CG input impedance, with which it's in parallel. Since the gate and bulk are booth tied to ground, one can easily generalize equation 2.21 for high frequencies. By replacing R_x with $R_x // \frac{1}{sC_D}$ where C_D is the total capacitance in the drain node ($C_D = C_{db} + C_{gd} + C_X$) and then making the parallel of this modified input impedance with $\frac{1}{sC_S}$ where C_S equal to the total capacitance in the source node ($C_S = C_s + C_{gs} + C_{sb}$) we obtaining equation 2.22.

$$Z_{in}(s) = \frac{sR_x r_o C_D + R_x + r_o}{s^2 R_x r_o C_D C_S + sR_x(C_D + C_S + (gm + gm_b)r_o C_D) + sr_o C_S + (gm + gm_b)r_o + 1} \tag{2.22}$$

By combining the voltage gain and the the input impedance, the transimpedance function can be obtained. Equation 2.23 is the common-gate voltage gain $V_{out}(s)/V_{in}(s)$ derived from [12].

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_x(r_o(gm + gm_b) + 1)}{sR_x r_o C_D + R_x + r_o} \tag{2.23}$$

Since the numerator of 2.22 and denominator of 2.23 cancel out, it's straightforward to obtain the transimpedance function $A(s)$ in equation 2.24. Note that as stated before, for low frequencies the tranimpedance gain equals R_x ,

$$A(s) = \frac{R_x(r_o(gm + gm_b) + 1)}{s^2 R_x r_o C_D C_S + sR_x(C_D + C_S + (gm + gm_b)r_o C_D) + sr_o C_S + (gm + gm_b)r_o + 1}. \tag{2.24}$$

In the common-gate TIA there are three noise current sources relating to the thermal noise of the common-gate transistor, the noise in the drain resistor R_x and the noise of the bias current I_B. It can be shown that the noise contribution of the common-gate transistor is dominant and has a noise transfer function given by [14]

$$\frac{V_{no}}{I_n(s)} = -\frac{R_x}{gm * R_{ob}} \frac{1 + sR_{oB}}{(1 + sgm^{-1}C_S)(1 + sR_x C_D)} \tag{2.25}$$

Although from equation 2.25 the noise might appear to decrease with gm because it's in the denominator, if we consider the total integrated output noise the effect of the reduction of the bandwith with a decrease in gm is actually dominant as proved in [14]. So in order to decrease the total output noise a lower gm is required, which conflicts with the need to have a high gm in order to obtain a low input impedance.

2.5.3 Regulated Common Gate Transimpedance Amplifier

The regulated common gate (RCG) stage presented in subsequent Chapter is a widely known TIA, with applications in many optical receivers [8]. Note that the RCG is also referred to as Regulated Cascode (RGC) in the literature. Although the RCG and RGC are effectively the same circuit, the same way that single-stage amplifiers have different names depending on where the input/output is taken so should this circuit. The RCG

name will be used trough out this work since it better reflects the working principle of this amplifier.

The RCG consists of a common-gate stage with gm boosting [15] which, boost's the transconductance of the input transistor by a factor of $(A+1)$, where A is the gain of the feedback loop. Compared to the CG stage, the RCG allows for a lower input impedance for the same bias current in the input transistor, which relates to a higher bandwidth, and potentially a better noise performance. Because the input transistor dominant noise source, which depends on its gm, is no longer tied to the input impedance/bandwidth determination as in the common-gate TIA, an extra degree of freedom is given to the designer to optimize the circuit. Since the proposed TIA is based on the RCG topology, it will be studied in detail in the following Chapter.

Chapter 3

Regulated Common Gate Stage

The regulated common gate (RCG) stage presented in Fig. 3.1 is a widely known TIA. It derives from the CG, in which, a gm boosting technique that consists of a local feedback loop is applied. In this Chapter, an intuitive explanation of how the RCG works is done besides a more in depth analysis of the key parameters of the RCG TIA. Transimpedance gain, input impedance and noise performance is studied. The derived equations are validated by simulation.

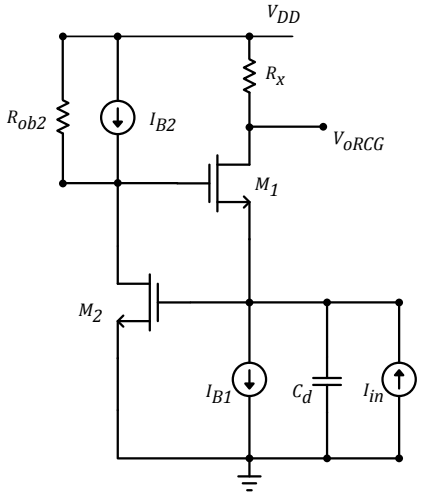


FIGURE 3.1: Regulated Common Gate Stage.

3.1 Working Principle

The RCG TIA, derives from the CG TIA. By applying a local feedback loop the RCG is capable of a lower input impedance then the CG stage with the same input transistor bias current and thus the same gm. This effectively increases the bandwidth by moving the input pole into higher frequencies while maintaining a good noise performance.

The effect that the source degeneration has in increasing both input and output impedance by a factor of $1 + gmR_S$ is well known. This feedback mechanism can be intuitively understood if ones thinks of a transistor as a transconductance amplifier as in Fig.3.2, where the output current is equal to the negative input current.

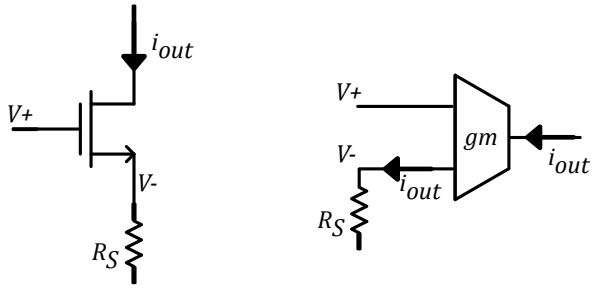


FIGURE 3.2: Feedback mechanism in source degeneration.

The source resistance effectively generates a series-series feedback loop by converting the output current into a voltage, while it's applied to the negative input of the transconductance amplifier. By using this principle with an active load we obtain the regular cascode circuit. This same concept can be applied to the common gate amplifier using an active feedback loop as depicted in Fig.3.3(a). This feedback loop then has the effect of decreasing the input impedance. In order to obtain negative feedback, a CS stage is used thus obtaining the circuit in Fig. 3.1.

By taking the simplified small signal equivalent in Fig.3.3(b) we can derive the approximate input impedance and transimpedance gain of the RCG. By observing the small signal circuit we can write

$$v_{gs} = -A \cdot v_{in} - v_{in} = -(A+1)v_{in} \tag{3.1}$$

$$i_{in} = i_{in} = (A+1)v_{in}gm_1 \tag{3.2}$$

Since $R_{in} = v_{in}\ i_{in}$ we obtain

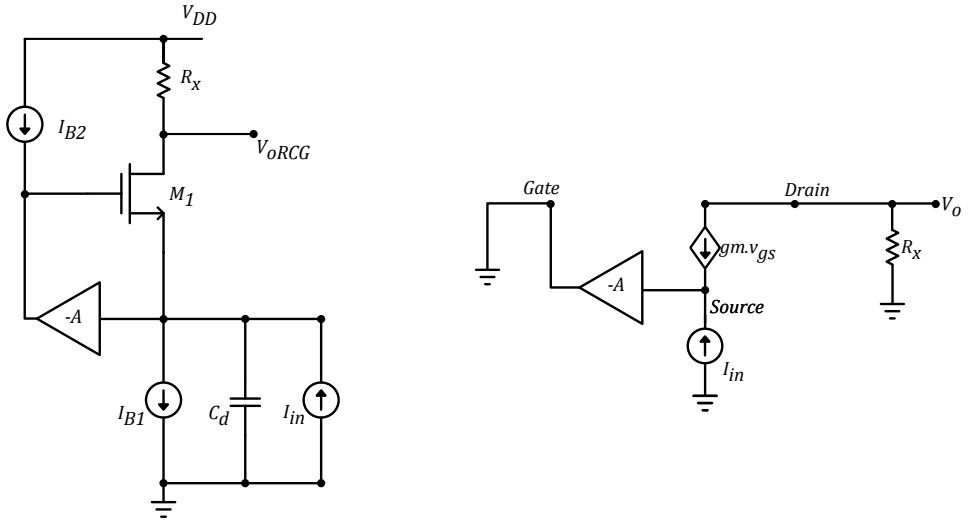


FIGURE 3.3: (a) Common Gate stage with local feedback and (b) it's small signal equivalent.

$$Z_{in} = \frac{1}{(A+1)gm_1}. \tag{3.3}$$

Compared to the CG stage, the input impedance is now A times smaller. In regards to the transimpedance gain, it's easy to see that the input current is the same as the output current. Like the CG stage the RCG effectively works as a current conveyor, where the current-voltage conversion is accomplished in the load resistor R_x.

3.2 Frequency Response of the RCG

In the small signal equivalent circuit in the previous chapter, the transistors output resistance was discarded, as well as all the capacities present. If we take into account all the capacities involved we obtain the small circuits circuit in Fig. 3.4 where C_{in} is the sum of the photodiode capacitance and the transistors parasitic capacitance C_{sb}, and C_o is equal to a load capacitance plus C_{db}.

The gain $-A$ in the Fig. 3.4 is obtained via a CS gain stage so for low frequencies it is approximately equal to

$$A_{vCS} = -gm_2 \frac{r_{o2} R_{ob2}}{r_{o2} + R_{ob2}} \tag{3.4}$$

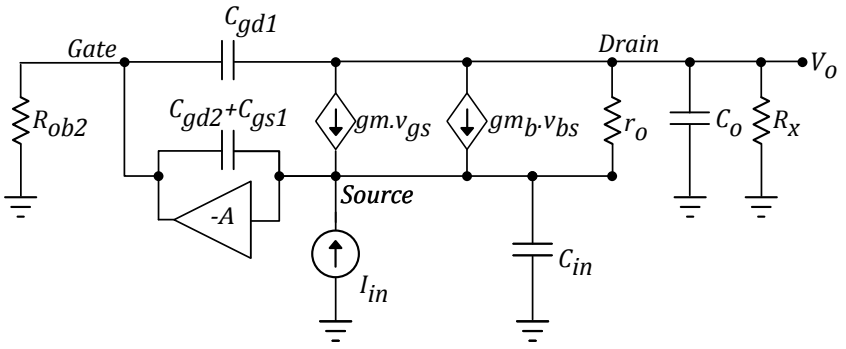


FIGURE 3.4: RCG stage small signal equivalent circuit.

If we look into the small signal equivalent we can write the total input capacitance by taking the miller effect into acount, and thus obtaining

$$C'_{in} = C_{in} + (1+A)(C_{gs} + C_{gd2} + C_{gs1}) = C_d + C_{sb} + (1+A)(C_{gs} + C_{gd2} + C_{gs1}) \quad (3.5)$$

3.2.1 Input Impedance

The impedance of the total input capacitance, C'_{in}, is in parallel with the input impedance for small signals. For simplicity we will disregard the input capacitor, and then add its contribution in the end. We can then write the input current to be given by equation

$$I_{in} = -gm_1 V_{gs} - gm_b V_{bs} + \frac{1}{r_o 1}(V_{in} - (R_x//C_o)I_{in}) \quad (3.6)$$

We can then write $V_{gs} = -(A+1)V_{in}$, so comparing to the CG stage, where $V_{gs} = V_{sb}$, in the RCG $V_{gs}$is $(A+1)$ times bigger then V_{sb}. Since gm_b is already smaller then gm, the current caused by the body effect can be neglected. We can now write

$$I_{in}\left(1 + \frac{R_x}{(sR_xC_o+1)r_o}\right) = V_{in}\left[(A+1)gm_1 + \frac{1}{r_o}\right] \quad (3.7)$$

and from there obtain the following equation for the input impedance without considering the input capacitance

$$Z'_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{(A+1)gm_1 + \frac{1}{r_o}} + \frac{\frac{R_x}{(sR_xC_o+1)r_o}}{(A+1)gm_1 + \frac{1}{r_o}} \quad (3.8)$$

Now we just have to make $Z'_{in}//\frac{1}{sC'_{in}}$ to obtain the input impedance.

3.2.2 Transfer Function

As noted before, the input current is divided between the input impedance, and C'_{in}. Noting that we are dealing with a current divider, the incremental source current in M_1 can then be expressed as

$$I_{s1} = \frac{1/sC'_{in}}{Z'_{in} + 1/sC'_{in}} I_{in} = \frac{1}{1 + sZ'_{in}C'_{in}} I_{in} \tag{3.9}$$

which can be written in the form $\frac{1}{1+s\tau_1} I_{in}$ where $\tau_1 = Z'_{in}C'_{in}$. This current flows through the output impedance $Z_x = \frac{R_x}{1+sR_xC_o}$. Whe can then write the approximate transimpedance function to be given by

$$\frac{V_o}{I_d} \approx \frac{R_x}{(1 + sC'_{in}\frac{1+\frac{R_x}{(sR_xC_o+1)r_o}}{(A+1)gm_1+\frac{1}{r_o}})(1 + sR_xC_o)} \tag{3.10}$$

3.2.3 Considerations about stability

The approximate transfer function derived before could lead one to believe that this RCG is always stable, but because it has a feedback loop, the stability of the amplifier should be studied. From the approximations made, the transfer function has two poles, at the input and output, while the loop gain only has one pole. This might lead one to believe that the system is intrinsically stable, because the maximum phase shift in a 1 pole system is 90°, thus meeting the criteria for a stable system that the loop gain must be lower then unity when the phase has shifted by 180°. However the common-source stage used in the loop gain has two poles. This third pole can be traced back to the node at the gate of the input transistor. This pole is approximately given by

$$\tau = (R_{ob2}//r_{o2}) \cdot \left[(C_{gd2} + C_{gs1})(1 - A^{-1}) + C_{db2}\right] \tag{3.11}$$

where some capacities are multiplied by the Miller effect.

In [16] it's suggested that this pole has to be in a frequency at least three times higher then the frequency in which the loop gain is lower then one. This should allow for a phase margin of 72°, which should guarantee there is not any overshoot in the time domain [16].

3.3 Noise

For the noise analysis we will first determine the noise voltage spectral density at the output. For wideband circuits the flicker noise can be neglected [14]. Since in pulse oximetry the signals involved are low frequency by nature, flicker noise should be considered. In Fig. 3.5 all the noise sources of the RCG stage are represented.

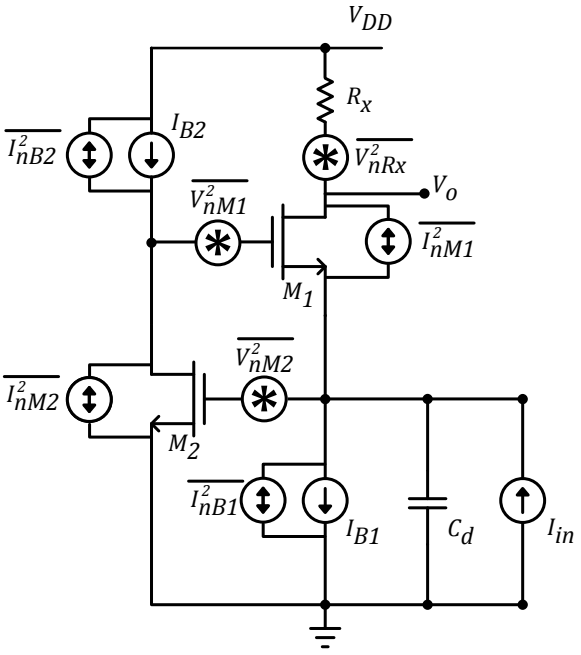


FIGURE 3.5: RCG stage with noise sources.

3.3.1 Thermal Noise

The noise sources present in Fig. 3.5 are related to the thermal and flicker noise. We will first consider the thermal noise sources, generated by the current sources $\overline{I^2_{nB1}}$, $\overline{I^2_{nB2}}$, $\overline{I^2_{nM2}}$ and $\overline{I^2_{nM1}}$, and voltage source $\overline{V^2_{nRx}}$.

3.3.1.1 I_{B1} current source

The noise contribution of the input transistor biasing current source is given by $\overline{I_{nB1}^2}$. It can be seen in Fig. 3.5 that it is in parallel with the input current, so it's noise transfer function, V_{no}/I_{nB1} is equal to the RCG transfer function given by 3.10. The noise contribution to the total output noise can then be expressed as

$$\overline{V_n^2 Out, B1} = \overline{I_{nB1}^2} \cdot \left| \frac{R_x}{(1 + sC'_{in} \frac{1+\frac{R_x}{(sR_xC_o+1)r_o}}{(A+1)gm_1+\frac{1}{r_o}})(1 + sR_xC_o)} \right|^2 \tag{3.12}$$

3.3.1.2 Regulaton transistor and I_{B2} current source

In the small signal equivalent, where V_{dd} is short-circuited to ground, the noise currents generated by the regulation transistor, M_2, and given by $\overline{I_{nM2}^2}$, and the noise from the biasing current source I_{B2}, given by $\overline{I_{nB2}^2}$ are in parallel, so they share the same noise transfer function.

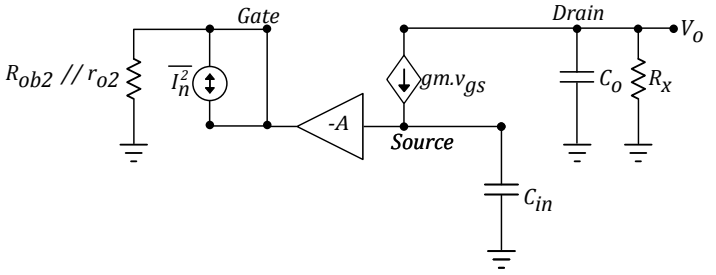


FIGURE 3.6: Small signal equivalent with I_{B2} and M_2 noise source.

By taking the simplified small signal circuit in Fig. 3.6 we can derive the noise transfer function. We start by writing the straightforward voltages at the gate, source and drain of the transistor thus obtaining the following equations.

$$V_g = -AV_s + I_n R_{ob2}//r_{o2} \tag{3.13}$$

$$V_s = gmV_{gs} \frac{1}{sCin} \tag{3.14}$$

$$V_o = gmV_{gs} \frac{R_x}{sR_xC_o} \tag{3.15}$$

Combining equations 3.13 and 3.14 we can write I_n as follows

$$I_n = \frac{V_{gs} s C_{in} + gm V_{gs}(A+1)}{s C_{in} R_x} \tag{3.16}$$

We can obtain the noise transfer function by dividing equations 3.15 by 3.16 thus obtaining the noise transfer function V_{no}/I_n bellow.

$$\frac{V_{no}}{I_n} = \frac{s\frac{R_{ob2}//r_{o2} R_x C_{in}}{(A+1)}}{(s\frac{C_{in}}{gm(A+1)} + 1)(sR_x C_o + 1)} \tag{3.17}$$

3.3.1.3 Input transistor

We will now analyse the effect of the input transistors thermal noise. Note that in the common-gate stage, this was the dominant noise source.

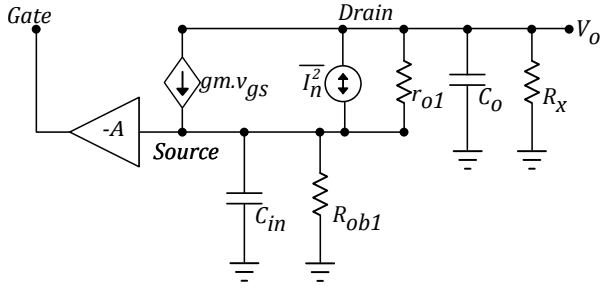


FIGURE 3.7: Small signal equivalent with M_1 noise source.

Using the small signal circuit in Fig. 3.7 we will now derive the noise transfer function. We can write the voltage at the output node as

$$V_o = \frac{R_x}{sR_x C_o + 1}\left[gm_1(A+1)V_s + \frac{V_s - V_o}{r_{o1}} + I_n\right] \tag{3.18}$$

$$V_o\left(1 + \frac{R_x}{(1+sR_x C_o)r_{o1}}\right) = \frac{R_x}{1+sR_x C_o} \cdot (I_n + gm_1(A+1)V_s) \tag{3.19}$$

where V_s is the voltage at the source node, and in equation 3.19 we have taken into acount that $gm_1(A+1) >> 1/r_{o1}$. Since the current at the output node is the same as the current in the input, we can write V_s in terms of V_o so we have

$$V_s = V_o \cdot \frac{sR_x C_o + 1}{R_x} \cdot \frac{R_{ob1}}{sR_{ob1} C_{in} + 1} \tag{3.20}$$

Combining equations 3.19 and 3.20 with then obtain

$$V_o\left(1+\frac{R_x}{(sR_xC_o+1)r_{o1}}-gm_1(A+1)\frac{R_{ob1}}{sR_{ob1}C_{in}+1}\right)=\frac{R_x}{1+sR_xC_o}I_n \tag{3.21}$$

We know simplify the multiplying factor of V_o in the left-hand side of equation 3.21 o obtain the the factorized equation in 3.22.

$$\frac{(sR_xC_o+1)(sR_{ob1}C_{in}+1)+R_x/r_{o1}(sR_{ob1}C_{in}+1)+gm1(A+1)R_{ob1}(sR_xC_o+1)}{(sR_xC_o+1)(sR_{ob1}C_{in}+1)} \tag{3.22}$$

In order to further simplify 3.22, we will assume that $gm_1(A+1)R_{ob1} >> R_x$ and $gm(A+1)C_x >> C_{in}/r_{o1}$. With this simplifications, and equations 3.20 and 3.21 we can then write the noise transfer function below.

$$\frac{V_o}{I_n}=\frac{R_x}{gm_1(A+1)R_{ob1}}\frac{1+sR_{ob1}C_{in}}{(s\frac{Cin}{gm_1(A+1)}+1)(sR_xC_o)} \tag{3.23}$$

Chapter 4

Balun operation and noise cancellation techniques

Differential operation has many benefits, such as reducing second-order distorion and rejection of power supply and substrate noise[17] . Many RF wideband LNA circuits have been publishing integrating the LNA and balun in the same circuit, while exploiting the noise cancellation technique proposed in [18]. This consists of a CG stage in parallel with a CS stage, as depicted in Fig. 4.1.

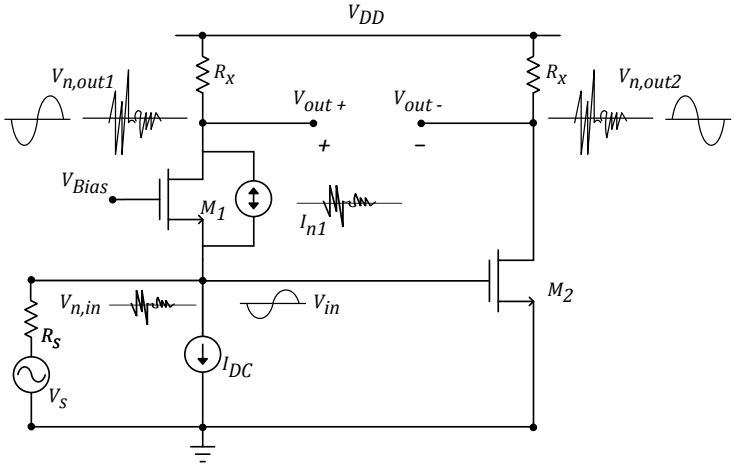


FIGURE 4.1: Basic CG-CS topology exploiting the input transistor thermal noise cancelling.

The basic principle is clearly illustrated in Fig. 4.1. The input current, I_{in}, generates a voltage , V_{in} at the input node. This voltage is given by the product of the input current and the input impedance. This voltage is then amplified on the CG stage, thus creating

a in phase output voltage V_{out+}. Since V_{in} is also amplified by the CS, at the CS output we have V_{out-} in phase opposition to V_{in} and V_{out+}. The gain can then be expressed as

$$A_{vCS} = A_{vCG} + A_{vCS} \tag{4.1}$$

which is the sum of the gain of the CG stage and the CS stage. Assuming both the CG and CS gains are matched, by taking the output as $V_{out+} - V_{out-}$ we achieve our differential output, and consequently increase the gain by 6 dB. In a analogous way, the thermal noise, represented by the current source between the source and drain of the input transistor, M_1, generates a noise voltage V_{nCG} at the output node, and an anti-phase noise voltage, V_{nIN}. When V_{nIN} is amplified by the CS stage, we obtain a noise voltage, V_{nCS}, which is in phase with V_{nCG}. The noise cancels because it becomes a common-mode signal at the differential output. Comparatively to other noise cancelling techniques employing feedback, this is a strictly feed-forward technique, so instability risks are greatly relaxed [18].

4.1 Common-Source Stage

Some considerations must be made in regards to the common-source stage being added to the circuit. The basic common-source topology is presented in Fig. 4.2.

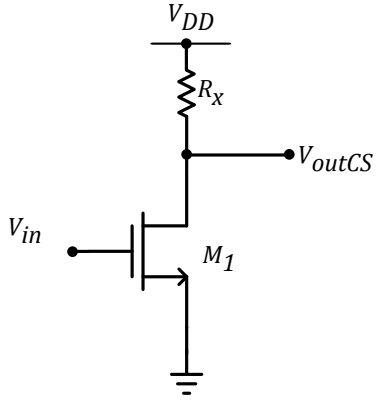


FIGURE 4.2: Common-source amplifier topology.

One of the first aspects that we should study in the CS stage is its gain. If we take the small signal model for low frequencies we can write the gain as:

$$A_{vCS} = -gm\frac{r_o R_x}{r_o + R_x} \approx -gmR_x \tag{4.2}$$

Since the photodiodes input capacitance is high and we are interested in low frequencies, the CS transistor parasitic capacitances aren't expected to degrade the bandwidth and input impedance significantly. Unfortunately, in order to obtain differential operation and noise cancelling, we are adding new noise sources which should be considered.

The flicker and thermal noise of the transistor, can be expressed as 4.3 and 4.4

$$\overline{v^2_{nf_{CS}}} = \frac{K}{C_{ox}WL}\frac{1}{f^n} \cdot (gmR_x)^2 \tag{4.3}$$

$$\overline{v^2_{ntCS}} = 4kT\gamma R_x^2 \tag{4.4}$$

Note that booth of these noise sources will be added to the total output noise in order to obtain the differential gain. Since the gain is doubled, a better noise factor can be achieved in some situations. Careful design should guarantee that the benefits of adding the CS stage aren't surpassed by the additional noise introduced.

4.2 LNA's

As said earlier, the CG-CS topology has been reported in a multiple applications for wide-band LNA's. We will now show some simple equations that allow both a balanced differential output and noise cancelling.

4.2.1 Balun Operation

To achieve the balun operation, it's crucial that booth stages have the same gain. Simple equations for the conditions in which the gain is balanced can be derived. For CG stage, we know from our previous analysis that the input and output current are the same, and as such, the output voltage is given by $V_o = R_x I_{in}$. We can then write

$$I_{in} = I_o = \frac{V_{out+}}{R_x} = \frac{R_x}{A_{vCG}} \tag{4.5}$$

where A_{vCG} is the voltage gain of the CG amplifier stage and is aproximately equal to $gm \cdot R_x$. Since the input impedance is also known to be approximately given by $1/gm_{CG}$, and for a LNA the equal the source resistance, R_S we get that the gain of the CG stage to be given by [17]

$$A_{vCG} = \frac{R_x}{Z_{in}} = \frac{R_x}{R_S} \tag{4.6}$$

Since the gain has to be balanced, but in phase opposition, the gain of the CS stage is then given by

$$A_{vCS} = -\frac{R_x}{R_S} \tag{4.7}$$

If the condition in 4.7 is met, then the LNA will have a balanced balun operation. We shall now derive the equations that guarantee that we can also cancel the thermal noise. We will now study the conditions required to cancel the thermal noise produced by the CG input transistor, modelled by the current source I_n in Fig. 4.1.

4.2.2 Noise Cancellation

In the CG-CS, the thermal noise current generates a voltage at the input node, and a fully correlated anti-phase voltage at the CG output [17]. The voltage at the input can be expressed as $V_{nIN} = \alpha_1 \cdot I_n \cdot R_S$ while the output voltage can be written as $V_{nCG} = -\alpha_1 \cdot I_n \cdot R_x$, where α_1 accounts for the the voltage division between R_S and Z_{in}, which is $1/2$ when the input is matched. In order for the noise to cancel, we must have $V_{nCG} = V_{nCS}$. We can write the output noise voltage at the CS stage as 4.8 bellow.

$$V_{nCS} = V_{nIN} \cdot A_{vCS} = \alpha_1 \cdot I_n \cdot R_S \cdot A_{vCS} \tag{4.8}$$

By replacing equation 4.7 in 4.8 we guarantee that noise cancelling and balanced balun operation are achieved simultaneously.

4.2.3 Distortion Cancelling

The proposed technique cancels all signals that can be modelled as a current source between the drain and source as such, in [18] it's shown that this can effectively cancel the nonlinearity of the input transistor, assuming it's modeled as a current source controlled by the gate. In [17] further proof is presented that all the noise and distortion currents generated by the input transistor can be cancelled. It's also shown that the gain of the CS required for the distortion products of the CG is the same required to guarantee noise cancelling and output balancing.

4.2.4 Design Considerations

From the equations derived in the previous subsections two different design options can be considered while maintaining balanced balun operation and noise cancelling.

1) The traditional way to implement the CG-CS amplifier is with balanced gains on the CG and CS. For simplicity $gm_{CS} = gm_{CG}$ and $R_{CS} = R_{CG}$

2) The transconductance of the CS stage is sized to be n times bigger than the transconductance of the CG stage, while the load resistor of the CG stage is n times smaller. This was the design option chosen in [17] to minimize the noise contribution of the CS stage. Note that for LNA applications, the CG transconductance is imposed because the input match depends on it.

In [17] it's shown that option 2) has an improved noise figure compared to option 1), as it reduces the noise of the CS stage, thus reducing the total output noise (the CG noise is already considered to be cancelled).

4.3 TIA's

Although extensively used in LNA's, the CG-CS topology hasn't, to the authors knowledge, been used in TIA's. We will know show that the same considerations made for the LNA amplifier, also apply to the TIA.

4.3.1 Balun Operation

For TIA's, we can write V_{in} as the voltage at the input node to be the product of I_{in} and Z_{in}, while $V_{out+} = R_x I_{in}$ still holds. Thus, we obtain

$$I_{in}R_x = V_{in}A_{vCS} = I_{in}ZinA_{vCS} \tag{4.9}$$

$$R_x = \frac{1}{gm_{CG}}A_{vCS} \tag{4.10}$$

If the condition in 4.10 is true, then we achieve balanced balun operation in the CG TIA.

4.3.2 Noise Cancelling

Simultaneous output balancing and noise cancellation can also be obtained in the CG TIA. It's straightforward to obtain the equality for V_{nCG} and V_{nCS}

$$A_{vCS} \cdot \frac{I_{nIN}}{gm_{CG}} = I_n \cdot R_x \tag{4.11}$$

If we replace equation 4.10 in 4.11 it's always true, so as in the LNA operation, balanced operation and noise cancelling are achieved simultaneously.

We have thus proved that any signal that can be modelled as a current source between the drain and source of the input transistor in the CG LNA or TIA can be cancelled. Although flicker noise is usually modelled as a voltage source connected in series with the gate of the transistor it can be modelled as a current source because the current in the MOS transistor is dependent on the V_{gs}. So in this circuit, besides thermal noise cancelling, we also achieve flicker noise cancelling.

4.4 Regulated Common-Gate Stage with Noise Cancelling

From the previous analysis we have shown that the RCG topology has a lower input impedance, and can be designed in order to obtain a better noise performance then the

CG stage. It's then a natural step to employ the technique explained earlier in this chapter to the RCG topology. In order to harness the benefits of differential operation, a CS stage is added in parallel to the RCG, as can be seen in Fig. 4.3. By means of the CS stage, balun operation and potential noise cancelling of the input transistor, M_1 can be achieved.

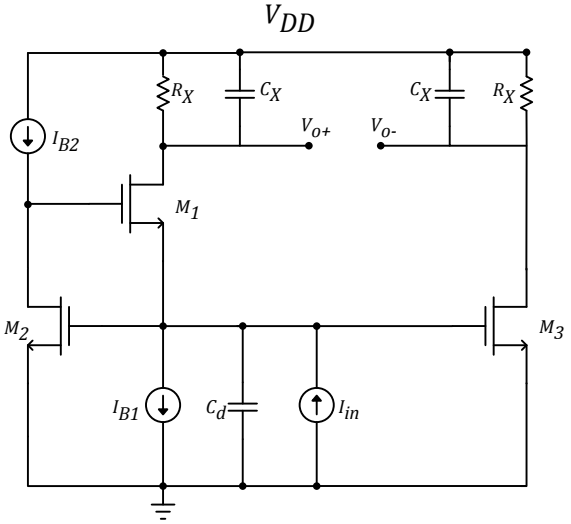


FIGURE 4.3: Balun RCG exploiting thermal noise cancelling.

4.4.1 Balun Operation

In order to guarantee a balanced balun operation, booth the voltage gains of the RCG and CS must be matched. From our previous analysis of the RCG stage, we now that the input impedance of the RCG stage can be written as $Z_{in} = 1/gm_1(A+1)$. In an analogue case to the CG-CS, for low to moderate frequencies, the RCG provides a purely resistive input impedance and we can say that the input current is equal to the RCG output current. We can then write

$$I_{in}R_x = V_{in}A_{vCS} = I_{in}\frac{1}{gm_1(A+1)}A_{vCS} \tag{4.12}$$

$$R_x gm_1(A+1) = gm_3 R_X \tag{4.13}$$

Equation 4.13 lays the condition to guarantee balanced balun operation, when booth the output resistance of the RCG and CS are equal.

4.4.2 Noise Cancelling

In the CG-CS case, simultaneous output balancing and noise cancellation could be obtained. Because the RCG is effectively a CG stage with gm boosting, the same principle applies. The thermal noise current between the drain and source of the M_1 transistor generates a voltage at the input node, and a anti-phase voltage at the RCG output. We can write these voltages as The $V_{nIN} = I_n \cdot Z_{in}$ while the output voltage can be written as $V_{nCG} = -I_n \cdot R_x$. Since $V_{nCS} = -V_{nIN} gm_3 R_x$ we can write

$$-I_n \; R_x = -V_{nIN} gm_3 R_x \Leftrightarrow \tag{4.14}$$

$$\Leftrightarrow gm_1(A+1)R_x = gm_3 R_x \tag{4.15}$$

So the same way that output balancing and noise cancelling where achieved simultaneously in the CG-CS, the same proves to be true for the RCG-CS topology. The same way that thermal noise cancelling of M_1 is achieved, so is any signal that can be be modelled by a current source between it's gate and source.

Chapter 5

Discrete Time Parametric Amplifier with Adjustable Gain

In this chapter the working principle of the Discrete Time (DT) MOS Parametric Amplifier (MPA) is discussed, as well as a brief explanation of the variable MOS capacitors (varactor) which is the basic building block of the DT MPA. The use of the DT MPA in the proposed architecture will cover the need of an extra sample-and-hold (S&H) block between the TIA and ADC while providing a virtually noiseless and controllable amplification stage.

5.1 Basic Principles of the DT MPA

A parametric amplifier is a circuit in which the amplification is achieved by using a variable (time-dependent) parameter or circuit element [9]. In this work, the variable element used is a variable capacitor or varactor. While at a first glance, the idea of varying a capacitance to achieve an amplification might sound odd, the basic working principle of the parametric amplifier is actually quite simple. It's known that the charge stored in a capacitor is given by the well known equation

$$Q = C \cdot V \tag{5.1}$$

where Q is the charge, C the capacitance and V the voltage applied to the capacitor. Then, if charge is preserved, by varying the capacity of a device, a higher or lower voltage

can be obtained. The principle operation of the circuit can be seen in Fig. 5.1. In ϕ_1 the input voltage is sampled. Then the top plate of the capacitor is disconnected and left floating while it's capacity is decreased. Finally, during ϕ_2, the amplified voltage is then passed to the output. Note that it's very important the ϕ_1 and ϕ_2 are non overlapping phases to guarantee that when the capacity is reduced, the capacitor node is floating. This is required to guarantee charge conservation from ϕ_1 to ϕ_2.

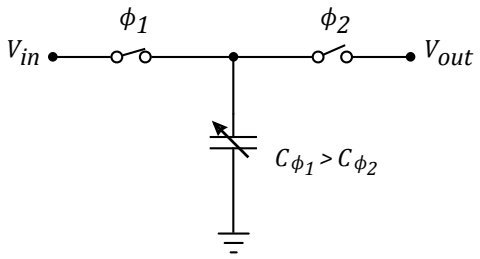


FIGURE 5.1: Principle of operation of the discrete time MOS parametric amplifier.

A first approach reveals that the gain of the amplifier might then be expressed as

$$A_v = \frac{V_o}{V_{in}} = \frac{C_{\phi 1}}{C_{\phi 2}} \tag{5.2}$$

where $C_{\phi 1}$ and $C_{\phi 2}$ are the capacitance values in the falling edges of $\phi 1$ and $\phi 2$ respectively. While this first analysis might give some insight into amplification principle, and give an idea of what to expect from the gain, one must note that the parasitic capacitances of the switches and load will lead to a reduction of the effective gain so, in reality, the gain is given by

$$A_v = \frac{V_o}{V_{in}} = \frac{C_{\phi 1} + C_p}{C_{\phi 2} + C_p + C_L} \tag{5.3}$$

In order to implement this technique, in this work we will use the same type of MOS varactor proposed in [3][9], which consists of a MOS transistor switched between two operating modes.

5.2 The MOSCAP and the three terminal MOS varactor

In order to understand how a variable gain is possible, one must first understand how and why the capacitance in a MOS structure varies, so that we can control it. In Fig. 5.2 a very simple cross section of a MOS capacitor can be seen, along with a simple equivalent circuit which consists of two capacitances in series.

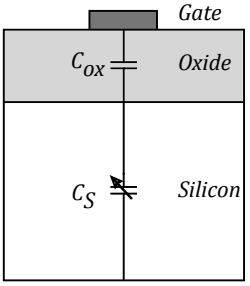


FIGURE 5.2: Simplified cross section of a MOS Capacitor showing a simple equivalent circuit.

The oxide capacitance, C_{ox} is simply a parallel plate capacitor [19]. The capacitance of a parallel plate capacitance is given by $C = \epsilon A/d$, where A is the area of the capacitors plates, ϵ is the permittivity of the oxide and d de distance between the plates. We can then write the capacitance per unit area, C'_{ox}, as

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{5.4}$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the permittivity of the oxide insulator. In the semiconductor region, charge will vary depending on the biasing of the MOS device, and that's why in Fig. 5.2 the substrate capacitance is denoted by a variable capacitance C_S. For small signals, the capacitance can be expressed by $C_S = \frac{\partial Q}{\partial V}$, so as charge distribution varies within the semiconductor structure due to the potential, so will the capacitance C_S. A theoretical plot of the capacitance in terms of gate voltage can be seen in Fig. 5.3, where the different regions of operation are clearly shown.

Because the substrate is doped, an internal potential drop forms across the gate and the substrate. We define this potential drop as the flatland voltage, V_{FB}. Note that from now on, for simplicity, we will consider the bulk to be tied to ground, and when the gate voltage is referred, in fact we are referring to the gate to bulk voltage. If a voltage is

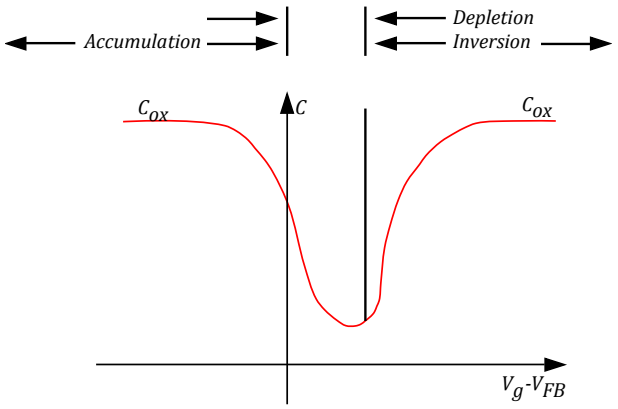


FIGURE 5.3: Typical capacitance/voltage characteristic of a NMOS capacitor.

applied to the gate that is lower then the flatband voltage, then the gate is at a potential lower then the potential at the substrate. This causes holes to accumulate at the top of the substrate and electrons to accumulate at the bottom of the gate. This increase in holes/electrons is linear. This is the type of behaviour that is to be expected from a parallel plate capacitor, so in accumulation the capacitance is given by C_{ox}.

When $V_{FB} < V_g < V_t$, where V_t is the threshold voltage of the device, we say the capacitor is in depletion region. In this region, besides de oxide capacitance, C_{ox}, there is a depletion region, and thus a depletion capacitance given by $C = \frac{\partial Q}{\partial V}$. The depletion region will have a width that is dependent on the bias, does varying the capacitance. As the bias voltage V_g increases, so does the depletion width, and with it there is a decrease in C_S. Note that this capacitance appears to be in series with C_{ox}, which is constant. Like is the case for parallel resistances, for capacitors in series, the total equivalent capacitance approaches the value of the smaller capacitance, so as C_S decreases, so does the total capacitance.

Inversion occurs when $V_g > V_t$. In this case, the concentration of electrons at the top of the substrate, is such that the p-type semiconductor becomes inverted. In this inversion layer, the concentration of electrons is such, that the p-type silicon acts as n-type silicon, hence why we say it's inverted. Once the device is in inversion, the depletion region reaches it's maximum width, and the increase in the gate charge relates to only an increase in the electrons in the inversion layer. Since the with of the depletion region doesn't increase no matter what happens to V_g, then the derivative $C_S = \frac{\partial Q}{\partial V}$ is always zero. Since C_S is zero, then the total equivalent capacitance is ,like in the accumulation region, only equal to C_{ox}

In order to harness the possibility to vary the MOS capacitance, in a typical application

a large control signal would be required, with a small signal over it. In this case since booth the large controlling signal and the control voltage booth face the same capacitance the input signal amplitude is very limited [9]. By using the three-terminal MOS varactor proposed in [3], booth the input signal and control signal can be electronic.

The varactor proposed in [3] consists of a four terminal MOS transistor with the drain and source connected together, while the capacitance of interest is the capacitance between the gate and ground. The capacitor is changed between inversion and depletion regions by applying a voltage to the source terminal. This voltage, if high enough, will remove the inversion layer electrons, thus shifting the operating region from inversion to depletion, and reducing the capacitance in the progress. The capacitance in depletion is 5-10 times lower then the capacitance in inversion [9], so gains of this magnitude can be achieved.

In Fig. 5.4 we can see a simulation result where the capacitance of PMOS varactor is plotted against the gate to source voltage. Note that Fig. 5.4 is a mirror image of Fig. 5.3, because the first is a PMOS capacitor while the second is an NMOS.

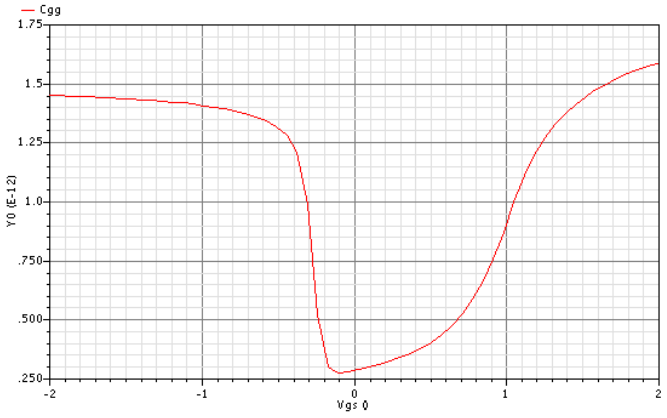


FIGURE 5.4: Simulated Capacitance/voltage characteristic of a PMOS 3 terminal varactor.

By exploiting the voltage/capacitance characteristic in Fig. 5.4 we can achieve a variable gain by adequately choosing different points of operation.

5.3 The DT MPA

Following on the discussion on the MOS varactors in the previous section, we shall now elaborate on the principle of operation of the DT MPA. In Fig. 5.5 the principle of

operation of the MOS parametric cell in [3] is illustrated.

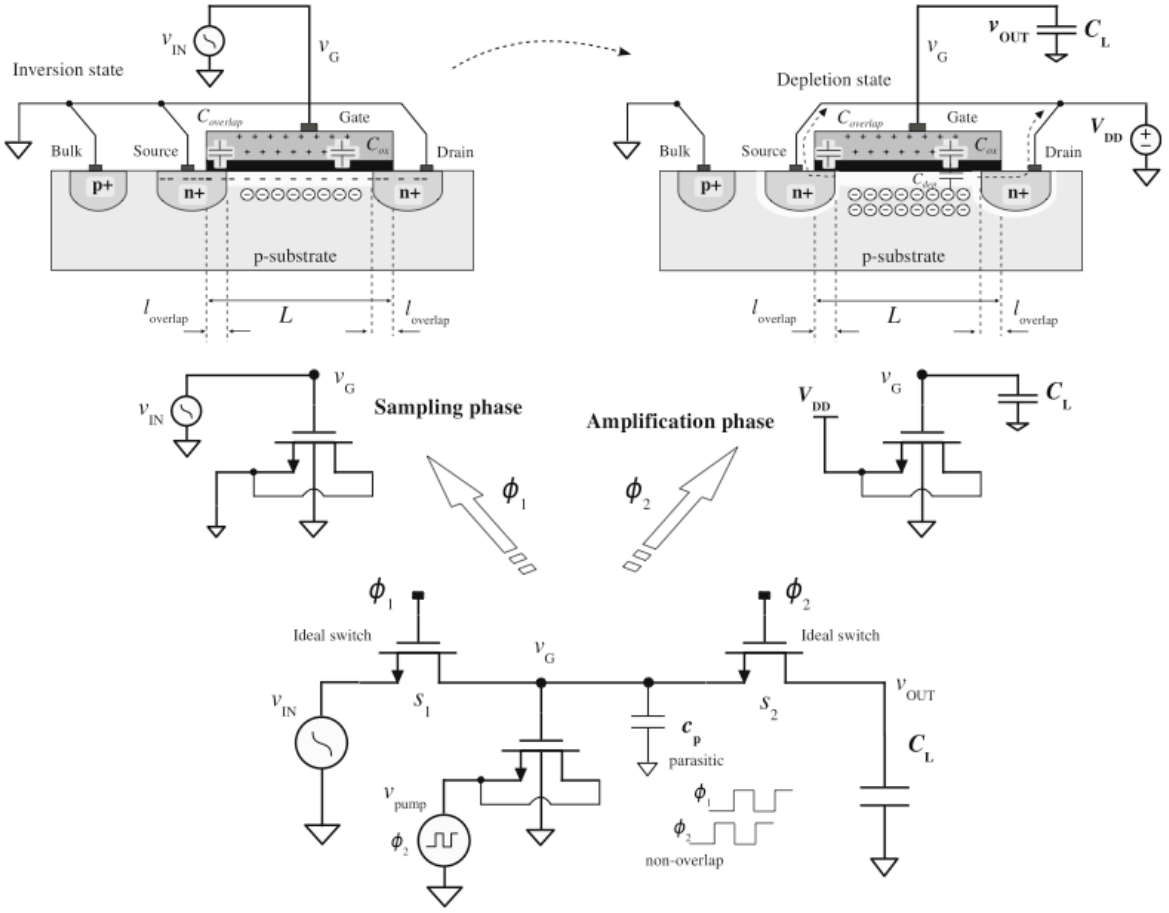


FIGURE 5.5: DT MPA cell based on [3].

During ϕ_1 the input voltage is sampled by the total gate capacitance. If the input voltage is high enough, then a thin layer of inversion charges forms beneath the gate/substrate interface. The MOS device is then biased in the inversion state. The conductive layer extends from the drain to the source terminal (which are short-circuited) forming the equivalent of a capacitor plate, being that the other capacitor plate is formed by the gate material. Intuitively we can then approximate the capacitance in ϕ_1 to be approximately equal to C_{ox}.

In ϕ_2, while the sampling switch is turned off and the gate is left floating to preserve it's charge, the drain and source terminals are connected to a large voltage (Vdd). This has the effect of removing all the inversion charges between drain and source, leaving the MOS device in the depletion region. As explained in the previous section, in the depletion region the capacitance can be expressed as the series of the oxide capacitance,

C_{ox}, and the capacitance associated with the depletion region, C_S, which is small. The total capacitance is therefore greatly reduced. The amplification gain is then obtained according to equation 5.3.

5.4 Proposed DT MPA

The proposed circuit is presented in Fig. 5.6. The maximum gate capacitance when in strong inversion was chosen to be around 1.5 pF (in order to minimize load and parasitic capacitance effects on the gain) and the MOS device was sized accordingly using a PMOS structure. The non-overlapping phases are assumed to be provided by the existing clock driving the ADC. In our simulations a 100 kHz sampling frequency was used. A simple resistive ladder is used, together with an analog multiplexer (not shown in the schematic), to provide V_{ctrl} : this circuit is basically a 2-bit voltage-mode digital-to-analog converter, DAC. The gain is adjustable in 4 steps, by controlling the two input bits of the DAC.

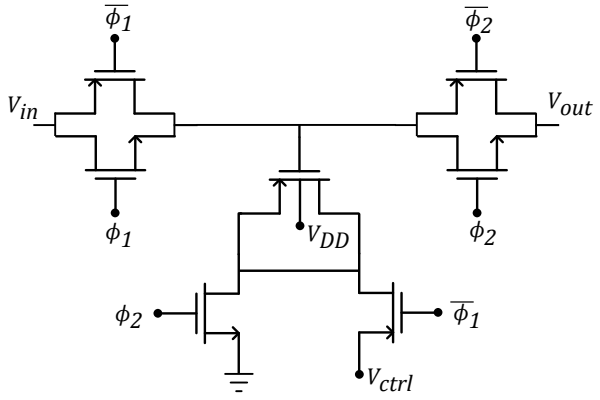


FIGURE 5.6: Proposed DT MPA circuit.

The TIA that precedes the DT MPA is differential, so two equal structures are used in parallel connected to the TIA. This pseudo differential structure enables the rejection of the amplified common-mode voltage, and allows for cancelling of the even-order distortion of the parametric amplifier [20].

A simulation of the capacitance/voltage characteristic of the PMOS structure used has already been presented in Fig. 5.4. In ϕ_2 the capacitor is pulled into the depletion region. By looking at the simulated characteristic in Fig. 5.4 , we can observe that it's capacitance in the depletion region is around 0.25 pF. In order to obtain the correct V_{ctrl} voltages to obtain the desired gains, one need to carefully choose the gate bias voltage

from the preceding stage, and V_{ctrl}. For instance, to obtain a gain of 4, we would need a capacity of 1 pF in ϕ_1. By observing the simulated capacitance/voltage characteristic, we can observe that if $V_{gs} = 0.3$ V the capacitance is aproximately 1 pF.

Using a 100 kHz sampling frequency and a 10 kHz test signal two simulation were performed with the input voltage set at $0.9V$ and $V_{ctrl} = 1.2V$. This yields the necessary V_{gs} in order to obtain a gain of 4 . This simulation is presented in Fig. 5.7 were the two output signals can be clearly seen, and the different gains can clearly be observed. In Fig. 5.8 a FFT of the signal in Fig. 5.7 is presented with a hamming window and 1024 points.

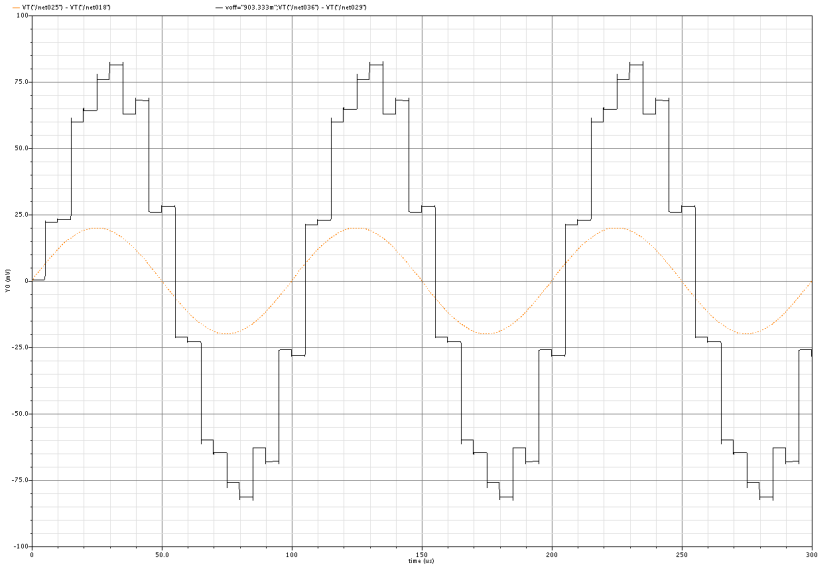


FIGURE 5.7: DT MPA simulation with $V_{gs} = 0.3$ V, $V_{in} = 20$ mV, $f_{in} = 10$ kHz, $F_s = 100$ kHz.

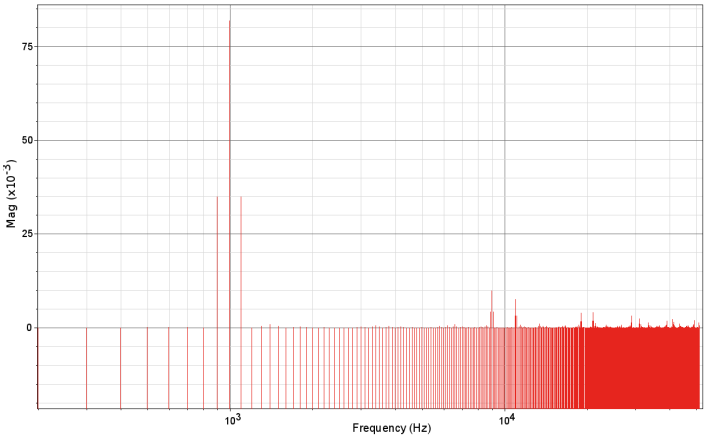


FIGURE 5.8: Hamming window FFT with 1024 points for DT MPA with $V_{gs} = 0.3$ V, $f_{in} = 10$ kHz , $F_s = 100$ kHz.

Chapter 6

Circuit Implementation

In this chapter, we will discuss the implementation of the TIA and of the complete front end. Simulation results are presented for booth the building blocks separated, and connected together. A comparison between the proposed TIA and other TIA's in the literature is also made.

6.1 Balun RCG TIA

The chosen topology for the TIA is the balun regulated common-gate, based on the common-gate/common-source topology. This circuit has been discussed in the previous chapters and we will know focus on it's implementation and sizing.

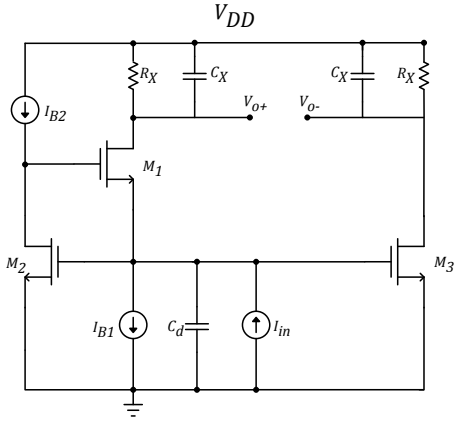


FIGURE 6.1: Balun RCG exploiting thermal noise cancelling.

The balun RCG can be seen in Fig. 6.1. The transimpedance gain is determined mainly by the resistor R_x, so a value of 20 kΩ was chosen. The regulation gain was chosen to be around 25, which is achieved with a biasing current of 25 μA. The gm boosting that the regulation feedback loop generates, enables the use of a low current of 10μA to bias the input transistor M_1. Since the CS transistor gm has to $(A+1)$ times bigger than the gm of M_1, a higher current of 300 μA was required. Note that booth the outputs must have the same DC level, in order for the DTPA function properly. Because of the high current in the CS stage, although not shown, current bleeding in the load resistance was needed.

In Fig. 6.2 the simulated frequency response of booth the RCG and the CS stages of the TIA can be observed. It's can be observed that the gains are matched and the booth stages are in phase opposition as expected, so balun operation is guaranteed and noise cancelling should be possible.

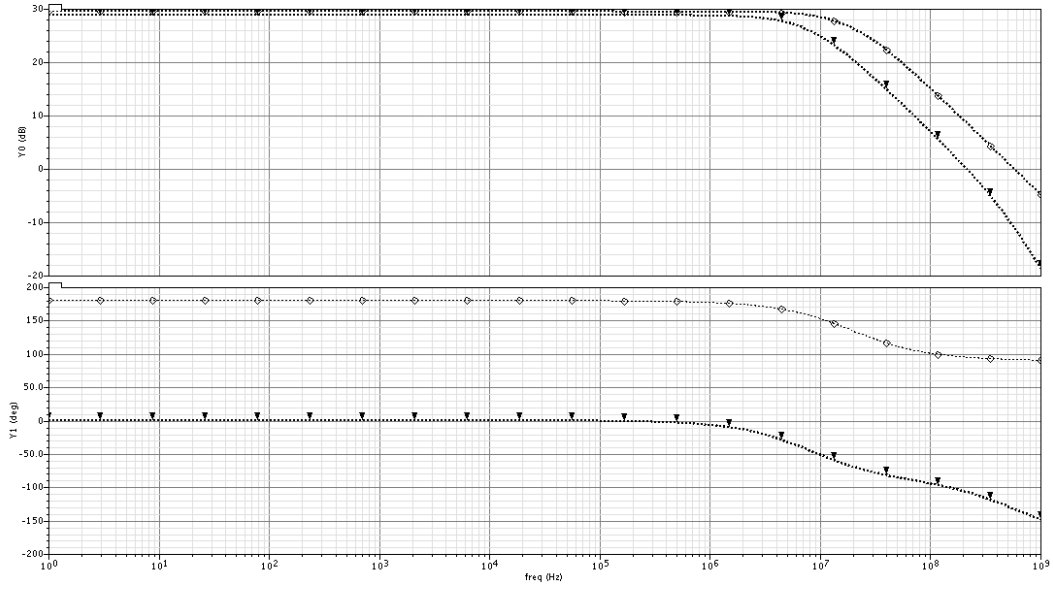
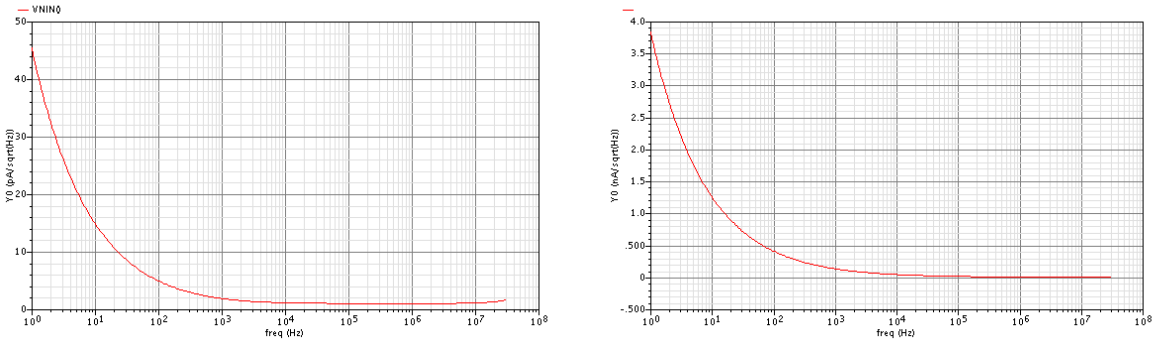


FIGURE 6.2: Frequency response of the RCG (circles) and CS (triangles).

As far as noise is concerned in Fig. 6.3(a) and 6.3(b) we can observe a simulation result of the input referred noise of the single-ended RCG, and the balun TIA. As expected the RCG has very low noise. In the differential TIA there is a considerable increase in the input referred noise due to the noise contributions of the CS stage. Still, when compared to other differential topologies, offers a comparable noise performance. In Table 6.1 the spot noise for different frequency's can be observed. Although there is a big increase in the total noise at low frequencies, for high frequencies, booth the differential and single ended TIA's have noise of the same order.



(a) (b)

FIGURE 6.3: Simulated input referred noise of: (a) RCG, (b) Balun RCG.

	1 kHz	10 kHz	100 kHz	Balun
RCG	1.88	1.131	1.019	No
RCG/CS	134.7	44	14.89	Yes

TABLE 6.1: Spot noise for different frequencies for the RCG and RCG/CS (pA/$\sqrt{Hz}$).

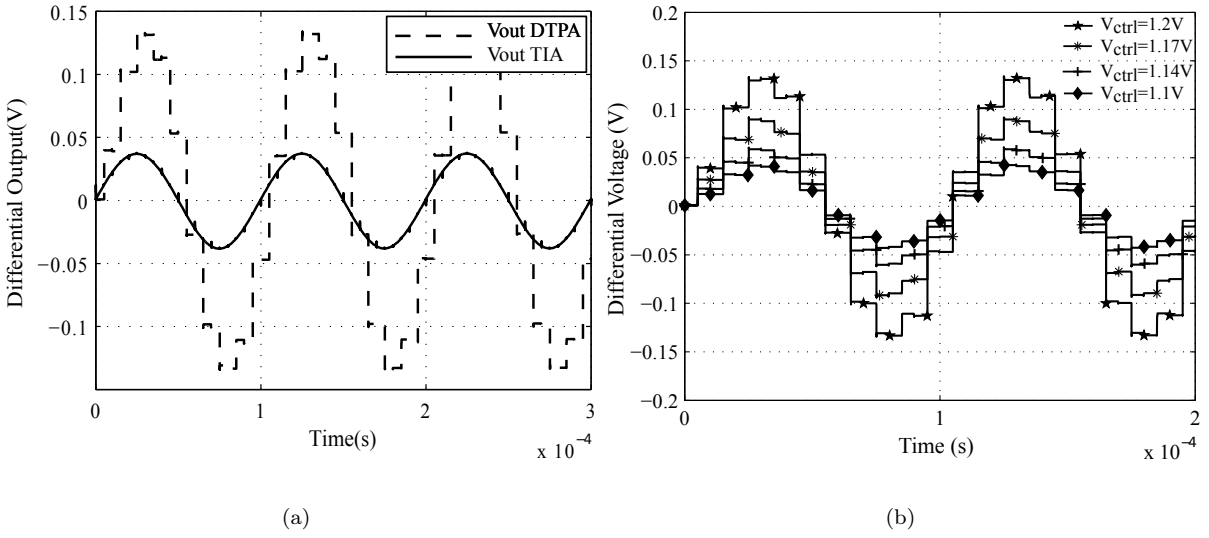
A comparison table between the TIA in this work, and other TIA's in the literature can be found in Table 6.2. Note that some of the TIA's in Table 6.2 are designed for the acquisition of a physiological signals very similar to the *SpO*2 signal envisaged in this work. Such is the case for the near-infrared spectroreflectometry (NIRS) TIA's in [21] and [22].

Ref.	Technology (nm)	Suply Voltage (V)	Power (mW)	Gain (dBΩ)	BW (MHz)	Input Referred Noise @ 1 kHz (pA/$\sqrt{Hz}$)	Balun
[21] 2008	180	1	0.0109	71.4	0.4	208	No
[23] 2011	180	2	7.2	76	2500	< 10	No
[22] 2010	350	2.6	0.14	63.5	N/A	N/A	No
This Work	130	1.2	0.035	85.96	8.3	1.88	No
			0.250	92.3		134.7	Yes

TABLE 6.2: Comparison with state-of-the art TIA's.

6.2 TIA and DTPA

In Fig. 6.4(a) a simulation is presented of the complete front end comprising the DTPA and TIA. The input signal is sinusoidal wave with 0.1 μA amplitude and a frequency of 10 kHz. Booth the output voltage of the TIA and the output voltage of the DTPA can be clearly seen. By adjusting the V_{ctrl} voltage in hte DTPA according to the method described in the previous chapter, the gain can be adjusted in stages. The proposed circuit features 4 discrete gains. In Fig. 6.4(b) The different gains can be observed for the different control voltages. Results show that the power consumption of the DTPA, excluding the V_{ctrl} generation circuit is extremely low when compared to the TIA . So for a very low power budget a maximum 8.9 dB increase in the gain can be expected, with a very low added noise and solving the problem of sampling the input for the ADC.



(a) (b)

FIGURE 6.4: Simulated transient output of: (a) TIA and DTPA, (b) Multiple gains of the DPTA.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this work, we set to design a novel front end amplifier for a pulse oximeter, which could ultimately be integrated with other sensors in a remote monitoring device for medical applications. The architecture, comprises two main blocks, the transimpedance amplifier and the discrete time parametric amplifier. Booth blocks were successfully designed and simulated in a 130 nm standard CMOS process.

We presented in this thesis a new balun TIA topology based on a combination of the well known regulated common gate and common source topologies. It was expected that exploiting thermal and flicker noise of the input transistor could lead to a better overall performance, while harvesting the benefits of differential operation. The single ended RGC presented is booth a low power and low noise, with a performance comparable to the state of the art in TIA's designed for the acquisition of physiological signals. The differential structure presented, although cancelling the noise of the input transistor as expected, introduces considerable noise, seriously degrading performance. Even so, the TIA exhibits a noise performance of the same degree of the state of the art TIA's.

Since the ADC in this architecture is expected to be multiplexed in the time domain to serve a whole array of different sensors, a sample and hold circuit would be needed. The proposed discrete time parametric amplifier renders the use of an extra S & H block useless, while adding a very low noise and ultra low power stage of amplification. At the

same time, a new method to control the gain of the parametric amplifier was proposed and verified through simulation.

7.2 Future Work

Due to limitations in time, this work only validated the proposed architecture through simulation, so further developments are left for future work and were left aside because they fall out of the scope of this thesis.

In order to implement the proposed front end, the photodiode needs to be fully characterised first. With a sensitivity and noise analysis of the photodiode a more strict design specification for the front-end should then be established. With this specification, the circuit could then be further optimized.

The proposed differential RCG/CS TIA was found to have more noise then the single ended RCG. We have discovered that CS noise contribution is more evident at low frequencies. For high frequencies, because there is a zero in the noise transfer function of the CS, the noise cancellation technique proves to be efficient. In our circuit, we designed the RCG and the CS with the same load impedances and with the same absolute transconductance for booth stages. In [17] noise performance in a CG/CS topology is improved by using a higher transconductance and a lower load impedance in the CS stage. It's likely that the same applies to the RCG/CS, so this option should be investigated as it should yield a better noise performance although at the cost of extra power consumption.

Once a proper specification is met and a new circuit designed, this work should then be validated through measurements in a test-circuit because the work in this thesis is mainly theoretical and supported by simulations only.

Appendix A

Published Paper

A Balun Transimpedance Amplifier with Adjustable Gain for Integrated SP02 Optic Sensors

A Balun Transimpedance Amplifier with Adjustable Gain for Integrated SP02 Optic Sensors

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Abstract— **The oxygen level in blood, usually referred as SPO_2 (Saturation of hemoglobin with oxygen as measured by pulseoximetry) is an essential medical information. Measuring the oxygen level of the human blood using non-intrusive techniques is a vital achievement in modern medicine. This can be performed by processing the infrared and red light transmitted by the patient's finger and received by a photoreceptor. Before being applied to an analog-to-digital converter (ADC), the incoming light has to be converted to a voltage and the range should be dynamically adjusted in order to use always the full input range of the ADC. Since the photoreceptor generates an output current, a transimpedance amplifier (TIA) with gain control is required. The two-stage TIA proposed in this paper, uses a regulated common-gate in first stage employing noise cancellation and balun operation using an additional CS stage, while the adjustable gain is implemented in the second-stage, which is based on an intrinsically noiseless MOS parametric amplifier (MPA). This MPA operates in the discrete-time domain, thus eliminating the need of an input sample-and-hold (S/H) block in the ADC. The proposed circuit has been designed in a 130 nm digital 1.2 V CMOS technology. The electrical simulations show that the overall power consumption is lower than 250 µW and input referred noise power density is extremely low.**

Index Terms—**Transimpedance amplifier (TIA), oximeter, noise cancelation.**

I. INTRODUCTION

Nowadays, there is a need for ubiquitous healthcare remote monitoring. Economic and reliable devices are required, able to continuously and remotely observe the health of patients. The blood oxygen level is one of the most important vital signs, alongside with blood pressure, heart beat rate, breathing rate, and body temperature, and it's constant monitoring can give early warning of problems in the circulatory and respiratory systems.

Typical applications are home care monitoring of the elderly or chronically ill, wireless medical sensing, remote monitoring of the health status of military personnel in the battlefield and fire-fighters engaged in fire control and rescue missions. One key target feature of the equipment it that it must be non-invasive, eliminating the need of surgical intervention to implant the sensors.

Pulse oximetry is a non-invasive method to measure the percentage of oxygenated hemoglobin in a patient blood. Pulse oximeters are widely used in intensive care, operating rooms, emergency care, birth, neonatal and pediatric care, sleep studies, and also in veterinary care. A transducer is usually clipped or taped to a translucent area of the patient, such as an earlobe or a finger. The transducer generates an electrical current signal, which is converted to a voltage signal by a transimpedance amplifier (TIA), as shown in Fig. 1.

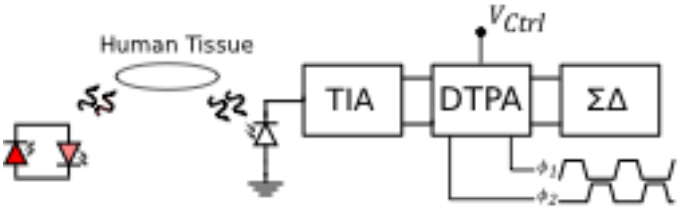

Figure 1. Pulse oximeter microsystem architecture.

In this work, a CMOS differential output TIA with adjustable gain is proposed. The proposed pulse oximeter architecture includes, besides the TIA, a photo-detector (PD) and an ADC, as shown in Fig. 1. The TIA must have low power dissipation and gain control. Adjustable gain is necessary to accommodate variations due to different light sources and intensities and transducer positioning, thus adapting the signal swing to the ADC's input dynamic range (DR).

The paper structure is as follows. In Section II, the architecture of a pulse oximeter is reviewed. In Section III, the continuous-time first stage of the TIA is described. Section IV describes the variable gain discrete-time second stage of the TIA, using MOS parametric amplification. In Section V simulation results obtained in a 130 CMOS technology are given and, finally, the conclusions are drawn in Section VI.

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II. Review of Pulse Oximetry

In the oximeter measuring system shown in Fig. 1, two light-emitting diodes (LEDs), for red and infrared range light are pulsed at a low frequency with a low duty cycle pulse signal, in order to reduce the pink-noise and the power consumption. The light transmitted through the patient skin and tissues, generates a current in the silicon photo-diode. This current is then converted into a voltage by the first stage of the TIA and in the second stage it is amplified using a Discrete Time MOS Parametric Amplifier (DT MPA) block, then the signal is held and quantized by the ADC.

The percentage of oxygen in blood (SPO2), is expressed as the ratio between oxygenated hemoglobin and the total hemoglobin (HbO_2) according to,

$$\mathrm{SP02} = \frac{HbO_2}{Hb + HbO_2} \tag{1}$$

where Hb is the amount of hemoglobin with reduced oxygen. Oxygenated hemoglobin is bright red, so it absorbs more infra-red (IR) light, letting more red photons pass through in contrast to the dark red hemoglobin with reduced oxygen. It is this different absorption of red light (660 nm) and IR light (940 nm) that makes it possible to measure the blood oxygenation by measuring the ratio of absorption of red and IR light.

The light sources, usually LEDs, emit red and IR light through a translucent part of the patient's body, such as an earlobe, a finger or a toe. The light passes through the patient's skin and tissue, and is then measured by the photo-diode. Light has to travel through different tissues, such as skin, bones and muscle. Blood vessels expand and contract with the heartbeat, so the oximeter signal appears modulated, making it possible to effectively separate the blood transmitted signal, an AC signal, from the signal from other tissues in the background, a DC signal [1].

The physics behind the working principle of the pulse oximeter is the Beer-Lambert law. This law relates the transmitted and incident light through a medium that contains an absorbing substance of concentration (C), length(L), and a wavelength dependent absorption coefficient $\varepsilon(\lambda)$ according to

$$I_{TRANS} = I_{INC} e^{-\varepsilon(\lambda) CL} . \tag{2}$$

where I_{TRANS} and I_{INC} are the intensity of the transmitted and incident light, respectively.

One can define the transmittance T as I_{TRANS} / I_{INC} and the un-scattered absorbance A as $-ln(T)$, resulting in the total light absorbance of blood, A_{bld}, given by

$$A_{bld} = [\varepsilon_{HbO2}(\lambda_R) C_{HbO2} + \varepsilon_{Hb}(\lambda_R) C_{Hb}] L . \tag{3}$$

when the blood vessels expand and contract, their thickness varies, and so does the absorbance of the blood in them with L in (3). If R is the ratio of relative absorbance at the red and IR wavelengths, we get

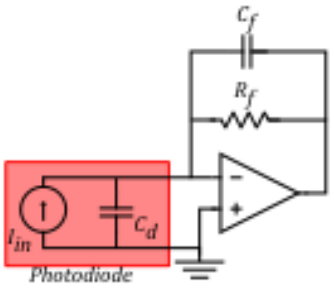

Figure 2. Shunt feedback transimpedance amplifier and photodiode equivalent circuit.

$$R = \frac{\ln(I_{H,Red} / I_{L,Red})}{\ln(I_{H,IR} / I_{L,IR})} \approx \frac{I_{ac}^{Red} / I_{DC}^{Red}}{I_{ac}^{IR} / I_{DC}^{IR}} \tag{4}$$

which leads to

$$R = \frac{\varepsilon_{HbO2}(\lambda_{Red}) C_{HbO2} + \varepsilon_{Hb}(\lambda_{Red}) C_{Hb}}{\varepsilon_{HbO2}(\lambda_{IR}) C_{HbO2} + \varepsilon_{Hb}(\lambda_{IR}) C_{Hb}} . \tag{5}$$

It's known that the approximation in equation (4) is good, as long as the AC signals are small when compared to the DC component [1]. We can combine (1) and (5) to obtain

$$SpO_2 = \frac{\varepsilon_{Hb}(\lambda_R) - \varepsilon_{Hb}(\lambda_{IR}) R}{\varepsilon_{Hb}(\lambda_R) - \varepsilon_{HbO2}(\lambda_R) + [\varepsilon_{HbO_2} \lambda(_{IR}) - \varepsilon_{Hb}(\lambda_{IR})] R} \times 100\% \tag{6}$$

The absorbance for Hb and HbO_2 are known for the red and IR wavelengths, so it's now clear that the pulse oximeter measures the ratio R , which is related to SP02 by means of (4, 5).

III. TIA First Stage: I/V Converter

To convert the light signal at reduced cost an integrated CMOS photodiode is used as the transducer. A photodiode can be modeled as a current source in parallel with a capacitor [4], as shown in Fig. 2. The capacitance value is usually high, and is bias dependent: typical values are of the order of the pico-farad (pF) for a device of 50 $m \times 50$ m [9]. This capacitance is dependent on the technology, device size and biasing [9], and the value of 1 pF is assumed for the design and simulation here.

The current of an integrated photodiode is highly dependent on its junction area [9]. In this work, it is assumed that the current is between 0.1 – 10 μA. The sizing of the photodiode is outside the scope of this work, and it should be done according to this current specification.

In this application the TIA should satisfy several requirements, high gain-bandwidth product (GBW), low noise and low power consumption.

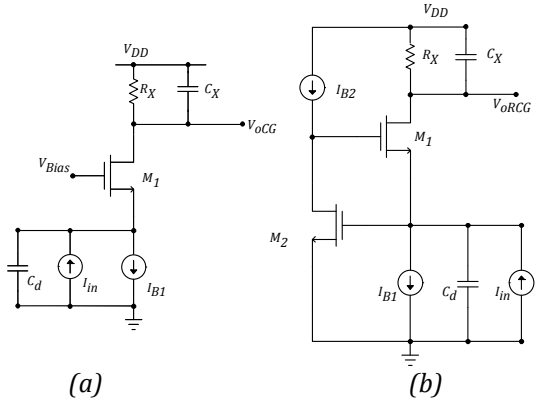

Figure 3. CG TIA (a) and RCG TIA (b).

The choice of the TIA is considered derivation of the proposed TIA circuit is supported in the following subsections.

A. Feedback I/V converter

The feedback I/V converter is commonly used in optoelectronic integrated circuits [2]. It consists of an operational amplifier (OA) with feedback, as illustrated in Fig. 2. Making the same assumptions as in [3] the following transimpedance function is

$$\frac{V_o}{I_{in}} = \frac{R_f}{1 + sR_f(C_f + \frac{C_d}{A_o}) + s^2 R_f C_d B^{-1}}, \tag{7}$$

where B is the gain bandwidth product of the OA (assuming it has a dominant Pole) and A_o is the low frequency gain. Although the feedback amplifier has a good noise performance [3], the power consumption would be high to have a high gain OA, so alternative topologies are considered.

B. Common-Gate I/V Converter

Another basic I/V converter is the common-gate (CG) stage represented in Fig. 3(a), where I_{B1} and V_{Bias} are a bias current and voltage, respectively. This topology has the advantage of low input impedance, broadband, and well behaved time response [4].

The transimpedance is R_x, and is required to have a value of tens of kOhm, thus creating a high DC voltage drop. To keep the power low and headroom for a voltage swing, a low current has to be used to bias the input transistor. This leads to a low g_m, which increases the input impedance

$$Z_{inCG} \approx \frac{1}{g_{m1}}. \tag{8}$$

In addition, a low g_m compromises the noise and stability performance of the amplifier [5].

C. Regulated Common-Gate I/V converter

To lower the input impedance without increasing g_m, a regulated common-gate (RCG) circuit can be used. This is presented in Fig. 3(b). This can be viewed as a CG stage to which an amplifier loop is added, which has the effect of boosting g_m [3], which is multiplied by the added amplifier gain. The input impedance is approximately

$$Z_{in} \approx \frac{1}{Ag_{m1}} \tag{9}$$

A is the gain of the common-source transistor M_2 (with active load I_{B2}) in Fig. 3 (b)

$$A = g_{m2}(r_{o2} // R_{oB2}) \tag{10}$$

where R_{oB2} is the incremental resistance of current source I_{B2}.

D. Noise Canceling

It is convenient that the TIA, with a single-ended input, has a differential output (balun operation). By implementing the I/V conversion and balun together, noise cancelling of the thermal noise of the input transistor can be achieved. The thermal noise of the CG transistor (M_1) is represented by the current source I_{n1} in Fig. 4, which generates a noise voltages $V_{n,in}$ at the input and $V_{n,out1}$ at the output, which are in anti-phase, while the signal at the input and output is in-phase. Since the gain of the CS is negative, the output signals V_{out1} and V_{out2} are in anti-phase, effectively doubling the gain, while $V_{n,out1}$ and $V_{n,out2}$ are cancelled. The gain matching between the two stages is crucial to obtain the noise cancelling [6].

E. Proposed I/V Converter

The TIA proposed here, comprises a RCG with noise cancelling, shown in Fig. 5.

The current sources are implemented by current mirrors sized so that I_{B2} = 50 A, I_{B1} = 10 A and I_{B3} = 200 A. To balance the gain and DC offset the load resistors of both the RCG and CS stages are equal. The CS transconductance was chosen to achieve output balancing and noise cancelling. The high transimpedance gain required is obtained by having $R_{RCG} = 20k\Omega$.

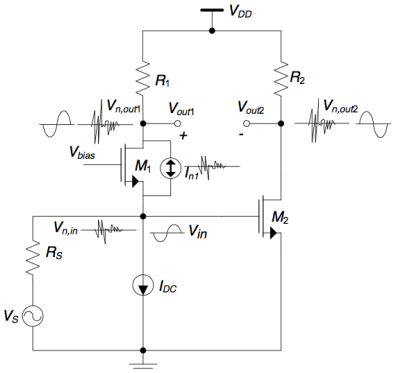

Figure 4. Noise cancellation technique, [6].

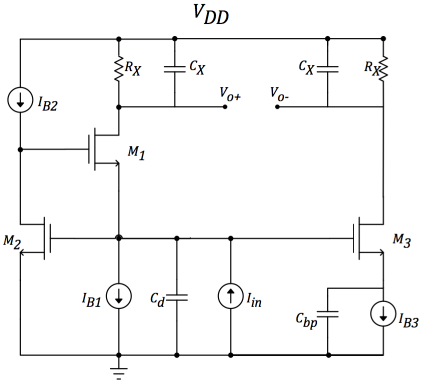

Figure 5. Proposed RCG TIA with noise cancellation.

IV. Second Stage: Discrete-Time Parametric Amplifier with Variable Gain

From the capacitor equation $Q = CV$, if the capacitance of a varactor is changed from an initial value C_1 to a lower value C_2, while conserving the charge, a voltage gain is achieved, given by,

$$A_v = \frac{V_o}{V_i} = \frac{C_1}{C_2} \ . \qquad (11)$$

This principle can be implemented in MOS technology by controlling the gate-to-bulk capacitance of an MOS device. This control is achieved through a voltage that is applied simultaneously at the drain and source [5, 6] terminals. As explained in [6], considering a discrete-time signal configuration, an input signal sampled at one phase can be amplified and held in a second phase if one can reduce the gate-to-ground capacitance, while maintaining the total gate charge.

The principle of this amplifier is illustrated in Fig. 6. In the sampling phase Φ_1, the input signal is sampled by the PMOS varactor in strong inversion and it is held at the beginning of Φ_2, by maintaining the gate terminal floating. Amplification is then obtained, during Φ_2, when the capacitance value is reduced, since the device is forced to enter into depletion state. A first order analysis indicates a maximum amplification gain of $v_o/v_i = C_{ox}/C_{gb}$, where C_{ox} is the total oxide capacitance and C_{gb} is the gate-bulk capacitance during the amplification (boost) phase [6].

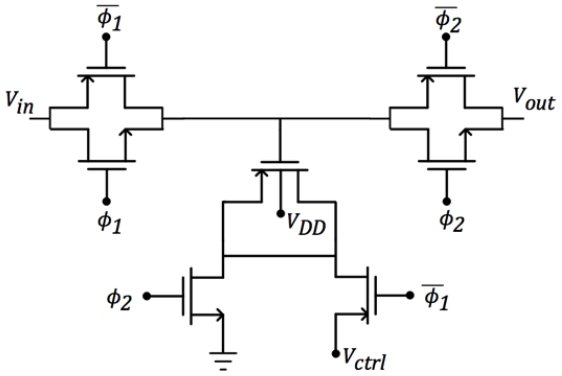

Figure 6. The DT MOS parametric amplifier based on a PMOS varactor.

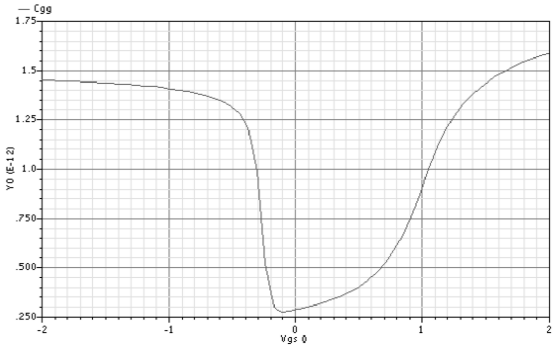

Figure 7. Total gate capacitance of PMOS varactor device.

The total gate capacitance of a PMOS device as a function of the applied common-mode gate voltage is shown in Fig. 7. One can conclude that biasing the device in moderate inversion during the sampling phase, a lower value (lower than C_{ox}) gate capacitance is obtained. Therefore, by controlling this capacitance, the gain of the circuit can be adjusted. This gain control voltage has been included in the proposed circuit, shown in Fig. 6. By varying the voltage applied to the drain/source terminal during the sampling phase (V_{ctrl}), a variation of the device sampling capacitance is possible, thus enabling a voltage gain control.

The maximum gate capacitance when in strong inversion was chosen to be 1 pF (in order to minimize load and parasitic capacitance effects on the gain) and the MOS device was sized accordingly using a PMOS structure. The non-overlapping phases are assumed to be provided by the existing clock driving the ADC. In our simulations a 100 kHz sampling frequency was used. A simple resistive ladder is used, together with an analog multiplexer, to provide V_{ctrl} : this circuit is basically a 2-bit voltage-mode digital-to-analog converter,

DAC. If the gain is adjustable in 4 steps, by controlling the two input bits of the DAC.

V. Simulation Results

The regulated common-gate topology with noise cancellation (Fig. 5) was used as the first stage balun I/V converter. The second stage is a fully-differential DT MPA (two circuits similar to that in Fig. 6. The circuit is designed in a standard (purely digital) 130 m CMOS process.

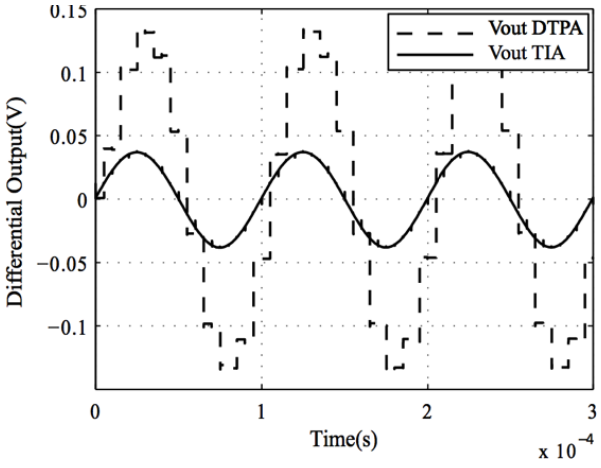

Figure 8. Differential output signal.

In Fig. 8 the simulated differential output signals of the I/V converter and of the DTPA can be observed, when an input 10 kHz sine wave with 1 A amplitude is assumed as the photodiode input.

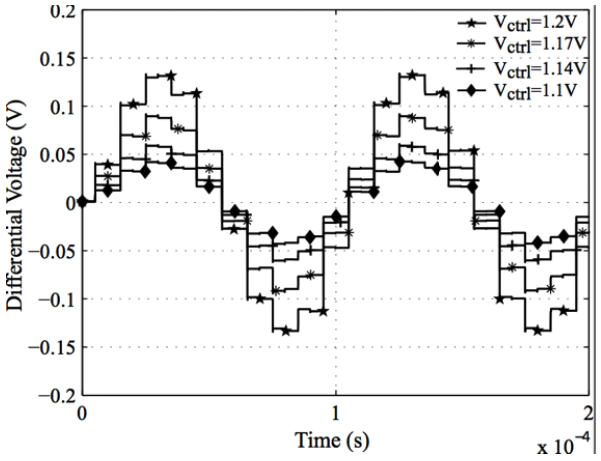

Figure 9. Simulated output of the DT MPA circuit for different gains.

In Fig. 9, different gains of the DT MPA can be clearly observed for the same input signal. By varying the PMOS varactor drain voltage between 1.2 V to 1.1 V, the different gains are obtained. Since low noise is a requirement for the TIA the input referred noise is also simulated and is shown in Fig. 10.

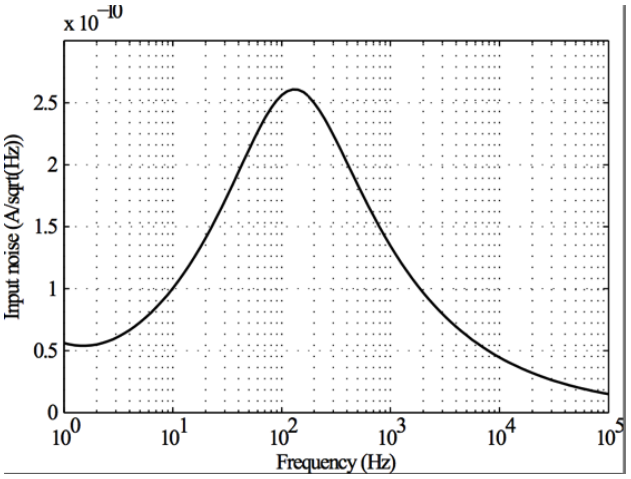

Figure 10. Input referred noise power density.

VI. Conclusions

This paper presents a two-stage TIA with gain control. The proposed amplifier uses a RCG employing a balanced noise cancellation technique in the first stage. For the second state a DT variable gain MPA circuit was presented. Simulations results were given with supply 1.2 V for the circuit designed in a 130 nm digital CMOS technology. These results demonstrate the feasibility of the proposed circuit with a power consumption lower than 250 µW.

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