UNIVERSIDADE NOVA DE LISBOA
Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Low Power Low Voltage Quadrature RC Oscillators For Modern RF Receivers

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Abstract

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestre em Engenharia Electrotécnica e de Computadores

by Hugo Filipe da Rocha Lopes

This thesis proposes a study of three different RC oscillators, two relaxation and a ring oscillator. All the circuits are implemented using UMC 130 nm CMOS technology with a supply voltage of 1.2 V.

We present a wideband MOS current/voltage controlled quadrature oscillator constituted by two multivibrators. Two different forms of coupling named, soft (traditional) and hard (proposed) are differentiated and investigated. It is found that hard coupling reduces the quadrature error and results in a low phase-noise (about 2 dB improvement) with respect to soft coupling. The behaviour of the singular and coupled multivibrators is investigated, when an external synchronizing harmonic is applied.

We introduce a new RC relaxation oscillator with pulse self biasing, to reduce power consumption, and with harmonic filtering and resistor feedback, to reduce phase-noise. The designed circuit has a very low phase-noise, -132.6 dBc/Hz @ 10 MHz offset, and the power consumption is only 1 mW, which leads to a figure of merit (FOM) of -159.1 dBc/Hz.

The final circuit is a two integrator fully implemented in CMOS technology, with low power consumption. The respective layout is made and occupies a total area of $5.856\text{x}10^{-3}$ mm^2, post-layout simulation is also done.

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Resumo

Faculdade de Ciências e Tecnologia
Departamento de Engenharia Electrotécnica e de Computadores

Mestre em Engenharia Electrotécnica e de Computadores

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Nesta tese é proposto um estudo de três distintos osciladores RC, dois de relaxação e um oscilador em anel. Todos os circuitos são implementados usando a tecnologia UMC 130 nm com uma tensão de alimentação de 1,2 V.

Apresentamos um oscilador em quadratura controlado por corrente/tensão constituído por dois osciladores de relaxação. Duas formas distintas de acopulamento, *soft* (tradicional) e *hard* (proposta), são investigadas e comparadas. O acopulamento *hard* reduz erros de quadratura e obtém uma melhoria do ruído de fase (à volta de 2 dB), em comparação com o acopulamento *soft*. O comportamento do oscilador individual e acopulado é investigado ao ser aplicado uma harmónica externa.

Propomos um novo oscilador RC de relaxação com *pulse self biasing*, para reduzir o consumo e também *harmonic filtering* e *resistor feedback*, para reduzir o ruído de fase. O circuito desenvolvido possui um ruído de fase baixo, -132,6 dBc/Hz @ 10 MHz, e um consumo de apenas 1 mW, que conduz a uma figura de mérito de -159,1 dBc/Hz.

O último circuito é um *two integrator* totalmente implementado na tecnologia CMOS, com um consumo reduzido. Foi feito e simulado o *layout* deste circuito, que ocupa uma área de $5.856\text{x}10^{-3}$ mm^2.

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Abbreviations

CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
DLL	**D**elay **L**ocked **L**oop
DRC	**D**esign **R**ule **C**heck
FOM	**F**igure **O**f **M**erith
IF	**I**ntermediate **F**requency
LNA	**L**ow **N**oise **A**mplifier
LTI	**L**inear **T**ime **I**nvariant
LvS	**L**ayout vs. **S**chematic
NMOS	**N**channel **M**etal-**O**xide-**S**emiconductor
ODE	**O**scillator **D**esign **E**fficiency
PMOS	**P**channel **M**etal-**O**xide-**S**emiconductor
Q	**Q**uality factor
SSB	**S**ingle **S**ide **B**and
VCO	**V**oltage **C**ontrolled **O**scillator
WMTS	**W**ireless **M**edical **T**elemetry **S**ervice

Dedicated to my Family...

Chapter 1

Introduction

1.1 Background

Wireless communication evolution through out the years have been influenced by many factors like power consumption, size, cost, and noise. Nowadays, the boom on wireless communications led to new requirements such as: low supply voltage, low cost, and small area circuits. The use of CMOS technologies is a way to attain these objectives, by adapting old architectures or by implementing new circuit designs.

The RF front-end is generally defined as the circuits between the antenna and the digital part. The receiver front-end has the most crucial role in communications, their blocks have very demanding specifications. There are two basic architectures: heterodyne and homodyne, the first converts the signal to a intermediate frequency (IF) and the latter downconverts directly to the baseband. The Low-IF receiver is a modified version of the homodyne and is becoming a good alternative, because it combines the advantages of both basic architectures.

Modern receivers demand quadrature outputs, so the oscillator must be able to generate wave signals with a 90° phase shift, so the outputs must be stable in frequency and phase otherwise any deviation may compromise the system. One way to obtain accurate quadratures outputs is cross coupling two symmetric oscillators. Due to this, new

architectures have emerged using RC and LC oscillators, some of them have inherent quadrature outputs, for example the two integrator oscillator.

When comparing a single LC and RC oscillator, the first one has a better phase-noise. To reduce the discrepancy new techniques have been develop for this purpose. With new market requirements and the study of cross coupled oscillators the RC oscillators have proved to be a good choice for quadrature outputs, coupled LC oscillators on the contrary have a higher phase-noise, due to the degradation of the quality factor (Q), [10]. There are other advantages such as fast synchronization, wide frequency tuning range, and low area. Recent studies of RC oscillators in CMOS technology, have demonstrated the possibility to integrate other receiver blocks within the oscillator circuit, [10]. The main objective of this thesis is to show the advantages mentioned through three different RC circuits.

1.2 Motivation

The main motivation is the study of quadrature oscillators with reduced area, power, and low phase noise, for modern low-IF and direct conversion receivers. In this thesis we present three different approaches to this matter. In the first part we will simulate the behaviour of a coupled RC oscillator when some of his components are mismatched, we will also see how much time a single and coupled oscillator takes to synchronize when an external current source with a frequency equal to an odd multiple of the oscillation frequency. Then we will apply some methods to a simple RC oscillator with the objective of improving power consumption and noise. These segments serve to prove the advantages of RC oscillators and how some of their disadvantages can be surpassed. We have implemented a fully integrated CMOS two integrator to reinforce the idea of a small area circuit, the total area occupied is $5.856\text{x}10^{-3}$ mm^2.

1.3 Thesis Organization

This thesis is organized in five chapters. The current one gives an introduction to the work done, the motivation, the structure of this thesis, and the main contributions.

The second chapter focus on receiver architectures, their differences and features. We will also discuss conventional quadrature signal generators.

In chapter three we present some oscillator basics and analyse three different oscillators architectures. The first is a LC oscillator known for its low noise, the second is RC oscillators that have been the focus of many studies in recent years, the last is the two integrator oscillator, a oscillator that has quadrature outputs. We also discuss how RC and LC oscillators can produce quadrature outputs.

The main chapter of this thesis is the fourth one. Here we discuss, analyse and implement different oscillators. These circuits are designed with the objective of obtaining reduced noise, power and area circuits. First, we tested a RC oscillator for component mismatches and how they affect the behaviour of the oscillator. In the second part we implement some methods to reduce phase noise, and finally, we present a fully integrated CMOS two integrator with the respective layout and post-layout simulations. All oscillators were implemented in Cadence software using 0.13 µm CMOS technology.

In the fifth chapter we present some conclusions and indicate some future research work that can be done concerning the topics of this thesis.

1.4 Main Contributions

The main contributions for this thesis are:

- The study and simulation of numerous techniques to reduce phase noise applied on a simple relaxation oscillator is made. One of them is unique and only possible on CMOS. A paper was submitted, at the moment of writing this thesis we were waiting for approval.
- The study of a multivibrator for CMOS technology. The utilization of that oscillator for a cross coupled version using both soft and rigid coupling, and comparing both. The study of frequency locking at a sub-harmonic frequency when an external current source is applied. This work lead to a article [1] for the MIXDES conference, where it received one of the awards for outstanding paper, and it was invited for an extended version for a magazine.
- The creation of a fully integrated CMOS two integrator oscillator, by substituting the capacitors and resistors for CMOS transistors, making it a low cost, low power and small area oscillator. A layout was made for a future test-chip, at the present this chip was submitted for fabrication. If the chip results are satisfactory, then this work may have a future publication.

Chapter 2

Receivers Architectures and Quadrature Signals Generation

2.1 Introduction

In this chapter we present a brief introduction to some receiver architectures and the last part will focus on some conventional quadrature signal generators.

Receivers are used for demodulation of a signal sent by a transmitter, first the received signal in the antenna is amplified and then downconverted to a lower frequency at the end we obtain the demodulated signal at the output. The transmitter performs the opposite actions, it modulates the signal, then upconverts and finally amplifies and sends it through the antenna. Both transmitter and receivers can be classified as in two basic architectures: homodyne or heterodyne [10, 13]. In heterodyne the signal is downconverted to intermediate frequencies (IF), in the homodyne the conversion is done directly to the baseband. Nowadays the homodyne architecture is preferred because of its simplicity, lower power and low cost [10]. New architectures have appeared in recent years based on the ones mentioned, one of them is being used on FM receivers it is called low IF receiver [13].

The signal received in the antenna goes through many stages in the receiver, each one with a specific role. The amplifier is the first main block and has a crucial influence on the overall noise that why the LNA as to amplify the signal without introducing noise. Another block is the oscillator, this block generates a frequency, which combined with the mixer will change the signal frequency.

Modern receivers require quadrature outputs, due to this the oscillator must be able to generate two waveforms with a 90° difference between them. The last part of this chapter presents some methods to generate quadrature outputs without feedback topologies. First, we discuss a basic circuit using known electronic components, then more complex architectures such as Havens' technique and frequency division.

2.2 Receivers

There are three popular architectures of receivers heterodyne, homodyne and low-IF, [10, 13]. The first one is widely used, in a first stage the signal goes from RF to IF and on a second stage from IF to the baseband. The second receiver translates the signal directly from the RF to the baseband, that is why they are also called direct IF or Zero-IF architectures. The low-If receiver is based on the heterodyne, the signal goes from RF to a low-IF frequency and only after its conversion to the digital domain, is brought to the baseband.

2.2.1 Heterodyne or IF Receivers

The block diagram of a modern heterodyne is shown figure 2.1. The incoming signal is first passed through a band pass filter, which isolates the wanted frequencies, then it is amplified by the LNA. The image reject filter attenuates the signals at image band frequencies from the LNA. With the mixer and the oscillator, the signal goes to IF then another band pass filter is applied to obtain the IF band of interest and reject the others and finally is amplified. The downconversion requires both in-phase (I) and quadrature

(Q) components of the signal so the mixer can bring it to the baseband. After that, the signal goes through a low pass filter and then is converted to digital. All filters used must be implemented off-chip to obtain a high quality factor (Q), this is one of the reasons why this architecture is not used in nowadays technology. There are two main drawbacks of this architecture, the need for a high performance oscillator and the image frequency.

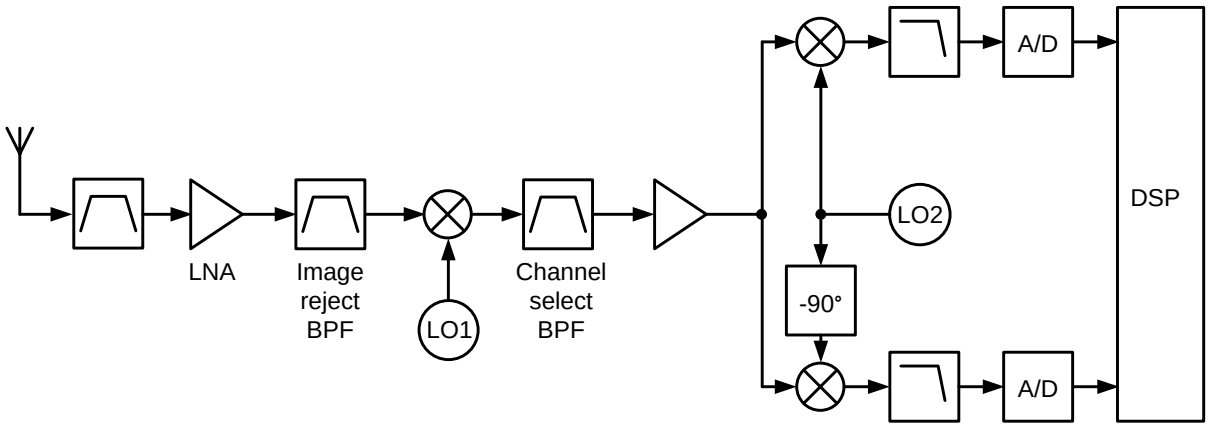

FIGURE 2.1: Heterodyne Architecture.

The image frequency problem is caused by the mixer, it moves both sum and difference frequencies, converting two frequencies at the same IF. We want to downconvert a signal with a frequency ω_{RF} to ω_{IF}, but the image frequency at ω_{IM}, as shown on figure 2.2 is also downconverted. Even after the image reject filter there is still a small signal at that frequency. When the signal goes through the mixer both frequency are downconverted to ω_{IF}. Let us give a practical example, assuming that ω_{IM} is 6 GHz, ω_{LO} is 4 GHz and ω_{RF} is 2 GHz, when both frequencies pass the mixer both end up at 2 GHz.

There is a trade-off in this architecture related to the IF frequency. The value chosen influences some blocks of the receiver. With higher value it becomes easier to design an image rejection filter, because the image is far away from the desired frequency. At a lower value the band pass filter next to the mixer is less demanding making it easier to implement, the same goes for the IF signal amplifier.

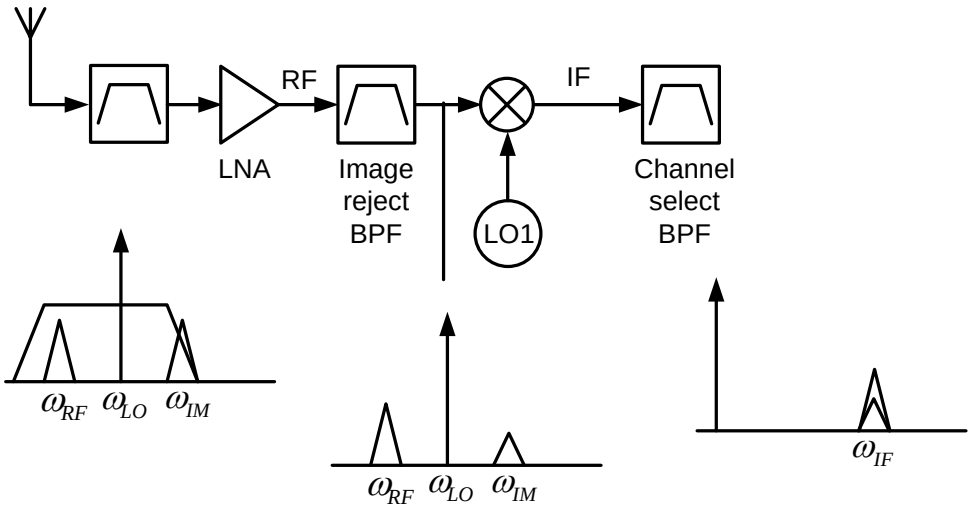

FIGURE 2.2: Image Rejection.

2.2.2 Homodyne or Zero IF Receivers

In homodyne receivers the signal is directly translated from the RF to baseband. The most obvious difference between homodyne and heterodyne is the absence of a mixer stage, which is why the band filtering is only made before the LNA and after the downconvertion.

In the heterodyne, as seen before, the first mixer causes a overlap between two signals on IF, in this case since the IF is zero the desired frequency is its own image, so there is no need for a image reject filter. Other advantage is amplification, since it is done on baseband the power consumption is reduced. Furthermore there is no need to use a band pass filter, instead, only a low pass filter is used after the downconversion. Since there is no image reject filter the LNA does not need to match 50 ohm. This architecture as less blocks, as shown on figure 2.3, thus, consuming less power than the heterodyne receiver.

There are some disadvantages when compared with the heterodyne, but this architecture is still in research for more demanding applications [10]. Those disadvantages are:

– Local oscillator leakage, normally, there will be a imperfect isolation between the local oscillator and the input port of the mixer and LNA, this leakage mixes with the original wave from the oscillator producing DC offsets in the mixer output.

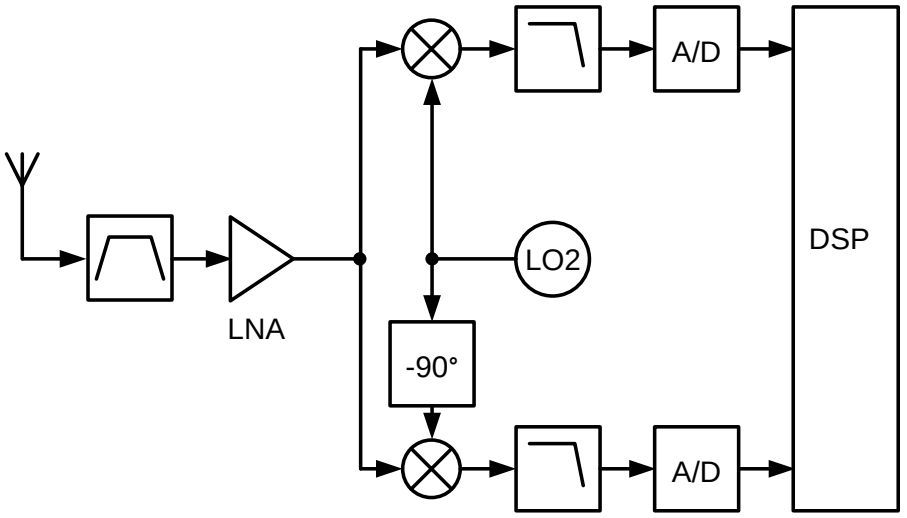

FIGURE 2.3: Homodyne Architecture.

This leakage may also go to the antenna, which interferes with the same frequency receivers.

– DC offsets, because of the local oscillator leakage an voltage offset at the mixer output appears and causes the saturation of the following stages.

– Flicker noise from a active device may contaminate the base band signal, due to the spectrum close to DC.

– Quadrature mismatch and error, ideal baseband signals can be obtained if the gains of I and Q branches are equal and have a phase difference of 90°. This error causes a mismatch between the branches and corrupts the signal.

– Even order distortion, produces a DC offset so the receivers must have a high IIP2 (second-order intermodulation intercept point).

This receiver is mostly used due to the low cost, low area, and low power consumption. The heterodyne needs external high quality components, but the performance is better than the homodyne. The next architecture combines both advantages of these receivers into one.

2.2.3 Low-IF receivers

The low-IF receiver, as a similar structure to the one of the homodyne, but instead of downconvert to the baseband it converts to an intermediate frequency close to the baseband. The signal first passes through a band pass filter, then is amplified and mixed in quadrature to a low IF; finally, the signal is once again amplified and filtered before being sampled by the ADC. The IF frequency is once or twice the bandwidth of the desired signal, which avoids the DC offset problems caused by LO leakage in the homodyne, but introduces the image frequency disadvantage of the heterodyne.

Unlike the heterodyne a image rejection filter is impossible to use, because it would demand a filter with a extreme quality factor (Q) for the low IF. Two image reject techniques have been proposed, Hartley and Weaver architectures. Both solutions are implemented after the low pass filter and combine both outputs into a single one, variations of these architectures were also made for quadrature outputs.

A way to quantify the degree of image rejection in a receiver is the image rejection ratio, which is given by (2.1), where P_{IM} and P_S are the average power of the image and the signal respectively, V_{IM} and V_S their amplitude. In the ideal case the image signal level is equal to zero, making $IRR = \infty$.

$$IRR = \frac{\frac{P_{IM}}{P_S}}{\frac{V_{IM}^2}{V_S^2}} \tag{2.1}$$

We assume that the oscillator produces a phase difference of 90° with no mismatches. The Hartley solution, shown on figure 2.4, shifts the Q signal another 90° and then both are summed. Figure 2.4 shows in detail how this solution works, since there was already a shift of 90°, the image signal will be in opposition of the I channel, when adding both, the signal at ω_{RF} is maintained and both images cancel each other.

There is a variation of this architecture, but the same principle is applied. Instead of using a 90° shift, the in-phase signal is shifted -45° and the quadrature 45°.

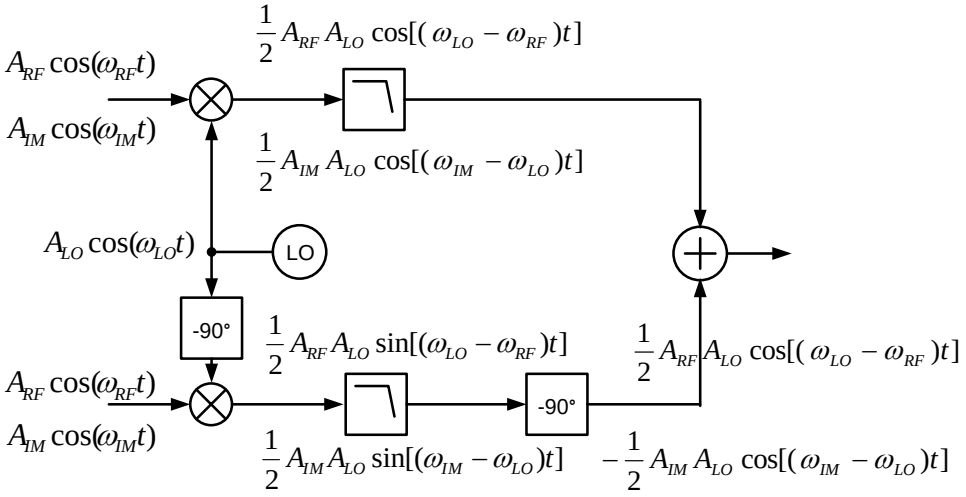

FIGURE 2.4: Hartley Solution.

The basic Weaver solution does the exact same thing as Hartley architecture, by using a new quadrature mixing stage, as shown on figure 2.5, the same image canceling effect is obtained. With a few changes this architecture can be used for quadrature outputs, but for a single output the Hartley solution is more suitable because a second mixing stage could produce more phase deviations.

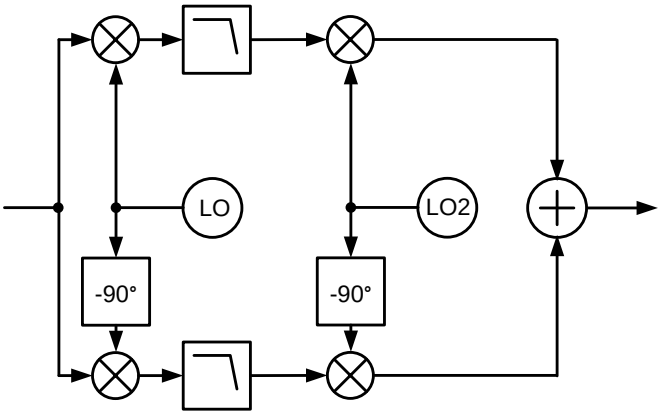

FIGURE 2.5: Weaver Solution.

A mismatch in phase and amplitude affects the remaining circuit. A amplitude imprecision is not so influential because after the band pass filter the signal is amplified, but a phase error cannot be corrected easily corrected. The phase error also influences both image and signal of interest average power, assuming only a quadrature mismatch in the oscillator (2.1) becomes equal to (2.2), where θ represents the phase error. We can conclude that the image suppression success depends on the accuracy of the oscillator.

$$IRR = \frac{\theta^2}{4} \tag{2.2}$$

2.3 Quadrature Signal

Communications systems use In-Phase (I) and Quadrature (Q) signals for modulation and demodulation, these signals have a phase difference of 90°. This requirement raises an important matter on mismatches because the error rate in detecting the base band signal increases, [10, 13]. The oscillator assumes a critical role on quadrature outputs, because of the required low quadrature error.

In this section we will discuss three common methods for generating quadrature signals those are RC-CR network, frequency division, and Haven's technique.

2.3.1 RC-CR Network

The RC-CR network, shown on figure 2.6, simply shifts the phase of the signal by +45° in the CR network, and -45° in the RC network. This way the phase difference between the outputs will be 90° for all frequencies. The amplitude, on the other hand, always varies with frequency with the exception of the pole frequency, $\omega = \frac{1}{RC}$. All of this can be easily seen by analyzing the bode diagram of each branch, the CR network is a high pass filter and the RC is a low pass filter.

The optimum working frequency is the pole frequency, this value has to be equal to the carrier frequency. The problem is the variation of the absolute values of the resistors and capacitors, caused by temperature or process. As a consequence, there is a different frequency in each branch, and thus, on the amplitude. A solution to this is the use of a limiting stages based on differential pairs or variable gain amplifiers, [10]. Amplitude limiting becomes difficult in gigahertz circuits unless several of them are placed in cascade [13], but in this conditions the phase and gain mismatch of this chain becomes significant.

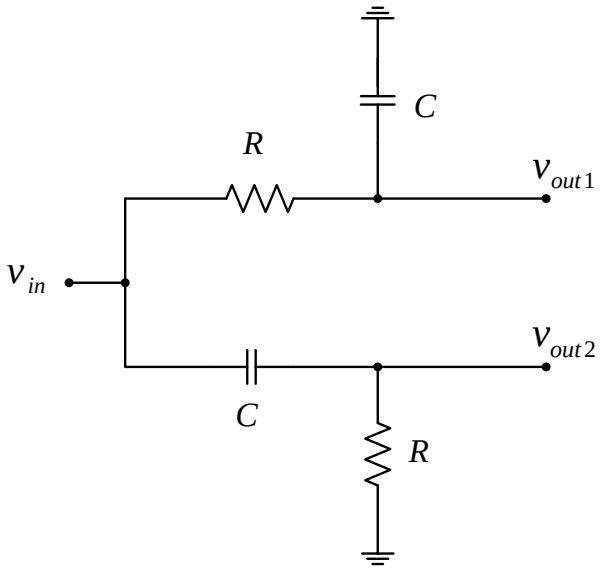

FIGURE 2.6: RC-CR quadrature network.

The phase shift on each branch is given by (2.3). We know that the phase shift of the network (θ) is given by the difference of each stage and is equal to (90°). Assuming there is a mismatch α for the resistance and β for the capacitance on the RC branch we obtain, (2.4).

$$\begin{cases} \Phi_{RC} = -\arctan(\omega RC), \\ \Phi_{CR} = \arctan\left(\frac{1}{\omega RC}\right). \end{cases} \tag{2.3}$$

$$\theta = \frac{\pi}{2} - (\arctan[\omega R(1+\alpha)C(1+\beta)] - \arctan(\omega RC)) \tag{2.4}$$

Applying some trigonometric relationships we get

$$\theta = \frac{\pi}{2} - \arctan\left[\frac{RC\omega(1+\alpha)(1+\beta) - (RC\omega)}{1 + RC\omega(1+\alpha)(1+\beta)RC\omega}\right] \tag{2.5}$$

We can further simplify the equation by assuming small variations, $\alpha << 1$ and $\beta << 1$

$$\theta = \frac{\pi}{2} - \arctan\left(\frac{\alpha+\beta}{2}\right) \tag{2.6}$$

$$\theta = \frac{\pi}{2} - \frac{\alpha + \beta}{2} \tag{2.7}$$

We can also see that the phase and amplitude imbalances do not depend on the load capacitance connected to the outputs of the network, as shown on figure 2.6. Such capacitance only affects the pole frequency but not the phase in each branch, so the phase shift maintains its value 90°. However, a capacitance between both outputs will introduce phase error.

2.3.2 Havens' Technique

To produce quadrature outputs this technique first splits the input signal by approximately 90°, generating signal v_1 and v_2. The signals then go trough soft-limiter stages to equalize the amplitude to obtain $v_1(t) = A\cos(\omega t)$ and $v_2 = A\cos(\omega t + \theta)$. Finally they are added and subtracted making the outputs, as shown on figure 2.7.b), making the output of this circuit equal to :

$$v_{out1} = v_1(t) + v_2(t) = 2A\cos\left(\frac{\theta}{2}\right)\cos\left(\omega t + \frac{\theta}{2}\right) \tag{2.8}$$

$$v_{out1} = v_1(t) - v_2(t) = 2A\sin\left(\frac{\theta}{2}\right)\sin\left(\omega t + \frac{\theta}{2}\right) \tag{2.9}$$

The limiting stages located before and after the signal operations solve the problem of amplitude mismatch caused by an error on the phase shift ($\theta \neq 90°$).

Although the Heavens' technique solves a problem of amplitude on the RC-CR network. This circuit needs two pairs of limiters and two adders, which causes an increase of area and power consumption. This devices also generate unwanted harmonics, even harmonics, which will cause quadrature errors and odd ones will cause amplitude errors. Moreover, the capacitive coupling between the two inputs of the adders will also cause amplitude

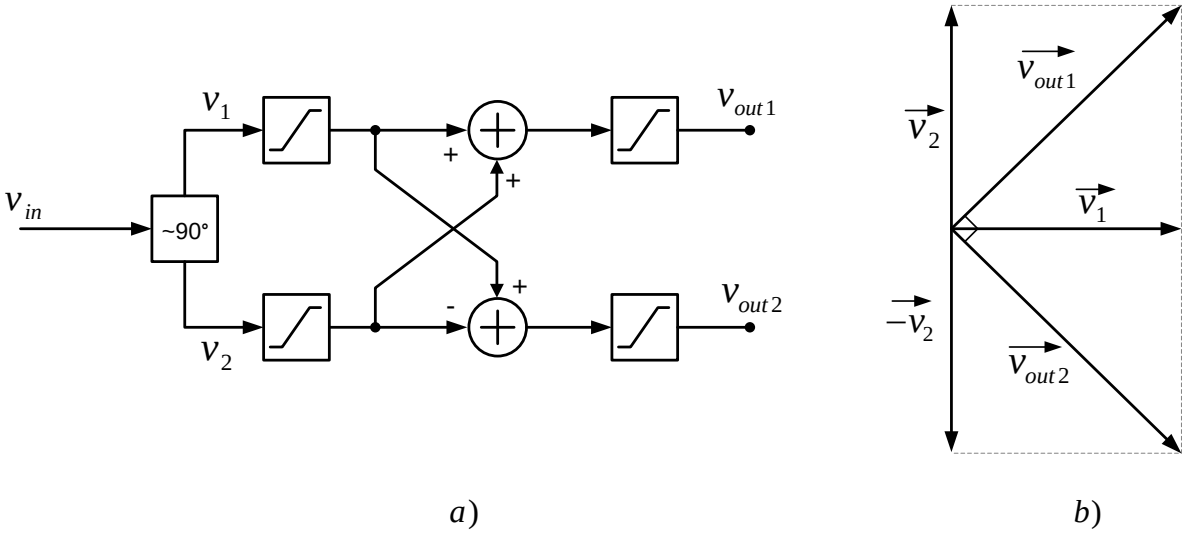

FIGURE 2.7: a) Havens quadrature circuit. b) Phasor diagram.

mismatch. All of these drawbacks make this technique less attractive to use on nowadays systems that demand low power and low area.

2.3.3 Frequency Division

The final method for generating quadrature outputs is frequency division, this approach divides by two a signal with twice the wanted frequency. The division is made using master-slave flip-flops, as shown on figure 2.8. If V_{in} as a duty cycle of 50% then the outputs will have a phase shift of 90°. Although this technique provides a balanced quadrature outputs in a broad frequency range, some problems reside on the solution itself. The generation and division of the signal at twice the frequency may consume substantial power and there is also a limitation of the achievable frequency by the technology. The mismatches in the signal paths trough the flip-flops contribute to the phase error as does the deviation of the duty cycle from 50%.

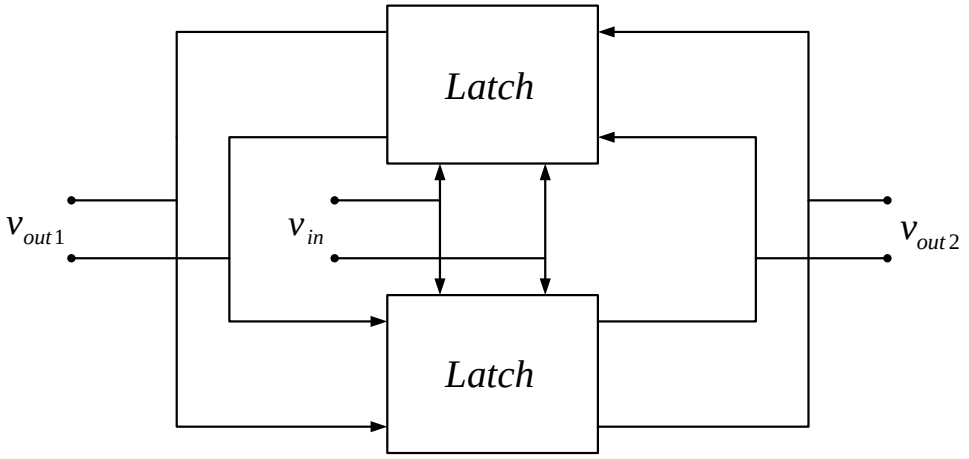

FIGURE 2.8: Frequency divider as a quadrature generator.

There are also other techniques that measure the phase imbalance of the quadrature outputs and correct them, [24]. Some use a delay-locked loop (DLL), where the input signal is split in two paths, one of them delayed by 90°, then a phase detector controls the current in the phase shifter and adjusts the phase different between two split paths. Another calibration is a first order phase shifter with a self-calibration loop to tune each branch of the phase shifter.

In modern communications, voltage controlled oscillator (VCO) architectures with inherent quadrature outputs provide a alternative to the techniques mentioned. This can be accomplished using two cross coupled VCO or a oscillator that has inherent IQ signals, such as, the two integrator oscillator.

Chapter 3

Oscillators

3.1 Introduction

In the first part of this chapter, we review the basics for designing a oscillator. Some important features such as noise and quality factor determine the overall quality and efficiency of a oscillator. It is important to note that, the Barkhausen criterion and the quality factor definition, can only be applied to oscillators with a linear behaviour. We will only discuss basic concepts and how they are affected.

This chapter also introduces different architectures: LC oscillators, RC oscillators and, the Two-Integrator. LC oscillators are known for their low phase noise as opposed to the RC oscillators, but some disadvantages, such as, area and cost make the choice of which architecture to use more difficult.

As mentioned before quadrature outputs are important in nowadays communications, but single LC and RC oscillators cannot produce them. We will discuss how two of these oscillators can generate quadrature outputs, and also, why the two-integrator has inherent quadrature outputs.

3.2 Oscillator Basics

3.2.1 Barkhausen Criteron

A oscillator generates a output signal without an external source. To accomplish that we need a natural oscillator such as a quartz crystal, or a unstable system where his own noise creates a periodic signal.

A feedback circuit, shown on figure 3.1, with a unstable state creates a oscillation. The feedback systems can be positive or negative each one with respective transfer function, (3.1) and (3.2)

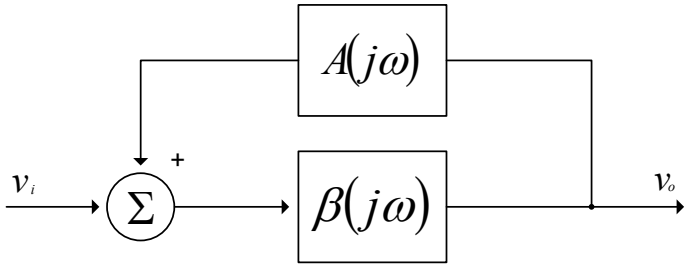

FIGURE 3.1: Feedback system.

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)\beta(j\omega)} \tag{3.1}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)} \tag{3.2}$$

Considering the negative feedback system, the denominator of (3.2) should be zero to achieve a unstable state. We can conclude that the open loop gain $A(j\omega)\beta(j\omega)$ is equal to the unity and since it does not have a imaginary part we get (3.3) in polar form. For the positive feedback $A(j\omega)\beta(j\omega)$ must be equal to -1.

Using complex analysis:

$$A(j\omega)\beta(j\omega) = 1\ e^{0} \tag{3.3}$$

These are the basis for the Barkhausen criterion conditions, which guarantee a stable oscillation:

$$|A(j\omega)\beta(j\omega)| = 1 \tag{3.4}$$

Considering positive feedback

$$\angle A(j\omega)\beta(j\omega) = 0 + 2k\pi, k = 0..n, n \in N \tag{3.5}$$

and negative feedback

$$\angle A(j\omega)\beta(j\omega) = \pi \tag{3.6}$$

These conditions are not enough for the system to start oscillating. For the oscillator start-up, the open loop gain initially must be larger than the unity, (3.7).

$$|A(j\omega)\beta(j\omega)| > 1 \tag{3.7}$$

After the start-up the feedback and the internal noise will allow the oscillator to reach a stable state, when the open loop gain complies the first Barkhausen condition.

3.2.2 Phase Noise

Phase noise is the most crucial factor of a oscillator, it can be seen as the immunity level against nearby interference signals. The phase noise spectral density is higher at the local oscillator frequency ω_0 and falls off at frequencies away from it, as shown on figure 3.2. Phase noise is represented by ($\mathcal{L}(\Delta\omega)$) and is specified in dBc/Hz at a offset frequency $\Delta\omega$ from the carrier ω_0, where dBc is the level in dB relative to the carrier. One way of quantizing this is by doing the ratio between the power in a 1 Hz bandwidth at the offset frequency to the total power of the carrier, (3.8)

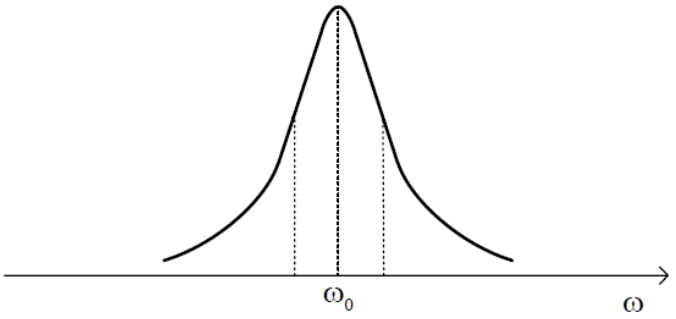

FIGURE 3.2: Phase-noise power spectre.

$$\mathcal{L}(\Delta\omega) = \frac{P(\Delta\omega)}{P(\omega_0)} \tag{3.8}$$

Phase noise in the time domain is called jitter noise. We can see how this noise acts by comparing a noisy sinewave with a relative time grid set by a noiseless sinewave. At the zero crossing baseline we can see the deviations from the rising edges caused by the noise. This serves as basis to a time variant approximation of the phase-noise that will be mentioned, we will also discuss the time invariant approximation of Leeson.

In a receiver the local oscillator is tuned to ω_0, when the downconversion occurs the phase noise of nearby frequencies will also be downconverted. The output signal will be a mix of the spectra of the desired signal and some of the side band spectra of the unwanted signals, as seen in figure 3.3.

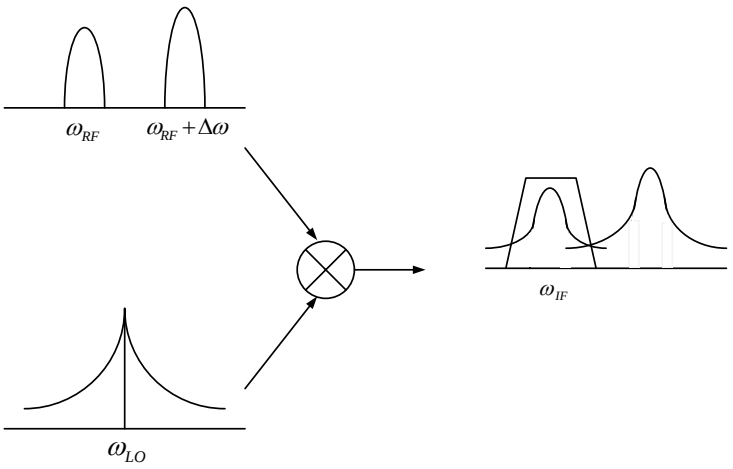

FIGURE 3.3: Phase-noise influence.

Passive and active elements of other blocks of the receiver introduce noise, also voltage and current noise sources through the system influence noise. All this factors make phase noise very difficult to predict. However, the noise sources within the oscillator loop have more influence on phase noise, [25]. They may be enhanced by the sharp frequency selectivity of the loop, and become the dominant source of phase noise. The noise on the loop may also modulate the oscillation frequency.

In an oscillator, phase noise is best described in the frequency domain, where the spectral density is characterized by measuring the noise sidebands on either side of the output signal center frequency. The Single Side Band (SSB) can be divided into three regions as shown on figure 3.4, the first has a slope of -30 dB/decade it represents the noise of active devices on the circuit, the second part goes from ω_1 to ω_2 with a -20 dB/decade slope it is the white noise within the oscillator, finally the last region is the white noise caused by neighbour devices.

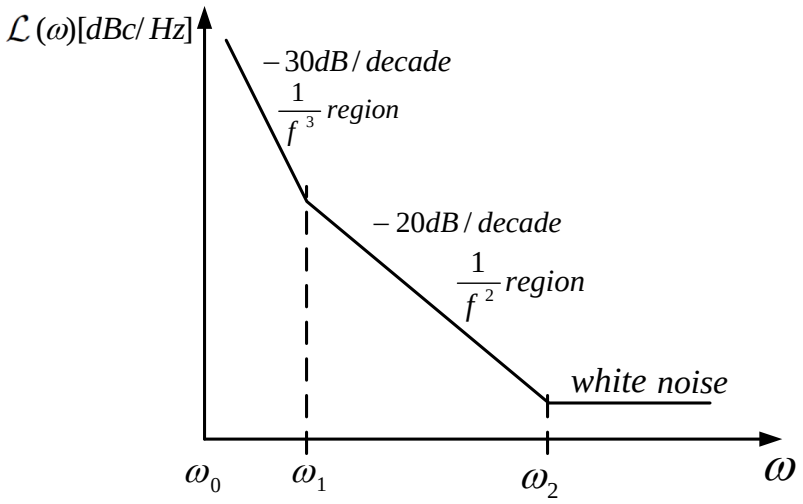

FIGURE 3.4: Phase-noise single side band.

The Leeson-Cutler phase noise model proposed in [9] is the most used and best known model, (3.9). This equation only applies between ω_1 and ω_2 and it is based on the assumption that the oscillator is a linear time invariant system (LTI). This LTI theory provide a important qualitative design but is limited in their quantitative predictive power [8], because the device noise undergoes through multiple frequency translations to become phase noise.

$$\mathcal{L}(\Delta\omega) = 10\log\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{3.9}$$

Where:

k - Boltzman constant;

T - Absolute temperature;

P_S - Average power dissipated in the resistive part of the tank;

ω_0 - Oscillation frequency;

Q - Quality factor;

$\Delta\omega$ - Offset from the carrier;

$\Delta\omega_{1/f^3}$ - Corner frequency between $1/f^3$ and $1/f^2$ zones of the noise spectrum;

F - Empirical parameter called excess noise factor.

When comparing the equation to the spectre of the phase noise, shown on figure 3.4 one can conclude that the white noise and the flicker noise are represented by (3.10). The -20 dB/decade region starts at a frequency equal to half bandwidth of the oscillator, in figure figure 3.4 corresponds to the ω_2 frequency.

$$S(\Delta\omega) = \frac{FkT}{2P_s}\frac{1}{\Delta\omega^2} \tag{3.10}$$

There have been considerations using oscillators as linear time-varying systems on [8, 16], where the following equations were reached, (3.11).

$$\mathcal{L}(\Delta\omega) = \begin{cases} 10\log\left\{\frac{C_0^2}{q_{max}^2}\frac{i_n^2}{8\Delta f\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right\} & \text{for}\,\frac{1}{f^3}\,\text{region} \\ 10\log\left\{10\log\left[\frac{T_{rms}^2}{q_{max}^2}\frac{i_n^2}{4\Delta f\Delta\omega^2}\right]\right\} & \text{for}\,\frac{1}{f^2}\,\text{region} \end{cases} \tag{3.11}$$

Where:

$i_n^2/\Delta f$ - Noise power spectral density;

Δf - Noise bandwidth;

$\Gamma_{rms}^2 = 1/\pi \int_0^{2\pi} |\Gamma(x)|^2 \mathrm{d}x = \sum_{n=0}^{\infty} C_n^2$ - Root mean square value of $\Gamma(x)$;

$\Gamma(x) = C_0/2 + \sum_{n=1}^{\infty} C_n cos(nx + \theta_n$ - Impulse sensitivity function;

C_n - Fourier series coefficient;

C_0 - 0th order of the impulse sensitivity function (fourier series);

θ_n - phase of the nth harmonic;

$\omega_{1/f}$ - Flicker corner frequency of the device;

q_{max} - Maximum charge stored across the capacitor in the resonator.

3.2.3 Quality Factor

Quality factor is a important feature for a oscillator and is related to the phase noise. The most general formula used is (3.12). This equation is normally applied to a RLC resonator. The maximum energy stores is related to the L and C components and the energy dissipated is associated with the resistor.

$$Q = 2\pi \frac{\text{Maximum energy stored in a period}}{\text{Energy dissipated in a period}} \tag{3.12}$$

Leeson defines the Q factor, (3.13), considering a resonant circuit with a -3 dB bandwidth B and a frequency ω_0. In the Leeson-Cutler phase noise model, half bandwidth of the oscillator is taken into account $\omega_0/2Q$. With a high Q factor the bandwidth will be reduced, as seen in figure 3.5, and the influence of the $1/f^2$ noise on the phase noise will decrease making the slope starting to disappear, [9, 16]. When this happens the slopes $1/f^3$ and $1/f^2$ will come close to the carrier frequency and reduces the phase noise.

$$Q = \frac{\omega_0}{B} \tag{3.13}$$

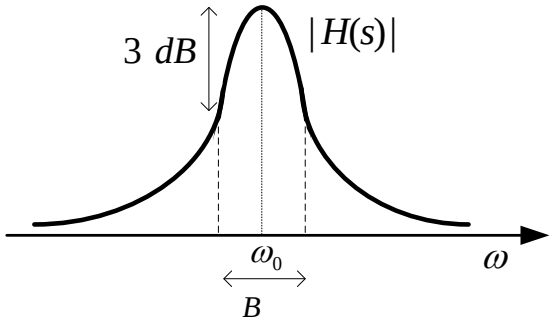

FIGURE 3.5: Q definition for a second order system.

3.2.4 Figure of Merit

Figure of Merit is a characteristic that gives a overall perspective of the oscillator performance, it is usually used in literature for benchmark comparison. It takes into account not only the phase noise but also power consumption and frequency, (3.14), P_{ref} is the reference power level equal to 1 mW and P_{DC} the power consumption in mW. The inclusion of all three aspects help the designer to achieve an optimal and balanced design, [26, 27].

$$FOM = \mathcal{L}_{measured} + 10\log\left(\left(\frac{\Delta\omega}{\omega_0}\right)^2 \frac{P_{DC}}{P_{ref}}\right) \tag{3.14}$$

There is also a figure of merit concerning the layout area, (3.15), where A_{ref} is equal to 1 mm^2 and A_{chip} the circuit area in mm^2, [11, 27].

$$FOMA = \mathcal{L}_{measured} + 10\log\left(\left(\frac{\Delta\omega}{\omega_0}\right)^2 \frac{P_{DC}}{P_{ref}} \frac{A_{chip}}{A_{ref}}\right) \tag{3.15}$$

The FOM of an oscillator provides a qualitative insight on the relations between design parameters, allowing a designer to further optimize the circuit.

There are other FOM that allow a more in depth analysis on the performance of the oscillator, called Oscillator Design Efficiency (ODE), [26, 27]. This benchmark compares

the measure phase noise with a first order estimation of the best phase noise case achievable, (3.16). This equation is used for LC oscillators, but it as been modified specifically for N-stage ring oscillators [27], such as the Two Integrator (3.17).

$$ODE_{LC} = \mathcal{L}_{measured} - 10\log\left(\left(\frac{kT}{2P_{DC}}\frac{1}{Q^2}\frac{\Delta\omega}{\omega_0}\right)^2\right) \tag{3.16}$$

$$ODE_{ring} = \mathcal{L}_{measured} - 10\log\left(\left(\frac{N^2kT}{4P_{DC}}\frac{1}{(\frac{\pi}{2})^2}\frac{\Delta\omega}{\omega_0}\right)^2\right) \tag{3.17}$$

3.3 LC Oscillators

LC oscillators are known for having a quasi linear behaviour and low phase noise, but because of its elements the circuit area is larger when compared with RC oscillators.

A basic circuit is shown figure 3.6, it features two active RF components acting as amplifiers and four passive elements (L and C). The transistors act as switches for conducting the current into either branch of the oscillator.

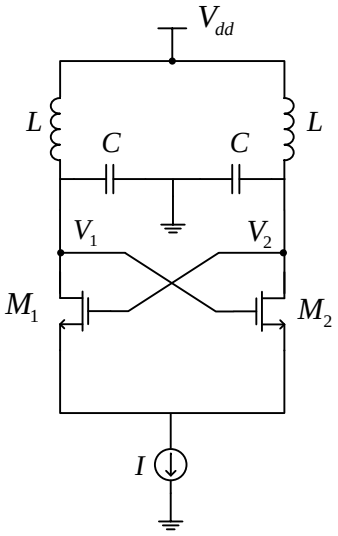

FIGURE 3.6: LC oscillator circuit.

Since the LC oscillator as a quasi linear behaviour, the Barkhausen criterion applies. At the carrier frequency the amplitude of the loop must be one and the phase, zero. The

last condition is complied because the capacitors give a -90° and the inductors a 90°, giving a total of 0°. To understand how the first condition is attained we can use the behaviour model of this oscillator presented in figure 3.7.

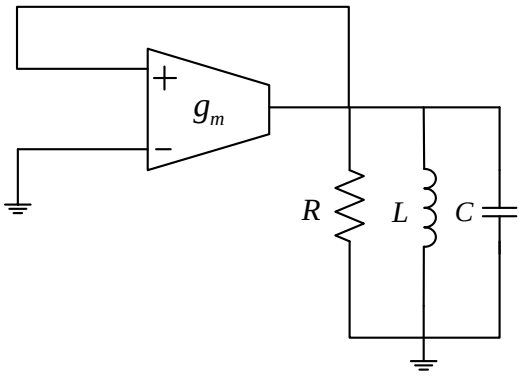

FIGURE 3.7: LC oscillator behaviour.

The open loop gain can be extracted using the impedances of the circuits, the transfer function $A(j\omega)$ comes from the transconductance g_m of the transistors. The feedback transfer function (3.18) is formed by the RLC impedance, where R represent losses. At ω_0 the $B(j\omega_0)$ equation only as the real part so the open loop gain $|A(j\omega_0)B(j\omega_0)|$ is equal to $g_m R$ and by the first Barkhausen condition, $g_m R = 1$. Since the g_m cancels R we can calculate the frequency of this oscillator considering only a LC resonator, (3.20). The Q factor is given by (3.19)

$$B(j\omega) = \frac{R}{1 + j\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)Q} \tag{3.18}$$

$$Q = R\sqrt{\frac{C}{L}} \tag{3.19}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.20}$$

Although the condition $g_m = 1/R$ is sufficient for a steady-state oscillation, we need a small difference between them for the oscillator start-up. Figure 3.8 shows the effect for

a g_m value different than $1/R$, the transconductance must be higher than $1/R$, making $|A(j\omega_0)B(j\omega_0)| > 1$ thus complying with the condition mentioned before.

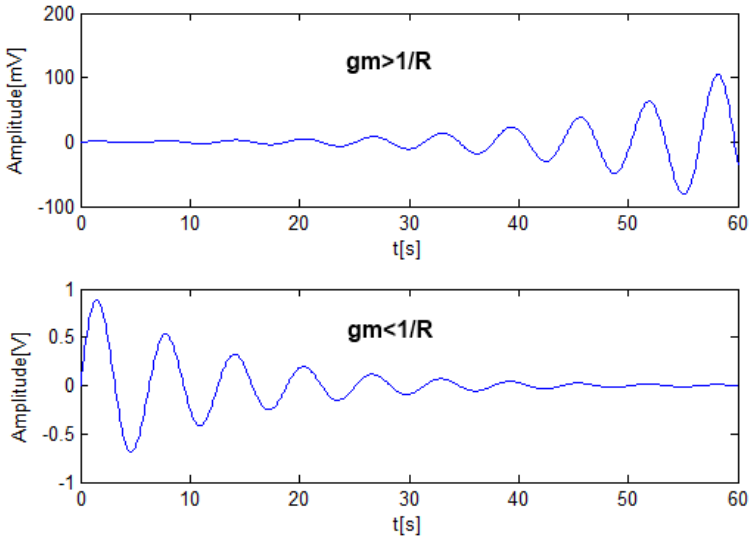

FIGURE 3.8: Start up condition.

3.3.1 Coupled LC Oscillators

To obtain quadrature outputs we need to couple two symmetric LC oscillator, [15]. This can be done by introducing two new differential pairs [10] acting as soft-limiters. Figure 3.9 shows the coupled version of the LC oscillator circuit. We also need a cross coupled connection to give a -180° phase shift, this way we comply with the negative feedback loop phase condition of the Barkhausen criterion.

The gates of transistors M_c connect to the outputs of a singular LC and the drains connect to the outputs of the other oscillator. When one pair senses the voltage variation at the gate, it varies the current injected in the other oscillator. The oscillation frequency will be synchronized in both oscillators and the outputs will have a phase shift of 90°.

Although single LC oscillator have low phase noise, when coupled they show some phase noise degradation. Besides this disadvantage there is also the difficulty of implementing them with a low supply voltage and also the large area occupied by the circuit. To give a

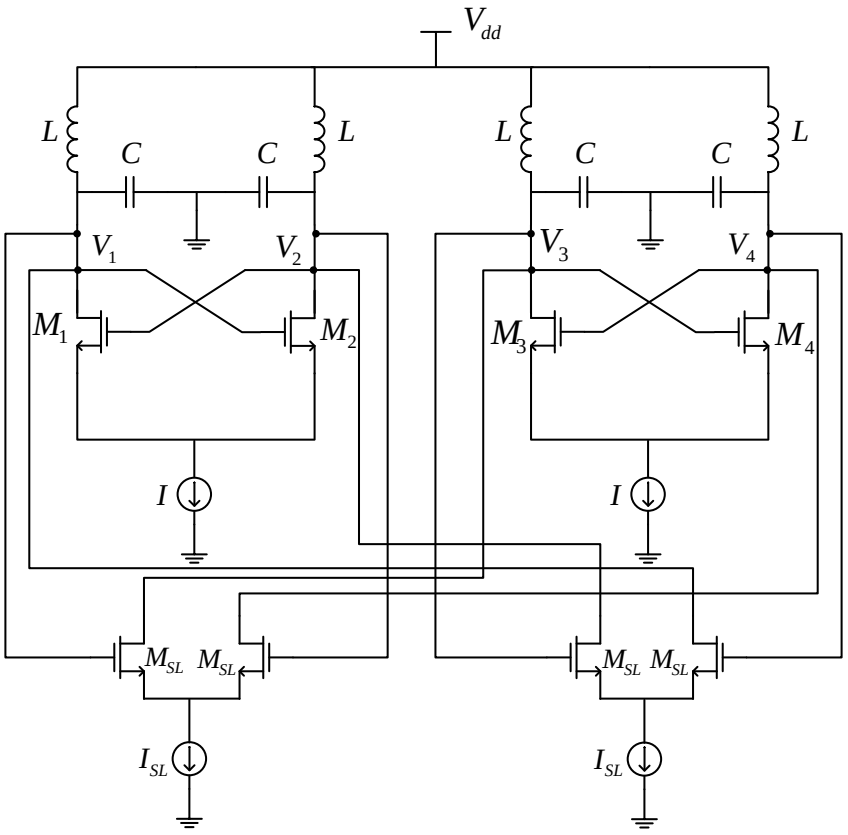

FIGURE 3.9: Coupled LC oscillator circuit.

perspective of how large the circuit is lets say a RC oscillator can occupy the same layout area as an inductor.

LC oscillators need a strong coupling to be able to synchronize both outputs with a 90°. To increase the coupling, the gates size of the coupling transistors should be increased. When doing that we are also increasing the parasitics on those transistors, making the oscillation frequency decrease and degrading the phase noise. Due to this disadvantage coupled RC oscillators can have similar phase noise performance to that of a LC coupled oscillator, [10].

3.4 Relaxation Oscillators

RC oscillators have become more important in recent years due to the reduced space and the improvement of phase noise, when coupled. In this section and the following,

we will discuss two different RC oscillators, one with a relaxation (non-linear) behaviour oscillator and one oscillator with inherent quadrature outputs (Two-Integrator). Initially we approach the behaviour of those oscillators using ideal blocks, then one basic implementation to allow a more deep study at circuit level.

A basic operation of an RC oscillator, with a non-linear behaviour, can be describe using a high level structure shown in figure 3.10, to model its behaviour. The model which is composed by a inverted Schmitt-trigger and a integrator. The Schmitt-trigger output is fed to the integrator, and its input is the output of the integrator. The Schmitt-trigger also imposes a threshold to the integrator, making it change his behaviour when that value is reached.

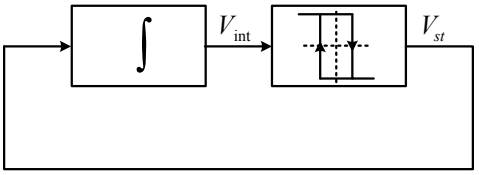

FIGURE 3.10: High level model.

The output V_{st} is a square wave that depends on the integrator signal, this block is basically an saturated amplifier that forces a value at the output, acting like a memory element. Afterwards the square wave is integrated creating a triangular wave (V_{int}), when it reaches a threshold the inverted Schmitt-trigger changes the signal value of V_{st} causing a variation on the behaviour of the integrator. We can assume two states, one corresponds to the ascending signal at the output of the integrator and the other the descending signal, as seen in figure 3.11.

The amplitude value at the output is given by the Schmitt-trigger and the frequency depends on the time the triangular wave reaches both thresholds.

A basic and well known implementation of an RC oscillator is shown in figure 3.12, because of its simplicity there are less noise sources which is essential for very high frequencies. The noisier element is the Schmitt-trigger, because it will perform a high speed switching during the oscillation. When comparing this circuit with the high level model, the integrator is implemented by the capacitor and the two current sources and the Schmitt-trigger by the resistors and MOSFET transistors.

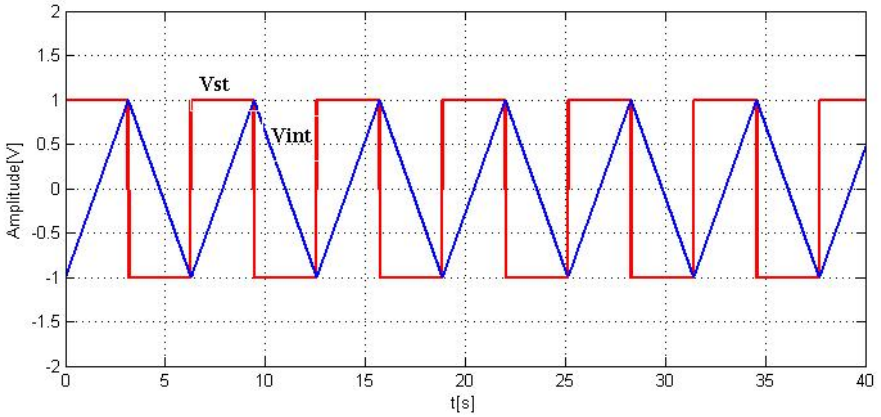

FIGURE 3.11: High level model signals.

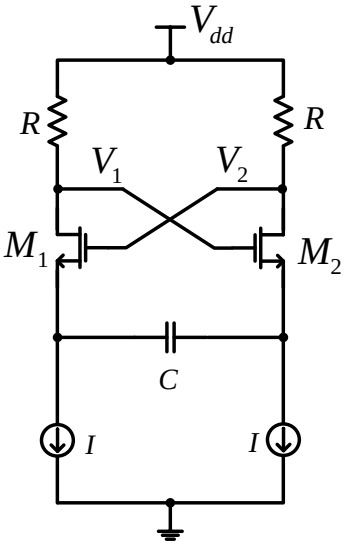

FIGURE 3.12: Relaxation Oscillator Implementation.

To understand the relaxation operation, we consider a initial state with transistor M_1 on the cut-off region, as presented in figure 3.13a, this means no current is flowing through it, making V_1 equal to V_{dd} it is also assumed that the transistors change working region instantly. The voltage at the gate of transistor M_2 is greater than the one at the source, so $V_{gs2} > 0$, moreover there is a current of value $2I$ on this transistor making V_2 equal to $V_{dd} - 2RI$. Since at first the capacitor is charged the source voltage of M_1 is higher than the gate voltage, making $V_{gs1} < 0$. One of the currents on transistor M_2 is discharging the capacitor making the voltage drop at the sources of the transistors, when this happens the oscillator changes state, because there will be a point when the voltage at the source of M_1 is lower than the voltage at the gate, so $V_{gs1} > 0$. The current will pass through M_1

and the voltage at the gate of M_2 becomes $V_{dd} - 2RI$, moving the transistor to the cut-off region, as shown in figure 3.13b. The process described is repeated. This behaviour is considered non linear, RC oscillator are known as relaxation oscillators when working in this behaviour. It has been proved that they also have a quasi linear behaviour.

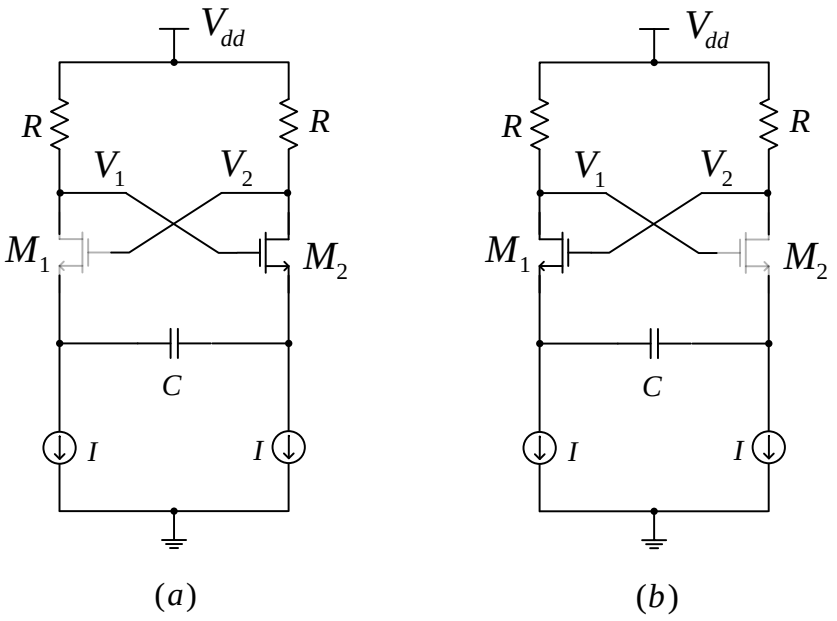

FIGURE 3.13: Relaxation Oscillator Basic Operation.

The differential output of the oscillator is seen from the drains of the transistors and is equal to $V_1 - V_2$, assuming the first state is figure 3.13a and the second state figure 3.13b, one can obtain the results shown on (3.21). This values correspond to the threshold limits caused by the Schmitt-trigger.

$$V_{out} \begin{cases} V_{dd} - (V_{dd} - 2RI) = 2RI & \text{if first state} \\ V_{dd} - 2RI - V_{dd} = -2RI & \text{if second state.} \end{cases} \tag{3.21}$$

The voltage drop on the capacitor varies accordingly to the current that flows through it, making the integration constant (k_{int}) dependent on the current and capacitor values, (3.22), this constant influences the frequency of the oscillator and is equivalent to the slope of the triangular wave. Another important element in the frequency is the peak to peak amplitude of the triangular wave, from (3.21) with its value being given by $4RI$. With both this elements we can conclude the following expression for the frequency, (3.23).

$$k_{int} = \frac{I}{C} \tag{3.22}$$

$$f_0 = \frac{I}{2C(4RI)} = \frac{1}{8RC} \tag{3.23}$$

Transistors M_1 and M_2 don't switch between the cut-off region and the saturation region instantly. There is a period of time where the transistors act as resistors (triode region), which is one of the noise sources of the circuit. At higher frequencies, reduced C value, the transistor parasitics will influence the Schmitt-trigger input impedance. Instead of having just a real part there is also a positive imaginary equivalent to a inductor. The imaginary part is then canceled by the capacitor impedance, making the oscillator have a quasi linear behaviour, [2], where the Barkhausen conditions apply. With this behaviour instead of having a square wave at the output (relaxation oscillator) the oscillator will have a sinusoidal signal.

3.4.1 Sinusoidal and Relaxation behaviour

Using the basic RC oscillator we can make the following small signal analyses presented in figure 3.14.

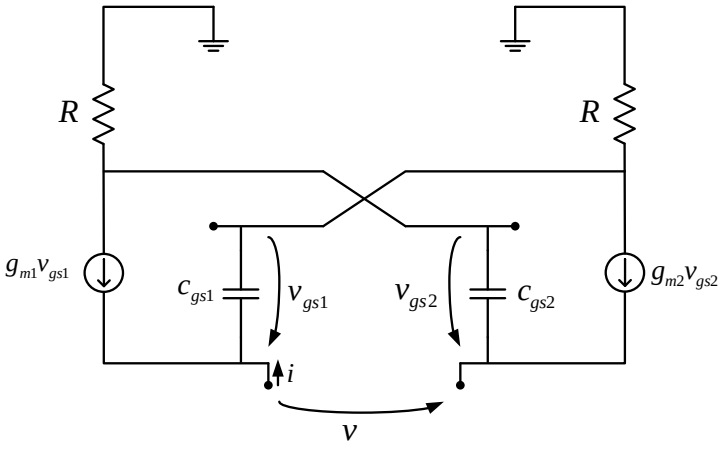

FIGURE 3.14: Small signal analysis of a RC oscillator.

$$z_{in} = \frac{(C_{gs}s + G)}{G}\frac{(g_{m1} + g_{m2})}{g_{m1}g_{m2}} - \frac{2}{G} \tag{3.24}$$

Where $G = 1/R$. The characteristic equation is the sum of impedances, (3.25). Substituting (3.24) in (3.25) we obtain (3.26)

$$\left(\frac{1}{sC}\right) + z_{in} = 0 \tag{3.25}$$

$$s^2 + \frac{1}{RC_{gs}}\left(1 - 2R\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}}\right)s + \frac{g_{m1}g_{m2}}{RCC_{gs}(g_{m1}g_{m2})} = 0 \tag{3.26}$$

When the oscillation starts we can consider that the current does not flow more in one branch than the other of the differential pair, so the transconductance of both transistor are equal, (3.27). This allow us to rewrite (3.25) into (3.28).

$$g_{m1} = g_{m2} = g_{m0} = \sqrt{\frac{2I_d}{K_n\frac{W}{L}}} \tag{3.27}$$

$$s^2 + \frac{1}{RC_{gs}}(1 - Rg_{m0})s + \frac{g_{m0}}{2RCC_{gs}} = 0 \tag{3.28}$$

The oscillation will start if the roots of (3.28) are located in the right half of the s plane, meaning $g_{m0} > 1/R$. The oscillation will have the frequency (3.29).

$$\omega_0 = \sqrt{\frac{g_{m0}}{2RCC_{gs}}} \tag{3.29}$$

The roots of (3.28) are equal to (3.30). If capacitor C varies and all the other parameters are constant the roots will move between planes. For small values of C they are complex-conjugate, so the oscillator will have a quasi-linear behaviour and sinusoidal outputs. When increasing C the poles start to arrive the positive real axis, this happens when the square root of (3.30) is zero, making $C = (2C_{gs}g_{m0}R)/(g_{m0}R - 1)^2$ at this value

the oscillator starts to have a non linear behaviour. With further increase of C the roots are moving along the positive real axis arriving to the final values of $s_1 = 0$ and $s_2 = (Rg_{m0} - 1)/(RC_{gs})$. The transition from one type of behaviour to another is smooth, it represents a gradual increase of distortions on the sinusoidal wave, then the oscillations start to have a square waveform, just like relaxation oscillators.

$$s_{1,2} = \frac{g_{m0}R - 1}{2RC_{gs}} \pm \sqrt{\left(\frac{g_{m0}R - 1}{2RC_{gs}}\right)^2 - \frac{g_{m0}}{2RCC_{gs}}} \tag{3.30}$$

Before moving into the oscillation differential equation we need to do the following approximation, (3.31), where i is the capacitor current. Then, we can write for this current the differential equation (3.32). Introducing the normalized variable $x = i/(\sqrt{2}I)$ and notations $\delta_0 = (Rg_{m0} - 1)/(2RC_{gs})$ and $\delta_2 = g_{m0}/(2C_{gs})$ the equation is reduced to (3.33).

$$\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}} \approx \frac{g_{m0}}{2}\left[1 - \left(\frac{i}{\sqrt{2}I}\right)^2\right] \tag{3.31}$$

$$\frac{d^2}{dt^2} + \frac{1}{RC_{gs}}\left(1 - Rg_{m0}\left[1 - \left(\frac{i}{\sqrt{2}I}\right)^2\right]\right)\frac{d}{dt} + \omega_0^2 i = 0 \tag{3.32}$$

$$\frac{d^2x}{dt^2} - 2(\delta_0 - \delta_2 x^2)\frac{dx}{dt} + \omega_0^2 x = 0 \tag{3.33}$$

The solution to (3.33) is (3.34). The amplitude of the voltage between the drain resistor will be (3.35).

$$x = 2\sqrt{\frac{\delta_0}{\delta_2}}\sin f_0 t = 2\sqrt{1 - \left(\frac{1}{Rg_{m0}}\right)}\sin f_0 t \tag{3.34}$$

$$V_{dm} = 4\sqrt{2}I\sqrt{1 - \left(\frac{1}{Rg_{m0}}\right)} \tag{3.35}$$

3.4.2 Coupled RC oscillators

Like LC oscillators, to obtain quadrature outputs we need to connect two symmetrical RC oscillators. The connection is made using a soft-limiter at the output of the integrator, if we increase its gain then we will obtain a square wave signal at the output. Unlike the Schmitt-trigger that only changes when a threshold is reached, the soft-limiter saturates when the triangular wave goes above zero. This way we obtain a square wave with a 90° difference from the Schmitt-trigger output.

Figure 3.15 shows a high level block diagram of the coupled RC oscillator. The output of the soft-limiter is used to synchronize the other RC oscillator. Its square signal is added to the triangular output signal of the other integrator, then this new signal goes to the Schmitt-trigger creating a feedback structure. This way both outputs have always a 90° phase shift and the same frequency.

The resulting wave of the signal addition, assumes a important part on the overall noise. This signal as a steeper slope and defines each oscillator state transitions, which means the switching times are less sensitive to noise [10]. As mentioned, the higher the gain of the soft-limiter the more square the output becomes, and thus, increasing the slope, making the oscillator less sensitive to noise.

At circuit level the soft-limiter is implemented by a differential pair, shown on figure 3.16. This coupling method as the same features as the one presented on the LC oscillators, but in this case the gates are connected to the capacitor terminals. When the voltage at the gate varies, the current on the other oscillator also changes. To see the how it influences the output amplitude, lets analyse one of the oscillators when transistor M_1 is off and M_2 is on. As we seen before the M_1 would have a voltage equal to V_{dd} and the M_2 branch $V_{dd} - 4RI$, but in a coupled version the outputs will be (3.36), with the current i_{sl1} lower than i_{sl2}.

$$\begin{cases} v_1 = V_{dd} - i_{sl1}R \\ v_2 = V_{dd} - 2RI - i_{sl2}R \end{cases} \tag{3.36}$$

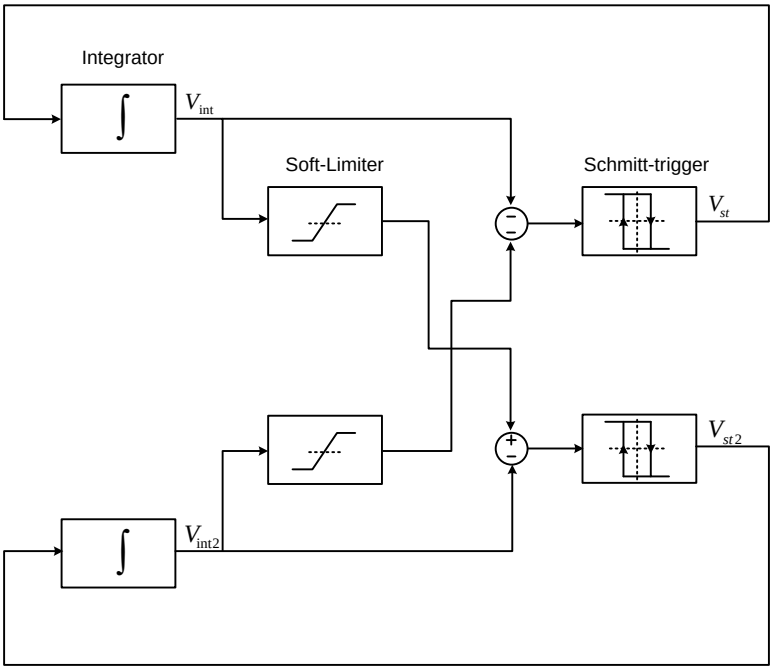

FIGURE 3.15: High level model of quadrature RC oscillator.

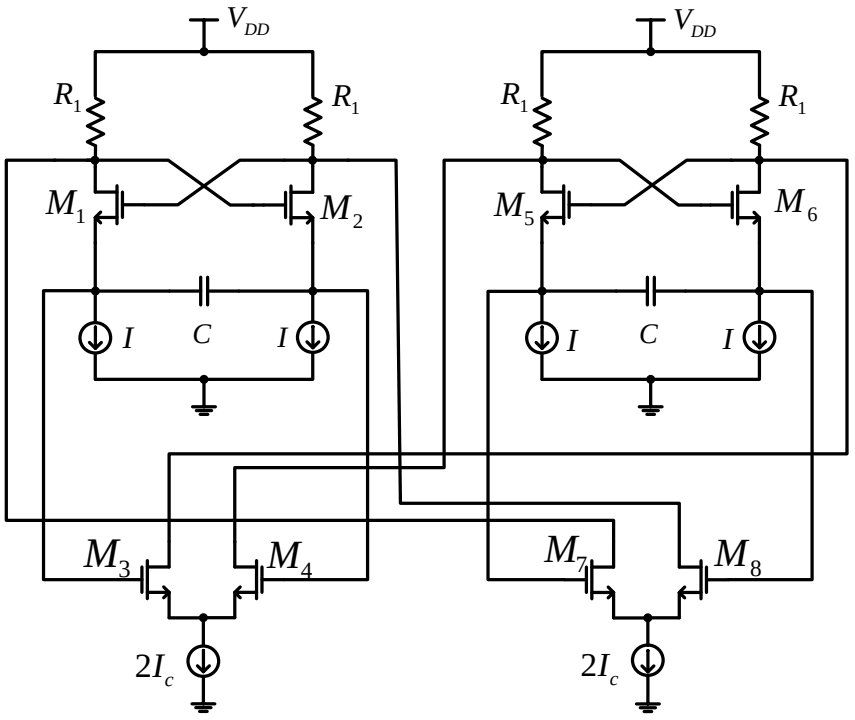

FIGURE 3.16: Quadrature RC oscillator circuit.

When coupling two symmetrical oscillators, one of the new differential pairs must be cross coupled to guarantee the synchronization of both oscillators and, if in the quasi linear behaviour, maintain the Barkhausen conditions. Coupling will also introduce some

changes in the single RC oscillator performance. It adds new noise sources due to the new active elements, but the advantages given are superior. The phase noise improves, but on the other hand, the frequency is reduced.

The supply voltage is decreasing this combine with the need to use low power circuits. From (3.36) we can see how troublesome it will become for implementing coupled oscillators, by introducing new differential pairs we need to be careful about the supply voltage. Some new coupling techniques have been developed to solve this problem. Instead of using a current and a differential pair, the coupling is made using capacitors, this reduces not only the power consumption but also some noise sources.

In recent years coupled RC oscillators have become the subject of many studies, due to the good performance, low area, and quadrature outputs. Coupled LC oscillators have the same performance as RC but occupy a larger area. As mentioned many times the goal is to attain a single chip transceiver, this oscillator type combined with CMOS technology allows that. Many RC architectures have been developed and some are being restudied with the goal to reduce power consumption, improve phase noise and increase tunning frequency.

3.5 Two-Integrator Oscillator

The Two-Integrator oscillator unlike the previous ones, generates quadrature outputs without the need of a coupling circuit, but as a result it only works with quadrature outputs. Although the operation is similar to RC oscillators the structure is different, the Schmitt-trigger is substituted by another integrator.

At a high level model the two integrator oscillator can be seen as two stages, each with an ideal integrator and a amplifier. These two stages are in cascade, and the output of the second stage is inverted and fed back to the first stage, as shown on figure 3.17. Depending on the amplifier, the oscillator has two types of behaviour, non linear and quasi-linear [10, 27].

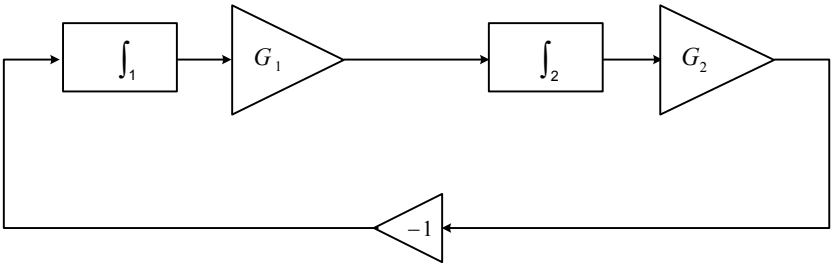

FIGURE 3.17: High level study of two integrator oscillator.

At circuit level each integrator is implemented by a capacitor and a differential pair (transistors T_f) and produces a phase shift of -90°, due to the capacitor impedance $\frac{1}{j\omega C}$. The signal inversion, is made by the cross wired connection between the two stages, as shown in figure 3.18 producing an extra phase shift of -180°, which guarantees that the oscillator only works with quadrature outputs.

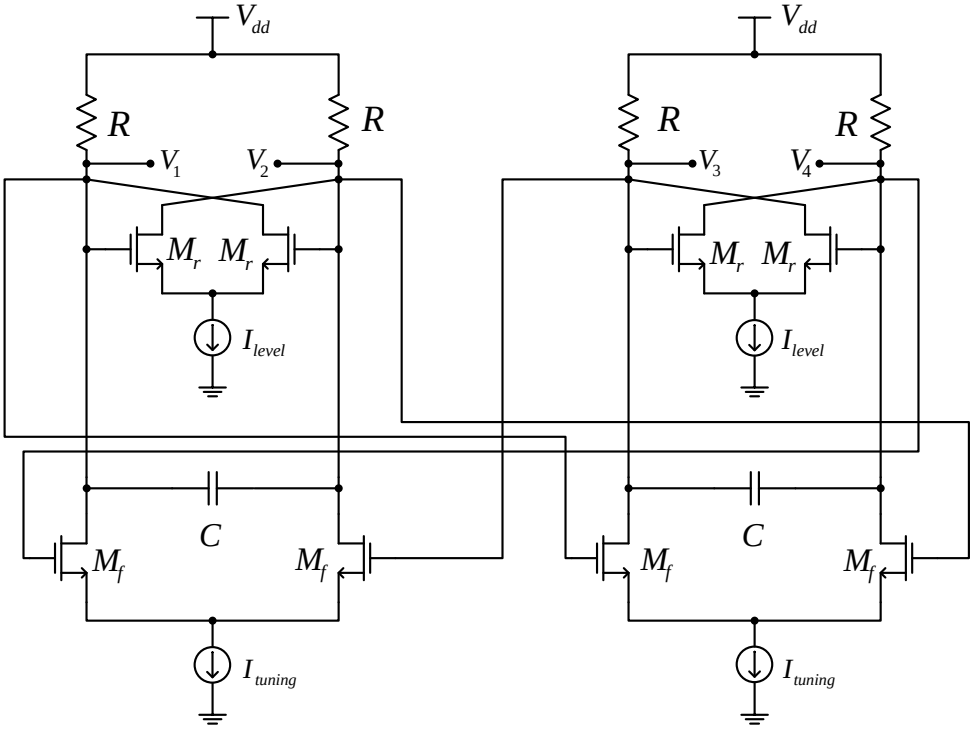

FIGURE 3.18: Two integrator oscillator.

3.5.1 Non Linear behaviour

3.5.1.1 High Level Study

For the oscillator to have a non linear behaviour, the differential pair made by transistors T_r must be in the saturation region of figure 3.20. When increasing the current I_{level}, the transconductance $g_m = \frac{2I_d}{V_{dsat}}$ also increases, making the slope steeper and saturating the outputs more easily, (3.37). In the saturation state the output will form a square wave, depending on the value of the input signal (if it is positive or negative). Then the square wave is integrated resulting on a triangular wave. This behaviour is similar to the one seen on a relaxation oscillator.

The lower differential pair determines in which way the current flows through the capacitor, depending on the voltage at his terminals. Transistors T_f will change their working regions, depending on the signal at the gate. In theory both transistor work as a switch, when one is open the other is closed, so all the current flows through the latter one. In reality both transistors are conducting, as shown on figure 3.19, but there is more current in one of them.

Since the current is always changing, the capacitor is charging in different directions repeatedly thus creating the oscillation frequency, given by (3.38). The upper differential pair has the same behaviour delivering $-I_{lim}$ and I_{lim} with a 50 % duty cycle. In this case the oscillator amplitude is (3.39).

$$I_{out}(V_{in}) \begin{cases} I_{lim} = g_m V_{lim} & \text{if } V_{in} \geq V_{lim}, \\ g_m V_{in} & \text{if } -V_{lim} < V_{in} < V_{lim}, \\ -I_{lim} = -g_m V_{lim} & \text{if } V_{in} \leq -V_{lim}. \end{cases} \tag{3.37}$$

$$\omega_0 = \frac{I_{tuning}}{2CV_{out}} \tag{3.38}$$

$$V_{out} = RI_{level} \tag{3.39}$$

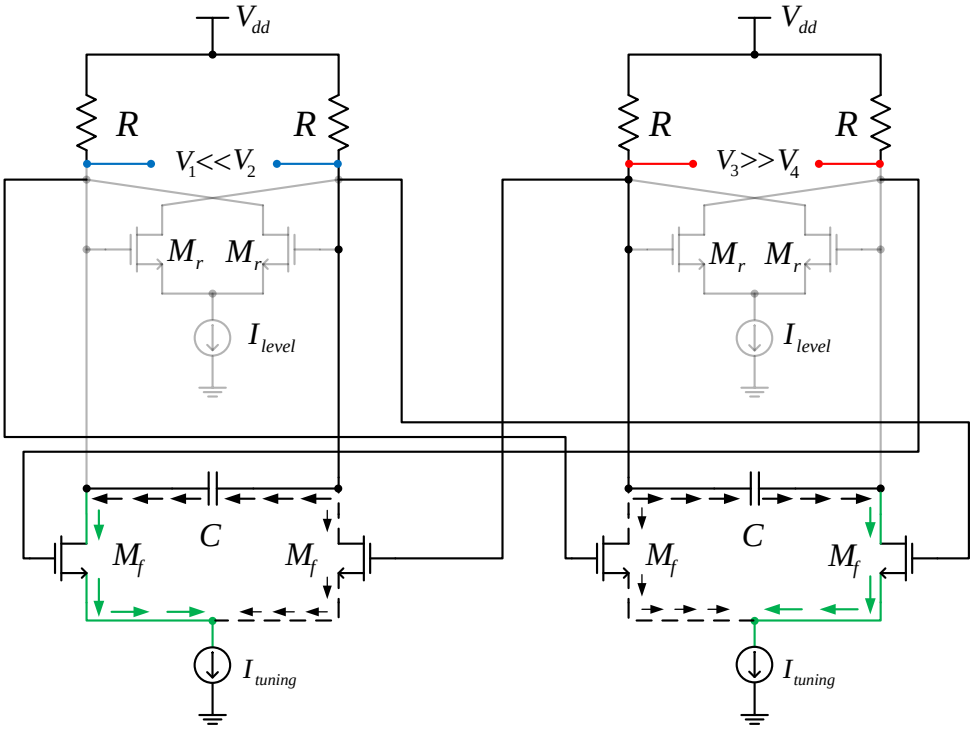

FIGURE 3.19: Current flow.

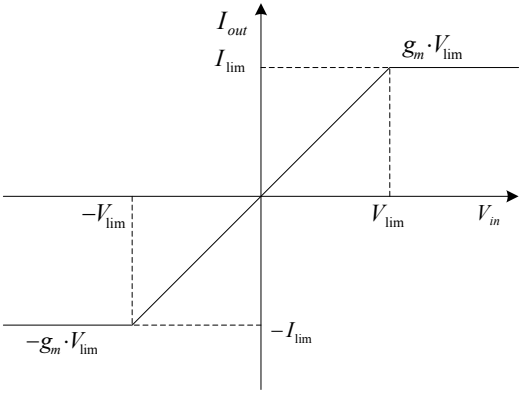

FIGURE 3.20: Ideal transfer characteristic of differential pair.

When the current I_{level} reaches a certain value, the differential pair independently of the input will always saturate. This behaviour is close to the one of a Schmitt Trigger, so it is possible to introduce a saturated amplifier in the high level model and thus obtaining figure 3.21. The outputs of each integrator determines the input signal of the other integrator. Just like relaxation oscillators the wave forms are rectangular at the amplifier output and triangular at the integrator output.

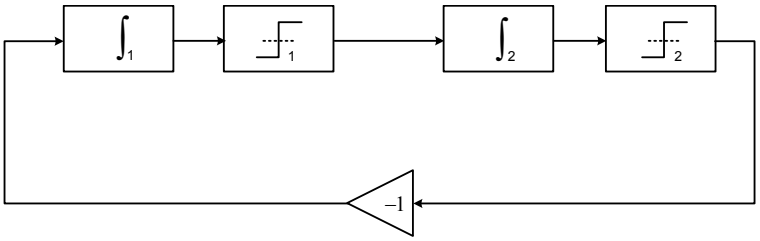

FIGURE 3.21: High Level model for the Two-Integrator oscillator with non linear behaviour.

3.5.2 Quasi Linear behaviour

3.5.2.1 High Level Study

In the previous behaviour the amplifier generated a square wave, as we all know to obtain a perfect square wave we need a infinite number of harmonics. This generation of unwanted harmonics cause a degradation of the phase noise. To obtain the best performance, the two integrator oscillator should have a quasi linear behaviour.

In this behaviour both the differential pairs work in the linear region of figure 3.20, giving sinusoidal outputs. The amplifier can be replaced in the high level model by a soft-limiter, as shown on figure 3.22.

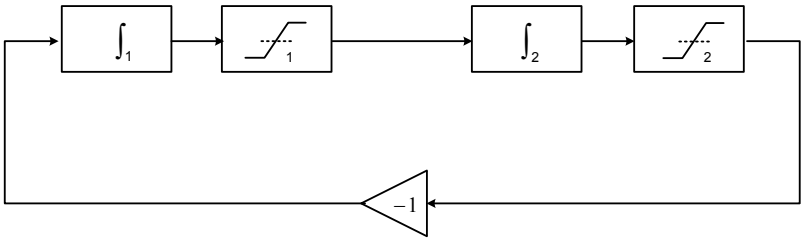

FIGURE 3.22: High Level model for the Two-Integrator oscillator with linear behaviour.

The resistor is used to obtain a current on the circuit and limit the amplitude signal, but by using it we introduce noise and create an unwanted real part on the poles. To compensate that, we use the differential pair of transistors M_r ([10, 27]) from figure 3.19, his equivalent impedance is given by (3.40), this value is obtained by doing the small signal analysis, presented on figure 3.23. The cross wire cancels the real part of the poles to, theoretically, obtain only the imaginary part. To increase the g_m to compensate the real part we can increase the current I_{level}. If we over-compensate the oscillator will have a non

linear behaviour, on the other hand, if a balanced compensation is made the differential pair avoids saturation.

$$r_x = \frac{v_x}{i_x} = -\frac{2}{gm} \tag{3.40}$$

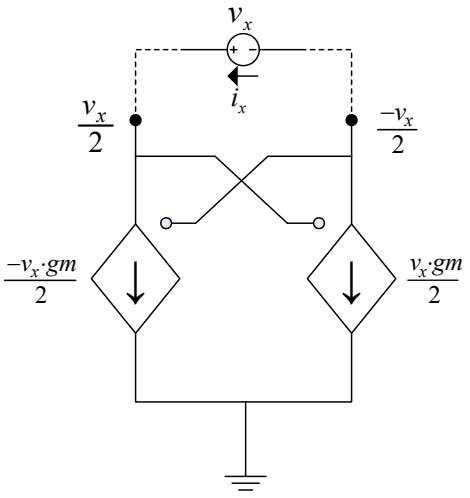

FIGURE 3.23: Small signal analysis of differential pair.

Observing the small signal analysis of a transconductance one can see that is equivalent to a slope as shown on (3.41). The v_{gs} of transistor T_r is always changing and therefore the g_m also changes, as seen in figure 3.24. As mentioned before the role of this transconductance is to cancel the real part caused by the resistors, since their value is always changing, the poles will move between the stable and unstable region. This is one of the noise source that contribute to the phase noise, since in reality it is impossible to obtain a constant frequency at the output.

$$g_m = \frac{\partial i_d}{\partial v_{gs}} \tag{3.41}$$

Figure 3.25 represents a practical approach of the two-integrator in the linear operation. Resistors R_{eq} model all the resistors in one stage and also represents any losses in the circuit.

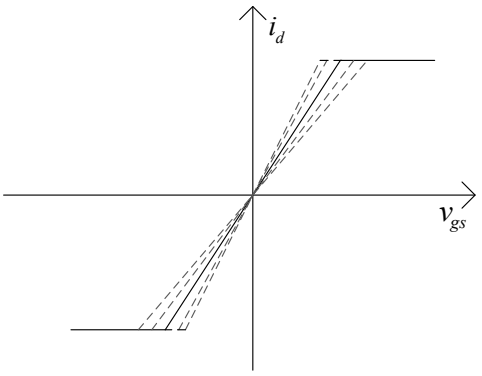

FIGURE 3.24: Small signal analysis of transconductance.

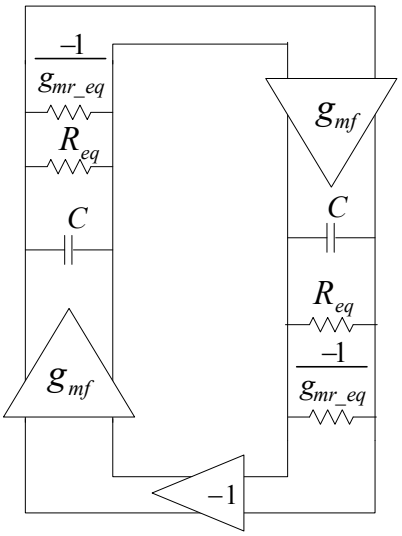

FIGURE 3.25: Linear model.

This differential implementation helps to calculate the transfer function of the system. Assuming that the real part is canceled (3.42), we can obtain the loop gain equation, (3.43). In [27] is given a more detailed approach without the resistor cancellation.

$$\frac{1}{g_{mr_eq}} = R \tag{3.42}$$

$$|H(j\omega)| = \frac{g_{mf}^2}{\omega^2 C^2} \tag{3.43}$$

To guarantee a stable oscillation on quasi linear behaviour, the oscillator must comply to both conditions of the Barkhausen criterion mentioned early. We considered the direct

coupling, meaning a positive feedback, so the second condition says the phase shift must be equal to a multiple of 360°, Equation 3.5. Each capacitor creates a phase shift of 90°, since we have two, the total will be 180°, there is also a signal inversion block that adds a phase shift of 180°. This complies to the second condition of the criterion.

The oscillation frequency is obtained by applying the Barkhausen condition,(3.44). Through the equation one can conclude that there are two ways of changing the value of the frequency, one is changing the capacitor value and the other the current I_{tuning} that consequently changes the transconductance of the transistor T_f. If the capacitor value is too low, the parasitic capacitors of the transistors will influence the frequency, making the value of the capacitor higher and thus lowering the frequency.

$$\omega = \frac{g_{mf}}{C} \tag{3.44}$$

Assuming that the current in the differential pair is equal to the source current the oscillator amplitude is given by (3.45). When working with a non linear behaviour we will have the maximum output amplitude possible. In the linear behaviour the amplitude is limited by the slope of the amplifier. To achieve a optimum point, the current I_{level} must be close to saturation, [27]. But this brings some disadvantages, the power consumption increases and the FOM worsens and there is the risk of entering the non linear region.

$$V_{out} = RI_{level} \tag{3.45}$$

Chapter 4

Circuit Design and Implementation

This is the main chapter of this thesis. We will present the designed RC oscillators circuits and their simulation results. The first two are relaxation oscillators implementations and the last circuit is a ring oscillator (Two-Integrator).

The first circuit shows a wideband MOS quadrature oscillator with two coupled relaxation oscillators, also called multivibrators. Two different forms of coupling (soft and hard) are implemented and compared. We investigated the influence of capacitor and current mismatches in quadrature errors. In the last part we will analyse how the multivibrator locks with a external synchronizing harmonic.

The second circuit is a simple RC oscillator with some circuit modifications, based on known techniques and a new method for reducing the phase noise. The influence of each technique will also be discussed.

The last circuit is a fully integrated CMOS two-integrator with low area and power consumption. The design of some components in CMOS will be discussed. The layout of the circuit in a 130 nm technology is also presented.

4.1 CMOS Current Controlled Quadrature Oscillator

This oscillator is intended for use in the WMTS, which establishes wireless communication between an externally medical device and other equipments. There are three frequency band allocated to WMTS: 608 - 614 MHz, 1395 - 1400 MHz and 1427 - 1432 MHz.

4.1.1 Sinusoidal and Relaxation Behaviour

The circuit in figure 4.1 is based on the circuits shown on [3, 4], which was known for having a reliable and stable behaviour. As mentioned early, with MOS technology and high frequencies the circuit is able to operate with a quasi linear behaviour, and the non linear behaviour should be considered the limit form of sinusoidal behaviour.

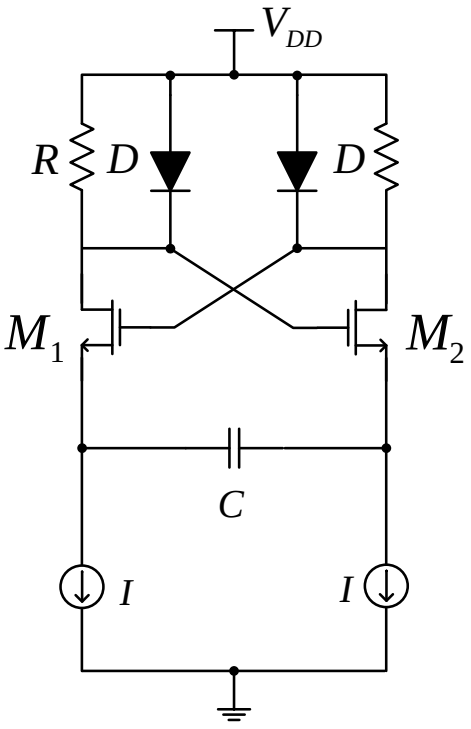

FIGURE 4.1: Current controlled multivibrator.

Assuming that the oscillation amplitude developed on the resistors R is small that the diodes are turned off, making the circuit equal to the basic RC oscillator. Then, the previous small signal analysis made in the previous chapter, applies to this case.

At a lower frequency, with a relaxation behaviour the amplitude is limited by the diodes. The frequency may be approximated by (4.1), where V_{ON} ≈0.5 V (MOS diodes) is the voltage drop on the diode-connected transistors.

$$f_0 = \frac{I}{4V_{ON}C} \tag{4.1}$$

Due to the transitions between behaviors and two complementary amplitude stabilization mechanisms the frequency tunning range of such oscillators may be very wide. It can be further increased by a small modification of figure 4.1 that allows a higher oscillation frequency and is suitable for coupling two oscillators to obtain a quadrature output. The frequency will become (4.2).

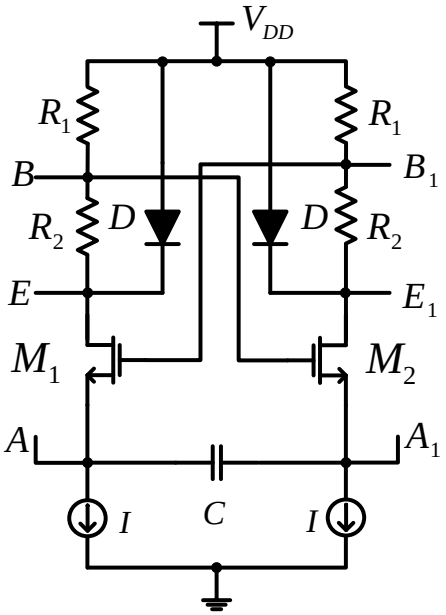

FIGURE 4.2: Modified controlled multivibrator.

$$f_0 \approx \frac{I}{4V_{ON}\frac{R_1}{R_1+R_2}C} \tag{4.2}$$

As mentioned earlier to obtain a quadrature output we need two new differential pairs. the inputs should be connected to the capacitor terminals (A and A_1). Their outputs can be connected to either nodes B and B_1 or E and E_1. The current source I_c injected at node B will produce a voltage V_b given by (4.3). Assuming that $r_d << R_2$, where r_d is

the diode dynamic resistance. If I_c is injected at node E then V_b will be reduced to (4.4), assuming that $r_d << R_1 + R_2$.

$$V_b \approx \frac{I_c R_1 R_2}{R_1 + R_2} \tag{4.3}$$

$$V_b \approx \frac{I_c R_1 r_d}{R_1 + R_2} \tag{4.4}$$

When the coupling is made at nodes E and E_1 it is called "soft coupling", when connected to nodes B and B_1 it is called "hard coupling". If $R_1 + R_2$ is constant the maximum coupling is achieved for $R_1 \approx R_2$.

Figure 4.3 shows the coupled circuit, in this case the hard coupling case. The coupling current changes the gate voltages of M_1 and M_2. If the current is low in comparison with the tunning current, its influence on the oscillation frequency is very weak. However, this current is able to change the switching time of transistors M_1 and M_2 leading to synchronous oscillations of both multivibrators. This minimizes the influence of noise sources in the switching point, which results in a reduction of the phase noise. The synchronous frequency is approximately given by (4.2).

4.1.2 Simulation Results

The circuit shown in figure 4.3 is simulated in Cadence Spectre RF using 130 nm MOS technology. The transistors and resistors sizing are equal for all bands mentioned earlier, as well as the supply voltage (1.2 V). We could not cover the whole WMTS band with the implemented circuit because when increasing the tunning current I we are reducing the voltage at the coupling circuit, but using some techniques (e. g. two capacitors controlled by switch) would make it possible. We establish a minimum of 100 mV at the current source for a possible current mirror implementation. For the lower band (608 - 614 MHz) the capacitor is C=1.8 pF, for the higher band (1395 - 1400 MHz and 1427 - 1432 MHz) is C=400 fF. Other values are as follows: R_1=R_2=R=250 Ω, transistors M_1, M_2, M_5 and

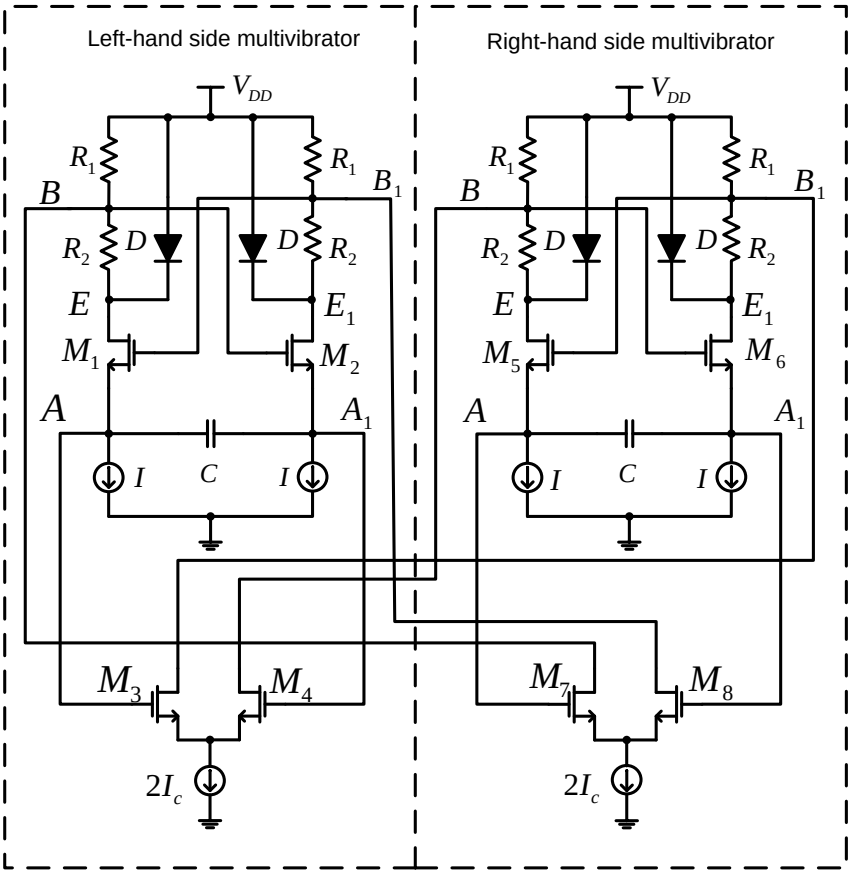

FIGURE 4.3: Quadrature current controlled oscillator with "hard" coupling.

M_6 have W=80 µm and L=300 nm; M_3, M_4, M_7 and M_8 have W=100 µm and L=300 nm. The coupling current I_c is equal to 0.5 mA. Diodes D were made using PMOS transistors instead of NMOS, because of their temperature characteristics, [7].

Figures 4.4 and 4.5 are obtained by changing the tuning current (I) and the capacitor. Both "soft" and "hard" coupling are simulated and compared.

In figure 4.4 the graphic has a almost linear characteristic, after the tunning current (I) reach a value of 0.5 mA, which is the value of the coupling current (I_c). If the tuning current is lower than the coupling one, the later will have a strong influence on the frequency. This means that at a low tuning current values both currents influence the oscillation period. Figure 4.5 is obtained by reducing the capacitor value to C=400 fF, which causes a decrease of the capacitor charging time thus increasing the frequency.

Although one could expect a square wave at the output, at least for the lower frequency, that does not happen, as seen on figures 4.6 and 4.7, due to the parasitic capacitors of the

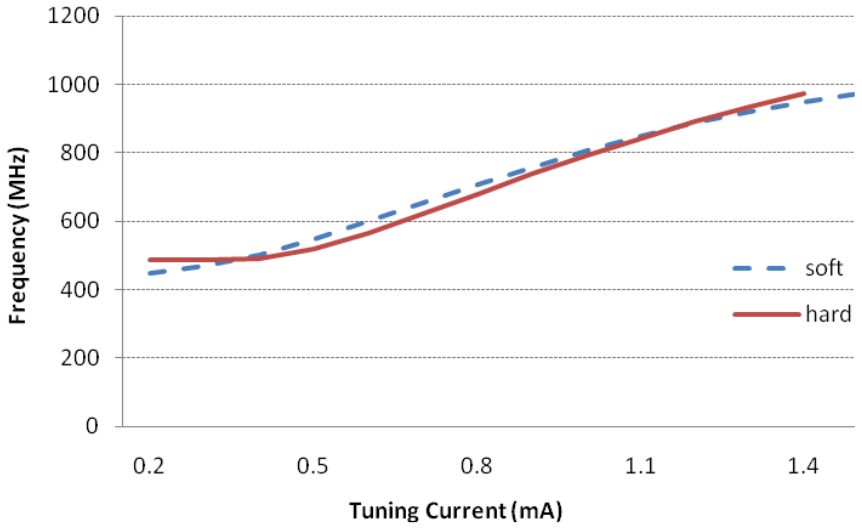

FIGURE 4.4: Tuning characteristic for $2I_c$=0.5 mA with C=1.8 pF.

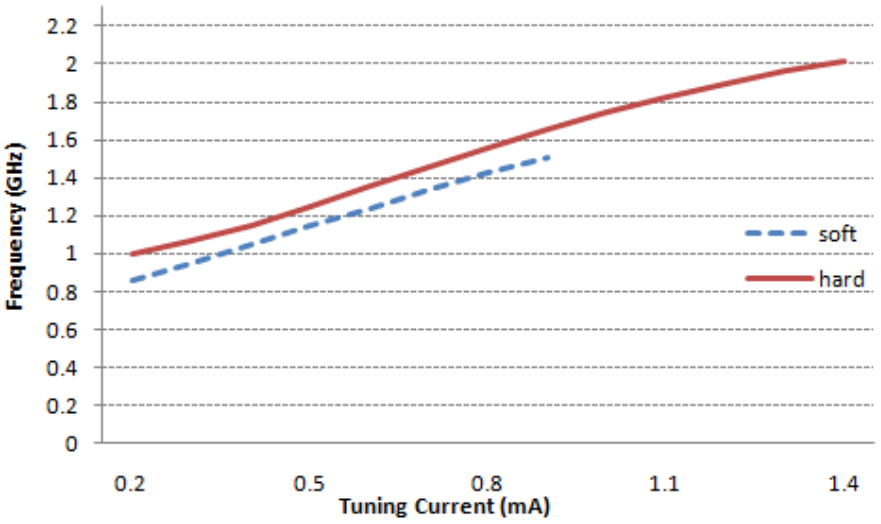

FIGURE 4.5: Tuning characteristic for $2I_c$=0.5 mA with C=400 fF.

transistors that filter higher harmonics and also because of the diodes. For 1.4 GHz, with "soft" coupling the oscillations stopped due to the voltage at points E in figure 4.3, causing the diodes to start conducting. The parasitics are also responsible for the deviation of the linear behaviour at high current values.

The oscillator phase-noise for the 600 MHz is -119.5 dBc/Hz@10 MHz offset for "soft" coupling and -121.6 dBc/Hz @ 10 MHz offset for "hard" coupling. At 1.4 GHz the phase noise is -114.2 dBc/Hz@10 MHz offset for "soft" coupling and -117.6 dBc/Hz@10 MHz

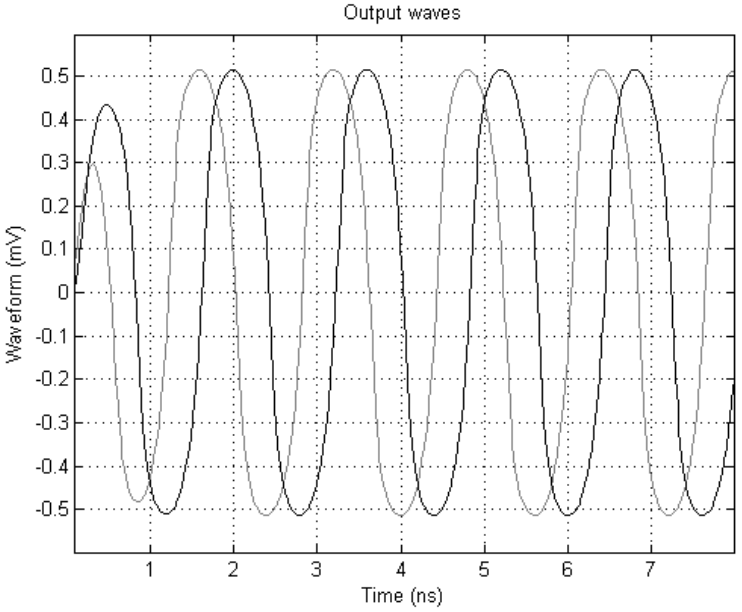

FIGURE 4.6: Output waveforms (600 MHz).

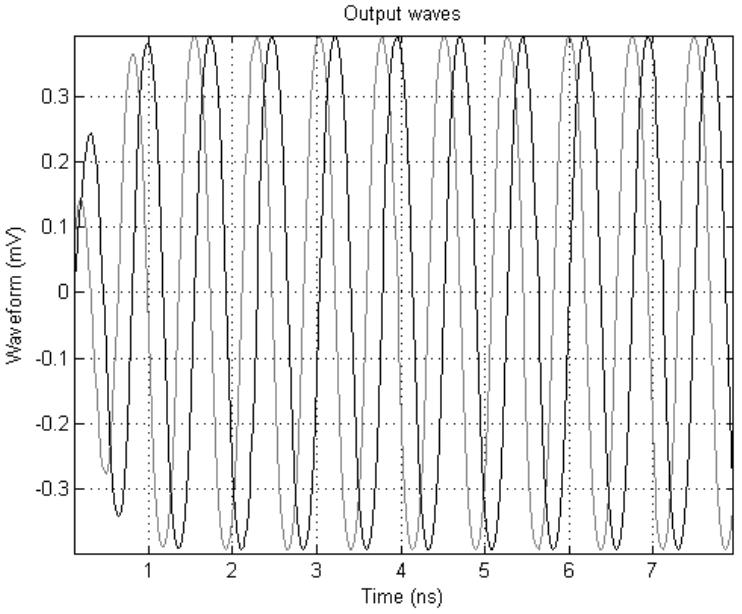

FIGURE 4.7: Output waveforms (1.4 GHz).

offset for "hard" coupling. We can conclude that the phase noise is reduced for "hard" coupling in both bands as seen in figures 4.8 and 4.9.

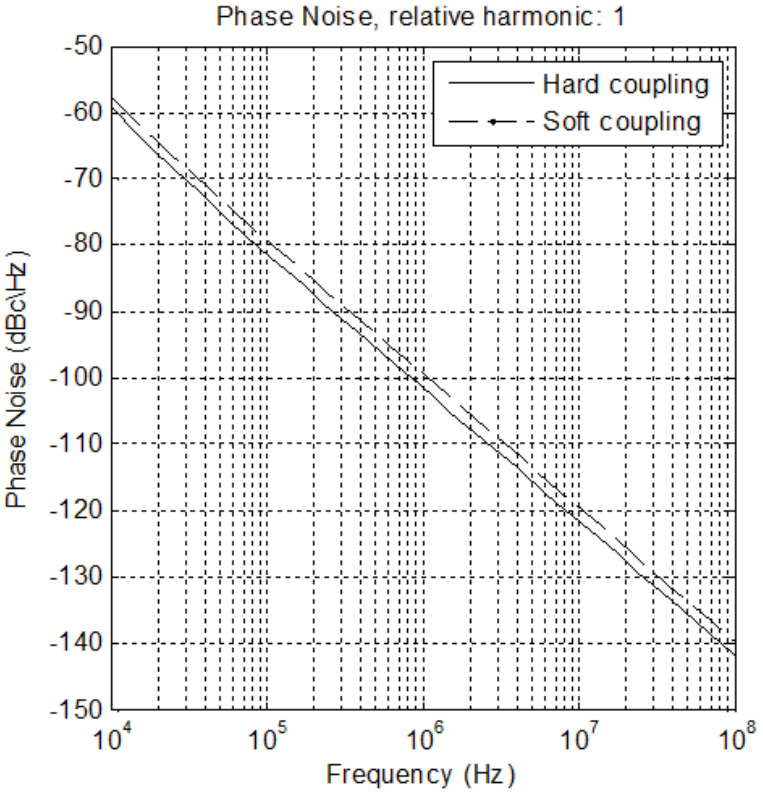

FIGURE 4.8: Oscillator phase-noise ("hard" coupling-600 MHz).

We also did simulations for mismatches between the coupled oscillators. Table 4.1 and Table 4.2 show the influence of a capacitor mismatch for both "hard" and "soft" coupling. There is no oscillation for low values of "soft" coupling current at 1.4 GHz. The "hard" coupling offers a lower phase error (about 1°) and a small frequency shift in the lower band.

A larger mismatch requires a larger coupling current for the oscillator to synchronize, but this leads to an increase frequency shift. The same principle applies when the tuning currents are mismatched, as shown on Table 4.3 and Table 4.4.

From the simulations made we can conclude that the hard coupling provides a lower quadrature error and allows higher coupling currents without stopping the oscillations, because the frequency shift increases with the current.

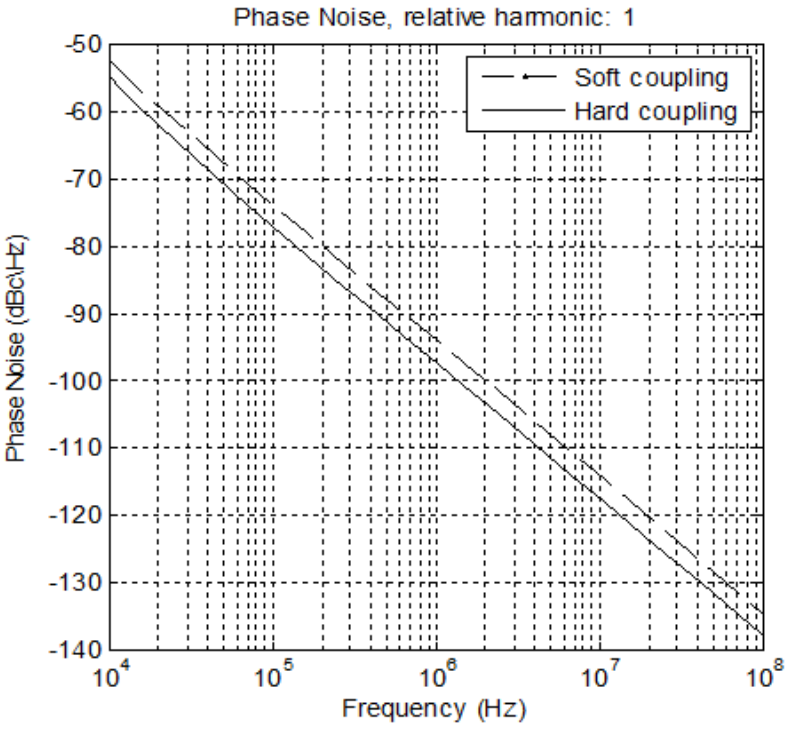

FIGURE 4.9: Oscillator phase-noise ("hard" coupling-1.4 GHz).

	Soft coupling		**Hard coupling**	
$2I_c$ (μA)	Δf (MHz)	**Phase error** (°)	Δf (MHz)	**Phase error** (°)
0.1	53.85	10.28	12.27	7.95
0.2	45.21	5.19	12.49	4.22
0.3	34.35	3.23	11.62	2.97
0.4	21.93	2.38	10.44	2.15
0.5	8.22	1.91	8.95	1.66
0.6	6.64	1.62	7.44	1.61
0.7	22.24	1.33	5.92	1.39
0.8	38.43	0.99	4.41	1.17
0.9	54.82	0.95	2.76	0.95

TABLE 4.1: Effect of 5% mismatches in capacitances (600 MHz).

	Soft coupling		**Hard coupling**	
$2I_c$ (μA)	Δf (MHz)	**Phase error (°)**	Δf (MHz)	**Phase error (°)**
0.1	No Oscillation		71.86	1.45
0.2	No Oscillation		59.49	1.59
0.3	25.19	0.92	46.28	1.09
0.4	20.87	0.86	32.12	0.76
0.5	13.43	0.84	17.33	0.57
0.6	3.56	0.93	2.33	0.4
0.7	8.16	1.02	12.54	0.34
0.8	21.03	1.09	26.96	0.33
0.9	34.51	1.2	40.74	0.29

TABLE 4.2: Effect of 5% mismatches in capacitances (1.4 GHz).

	Soft coupling		**Hard coupling**	
$2I_c$ (μA)	Δf (MHz)	**Phase error (°)**	Δf (MHz)	**Phase error (°)**
0.1	36.34	10.82	5.81	7.86
0.2	27.96	5.47	5.94	4.03
0.3	16.77	3.65	5.46	3.35
0.4	4.41	2.71	8.69	2.09
0.5	9.29	2.21	10.49	1.74
0.6	24.13	1.88	12.17	1.43
0.7	39.66	1.71	14.03	1.2
0.8	55.85	1.47	15.63	1.05
0.9	72.04	1.52	17.33	0.96

TABLE 4.3: Effect of 5% mismatches in tuning currents (600 MHz).

4.1.3 Frequency Locking

We also investigated frequency locking when a external current source is applied between nodes B and B_1, as shown on figure 4.10. A single oscillator at 600 MHz can be synchronized by a current source with an amplitude of 100 µA, as seen on figure 4.11. Because of the differential output we only have odd harmonics, that why the locking is only possible for those harmonics.

It is possible to lock the oscillator up to the 11^th sub-harmonic frequency, as shown

	Soft coupling		**Hard coupling**	
$2I_c$ (μA)	Δf (MHz)	**Phase error** (°)	Δf (MHz)	**Phase error** (°)
0.1	No Oscillation		No Oscillation	
0.2	No Oscillation		26.91	4.6
0.3	6.15	3.87	13.1	3.39
0.4	9.41	3.01	1.9	2.73
0.5	16.24	2.58	17.62	2.3
0.6	25.51	2.34	33.58	2.01
0.7	36.49	2.08	49.35	1.81
0.8	48.61	1.94	64.76	1.57
0.9	61.23	1.95	79.6	1.45

TABLE 4.4: Effect of 5% mismatches in tuning currents (1.4 GHz).

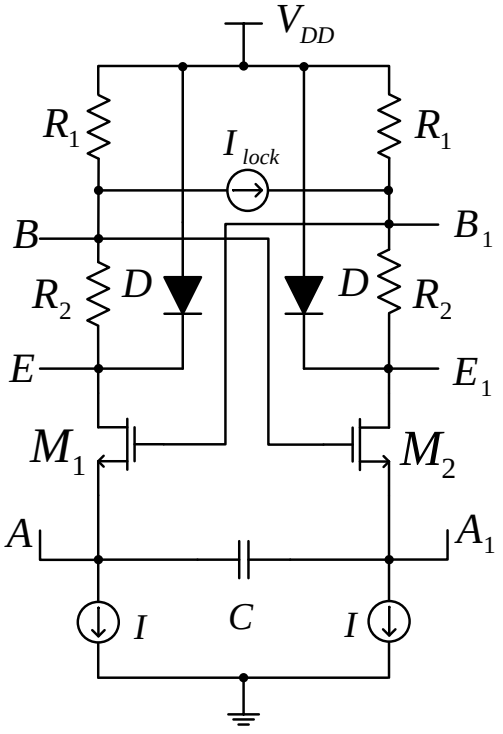

FIGURE 4.10: Sub-harmonic injection-locked multivibrator.

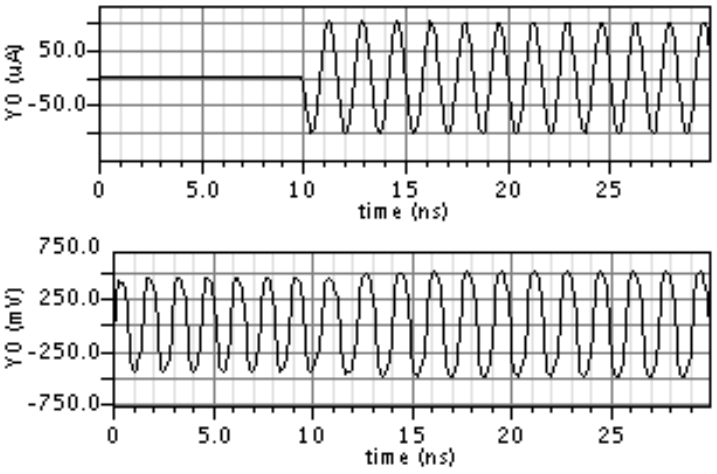

FIGURE 4.11: Waveforms for the injection locking.

Table 4.5. Figure 4.11 shows the locking signal application at 10 ns and the locking after approximately two periods. This is one of the advantages of RC oscillators, they can adjust in a small period of time, unlike the LC oscillators that can take hundreds of periods to adjust the oscillation frequency. Similar results are obtained for 1.4 GHz, but in this case the maximum sub-harmonic frequency was the fifth. From Table 4.5 we can conclude that the oscillator only locks between a minimum frequency and a maximum frequency, also with higher harmonics this locking range is reduced.

The coupled version is also tested for frequency locking, the locking range is smaller than the one of a single oscillator. Table 4.5 shows that the coupled oscillator is able to lock up to the 5^th harmonic.

	Single Oscillator		**Coupled Oscillator**	
Harmonic Number	**Low Freq.** (GHz)	**High Freq.** (GHz)	**Low Freq.** (GHz)	**High Freq.** (GHz)
1	0.55	0.86	0.46	0.75
3	1.85	2.2	1.7	2.1
5	3.33	3.45	3.04	3.33
7	4.73	4.75	-	-
9	6.08	6.1	-	-
11	7.43	7.44	-	-

TABLE 4.5: Oscillator Locking Range.

With a tuning current mismatch, the oscillator can only lock at up to the fifth harmonic. This value is reduced to the third when the mismatch is increased to 10 %. Mismatches in capacitors have the same effect.

This investigation serves to prove that both coupled oscillators when not running at the same frequency due to mismatches, the system is capable of synchronizing in a short period of time. This is one of the reasons why RC oscillators have survived and are still a object of interest for future development.

4.2 Methods for Improving Phase-Noise and Figure of Merit

In this sub chapter we present three methods, the first reduces power consumption and the last two, improve phase-noise and figure of merit on a RC oscillator. We also introduce some equations for the noise sources in the circuit based on [17]. This oscillator is based on the basic circuit mentioned before, but with a slight difference. The resistors are substituted by transistors in the linear region, figure 4.12 shows the modification. The first two methods are based on ([6] e [17]) but the last one can only be applied with MOS resistors.

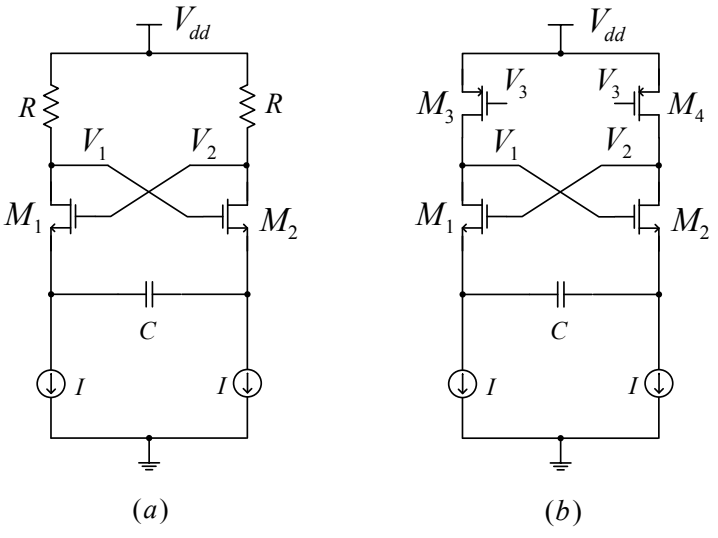

FIGURE 4.12: Relaxation Oscillator MOSFET modification.

4.2.1 Pulse Self Biasing

A disadvantage of the RC oscillator is the two current sources, seen on figure 4.12. This issue affects the power consumption and degrades the FOM. This application of this method on our circuit, reduces the power to half but increases the thermal noise on the circuit. In [17] it has been proved that when the current pulse width is small, the phase noise of the circuit is reduced.

The $1/\Delta\omega^2$ component of phase-noise is deeply influenced by the thermal noise from the components of the circuit. Equation (4.5) from [17], is a simplified modification of the phase-noise equation representing that influence. The thermal noise power spectral density of M_1, the current mirror and circuit losses is equivalent to $(i^2_{n,M1}/\Delta f)$, $(i^2_{n,tail}/\Delta f)$ and $(i^2_{n,Rp}/\Delta f)$ respectively; Γ_{M1}, Γ_{tail} and Γ_{Rp} are the root mean square values of their impulse sensitivity function.

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{\left(\frac{i^2_{n,Rp}}{\Delta f}\right)\Gamma^2_{Rp} + \left(\frac{i^2_{n,M1}}{\Delta f}\right)\Gamma^2_{M1} + \left(\frac{i^2_{n,tail}}{\Delta f}\right)\Gamma^2_{tail}}{2V^2_{max}C^2_T(\Delta\omega)^2}\right) \tag{4.5}$$

When the tail current is constant, the thermal noise from the oscillator losses is $i^2_{n,Rp}/\Delta f = 4kT/Rp$. The thermal noise spectral density of M_1 is $i^2_{n,M1}/\Delta f = 4kT\gamma\xi/Rp$ where $\xi = g_{m0}Rp$, g_{m0} represents the transconductance of M_1. Finally the tail current thermal noise is given by $i^2_{n,tail}/\Delta f = 4kT\gamma/Rp\sqrt{2\eta_0}$, where η_0 is the ratio of the size between transistor M_1 and the tail device. Since the current is constant the impulse sensitivity function is also constant. By substituting all elements in (4.5) we get (4.6).

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{kT(1+\frac{1}{2}\gamma\xi+\frac{1}{2}\gamma\xi\sqrt{2\eta_0})}{\left(\frac{2}{\pi}\right)^2 Rp^3I^2C^2_T(\Delta\omega)^2}\right) \tag{4.6}$$

With a pulsed tailed current (4.7) with a duration of 2Φ in radians, where ϕ is the oscillator phase ($\phi = \omega_0 t$) and I_p is the peak value, each component of (4.5) will change. The thermal noise of M_1 will become (4.8), but in this case the impulse sensitivity function will be (4.9).

$$I = I_p \sum_{n=-\infty}^{\infty} \Pi\left(\frac{\phi - n\pi}{2\Phi}\right) \tag{4.7}$$

$$\frac{i_{n,M1}^2}{\Delta f} = 4kT\gamma g_{m0}\sqrt{\frac{\pi}{2\Phi}\Pi\left(\frac{\phi}{2\Phi}\right)} \tag{4.8}$$

$$\Gamma_{M1} = \frac{1}{2\pi}\left(\Phi - \frac{1}{2}\sin(2\Phi)\right) \tag{4.9}$$

For the tail transistor the thermal noise will be (4.10) and the impulse sensitivity (4.11). The thermal noise of the oscillator losses are kept the same. By substituting all the previous equations on (4.5) we will get the phase-noise equation for a pulsed tail current, (4.12), where $A(\Phi)$ and $B(\Phi)$ are the thermal noise of M_1 and the tail transistor, respectively and are given by (4.13) and (4.14). We can see that the pulse width (2Φ) of the current influences the phase-noise of the oscillator.

$$\frac{i_{n,tail}^2}{\Delta f} = 4kT\gamma\frac{\xi}{Rp}\frac{\pi}{2\Phi}\sqrt{2\eta_0} \tag{4.10}$$

$$\Gamma_{M1} = \frac{1}{2\pi}\left(\Phi - \frac{1}{2}\sin(2\Phi)\right) \tag{4.11}$$

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{kT[1 + A(\Phi) + B(\Phi)]}{sinc(\frac{\Phi}{\pi})Rp^3I^2C_T^2(\Delta\omega)^2}\right) \tag{4.12}$$

$$A(\Phi) = \frac{\gamma\xi}{\sqrt{2\pi\Phi}}\left(\Phi - \frac{1}{2}\sin(2\Phi)\right) \tag{4.13}$$

$$B(\Phi) = \frac{\gamma\xi\sqrt{2\eta_0}}{2\Phi}\left(\Phi - \frac{1}{2}\sin(2\Phi)\right) \tag{4.14}$$

Figure 4.13 shows the current flow on the RC oscillator when transistor M_1 is ON. There is a waste of current, the only current that matters is the one on the capacitor. Here the idea of switching can be applied, since the objective is guarantee a current through the capacitor we need a opposite switching to those of transistors M_1 and M_2. When M_1 is ON the transistor bellow M_2 must be conducting. With this technique instead of having two current sources we only have one, thus reducing power consumption to half and changing the output amplitude, (4.15). The new differential pair introduces more noise, but allows us to implement the pulse modification [17].

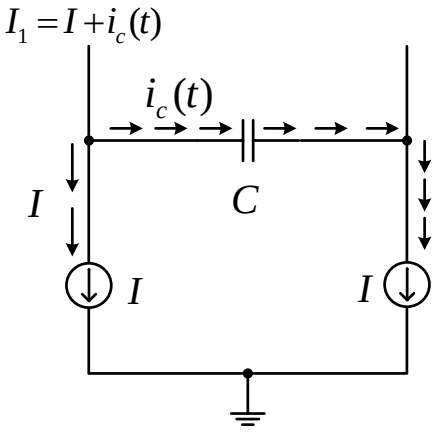

FIGURE 4.13: Current flow.

$$V_{out} \begin{cases} V_{dd} - (V_{dd} - RI) = RI & \text{if first state} \\ V_{dd} - RI - V_{dd} = -RI & \text{if second state.} \end{cases} \tag{4.15}$$

Figure 4.14 shows the effect of the pulse bias on the output waveform. The figure presented is for a LC oscillator but one can conclude that when applying the same method for a Relaxation oscillator the outputs will be more "squared", not only the current will flow trough each branch for a smaller period of time but also the distortion is reduced. From (4.12) we can see that a narrow pulse current will reduce the total thermal phase noise, this was proved by simulation in [17], in our circuit we used the outputs of the relaxation oscillator as a pulse source to connect to control the current.

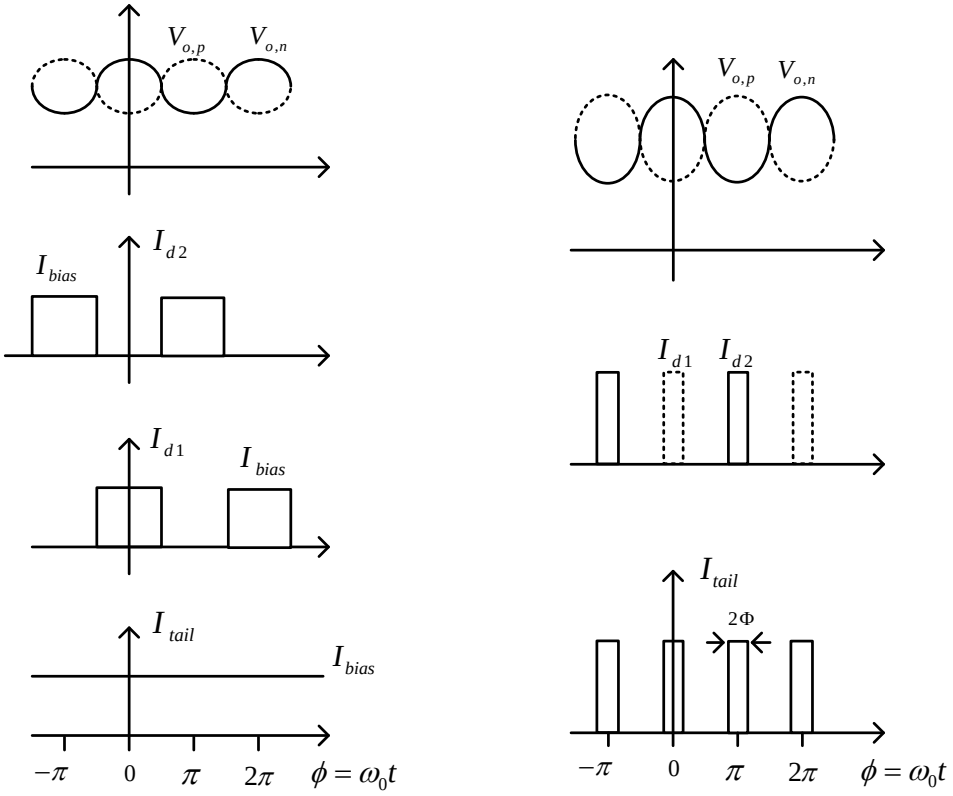

FIGURE 4.14: Pulse biasing.

When applying the pulse theory to a RC oscillator with a non linear behaviour, we can use its outputs to control the current. The new differential pair will switch regions accordingly with the output. The voltage at the gate is higher than the one on the source, causing the transistors to work on the triode region thus behaving like a resistor. Actually the biasing current wont became a series of pulses but more a series of triangles. The circuit implementation and operation is shown on figure 4.15. The resistors made by M_5 and M_6, will increase or decrease during the oscillations, changing the current in each branch.

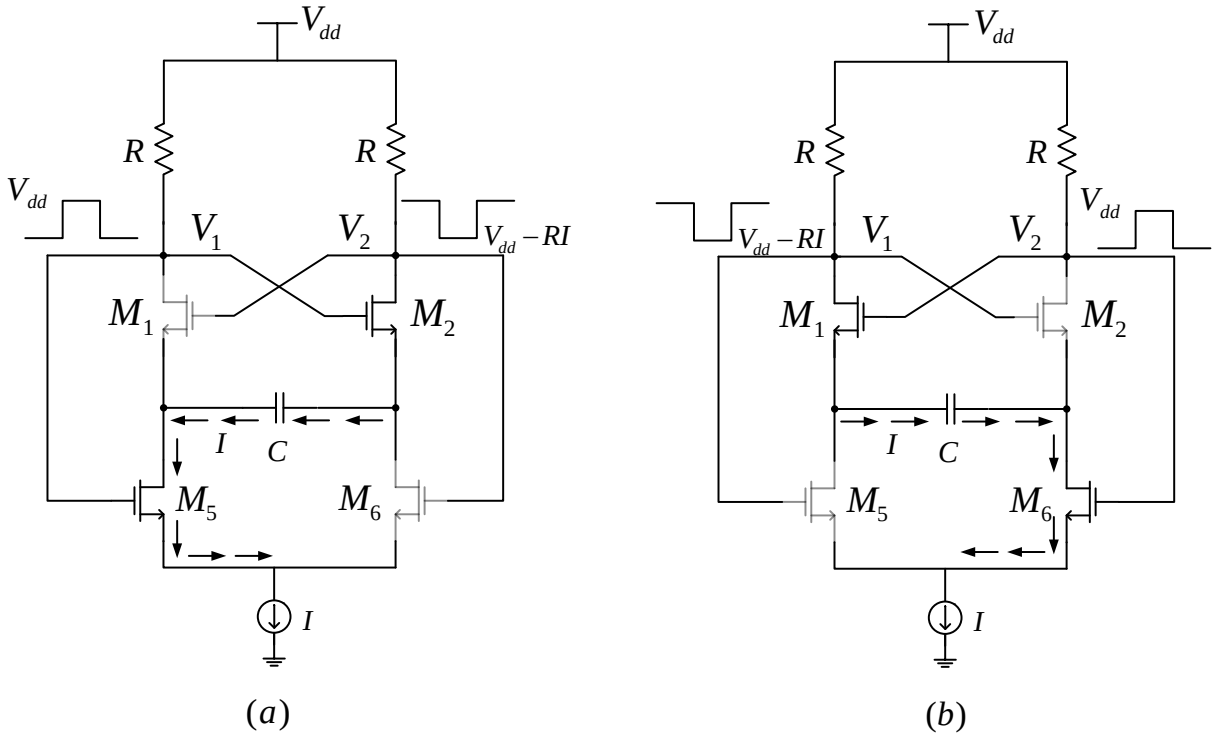

FIGURE 4.15: Self Biasing.

4.2.2 Harmonic Filtering

Before explaining this method we need to understand how the harmonics work on the modified RC oscillator. To simplify the calculations it will be assumed up to the third harmonic, (4.16) by solving it we get (4.17). On the left branch of the circuit there is positive signal A equal to (4.17), on the other branch an opposite signal with $-A$ given by (4.18). The differential output $y_1 - y_2$ will cancel the even harmonics leaving only the odd one and thus creating the square wave.

$$y = a_0 + a_1 A\cos(\omega_f t) + a_2 A\cos^2(\omega_f t) + a_3 A\cos^3(\omega_f t) \tag{4.16}$$

$$y_1 = a_0 + \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega_f t) + \frac{a_2 A^2}{2}\cos(2\omega_f t) + \frac{a_3 A^3}{4}\cos(3\omega_f t) \tag{4.17}$$

$$y_2 = a_0 + \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3(-A)^3}{4} \right) \cos(\omega_f t) + \frac{a_2(-A)^2}{2} \cos(2\omega_f t) + \frac{a_3(-A)^3}{4} \cos(3\omega_f t) \tag{4.18}$$

After applying the previous method there is only one current source and a common mode. On the current source the odd harmonics are canceled because the common mode sums both opposing signals, as seen in figure 4.16.

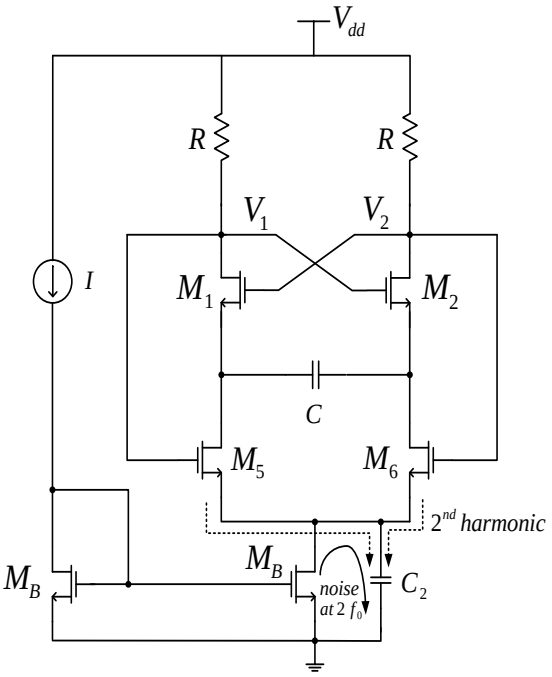

FIGURE 4.16: Second harmonic filtering.

The current source will be substituted by a current mirror, which will introduce thermal noise as seen before. This noise is located at the common mode, the differential pair introduced in the first method acts as a mixer [6], so the noise frequencies at the second harmonic downconvert close to the oscillation frequency. Then we have another differential pair also acting as a mixer and introducing more noise frequencies close to the first harmonic causing an increase of the phase noise. The fact of having a common mode at the current source allows us to cancel the troublesome frequencies. Placing a large capacitor in parallel with the current mirror transistor, we have a low pass band filter that removes the even harmonics, as shown on figure 4.17. This also cancels the noise frequencies and

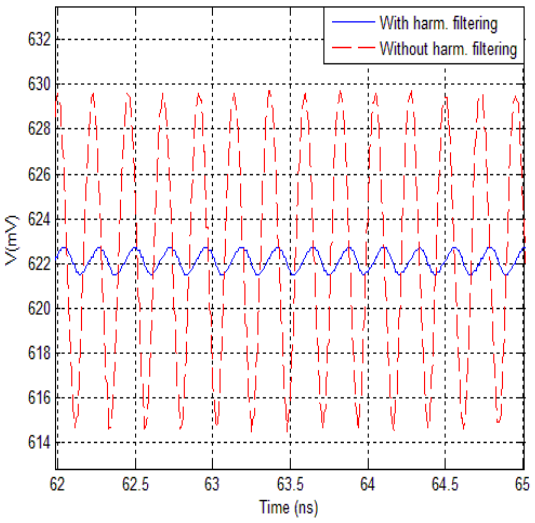

FIGURE 4.17: Second harmonic waves with and without filtering.

guarantees a stable voltage at the current source making the current mirror appear as an ideal current source to the oscillator.

4.2.3 Resistor Feedback

The last method can only be applied, when using MOS resistors. The output of an RC oscillator varies with the current on each branch but is also influenced by the noise sources that may cause a more disfigured wave. The basic idea of this method is to assure a more rapid current and resistor variation. By using the oscillation itself we can improve the variation of the resistor. The changes on the circuit are shown on figure 4.18, the capacitor filters the DC voltage allowing only the AC signal to reach the gates making the transistors M_3 and M_4 have the opposite signals between their gate and drain. This small circuit works as a high passband filter, with high values of C and R the pole will be close to the origin letting all the harmonics pass. When the signal v_3 has its lower value, meaning there is current on the opposite branch, the v_{sg} as a higher value making the resistance decrease, forcing a faster increase of signal v_1.

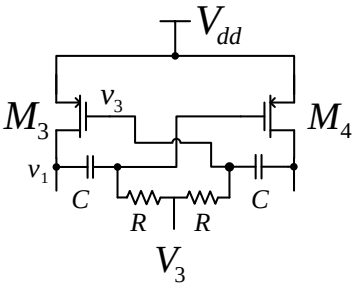

FIGURE 4.18: Implementation.

4.2.4 Simulation Results

After applying all the methods we obtain the final circuit shown on figure 4.19. Using the software Cadence and one of his tools (Periodic Steady State Analysis) we were able to simulate with a good precision all the important features of the oscillator.

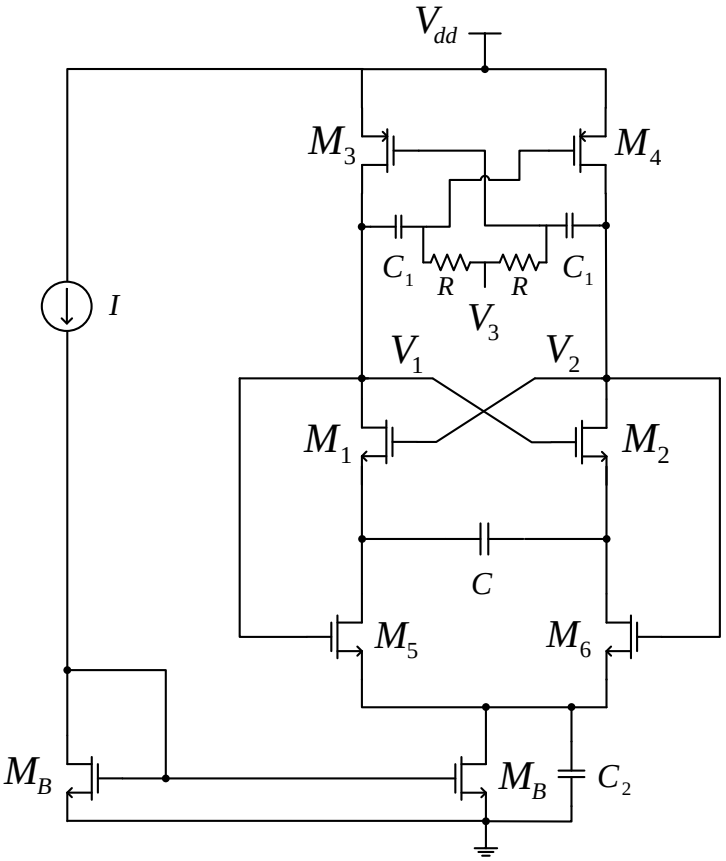

FIGURE 4.19: Final circuit.

The circuit is implemented using 130 µm CMOS technology. The components have the following sizing $(W)_{1,2} = 80$ µm, $(L)_{1,2} = 400$ nm, $(W)_{3,4} = 15$ µm, $(L)_{3,4} = 260$ nm,

$(W)_{5,6}$ = 15 µm, $(L)_{5,6}$ = 260 nm, the current mirror transistors (M_B) has $(W)_B$ = 15 µm, $(L)_B$ = 360 nm, C = 1.8 pF, $C_1 = C_2$ = 5 pF and R = 20 kΩ. The V_3 voltage is biasing the PMOS transistors with 100 mV and V_{dd} = 1.2 V making a resistor value of 300 Ω.

The optimal point for the original RC oscillator (with no methods applied) was obtained for a current equal to 700 µA, with a phase noise of -129.7 dBc/Hz, a figure of merit of -155.213 dBc/Hz and a power consumption equal to 1.68 mW.

During simulations we observed some unexpected results. Instead of increasing the frequency when we increased the current, it diminished. The problem was related to the PMOS transistors, during the operation of the oscillator, when the amplitude increased there is a point when this transistors reach the saturation region, when that happens the equivalent resistor changes, reducing the oscillation frequency and the phase-noise. From figure 4.20 we can see the simulation result when the transistor switches from the triode region to the saturation region. On Table 4.6, only the feedback resistor method was applied, the PMOS transistor stays on the triode region [150 µA;300 µA], switches from the triode region to a mixed region [350 µA] and finally switches from triode to saturation region [400 µA;800 µA]. This region change only occurs during the transition, when the gate is going to his highest amplitude and the drain to its lowest, figure 4.20 shows this situation.

Table 4.7 shows how each method influences the frequency value. The circuits were tested using a current from 400 µA to 1000 µA, the transistor sizing was kept the same. As mentioned the PMOS transistors are biased in the triode zone, however during the switching they can operate in different regions. For low biasing currents they are always stay in triode, but, for high currents they reach saturation, which changes the equivalent resistance value, thus reducing the oscillation frequency.

A comparison between simulation values of phase-noise and FOM was also made. The first graphic , seen in figure 4.21, shows the phase noise variation with the current. As one can see the use of all methods caused and overall improvement on the phase noise.

current (μA)	frequency (MHz)
150	417.7
200	391.7
250	342.1
300	281.3
350	25.9
400	11
450	8.7
500	7.3
550	6.4
600	5.7
650	5.2
700	4.7
750	4.3
800	3.9

TABLE 4.6: Frequency variation with only resistor feedback.

	frequency (MHz)		
current (μA)	self pulse biasing	self pulse and filtering	all methods
400	575.9	579.3	504.5
450	586.6	594.6	513.9
500	592.1	605.5	518.2
550	593.3	612.9	518.4
600	591.7	617.9	514.8
650	587.9	621.1	506.7
700	582.8	622.8	490.9
750	576.6	623.3	459.2
800	569.9	622.5	387.7
850	562.5	620.5	213.6
900	554.6	616.8	196.9
950	546.1	611.4	188.8
1000	537.3	604.3	183.7

TABLE 4.7: Oscillators same sizing comparison.

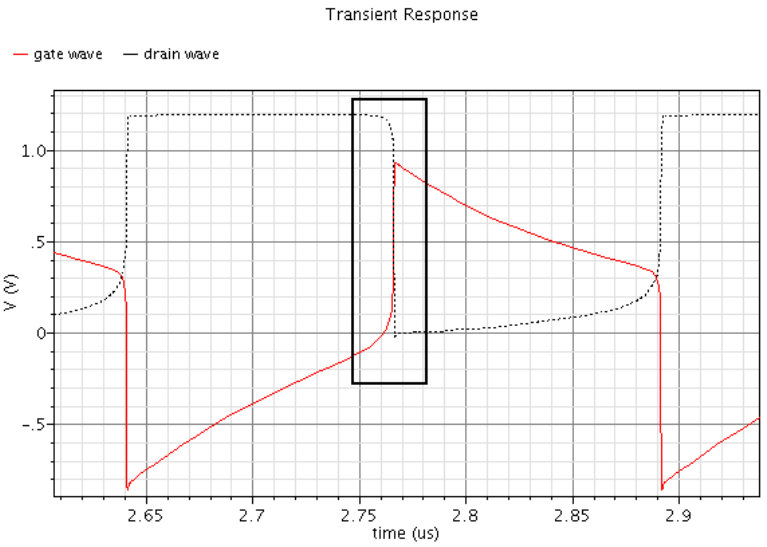

FIGURE 4.20: Region change.

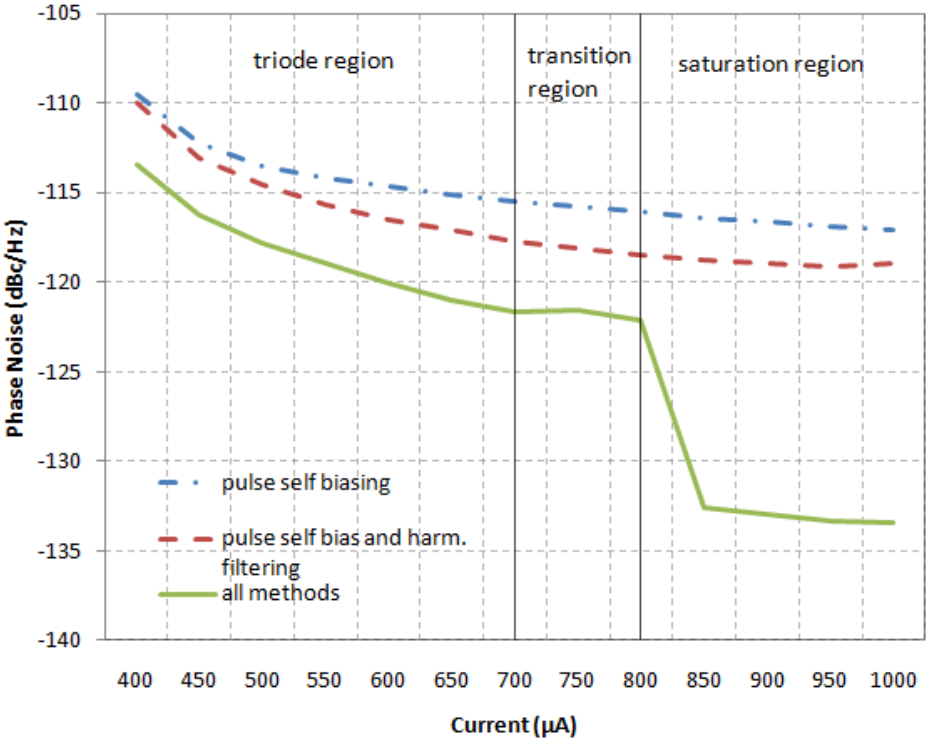

FIGURE 4.21: Phase Noise(@10MHz) improvement with and without harmonic filtering.

The last graphic, shown on figure 4.22, shows a comparison of the absolute value FOM. When comparing the optimal FOM of the circuit without methods with only the self pulse biasing we can see that it as a worst performance, this happens due to the introduction of more transistor causing the phase noise to increase due to thermal noise introduced, but at the same time there is a reduction of half the power consumption. The harmonic filtering improves the FOM, this is due to the reduction of the phase noise. When combining all the methods most of the current values have a better FOM than the optimal point of the normal oscillator, reaching a value of -159.1 dBc/Hz for a current of 850 µA. As mentioned early the region change of PMOS transistors during the oscillation, causes a worst FOM when switching to the mixed region, but when it changes to saturation the phase noise is reduced, as seen on figure 4.21.

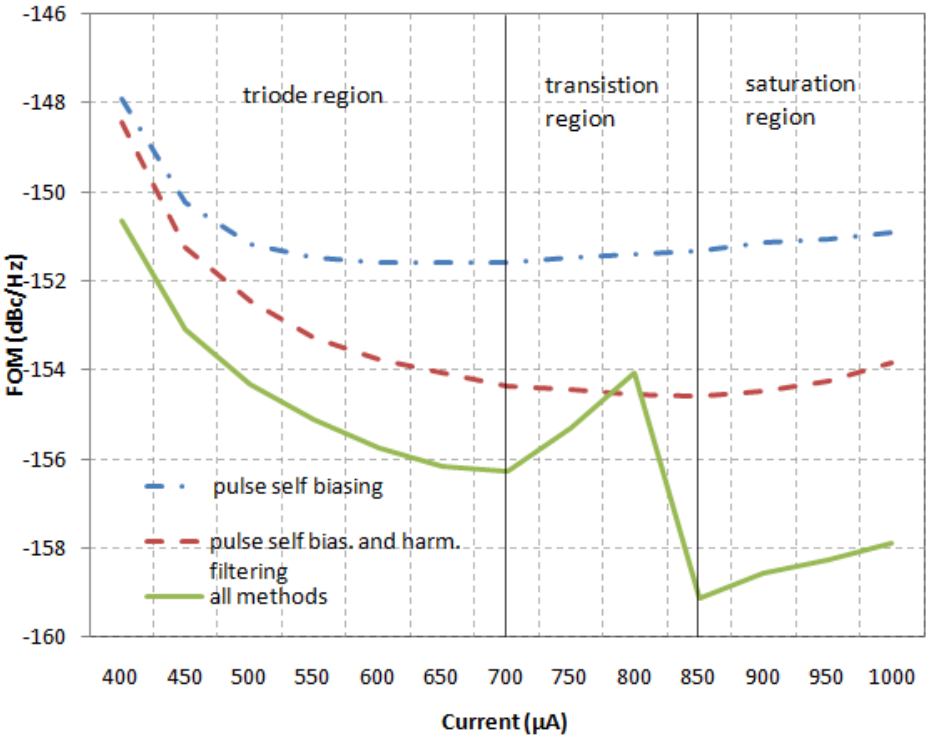

FIGURE 4.22: FOM comparison.

The use of only one current source reduces power consumption but increases the phase noise, by filtering the second harmonics those loses are compensated. The combination of the three methods made an improvement of almost 4 dB on the FOM.

An attempt to obtain quadrature outputs was made by connecting transistors M_5 and M_6 to the output of the other oscillator. The results obtained were unsatisfactory, the frequency would always drop when we increased the current,thus reducing the FOM. We also tried coupling through the second harmonic using the current sources ([23]), the results were similar to the ones we saw for a single oscillator with a improvement of 1 to 2 dB on the FOM.

4.3 Fully Integrated CMOS Two-Integrator

We have seen the circuit implementation of the two integrator in a previous chapter, before we go into the simulation results we need to make some modifications. We did not use capacitors for oscillation, the parasitic capacitors in the transistors were enough. Based on the harmonic filtering mentioned on the previous section, we decided to use a capacitor connected between both common modes to cancel the even harmonics. The resistors were substituted by PMOS transistors in the triode region also the capacitor is substituted by transistors.

4.3.1 CMOS Capacitors

CMOS transistor have a capacitance between the gate and the substrate C_{ox}. Depending on the gate voltage we consider three different bias modes. One below the flat-band voltage, V_{FB}, a second between the flat-band voltage and the threshold voltage, V_{th}, and finally one larger than the threshold voltage, [21]. These bias regimes are called the accumulation, depletion and inversion mode of operation, as shown on figure 4.23.

In accumulation mode the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Only a small amount of band bending is needed to build up the accumulation charge so that almost all of the potential variation is within the oxide. The capacitance is equal to C_{ox}.

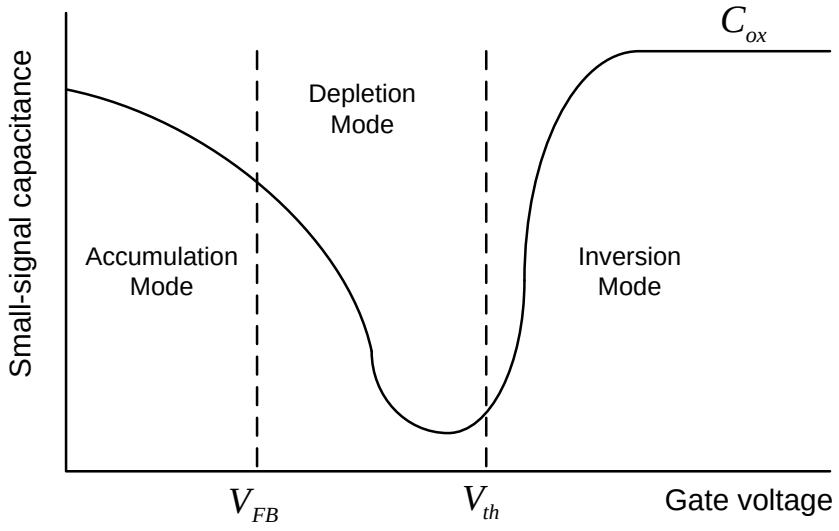

FIGURE 4.23: Capacitor value of a NMOS transistor.

In depletion mode a negative charge builds up in the semiconductor. Initially this charge is due to the depletion of the semiconductor starting from the oxide-semiconductor interface. The depletion layer width further increases with increasing gate voltage. A new capacitance (C_d) appears in series with C_{ox} (4.19).

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} \tag{4.19}$$

In inversion mode a negative charge emerges at the oxide-semiconductor interface. This charge is due to minority carriers, which form a inversion layer. As one further increases the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential. The capacitance is equal to C_{ox}.

A circuit design is proposed in [22] for a capacitor. This version uses a series compensation of depletion mode CMOS transistors seen in figure 4.24. This implementation is suitable for the two-integrator, because when the voltage at the bulk varies the capacitor value is kept the same. The capacitor connects between the common mode of each side of the two integrator, by doing so the second harmonics, which are in opposition, cancel each other.

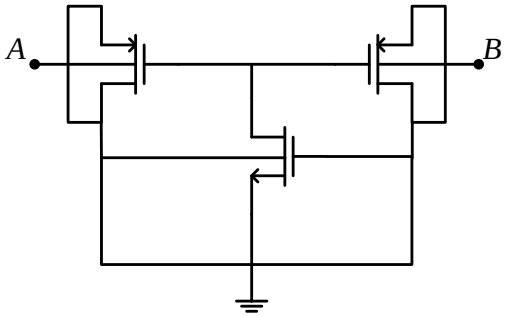

FIGURE 4.24: Capacitor implementation.

4.3.2 CMOS Implementation and Results

After applying all modifications mentioned we obtain the following circuit shown on figure 4.25. The circuit was implemented using the 130 nm CMOS technology and simulations were made using the Periodic Steady State Analysis from the software Cadence.

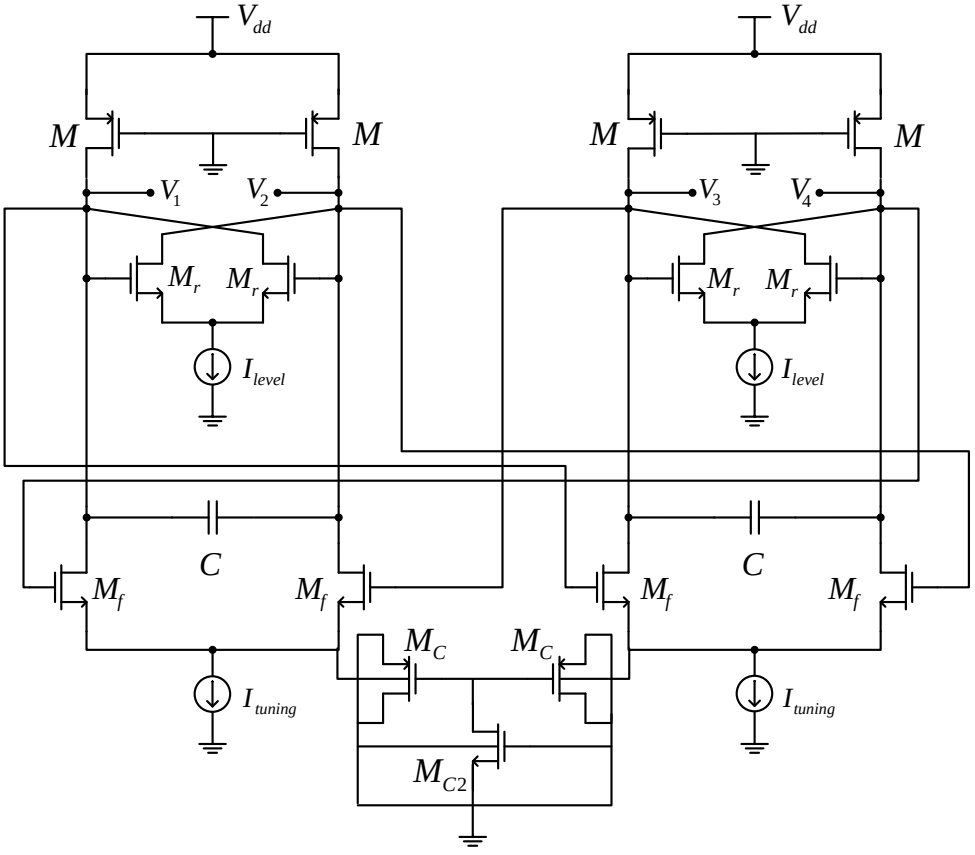

FIGURE 4.25: Full integrated CMOS two integrator.

When designing the oscillator we need to take into account all the information mentioned in the previous chapter, but a more practical approach is taken for transistor sizing.

Although we use the inverted differential pair to cancel the real part of the oscillator, we have to make small variations of the W/L ratio and observe the results to see how close we are to the desired value. The circuit was develop for a resistor of 300 Ω so the $1/g_m$ of the upper differential pair should be close to that value. As in the other oscillators presented in this thesis the supply voltage is 1.2 V, the current I_{level} is equal to 500 µA. The implementation uses M_r transistors with $W = 5.5$ µm, $L = 360$ nm with nf=5 and transistors M_f with $W = 7$ µm, $L = 360$ nm with nf=6. All the current biasing transistors have $W = 20$ µm, $L = 360$ nm with nf=4. The PMOS transistors have $W = 3.6$ µm, $L = 130$ nm with nf=2. For the capacitor transistors M_c we have $W = 3$ µm, $L = 200$ nm with nf=3 and transistor M_{c2} with $W = 3$ µm, $L = 360$ nm and nf=4, with this sizing the capacitor value is around 300 fF. All transistor with the exception of the current mirrors were implemented with RF transistors. The circuit has a tunning range from 435.7 MHz to 2.52 GHz, with the current $I_{tunning}$ from 0.1 mA to 1.9 mA. Table 4.8 shows the results for each WMTS frequencies and Wi-Fi.

Current (mA)	Frequency (GHz)	Phase Noise (dBc/Hz@$10MHz$)	Power (mW)	FOM (dBc/Hz)
0.15	0.6	-103.5	1.56	-137.1
0.5	1.4	-105.7	2.4	-144.8
1.5	2.4	-109.7	4.8	-150.5

TABLE 4.8: Oscillator Frequency.

We have implemented the layout of this circuit for a future fabrication of a test-chip. We need a match of 50 Ω to be able to do measurements of the chip. Since we did not take into account these specification we need to resort to buffers, as shown on figure 4.26. Each one of them is a source-follower and the output impedance is given by $1/g_m$. The transistor sizing for the current mirrors are equal to the previous ones, transistors M_{b1} has $W = 5$ µm, $L = 120$ nm with nf=7, the current I_{buffer} is 2 mA, with this sizing the output impedance is close to 55 Ω. The buffer current could be a lot less if we had increased the transistor size, but when doing that the frequency would decrease. Instead of covering the whole 2.4 GHz frequency, the maximum frequency achievable at 1.9 mA of tunning current, would be 2.3 GHz, after this current value the frequency starts to

decrease. To allow the two integrator to cover WMTS and the wireless frequency we decided to keep transistors M_{b1} small and increase the current.

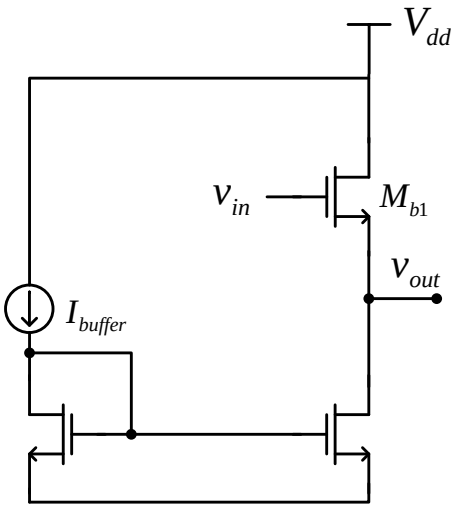

FIGURE 4.26: Buffer.

We have tried to reduce the occupied area to its minimum, the two integrator and buffers occupy a area of 80 x 73.2 µm^2, as shown on figure 4.27. The final layout has the two integrator oscillator, buffers, protective diodes and pads, with a total area of 280 x 368 µm^2. Some precautions have been taken into consideration when designing the layout such as symmetry, so that both sides have small differences; the thickness and size of the tracks to avoid introducing more parasitics and because of the current in each part of the circuit. Adding the buffers with the circuit shown on figure 4.25 and comparing with figure 4.27 the buffers (transistors M_{b1}) were placed at both ends (left and right) and in the middle, between them are the triode region PMOS transistors (transistors M) and bellow the upper differential pair (transistors M_r). At the bottom of the layout we have the lower differential pair (transistors M_f) and between them the CMOS capacitor (transistors M_C and M_C) finally the smaller transistors are current mirrors. After the layout completion we need to run the Design Rule Check (DRC) and the Layout vs. Schematic(LVS), these tools allow to verify if the layout was done correctly. Only after we can extract the layout, this version includes the parasitics and allow a more realistic simulation. The results are shown on Table 4.9 for the same currents on Table 4.8, although the frequency is reduced the phase noise is improved as does the FOM, this happens because the extracted circuit

only considers R and C parasitics creating in some parts filters, which improve the overall noise of the system. With the layout area we can calculate the FOMA, Table 4.9.

Current (mA)	Frequency (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FOM (dBc/Hz)	FOMA (dBc/Hz)
0.15	0.56	-104.5@10MHz	1.56	-137.5	-159.8
0.5	1.31	-106.5@10MHz	2.4	-145.7	-167.4
1.5	2.21	-110.6@10MHz	4.8	-150.6	-173

TABLE 4.9: Extracted Layout Frequency.

We can compare this oscillator with others in literature using the FOM or FOMA, table Table 4.10 compares other ring oscillators presented recently with various technologies and voltage supply. What really distinguishes this oscillator from the others is the low power consumption and low area. This proves the benefits of using a fully integrated CMOS circuit, with a small area we get a good result for FOMA, as shown on Table 4.10.

Ref	$F_{min} - F_{max}$ (GHz)	Phase Noise (dBc/Hz)	FOM (dBc/Hz)	FOMA (dBc/Hz)
[28]	0.397-4.4	-94.6@1MHz	-157	-
[20]	0.65-1.6	-108@0.2MHz	-169.2	-179
[5]	3.03-5.36	-107@1MHz	-161.35	-182.8
[19]	4.3-6.1	-105@10MHz	-139.9	-145.5
[14]	2.5-9	-82@1MHz	-139.3	-158
[18]	8.4-10.6	-85@1MHz	-147.8	-154.8
[12]	2.3-2.5	-105@1MHz	-155	-165
[11]	3.1-10.6	-108.5@10MHz	-158	-177
this work	0.4-2.2	-110.2@10MHz	-149.5	-171.8

TABLE 4.10: Oscillator Comparison.

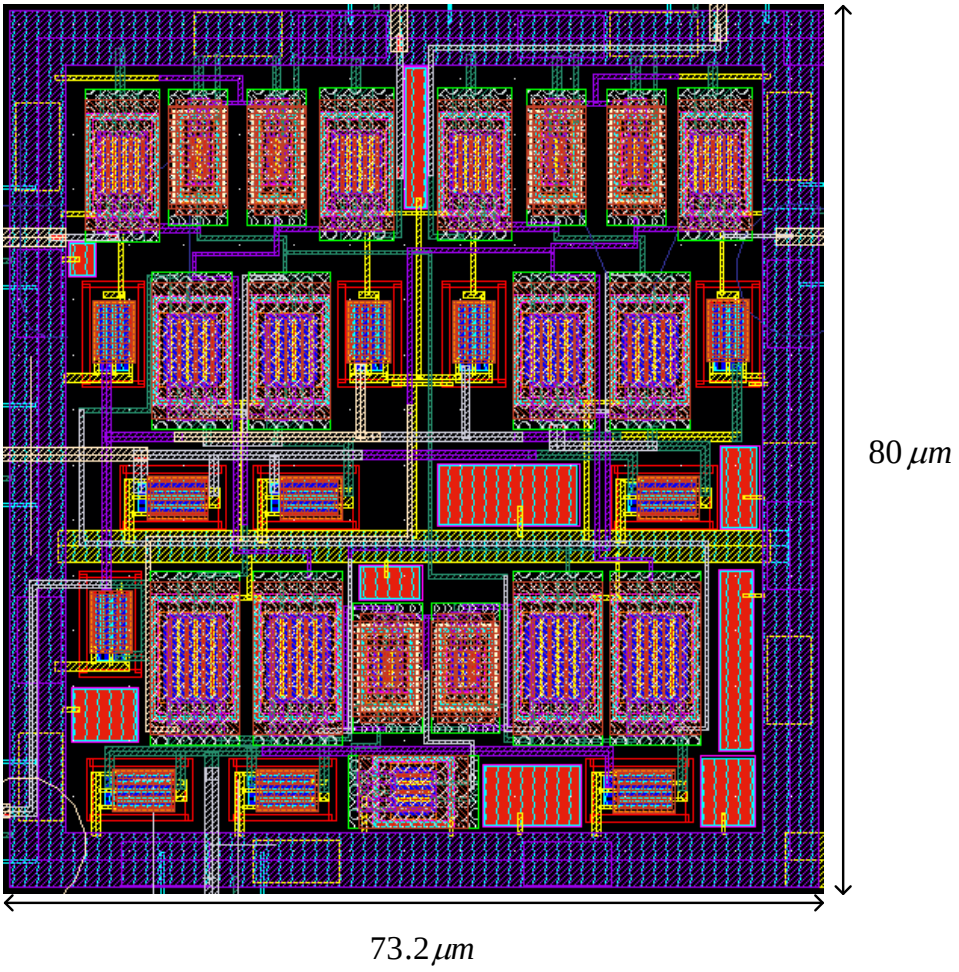

FIGURE 4.27: Layout.

Chapter 5

Conclusions and Future Work

In this thesis we have implemented various oscillators with the objective to comply to the demands of low area, low power consumption, and accurate quadrature outputs. Coupled RC oscillators prove to be a good solution, although single LC oscillator have a better phase noise, they occupy a larger area and when used in quadrature their advantage is lost.

The first circuit presented shows not only a noise improvement in a coupled RC oscillator, but also, how the circuit reacts with mismatches and how much time it takes to synchronize. RC oscillators allow to build a fully integrated CMOS circuit, with this feature we can develop methods to reduce the overall noise. For this purpose, three methods were presented one of them being completely new. With all methods applied to a simple Relaxation oscillator we obtained a phase noise improvement of almost 5 dB. The last circuit was a fully integrated CMOS two integrator with a small area, reduced power consumption, and wide tunning range, its performance were compared with other ring oscillators proposed in recent years.

The CMOS current controlled quadrature oscillator was able to operate in the frequency range of WMTS applications. We tested two types of coupling "hard" and "soft", with the first one showing better results in phase noise, about 2 dB for 600 MHz and 4 dB for 1.4 GHz and also concerning mismatches. The circuit was submitted to a external current with a frequency that is an odd multiple of the oscillation frequency, the oscillator was

able to synchronize after a few periods. At higher frequencies for the "soft" coupling the oscillations stopped, we were unable to determine the reason, further investigation can be made in this matter.

Three methods to reduce phase noise and improve the FOM were implemented. These methods were tested separately and compared with the optimum point before the application of the methods. The new technique introduced in this thesis improves the overall noise, but causes the PMOS transistors to leave the linear region and enter the saturation, during transitions. This situation caused a great reduction of the phase noise around (-132.6 dBc/Hz@10 MHz) but also decreased the frequency around 300 MHz with all methods applied, making a FOM of -159.1 dBc/Hz. The other methods affected the power consumption and the current thermal noise. The pulse self biasing method could have better results by controlling the width of the pulses.

The two integrator covered the WMTS and wireless frequencies. All the resistors and capacitors were implemented with CMOS transistors, making the layout area small, with a total area of $5.856\text{x}10^{-3}$ mm^2 without pads. The fully integrated CMOS circuit shows that it is possible to reduce the occupied area by simply using transistors, there are some implementations that combine this oscillator with a mixer, reducing the total area of a transceiver.

5.1 Future Work

- Layout implementation for all circuits, for future fabrication and measurements;
- The techniques showed can be further applied to other oscillators at higher frequencies;
- New methods can be developed with the substitution of passive elements by transistors.
- Combine more receiver blocks such as the LNA in a single chip, using CMOS technology.

Appendix A

Submitted Papers

A.1 JMCS, 2010

Analysis and Design of CMOS Coupled Multivibrators

International Journal of Microelectronics and Computer Science

Analysis and Design of CMOS Coupled Multivibrators

João Casaleiro, Hugo F. Lopes, Luis B. Oliveira, and Igor Filanovsky

Abstract— **In this paper a wideband MOS quadrature oscillator constituted by two multivibrators is presented. Two different forms of coupling, named here as soft and hard, are investigated. Simulations are performed in a 0.13 µm CMOS technology to obtain the tuning range, the synchronization transients, and the influence of mismatches in timing capacitors and charging currents on synchronization. It is found that hard coupling reduces the quadrature error (about 1º, with 5% mismatches in timing capacitors and charging currents) and results in a low phase-noise (about 2 dB improvement) with respect to soft coupling. Either a single multivibrator or coupled multivibrators can be locked to an external synchronizing harmonic frequency, and the locking range is investigated by simulations. The simulations are done for oscillators covering the WTMS frequency bands.**

Index Terms—**CMOS oscillator, multivibrator, quadrature outputs, van der Pol oscillator, WMTS applications.**

I. Introduction

Quadrature oscillators are key blocks in the design of modern transceivers. In recent years, significant research efforts have been invested in the study of low area and low cost oscillators, with accurate quadrature outputs [1 - 7].

The circuit presented in this paper is intended for use in the Wireless Medical Telemetry Service (WMTS), which establishes wireless communication between an externally worn medical device and other equipment [8]. There are three frequency bands allocated to WMTS: 608 - 614 MHz, 1395 - 1400 MHz and 1427 - 1432 MHz. With the proposed circuit we intend to cover all the bands allowed for these applications.

Emitter and source-coupled multivibrators are used frequently as voltage-controlled oscillators (VCOs) [9-11]. These multivibrators may be coupled [12] to produce quadrature oscillators.

In this paper (Section II) we show why the chosen multivibrator is the most suitable for coupling. In Section III the MOS quadrature oscillator is described. Section IV gives simulation results in a 0.13 µm CMOS technology for the tuning range, the synchronization transients, and the influence of mismatches of timing capacitors and charging currents on synchronization. Section V gives some results for external synchronization. A discussion and some conclusions are given in Section VI.

II. Sinusoidal and Relaxation Oscillations

The bipolar version of the circuit in Fig. 1 (a) was widely used in VCOs [13, 14] and the circuit was considered as a very stable and reliable multivibrator. The tendency to operate at higher frequencies using modern CMOS technologies confirmed that this circuit is able to have sinusoidal operation as well, and the relaxation operation should be considered as the limit form of such operation. As shown below, this circuit is a van der Pol oscillator, for which the transition from sinusoidal to relaxation operation is the natural process connected with continuous change of one of the circuit parameters [11]. Because this circuit has both kinds of operation we will use the words "oscillator" and "multivibrator" rather indiscriminately.

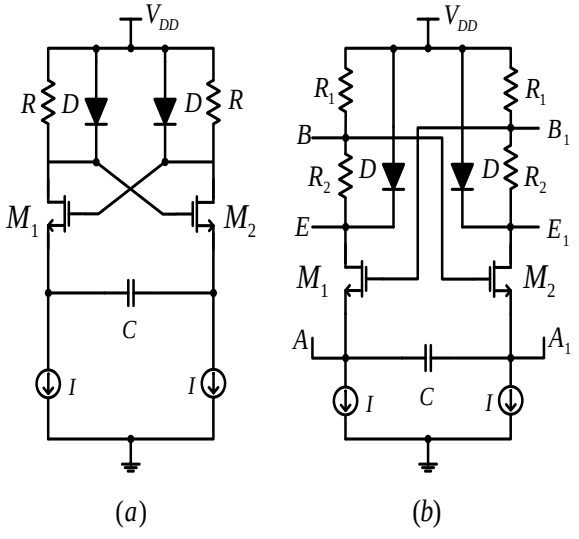

Figure 1. Current-controlled multivibrator (a) and its modification (b).

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Assume that the oscillation amplitude developed on resistors R is so small that the diodes are OFF. Using simplified models (controlled transconductance and gate-source capacitance) for transistors M_1 and M_2 it is possible to show that the capacitor C "sees" the impedance

$$z_{in} = \frac{(C_{gs}s + G)}{G}\frac{(g_{m1} + g_{m2})}{g_{m1}g_{m2}} - \frac{2}{G} \quad (1)$$

where $G = 1/R$. The oscillator characteristic equation is

$$(1/Cs) + z_{in} = 0 \quad (2)$$

Substituting (1) in (2) one obtains that

$$s^2 + \frac{1}{RC_{gs}}\left(1 - 2R\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}}\right)s + \frac{g_{m1}g_{m2}}{RCC_{gs}(g_{m1} + g_{m2})} = 0 \quad (3)$$

When the oscillation starts one may consider that $g_{m1} = g_{m2} = g_{m0} = \sqrt{2\mu_n C_{ox}(W/L)I}$, and (3) can be rewritten as

$$s^2 + \frac{1}{RC_{gs}}(1 - Rg_{m0})s + \frac{g_{m0}}{2RCC_{gs}} = 0 \quad (4)$$

The oscillations will start if the roots of this equation are located in the right half of the *s*-plane. This requires that

$$g_{m0} > 1/R \quad (5)$$

The oscillations will have the frequency

$$\omega_0 = \sqrt{g_{m0}/(2RCC_{gs})} \quad (6)$$

The roots of (4) are

$$s_{1,2} = \frac{g_{m0}R - 1}{2RC_{gs}} \pm \sqrt{\left(\frac{g_{m0}R - 1}{2RC_{gs}}\right)^2 - \frac{g_{m0}}{2RCC_{gs}}} \quad (7)$$

If C varies and all other parameters are constant, the roots move in the right half of the *s*-plane only. For small values of C they are complex-conjugate and located in the vicinity of $j\omega$-axis. The oscillator has quasi-sinusoidal oscillations). With increase of C they move towards the positive real axis. The oscillations become more and more distorted. When $C = (2C_{gs}g_{m0}R)/(g_{m0}R - 1)^2)$ the roots are positive real axis, and one may consider that the circuit has now relaxation oscillations. With further increase of C the roots move along positive real axis arriving to the final values of $s_1 = 0$ and $s_2 = (Rg_{m0} - 1)/(rC_{gs})$. The circuit oscillations are closer and closer to relaxation oscillations with discontinuous waveform. The transition from sinusoidal to relaxation oscillations is smooth with a gradual increase of distortions in the waveform [10] and specific amplitude limiting.

Let us do the approximation

$$\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}} \approx \frac{g_{m0}}{2}\left[1 - \left(\frac{i}{\sqrt{2}I}\right)^2\right] \quad (8)$$

in the damping term of (3), and leave the frequency term the same as in (4). Here i is the capacitor current. Then, one can write for this current the differential equation

$$\frac{d^2i}{dt^2} + \frac{1}{RC_{gs}}\left\{1 - Rg_{m0}\left[1 - \left(\frac{i}{\sqrt{2}I}\right)^2\right]\right\}\frac{di}{dt} + \omega_0^2 i = 0 \quad (9)$$

Introducing the normalized variable $x = i/(\sqrt{2}I)$ and using the notation $\delta_0 = (Rg_{m0} - 1)/(2RC_{gs})$ and $\delta_2 = g_{m0}/(2C_{gs})$, one reduces this equation to the standard van der Pol form

$$\frac{d^2x}{dt^2} - 2(\delta_0 - \delta_2 x^2)\frac{dx}{dt} + \omega_0^2 x = 0 \quad (10)$$

The solution of this equation for small distortions is

$$x = 2\sqrt{\delta_0/\delta_2}\sin\omega_0 t = 2\sqrt{1 - (1/Rg_{m0})}\sin\omega_0 t \quad (11)$$

The amplitude of the voltage between the drain resistors (the usual points of measurements) will be

$$V_{dm} = 4\sqrt{2}I\sqrt{1 - (1/Rg_{m0})} \quad (11)$$

If this amplitudes increases (say, if I increases as a result of tuning) the diodes eventually limit the amplitude. When the circuit moves to relaxation oscillation (at lower frequency) then the amplitude limiting by the diodes is dominating. The frequency may be approximated as

$$f_0 \approx I/(4V_{BE(ON)}C) \quad (12)$$

where $V_{BE(ON)} \approx 0.5$ V (MOS diodes) is the voltage drop on the diode-connected transistors *D*.

Due to the smooth transition from sinusoidal to relaxation oscillations and the existence of amplitude stabilization mechanisms, the frequency tuning range may be very wide [13 - 15]. It can be further increased by the modification shown in Fig. 1 b that allows higher oscillation frequencies, and is suitable for coupling two multivibrators in a quadrature oscillator. The voltage amplitude at the timing capacitor is now lower, but the oscillation frequency is

$$f_0 \approx I/\{4V_{BE(ON)}R_1/[(R_1 + R_2)C]\} \quad (13)$$

To obtain a quadrature oscillator one couples two similar oscillators using differential pairs [12, 16]. The inputs of the coupling differential pairs should be connected to the timing capacitors (at A and A_1). Their outputs can be connected either to nodes B and B_1 or E and E_1. A source with incremental current I_c injected at node B will create an incremental voltage V_b

$$V_b \approx (I_c R_1 R_2)/(R_1 + R_2) \quad (14)$$

(assuming that $r_d << R_2$, where r_d is the diode dynamic resistance). If I_c is injected at node E then V_b will be reduced to

$$V_b \approx (I_c R_1 r_d)/(R_1 + R_2) \quad (15)$$

assuming that $r_d << R_1 + R_2$.

The coupling at E and E_1, is called here "soft coupling"; at the divider taps B and B_1, it is called "hard coupling". If $R_1 + R_2$ is constant the maximum coupling is achieved for $R_1 \approx R_2$.

III. Quadrature Oscillator

To obtain a quadrature oscillator one connects two multivibrators using two coupling differential pairs. Fig. 2 shows the "hard coupling" case. The synchronization mechanism is similar to that described for the coupling of unmodified multivibrators [16]: the coupling current changes the gate voltages of M_1 and M_2.

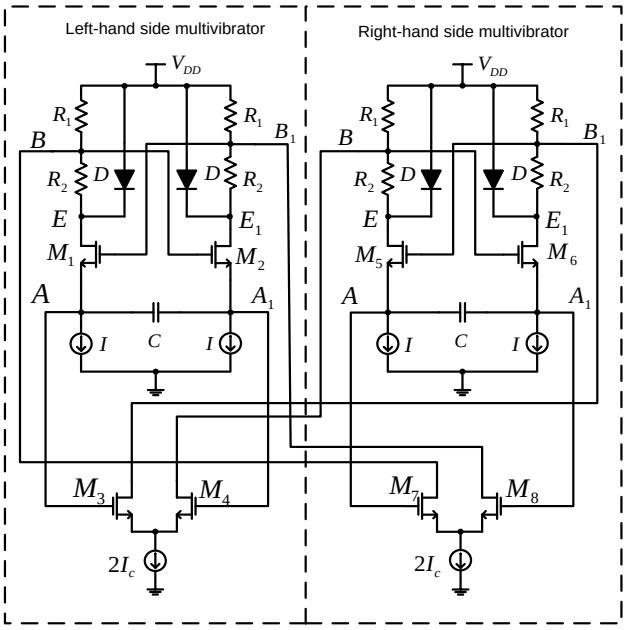

Figure 2. Quadrature current-controlled oscillator with "hard" coupling.

If the coupling current is low in comparison with the tuning current, its influence on the oscillation frequency is very weak. However, this current is able to change the switching time of the transistors M_1 and M_2, and this leads to synchronous oscillation of the constituent multivibrators. This minimizes the influence of noise sources in the switching point, which results in a reduction of the oscillator phase-noise and jitter. The synchronous frequency is approximately given by (13).

The synchronization theory of oscillations in the coupled system with relaxation oscillations is still under development, and we will give the results of simulations, thus, creating the basis for this theory.

IV. Simulation Results

The circuit shown in Fig. 2 is simulated using 130 nm MOS technology. The transistors and resistor sizing are equal for both bands mentioned earlier, as well as the supply voltage (1.2 V). For the lower band the timing capacitor is C = 1.8 pF, and for the other band C = 400 fF. Other values are as follows: $R_1 = R_2 = R$ = 250 Ω, transistors M_1, M_2, M_5 and M_6 have W = 80 µm and L= 300 nm, M_3, M_4, M_7 and M_8 have W = 100 µm and L= 300 nm. The diode-connected transistors have W= 30 µm and L= 300 nm. The coupling current (I_C) is equal to 0.5 mA. Diode-connected PMOS transistors are used, because their temperature characteristics are better than those of NMOS devices.

The oscillator tuning characteristics are obtained by changing the tuning current (I) and the timing capacitor. Simulation results for MOS quadrature oscillators using the traditional "soft" coupling and the new "hard" coupling are presented in Figs. 3 and 4.

The characteristics of Fig. 3 are nearly linear after I = 0.5 mA, which is equal to the value of the coupling current I_C. If the tuning current is lower than the coupling current, the later will have a strong influence on the frequency. This means that, for low tuning currents, the switching times of transistors M_1, M_2, M_5 and M_6 must be taken into account. Hence both currents influence the oscillation period. In the quasi-linear zone these switching times can be neglected [13].

Fig. 4 is obtained by reducing the capacitance C = 400 fF. This causes a decrease of the capacitor charging time and the increase of the oscillation frequency.

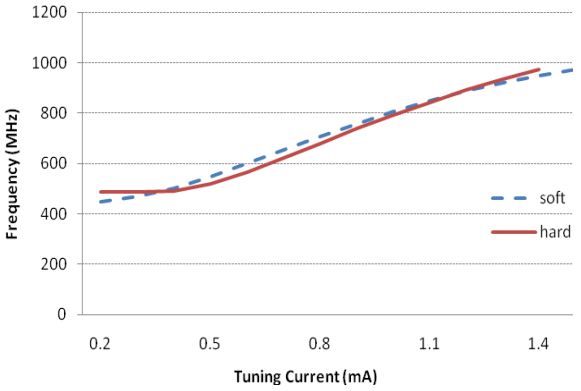

Figure 3. Tuning characteristic for $2I_C$ = 0.5 mA.

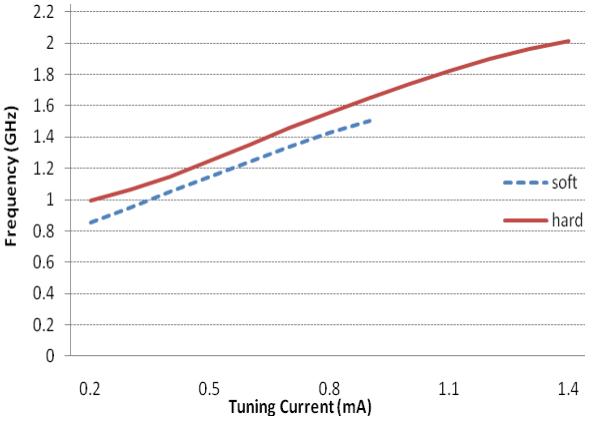

Figure 4. Tuning characteristic for $2I_C$ = 0.5 mA.

Figs. 5 and 6 show the output waveforms at 600 MHz and 1.4 GHz, respectively. Although one could expect a square wave at the output, that doesn't happen due to the "soft" operation of the limiting diodes and the filtering of higher harmonics caused by the parasitic capacitances of the transistors. These parasitics are also responsible for the deviation from linearity at high tuning currents in Figs. 3 and 4.

The oscillator phase-noise is -119.5 dBc/Hz @ 10 MHz offset for "soft" and -121.6 dBc/Hz @ 10 MHz offset for "hard" coupling (as shown in Fig. 7), for the 600 MHz band. For the 1.4 GHz band the oscillator phase-noise is -114.2 dBc/Hz @ 10 MHz offset for "soft" and -117.6 dBc/Hz @ 10 MHz offset for "hard" coupling. Thus, in both frequency bands, we observe a significant reduction of phase-noise for hard coupling.

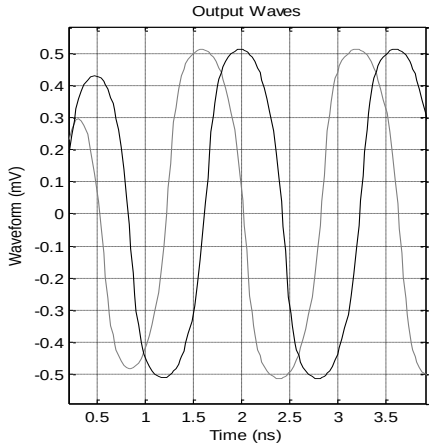

Figure 5. Output waveforms (600 MHz).

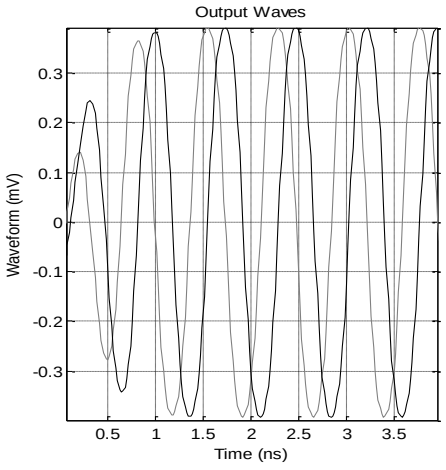

Figure 6. Output waveforms (1.4 GHz).

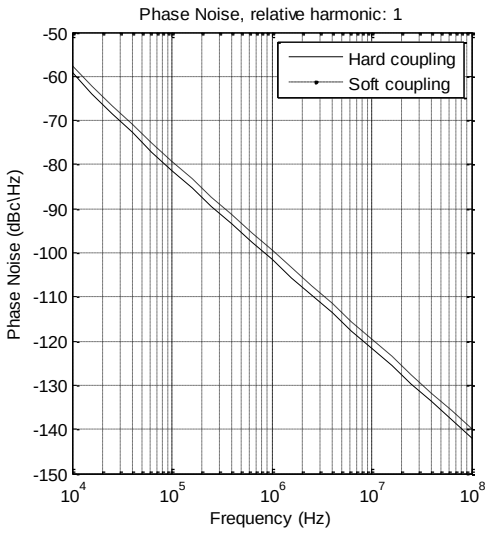

Figure 7. Oscillator phase-noise ("hard" coupling – 600 MHz).

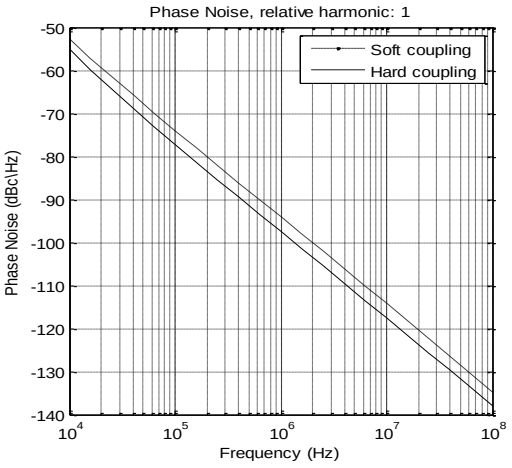

Figure 8. Oscillator phase-noise ("hard" coupling – 1.4 GHz).

Tables I and II show the influence of mismatches in the timing capacitances for "soft" and "hard" coupling for 600 MHz and 1.4 GHz, respectively. There is no oscillation for low values of the "soft" coupling current. In general the "hard" coupling provides significant lower phase error (about 1º) than the "soft" coupling. In Tables III and IV when the frequency mismatch starts to decrease reaching a value close to zero, the "soft" coupling starts to have reduced phase error, when compared to "hard" coupling. For a mismatch of 1% of the capacitances, the phase error is below 0.1º for all currents.

TABLE I. EFFECT OF 5% MISMATCHES IN CAPACITANCES (600 MHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	53.85	10.28	12.27	7.95
0.2	45.21	5.19	12.49	4.22
0.3	34.35	3.23	11.62	2.97
0.4	21.93	2.38	10.44	2.15
0.5	8.22	1.91	8.95	1.66
0.6	6.64	1.62	7.44	1.61
0.7	22.24	1.33	5.92	1.39
0.8	38.43	0.99	4.41	1.17
0.9	54.82	0.95	2.76	0.95

TABLE II. EFFECT OF 5% MISMATCHES IN CAPACITANCES (1.4 GHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	No oscillation		71.86	1.54
0.2			59.49	1.59
0.3	25.19	0.92	46.28	1.09
0.4	20.87	0.86	32.12	0.76
0.5	13.43	0.84	17.33	0.57
0.6	3.56	0.93	2.33	0.4
0.7	8.16	1.02	12.54	0.34
0.8	21.03	1.09	26.96	0.33
0.9	34.51	1.2	40.74	0.29

TABLE III. EFFECT OF 10% MISMATCHES IN CAPACITANCES (600 MHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	59.28	21.23	19.66	15.9
0.2	52.33	9.77	20.31	8.22
0.3	41.63	6.29	19.68	5.7
0.4	29.24	4.5	18.44	4.37
0.5	15.59	3.59	16.98	3.61
0.6	0.83	2.71	15.49	3.12
0.7	14.66	2.19	14	2.77
0.8	30.83	1.84	12.5	2.48
0.9	47.23	1.37	10.97	2.26

TABLE IV. EFFECT OF 10% MISMATCHES IN CAPACITANCES (1.4 GHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	No oscillation		88.93	5.69
0.2			75.18	4.38
0.3	39.09	2.72	62.13	3.04
0.4	34.26	2.47	48.2	2.27
0.5	26.52	2.09	33.73	1.76
0.6	16.4	1.6	19.11	1.37
0.7	4.46	1.01	4.66	1.13
0.8	8.6	0.34	9.45	1.04
0.9	22.29	0.48	22.9	0.91

TABLE V. EFFECT OF 5% MISMATCHES IN TUNING CURRENTS FOR 600 MHZ

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	36.34	10.82	5.81	7.86
0.2	27.96	5.47	5.94	4.03
0.3	16.77	3.65	5.46	3.35
0.4	4.41	2.71	8.69	2.09
0.5	9.29	2.21	10.49	1.74
0.6	24.13	1.88	12.17	1.43
0.7	39.66	1.71	14.03	1.2
0.8	55.85	1.47	15.63	1.05
0.9	72.04	1.52	17.33	0.96

TABLE VI. EFFECT OF 5% MISMATCHES IN TUNING CURRENTS (1.4 GHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	No oscillation		No oscillation	
0.2			26.91	4.6
0.3	6.15	3.87	13.1	3.39
0.4	9.41	3.01	1.9	2.73
0.5	16.24	2.58	17.62	2.3
0.6	25.51	2.34	33.58	2.01
0.7	36.49	2.08	49.35	1.81
0.8	48.61	1.94	64.76	1.57
0.9	61.23	1.95	79.6	1.45

TABLE VII. EFFECT OF 1% MISMATCHES IN TUNING CURRENTS (600 MHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	44.26	2.2	1.75	1.57
0.2	35.27	1.17	1.73	0.82
0.3	24.31	0.76	0.87	0.52
0.4	11.86	0.68	0.54	0.32
0.5	1.81	0.53	2.06	0.24
0.6	16.6	0.64	3.65	0.15
0.7	32.16	0.56	5.26	0.09
0.8	48.38	0.6	6.85	0.27
0.9	64.87	0.67	8.45	0.32

TABLE VIII. EFFECT OF 1% MISMATCHES IN TUNING CURRENTS 1.4 GHZ

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	No oscillation		No oscillation	
0.2			40.04	1.91
0.3	7.65	2.49	26.46	1.43
0.4	3.85	1.98	11.79	1.17
0.5	3.31	1.79	3.49	0.97
0.6	12.92	1.59	18.98	0.87
0.7	24.32	1.57	34.38	0.81
0.8	36.91	1.55	49.3	0.73
0.9	50.12	1.52	63.74	0.57

TABLE IX. EFFECT OF 10% MISMATCHES IN TUNING CURRENTS (600 MHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	24.29	23.23	15.73	15.93
0.2	17.79	10.86	15.82	8.42
0.3	7.18	7.11	17.28	5.79
0.4	5.12	5.27	19.17	4.42
0.5	18.67	4.33	21.16	3.64
0.6	33.31	3.62	23.19	2.95
0.7	48.75	3.03	25.13	2.59
0.8	64.73	2.72	27.04	2.32
0.9	80.69	2.53	28.73	1.97

TABLE X. EFFECT OF 10% MISMATCHES IN TUNING CURRENTS (1.4 GHZ)

	Soft coupling		Hard Coupling	
2 I_C (mA)	**Δ f (MHz)**	**Phase error (º)**	**Δ f (MHz)**	**Phase error (º)**
0.1	No oscillation		No oscillation	
0.2			10.92	8
0.3	22.66	5.92	3.18	5.83
0.4	25.24	4.51	18.61	4.66
0.5	31.63	3.81	34.84	3.95
0.6	40.43	3.21	51.33	3.44
0.7	50.89	2.85	67.72	3.06
0.8	62.36	2.65	83.78	2.77
0.9	74.4	2.41	99.11	2.42

A larger mismatch requires a larger coupling current to establish synchronous operation (locking), but this leads to a much increased phase error. This error may be reduced by further increasing the coupling current, but this influences the frequency.

Simulations show that the coupling current should be increased when the tuning currents are mismatched, since the phase error is reduced with increase of the coupling current. The phase error is lower for "hard" than for "soft" coupling. The "hard" coupling provides a significant lower quadrature error and allows higher coupling currents without stopping the oscillations. In comparison with the results presented in [7] the proposed circuits exhibits a lower phase error, assuming the same coupling current, i.e. 0.5mA.

V. FREQUENCY LOCKING

We also investigated frequency locking at a sub-harmonic frequency when an external current source is applied between points B and B_1 (see Fig. 1b). The oscillator at 600 MHz can be synchronized by a current source with 100 μA of amplitude, as shown in Fig. 9.

It should be noted that locking is observed only for odd harmonics, since the multivibrator output signal has odd symmetry, and, therefore, has odd harmonics only.

We injected a locking signal in the oscillator running at the frequency of 600 MHz. It was possible to lock the oscillator up to the 11^{th} sub-harmonic frequency. Fig. 10 shows the free running oscillations (up to 10 ns) and the application of locking signal after 10 ns. It is seen that the multivibrators are locked in just 2 periods. This is an advantage of multivibrators: they have short transients, and therefore, they can adjust the frequency in one or two periods. This is one reason (sometimes neglected) why RC oscillators survive. The LC oscillators would have long transients and they need, in some cases, hundreds of periods to adjust the oscillation frequency. Similar results are obtained for the free-running frequency of 1.4 GHz, but, the maximum sub-harmonic frequency to lock the oscillator is the 5^{th}.

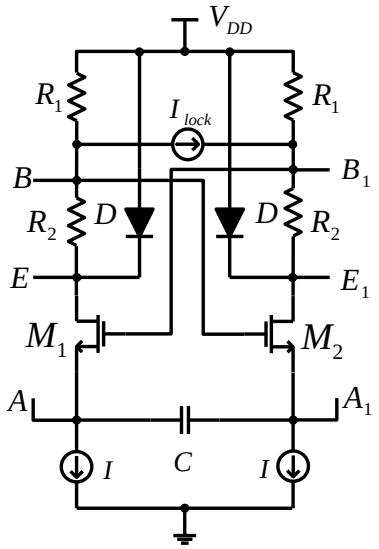

Figure 9. Sub-harmonic injection-locked multivibrator.

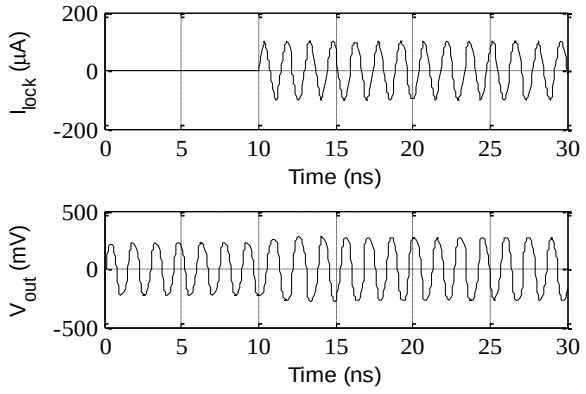

Figure 10. Waveforms for the injection locking.

We also investigated the locking range of the single multivibrator for a particular harmonic. For example, the oscillator does not lock with a frequency lower than 550 MHz, and higher than 860 MHz for the first harmonic. With higher harmonics the oscillator will have lower locking range, as shown in Table XI.

Considering two coupled multivibrators and injecting a current in one of them, the locking range is much smaller, as it is also shown in Table XI. This locking is possible only if the injection current is higher than the coupling current (in the presented case I_C = 500 μA) and one can only synchronize the system up to the 5th harmonic. For 1.4 GHz the locking range goes to the 7th (as shown in Table XII).

With a mismatch of 5 % in currents *I*, one can lock the oscillator with an external signal of frequency (3.379 GHz) up to 5 times the free-running frequency (about 600 MHz), as shown on Table XIII. This frequency ratio is reduced to 3 if we increase the mismatch to 10 % (2.027 GHz). Thus, the frequency ratio and the locking range are reduced when there are mismatches in bias currents. Mismatches in capacitors have the same effect.

TABLE XI. OSCILLATOR LOCKING RANGE

	Single Oscillator		**Coupled Oscillators**	
Harmonic number	**Low freq. (GHz)**	**High freq. (GHz)**	**Low freq. (GHz)**	**High freq. (GHz)**
1	0.55	0.86	0.46	0.75
3	1.85	2.2	1.7	2.1
5	3.33	3.45	3.04	3.33
7	4.73	4.75	-	-
9	6.079	6.1	-	-
11	7.4345	7.44	-	-

TABLE XII. OSCILLATOR LOCKING RANGE 1.4 GHZ

	Coupled Oscillators	
Harmonic number	**Low freq. (GHz)**	**High freq. (GHz)**
1	1.1	1.65
3	3.8	4.2
5	6.7	6.8
7	9.45	9.48
9	-	-

TABLE XIII. OSCILLATOR LOCKING WITH MISMATCH

	Single Oscillator			
	Mismatch 5%		**Mismatch 10%**	
Harmonic number	**Low freq. (GHz)**	**High freq. (GHz)**	**Low freq. (GHz)**	**High freq. (GHz)**
1	0.56	0.86	0.57	0.88
3	1.88	2.2	1.95	2.2
5	3.38	3.45	-	-
7	-	-	-	-

Simulation results with external locking show that the multivibrators in Fig. 2 do not necessarily run at the same frequency. The multivibrator of lower frequency can be in lock with a multivibrator running at a higher frequency, and the locking has the properties similar to the locking at an external synchronizing source.

VI. DISCUSSION AND CONCLUSIONS

The simulation results show that using the proposed low area and low cost oscillator circuit, we can cover the frequency range required for WMTS applications.

The proposed oscillator has three degrees of freedom to control the oscillation frequency: the timing capacitance, the gate voltage (which depends on the resistor divider ratio), and the tuning current. These can be used to maximize the tuning range, to alter the shape of the tuning characteristic and to move it to a desirable range. The same degrees of freedom are preserved when two oscillators are coupled to obtain a quadrature oscillator.

Simulations in a 130 nm CMOS technology show that the quadrature oscillator is very robust with respect to mismatches of timing capacitors and of charging currents, especially with "hard coupling". The frequency tuning range is from 450 MHz to about 1 GHz, covering the 600 MHz band. By reducing the capacitor value (this can be done using a varactor and/or a discrete control), the tuning range becomes 1 GHz to 2 GHz

for “hard” coupling, thus, covering the 1.4 GHz band. These bands are required for biomedical applications.

We are unable, at the present time, to explain why the oscillations stop at higher frequencies. This problem requires further investigation.

The circuit presented in this paper can be synchronized by an external current with a frequency that is an odd multiple of the oscillation frequency. This synchronization can be applied to one of the two multivibrators in the quadrature oscillator. The synchronization transient is fast, and synchronized oscillation is set in a few periods. This sub-harmonic locking can be useful in design of PLL frequency dividers.

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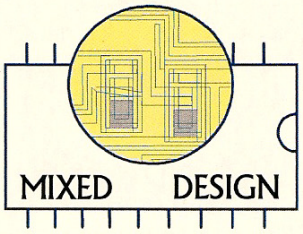

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A 1 mW Low Phase-Noise Relaxation Oscillator

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A 1 mW Low Phase-Noise Relaxation Oscillator

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***Abstract*— We present a new RC relaxation oscillator with pulse self biasing, to reduce power consumption, and with harmonic filtering and resistor feedback, to reduce phase-noise. A circuit prototype designed in a 130 nm CMOS technology has a very low phase-noise, -132.6 dBc/Hz @ 10 MHz offset, and the power consumption is only 1 mW, which leads to a figure of merit (FOM) of -159.1 dBc/Hz.**

I. INTRODUCTION

RC-oscillators have higher phase-noise than LC-oscillators [1, 2]. Yet, RC-oscillators have lower area (inductors are not required), and can be realized in a low cost technology (several metal layers and a thick top metal layer, required for high Q inductors, are avoided). Thus, RC-oscillators are, in some applications, a viable alternative to LC-oscillators when minimization of area (and cost) is important [3].

RC oscillators can be divided into ring oscillators and relaxation oscillators. Relaxation oscillators have two advantages with respect to ring oscillators: they have a constant frequency tuning gain, and their triangular waveform is required in some applications [4].

The oscillators phase-noise can be compared using the FOM definition given in [5] (for the $1/f^2$ region). In [6] it is shown that, at 290K, thermodynamics limits FOM of ring oscillators to -165.3 dBc/Hz and FOM of relaxation oscillators to -169.1 dBc/Hz. Interestingly, it is also shown that FOM of practical ring oscillators is generally below than -160 dBc/Hz, while FOM of practical relaxation oscillators is about 10 dB worse. Thus, in theory relaxation oscillators can be better than ring oscillators, but in practice they are not. An explanation is given in [2]: the noise added by the comparator, used in relaxation oscillators but not in ring oscillators, increases the phase-noise.

The objective of this paper is to present a very low power, 1 mW, relaxation oscillator. We use switched biasing and harmonic filtering (similar to what have been used in LC oscillators [7]). A new local feedback, in which the resistance value changes during the switching, allows a significantly reduction of the effect of comparator noise. This results in a low phase-noise oscillator, with FOM better than -159 dBc/Hz.

Section II reviews relaxation oscillators and section III presents the new relaxation oscillator, and the techniques of pulse self biasing, harmonic filtering, and local resistor feedback are described in detail. Section IV presents the simulation results, and in Section V we draw some conclusions.

II. RELAXATION OSCILLATORS

RC relaxation oscillators have a high level model composed of an integrator and an inverting Schmitt-trigger, as shown in Fig. 1. The typical circuit implementation of the oscillator is shown in Fig. 2. The integrator is simply a capacitor, which is charged and discharge by two current sources. The Schmitt-trigger is the remaining circuit, shown in Fig. 3; it is assumed that the transistors act as switches [3].

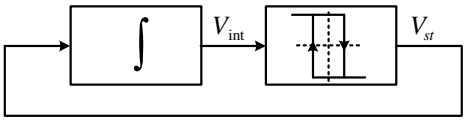

Figure 1. High level model of relaxation oscillator.

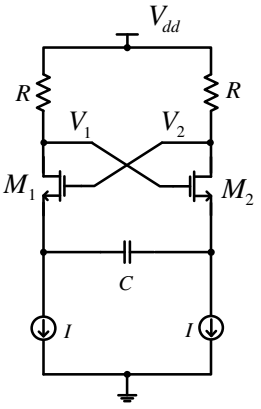

Figure 2. Relaxation oscillator implementation.

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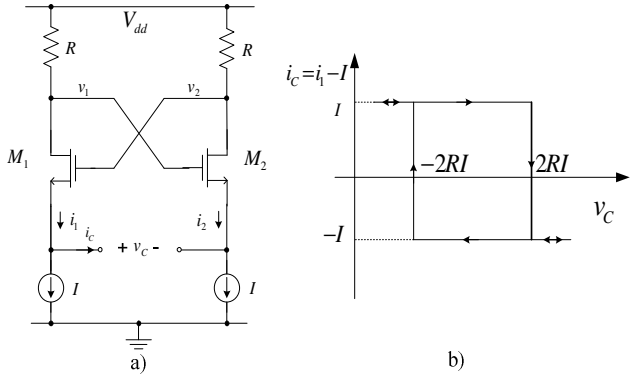

Figure 3. a) Schmitt trigger b) transfer characteristic.

III. PROPOSED RELAXATION OSCILLATOR

In this section we will describe in detail the three techniques that are used for minimizing the oscillator power consumption and phase-noise.

A. *Pulse Self Biasing*

Conventional relaxation oscillators have two current sources that charge and discharge the capacitor. Each one is active only during half of the period. Pulse self-biasing consists of replacing the two current sources by one and switch its current using a differential pair, controlled by the oscillator outputs, as shown is Fig. 4.

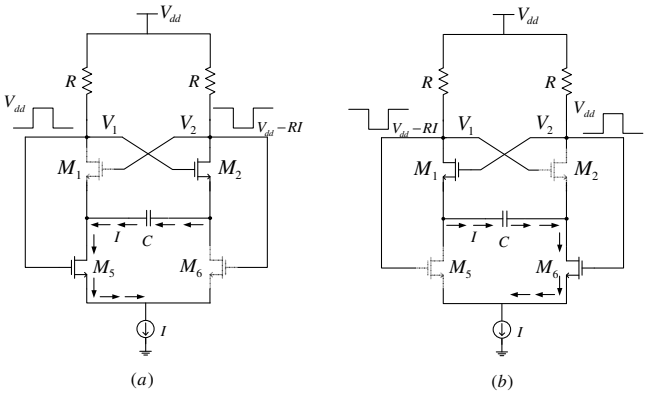

Figure 4. Self Biasing.

This current reuse reduces the power consumption by 2. However, it requires two extra transistors (higher die area), and adds two extra noise sources.

B. *Hamonic filtering*

To minimize the noise of the current source, one should filter out the even harmonics (especially the second harmonic) of its voltage (Fig. 5). This is similar to what has been done in LC oscillators [7]. Since the differential pair introduced in the first method acts as a mixer [7], the noise frequencies at the second harmonic are down-converted to the oscillation frequency, causing an increase of phase-noise. This is avoided by placing a large capacitance in parallel with the current source: the resulting low pass filtering, removes the even harmonics.

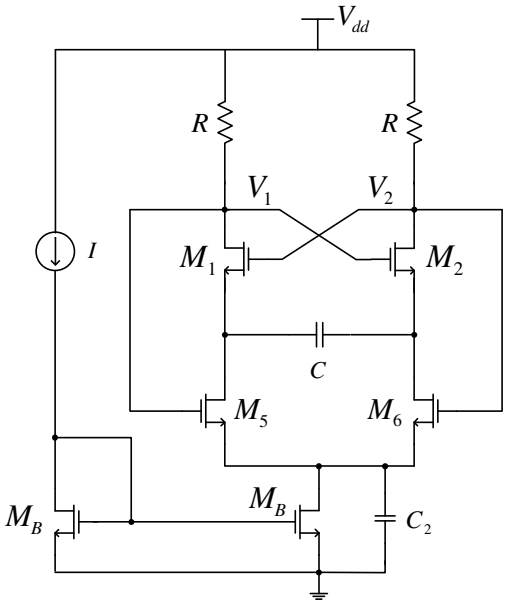

Figure 5. Harmonic content in a Oscillator.

C. *Resistor feedback*

This method can be applied if we replace the resistors by MOS transistors. The oscillator switches when the capacitor voltage reaches the Schmitt-trigger input switching levels. The idea is to modify these levels close to the switching time to obtain a faster switching. This can be archived by using local feedback, as shown in Fig. 6.

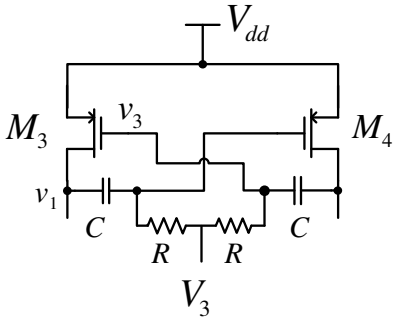

Figure 6. Local feeback.

By combining all the above three methods ,the final circuit, shown in Fig. 7, is obtained.

IV. SIMULATION RESULTS

The circuit of Fig. 7 is implemented using a 130 µm CMOS technology. The components have the following sizing $W_{1,2}$ = 80 µm, $L_{1,2}$ = 400 nm, $W_{3,4}$ = 15 µm, $L_{3,4}$ = 260 nm, $W_{5,6}$ = 15 µm, $L_{5,6}$ = 260 nm, the current mirror transistor M_B has W_B = 15 µm and L_B = 360 nm; C = 1.8 pF, $C_1 = C_2$ = 5 pF, and R = 20 kΩ. The PMOS transistors biasing voltage is V_3 = 100 mV and V_{dd} = 1.2 V (the equivalent resistance is 300 Ω).

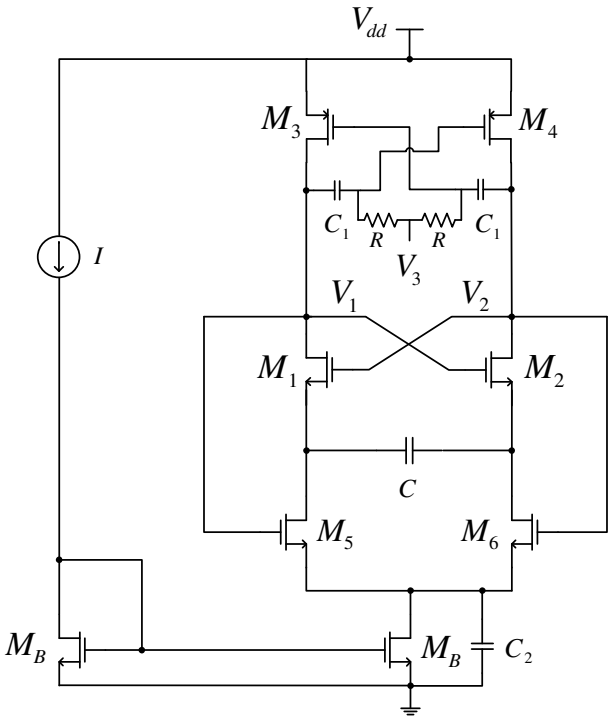

Figure 7. The proposed oscillator circuit.

In Fig. 8 it is observed that the oscillator phase noise is reduced with harmonic filtering (the reduction of second harmonic is shown in Fig. 9), and a stronger reduction results from local feedback.

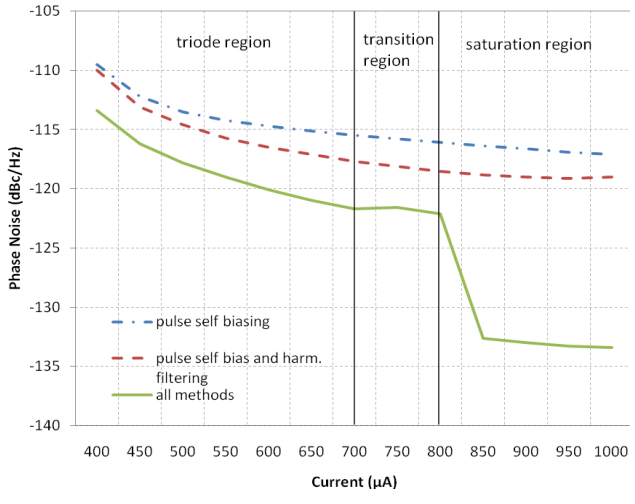

Figure 8. Oscillator phase-noise.

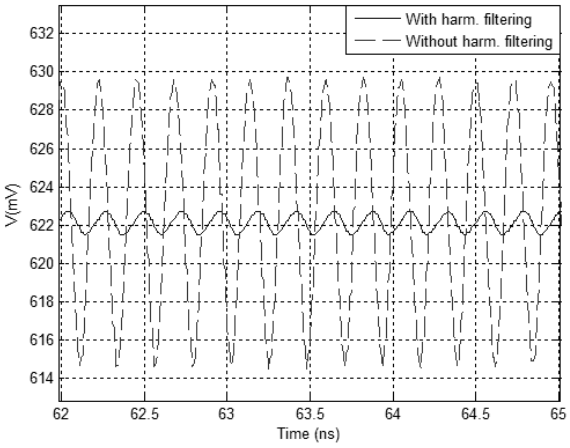

Figure 9. Second harmonic filtering (effect of adding C_2).

The PMOS transistors are biased in the triode zone and have an equivalent resistance of 300 Ω. However, during the switching they can operate in different regions. For low biasing currents they are always in triode, but, for high currents they reach saturation, which changes the equivalent resistance value and reduces the oscillator phase-noise (as shown in Fig. 8) and the oscillation frequency (as shown in Table I).

TABLE I. OSCILLATION FREQUENCY.

Current (µA)	Pulse self-biasing	Pulse self-biasing and filtering	All Methods
400	575.9	579.3	504.5
450	586.6	594.6	513.9
500	592.1	605.5	518.2
550	593.3	612.9	518.4
600	591.7	617.9	514.8
650	587.9	621.1	506.7
700	582.8	622.8	490.9
750	576.6	623.3	459.2
800	569.9	622.5	387.7
850	562.5	620.5	213.6
900	554.6	616.8	196.9
950	546.1	611.4	188.8
1000	537.3	604.3	183.7

In order to compare this circuit with the state-of-the art relaxation oscillators, we will use the conventional figure of merit (FOM) [8]

$$\text{FOM} = \mathcal{L} + 10\log\left(\left(\frac{\Delta f}{f}\right)^2 \frac{P_{DC}}{P_{ref}}\right) \quad (1)$$

where $\mathcal{L}$ represents the oscillator phase-noise (normalized single sideband noise spectral density expressed in decibels below the carrier per hertz), P_{DC} is the power consumption, and P_{ref} is a reference power level (1 mW).

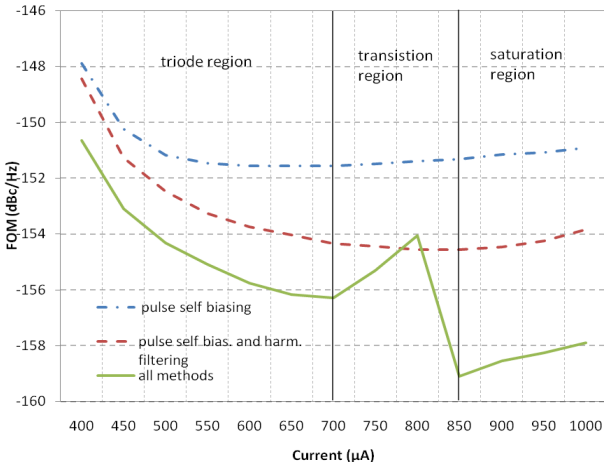

Figure 10. Oscillator FOM.

From Fig. 10, we can conclude that the oscillator at 850 µA reaches an optimal FOM of -159.1 dBc/Hz. This is at least 4 dB better then sate-of-the art relaxation oscillators, with the same circuit topology [9 - 11]. This result is below the best relaxation oscillator, published by Nauta in ISSCC [4], but this has a completely different circuit, using switched-capacitors, and operates at only 12 MHz, so it is not included in the comparison. In Table II the performance of the proposed relaxation oscillator is compared with state-of-the art continuous-time relaxation oscillators with the same frequency range.

TABLE II. COMPARISON WITH STATE-OF-THE ART RELAXATION OSCILLATORS.

Ref.	**Freq. [MHz]**	**$\mathcal{L}$ (Δf) [dBc/Hz]**	**Power [mW]**	**FOM [dBc/Hz]**
[5]	1.5	-102 @ 10 kHz	0.3	-150
[9]	920	-102 @ 1 MHz	10	-151.3
[12]	6	-110 @ 10 kHz	20	-153.6
[11]	6000	-97.1 @ 10 MHz	36	-154
[10]	2400	-105 @ 1 MHz	48	-155
This Work	**210**	**-132.6 @ 10 MHz**	**1**	**-159.1**

V. CONCLUSIONS

In this paper we presented a low phase-noise and low power RC relaxation oscillator. The technique to reduce power consumption is pulse self-biasing, which allows the use of a single current source, with current reuse. The phase-noise is reduced by harmonic filtering, and by a local feedback.

Simulation with a 130 nm CMOS technology shows a very low phase-noise: -132.6 dBc/Hz @ 10 MHz offset, with only 1 mW power consumption. The FOM is -159.1 dBc/Hz, which is better than state-of-art relaxation oscillators for the same frequency range.

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