Efficient Digital Self-Calibration of Video-Rate Pipeline ADCs using White Gaussian Noise

M. Unterweissacher[1,3], J. Goes[1,2], N. Paulino[1,2], G. Evans[1] and M. D. Ortigueira[1,2]

[1] UNINOVA – CRI
Campus da FCT/UNL
2825 – 114 Caparica – PORTUGAL
E-mail: martin@unterweissacher.at

[2] Faculdade de Ciências e Tecnologia
Campus da FCT/UNL
2825 – 114 Caparica – PORTUGAL
E-mail: jg@uninova.pt

[3] Technische Universität Graz
Institut für Elektronik
Infeldgasse 12, 8010 Graz – AUSTRIA
E-mail: martin@unterweissacher.at

Abstract - *A digital-domain self-calibration technique for video-rate pipeline A/D converters based on a white Gaussian noise input signal is presented. The implementation of the proposed algorithm requires simple digital circuitry. An application design example of the self-calibration of a 12b, 40 MS/s CMOS pipeline ADC is shown to illustrate that the overall linearity of the ADC can be highly improved using this technique.*

1. INTRODUCTION

A broad area of applications with enhanced performance requires high-resolution analogue-to-digital (A/D) conversion with sampling rates (F_S) in the range of tens of MHz. The most attractive solutions for implementing this kind of A/D converters (ADC's) employ pipelining as a way to relax the speed requirements of the analogue components. Such architectures use a cascade of stages comprising a low-resolution flash quantizer and a multiplying digital-to-analogue converter (MDAC), which computes and amplifies the residue for the next stages. As a consequence, the precision requirements are more critical in the front-end stage of the pipeline, which must exhibit the accuracy of the overall ADC, and are progressively relaxed towards the last stage. Without using trimming or self-calibration techniques, the overall resolution of these ADC's is limited by the linearity and gain errors of the front-end MDAC's. These errors are bounded around the 8-10 bit level by the component matching accuracy of most available CMOS processes. As trimming is expensive, self-calibration either in the analogue or in the digital domain must be considered for extending the resolution of such ADC's above 10-bits. Analogue techniques require calibration DACs and precision analogue components [1, 2]. Although, digital calibration techniques do not require sophisticated analogue circuitry they put an extra burden on the digital part [3, 4]. Furthermore, the MDAC of a calibrated stage has to be modified (additional switches) to perform the required code-error measurements [4]. Moreover, the technique proposed in [3] can only be employed in 1.5-bit MDACs and, therefore, it is not suitable for power-optimized high-resolution architectures where multi-bit front-end stages are preferred [5].

2. DESCRIPTION OF THE PROPOSED TECHNIQUE

The technique proposed in this paper and conceptually described in [6] consists off applying a white Gaussian noise (WGN) stimulus to the ADC and calculating the calibrating-codes from the histogram of the output codes. There are several advantages of this self-calibration technique compared with those reported in [3, 4]: 1. The entire ADC does not need to be modified; 2. It is suitable for ADC's with multi-bit front-end stages; 3. Wide-band WGN is relatively easy to generate on-chip using a high closed-loop gain amplifier (*e. g.* ≈ 70dB) with small input transistors and input resistors as main noise sources [7]. 4. The accuracy requirements of the standard deviation are relaxed. 5. WGN having a uniform power spectral density allows a full-speed characterization of the ADC [8]; 6. On-chip self-testing can be done. 7. The use of a histogram will eliminate uncertainties from the calibrating-codes due to noise; 8. The input noise stimulus has not to be necessarily white as long as it remains Gaussian.

In an N-bit pipeline ADC comprising an M_1-bit front-end stage and N_S stages, the overall linearity is mainly limited by the mismatches in the first MDAC. A typical conversion characteristic consists basically off 2^{M_1} segments dislocated from an "almost" ideal straight-line. The gain-error of the MDAC affects the slope of these segments and it is added to the jumps between 2 segments. A slightly lower than radix 2 inter-stage gain should be used in the first MDAC, because a gain-error, where the residue exceeds the allowed range, cannot be corrected by a digital method. This slightly reduces the full-scale range of the entire ADC, but, on the other hand, ensures a successful self-calibration. The digital amounts of displacement can be measured during a calibration cycle and stored in a memory. Because fully differential MDAC's exhibit code error symmetry, only one half of the calibrating-codes has to be calculated. These $2^{(M_1-1)}$ calibrating-codes can be later addressed and recalled during normal conversion-mode, using the coarse digital outputs from the first stage M_1-bit quantizer and, the conversion characteristic is moved back to the ideal line (minus the reduced gain) by digitally subtracting these codes. Applying centered WGN to the input of the ADC, a $(2^{(M_1-1)}+1)$ bin histogram can be computed by counting the number of occurrences of the output-codes inside these bins, where each bin covers a range of output codes that contain one expected step in the transfer characteristic. This histogram, $H[i]$, will have a Gaussian-shape, more or less "distorted" by the existing deviations of the segments. Assume now that there is a

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specific table, $T[i]$, with $2^{(M_1-1)}+1$ values, truncated and stored in a memory, and defined by

$$T[i]=(A[i])^{-1},\quad A[i]=\int_{C_{bin}(i)-\frac{binwidth}{2}}^{C_{bin}(i)+\frac{binwidth}{2}}\left(\sigma\cdot\sqrt{2\pi}\right)^{-1}e^{\frac{-(x-\mu)^2}{2\sigma^2}}dx\ , \tag{1}$$

where C_{bin} is the center of the bin and $A[i]$ represents the ideal histogram produced mathematically using a Gaussian distribution function with $\mu=2^{(N-1)}$ and $\sigma=2^{(N-1)}/2$. $T[i]$ is used to normalize $H[i]$ resulting, in the ideal case, in a uniformly distributed histogram with 2^n occurrences in each bin. The differences from this expected value can be used to calculate the calibrating-codes. Thus, assuming a large number of samples, n the nonlinearity step is given by

$$D[i]=\frac{(H[i]\cdot T[i]-2^n)\cdot binwidth}{2^N}\cdot\frac{1}{2^{(n-N)}}\ , \tag{2}$$

where the first term comprises the difference of the normalized occurrences to the ideal number reduced from 2^n to the bin-size related value and, the second term, scales this value using the expected number of samples in one bit. So *D[i]* contains the summed non-linearity of one bin scaled to an equivalent INL step in one bit. With these values it is possible to calculate the segment deviations from the ideal transfer characteristic using:

$$\begin{aligned} &Dev[k]=D[k]+D[2^{M_1-1}-k]\quad \text{for}\quad 1\le k<2^{M_1-1}\\ &Dev[k]=D[k]\quad \text{for}\quad k=2^{M_1-1}\end{aligned} \tag{3}$$

D[i], except the central bin, is then added to the corresponding symmetric bin to eliminate small errors in symmetry caused by a small offset voltage. The gain-error of the ADC, ε_{GAIN}, as well as the $2^{(M_1-1)}$ calibrating codes, $C_{CODE}(k)$, can be found according to

$$\begin{aligned} &C_{CODE}(1)=-\varepsilon_{GAIN}=-0.5\sum_{k=1}^{2^{(M_1-1)}}Dev[k]\\ &C_{CODE}(k)=C_{CODE}(k-1)+0.5\cdot Dev[k],\ 1<k\le 2^{(M_1-1)}\end{aligned} \tag{4}$$

Due to the code error symmetry it is then possible to use the same calibrating-codes for the remaining segments:

$$C_{CODE}(k)=-C_{CODE}\left(2^{M_1}-k+1\right),\quad k>2^{(M_1-1)} \tag{5}$$

The number of samples in each bin is described by the binomial distribution, $B(\mu=n\cdot p[i],\sigma=\sqrt{n\cdot p[i]\cdot(n-p[i])})$, where $p[i]$ represents the probability of a given sample falling into the i-th bin (that depends on the *bin width* and on the σ of the WGN generator). An accuracy of 1/16 LSB@*N*-bit with a yield of 3σ has to be reached to limit accumulated measurement errors below 0.5 LSB. To ensure this the outermost bins, representing the worst case, are used to calculate the minimum number of samples. The number of samples needed to adjust the offset and the standard deviation of the WGN generator is calculated in the same way but using different bins and accuracy limits.

The required accuracy concerning the statistical properties of the WGN stimulus depends mainly on the size of the bins. The standard deviation σ has a linear influence on the measured transition voltages [8] and on the non-linearities. Because the measurement errors due to a not exactly adjusted σ accumulate over the observed code range, it is an advantage to use narrow bins at the code transitions of interest. To reach a DNL measurement error with less than the desired value ξ_{BIN} , $\Delta\sigma_{\max}$ is defined by:

$$\Delta\sigma_{\max}=\frac{\xi_{BIN}\cdot 2^N}{binwidth} \tag{6}$$

In the presented simulation examples, a *bin width* of 64 bits and a required $\xi_{BIN}\le 1/16\,LSB$ allow the use of a 9 bit accurate σ to calibrate a 12 Bit ADC! The offset of the WGN and of the ADC is calibrated digitally during the generator setup to obtain a symmetric histogram. This is sufficient to ensure that the subsequent steps of the calibration of the ADC do not fail.

3. Simulated Results

To validate the theoretical findings and assess the performance of the proposed technique a 12 bit ADC with the architecture presented in Fig. 1 was modeled using MATLAB code. The main static non-ideal effects were included namely, the offset voltages in the comparators of the quantizers and the matching accuracy (9-bit) in the capacitor-arrays in all MDAC blocks. The gain of the 3-bit front-end MDAC was nominally set to 3.9. The input-referred thermal noise of the ADC was also included and defined at 0.5 LSB below the quantization noise.

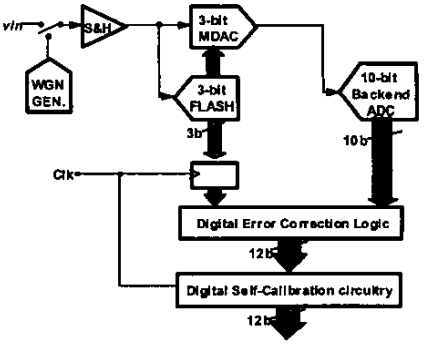

Fig. 1: Architecture of the simulated ADC

An amount of $n = 2^{24}$ samples was used to compute the histogram $H[i]$ with 7 bins. This number of samples is sufficient for adjusting the WGN-generator and performing the

self calibration. To save simulation time only the histogram for the calibration algorithm but not for the WGN adjustment was calculated. The standard deviation of the WGN was set to $\pm 2\sigma$ @ full-scale plus the maximal allowed error. The figures 2 and 5 show, respectively, the INL of the ADC before and after calibration, measured using a static method by sweeping the input of the ADC with a full-scale ramp with steps of 1/8 LSB@12-bit. After calibration the initial INL of +4.5/-4.0 LSB is improved to values between ± 1LSB. Fig. 3 shows the averaged (*binwidth* = 10) histogram distortions caused by the ADC and Fig 4 shows the steps in the conversion characteristic calculated by the self-calibrating algorithm (*binwidth* = 64). Several simulations were carried-out with variations of the WGN generator offsets between ± 8 mV and the maximum INL errors after calibration were always within ± 1 LSB, since about 1 bit is lost due to the accumulation of the digital truncation errors. The expected time for a complete calibration-cycle is about 600ms if the ADC is sampling at F_S = 40 MS/s.

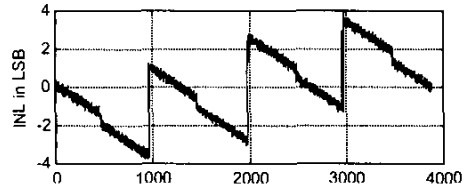

Fig. 2: INL before calibration

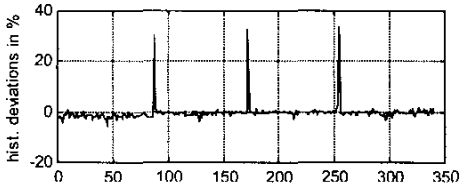

Fig. 3: averaged histogram deviations

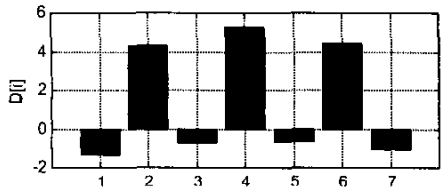

Fig. 4: calculated steps in conversion characteristic

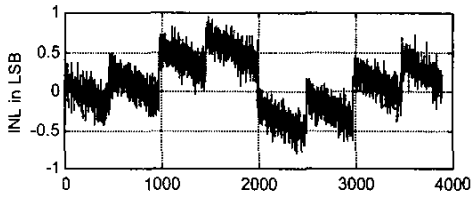

Fig. 5: INL after calibration

4. IMPLEMENTATION OF THE BASIC BLOCKS

A) The Digital Circuitry

To implement the proposed digital self-calibration algorithm, the system presented in Fig. 6 is used. The 12 bit adder/subtractor performs the correction using the calibrating-codes that are saved in 4 registers (C1 to C4). The most significant bit of the ADC output decides if the codes are added or subtracted to reduce the number of required code-registers. Calibrating-codes with seven bits length allow correcting nonlinearities up to 128 LSB including the corrections enforced by the reduced interstage gain.

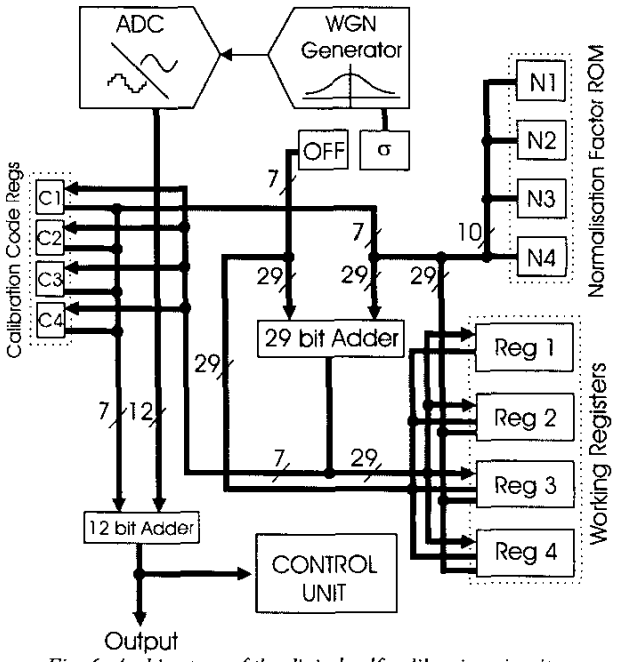

Fig. 6: Architecture of the digital self-calibration circuitry.

The offset register (OFF) and the gain adjustment register (σ) are set during the initial calibration of the WGN-generator using a similar method like the one presented in this paper. Then the offset is subtracted from the calibrating-codes before the next histogram is taken, to ensure a symmetric behavior of the system after the WGN-generator setup. During the initial sampling phase, the working registers (Reg 1 to Reg 4) contain the normalized values of the histogram bins and all following calculations like the subtractions and the scaling can be done within these registers. As soon as the calculations described in part 2 (expressions 2 to 4) are finished, the working registers contain the new calibrating-codes and the calibrating-code registers are updated. Normalization factors stored in a ROM (N1 to N4) are employed, which are accumulated in the working registers every time a sample falls into the corresponding bin. This avoids the multiplication needed to normalize the his-

togram (2). All divisions to scale the calibrating-codes are radix 2 divisions, so they can be performed as a shift operation when the codes are written into the code registers. The 7 bit lines of the code registers are connected at the right position to the bus, so no additional shift unit is needed. The advantage of this system is the ability to perform multi-step calibration because already existing codes are used for new histograms but not affected until they are updated. On-line self-calibration is possible in applications where the ADC is not always in use. During the initial calibration step the calibrating-codes are set to the values of an ideal ADC with the reduced inter-stage gain. The complete digital circuit uses less than 1500 gates and, when laid-out with 0.35um CMOS standard cells and 3 layers of metal, it occupies only 0.49mm^2.

B) The high-amplitude wide-band WGN generator

Fig. 7 shows the schematic of a continuous-time implementation of a WGN generator. A similar one with lower *rms* noise can be found in [7]. Resistors R are used to generate additional wideband thermal-noise that is limited by the bandwidth of the amplifier (opamp) in the form of $V_{Rrms} = \sqrt{4kT \cdot R \cdot BW_{Amp}}$, where k is Boltzmann's constant, T is absolute temperature and BW_{Amp} represents the closed-loop bandwidth of the opamp. The second source of input-referred thermal noise is the opamp itself. For a low-voltage realization a four-stage opamp with a folded-input stage is used. This opamp was designed to have input transistors with quite low transconductance, gm_1, quite-large excess noise factor, γ, and it should be optimized in order to maximize several performance parameters, namely, the bandwidth, the output-referred noise, Vno_{rms}, and the open-loop dc gain, A. To correct the offset voltage and remove most of the flicker noise, stages 2 and 4 have a high-pass response, resulting in a noise bandwidth, after proper compensation within the 70 kHz to 9.5 MHz range.

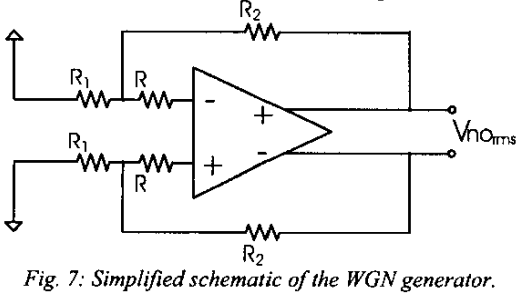

Fig. 7: Simplified schematic of the WGN generator.

Using $R_2 \approx 4000 \cdot R_1$, a closed-loop gain of about 72dB is achieved and the σ of the output-referred noise can be made of the order of several hundreds of milli-volts. Since the opamp is used in a high-gain closed-loop configuration only a simple Miller-compensation is required. In fact, the *rms* output referred-noise is approximately given by

$$Vno_{rms} \approx \left(\frac{R_1+R_2}{R_1+(R_1+R_2)/A}\right) \cdot \sqrt{2 \cdot \left[(4kT \cdot R + \frac{8kT \cdot \gamma}{3 \cdot gm_1}) \cdot BW_{Amp}\right]} \quad (7)$$

Note that the Gaussian noise has not to be necessarily white over the entire bandwidth, like in this noise generator as long as it remains Gaussian. Since the value of Vno_{rms} is highly dependent on the temperature and process variations, a programmable-gain amplifier (PGA) can be used to perform coarse variance adjustments after the WGN generator. The fine trimmings can then be done by digitally adjusting the normalization codes. Using $R = R_2 = 100k\Omega$, $R_1 = 25\Omega$ and an opamp with $gm_1 \approx 0.5mS$ and $\gamma \approx 9$ (single-ended), a differential WGN output with σ = 600 mV can be achieved over a bandwidth of about 9.5 MHz ($\approx F_S/4$) as verified through several electrical AC simulations.

5. Conclusions

A digital-domain self-calibration technique for video-rate pipeline A/D converters based on a white Gaussian-noise input signal was presented together with the design of the required additional building-blocks. It was shown that the overall linearity of the ADC can be highly improved using this technique.

Acknowledgments

The research work that led to this implementation was partially supported by the Portuguese Foundation for Science and Technology (FCT/MCT) under ADOPT (POCTI/ESE/33311/1999), S2A (POCTI/ESE/38689/2001), SAMBA (POCTI/ESE/41804/2001) and SECA (POCTI/ESE/47061/2002) Projects.

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