UNIVERSIDADE NOVA DE LISBOA
Faculdade de Ciências e Tecnologia
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Digitally Programmable Delay-Locked-Loop with Adaptive Charge Pump Current for UWB Radar System

por
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Dissertação apresentada na Faculdade de Ciências e Tecnologia da Universidade Nova de Lisboa para obtenção do grau de Mestre em Engenharia Electrotécnica e Computadores.

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2010

Acknowledgements

It was a long road until the end of this thesis, nevertheless I would never have had finished it without the support, patience and love from my family. A special kiss and hug to my dear sister because she will always be a part of my life.

When I ear the word teacher, the first name that occurs to me is of my advisor, Professor Nuno Paulino whose support and knowledge made this thesis possible. It was a great pleasure having him as my advisor.

For last, but with a great importance in my life, to Cintia the love of my life. Thanks for everything.

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Abstract

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Mestre em Engenharia Electrotécnica e de Computadores

by Bruno Miguel Lopes

The objective of this thesis is to study and design a digitally programmable delay locked loop for a UWB radar sensor in 0.13 μm CMOS technology.. Almost all logic systems have a main clock signal in order to provide a common timing reference for all of the components in the system. In certain cases it is necessary to have rising (or falling) edges at precise time instants, different from the ones in the main clock. To create those new timing edges at the appropriate time it is necessary to use delay circuits or delay lines. In the case of the radar system its necessary to generate a clock signal with a variable delay. This delay is relative to the transmit clock signal and is used to determine the target distance. Traditionally, delay lines are realized using a cascade of delay elements and are typically inserted into a delay-locked-loop (DLL) to guaranty that the delay is not affected by process and temperature variations. A DLL works in a similar way to a Phase Locked Loop (PLL).

In order to facilitate the operation of the radar system, it is important that the delay value should be digitally programmable. To achieve a digitally programmable delay with a large linearity (independent from matching errors), the architecture of the system is constituted by a digital $\Sigma\Delta$ modulator that controls a 1-bit digital to time converter, whose output will be filtered by the DLL, thus producing the delayed clock signal.

The electronic sub-blocks necessary to build this circuit are describe in detail as the proposed architectures. These circuits are implemented using differential clock signals in order to reduce the noise level in the radar system. Design and simulation results of the digitally programmable DLL shows a high output jitter noise for large delays. In order to improve this results a new architecture is proposed. Conventional DLL's have a predefined charge pump current. The new architecture will make the charge pump current variable. Simulations results will show a improved jitter noise and delay error.

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Abbreviations

CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CP	**C**harge **P**ump
DLL	**D**elay **L**ocked **L**oop
FCC	**F**ederal **C**ommunications **C**ommission
GBW	**G**ain **B**and**W**idth Product
NMOS	**N** channel **M**etal-**O**xide-**S**emiconductor
PD	**P**hase **D**etector
PLL	**P**hase **L**ocked **L**oop
PMOS	**P** channel **M**etal-**O**xide-**S**emiconductor
PRF	**P**ulse **R**epetition **F**requency
RADAR	**RA**dio **D**etection **A**nd **R**anging
rms	**r**oot **m**ean **s**quare
$\Sigma\Delta$	**S**igma **D**elta **m**odulator
UWB	**U**ltra **W**ide **B**and
VCDL	**V**oltage **C**ontrolled **D**elay **L**ine
VCO	**V**oltage **C**ontrolled **O**scillator

Dedicated to my Family...

Chapter 1

Introduction

1.1 Background and Motivation

The objective of this thesis is the study and design of a digitally programmable delay locked loop (DLL) for Ultra Wideband (UWB) Radar systems. A DLL is a feedback system, in many ways similar to a phase locked loop (PLL), where it produces a clock signal with a controlled delay.
In 2008, a book [2] was published with a study and design of a low-cost, low power radar sensor, using 0.18 μm CMOS technology. Traditionally radar systems are based on RF signals, the design in this book presented some new ideas and concepts since it was study for UWB signals. A new architecture for a digitally programmable DLL was presented. Based on this architecture, it is the objective of this thesis to present a more detail study and design of this digitally programmable DLL, using 0.13 μm CMOS technology.
There are some conference papers and articles presenting some ideas to design a DLL to achieve many purposes. In this thesis a design of a new technique based on making the charge pump current variable is presented.

1.2 Thesis Organization

The thesis is divided into 5 chapters, including this one. A brief overview of the following chapters is given next.

In chapter 2 a introduction of UWB radar systems is made, starting by explaining the definition of a UWB signal and some differences between a narrow band signal are presented. Follow by some applications of UWB. The second part of this chapter explains the operation of a pulse radar system. Traditionally radar systems uses narrow band signals (sine wave carrier) and using short duration pulses requires a high carrier frequency. Since UWB signals don't have a carrier wave it is possible to have a very short duration pulse resulting in a better radar resolution that can distinguish two targets in a given direction.

Chapter 3 presents an Delay Lock Loop (DLL) overview. The theory of operation of the DLL is explained, with some differences between a DLL and a Phase Lock Loop (PLL) presented. The purpose of the DLL in a radar system is explained as the need for having a digitally programmable DLL also. The architecture of this circuit can have a large programming linearity is presented and analyzed at high level, to meet the required specifications for the radar system. The digitally programmable DLL will generate a clock signal with a programmable delay. This delay is relative to the transmit clock signal and is used to determine the target distance. The electronic sub-blocks necessary to build this circuit are describe in detail as the proposed architectures. These circuits are implemented using differential clock signals in order to reduce the noise level in the radar system.

The fourth chapter describes the design and simulation results for all of the circuits needed to build the digitally programmable DLL. Simulation results of this circuit shows a high output jitter for large delays. A new architecture is proposed to deal with this problem, making the charge pump current variable. This solution will show improvements in the operation of the circuit.

The thesis ends with a final chapter dedicated to some final conclusions and further research suggestions.

1.3 Contributions

This thesis presents a digitally programmable delay architecture based on the one describe in [2]. This architecture allows to obtain a large programming resolution, with a small delay step and is less sensitive to mismatch errors. The architecture is based in a digital sigma delta modulator controlling a 1-bit digital to time converter whose output is filtered by a delay lock loop (DLL). Conventional DLL's have a predefined charge pump current. This thesis presents a new technique based on an adaptive charge pump current.

Although the circuit was not tested, simulations showed a very promising results with low power consumption.

Chapter 2

UWB Systems

2.1 Introduction

Alternately referred to as impulse, baseband or zero-carrier technology, Ultra Wideband (UWB) systems transmit signals across a much wider frequency than conventional systems [3]. There are several signals that can be classified as UWB signals, these are typically constituted by a repetitive sequence of short pulses with a certain repetition frequency (PRF). The amount of spectrum occupied by a UWB signal, i.e. the bandwidth of the UWB signal (fractional bandwidth B_{frac}) is at least 25% of the center frequency. A narrow band signal fractional bandwidth is inferior to 10%. For example, a UWB signal centered at 2 GHz would have a minimum bandwidth of 500 MHz and the minimum bandwidth of a UWB signal centered at 4 GHz would be 1 GHz. The formula proposed by the Federal Communications Commission (FCC) [4], that defines the B_{frac} is:

$$B_{frac} = \frac{2 \cdot (f_H - f_L)}{f_H - f_L} \tag{2.1}$$

where f_H is the upper frequency of the -10 dB emission point and f_L is the lower frequency of the -10 dB emission point. The center frequency of the transmission was defined as the average of the upper and lower -10 dB points and in given by the next expression.

$$f_c = \frac{f_H + f_L}{2} \tag{2.2}$$

Fig. 2.1 shows a comparison between the UWB fractional bandwidth and the narrow band systems.

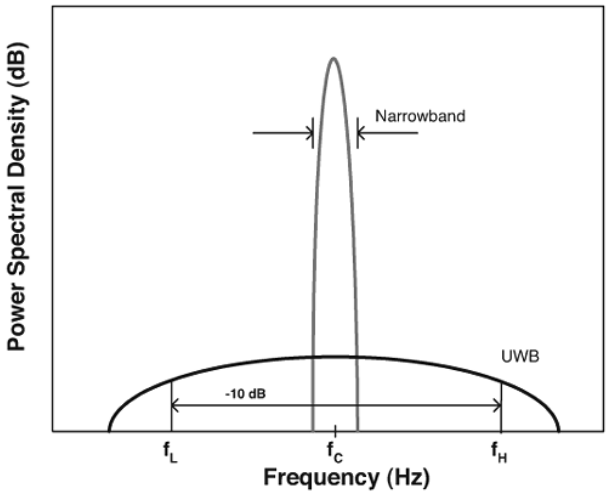

FIGURE 2.1: UWB Fractional bandwidth compared with narrow band systems [1].

The most common technique for generating a UWB signal is to transmit pulses with durations less than 1 nanosecond. Because of the narrow or short duration of the pulses, that results in a large transmission bandwidth, UWB devices can operate using spectrum occupied by existing narrow band radio services without causing interference, thereby permitting scare spectrum resources to be used more efficiently [2]. Nevertheless any electronic or electric equipment always emits unwanted radiation that can interfere with narrow band radio systems, a example of this is digital systems such as computers. Therefore every electronic and electrical device is required to limit the power of these unwanted emissions level. The transmitted power of UWB devices is controlled by the Federal Communications Commission (FCC), so that narrow band systems are affected from UWB signals only at a negligible level [4].

UWB has several applications all the way from wireless communications to RADAR[1] imaging, and vehicular radar. The ultra wide bandwidth and hence the wide variety of material penetration capabilities allows UWB to be used for radar imaging systems, including ground penetration radars, wall radar imaging, through-wall radar imaging, surveillance systems, and medical imaging. Images within or behind obstructed objects can be obtained with a high resolution using UWB. Similarly, the excellent time resolution and accurate ranging capability of UWB can be used for vehicular radar systems for collision avoidance, guided parking, etc. Positioning location and relative positioning

[1]RADAR stands for Radio Detection And Ranging

capabilities of UWB systems are other great applications that have recently received significant attention [5].

2.2 UWB RADAR Systems

The operation of a a pulsed radar system is very simple [6], an electromagnetic signal (pulse) is radiated, this signal travels at the speed of light (c) (assuming that the signal propagates in space), when the signal encounters an object (target) part of its energy is reflected back (re-radiated), therefore creating an echo, the echo signal travels back at the speed of light to the point of the radiation of the original signal. The radar can use a single antenna for transmission and reception of the pulse or two separate antennas. The radar operation principle is showed in Fig. 2.2.

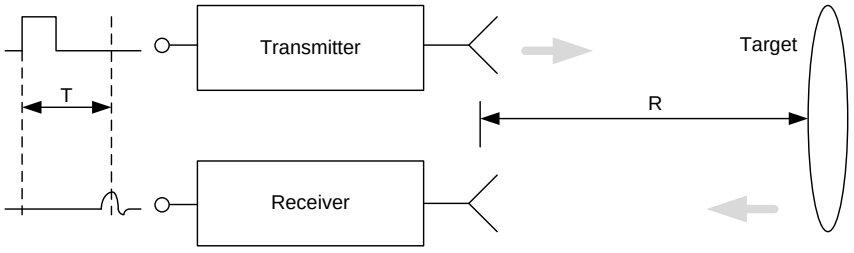

FIGURE 2.2: Simple diagram of the RADAR operation principle.

The time interval (T) between the transmission of the signal and arrival of the echo can be measured, making the distance (or range) (R) at which the target is located possible to calculate using the following formula

$$R = \frac{c \cdot T}{2} \tag{2.3}$$

The radar systems that this thesis is based on, is a low-cost, low power radar sensor. This radar sensor can have several applications such as a proximity sensor (detects any intruders that enter a predefined perimeter), a motion detector (detects motion of objects), a ground penetrating radar (detects objects buried at a small depth in some types of soil) and 2D/3D imaging (with more than one or two sensors and using signal processing techniques it is possible to obtain a 2D/3D image).

Since this radar sensor as several applications the time interval between the transmitted signals is an important issue to discuss. If the radar sensor is used as a proximity sensor configuration there is no problem if two echoes are received at the same time, but if the

sensor is used to locate two different objects, then receiving two echoes at the same time will not be adequate. The time interval between two transmitted signal must be large enough so that the first echo will not be confused with the echo received from the second transmission. The time interval between two pulses must increase as the potential targets are located further away. The maximum Pulse Repetition Frequency (PRF) of a radar system is dependent on the maximum distance that a target can be detected. If, for example, the maximum range a target might be detected is 300 Km, the maximum value for the PRF would be limited to 500 Hz, but if the maximum range is 30 m, the maximum PRF value can be as high as 5 MHz [2]. The maximum range of the radar (R_{max}) is given by

$$R_{max} = \frac{c \cdot T_{PRF}}{2} \tag{2.4}$$

The PRF value is usually also selected so that echoes from outside the maximum radar range have an amplitude smaller than the minimum detectable amplitude by the radar receiver.

The echoes received by the radar receiver can have different shapes and longer duration than the transmitted pulse depending on the target shape and size. Considering this, it is possible that two echoes can be interpreted as one (the two echoes combined) in the radar receiver. Any two targets separated by a radial distance from the radar inferior to $c.\tau$ (where τ is the pulse width) produce a combined echo signal that can be interpreted as the one created by a single target [2]. This means that the value of the pulse width will determine the resolution that the radar can distinguish two targets in a given direction.
Traditional radar systems uses narrow band signal (sine wave carrier) and using short duration pulses requires a high carrier frequency. If a pulse signal is used to modulate a sine wave carrier, the resulting signal will have approximately the same bandwidth as the pulse signal centered around the carrier frequency. This is one of the advantages of the UWB signals, since they don't have a carrier wave it is possible to have small pulse duration.
Using UWB signals has also the advantage of producing an echo signal with more information about the target. Due to the large bandwidth occupied by this type of signal, several resonant frequencies of the target can be activated. The fact that the pulse width is very small, can also be used to determine the shape of targets larger than $c.\tau$, since multiple echoes can be obtained from such a target. This extra information requires complex signal processing techniques and depending on the target and on the environment

conditions might not be possible [2].

One of the disadvantages of using UWB signals compared to the narrow band signals is the fact that the amount of noise generated by a circuit is proportional to its bandwidth, the larger the bandwidth the larger the noise generated by the circuit (assuming constant impedance). Therefore UWB circuits have an inherent high noise level and thus a low sensitivity. This is one of the reasons for a UWB radar system to have a short range when compared to a traditional radar system. UWB radar systems are more suited for a short range high resolution applications, where the lower cost of a CMOS UWB system (compared to a narrow band radar system) is an advantage [7].

Chapter 3

Delay-Lock Loop (DLL)

3.1 Introduction

Almost all logic systems have a main clock signal in order to provide a common timing reference for all of the components in the system. In certain cases it is necessary to have rising (or falling) edges at a precise time instants, different from the ones in the main clock. To create those new timing edges at the appropriate times it is necessary to use delay circuits or delay lines [8].
In the case of the architecture of the radar system its necessary to generate a clock signal with a variable delay. This delay is relative to the transmit clock signal and is used to determine the target distance. Traditionally, delay lines are realized using a cascade of delay elements and are typically inserted into a delay-locked-loop (DLL) to guaranty that the delay is not affected by process and temperature variations [2].
A Delay Lock Loop (DLL) is a feedback system, where the delay produced by a voltage controlled delay line (VCDL) into a clock signal, is adjusted until is equal to one or more periods of the reference clock [8], [9], [2].

The DLL, as shown in Fig. 3.1, works in a similar way to a Phase Locked Loop (PLL). Instead of having a voltage controlled oscillator (VCO), the DLL has a voltage controlled delay line (VCDL) that does not suffer from jitter accumulation, since normally is not used in a closed loop configuration as the VCO.
The DLL loop compares the phase (delay) of the reference clock with the phase of the delayed clock using a phase detector (PD). The output of the charge pump (CP), goes through a low-pass filter to attenuate the excess jitter noise from the clock signals, and

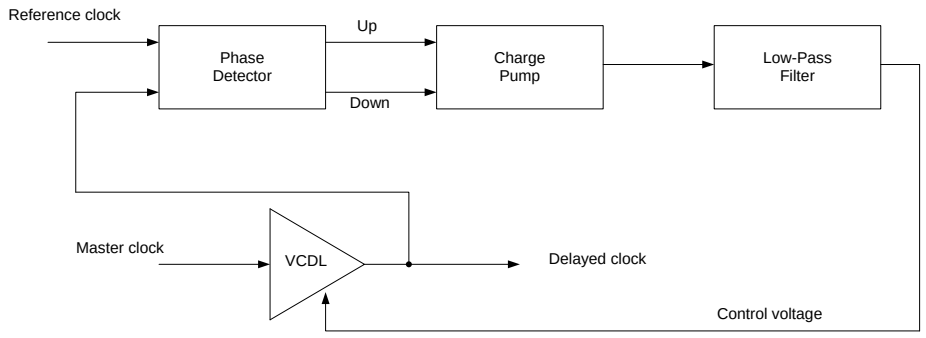

FIGURE 3.1: Architecture of the Delay Lock Loop.

the resulting voltage is used to control the delay value in the voltage controlled delay line (VCDL) until the rising (or the falling) edges of both clocks coincide. Since the output of the DLL is just a delay version of the master clock, the output frequency value is always the same as the input frequency.

3.2 Digitally Programmable DLL

In order to facilitate the operation of the radar system, it is important that the delay value should be digitally programmable. The maximum delay of the digitally programmable delay must be equal to 100 ns, corresponding to a radar range of 15 m, and a delay programming step smaller than 0.2 ns, corresponding to a ranging resolution smaller than 3 cm. If a large maximum delay and a small delay step is required, the delay line will be composed by a large number of delay elements [10], [11], each one having a delay equal to the delay step, in this case this approach would result in at least 256 delay elements (8-bit resolution) [2]. This would result in a large power dissipation and in a large area. Also this type of delay line suffers from element mismatch, resulting in limited delay resolution [12]. The digitally programmable delay will make each programming code correspond to a precise distance, if the delay resolution is limited then a programming code will not correspond to a precise distance. For these reasons the architecture for the digitally programmable DLL [13], will be as the one depicted in Fig. 3.2 whose resolution is not affected by element mismatch and is only limited by the response time to a new programming code.

To guaranty the maximum delay and the delay programming step the programmable delay must have a programming resolution of 9 bits [2].

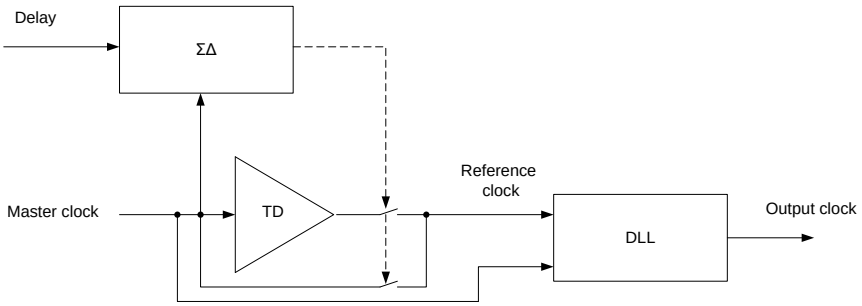

FIGURE 3.2: Architecture of the digitally programmable DLL.

In order to achieve a digitally programmable delay with a large linearity (independent from matching errors), the architecture of the system is constituted by a digital ΣΔ modulator that controls a 1-bit digital to time converter, whose output will be filtered by the DLL, thus producing the delayed clock signal [2]. The digital code apply to the digital ΣΔ will control the two switches that generate the reference clock. This clock is created with the help of the master clock and a delayed version of this same clock and will have an average delay value corresponding to the digital code. The delayed clock was a fixed delay equal to T_D. To avoid spikes in the reference clock, the maximum delay T_D should be inferior to half period of the master clock. The reference clock will have a large jitter noise generated by the switching sequence that will be mostly filtered by the low-pass characteristic of the DLL.

The minimum order of the DLL is related to the order of the ΣΔ, however the DLL must be a second-order system because of closed loop stability problems. The order of the ΣΔ modulator can be determined calculating the rms value of the jitter noise at the output of the DLL for different orders of ΣΔ modulators [2]. According to the graph in Fig. 3.3, a second order modulator produces the best resolution for a given closed loop pole frequency (f_p) value in the case of a second order DLL.

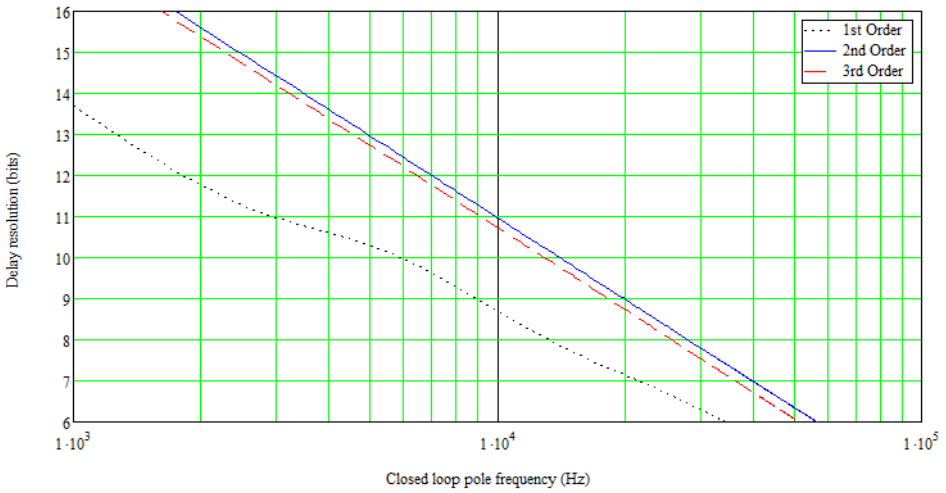

FIGURE 3.3: System resolution (in bits) of the DLL for different closed loop frequencies and a $\Sigma\Delta$ modulator order of 1, 2 and 3.

This graph was calculated considering that $T_D = 100$ ns, $F_{clk} = 2.5$ MHz and that the loop transfer function is a second order low-pass filter with a complex pole frequency given by

$$H_{DLL}(s) = \frac{W_p^2}{s^2 + \frac{W_p}{Q_p} \cdot s + W_p^2} \tag{3.1}$$

The value of the closed loop pole frequency can be obtain considering that the programming resolution must be equal to 9 bits, resulting in $f_p \approx 19.8$ KHz corresponding to an *rms* jitter of 56.03 ps. The closed loop pole quality factor Q_p does not affect this graph as long its value is between 0.5 and 1.5 as the Fig. 3.4 shows.

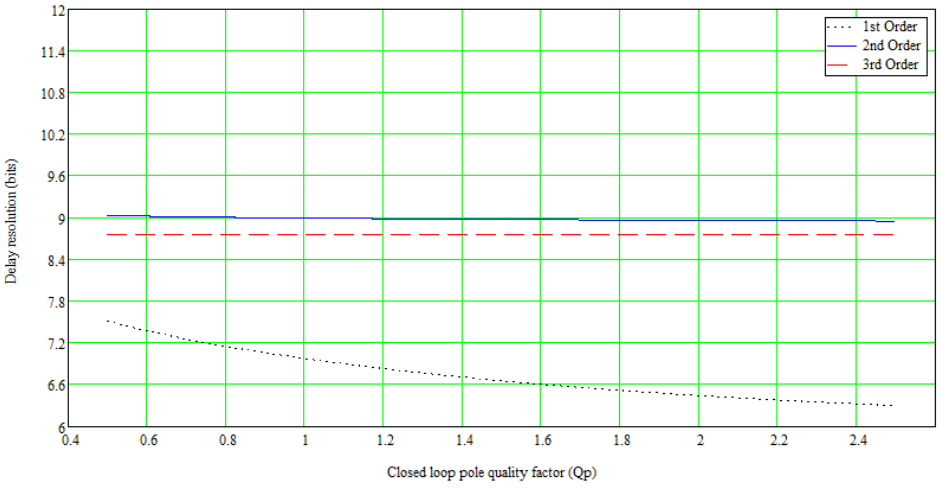

FIGURE 3.4: System resolution (in bits) of the DLL for different closed loop quality factor and a $\Sigma\Delta$ modulator order of 1, 2 and 3.

The DLL closed loop transfer function is obtained by a discrete time analysis resulting in [2]:

$$H_{DLL}(z) = \frac{G \cdot I_P \cdot K_{PD} \cdot K_{VCDL} \cdot T_{CLK} \cdot z}{G \cdot I_P \cdot K_{PD} \cdot K_{VCDL} \cdot T_{CLK} + C_1 \cdot \tau_{RC} \cdot (z-1) \cdot (z-1+\frac{T_{CLK}}{\tau_{RC}})} \tag{3.2}$$

where G is a gain in the filter, I_P is the charge pump current, K_{PD} is the phase detector gain, K_{VCDL} is the gain of the VCDL, C_1 is the output capacitance of the charge pump, τ_{RC} is the time constant of a first order filter introduced in the loop in order to obtain a second order transfer function. Evaluating this equation using $z = e^{j \cdot 2 \cdot \pi \cdot f} \approx 1 + j \cdot 2 \cdot \pi \cdot f$ it is possible to obtain an approximated continuous time transfer function. From this transfer function it is possible to obtain expressions for the closed loop pole frequency and quality factor:

$$f_p = \frac{1}{2\pi} \sqrt{K_{PD} \cdot K_{VCDL} \cdot \frac{I_P}{C_1} \cdot \frac{1}{\tau_{RC}} \cdot F_{clk}} \tag{3.3}$$

$$Q_p = \frac{\sqrt{K_{PD} \cdot K_{VCDL} \cdot \frac{I_P}{C_1} \cdot \frac{1}{\tau_{RC}} \cdot F_{clk}}}{\frac{1}{\tau_{RC}} + K_{PD} \cdot K_{VCDL} \cdot \frac{I_P}{C_1} \cdot \frac{1}{\tau_{RC}}} \tag{3.4}$$

These expressions are used to design the DLL loop in order to have the desired f_p and Q_p values. The main circuit parameters used in this design are $\frac{I_P}{C_1}$ and τ_{RC}. The other parameters in the circuit do not allow for much design freedom since they are dependent on the technology and on power dissipation constraints. In order to calculate this parameters, the frequency response of the DLL for the discrete transfer function (Eq. 3.2) and the second order low-pass filter transfer function (Eq. 3.1) were simulated as showed next.

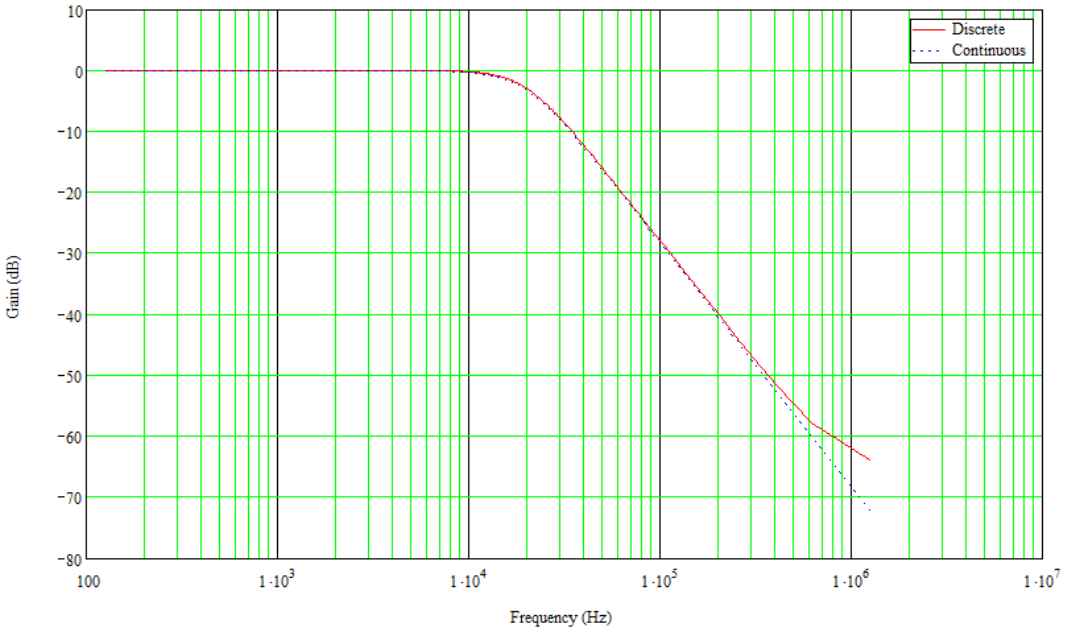

FIGURE 3.5: DLL closed-loop frequency response.

According to the graph, the attenuation of the DLL discrete transfer function is smaller than the the continuous one at high frequencies, causing an increase in the output jitter noise since the input jitter noise is located mainly at high frequencies [2]. Therefore the programing resolution will be smaller than the values shown in Fig. 3.3 and consequently the value of the closed loop pole frequency (f_p) will be smaller than the predicted 19.8 KHz. In fact, after simulation the discrete transfer function with the predicted f_p, a rms jitter value of 73.39 ps and a resolution of 8 bits is obtained. To achieve the 9 bits resolution, simulations results in a f_p value of 16 KΩ and a Q_p value of 0.7 corresponding to a rms jitter value of 47.69 ps (smaller than the predicted value of 56.03 ps). This results correspond to $\frac{I_P}{C_1} = 66.78$ volt/ms and $\tau_{RC} = 7.16$ μs. The transient behavior of the output delay of the system was simulated with a 75 ns step applied to the control signal and the system response is compared to the transient behavior of the ideal second order system. The results are depicted in the next figure.

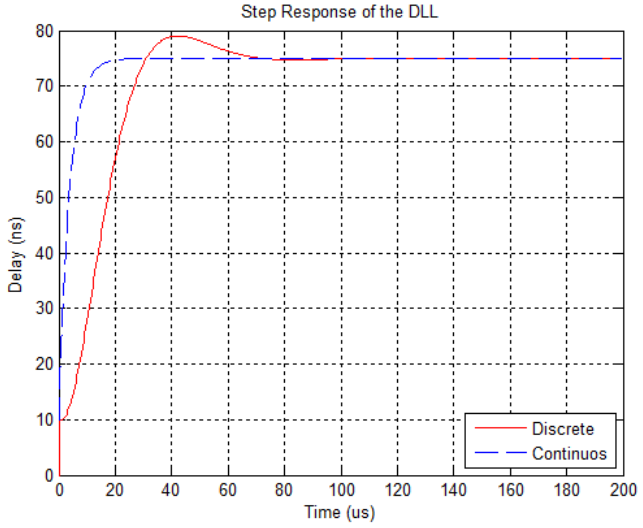

FIGURE 3.6: Step response of the DLL.

The real delay, the rms and peak-to-peak value of the jitter noise are measured by simulating the DLL discrete model with different delays selected. The results are depicted in the next figure.

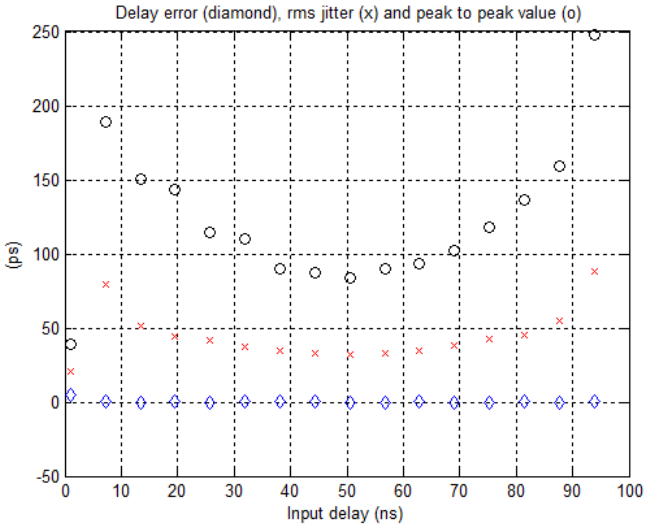

FIGURE 3.7: Simulated output delay error, rms jitter value and peak-to-peak jitter.

From this results it is possible to confirm the value of the *rms* jitter is approx. 47 ps (value calculated above), but for small and large delay values this value will increase. In section 4.5 the reason for this increase will be discussed.

3.3 DLL Constituting Blocks

3.3.1 Phase Detector

A phase detector (PD) is a circuit whose average output, $\overline{V_{out}}$, is linearly proportional to the phase difference, $\Delta\phi$, between its two inputs [14]. The typical example of a PD is the exclusive OR (XOR) gate. As the phase difference between the inputs varies so does the width of the output pulses, thereby providing a dc level proportional to $\Delta\phi$. The XOR phase detector is not suitable to this design since it detects phase differences in both rising and edges of the input signals. Instead a PD architecture depicted in Fig. 3.8 is selected. This PD is a digital state machine with 3 states, whose state transitions are determined by the rising (or falling) edges of the input clock signals [15]. The schematic of the PD is shown next

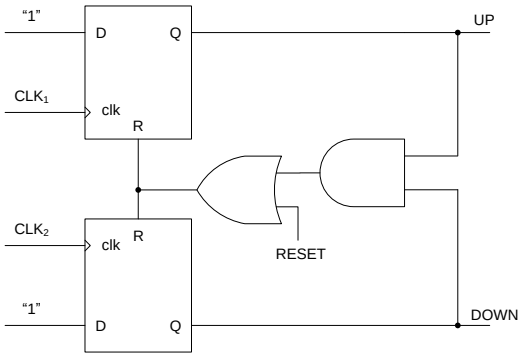

FIGURE 3.8: Schematic of the phase detector.

The 3 states correspond to the clock signal (CLK_1) being "ahead", being the same or being "behind" of the clock signal (CLK_2). Initially the PD is in inactive state, both UP and DOWN signals are OFF, if the rising edges of CLK_1 occur before the CLK_2, then the PD will activate the UP signal until a rising edge of CLK_2 occurs, resulting in the activation of the DOWN signal that will activate the RESET signals, returning to the inactive state. The time interval when the UP signals is ON measures the phase difference between the two input clock signals. The third state is the other way around, when the rising edge of CLK_2 occurs first and the DOWN signal is activated. The maximum amount of delay between the two clock signals with the same period (T_{clk}) is $\pm T_{clk}$. When the PD "awakes" it can be in any of the 3 states, which can be a problem. Because the loop gain of the delay locked loop can be positive or negative for the same delay between the two input clock signals. The solution for this problem is to reset the PD to the inactive

state at start-up, this is implemented with an OR gate and a new reset signal (generated at start-up), as shown in Fig. 3.8.
In this circuit, the minimum phase difference detected, is limited by the speed of the flip-flops and the AND gate. If the rising edge of the clock signals is very close, the RESET signal starts to activate before the outputs of the flip-flops have completely settled at the ON value, resulting that the outputs of the flip-flops resets before stabilizing. For very small phase differences this process causes the UP and DOWN signals not to activate at all and the phase difference is not detected. The solution to this problem is very simple [16] if a small delay is added to reset path, the UP and DOWN signals are always activated (even for zero phase difference) during a minimum time equal to the added delay. Now even a very small phase difference between the input signals is capable of generating a difference between the ON time of the UP and DOWN signals.

3.3.2 Charge Pump

To fully understand the operation of the charge pump (CP) it is better to first describe the operation of a single ended CP as show in Fig. 3.9 [17].

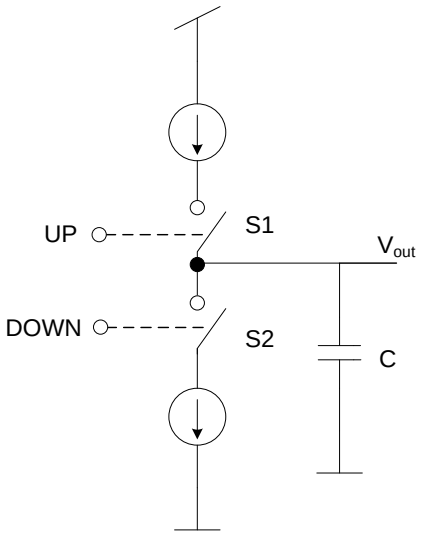

FIGURE 3.9: Schematic of single ended charge pump.

The CP is constituted by two current sources, two switches and a output capacitor (C). Both the current sources and the switches are made with NMOS and PMOS transistors. When the UP control signal is active the switch S1 is turned ON and the PMOS current

source will supply current to the output capacitor increasing the output voltage. When the DOWN control signal is active the switch S2 is turned ON and the NMOS current source will sink current from the capacitor decreasing the output voltage. Since the behavior of PMOS and NMOS transistors are different, due to matching errors, the supply current and the sink current will not be equal. This is one the biggest problems in a singled ended CP.

The CP architecture will be fully differential, as show in Fig. 3.10 since has several advantages over the conventional single-ended charge pump proposed in [18], [19], [20]. The output current will have symmetrical values for the up and down current and the output voltage is more immune to common mode noise [2]. The main disadvantage of the differential CP is the output resistance, since even when the charge pump is OFF, the current sources remain connected to the output node. This problem does not occur in the single ended architecture where the output resistance is almost infinite in the OFF state. This subject will be addressed later in the design chapter.

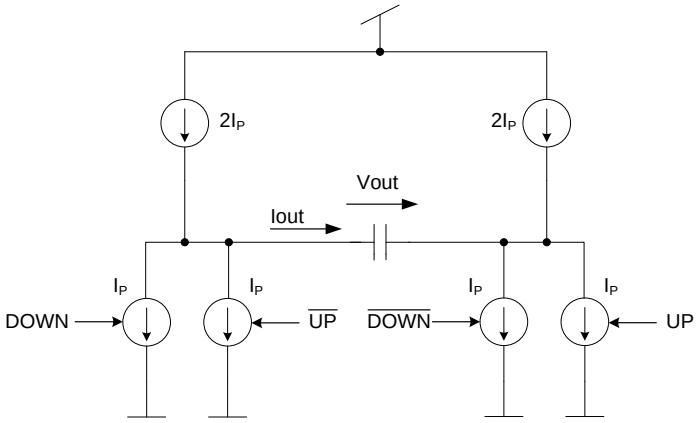

FIGURE 3.10: Differential charge pump architecture.

Up	Down	Iout
0	0	0
0	1	-I_P
1	0	+I_P
1	1	0

TABLE 3.1: Charge Pump operation table.

This CP is design to have a high output resistance, this means that any mismatch between the current values of the NMOS and PMOS current sources would result in the common mode output voltage saturating in either V_{DD} or GND [2]. To avoid this situation it is necessary to adjust the current level of the PMOS to match the NMOS current sources. This is done using the common mode feedback principle depicted next is Fig. 3.11.

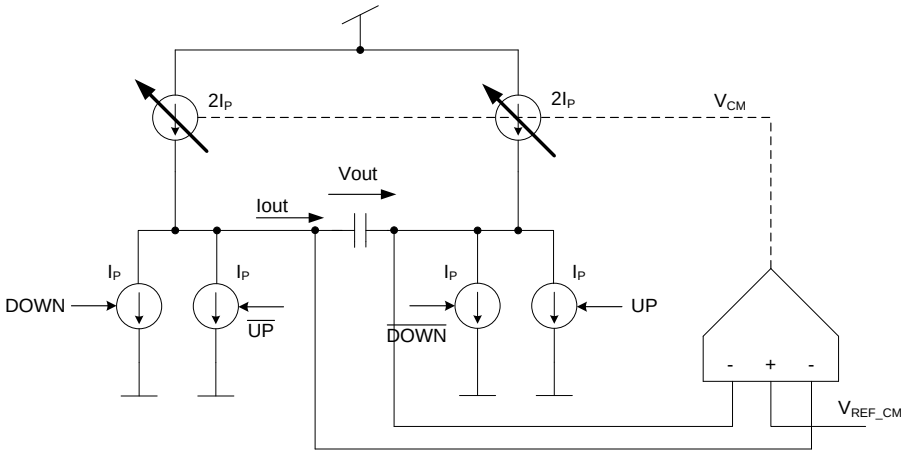

FIGURE 3.11: Common mode feedback circuit scheme.

The common mode voltage is adjusted comparing the output common voltage with the desired common mode reference voltage and then using this error voltage adjust the current of the PMOS current sources. This operation is equivalent to

$$V_{o\_CM} = \left(\frac{V_{op} + V_{om}}{2} - V_{REF\_CM} \right) \cdot G = \left(\frac{V_{op} - V_{REF\_CM}}{2} + \frac{V_{om} - V_{REF\_CM}}{2} \right) \cdot G \tag{3.5}$$

where G is the common voltage gain of the CP.

3.3.3 Loop Filter

The output of the CP is connected to a capacitor, resulting in the creation of a pole close to DC. The voltage across this capacitor increases or decreases according to the phase detector activity. An extra pole is needed in the loop in order to obtain a second order system, this pole is created in the differential to single ended converter circuit, by adding an extra capacitor to the output resistor. This circuit converts the differential output voltage of the charge pump into a single ended voltage used to control the voltage controlled delay line VCDL, and it is implemented as a differential pair with a current mirror load, that drives the output resistor, thus producing a single-ended voltage.

3.3.4 Voltage Control Delay Line

The voltage controlled delay line (VCDL) must be able to produce a variable delay with a maximum value of 100 ns. Since only one delay element is unable to accomplish this task, a cascade of delay elements will be used. For a maximum delay value of 100 ns it will be necessary to use three variable delay elements followed by three fast buffers. The purpose of these last three buffers is to recover the rise and fall times of the clock signal after the delay is introduced. The delay of this delay line is three times the delay of a single variable delay buffer plus the delay of the fast buffer at the output. The architecture is depicted in Fig. 3.12.

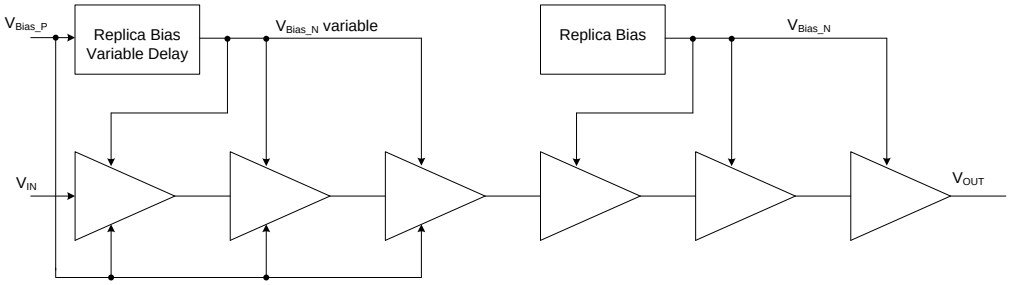

FIGURE 3.12: Architecture of the voltage controlled delay line (VCDL).

Chapter 4

Design and Simulation Results

4.1 Differential Buffer

This block is responsible for processing differential digital signals and it is composed by a differential pair and a resistive load, as shown in Fig. 4.1. The circuit, as the name

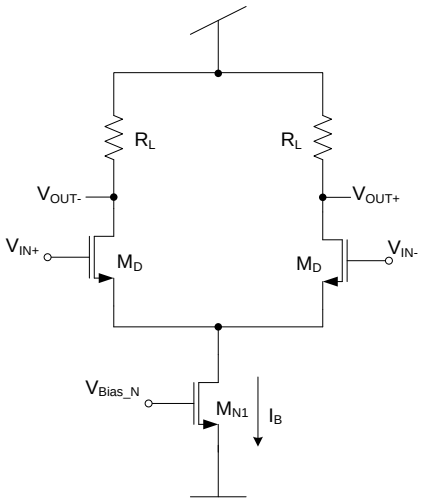

FIGURE 4.1: Differential buffer schematic.

indicates, operates with differential digital signals, i.e., signals that have only two valid voltage levels, each representing a digital value. By applying a differential signal to the input, the differential pair will be in one of two operations regions, when both M_D transistors are ON (linear region), and when one of the transistors is ON and the other OFF (saturation region), producing two differential output voltage levels. A complete study of this two operations regions in shown in [2]. These voltage levels will have maximum

value amplitude limited by the power supply (V_{DD}), the V_{dsat} voltage of the transistor M_{N1} and a safety margin voltage (V_{tol})(approx. 120 mV) to guaranty that transistor M_{N1} is in the saturation region. The output voltage swing (V_{swing}) is determined by the buffer bias current (I_B) and by the load resistance value (R_L) , using Ohm´s law

$$V_{swing} = R_L \times I_B \tag{4.1}$$

For the case of a bias current value of 100 μA and in order to obtain a voltage swing of 400 mV at the output, results in $R_L = 4$ KΩ. A voltage swing of 400 mV requires that

$$V_{DD} - V_{dsat}(M_{N1}) - V_{tol} \geq V_{swing} \tag{4.2}$$

where

$$V_{dsat}(M_{N1}) \leq 680mV \tag{4.3}$$

Transistor M_{N1} V_{dsat} voltage value is set to 400 mV and the channel lenght is set to 1.5 μm. The V_{dsat} voltage of the differential pair, M_D, is set to 80 mV, a value small enough to guaranty the saturation of the transistors by the input signal and the channel length is set to 120 nm. In Fig. 4.2, the simulation results of the design described above are shown.

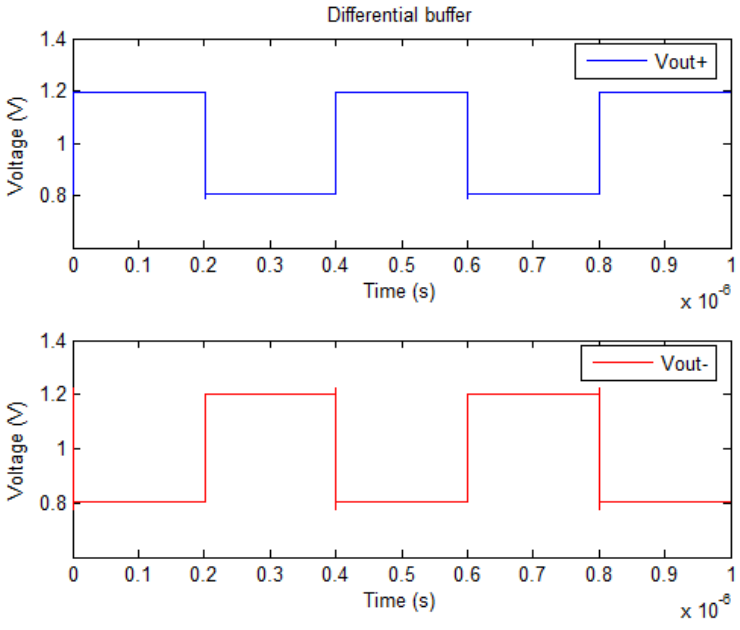

FIGURE 4.2: Plot of the buffer output voltage for a load resistor value equal to 4 KΩ.

	V_{dsat} (mV)	L(μm)	W(μm)
M_D	80	0.12	7.5
M_{N1}	400	1.5	3.7

TABLE 4.1: Buffer design summary for a bias current equal to 100 μA.

4.2 Replica Bias

In order to guaranty that the amplitude of the output voltage (V_{swing}) of the differential buffer will be constant, it is necessary to use a replica bias circuit to compensate the variation of the value of the resistance output. This value can vary with process and temperature up to 30% of its nominal value. The replica bias principle will be to adjust the bias current (I_B), by comparing the output voltage of a replica of the buffer circuit to the desired value (V_{ref}), using an amplifier. In fact only half of the buffer circuit is needed since one of the outputs is V_{DD}.
Therefore V_{ref} = V_{DD} - V_{swing}. The amplifier output voltage (V_{Bias_N}) determines the value of the I_B current through transistor M_{N1}. This bias current of this half-buffer can be mirrored to all the buffer circuits [21],[22]. The principle is shown in Fig. 4.3.

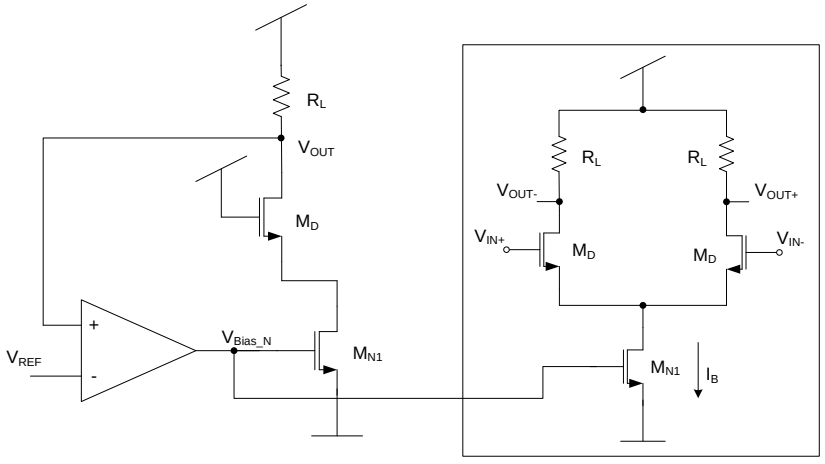

FIGURE 4.3: Replica bias principle.

The relative error between the V_{ref} voltage and the V_{out} voltage depends on the feedback loop gain of the replica bias and is given by

$$\frac{V_{out}}{V_{ref}} = \frac{1}{1 + A \cdot gm_{MN1} \cdot R_L} \tag{4.4}$$

where A is the amplifier gain. This expression shows that a loop gain value equal to 40 (32 dB) produces a voltage error inferior to 2.5%. As show in Fig. 4.4, the amplifier is a

single stage amplifier because using a low loop gain value (within the limits of the gain specification) improves the phase margin of the loop.

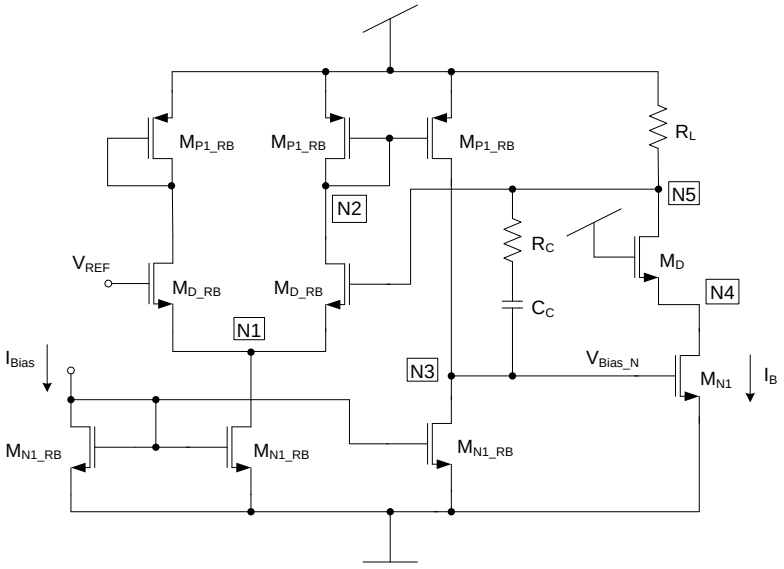

FIGURE 4.4: Replica bias circuit schematic.

The loop gain is given by

$$G_{loop} \approx \frac{gm_{D\_RB} \cdot gm_{N1} \cdot R_L}{gds_{P1\_RB} + gds_{N1\_RB}} \tag{4.5}$$

As show in Fig. 4.4 the loop has a total of 5 poles, these are associated to the 5 nodes of the circuit in the signal path (N1 to N5). The dominant pole of the loop is located, by design, at node N3, its approximate expression can be obtained using Miller theorem and is given by

$$p_3 \approx \frac{gds_{P1\_RB} + gds_{N1\_RB}}{C_C \cdot (1 + gm_{N1} \cdot R_L)} \tag{4.6}$$

The gain bandwidth product (GBW) is given by (assuming a phase margin larger than 60°)

$$GBW = p_3 \cdot G_{loop} \approx \frac{gm_{D\_RB}}{C_C} \tag{4.7}$$

The phase margin of the loop is determined by all the 5 poles of the circuit and by the 2 zeros, one zero created by the C_{gs} capacitance in the differential pair formed by the M_{D_RB} transistors and the other zero is associated to the compensation resistor R_C. The phase margin is the difference between 180°and the phase gain at the GBW frequency

and is calculated using

$$PM = 180^\circ - \left[\sum \arctan(\frac{GBW}{-p_i}) - \sum \arctan(\frac{GBW}{-z_i})\right] \tag{4.8}$$

The remaining poles are given by

$$p_1 \approx \frac{-2 \cdot gm_{D\_RB}}{2 \cdot Cgs_{D\_RB} + C_{p1}} \tag{4.9}$$

$$p_2 \approx \frac{-gm_{P1\_RB}}{2 \cdot Cgs_{P1\_RB} + C_{p2}} \tag{4.10}$$

$$p_4 \approx \frac{-gm_D}{2 \cdot Cgs_D + C_{p4}} \tag{4.11}$$

$$p_5 \approx \frac{-gm_{N1} \cdot C_C}{C_{p3} \cdot C_{p5} + C_C \cdot C_{p3} + C_C \cdot C_{p5}} \tag{4.12}$$

The value of C_{p5} is small compared to the C_{p3} value, it is approximately equal to $C_{p3} \approx M \cdot Cgs_{N1}$, since the transistors inside the buffers controlled by the replica bias have the same V_{dsat} voltages as the transistors of the half buffer. Under these condition the p_5 expression can be further simplified to

$$p_5 \approx \frac{V_{dsat\_N1}}{M \cdot L_{N1}^2} \cdot K \tag{4.13}$$

where K is technology dependent parameter.

As in any feedback loop, the replica bias amplifier must be designed to assure that the loop is unconditionally stable. Therefore the specifications for this circuit are a loop gain larger than 32 dB, since the control voltage V_{Bias_N} is essentially a DC signal, a GBW larger than 100 kHz is enough, and phase margin larger than 60°.

Inside the half-buffer the transistors have the same V_{dsat} voltages and channel lengths as the transistors inside the differential buffer. To reduce the parasitic capacitance the channel length of transistors M_{D_RB} should be small, therefore a value of 0.5 μm and a V_{dsat} value of 100 mV are defined to obtain the largest possible gain and GBW values for a given current value. The V_{dsat} values for the transistors M_{N1_RB} and M_{P1_RB} are selected to be 300 mV to reduce the parasitic capacitance. The channel length of M_{N1_RB}

is set to 2 μm to improve the gain and for the M_{P1_RB} is set to 2 μm. The values of the resistance and capacitor are selected together using AC simulations resulting in $C_C = 3$ ρF and $R_C = 4$ kΩ. After the previous design process the circuit design goals were obtain and are shown next in table 4.2.

	Design Goals	Typical Simulation Results
Gain(dB)	32	44.2
GBW(MHz)	0.1	16.7
Phase(°)	60	81.5

TABLE 4.2: Replica bias simulation results.

Since the simulations results can vary with temperature and supply voltage values, a corners analysis was made to assure that the loop is unconditionally stable.

Supply Voltage (V)	Section	Temperature (°C)	Gain (dB)	GWB (MHz)	PM (°)
Vdd = 1.2	Slow	0	42.9	19.4	73.1
		80	40.6	14.9	65.4
	Fast	0	45.8	17.2	98.3
		80	44.5	13.6	86.8
Vdd = 1.08	Slow	0	41.4	18.0	69.1
		80	39.1	13.7	61.9
	Fast	0	44.0	16.1	92.8
		80	42.0	12.6	80.8
Vdd = 1.3	Slow	0	43.8	20.1	75.5
		80	41.5	15.3	67.7
	Fast	0	46.6	17.8	100.9
		80	45.6	14.1	90.3

TABLE 4.3: Corners analysis simulation results confirming the stability of the loop.

This results showed that the circuit design parameters are well adjusted and the loop is unconditionally stable.

	V_{dsat}(mV)	L(μm)	W(μm)
M_{D_RB}	100	0.5	10
M_{N1_RB}	300	2	8.8
M_{P1_RB}	300	2	20

TABLE 4.4: Replica bias design summary.

4.3 Differential Buffer with Variable Delay

This circuit is used in the voltage controlled delay line (VCDL) to help produce a maximum value of 100 μs to accomplish the radar system specifications. The differential buffer in Fig. 4.1 can produce a variable delay [9], by changing the load resistance of the buffer using MOS transistors in the linear region. The differential buffer circuit with symmetric loads [9] is show in Fig. 4.5.

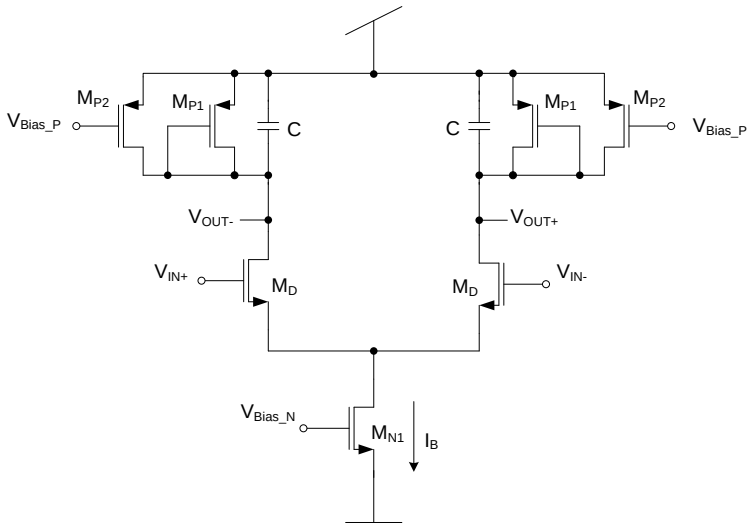

FIGURE 4.5: Schematic of the differential buffer with symmetric loads.

A PMOS transistor is in the linear region when $V_{SD} < V_{SG} - |V_T|$, when this condition applies the drain current is given by

$$I_D = \beta \cdot \left[(V_{SG} - |V_T|) \cdot V_{SD} - \frac{V_{SD}^2}{2} \right] \tag{4.14}$$

where $\beta = K_p \cdot \frac{W}{L}$ and K_p is the transistor transconductance which depends on the technology and varies with process and temperature. The drain resistance of the transistor is calculated using

$$r_{sd} = \left(\frac{dI_D}{dV_{SD}} \right)^{-1} = \frac{1}{\beta \cdot [(V_{SG} - |V_T|) - V_{SD}]} \tag{4.15}$$

The expression shows that the resulting resistor has a non-linear dependence on the V_{SD} voltage. The V_{SG} voltage should be as large as possible, compared to the maximum V_{SD} voltage, to reduce this non-linear behavior and to guaranty that the transistor is in the

linear region.
The drain current of the M_{P1} transistor is given by

$$I_D = \beta \cdot \left[(\frac{V_{SD}}{2} - |V_T|) \right] \cdot V_{SD} \tag{4.16}$$

The drain resistance of M_{P2} transistor is given by expression 4.15 and for M_{P1} transistor is calculated using

$$r_{sd} = \left(\frac{dI_D}{dV_{SD}} \right)^{-1} = \frac{1}{\beta \cdot (V_{SD} - |V_T|)} \tag{4.17}$$

From expressions 4.15 and 4.17 it is possible to calculate the equivalent resistance from the symmetrical load resulting in

$$r_{sdeq.} = \frac{1}{\beta \cdot (V_{DD} - V_{Bias\_P} - 2 \cdot |V_T|)} \tag{4.18}$$

The bias current of this circuit can be calculated using expression 4.14 and expression 4.16 resulting in

$$I_B \approx \frac{\beta}{2} \cdot (V_{DD} - V_{Bias\_P} - V_T)^2 + \frac{\beta}{2} \cdot (V_{swing} - V_T)^2 \tag{4.19}$$

This equation shows that the current in the buffer changes quadratically with both the control voltage (V_{Bias_P}) and the clock signal amplitude (V_{swing}).
If both PMOS transistors, in the symmetrical load, have the same size, this type of load exhibits an almost constant conductance, when the output voltage changes. The delay of each differential stage varies with the value of the load conductance, which can be adjusted using the control voltage V_{Bias_P}. The delay of the differential buffer is proportional to the RC time constant of the output node and it can be calculated [2] using :

$$T_D(V_{Bias\_P}) \approx \frac{0.7 \times C}{\beta \cdot [(V_{DD} - V_{Bias\_P} - 2 \cdot |V_T|)]} \tag{4.20}$$

From this expression it is clear that the delay depends only on the β, C and V_{Bias_P} values and only this last one can be used to vary the delay. The minimum delay is obtained when the V_{Bias_P} is equal to 0 volt ($V_{SG} = V_{DD}$) and the maximum delay is obtained when $V_{Bias\_P} = V_{DD} - |V_T| - V_{swing}$ ($V_{SG} = V_{swing} + |V_T|$) corresponding to the onset of saturation region in the PMOS transistor.

The maximum delay a single buffer can add is limited to $T_{Dmax} = T_{CLK}/4$ because a larger delay would result in an output signal with an amplitude smaller than the input signal amplitude. Therefore if a larger delay value is required it is necessary to use more than one delay element in cascade. A voltage controlled delay line (VCDL) is designed in section 3.3.4 to accomplish a larger delay.

The signal amplitude in this circuit must be large enough in order to guaranty that the differential pair saturates and that it is larger than the V_T of the load transistors for all the corners. The circuit is designed in order to have a voltage swing of 400 mV and a bias current (for the minimum delay case) of 100 μA. The load PMOS transistors are designed to have a small channel length (L = 250 nm) and a small W/L ratio. With this design the theoretical value to obtain the maximum delay is $V_{Bias\_P} = 470$ mV. Simulation results showed that this value could be approximate 670 mV. A larger value will not guaranty all of the design goals in the corner analysis. The value of the output capacitor (C) was determined by electrical simulations, in order to obtain the desired delay variation in the complete VCDL, resulting in C = 1.22 ρF. The transistors inside the differential pair and M_{N1} transistor have the same dimensions of the differential buffer in Fig. 4.1.

	V_{dsat} (mV)	L(μm)	W(μm)
M_D	80	0.12	7.5
M_{N1}	400	1.5	3.7
M_{P1}	870	0.25	0.7
M_{P2}	870	0.25	0.7

TABLE 4.5: Buffer design summary for a bias current equal to 100 μA.

4.4 Replica Bias for the Variable Delay Buffer

In the differential buffer with variable delay the V_{Bias_P} voltage is used to change the load resistance controlling the delay of the buffer. Varying the resistance value will also change the voltage swing of the buffer. In order to maintain the voltage swing constant we will use a negative feedback circuit to adjust the bias current to compensate the load resistance variation. This architecture is depicted in Fig. 4.6.

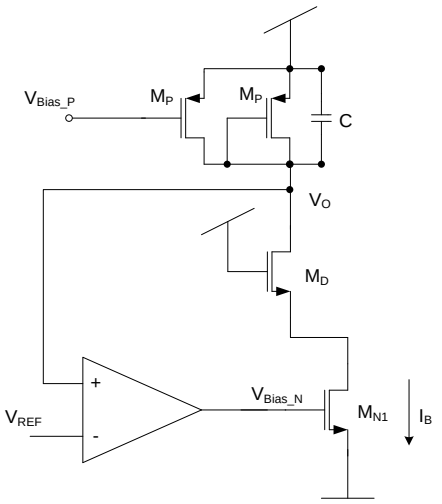

FIGURE 4.6: Architecture of the replica bias for the variable delay buffer.

This replica bias principle and design is the same as the one in section 4.2, the only difference is the resistive load made by PMOS transistors as showed in Fig. 4.7 .

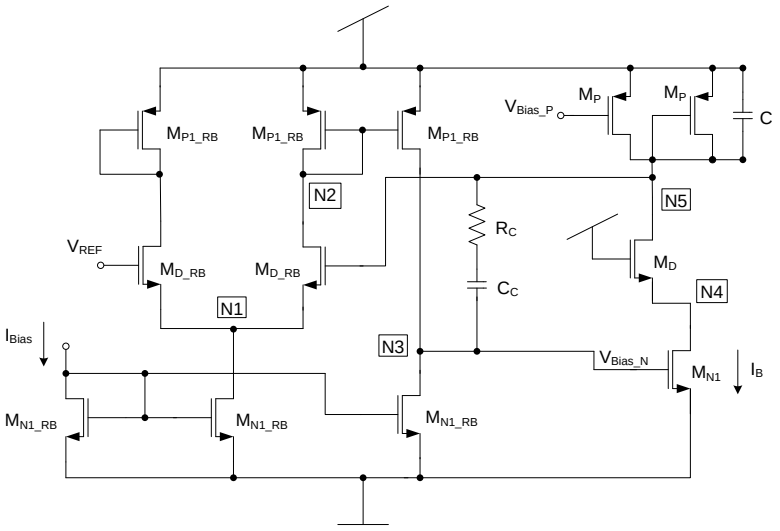

FIGURE 4.7: Replica bias for the variable delay buffer circuit schematic.

The replica bias circuit is designed to have a bandwidth larger than the clock frequency of the circuit (in order not to introduce any extra poles into the circuit) and in order to be stable for all the possible values of the control voltage V_{Bias_P}. If a clock frequency of 2 MHz is used, then the replica bias should have a loop bandwidth of at least 8 MHz. Inside the half-buffer the transistors have the same V_{dsat} voltages and channel lengths as the transistors inside the differential buffer with variable delay. The transistors M_{D_RB} inside the differential pair will have a V_{dsat} inferior to the ones in section 4.2 to increase the loop gain. The values of the resistance and capacitor will be selected together using AC simulations resulting in $C_C = 3.5$ ρF and $R_C = 13.5$ kΩ. DC and AC simulations were made considering the maximum and minimum values for V_{Bias_P}. Results are showed next in table 4.6.

	Design Goals	Simulation Results ($V_{Bias\_P} = 0$ V)	Simulation Results ($V_{Bias\_P} = 650$ mV)
Gain(dB)	32	48.28	43.76
GBW(MHz)	8	17.2	18.1
Phase(°)	60	69.7	81.6

TABLE 4.6: Replica bias for the variable delay buffer simulation results.

Since the simulations results can vary with temperature, supply voltage and in this case the V_{Bias_P} voltage values, a corners analysis was made to assure that the loop is unconditionally stable. The results are showed in the next page.

Voltages (V)	Section	Temperature (°C)	Gain (dB)	GWB (MHz)	PM (°)
Vdd = 1.2	Slow	0	50.76	22.6	66.6
		80	48.19	18	76.5
$V_{Bias\_P} = 0$	Fast	0	47.95	16.0	65.2
		80	45.69	12.7	75.6
Vdd = 1.2	Slow	0	49.18	21.6	69
		80	45.54	17.3	79.3
$V_{Bias\_P} = 0$	Fast	0	47.01	15.7	67.7
		80	42.06	12.3	79.4
Vdd = 1.2	Slow	0	50.42	22.3	65.9
		80	48.72	17.8	75.1
$V_{Bias\_P} = 0$	Fast	0	48.14	16.1	63.8
		80	46.94	12.9	73.6

Voltages (V)	Section	Temperature (°C)	Gain (dB)	GWB (MHz)	PM (°)
Vdd = 1.2	Slow	0	50.17	23.6	81.3
		80	38.18	16.8	93.2
$V_{Bias\_P} = 0.65$	Fast	0	46.38	17.5	69.3
		80	36.74	13.1	84.4
Vdd = 1.08	Slow	0	62.33	25.7	61.5
		80	44.62	17.3	77.1
$V_{Bias\_P} = 0.53$	Fast	0	51.19	19.1	70.4
		80	35.28	12.5	93.1
Vdd = 1.3	Slow	0	46.13	21.6	83.8
		80	38.18	16.9	93.3
$V_{Bias\_P} = 0.75$	Fast	0	46.19	16.9	67.7
		80	39.25	13.6	79.7

TABLE 4.7: Corners analysis simulation results confirming the stability of the loop.

	V_{dsat}(mV)	L(μm)	W(μm)
M_{D_RB}	75	0.5	18
M_{N1_RB}	300	2	8.8
M_{P1_RB}	300	2	20
M_P	870	0.25	0.7

TABLE 4.8: Replica bias for the variable delay design summary.

4.5 Voltage Controlled Delay Line

After the design of the circuits described in the previous sections, its possible to accomplish the architecture of the VCDL in Fig. 3.12. The delay of the VCDL as a function of the control voltage, was simulated for different process corners, the result is shown in Fig. 4.8.

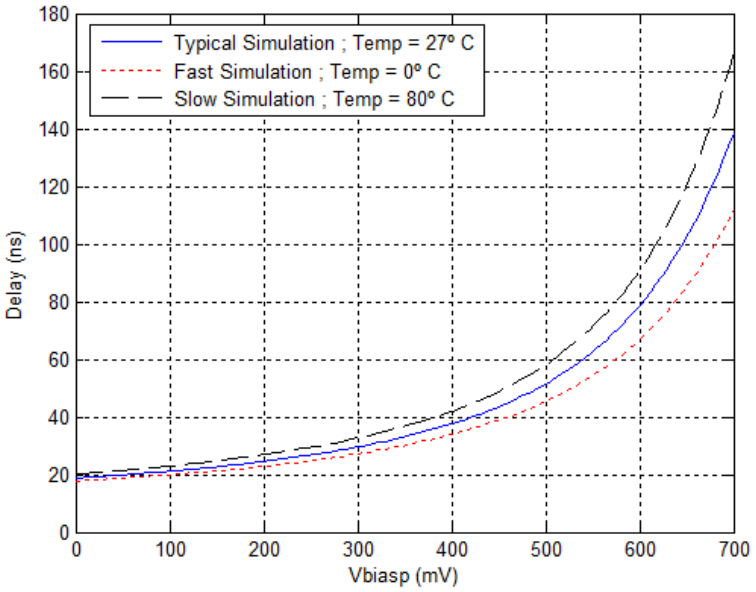

FIGURE 4.8: Simulated delay of the VCDL as a function of the control voltage.

This graphic shows that for a control voltage (V_{Bias_P}) of $\approx$ 650 mV the delay line can produce a delay of 100 ns and for a V_{Bias_P} voltage value of 0 V, a minimum delay of 18.7 ns.

The gain factor of the VCDL (K_{VCDL}) is given by the derivative of the delay to the control voltage (V_{Bias_P}), this is inversely proportional to the square of the control voltage:

$$K_{VCDL} = \left(\frac{dT_D}{dV_{Bias\_P}} \right) \propto \frac{1}{V^2_{Bias\_P}} \tag{4.21}$$

This gain can be obtained by numerically calculating the derivative of the delay of VCDL (obtained by electrical simulation Fig. 4.8). The value of the K_{VCDL} as a function of the control voltage is showned in Fig. 4.9.

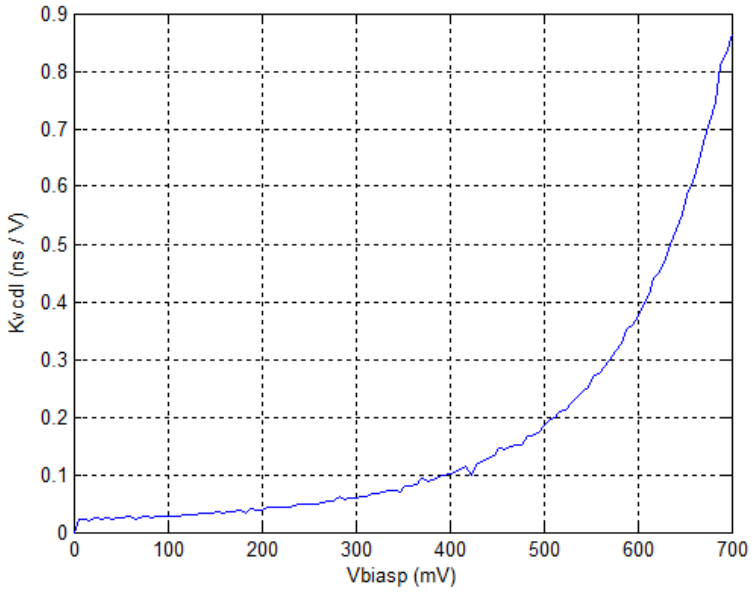

FIGURE 4.9: Simulated gain curve of the VCDL.

As expected, this graph shows that (K_{VCDL}) increases quadratically with the control voltage. This means that the loop gain of the DLL will increase quadratically with the desired delay. This is a problem, because it means that the DLL closed loop pole frequency and quality factor will change significantly with the delay (as shown by expressions 3.3 and 3.4). The end result is that for larger delays, the K_{VCDL} value is very large which means that the closed loop pole frequency increases (the quality factor also) and therefore the jitter noise at the output of the DLL will also increase. In order to maintain a small jitter noise at the output of the DLL it would be necessary to use a charge pump current (I_P) value that can produce a compromise between the jitter power for large delays and the DLL response time for small delays. This results in a value of I_P equal to 5 μA. This subject will be further address in the charge pump design section.

4.6 Phase Detector

The phase detector (Fig. 3.8) will be implemented with differential signals, because this type of signals generates much less noise than CMOS signals. The flip-flop circuits are implemented using NOR gates [16] as showed in Fig. 4.10.

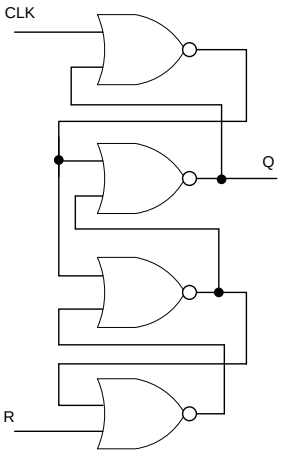

FIGURE 4.10: Flip-flop circuit schematic.

The differential gates are implemented using a differential buffer from section 4.1 with a second differential pair to obtain a logic function, as showed in Fig. 4.11.

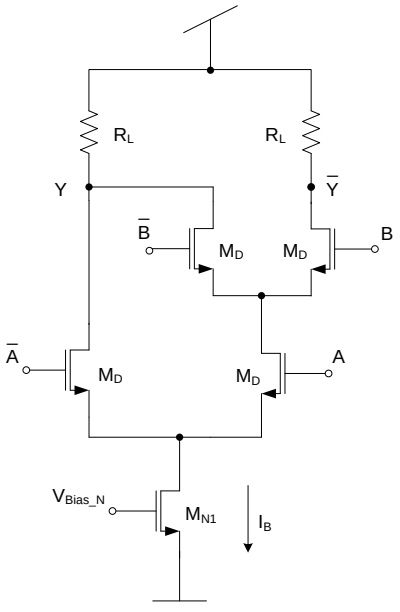

FIGURE 4.11: Differential AND gate circuit schematic.

This circuit can realize the four basic logic operations AND, NAND, OR and NOR, depending on how the input signals are connected. Fig. 4.11 shows a differential AND

gate, reversing the polarity of both input signals, would change the circuit into a OR gate. Realizing a NOT function using differential signals consists simply in inverting the output signals. This way we achieve the NAND and NOR gates. The truth table of the differential AND gate is shown in table 4.9. The design of the differential gates are equal to the differential buffer from section 4.1 (see table 4.1).

Differential A	Differential B	A	$\bar{A}$	B	$\bar{B}$	Y	$\bar{Y}$	Differential Y
0	0	0	1	0	1	0	1	0
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	0	1	0
1	1	1	0	1	0	1	0	1

TABLE 4.9: Truth table of the differential AND gate.

4.7 Charge Pump

In section 3.3.2 a brief introduction to the architecture of the CP was done. The main problem with a differential charge pump is the fact that it haves a lower output resistance made by the constant connection of the current sources to output node. The CP uses a folded cascode topology to increase the output resistance and maintain a large output voltage swing for a low power supply. Since the CP is completely differential the output resistance should be maximized through a careful design of the current source circuits inside the CP. This circuit is depicted in Fig. 4.12.

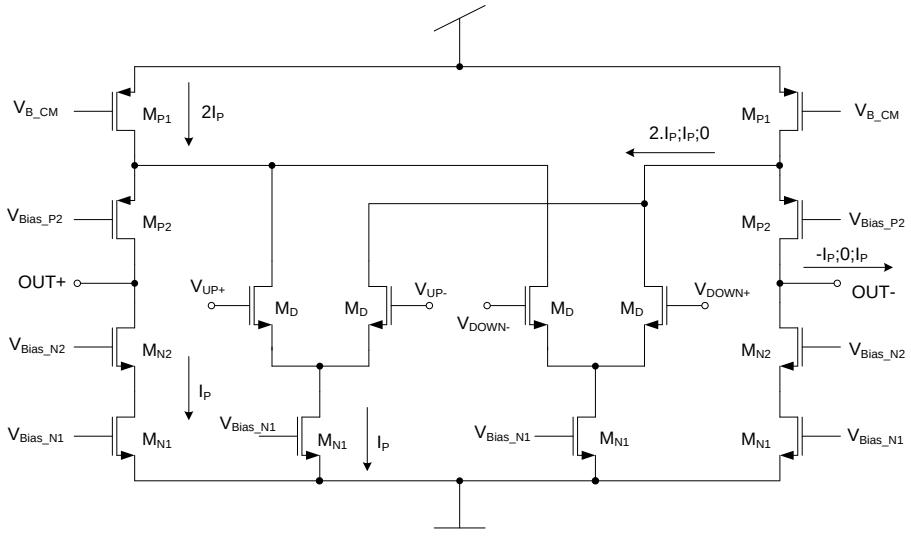

FIGURE 4.12: Folded cascode charge pump circuit schematic.

The transistors M_{P1} produce a current equal to $2.I_P$ and the transistors M_{N1} produce a current equal to I_P. This current will charge a capacitor (C_1) increasing or decreasing its voltage depending on which current source is on. The output current is determined by the two differential pairs that act as switches steering the current produced by the M_{P1} transistors from the output branch. Transistors M_{P2} and M_{N2} act as cascode devices and increase the output resistance of the current source transistors. The output resistance of the charge pump is given by [2]

$$R_{out} = \frac{R_N \cdot R_P}{R_N + R_P} \tag{4.22}$$

where

$$R_P \approx \frac{1}{g_{dsP1} + g_{dsND}} \cdot \frac{gm_{P2}}{g_{dsP2}} \tag{4.23}$$

and

$$R_N \approx \frac{1}{g_{dsN1}} \cdot \frac{gm_{N2}}{g_{dsN2}} \tag{4.24}$$

The maximum differential output voltage of the CP is given by

$$V_{swing\_CP} = V_{DD} - V_{dsat\_P1} - V_{dsat\_P2} - V_{dsat\_N2} - V_{dsat\_N1} - V_{tol} \tag{4.25}$$

where V_{tol} is the safety margin to guaranty that all the transistors are well into the saturation region (approx. 120 mV).

Since the operation of the CP depends on the common mode comparator (see Fig. 3.11), both this circuits must be design together in order to guaranty that the common mode feedback loop is stable. Expression 3.5 suggest that the common mode comparator circuit can be implemented using two differential pairs, each comparing the common mode reference voltage (V_{REF_CM}) with one of the output voltages [2]. The common mode comparator circuit is depicted in Fig. 4.13.

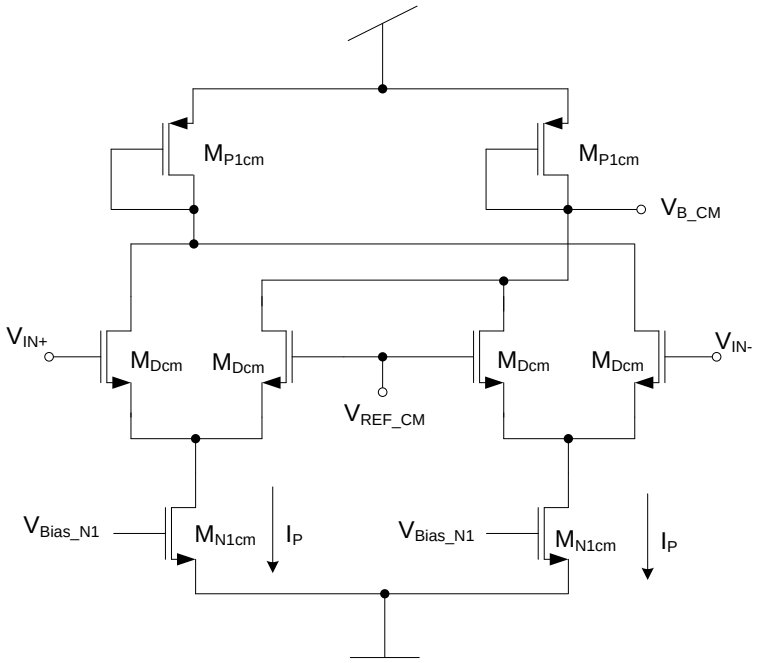

FIGURE 4.13: Common mode comparator circuit.

The differential pairs have an output current proportional to the difference between the positive or negative output voltage and the desired common mode voltage level. The currents produced by this differential pairs are summed in the transistor M_{P1}, generating a bias voltage for the transistor M_{P1} inside the charge pump circuit (these transistors should have the same channel length and V_{dsat} voltage). If the differential pairs saturate the common mode circuit will stop adjusting the output common voltage (V_{B_CM}), so in order to prevent this it is required that

$$V_{swing\_CP} < \sqrt{2} \cdot V_{dsat\_Dcm} \tag{4.26}$$

The minimum value of the desired common mode voltage is also limited by the minimum input common mode voltage of the differential pairs and is given by

$$V_{CM} \geq V_T + V_{dsat\_Dcm} + V_{dsat\_N1cm} \tag{4.27}$$

From the small signal analysis of this loop in [2], the common mode loop gain expression results in

$$G \approx 2 \times gm_{Dcm} \cdot R_{out} \tag{4.28}$$

The common mode feedback loop must have a bandwidth larger than the activation frequency of the charge pump, which is the DLL reference frequency (2.5 MHz), to assure that any common mode voltage wander is corrected within a clock cycle. A value of 5 MHz is established for the design goal. The common loop gain must be larger than 40 dB to guaranty that the error between the desired common mode voltage and the actual value is inferior to 1% and the phase margin of the loop must be larger than 60° to guaranty stability.

According to section 3.2, one of the main circuit parameters of the digitally programmable DLL is the $\frac{I_P}{C_1} = 66.78$ volt/ms. From this expression it is clear that a large I_P current will result in a large C_1 capacitor value. The results of the design of the VCDL in section 4.5, showed that because of the increase of the K_{VCDL} for large delays, the value of the I_P current must be a compromise between the jitter power for large delays and the DLL response time for small delays. This means that for large delays it is necessary a low I_P current value and for small delays a large one. Taking all of the above in consideration a value of 5 μA were established for I_P current, resulting in a C_1 capacitor value of approx. 74.54 pF.

From expression 4.24, transistors M_{N1} and M_{N2} are designed to maximize the R_N value, the channel lengths are set to 1.5 μm, the V_{dsat} voltages are set to 150 mV and 100 mV. The transistors M_D have the same channel lengths and V_{dsat} voltage as the transistors inside the differential pair inside the differential buffers. Transistor M_{P1} is designed to have a channel length equal to 1 μm and a V_{dsat} voltage value of 225 mV. This values are a compromise between the drain resistance and the parasitic capacitance of the transistor, because this transistor determines the value of two pole frequencies according to the study of the small signal analysis of the loop in [2]. Transistor M_{P2} is designed also to maximize the output resistance, the channel length are set to 1.5 μm and a V_{dsat} voltage value set to 100 mV.

With this design and from expression 4.25, the maximum differential output voltage of the CP is approximated 500 mV, this results in a V_{dsat} voltage of the transistors inside the differential pair inside the common mode comparator circuit (see expression 4.26), larger than 350 mV. Using this value in expression 4.27 results in a minimum value for the desired common mode voltage larger than 900 mV. Since the voltage supply of the circuit is 1.2 V, a $V_{CM} \geq 900$ mV is not possible with a V_{swing_CP} equal to 500 mV. In the other hand, if this values are not used this means that the common mode comparator circuit will not function as predicted. The solution encountered for this problem starts by setting

the V_{CM} value to 500 mV, resulting in a low V_{dsat} voltage value for the M_{Dcm} transistors, which at one point will make the transistors inside the differential pair saturate and the common mode voltage will stop being adjust. Simulation results showed that this will not affect the functionality of the DLL (with a careful design of transistors M_{Dcm}) since when the comparator stops adjusting the common mode voltage will maintain stable at approximate value of 500 mV.

Inside the common mode comparator circuit, transistors M_{P1cm} and transistors M_{N1cm} are designed with the same channel length and V_{dsat} voltage as the equivalent transistors inside the charge pump. Since transistors M_{N1cm} will have $2.I_P$ the size relation must be multiplied by 2. Transistors M_{Dcm} channel length are set to 1.2 μm and the V_{dsat} voltage are set with a low value. This transistor size relation W/L is adjusted by simulations results.

After the previous describe design process the circuit design parameters were obtain and are showed next in table 4.10.

	Design Goals	Typical Simulation Results
Gain(dB)	40	74.87
GBW(MHz)	5	6.89
Phase(°)	60	82.90
Rout(MΩ)	∞	63.18

TABLE 4.10: Charge pump simulation results.

Since the simulations results can vary with temperature, supply voltage values, a corners analysis was made to assure that the loop is unconditionally stable.

Supply Voltage (V)	Section	Temp.(°C)	Gain (dB)	GWB (MHz)	PM (°)	Rout(MΩ)
Vdd = 1.2	Slow	0	74.70	7.70	81.9	64.77
		80	69.60	6.92	82.0	39.88
	Fast	0	76.28	6.58	83.74	68.12
		80	72.50	5.79	83.88	49.77
Vdd = 1.08	Slow	0	74.70	7.70	81.93	54.42
		80	69.60	6.92	82.06	32.06
	Fast	0	76.28	6.58	83.74	61.60
		80	72.50	5.79	83.88	44.07
Vdd = 1.3	Slow	0	74.70	7.70	81.93	67.26
		80	69.60	6.92	82.06	39.25
	Fast	0	76.28	6.58	83.74	70.47
		80	72.50	5.79	83.88	49.79

TABLE 4.11: Corners analysis simulation results confirming the stability of the loop.

This results showed that the circuit design parameters are well adjusted and the loop is unconditionally stable.

	V_{dsat}(mV)	L(μm)	W(μm)
M_D	80	0.12	7.5
M_{N1}	150	1.5	1.3
M_{N2}	100	1.5	3
M_{P1}	225	1	4
M_{P2}	100	1.5	15

TABLE 4.12: Charge pump design summary.

	V_{dsat}(mV)	L(μm)	W(μm)
M_{Dcm}	80	1.2	4.8
M_{N1cm}	150	1.5	2.7
M_{P1cm}	225	1	4

TABLE 4.13: Common mode comparator design summary.

4.8 Biasing Circuit for the Charge Pump

This circuit is responsible for establishing the voltages to ensure that the transistors inside the charge pump are well in the saturation region. It is a simple circuit composed by current mirrors, as shown in Fig. 4.14 .

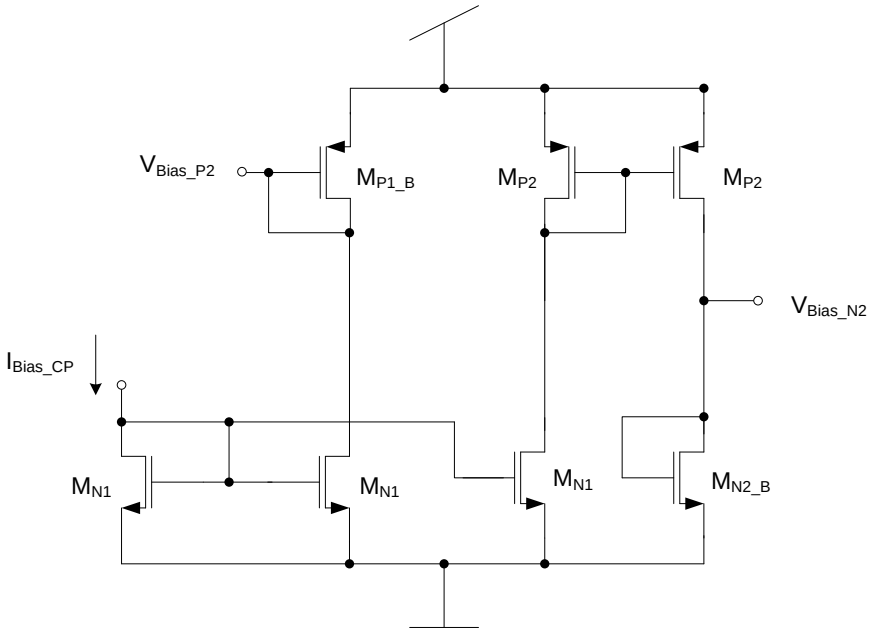

FIGURE 4.14: Biasing for the charge pump circuit schematic.

The I_{Bias_CP} is set to 5 μA as explained in the section above. Transistors M_{N1} are designed with the same channel length and V_{dsat} voltage as the transistors M_{N1} inside the charge pump. Transistor M_{N2_B} V_{dsat} voltage requires that

$$V_{dsat}(M_{N2\_B}) \geq V_{dsat}(M_{N1}) + V_{dsat}(M_{N2}) \tag{4.29}$$

where M_{N1} and M_{N2} are the transistors inside the charge pump, as shown in Fig. 4.15.

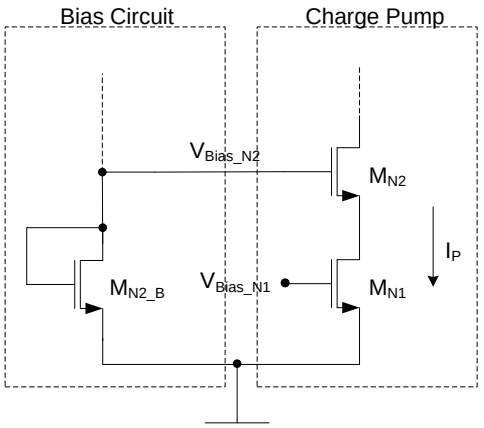

FIGURE 4.15: Design of transistor M_{N2_B} .

From the design of the charge pump, the V_{dsat} voltage value of transistor M_{N2_B} must be greater than 250 mV. The value is set to 350 mV and the channel width is set to 1 μm. Transistors M_{P1_B} channel width is set to 1 μm and the channel length is adjusted by simulation results, resulting in a value equal to 1.5 μm. The channel length of transistors M_{P2} is set to 1.2 μm and the V_{dsat} voltage value set to 150 mV.

	V_{dsat}(mV)	L(μm)	W(μm)
M_{N1}	150	1.5	1.3
M_{N2_B}	350	6.1	1
M_{P1_B}	$\approx$ 375	1.5	1
M_{P2}	150	1.2	5.3

TABLE 4.14: Biasing circuit design summary.

4.9 Differential to Single Ended Signal Converter

This circuit is responsible for creating an extra pole in the loop in order to obtain a second order system and for converting the differential output voltage of the charge pump into a single ended voltage, used to control the voltage controlled delay line (VCDL). The circuit will also provide some gain into the loop and is depicted in the Fig. 4.16 below.

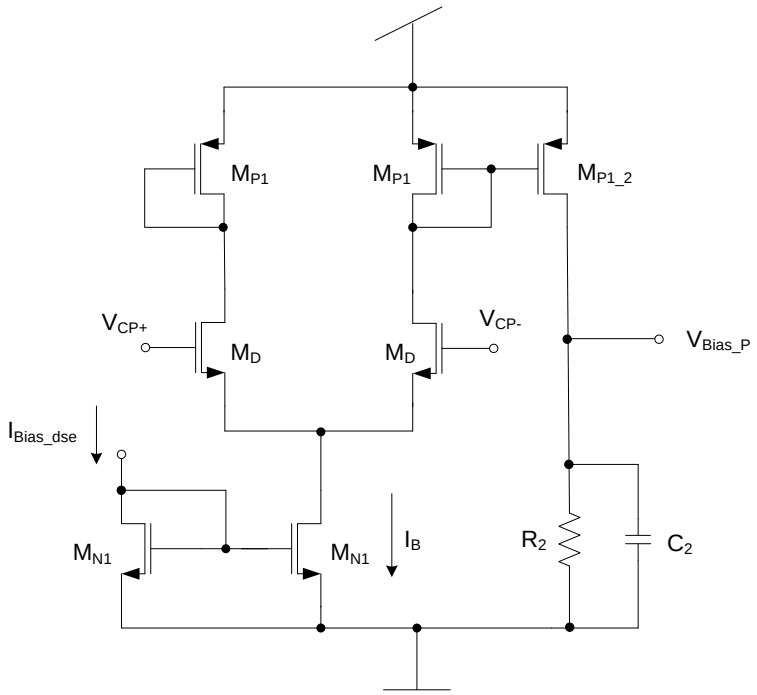

FIGURE 4.16: Differential to single ended conversion circuit and second pole.

The output resistor (R_2) together with the capacitor (C_2) implements the time constant (τ_{RC}) necessary to create the second pole of the DLL loop. The DLL clock frequency is 2.5 MHz, so the second pole frequency must be much smaller than this value. The value of the output resistance value is selected together with the output capacitance to obtain the desired value of τ_{RC} and a small area. According to section 3.2, one of the main circuit parameters of the digitally programmable DLL is the $\tau_{RC} = 7.16$ μs. The output resistor value is set to 150 KΩ resulting in a output capacitance value of 47.76 pF. With this values, the second pole frequency value is 22.2 KHz. The bias current (I_{Bias_dse}) is set to 2.5 μA. Transistors M_D are designed with a large V_{dsat} voltage value of 300 mV and the channel length are set to 1 μm. The V_{dsat} voltage value of transistors M_{N1} are set to 100 mV and the channel length are set to 1.2 μm. Transistors M_P1 and M_P1_2 are designed with a channel length of 1 μm and a V_{dsat} voltage value of 150 mV. Transistors M_P1_2 will have $2.I_B$ so the size relation must be multiplied by 2. This transistor was adjusted

with the simulations of the DLL in order for the maximum delay of the VCDL (100 ns), the output voltage of the circuit is equal to 650 mV. After the simulations the maximum gain measured was equal to 2.8 .

	V_{dsat}(mV)	L(μm)	W(μm)
M_D	300	1	9
M_{N1}	100	1.2	1.2
M_{P1}	150	1	2.2
M_{P1_2}	150	1	4.6

TABLE 4.15: Differential to single ended design summary.

4.10 Digitally Programmable DLL

All of the constituting blocks of the DLL were designed in the sections above. This section will show how the simulations of the digitally programmable DLL were made and the respective results. The architecture of the circuit is shown again in Fig. 3.2.

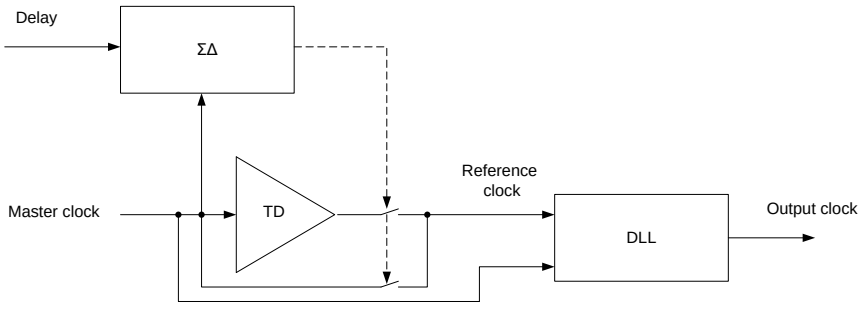

FIGURE 4.17: Architecture of the digitally programmable DLL.

The digital ΣΔ modulator controls the switching sequence that produces the reference clock. This clock is created by selecting between the input clock and a delayed version of the input clock. The switches used to do this selection can add jitter and extra delay to the clock signals, due to the ON resistance and the parasitic capacitance. These switches are implemented as CMOS switches as shown in Fig. 4.18. The transistors in these switches must be carefully designed in order to reduce the unwanted effects in the clock signals. The design parameters are shown in Table 4.16.

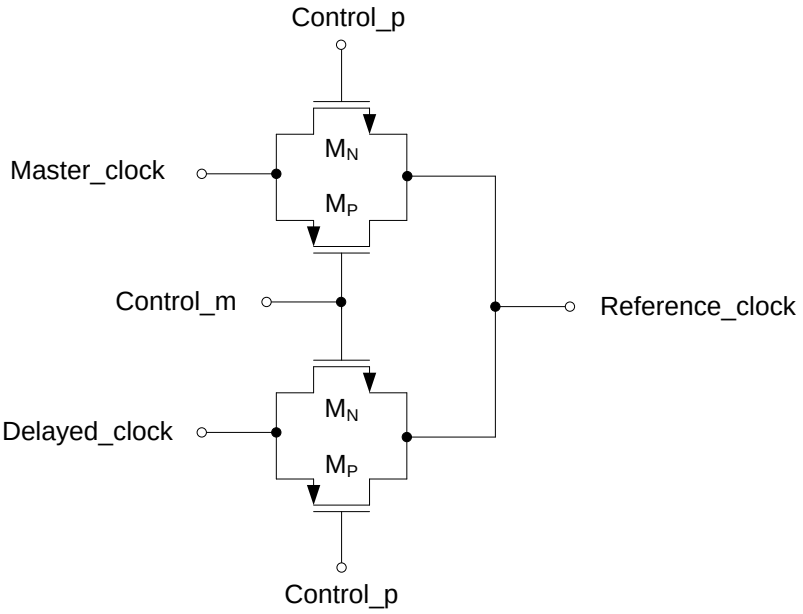

FIGURE 4.18: CMOS switches circuit schematic.

	L(μm)	W(μm)
M_N	0.12	0.16
M_P	0.12	20

TABLE 4.16: CMOS switches design summary.

The $\Sigma\Delta$ modulator was simulated at high level for different input values and the resulting output bit stream was imported into the electrical simulator to control several voltage sources. This voltage sources are responsible for the master clock, the delayed clock and the differential signal (Control_m and Control_p) used to switch between the master clock and the delayed clock. The master clock frequency is 2.5 MHz, corresponding to a clock period of 400 ns. These signals were used to run electrical simulations of the circuit with different delays, the resulting step responses of the programmable delay are shown next in Fig. 4.19. The delay produced by the circuit as a function of the programming delay is shown in Fig. 4.20, and the simulated output jitter noise of the circuit for different delays is shown in Fig. 4.21.

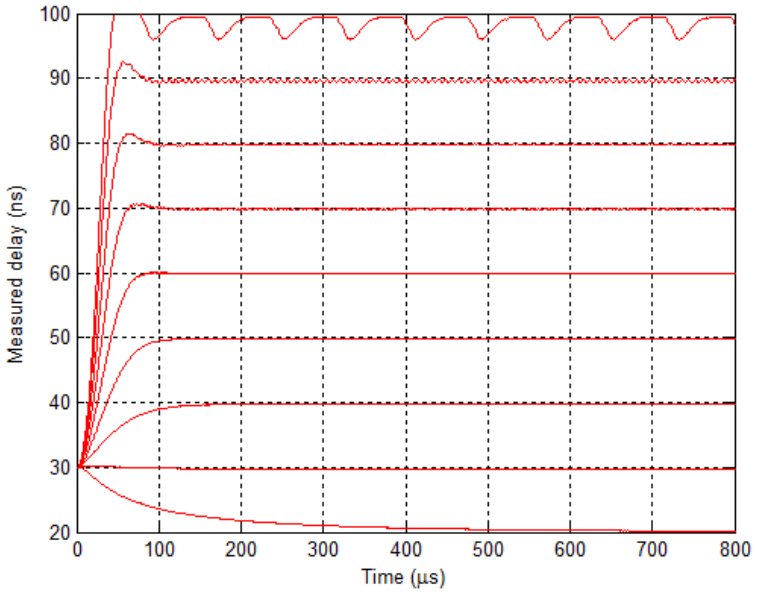

FIGURE 4.19: Simulated step response of the DLL. Programmable delay from 20 ns to 99 ns.

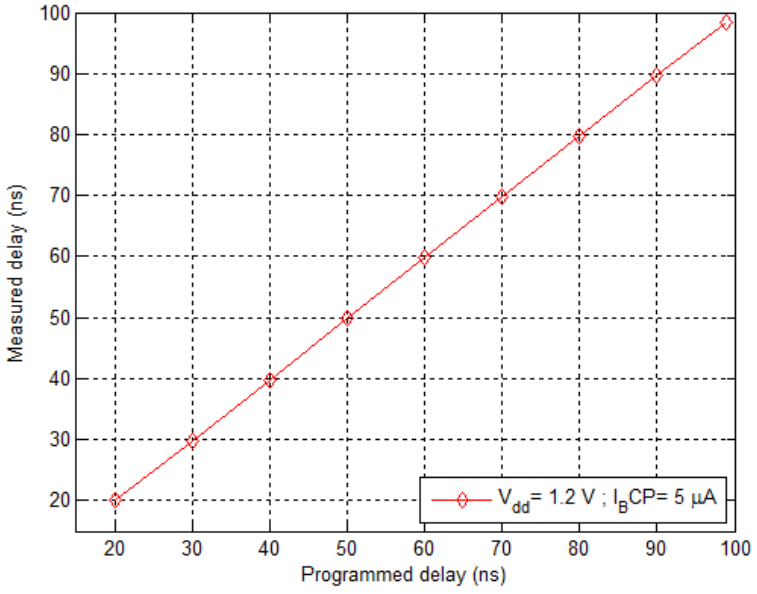

FIGURE 4.20: Simulated output delay as a function of the programming delay.

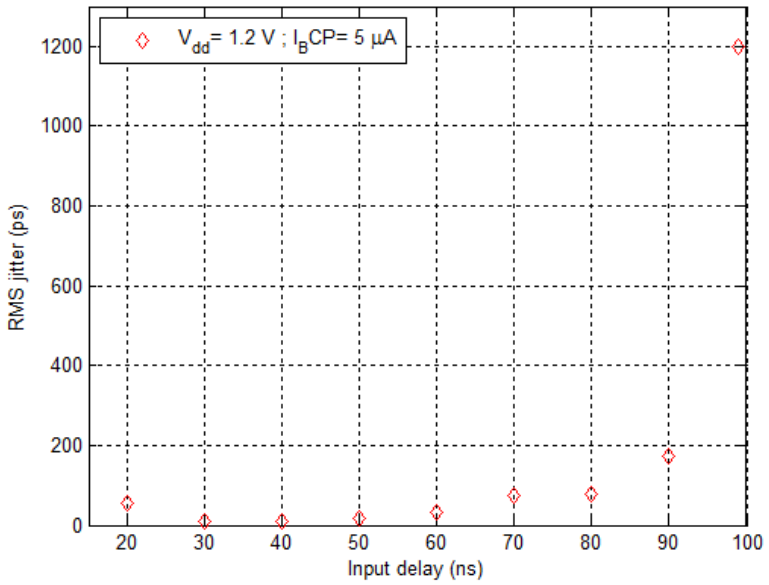

FIGURE 4.21: Jitter noise simulation results of the programmable DLL.

These simulation results shown that the DLL loop is stable for the different delays, but the output jitter increases with the desired delay. The cause for this increase is due to the increase of the gain factor of the VCDL (K_{VCDL}) (see section 4.5). For the programming delay value of 99 ns the output jitter value is equal to 1199 ps.

In order to obtain a better performance it would be necessary to adjust the charge pump current, in order to compensate for the variation of the K_{VCDL}. Noting that the bias current of the variable delay (given by expression 4.14) increases with the square of the control voltage value (V_{Bias_P}) and that the K_{VCDL} value decreases with the square of the control voltage (expression 4.21), it is clear that the product of these two variables can be independent of the control voltage (in a first order approach). Therefore the charge pump current value is determined according to the value of the bias current of the variable delay buffer. This is achieved by adjusting the bias current of the charge-pump circuit using the circuit in Fig. 4.22.

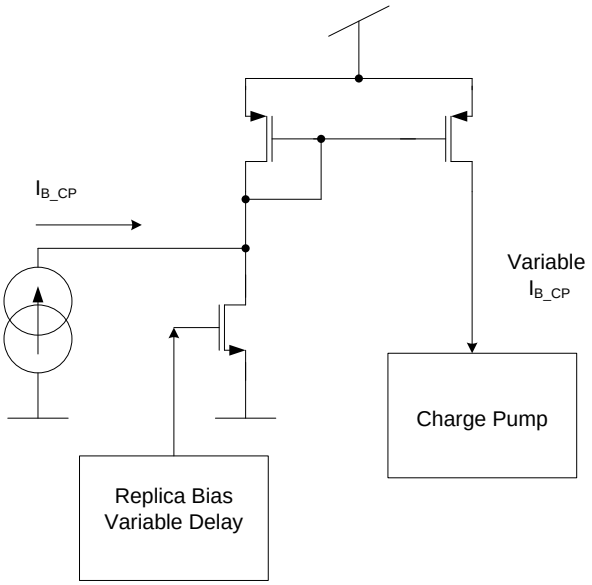

FIGURE 4.22: Architecture of variable charge pump current.

The previous circuit has a fixed bias current (I_{B_CP} value of 1.67 A, the variable bias current will change between approx. 6.5 μA (for a delay of 20 ns) and approx. 185 nA (for a delay of 99 ns). Since the charge pump current as a large variation, the closed loop frequency pole (f_p) value and the quality factor (Q_p) will also change. This values are very important since they are responsible for the system resolution (see section 3.2). Simulation results of the DLL discrete function (Eq. 3.2) with the maximum and minimum charge pump current values are shown in Table 4.17.

Charge Pump Current (μA)	f_p (KHz)	Q_p	Resolution (bits)
0.185	3.07	0.138	14
6.5	18.24	0.791	8.8

TABLE 4.17: Closed loop frequency pole (f_p) and quality factor (Q_p) simulations results with variable charge pump current.

From section 3.2, the programming resolution must be equal to 9 bits. This simulations results shows that for the minimum delay value of 20 ns the resolution is equal to 8 bits. This is a isolated case since for a approx. 22 ns delay the resolution will increase to 9 bits. The solution for this problem would be to increase the value of the output capacitor (C_1) of the charge pump. This value was calculated in the design of the charge pump and it is approx. 74.54 pF. Increasing this value to 83 pF will accomplish the goal. This solution will have minor effects on the simulation results of the DLL and since it is a isolated case, this modification was not done.

The resulting step responses of the programmable delay with the variable charge pump current are shown in Fig. 4.23. The delay produced by the circuit as a function of the programming delay is shown in Fig. 4.24, for the case of the variable charge pump current (I_{B_CP} = 1.67 A) and for the case of the fixed charge pump current (I_{B_CP} = 5 A). The relative error of the programmed delay are shown in Fig. 4.25. The simulated output jitter noise of the circuit for different delays is shown in Fig. 4.26. These simulation results show that the programmable delay, using the variable charge pump current, has an output jitter noise for the maximum delay equal to 105.18 ps.

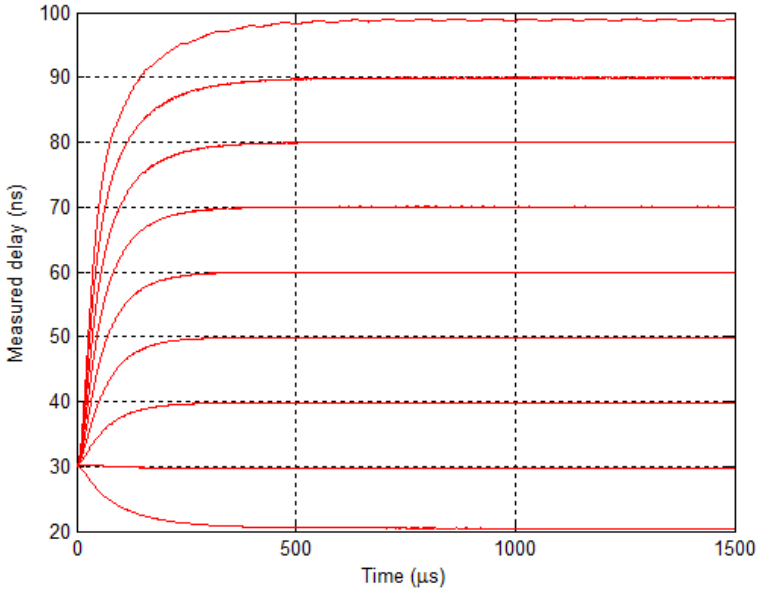

FIGURE 4.23: Simulated step response of the DLL. Programmable delay from 20 ns to 99 ns.

From this graph and Fig. 4.19 it is clear the improved results for the maximum delay of the system response.

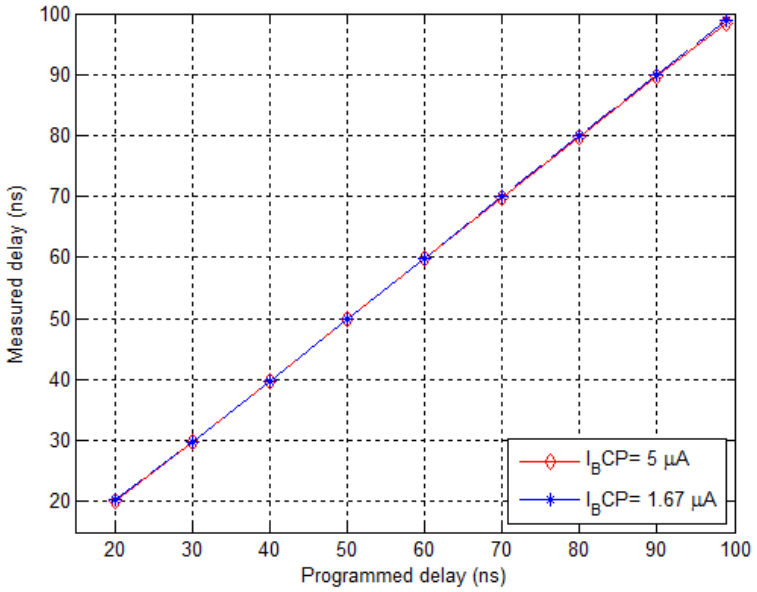

FIGURE 4.24: Simulated output delay as a function of the programming delay.

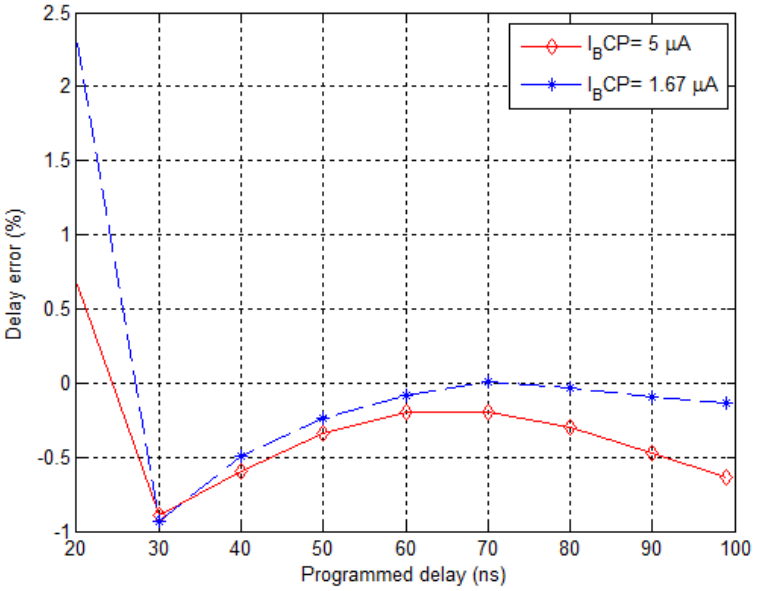

FIGURE 4.25: Delay relative error simulation results of the programmable DLL.

This results shows that using a variable charge pump current improves the programming linearity for large delays but does not for the minimum delay of 20 ns.

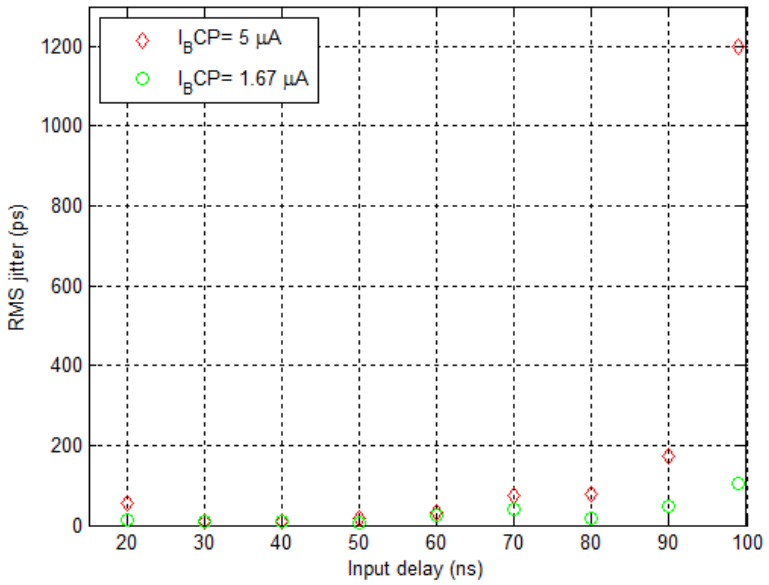

FIGURE 4.26: Jitter noise simulation results of the programmable DLL.

	Delay (ns)	Power dissipation (mW)	Jitter noise rms (ps)	Delay error (%)
Constant (5 μA)	20	2.28	53.7	0.65
	99	2.11	1199	-0.63
Variable (1.67 μA)	20	2.05	11.6	2.29
	99	2.31	105.1	-0.14

TABLE 4.18: Programmable delay results summary.

Chapter 5

Conclusion and Future Research

This thesis presents a digitally programmable delay locked loop intended for use as timing generator in a RADAR ranging system. The architecture presented uses a sigma delta modulator to generate a delay unaffected by matching and a delay lock loop (DLL) to filter the excess jitter noise from the output clock. Designs and simulations results of the DLL are presented, showing that by making the current of the charge pump variable results in a improved jitter noise and delay error.

There is some possible future work. The complete design of a UWB radar sensor is the most obvious, but it is also possible to study and design a third-order DLL since it is possible that will result in a improve ranging resolution of the radar and a better stability of the system.

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