Power-and-Area Efficient 14-bit 1.5 MSample/s Two-Stage Algorithmic ADC based on a Mismatch-Insensitive MDAC

B. Esperança[1], J. Goes[1], R. Tavares[1], A. Galhardo[2], N. Paulino[1], M. Medeiros Silva[3]

[1]Universidade Nova de Lisboa/UNINOVA
Campus da FCT/UNL
2829 – 517 Caparica – PORTUGAL
E-mail: bae@uninova.pt

[2] ISEL – DEEA
Av. Emídio Navarro, nº 1
1949 – 014 Lisboa – PORTUGAL
E-mail: galhardo@deea.isel.ipl.pt

[3] INESC-ID
Rua Alves Redol, 9
1000-029 Lisboa – PORTUGAL
E-mail: manuel.silva@inesc-id.pt

Abstract **– This paper presents a 14-bit 1.5 MSample/s two-stage algorithmic ADC with a power-and-area efficiency better than 0.5 pJmm^2 per conversion. This competes with the most efficient architectures available today namely, ΣΔ and self-calibrated pipeline. The 2 stages of the ADC are based on a new 1.5-bit mismatch-insensitive MDAC and simulations demonstrate that a THD of –79 dB and an ENOB better than 12 bits can be reached without self-calibration.**

I. Introduction

Two different figures-of-merit (*FM*) for ADCs are usually employed. The first one, FM_1, represents the used energy *per* conversion [1]

$$FM_1 = \frac{P}{2^{ENOB} \cdot Min\{2 \cdot BW, Fs\}} \quad \text{(pJ)} \qquad (1)$$

where *Fs* is the sampling rate, *BW* is the maximum bandwidth of the input signal, ENOB represents the effective-number-of-bits and *P* is the power dissipation.

A more complete figure-of-merit, FM_2, includes the area, *A* (in mm^2) [2]

$$FM_2 = A \cdot FM_1 \quad \text{(pJmm}^2\text{)} \qquad (2)$$

Sigma-Delta (ΣΔ) architectures, either continuous-time (CT) [3] or switched-capacitor (SC) [4-6] can simultaneously achieve high *BW*, high resolution, and low power. Multi-bit SC implementations of ΣΔ modulators (ΣΔM) can reach FM_1 of the order of 0.5 pJ to 0.7 pJ [4-6] and FM_2=0.54 pJ·mm^2 is obtained in [4]; however, the decimation filter is not taken into account. In [3] a CT-ΣΔ realization includes the decimation filter which dissipates an additional power of 50% and occupies an area of 30% of the ΣΔM. A high energy efficiency with FM_1=0.3 pJ is measured, but when area is also taken into account we end up with FM_2=2 pJmm^2. The state-of-the art is that CT-ΣΔ are in general, 1.5 times more energy efficient than their SC counterparts, but less area efficient.

For signal BW above a few tens of MHz, self-calibrated pipeline ADCs have proved to be a better solution to minimize power. Although digital calibration does not require sophisticated analogue circuitry, it puts an extra burden on the digital part, and requires additional resolution in each stage, which results in increased area. A very energy efficient self-calibrated ADC can be found in [7], with FM_1=0.37 pJ, but the FM_2 is 1.18 pJmm^2, and the digital circuitry is not included. The ADC in [8] has FM_1=0.8 pJ and FM_2=0.8 pJmm^2 but, again, the digital self-calibration circuitry is implemented off-chip.

For ultra-low area, the best approach is to trade conversion-time for area. In this paper, a 2-stage algorithmic architecture is proposed in which a single amplifier is shared. Each stage uses a 1.5-bit mismatch-insensitive multiplying-DAC (1.5-bit MI-MDAC) for residue amplification. This 1.5-bit MI-MDAC is based in a multiply-by-two amplifier (MBTA) with an accurate gain of two and with parasitic compensation.

This paper is organized as follows. In section II the overall architecture and timing are presented. In section III the most relevant active blocks are described. Section IV describes the new 1.5-bit MI-MDAC. Section V presents simulation results which demonstrate that, in theory, FM_2 below 0.5 pJmm^2 can be targeted. Finally, section VI draws the main conclusions.

II. Architecture Description and Timing

The proposed architecture, depicted in Fig. 1, consists of a cascade of two stages. Each stage comprises a 1.5-bit MI-MDAC and a 1.5-bit flash-quantizer (FQ).

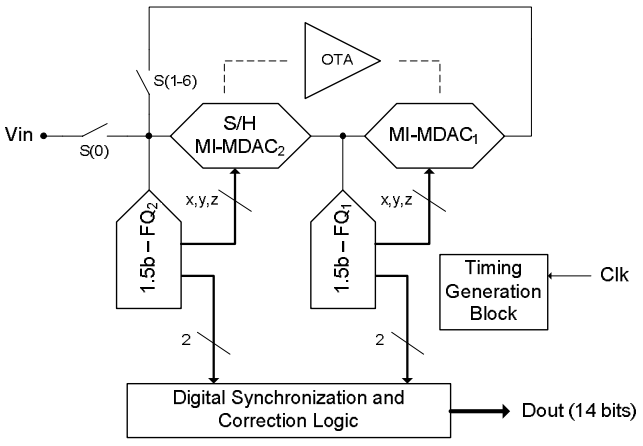


Fig.1: Proposed ADC architecture.

During the first clock cycle, $MDAC_2$ acts as a sample-and-hold (S/H) with a closed-loop gain of 2 and samples the dif-

ferential input signal. In the remaining 6 clock-cycles, the signal is successively recycled and amplified by 2 in an algorithmic manner. In each clock cycle, each 1.5-bit FQ provides 2 bits (4 bits total *per* clock cycle), and these bits are digitally synchronized and corrected, leading to a digital output with a net resolution of 14 bits. Since the two 1.5-bit MI-MDACs operate in opposite phases, they can share the same operational transconductance amplifier (OTA), allowing significant area and power savings. Moreover, since the failures in the comparators in the 1.5-bit FQs can be corrected digitally, the overall linearity of this A/D conversion architecture will be limited only by the gain accuracy of the 1.5-bit MI-MDACs (which should be accurately 2).

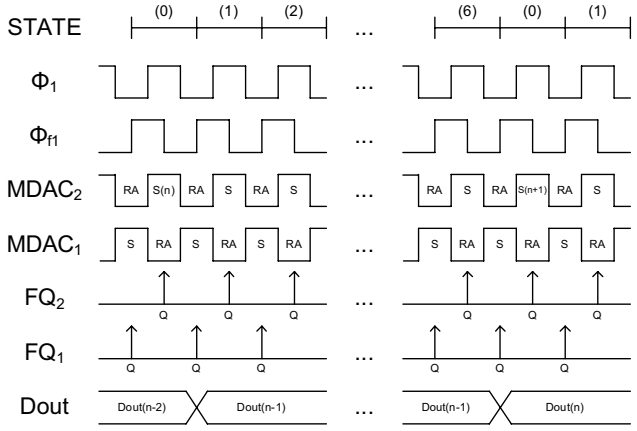


Fig. 2: Timing of operation of the different blocks of the ADC.

As stated before, to achieve simultaneously low power and low area, this architecture trades speed for low area. However, since two stages are used, this ADC has twice the speed efficiency of the conventional algorithmic architecture.

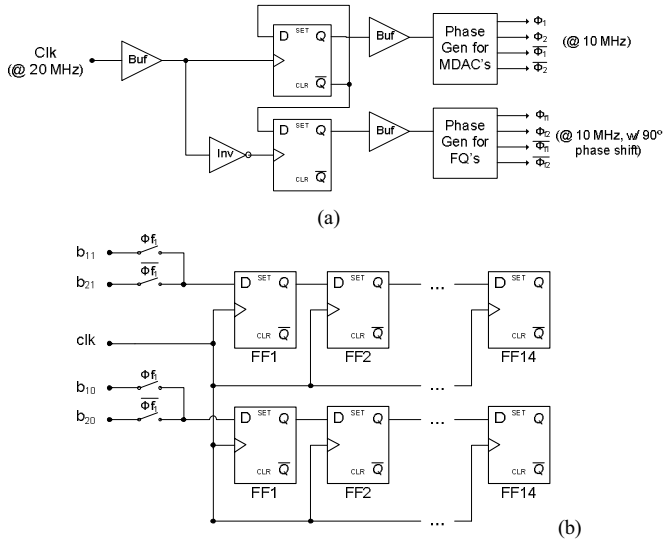


Fig. 3: (a) Clock phase generation; (b) Synchronization logic.

The output data latency and the timing of the different blocks are illustrated in Fig. 2. The 1.5-bit FQs quantize the input signal at the middle of the sampling phase of the 1.5-bit MI-MDACs. This allows more time for the amplifier to settle with the required accuracy, since, during the beginning of the residue amplification, the *x*, *y*, *z* digital signals provided by the 1.5-bit FQ are already available.

The clock phases shown in Fig. 2 are obtained using two D-type Flip-Flops (FFs), two standard non-overlapping clock-phase generators, and a few buffers, as depicted in Fig. 3(a). One FF is used to divide the input clock (@21.5 MHz) by 2, and the other is used to obtain a 90º phase shift in the clock phases supplied to the 1.5-bit FQs. Shift registers (based also on simple D-type FFs) are used to synchronize the data supplied by the FQs; they have to switch their inputs between FQ_1 and FQ_2 at the appropriate time, and this is done using CMOS switches to multiplex the bits, as shown in Fig. 3(b).

III. OTA AND COMPARATORS

The amplifier is shown in Fig. 4. To achieve high gain, a differential regulated folded-cascode structure is used for the input-stage (two auxiliary fully-differential single-stage folded-cascoded amplifiers, *SatN* and *SatP*, are used to boost the gain). The common-source second-stage increases the gain and, since it is fully differential, it allows the use of a single passive CMFB circuit.

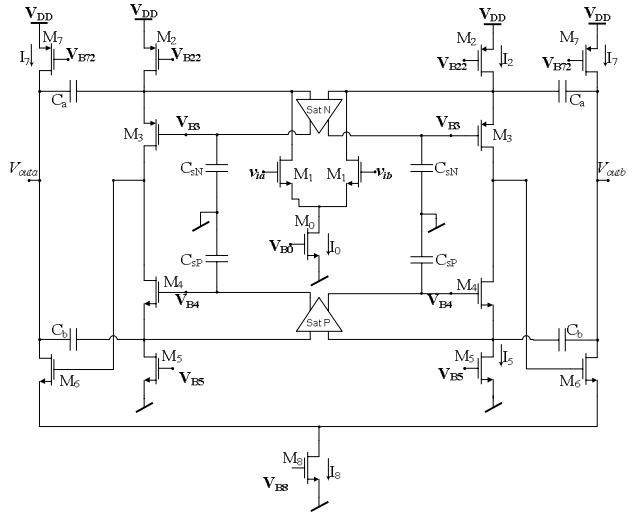


Fig. 4: Schematic of the 2-stage fully-differential OTA shared by both 1.5-b MI-MDACs (biasing and CMFB circuitry not shown).

In each signal path, two compensation capacitors, C_a and C_b provide hybrid cascaded-Miller compensation. Capacitors C_{sN} and C_{sP}, loading the auxiliary amplifiers, add an extra degree of freedom to control the frequency of the doublets (pole-zero pairs) caused by the gain-boosting loops. Optimization according to [9] leads to a settling time below 15ns and an error smaller than 20 µV is obtained by simulation (the simulated dc gain is higher than 100 dB in the most important PVT corners). Due to noise constraints, the sum of C_a and C_b is 8 pF and the complete amplifier dissipates only 8.4 mW. Fig. 5 shows the step response in a closed-loop with gain 2 of the OTA; the desired settling accuracy is within the available time slot. Two independent SC common-mode feedback circuits (CMFB) are used for the two stages.

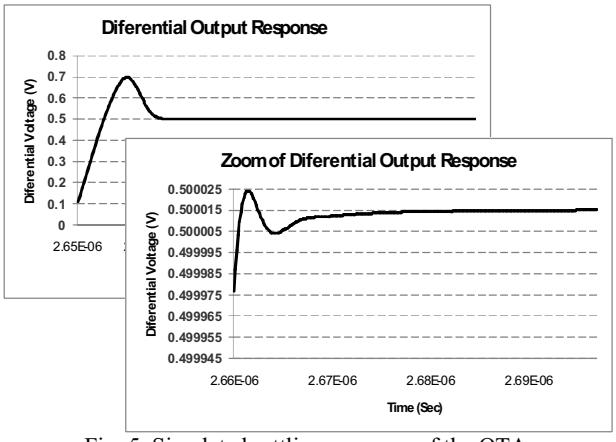


Fig. 5: Simulated settling-response of the OTA.

Each 1.5-bit FQ consists of 2 comparators followed by a thermometer-to-binary digital encoder and by a *x*, *y*, *z* encoder. Each comparator comprises an input SC divider network to define the threshold level, followed by an ordinary a dynamic preamplifier/positive-feedback latch. This comparator was optimized using exhaustive Monte-Carlo simulations in order to achieve low-offset (low enough to be corrected by the digital correction logic), reduced kickback noise, high mean-time to failure, and low-power dissipation at the desired speed of operation.

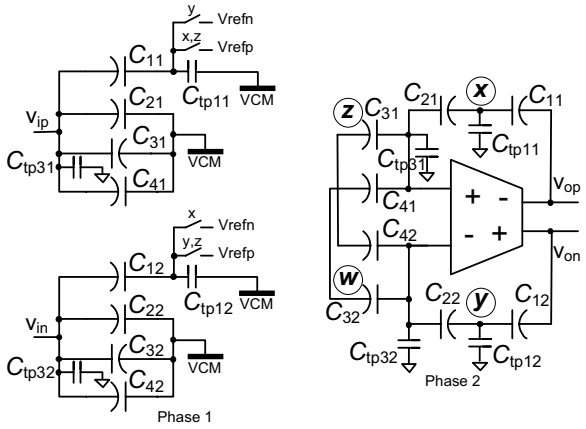
IV. The Mismatch-Insensitive Multiplying DAC

High-resolution architectures of ADCs, such as pipeline and algorithmic, often employ MI-MDACs based on SC amplifiers with gain 2 (MBTA circuits). Since the linearity of high-resolution ADCs (e.g., above 10 bits) is usually limited by the accuracy of these gain blocks, it is mandatory to use self-calibration [10, 11] or, alternatively, to employ active [12, 13] or passive [14] capacitor error-averaging techniques. However, all these solutions either increase hardware complexity (e.g., digital self-calibration circuitry), or they trade speed for accuracy, by using more than one clock cycle to provide the accurate amplified value. We use instead a practical 1.5-bit MI-MDAC based on some modifications made to the mismatch-insensitive MBTA described in detail in [15].

Fig. 6 shows the schematic in the two different clock phases of the new 1.5-bit MI-MDAC, based on the MBTA circuit in [15].

As depicted in Fig. 6(a), during phase ϕ_1, capacitors C_{11}, C_{21}, C_{12} and C_{22} sample the differential input signal, v_{id}, into the bottom-plates. In this scheme, the top-plates of capacitors C_{11} and C_{12} are not connected to the common-mode voltage (VCM), but rather to V_{REFP} or to V_{REFN}, depending on the *x*, *y* and *z* outputs provided by the corresponding 1.5-bit FQ in this phase.

During the amplification phase, ϕ_2, as illustrated in Fig. 6(b), capacitors C_{11} and C_{21} in series, are used as feedback element in the positive path. Likewise, C_{12} and C_{22} are connected in series in the other signal path. Neglecting initially, for the sake of simplicity, the effects of parasitic capacitances (C_{tp11} and C_{tp12}), but allowing the main capacitances to be mismatched, the differential output voltage, v_{od}, at the end of the amplification phase, ϕ_2, is exactly $v_{od} = 2v_{id}$. However, the circuit comprising only the referred 4 capacitors, is highly sensitive to the top-plate parasitic capacitance (TPPC) of capacitors C_{11} and C_{12}, C_{tp11} and C_{tp12}, respectively.



(a) *(b)*

Fig. 6: Two-phases of the 1.5-bit MI-MDAC: (a) sampling-phase; (b) residue-amplification.

As demonstrated in [15], to reach a completely stray-insensitive circuit, besides the main capacitors (C_{11}, C_{21}, C_{12}, and C_{22}), four auxiliary half-sized capacitors (C_{31}, C_{32}, C_{41}, and C_{42}) are used to compensate the TPPC of capacitors C_{11} and C_{12}. During the sampling-phase ϕ_1, capacitors C_{31} and C_{32} charge their TPPCs, respectively, C_{tp31} and C_{tp32} (expected to be half of values of C_{tp11} and C_{tp12}), to the differential input voltage (top-plate sampling). In the amplification phase, ϕ_2, the top-plates of C_{31} and C_{32} are connected to the inverting and non-inverting inputs of the OTA and, consequently, there is an opposite amount of charge which will cancel out the parasitic effects of C_{tp11} and C_{tp12}.

As shown in [15] (for *z*="1"), if the parasitic capacitances are not considered, the differential output voltage is precisely $v_{od} = 2v_{id}$. With parasitics, we have

$$v_{od} \approx 2v_{id}\left[1+\frac{1}{8}\frac{\alpha(2\varepsilon_{P11}-2\varepsilon_{P31}-\varepsilon_{11}+\varepsilon_{21}+\alpha)}{1+\varepsilon_{11}+\varepsilon_{21}+\varepsilon_{11}\varepsilon_{21}}+\frac{1}{8}\frac{\alpha(2\varepsilon_{P12}-2\varepsilon_{P32}-\varepsilon_{12}+\varepsilon_{22}+\alpha)}{1+\varepsilon_{12}+\varepsilon_{22}+\varepsilon_{12}\varepsilon_{22}}\right] \quad (3)$$

where ε_{ij} are the random mismatches of the main and auxiliary capacitors, ε_{Pij} are the random mismatches of the top-plate parasitic capacitors and α represents the average relative TPPC for the selected fabrication process.

In this equation, the first and second-order terms are kept but higher-order errors are neglected. This shows that the gain error becomes dependent on the products of the TPPC factor, α, and the mismatch errors of main and parasitic capacitances. Typical values in deep sub-micron CMOS technologies (*e.g.* 130nm) with Metal-Insulator-Metal (MiM) capacitors are $\sigma(\varepsilon_{ij}) = 0.2\%$, $\sigma(\varepsilon_{Pij}) = 2\%$, and $\alpha = 0.25\%$. As shown

in [15], the proposed circuit can, in theory, reduce the gain error from 0.1% down to 0.005%, when compared with the conventional circuit. This means a gain accuracy enhancement of 4 to 5 bits. Although auxiliary capacitors C_{31} and C_{32} sample the input voltage, they do not affect either the transfer function or the final gain accuracy. The reason is that capacitors C_{41} and C_{42} cancel out their charge and, they are also connected in series during the amplification phase in order to cancel any mismatch effects.

V. Circuit Implementation and Simulation Results

An integrated prototype of the 1.2 V, 14-bit, 1.54 MS/s 2-stage algorithmic ADC was designed in a 130nm 1P-8M CMOS technology with special MiM capacitor option. Fig. 7 shows a plot of the layout. To achieve an input full-scale of 1 V_{p-p} (differential) voltages V_{REFP}=VCM=0.8 V, V_{REFN}=0.3 V and V_{CMO}=0.55 V are provided to the ADC. Dedicated switch-linearization control circuits (SLCs) are used to improve the conductivity of the most critical switches [16]. The active area of the complete ADC is about 0.36 mm^2. Fig. 8 displays the FFT (256 bins) of the ADC output clocked at 10.75 MHz (after divided by 2) when a full-scale input of 534 kHz is applied. A peak SNR of 77 dB is obtained through analytical calculations when 4 pF unit capacitors are used to make C_{11}=C_{21}=C_{12}=C_{22}=8 pF, C_{31}=C_{32}=C_{41}=C_{42}=4 pF and C_a=C_b=4 pF. Simulations show a THD of –79.4 dB, a SFDR of 82 dB, and a peak SNDR larger than 75 dB corresponding to an ENOB better than 12.2 bits. The circuit dissipates less than 10 mW with 1.2 V and at 1.536 MS/s corresponding to, in theory (still to be verified experimentally), an area-and-energy efficiency better than 0.5 pJmm^2.

VI. Conclusions

This paper described a 14-bit medium conversion-rate two-stage algorithmic ADC with a very high power-and-area efficiency. The 2 stages of the ADC are based on a new 1.5-bit MI-MDAC and simulations show that a THD of –79 dB and an ENOB better than 12 bits can be reached without any self-calibration scheme, which makes this design a better alternative to ΣΔ and self-calibrated pipeline ADCs.

Acknowledgements

This work was partially supported by the Portuguese Foundation for Science and Technology (FCT/MCT) under Projects LEADER and SIPHASE.

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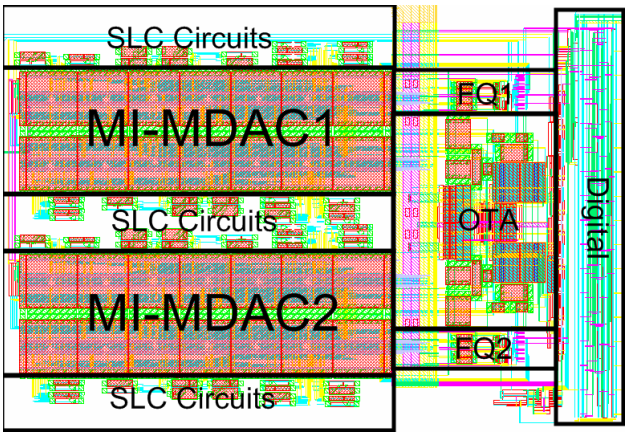

Fig. 7: Plot of the layout of the 14-bit 1.5MS/s 2-stage ADC.

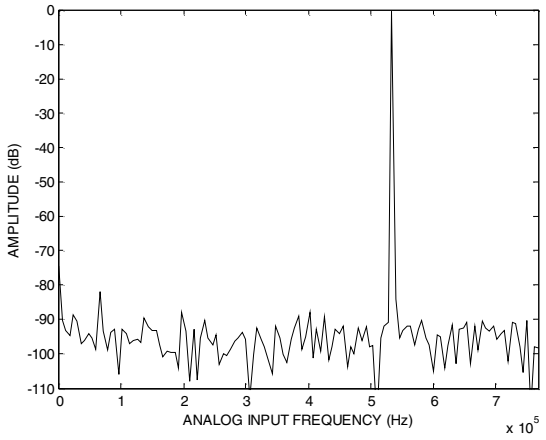

Fig. 8: Simulated FFT Spectrum with 256 bits for f_{clk}=10.752 MHz and f_{in}=534 kHz (coherent sampling).