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A MULTIPLYING-BY-TWO CMOS AMPLFIFIER FOR HIGH-SPEED ADCS BASED ON PARAMETRIC AMPLIFICATION

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ABSTRACT: In this paper a new structure for a multiplying-by-two amplifier is proposed. It is implemented by switching MOS capacitors with floating sources from inversion into depletion dropping the capacitance values in the amplification phase. Low-power is achieved since no operational amplifiers are required but, instead, simple source-followers are used to provide the required isolation. Simulation results show that linearity levels better than 60dB and gain accuracies of better than 1.6% are achieved making this circuit well suited to be used in ultra low-power high-speed 6-to-8 bits pipeline or multi-stage algorithmic ADCs.

INTRODUCTION

Next generation communications based on impulse radio Ultra-Wideband systems are targeted either for high data rate transfer or ultra-low power low data rate wireless sensor receivers [1]. In these applications, sampling-rates of the order of a few hundred of mega-samples per second (MSPS) together with resolutions of about 6 bits are specified for the Analog-to-Digital Converters [2].

Pipeline ADCs can achieve very high-speeds with low power dissipation. However, their energy efficiency is much dependent on the optimum resolution-per-stage, on the scaling of the capacitance values and in the residue-amplifier topology used in the multiplying digital-to-analog converters (MDACs) of the pipeline stages. In closed-loop approaches, amplifiers with very high gain-bandwidth products have to be designed which dissipate a significant amount of power.

Parallel pipeline ADCs have been used to achieve medium resolutions at very high sampling rates [3, 4]. Also sharing some common blocks between two or more parallel ADCs, in a time-interleaved fashion can reduce the total power. The closed-loop multiply-by-two residue amplifiers usually integrated in the pipeline ADCs can be replaced by open-loop amplifiers [5, 6], reducing global size and power. However, it becomes mandatory to employ either digital gain-calibration [5] or employ replica circuits for implementing global-gain control techniques [7].

The work presented here, shows for the first time, a mul-tiply-by-two residue amplifier (MBTA) implemented by switching a MOS capacitor from inversion into depletion within a clock-cycle (parametric amplification) using a new MOSCAP parametric amplifier configuration, [8, 9]. This circuit is well suited for ultra low-power high-speed 6-to-8 bits pipeline or multi-stage algorithmic ADCs. Moreover, low-power is achieved since amplifiers are no longer required in the high-frequency signal path, and just simple source-followers are used for isolation between stages.

LOW-GAIN PARAMETRIC AMPLIFIER

A MBTA can be implemented around a parametric MOS amplification configuration described in [8, 9] where a discrete-time amplifier was evaluated. In this amplifier, the gain is set through the reduction of the total equivalent gate capacitance of a single MOSCAP device, while maintaining the total gate charge between the sampling and the amplification phase. As explained in [8, 9], the capacitance reduction of a MOSCAP can be achieved by moving it from inversion into depletion, as result of changing the control voltage ($V_{control}$) applied to the drain from the lower power supply voltage (V_{SS}) to the positive power supply (V_{DD}), as shown in Figs.1 (a) and (b).

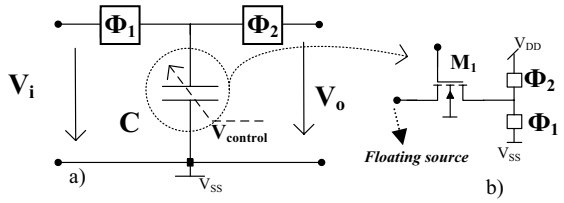

Fig. 1.(a) MOSCAP parametric amplifier; (b) MOSCAP implementation with floating source

The MOS parametric amplifier (MPA) circuit operates as follows. During phase Φ_1 the input signal is sampled by M_1 and a corresponding charge is stored. Considering that, in Φ_2 both gate charges remain constant (gates are floating), the gate voltage will change by a gain of, approximately, $v_o/v_i = C_{ox}/C_{gb}$, where C_{ox} is the total gate-oxide capacitance and C_{gb} is the gate-bulk capacitance during the amplification phase [9].

The main differences of the basic MOSCAP structure used here from the one used in [8, 9] lies on the fact that 2 half-sized MOSCAPs are used instead of a single one and, on the other hand, their short-circuited sources are left floating.

The main advantage of this structure is that it decreases the total gate capacitance during the amplification phase

since half of the value is left floating. Hence, the total loading capacitance in Φ_2 is reduced by half, and amplification gains above 4 (without load) can now be easily achieved with an nMOS-type MOSCAP (nMOSCAP) which is of paramount importance to allow the practical implementation of an overall gain of 2 for a complete MBTA. A simulation of the obtainable gain is shown in Fig. 2 by electrical simulations of the circuit shown in Fig. 1.

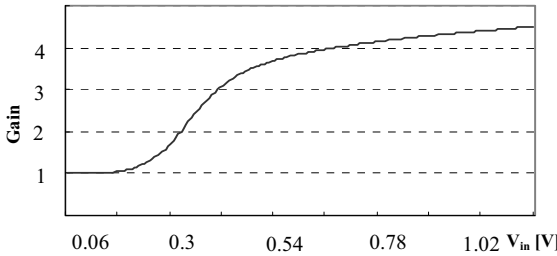

Fig. 2. Parametric amplifier gain as a function of the input DC level and without any load.

Fig. 2 also shows that the achieved gain depends on the common-mode level of the input voltage reflecting on how well the MOS device is in inversion state during the sampling phase. Therefore an appropriate DC level should be carefully chosen. Another problem to be solved is related with the existing DC level-shifting that occurs when an nMOSCAP (C_{1N}) changes from inversion into depletion. To avoid this level rise (which tends to be higher than V_{DD}) during the amplification phase, an additional pMOS-type MOSCAP (pMOSCAP), C_{2P}, should be added as shown in Fig. 3 in order to produce the opposite effect (negative DC level shifting).

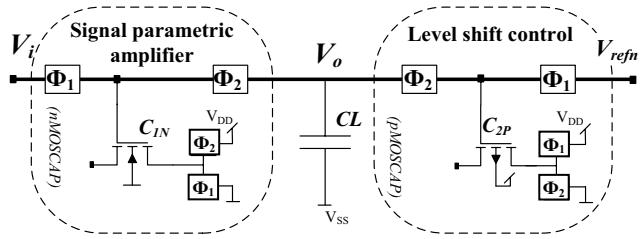

Fig. 3. CMOS discrete-time amplifier (MPA block) with output level shift control.

A first-order charge redistribution analysis applied to the described MOS Parametric Amplifier (MPA), results in an equation for the output voltage approximately given by

$$V_O \approx \frac{\alpha_{C1n}}{k} V_i + \frac{\alpha_2 - \alpha_4}{k} V_{DD} + \frac{\alpha_4}{k} V_{refn} + \frac{\alpha_3}{k} V_{CL,\phi 1} \quad (1)$$

where $C_{1N,\phi 1} = \alpha_{C1N} \cdot C_{1N,\phi 2}$, $C_{2P,\phi 2} = \alpha_2 \cdot C_{1N,\phi 2}$, $C_L = \alpha_3 \cdot C_{1N,\phi 2}$, $C_{2P,\phi 1} = \alpha_4 \cdot C_{1N,\phi 2}$ and $k = 1 + \alpha_2 + \alpha_3$.

Parameter k models the gain reduction due to the load parasitic capacitance C_L and C_{2P} during phase Φ_2. Parameter α_{C1N} reflects the capacitance variation from phase Φ_1 to phase Φ_2 for C_{1N}. Parameter α_2 represents the relation between C_{2P}, during phase Φ_2, and C_{1N} in phase Φ_1. The remaining parameters α_3 and α_4 describe the ratio of C_L and C_{2P} in phase Φ_2 with respect to the value of C_{1N} during phase Φ_2.

Equation (1) demonstrates that, besides a desired multiplying factor, the output voltage has an offset component partially controlled by the pMOSCAP. It also shows that the load parasitic capacitance, C_L affects the final gain of the circuit and the output offset level (depending on how the voltage is applied to C_L during Φ_1, $V_{CL,\Phi 1}$). To reduce this loading capacitance effect, a simple source-follower can be inserted at the parametric amplifier output node. This source-follower is also useful to buffer the output when this amplifying stage is loaded by another circuit or amplifier. Next section will describe the design of a MBTA based on the CMOS discrete time amplifier represented in Fig. 3.

MBTA CIRCUIT DESIGN

Circuit architecture

The proposed structure for the MBTA, represented in Fig. 4, comprises four single-ended MPA (n and p type respectively for the positive and negative signal paths) and two source-follower circuits. As stated before, these buffers are required to isolate the loading effect of the next stage (e.g., in a pipeline ADC). The schematic of each MPA block is depicted in Fig. 5.

Moreover, a time interleaved operation is easily implemented due to the discrete-time nature of the proposed MPA, meeting the requirements for high speed operation. A replica-bias circuit which, will be described later is used to provide the required bias voltage, V_{bias}, for the pMOS current sources in the source-followers.

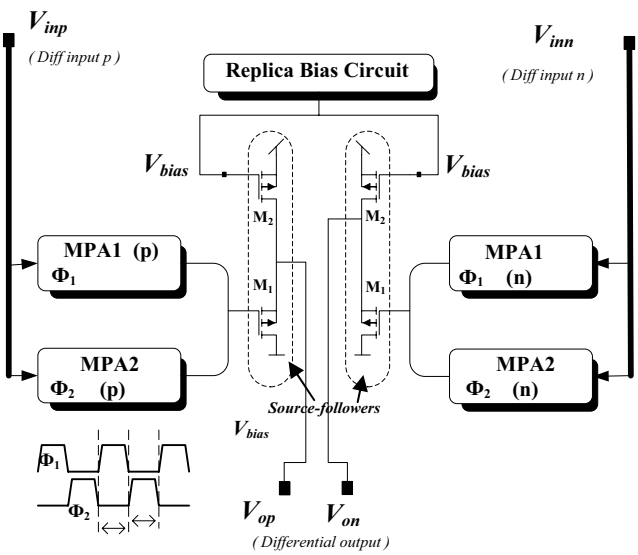

Fig. 4. Four MPA connected in a time interleaved structure.

The schematic of the MPA circuit shown in Fig. 5 corresponds to the pmos version. During phase Φ_1, the input signal is sampled into C_1, the positive reference voltage (V_{refp}) is sampled into C_2. In the parametric amplification phase, Φ_2, the capacitance values of C_1 and C_2 decrease due to the change from inversion into depletion region and are connected to the source-follower input for charge re-distribution.

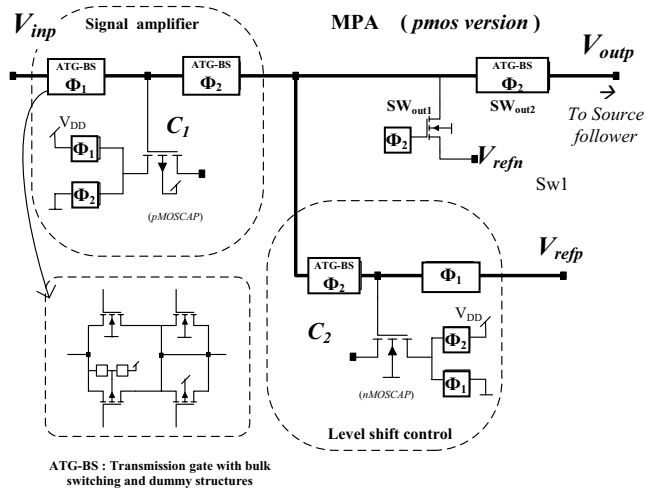

Fig. 5. Half MPA single-ended circuit (p version).

Applying, to this MPA, the same methodology used for the parametric amplifier transfer function, results in a similar equation to (1) where a new factor appears to take into account the source follower gain (lower than one). Additionally, when considering a differential output voltage, the common-mode components present in (1) are removed, resulting in a final expression for the differential voltage, V_{od}, at the outputs of the source-followers given by:

$$V_{od} \approx \frac{g_{m1}}{g_{m1}+g_{sb1}} \cdot \left(\frac{\alpha_{C1n}}{k} V_{id}\right) \qquad (2)$$

where $C_{1,\phi 1} = \alpha_{C1} \cdot C_{1,\phi 2}$, $C_{2,\phi 2} = \alpha_2 \cdot C_{1,\phi 2}$, $C_L = \alpha_3 \cdot C_{1,\phi 2}$, $C_{2,\phi 1} = \alpha_4 \cdot C_{1,\phi 2}$ and $k = 1 + \alpha_2 + \alpha_3$. Transconductances g_{m1} and g_{sb1} represent, respectively, the main and body-effect transconductances of the main device of the source-follower (M_1).

In (2), it has been assumed that all MPAs have equally sized transistors and equal load capacitance from the source followers.

Note that, due to the body-effect of the source-followers, their gain is smaller than one. Hence, to compensate this effect the complete MBTA circuit transistors are adjusted and sized to have a gain factor precisely equal to two.

Switches connected to the amplifier input and output signals are implemented with asymmetric transmission-gates employing bulk-switching (ATG-BS), switches connected to the constant reference voltage (V_{refp},V_{refn}, V_{DD}, V_{SS}) are simply MOS transistors. All switches connected to the input signal have dummy structures to reduce signal-dependent charge injection.

Switches SW_{out1} and SW_{out2}, are used to remove any memory effects that might appear due to the interleaved operation.

Replica-bias circuit output common-mode control

Another important aspect is that the output common-mode voltage (VCMO) at the outputs of the source-followers can not vary too much in order, for example, to avoid DC accumulation errors in subsequent stages (e.g., again in a pipeline ADC). A replica-bias circuit as the one depicted in Fig. 6 is used to guarantee that VCMO is restored at the MBTA output and adjusted to a proper value against process and supply variations.

It comprises two time-interleaved MPAs connected to a same replica source-follower. The average voltage at the buffer output is set and controlled by a negative feedback loop which includes a very simple amplifier. The objective is to replicate the operation of the differential MPA and controlling the common mode voltage present at the MPAs buffers outputs through a biasing voltage V_{bias}. As referred before, stabilizing the output common-mode component at the outputs of each stage prevents DC accumulation along the pipeline. Note that the OTA used here does not need a high bandwidth since it is not inserted in the main signal path. Therefore it can be designed with minimum biasing current (20µA was used).

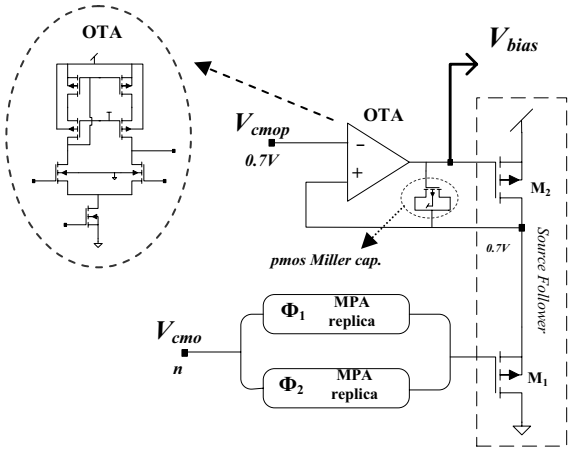

Fig. 6. Replica bias block used to generate V_{bias} for the 2 source-followers used in the MBTA block.

For an input differential signal full-scale swing of 400 mVp-p, V_{refp} of 1V and V_{refn} of 0V, the values of 0.4V and 0.7V were found to be optimal for the common mode components V_{cmon} and V_{cmop}, respectively.

SIMULATED RESULTS

The proposed parametric amplifier based MBTA circuit was designed and simulated at transistor level in a standard 130 nm CMOS technology. The simulation was performed in *Spectre/Cadence* electrical simulator using BSIM3v3 CMOS model. Fig. 7 displays the differential signal present at the MBTA output when a differential signal of 10MHz and 190mVp-p is injected at the input. The overall MBTA circuit is sampling the input signal at 100MHz. A gain error of 1.62% error was obtained for typical conditions, with is compatible to a 7bit level accuracy.

The output signal spectrum is represented in Fig. 8. It is based in a 512-bin FFT (coherent sampling) of the amplifier output when a sampling frequency of 100.0448MHz is used and a 10.388MHz input differential signal of 190mVp-p is injected at the input. A load capacitance of 250fF was considered at the amplifier output node. Simulations results exhibit a THD better than -60dB.

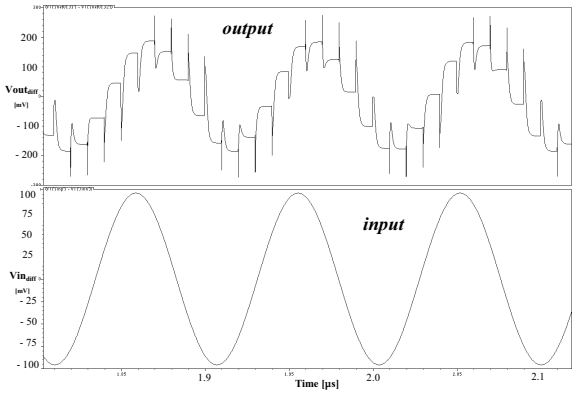

Fig. 7 .Differential output and input of the MBTA.

The complete circuit dissipates only 1mW (RMS; V_{DD}=1.2V) in typical conditions which indicates the power efficiency achieved by the proposed MBTA circuit topology. Table 1 summarizes the simulated results.

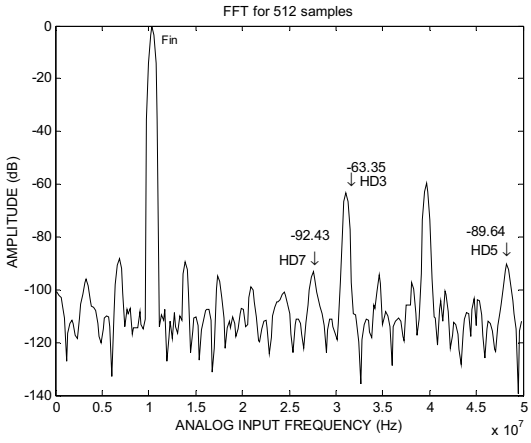

Fig. 8. Simulated FFT spectrum of the output signal for the proposed MBTA circuit operating at 100MHz for 10MHz input signal.

TABLE 1: Summary of the MBTA performance

Item	*Value*
Technology	130 nm CMOS
Supply voltage	1.2 V
RMS Power dissipation per comparator @ Fs=100MS/s	< 1mW
THD (Fin=10MHZ) @ FS=100MS/s	< -60dB
Gain-error	1.62%

CONCLUSIONS

In this paper a new structure for a MBTA was proposed. It is implemented by switching MOS capacitors with floating sources from inversion into depletion dropping the capacitance values in the amplification phase. Low-power is achieved since no operational amplifiers are required but, instead, simple source-followers were used to provide the required isolation. Simulation results show that linearity levels better than 60dB and gain accuracies of better than 1.6% were achieved making this circuit well suited to be used in ultra low-power high-speed 6-to-8 bits ADCs.

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