# Write-erase and read paper memory transistor

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We report the architecture and the performances of a memory based on a single field-effect transistor built on paper able to write-erase and read. The device is composed of natural multilayer cellulose fibers that simultaneously act as structural support and gate dielectric; active and passive multicomponent amorphous oxides that work as the channel and gate electrode layers, respectively, complemented by the use of patterned metal layers as source/drain electrodes. The devices exhibit a large counterclockwise hysteresis associated with the memory effect, with a turn-on voltage shift between 1 and −14.5 V, on/off ratio and saturation mobilities of about $10^4$ and 40 $cm^2\ V^{-1}\ s^{-1}$, respectively, and estimated charge retention times above 14 000 h. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3030873]

Nowadays the microelectronics industry is demanding for inexpensive, lightweight, and disposable memory devices. This has been pushing research toward the use of low cost materials and devices whose structures are easily fabricated at low temperatures and with low energy consumption. This demand is mainly fulfilled by organic devices and several attempts have been made to use them as memories: to write and read information,[1] for random access memory circuits for storing and retrieving information,[2] and nonvolatile memories.[3] Nevertheless, all these organic memory devices still suffer from a low carrier mobility (below 3–7 $cm^2\ V^{-1}\ s^{-1}$) that limits the device switching time and exhibit low charge retention times (4500 s)[3] that restricts their field of applications. Up to now, paper has been mainly used either as substrate in organic thin-film transistors (TFTs)[4], logic circuits,[5] and electrochromic displays,[6] or in thin-film flexible Li batteries.[7] Here we show the possibility to use multilayer mechanically compact natural cellulose fibers (paper) simultaneously as structural support and dielectric in *n*-type memory field-effect transistors able to write-erase and read (WERM-FETs). The channel and gate electrode layers are respectively based on active and passive multicomponent amorphous oxides such as gallium indium zinc oxide (GIZO)[8] and indium zinc oxide (IZO).[9]

The WERM-FETs were fabricated at room temperature in a three step process described elsewhere,[10] using paper from Renova[11] composed by long pine fibers mixed with polyester fibers, embedded in a matrix of an ionic resin and adhesive glue to give the need mechanical stiffness. The paper surface was treated with an amylaceous solution to make it hydrophobic. On one side of the paper sheet (55 $\mu$m thick), a 40 nm thick amorphous GIZO ($Ga_2O_3$–$In_2O_3$–ZnO; 1:2:1 mol %) deposited by rf magnetron sputtering coats the surface of the fibers (acting as the channel layer). This was followed by e-beam assisted evaporation of the Al or Au source/drain thick electrodes that connect all fibers over the edges of the patterned channel region, using shadow masks with a width-to-length ratio of 2165/216 $\mu$m, see Fig. 1(a). After, the paper is turned upside down, allowing to deposit on its backside, also by rf magnetron sputtering, a thick IZO ($In_2O_3$–ZnO; 5:2 mol %) film, aiming to achieve a continuous gate electrode, exhibiting typically an electrical resistivity below $10^{-3}\ \Omega$ cm, depending on the substrate used.[9,10,12] The procedures described reduce the effective device thickness when compared with the geometric paper thickness and introduce the concept of a noncontinuous dielectric network that allows a substantial

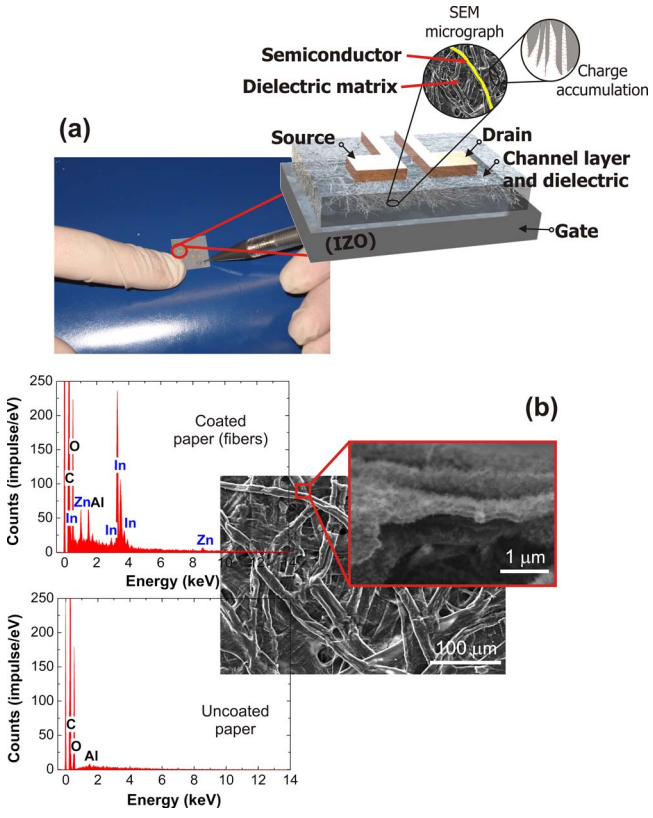


FIG. 1. (Color online) (a) Schematic of the device's structure. The magnified inset shows a photo of the real device and the fibers that constitute the dielectric structure. (b) SEM image and EDXS analysis of paper's surface and a magnification of a paper cross section, revealing the paper multilayer structure.

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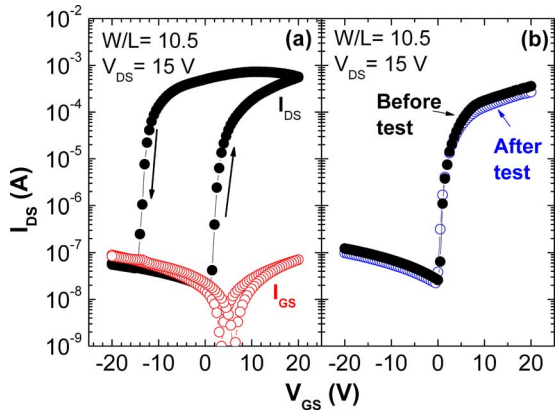


FIG. 2. (Color online) Transfer characteristics of the WERM-FET. (a) Double sweep measurements. (b) Transfer characteristic before and after the write-erase stress test.

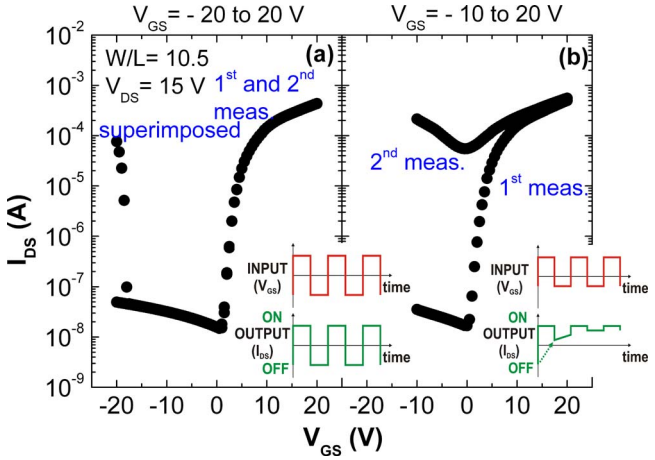


FIG. 3. (Color online) Successive single sweep transfer characteristics of the WERM-FET for (a) symmetric (−20 to 20 V) and (b) asymmetric (−10 to 20 V) $V_{GS}$ ranges. The insets show schematics for input ($V_{GS}$) and output ($I_{DS}$) signals for each $V_{GS}$ range.

enhancement on the device capacitance per unit area ($C/A$), in opposition to what is known, e.g., in nanowire TFTs, where conductive wires are embedded in a continuous dielectric.[13]

The paper surface morphology and composition before and after oxide coating was observed by scanning electron microscopy (SEM) using a SU-70 FE from Hitachi, equipped with energy dispersive x-ray spectroscopy (EDXS) analysis [Fig. 1(b)]. The SEM images reveal fibers with average widths of 8–10 $\mu$m and thicknesses of about 1–2 $\mu$m, randomly distributed. The EDXS analysis was performed in papers coated with IZO oxide in one side and uncoated in the other side. The data reveal the presence of IZO on the coated side and not on the uncoated one, as can be seen. The composition analysis is hard to be performed along the fibers due to the nature of the fibers that deteriorate for higher magnifications, leading to the fracture of the oxide film.[10]

The geometrical paper $(C/A)_g$ and the corresponding dielectric constant ($k_{\text{eff}}$) were measured using a precision impedance analyzer (Agilent 4294 A), depositing on both sides of the paper thick Al metal contacts, in one area of 2.45 $\times 2.45$ cm$^2$. The data led to $k_{\text{eff}} \cong 13 \pm 2$[14] to which it corresponds a $(C/A)_g$ of 0.18–0.24 nF cm$^{-2}$. The devices were electrically characterized in air, in the dark, and at room temperature using an Agilent 4155C semiconductor parameter analyzer. For the write-erase stress test, a symmetric square wave pulse with a peak to peak voltage of 20 V and an offset of 0 V at 1 Hz was applied to the gate electrode.

Figure 1 shows the device structure. The operation of the memory device relies on the capacity of the fibers to accumulate an enormous number of charges due to their structure with gaps between highly electrical resistive and randomly distributed fibers. The electronic transfer characteristics of the device are shown in Figs. 2 and 3. Figure 2(a) reveals a large drain-to-source current ($I_{DS}$) counterclockwise hysteresis with a turn-on voltage ($V_{on}$) shift from 1 to −14.5 V, a subthreshold swing ($S$) around 0.65 V/decade, on/off ratio of $10^4$, and gate leakage current ($I_{GS}$) at $|V_{GS}|=20$ V of $10^{-7}$ A. $I_{DS}$ remains almost constant ($\approx 0.55$ mA) for $-10\ \text{V} < V_{GS} < 20$ V due to the memory effect (on-state). When $V_{GS} < -15$ V, $I_{DS}$ is reduced by more than three orders of magnitude (off-state). This high-to-low $V_{GS}$ cycle corresponds to write and to erase the information (charges) stored in the device and is fully reproducible as long as symmetric $V_{GS}$ are used for the on and off-states, as explained below.

The high $I_{DS}$ are not explained by the $(C/A)_g$ measured values, which should lead to much lower $I_{DS}$. The $I_{DS}$ recorded are explained by the enhancement on $(C/A)_d$ due to the discrete dielectric, constituted by interconnected coated and uncoated fibers, forming a multilayer structure. Thus, the $(C/A)_d$ to be determined should correspond to the contribution of interconnected fibers distributed along the paper thickness. These conditions lead to an effective decrease of the device thickness and to a $(C/A)$ that depends on how fibers are associated, defining the carrier's path and so the charge induced process when a voltage is applied to the gate electrode. Based on that and assuming the fibers with a parallelepiped-shape (to decrease the complexity of the model), $(C/A)_d$ can be estimated as

$$\left(\frac{C}{A}\right)_d \approx \frac{1}{2} \times \frac{a}{b} \times \frac{W}{d} \times \left(\frac{C}{A}\right)_f \times F, \tag{1}$$

where $a$ and $b$ are the average thickness and width of the fibers, respectively, $d$ is the paper's thickness, $W$ is the channel width, and $F$ ($<1$) is the compactness ratio among fibers into the same layers and along the set of layers that form the multilayer paper structure. Taking into account the average sizes of the fibers and the measured $k_{\text{eff}}$, we obtain 6.5 nF cm$^{-2} < (C/A)_f < 8.9$ nF cm$^{-2}$ and 17.0 nF cm$^{-2}$ $< (C/A)_d < 23.2$ nF cm$^{-2}$, about two orders of magnitude larger than $(C/A)_g$. These values explain the high $I_{DS}$ obtained, leading to a saturation mobility ($\mu_S$), around 40 cm$^2$ V$^{-1}$ s$^{-1}$, closer to those expected for GIZO based TFTs.[8]

Stress tests performed by cycling the device between the on- and off-states for 1 h (more than $10^3$ cycles) reveal that the transfer characteristics do not significantly change, as depicted in Fig. 2(b). The analysis of the data shows that $\mu_s$ slightly decreases, while $S$ and $V_{on}$ maintain the same values, meaning that the WERM-FET is highly stable. However, if the absolute value of the off-state $V_{GS}(erase) <$ on-state $V_{GS}(write)$, the charges trapped/stored along the fibers sustain the electrons' accumulation layer in the channel region, avoiding the pull down of $I_{DS}$ toward its expected off-state

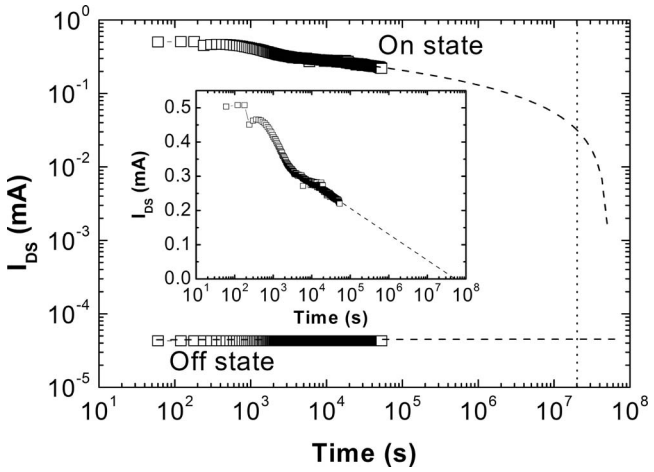


FIG. 4. Log-log plot of the on-state current vs time taken after a single sweep transfer characteristic and after opening the gate electrode terminal, keeping $V_{DS}$=15 V. The inset shows the same data, now using a semilog plot.

value (see Fig. 3). This leads to a small difference between on and off-states (on/off ratio close to 1), meaning that the on-state cannot be *erased* unless a symmetric $V_{GS}$ to the one used for *writing* the information is applied.

To demonstrate the WERM-FET storage capacity, after changing the device from off- to the on-state (write operation), the gate electrode terminal was opened and $I_{DS}$ evolution with time monitored for more than 15 h, keeping the drain voltage ($V_{DS}$) constant (15 V), see Fig. 4. As expected, the data reveal an exponential dependence of the current as a function of time.[15] The extrapolation of these data reveal that even after $5\times10^7$ s (almost 14 000 h, more than 1.5 years), the current differential is still $>10\times$ between the on- and off-state, which is adequate for modern sense amps, depending on the architecture of the memory.[15] After 4 months of fabrication, the electronic performances of the WERM-FET do not change, showing that they are environmentally stable, even without any passivation or encapsulation layers over the semiconductor surface.

In summary, the electronic characteristics of the WERM-FET are dependent on the discrete dielectric arrangements along the multilayers that constitute the paper, which determines the device performances, such as high $I_{DS}$, high stability, very low operating bias, high mobility, and high charge retention time. These characteristics outpace those of organic memory devices and rival with the ones obtained on conventional oxide TFTs.[8] The compatibility of these low cost self-sustained devices with conventional fabrication deposition techniques delineates a promising approach of using natural multilayer cellulose fiber paper on low cost high-performance flexible and disposable memories.

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[1] S. Moller, C. Perlov, W. Jackson, C. Taussig, and S. R. Forrest, Nature (London) **426**, 166 (2003).
[2] J. E. Green, J. W. Choi, A. Boukai, Y. Bunimovich, E. Johnston-Halperin, E. DeIonno, Y. Luo, B. A. Sheriff, K. Xu, Y. S. Shin, H. R. Tseng, J. F. Stoddart, and J. R. Heath, Nature (London) **445**, 414 (2007).
[3] J. C. Scott and L. D. Bozano, Adv. Mater. (Weinheim, Ger.) **19**, 1452 (2007).
[4] Y. H. Kim, D. G. Moon, and J. I. Han, IEEE Electron Device Lett. **25**, 702 (2004).
[5] D. Nilsson, N. Robinson, M. Berggren, and R. Forchheimer, Adv. Mater. (Weinheim, Ger.) **17**, 353 (2005).
[6] P. Andersson, D. Nilsson, P. O. Svensson, M. X. Chen, A. Malmstrom, T. Remonen, T. Kugler, and M. Berggren, Adv. Mater. (Weinheim, Ger.) **14**, 1460 (2002).
[7] V. L. Pushparaj, M. M. Shaijumon, A. Kumar, S. Murugesan, L. Ci, R. Vajtai, R. J. Linhardt, O. Nalamasu, and P. M. Ajayan, Proc. Natl. Acad. Sci. U.S.A. **104**, 13574 (2007).
[8] P. Barquinha, L. Pereira, G. Goncalves, R. Martins, and E. Fortunato, Electrochem. Solid-State Lett. **11**, H248 (2008).
[9] P. Barquinha, G. Goncalves, L. Pereira, R. Martins, and E. Fortunato, Thin Solid Films **515**, 8450 (2007).
[10] E. Fortunato, N. Correia, P. Barquinha, L. Pereira, G. Goncalves, and R. Martins, IEEE Electron Device Lett. **29**, 988 (2008).
[11] Renova, Portugal, paper producer.
[12] R. Martins, P. Barquinha, A. Pimentel, L. Pereira, and E. Fortunato, Phys. Status Solidi A **202**, R95 (2005).
[13] S. Ju, F. Ishikawa, P. Chen, H. K. Chang, C. W. Zhou, Y. G. Ha, J. Liu, A. Facchetti, T. J. Marks, and D. B. Janes, Appl. Phys. Lett. **92**, 3 (2008).
[14] A. Campbell, Proc. R. Soc. London, Ser. A **78**, 196 (1906).
[15] D. Dalton, F. Gnadinger, D. Klingensmith, V. Olariu, T. Kalkur, M. Rahman, and A. Mahmud, Integr. Ferroelectr. **81**, 187 (2006).