Low-Voltage Low-Power CMOS Analogue Circuits for Gaussian and Uniform Noise Generation

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Abstract - *A CMOS analogue circuit for Gaussian noise generation as well as a novel circuit for transforming Gaussian noise into uniform noise, both designed for operating with a supply voltage of 1.5V, are presented. Both circuits are optimized for a 0.35μm standard CMOS technology using an equation-based design methodology based on genetic algorithms. Electrical simulations demonstrate that high noise amplitudes together with reasonable bandwidths can be achieved with relatively low power dissipation. Potential applications include self-calibration and on-chip self-testing of video-rate analogue-to-digital converters.*

1. INTRODUCTION

A wide variety of applications require noise sources as building blocks namely, in electronic testing and measurement, communication systems and cryptography [1]. Digital circuits can be employed to create pseudorandom numeric sequences but, for very stringent requirements such as data encryptation, pseudorandom noise is often inadequate [2]. Discrete implementations usually lead to larger power dissipations and die areas since a digital-to-analogue converter and an anti-imaging low-pass filter are required to provide an analogue continuous-time output. Noise generators can be used for digital self-calibration of analogue-to-digital converters (ADCs) [3] and, since these generators have a uniform power spectral density, they are probably the best stimulus for on-chip full-speed characterization of video-rate ADCs through histogram tests [4].

This paper presents a CMOS analogue circuit for Gaussian noise generation as well as a new circuit for transforming Gaussian noise into uniform noise both operating with a single supply-voltage of 1.5V. The Gaussian noise generator (GNG) is based in a fully-differential high-gain inverting configuration. The amplifier (opamp) used employs a three-stage topology comprising a folded-input stage followed by two differential common-source stages with offset cancellation of the first and second stages. Different realizations of GNGs based deterministic chaotic circuits have also been reported and can be found in [11]. However, a full description of such technique as well as a comparison between it and the one used in this work is out of the scope of this paper. The specifications for the GNG require high closed-loop gain, a bandwidth of 10 MHz, an output swing of 0.8 V and an output-referred *rms* noise of, at least, two hundreds of mili-Volts. As shown in section 4 of this paper, this can be achieved by means of a powerful circuit optimizer based on genetic algorithms. The uniform noise generation can be then generated using a new low-voltage (LV) analogue circuit that transforms Gaussian noise into Uniform noise using two non-correlated GNG circuits. Finally, simulated results are presented and discussed.

2. LOW-VOLTAGE LOW-POWER CMOS GAUSSIAN NOISE GENERATOR (GNG)

A) Circuit Principles and Topology

The GNG generator can be realized by a continuous-time or discrete-time implementation. Two possible circuits, corresponding to each case are shown in Fig. 1 (a) and (b), respectively. In this paper, for simplicity reasons, only the continuous-time version of GNG is described. However, the design of the switched-capacitor (SC) version is straightforward. The continuous-time GNG shown in Fig. 1 (a), works by amplifying the thermal noise produced by large input resistors using a low voltage opamp in a high-gain closed-loop configuration. This method was reported in [2] but for the case of a GNG circuit supplied with 5V. Resistors *R3* are used to generate wideband thermal noise in the form of kT/C_{in}, where k is Boltzmann's constant, T is absolute temperature and C_{in} represents the equivalent input capacitance of the opamp. The second source of input-referred thermal noise is the opamp itself which should be designed to have input transistors with very low transconductance, gm_1, quite-large excess noise factor, γ, and it should be optimized in order to maximize the bandwidth (Δf), the output-referred noise, $V_{on}(rms)$, and the open-loop dc gain, A.

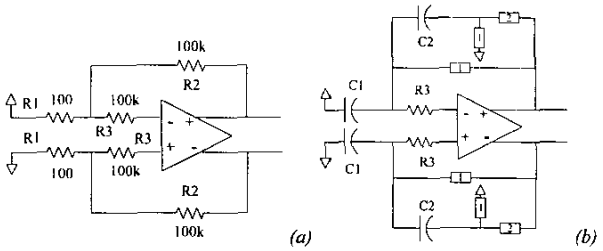

Fig. 1 - Gaussian noise generators: (a) a continuous-time realization; (b) a discrete-time SC realization.

In fact, the output-referred *rms* noise of this GNG generator is approximately given by:

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$$V_{on}(rms) \approx \frac{R1+R2}{R1+(R1+R2)/A} \cdot \sqrt{2 \cdot (v_{ni}^2(f) \cdot \Delta f + \frac{k \cdot T}{C_{in}})}\ , \qquad (1)$$

where $v_{ni}^2(f)$ represents the input-referred spectral noise density of the opamp. A schematic of the LV opamp is depicted in Fig. 2. The circuit comprises a folded-input stage followed by two differential common-source stages with input offset cancellation. For the sake of simplicity, the output-stage (third-stage) is not shown since it has exactly the same topology of the second (but, obviously, with a different sizing). The four low-pass filters (*LPF*) used for offset cancellation can be implemented using a simple 1st-order passive structure with the capacitors implemented using NMOS devices with large gate area. The undesirable effect of high $1/f$ noise because of using PMOS input devices with very low transconductance in the first stage is significantly attenuated by the high-pass response of the second and third stages due to the offset cancellation method employed. The poles of the LPFs can be placed at a frequency where the residual $1/f$ noise is negligible. Note that for the previously referred applications in ADCs, the noise does not necessarily have to be white over the entire bandwidth as long as it remains Gaussian.

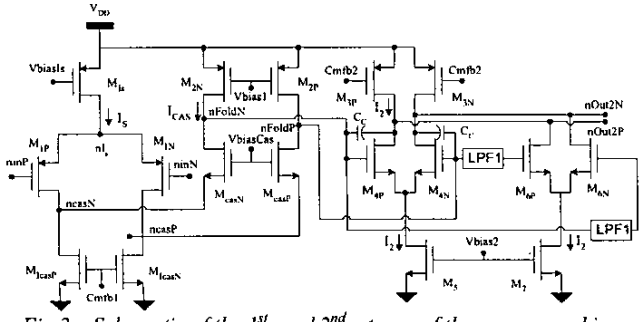


Fig.2 – Schematic of the 1st. and 2nd. stages of the opamp used in the GNG. The 3rd. stage (not shown) is equal to the 2nd.

The open-loop gain of the opamp is given by the product of the gain of all stages, yielding

$$A \approx \frac{gm_1}{(g_{ds2}+(g_{dsIcas}+g_{ds1})\cdot(g_{dscas}/gm_{cas}))} \cdot \frac{gm_4}{(g_{ds3}+g_{ds4}+g_{ds6})} \cdot Av_3 \qquad (2)$$

The input-referred spectral density of the opamp, $v_{ni}^2(f)$ is defined by the folded-input stage and given by

$$v_{ni}^2(f) = 4 \cdot k \cdot T \cdot \frac{2}{3 \cdot gm_1} \cdot \gamma, \qquad (3)$$

where gm_1 is the transconductance of the input PMOS differential-pair and γ is approximately given by:

$$\gamma \equiv 1 + \frac{gm_2}{gm_1} + \frac{gm_{Icas}}{gm_1}, \qquad (4)$$

which comprises basically the noise contributions of the current-sources of the folded-input stage (M_{Icas} and M_2 devices). The equivalent bandwidth of the opamp, Δf, is approximately given by:

$$\Delta f \equiv \frac{A}{G} \cdot \frac{1}{2\pi \cdot (\tau_{nin}+\tau_{ncas}+\tau_{nFold}+\tau_{nout2}+\tau_{nout3})} \qquad (5)$$

where G represents the closed-loop gain and τ_{nin}, τ_{ncas}, τ_{nFold}, τ_{nout2}, τ_{nout3}, are the time-constants associated respectively with nodes *nin*, *ncas*, *nFold*, *nOut2* and with the output-node (*nOut3*, not represented). These time-constants are only dependent on the impedance and the parasitic capacitances associated to each node, according to (for C_C <<):

$$\tau_{nin} \equiv R_3 \cdot C_{in}\ ,\ \tau_{ncas} \equiv \frac{C_{db1}+C_{dbIcas}+C_{sbcas}+C_{gscas}}{g_{ds1}+g_{dsIcas}},$$

$$\tau_{nFold} \equiv \frac{'C_{db2}+C_{dbcas}+C_{gs4}}{g_{ds2}+(g_{dsIcas}+g_{ds1})\cdot(g_{dscas}/gm_{cas})}, \qquad (6)$$

$$\tau_{out2} \equiv \frac{C_{db3}+C_{db4}+C_{db6}+C_{gs4(3rd.stage)}}{g_{ds3}+g_{ds4}+g_{ds6}},$$

$$\tau_{nout3} \equiv \frac{C_{db3(3rd.stage)}+C_{db4(3rd.stage)}+C_{db6(3rd.stage)}+C_L}{g_{ds3(3rd.stage)}+g_{ds4(3rd.stage)}+g_{ds6(3rd.stage)}+g_L}$$

Usually only one of these time-constants is dominant, typically τ_{nin} or τ_{nFold}, depending on the sizing and on the load. Finally the total power dissipated by this circuit, P_{TOT}, is given by (excluding the CMFB and the biasing circuitry):

$$P_{TOT} = V_{DD} \cdot (I_S + 2 \cdot I_{CAS} + 2 \cdot I_2 + 2 \cdot I_{2(3rd.stage)}) \qquad (7)$$

B) Circuit Optimization

The circuit was designed and optimised for a 0.35µm CMOS standard technology with $V_{Tp} = -0.65\text{V}$, $V_{Tn} = 0.52\text{V}$ and able to operate at a supply voltage of 1.5 V. An equation-based design methodology for optimization using genetic algorithms such as the one reported in [5,6] was used since many performance parameters had to be simultaneously optimized ($A, \Delta f, V_{on}, P_{TOT}$) with a relatively high number of devices (variables). The fitness function, $f(\vec{x})$, was defined according to expression (8), taking into account the low-frequency gain, the bandwidth, the output-referred *rms* noise and the total power dissipation.

$$f(\vec{x}) \approx (1-e^{-(\frac{A}{A\_desired})})(1-e^{-(\frac{\Delta f}{\Delta f\_desired})}) \\ (1-e^{-(\frac{V_{on}}{V_{on}\_desired})})(1-e^{-(\frac{P_{TOT}\_desired}{P_{TOT}})}) \qquad (8)$$

The genes comprised in each chromosome, $\vec{x}$, are basically the biasing currents (I_S, I_{CAS}, I_2 and $I_{2(3rd.\ stage)}$), the channel

lengths of all transistors, L_i, as well as their saturation voltages, $V_{DSsat\text{-}i}$.

3. LV ANALOGUE CMOS CIRCUIT FOR TRANSFORMING OF GAUSSIAN NOISE INTO UNIFORM NOISE (G2U)

The proposed novel circuit implements the following transformation function:

$$f(v_1, v_2) = e^{-((v_1^2+v_2^2)/2)} = e^{-(v_1^2/2)} \cdot e^{-(v_2^2/2)} \quad (9)$$

where v_1 and v_2 are two uncorrelated Gaussian input variables. If v_1 and v_2 have a Gaussian distribution with zero mean and variance equal to one, $N(0,1)$, then $f(v_1, v_2)$ is uniformly distributed $U(0,1)$ [7]. It should be noted that, a LV analogue implementation of the function $e^{-((v_1^2+v_2^2)/2)}$ becomes impossible since factor $-((v_1^2+v_2^2)/2)$ has necessarily to be a voltage and possible values are distributed in the interval $[(-(3\cdot\sigma)^2/2), 0]$ with σ = 1V. However, this function can be realized as a product of two Gaussian functions $(e^{-(v_1^2/2)} \cdot e^{-(v_2^2/2)})$ but it requires an additional multiplier as illustrated in the block diagram shown in Fig. 3. If the standard deviation of each GNG is smaller than 1 (for practical reasons), an additional constant, k_1, should be introduced to compensate this reduction.

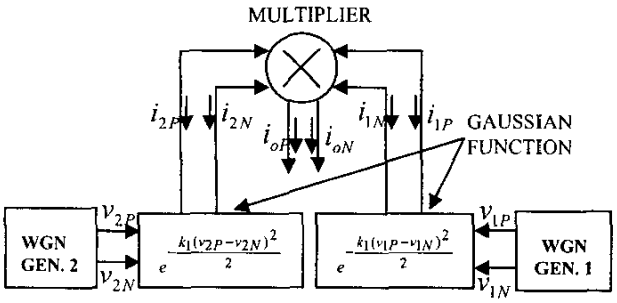


Fig. 3: Block diagram representing the circuit that implements the required transformation function (G2U).

Each Gaussian function can have a fully-differential implementation using the circuit shown in Fig. 4 (a) comprising two source-coupled differential-pairs biased by the same tail current [8]. Two additional current-sources (I_1 and I_2) with a nominal current of $I_B/2$ are required to make i_{iP} and i_{iN}, fully-differential current signals. Assuming v_{iP} and v_{iN} differential signals, due to the existence of resistors, R, the signal applied to the gate of devices M_{2a} and M_{2b} is always constant and equal to the input common-mode voltage. Since the biasing current, I_B, is constant, the shape of the differential drain-current, $(i_{iP} - i_{iN})$, as a function of the differential input voltage, $(v_{iP} - v_{iN})$, becomes essentially Gaussian. However, the implementation of the Gaussian function is not precise, since the referred currents have not an exact Gaussian form. In fact, the function is described by [9]:

$$(i_{iP} - i_{iN}) = \frac{2 \cdot K \cdot I_B}{2 \cdot \cosh(k_2 \cdot (v_{iP} - v_{iN})) + K} \quad (10)$$

where K represents the multiplicity of transistors M_2 in parallel (K = 2 in this case) and k_2 represents an adjusting constant. For relatively small input signals and reduced biasing currents the relative error can be made small. In order to perform the product of both Gaussian functions the differential trans-linear multiplier shown in Fig. 4 (b) is used [10]. Analyzing this circuit it can be found that its output is given by

$$i_{out} = i_{oP} - i_{oN} = \frac{(i_{1P} - i_{1N}) \cdot (i_{2P} - i_{2N})}{(I_B/2)} \quad (11)$$

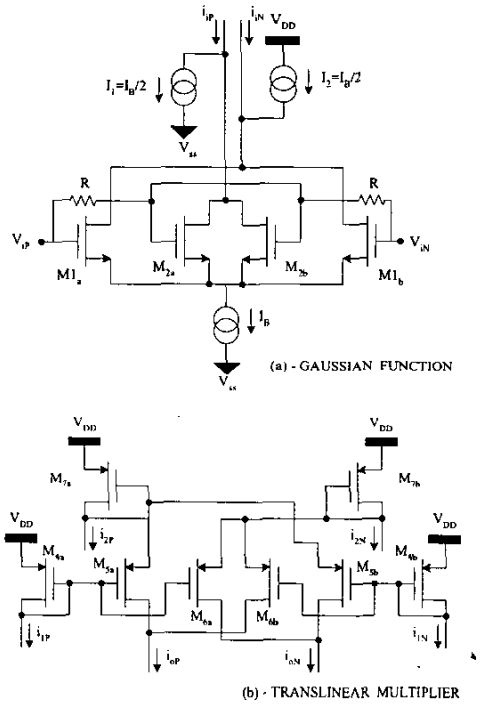


Fig. 4 (a) – Circuit used for realizing the Gaussian function; (b) – Four-quadrant trans-linear current-mode multiplier.

4. CIRCUIT'S SIZING AND SIMULATED RESULTS

A) The GNG block

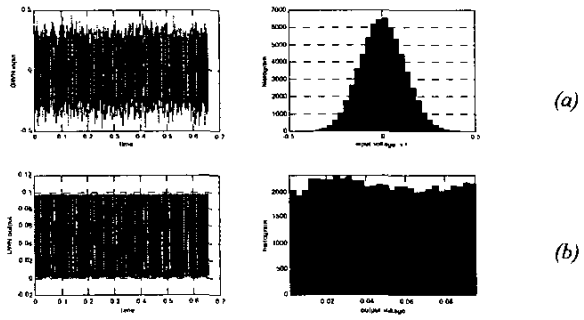
Table 1 compares the obtained values of the GNG after the optimization described with post-simulated (ac simulations) values for the circuit using an electrical simulator. Using $R3$=100kΩ, $gm_1 \approx$ 55μS, $I_s \approx$ 20μA, $I_{CAS} \approx$ 47μA, $I_2 \approx$ 37μA, $I_{2(3rd.\ stage)} \approx$ 196μA, $\gamma \approx$ 12 and $C_{in} \approx$ 0.1 pF a differential GNG with σ= 232mV and with bandwidth of about 10 MHz can be designed.

Table 1	Specs. desired	Specs. achieved by optimization	Electrical simulated results
$V_{on}(rms)$ [mV]	200	302	**232**
G [dB]	-	59	**52**
A [dB]	80	72	**64**
Δf [MHz]	10	8	**10**
P_{TOT} [mW]	< 5	0.87	**0.93**

The major differences appear in the open-loop gain, A, as well as in the bandwidth, Δf. The reason is mainly due to the equations used for the drain-source conductances, which are not precise for small drain-source voltages.

B) The G2U block

The complete circuit is designed for the same referred 0.35μm CMOS technology. Two of the GNG previously described designed with $\sigma \approx 0.25/3$V are used. The circuit is supplied with V_{DD} = 1.5V, the bias current is fixed at $I_B = 100\mu A$, and k_1 is adjusted to 72 by sizing M_{1a}, M_{1b}, M_{2a}, M_{2b} with W/L=100/0.4 ($V_{DSsat(M_{1i},M_{2i})} \approx 40$mV). Devices M_{4a}, M_{4b}, M_{5a}, M_{5b}, M_{6a}, M_{6b}, M_{7a}, M_{7b} are sized with W/L=50/0.4 ($V_{DSsat(M_{4i},M_{5i},M_{6i},M_{7i})} \approx 110$mV). Current-sources I_B, I_1, and I_2 are implemented with simple NMOS and PMOS current-mirrors. The output current is converted to voltage through 5kΩ resistors to achieve output-noise voltage amplitudes of about 100mV. Output loading capacitances of 0.2pF are used.



(a)

(b)

Fig. 5 (a) – Input differential Gaussian noise voltage and corresponding histogram; (b) – Output differential uniform noise voltage and corresponding histogram.

The transformation function, $f(v_1, v_2)$, was electrically simulated using two equal differential input ramp-signals producing a differential output current with less than 0.4% of maximum relative error to the ideal function. This error was obtained using

$$Error = \frac{100}{\max(f(v_1,v_2)) \cdot npts} \cdot \sum_{i=1}^{npts} \left| f_i^*(v_1,v_2) - f_i(v_1,v_2) \right| \quad (\%) \qquad (12)$$

where *npts* is the number of simulated points (*npts* = 10000) and, $f_i^*(v_1,v_2)$ and $f_i(v_1,v_2)$ represent, respectively, the simulated and the ideal transformation functions.

The complete circuit dissipates about 750μW for at 1.5V. This circuit was also electrically simulated by directly applying two differential Gaussian-noise signals with 2^{16} points generated in MATLAB. Fig. 5 (a) displays the input differential Gaussian noise voltage signal and its histogram and Fig. 5 (b) shows the output differential uniform noise current signal and its histogram.

5. Conclusions

A broadband CMOS analogue circuit for Gaussian noise generation as well as a new circuit for transforming Gaussian noise into uniform noise designed for a supply voltage of 1.5 V were presented. Electrical simulations proved that high noise amplitudes and reasonable bandwidths can be achieved with relatively low power consumption.

Acknowledgments

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