Thyristor-Bypassed Sub-Module Power-Groups for Achieving High-Efficiency, DC Fault Tolerant Multilevel VSCs

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Thyristor-Bypassed Sub-Module Power-Groups for Achieving High-Efficiency, DC Fault Tolerant Multilevel VSCs.

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***Abstract*—Achieving DC fault tolerance in modular multilevel converters requires the use of a significant number of Sub-Modules (SMs) which are capable of generating a negative voltage. This results in an increase in the number of semiconductor devices in the current path, increasing converter conduction losses. This paper introduces a thyristor augmented multilevel structure called a Power-Group (PG), which replaces the stacks of SMs in modular converters. Each PG is formed out of a series stack of SMs with a parallel force-commutated thyristor branch, which is used during normal operation as a low loss bypass path in order to achieve significant reduction in overall losses. The PG also offers negative voltage capability and so can be used to construct high efficiency DC fault tolerant converters. Methods of achieving the turn-on and turn-off of the thyristors by using voltages generated by the parallel stack of SMs within each PG are presented, while keeping both the required size of the commutation inductor, and the thyristor turn-off losses low. Efficiency estimates indicate that this concept could result in converter topologies with power-losses as low as 0.3% rated power, whilst retaining high quality current waveforms and achieving tolerance to both AC and DC faults.**

***Index Terms*—AC-DC Power Conversion, Converters, HVDC Converters, HVDC Transmission, Thyristor Converters, Thyristor Applications, DC Faults, Fault Blocking.**

I. Introduction

THE Half-Bridge (HB) Modular Multilevel Converter (MMC) is the standard topology for implementing Voltage Source Converters (VSCs) for HVDC applications [1]. Its Sub-Module (SM) based modular design results in high quality voltage and current waveforms. The efficiency is also high, though still below what is achievable with Line Commutated Converter (LCC) technology. Not with-standing these advantages, the MMC remains weak to DC-side faults because of the inability of its stacks to generate a negative output voltage. If DC fault tolerance is a required feature of the converter, this could be solved by replacing some of the HB SMs with Full-Bridge (FB) SMs in a hybrid design [2], [3]. Other options for achieving DC fault tolerance include designing the converter with different SM arrangements [4]–[7]. Other hybrid converter topologies, with different operating principles to the MMC, such as the Alternate Arm Converter (AAC) [8], [9] have also been proposed to address this issue.

None of these IGBT based solutions are capable of achieving the same efficiency levels as the HB-MMC, due to the extra semiconductor devices within the conduction path [10]. This paper details an investigation into a multilevel structure for achieving VSCs which combines thyristors and IGBTs. Thyristors have vastly superior conduction characteristics as well as higher available rated blocking voltages, which results in LCC-HVDC having higher efficiencies than current VSC technology can achieve. For example, an 8 kV thyristor conducting a load current of 1500 A can be expected to have a forward voltage drop in the region of 1.5 V, while a 3.3 kV IGBT can be expected to have a forward voltage drop in the region of 3 V for the same current load.

The idea of combining thyristors and controllable SM stacks to form a VSC has received some research interest in the literature. The parallel operation of a traditional thyristor based LCC converter with VSC has also been considered, however this can be considered as two separate converter stations [11]. One of the most notable examples of a true hybrid converter integrating thyristors and SMs is the Controlled Transition Bridge (CTB) [12]–[14], which combines a six-pulse bridge of thyristors, providing the majority of bulk power processing, with additional of SM stacks that provide filtering and current control. In [15] the author presented an MMC topology that is capable of isolating a DC side fault by utilising a parallel thyristor bridge and low current, high voltage DC circuit breaker. The thyristor bridge is not used during normal operation. In [16] the authors presented a cross-connected SM design that uses bi-directional switches, such as anti-parallel pairs of GTOs or IGCTs, to achieve DC fault tolerance without sacrificing converter efficiency. However the authors do not consider the requirement to rate some of the IGBT switches within the SM design to twice the SM capacitor voltage in the presented results. In [17] the authors propose a half-bridge SM rated to several tens of kV in which thyristors form the valves of the half-bridge, controlled by a stack of SMs that connects to the midpoint of a split SM capacitor. This structure requires inclusion in each SM of an inductor large enough to allow controlled ramping of the currents through the thyristors.

This paper examines the design of converters augmented

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with Power-Groups (PGs), a recently proposed hybrid multilevel structure [18], which combines IGBT-based SMs and a thyristor assembly forming a parallel branch. The intention of the PG concept is to achieve LCC efficiency levels, while also achieving DC fault tolerance and VSC controllability. The thyristor assembly is used as a low impedance bypass branch, which can be utilised during normal operation when the SMs within the PG are not required to generate part of the overall converter output voltage. The SMs within the PG are used to generate a voltage output when the thyristor assembly is in a blocking state, and to control the turn-on and forced commutation of the thyristor assembly as required. By series connecting PGs, any multilevel converter could be constructed. Results indicate that PGs have the potential to allow VSCs with power losses close to 0.3% rated power to be achieved, while retaining full independent P/Q control, high quality AC and DC current waveforms and tolerance to both AC and DC side faults.

This paper is structured as follows: Section. II gives a general introduction to the PG concept. Section. III investigates the impact of thyristor dV/dt limitations on the design of PGs. Section. IV then presents a proposed differential voltage technique for controlling the turn-on & turn-off of the thyristor assembly within each PG. Section. V then compares the design and efficiency of several converter topologies. A fault study based on the most promising topology identified is carried out in Section. VI. Finally some conclusions are drawn in Section. VII.

II. Power Groups

A Power-Group (PG), shown in Fig. 1, is a modular structure comprised of a series stack of SMs in one branch, with a parallel branch containing a commutating inductance in series with a thyristor assembly that contains anti-parallel series thyristors to allow for bi-directional current flow. The stack of SMs in this case is formed out of FB SMs, though it could potentially be formed out of a hybrid combination of HB and FBs, or other SM type. The stack of SMs is capable of generating a bipolar voltage output, while the thyristor branch acts as a low impedance bypass path which can be used when the stack of SMs is not required to generate a voltage. The thyristor branch within each PG can be independently commutated off when required by applying a voltage generated by the stack of SMs across the commutating inductor. PGs could be series connected in a similar manner to SMs to form a stack or chain-link valve within a modular converter. By using a series connected arrangement of PGs, any multilevel converter based upon SMs could be constructed.

The thyristors within each PG can be utilized when the SMs within the PG are required to generate zero volts. In modular converters for HVDC applications the current flowing through a valve is typically maximum when the voltage generated by the valve is at a minimum. The PG concept therefore has significant promise for reducing overall converter losses. Opportunities to use the PG thyristors can be created by dividing the overall voltage waveform of the stack between PGs so that they are mostly assigned to either generate their full available output voltage (i.e. insert all SMs within the PG) or generate zero volts. This is illustrated in Fig. 2 for the case of an MMC which has been augmented with five PG structures per converter arm. The top sub-plot shows how the stack voltage is divided between the five PGs within the arm. The following sub-plots show the voltage generated by each PG, and the current through the thyristor branch within each PG. A sorting algorithm is applied to ensure balancing of the SM voltages within each PG. Each PG tends to generate either zero volts, or their full available voltage. For a small portion of the cycle a PG may generate an intermediate voltage, in order to allow fine current current. When a PG is generating a voltage, the arm current flows through the SM branch of that PG and the PG's thyristors are in a blocking state. The portions of the cycle when each PG generates zero volts represent opportunities for the bypass thyristor branch within each PG to be utilised in order to reduce losses within the converter. The thyristor branch can then be force-commutated as required when the SMs within the PG are needed to generate part of the overall converter voltage waveform. The SMs within each PG are used to control the turn-on and turn-off of the thyristor bypass branch within each PG, this means that each PG's thyristor bypass branch can be managed independently of the other PGs within the converter arm.

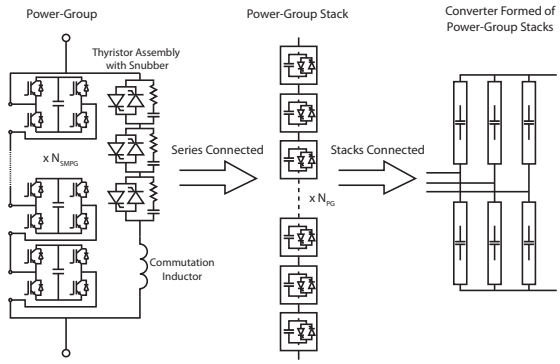

Fig. 1. Left: PG comprised of full-bridge SMs with a bypass branch consisting of an assembly of anti-parallel thyristors with a series commutating inductance. Middle: Series connected PGs formed into a valve stack. Right: Valve stacks, formed out of PGs, connected together to form a converter.

PGs could potentially be constructed with any number of SMs within each PG. For practical realisation, designs with only a few SMs is considered more advantageous, as this has the benefits of reduced voltage clearance requirements within each PG, as well as creating a more modular overall converter design. An example specification for a PG with 8 SMs is given in Table. I, with each SM operated at a nominal voltage of 1.8 kV, resulting in a overall PG rated voltage of 14.4 kV. The thyristors considered for use within the PG are 8 kV symmetrical devices. For the PG voltage rating considered this results in a requirement to include only three series thyristors (assuming a voltage de-rating factor of 0.6) in each direction within the PG, for a total of 6 thyristors when considering bi-directional current flow. The voltage drop through the thyristor branch is significantly lower (4.5 V, 1.5 V per thyristor, 3 thyristors in conduction path) at rated current in comparison to the voltage drop across the 8 full-bridge SMs (48 V, 3 V

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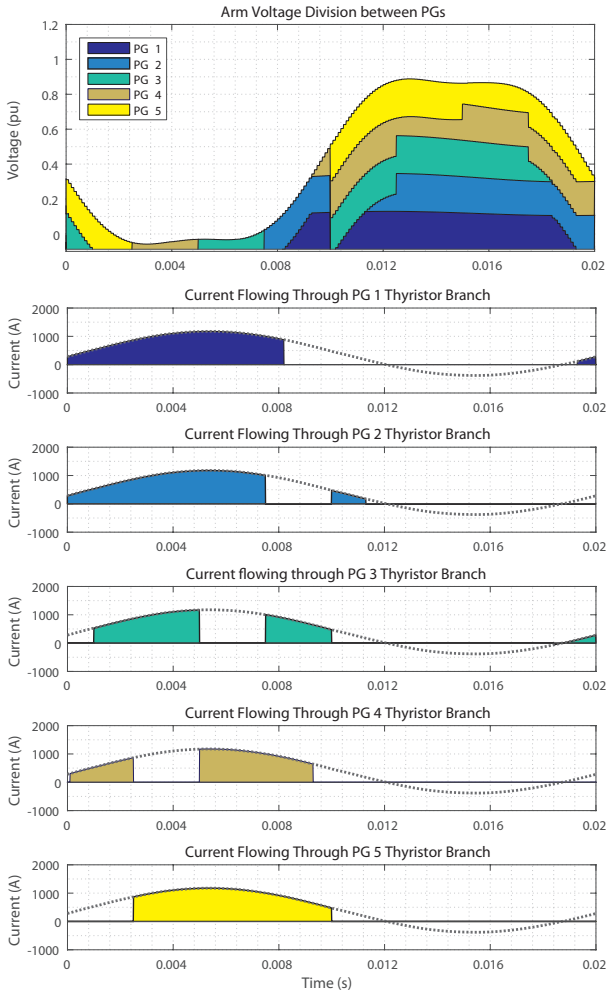

Fig. 2. Voltage and current waveforms for an MMC in which each converter arm is formed of 5 PG structures. Top: Arm voltage divided between PGs (per unit on DC pole to pole voltage). Sub-plots showing thyristor branch currents of the five PGs within one converter arm. Overall arm current is shown in dashed lines. Arm current not flowing through the thyristor branch of a PG flows through the parallel stack of SMs within that PG.

per IGBT, 16 IGBTs in the conduction path).

TABLE I
POWER-GROUP DESIGN SPECIFICATION

Number of SMs Per PG	8
SM Type	Full-Bridge
Number of Thyristors	6 (Anti-parallel arrangement of 3 in series)
Nominal SM Voltage	1800 V
Peak SM Voltage	2000 V
Nominal PG Voltage	14.4 kV
Rated Current	1500 A
IGBT Device	Infineon FZ1500R33HE3 - 3.3 kV 1.5 kA
Thyristor Device	Infineon T2871N - 8 kV 2.62 kA
Voltage drop through SM path at rated current	~48 V
Voltage drop through Thyristor Path at rated current	~4.5 V

The inclusion of thyristors within a multilevel structure introduces several challenges into how the PG must be designed and operated so as to respect the operational limits of the thyristors. Thyristors optimized for low conduction losses are sensitive to excessive dV/dt stress during forward blocking operation, as well as excessive di/dt values during the first few μs of turn-on. To ensure the thyristors operate within these limits it will be required for there to be a snubber network placed across the thyristor assembly, as well as including a series commutating inductor. The snubber network limits the dV/dt stress placed upon the thyristors, as well as ensuring that voltage is distributed equally between thyristors during turn-on and turn-off. The commutating inductor limits the di/dt values during turn-on and turn-off, as well as forming part of the overall dV/dt snubbering circuit. The use of saturable inductors has been found to be acceptable for use as the commutating inductor and this gives the advantage of reduced overall inductor volumes.

In addition to dV/dt and di/dt operational limitations, thyristors have to be maintained in reverse bias for a period of time after they have been turned-off sufficient to ensure recombination of carriers in the drift region. If this time is not met, then premature application of forward voltage can result in uncontrolled thyristor turn-on which would lead to device destruction. The minimum required time between the zero crossing of the anode current and the re-gaining of forward voltage blocking capability is called the thyristor turn-off time (t_q). For large phase-control thyristors the value of t_q can be up to 500-600 μs. In practical applications the period when the thyristor is held reverse biased after turn-off, referred to as the hold-off time, must exceed the t_q time. To give some safety margin a hold-off time of 1 ms is considered in this paper.

III. SNUBBER DESIGN

A dV/dt limiting snubber circuit must be placed across each of the thyristors within each PG. This snubber circuit is formed out of a combination of the commutating inductor and an RC network placed across the thyristors. If the entire stack of SMs is switched simultaneously, then the snubber design may be infeasible. To ease the snubber design the switching of the SMs can be limited so that they are inserted in a staircase ramp with a controlled slew rate, similar to the approach taken in [19]. The snubber design would then only have to be capable of limiting the dV/dt values generated by the switching of single SMs, rather than the entire SM stack. This is illustrated in Fig. 3. Switching intervals in the region of 10 μs between each SM switching have been found to give good performance, without limiting the dynamic performance of the converter.

The size of the commutating inductance has been found to have a large impact on the snubber design. This is illustrated in Fig. 4, showing the minimum achievable peak dV/dt stress that is placed upon each thyristor within the PG by a SM switching when it is at its peak rated voltage (2 kV). The Infineon T2871N thyristor has a critical dV_D/dt limit of 2000 $V/\mu s$. To achieve dV_D/dt values an order of magnitude below this critical limit it was found to be necessary for the commutating inductance to have a minimum value in the region of 20-30 μH, when considering a range of RC values. The switching of SMs results in some current draw into the snubber network, to prevent this causing the commutating inductor from saturating, the commutating inductor should be designed with a saturation characteristic above the peak current draw of the snubber. The snubber resistor must also be sized to limit the discharge current from the snubber capacitor during turn-on of the thyristors.

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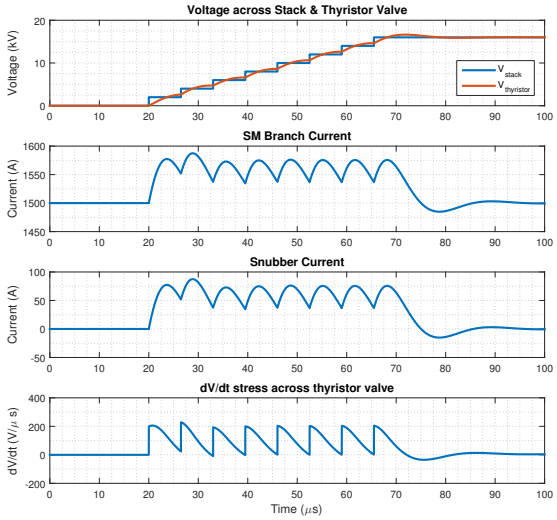

Fig. 3. Controlled switching of PG SM stack. R=4.5 Ω, C=0.6 μF. Commutating inductor is a 45 μH saturable inductor with a 300 A saturation characteristic.

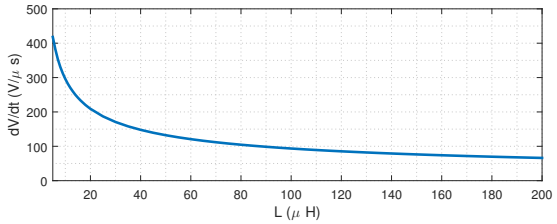

Fig. 4. Minimum achievable dV/dt stress placed upon each thyristor by a 2000 V SM switching event considering RC snubber designs with R in the range of 1-30 Ω and C in the range of 0.01-0.3 μF.

The inclusion of a snubber network will incur some additional losses within the converter, which may offset some of the efficiency gains achieved through utilising the thyristors. The losses incurred in the RC network in the simulation results shown in Fig. 3 are equal to about 0.1 J per SM switching event, significantly below the switching losses that may be expected in a high-power IGBT (2 J per turn-off event). Larger inductor sizes were found to result in slightly more efficient snubber designs being achievable, however the possible loss reductions ($\sim$ 0.05 J) are relatively small in comparison to the overall converter losses, and so are considered a less critical design consideration in comparison to ensuring the commutating inductor is kept small in size. Losses within the commutating inductor are not considered.

IV. Turn-On and Turn-Off Control

The turn-on and turn-off of the thyristors within each PG can be actively controlled by using the parallel stack of SMs to generate a voltage which will drive a circulating current around the PG, either forcing the converter arm current into or out of the thyristor assembly. This is illustrated in Fig. 5 for the case of the turn-off of the thyristors. In order to control this turn-on and turn-off, there must be some inductance included in series with thyristors within each PG. This inductance limits the di/dt through the thyristors during both turn-on and turn-off and also forms an important part of the dV/dt snubbering across the thyristors, as discussed in Section. III. The magnitude of the voltage used to commutate the thyristor has an impact on the required size of the commutating inductance, for di/dt limiting purposes, as well as the magnitude of the turn-off losses incurred within the thyristors.

To ensure the thyristors turn on correctly they must be forward biased prior to receiving a gate pulse. To prevent SM failure it is important that the SMs used to forward bias the thyristors are not then subsequently discharged through the thyristors once a firing pulse is applied. It has been found that it is possible to generate this forward biasing voltage using the blocked state of a full-bridge SM (i.e. when all of its IGBTs are de-gated), and thereby avoiding the possibility of discharge. This will be discussed further in the following subsections.

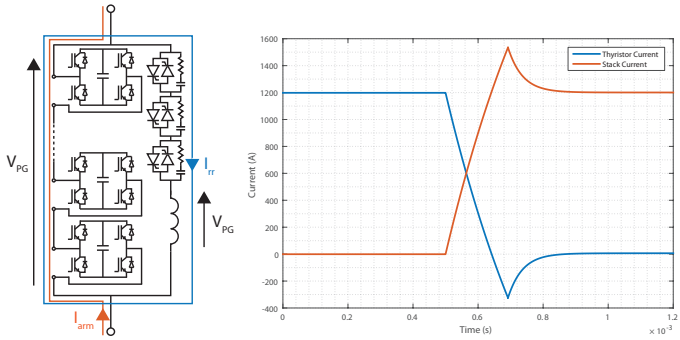

Fig. 5. Turn-off of PG thyristors - arm current is commutated from the thyristor branch to the SM branch within the PG. (a) Current Paths for Arm Current and Reverse Recovery Current. (b) Thyristor and Stack Currents during turn-off of the PG thyristors.

The di/dt through the thyristors at turn on will be dependent on both the commutating inductance size and the commutating voltage magnitude. The T2871N thyristor considered has a critical di/dt limit during turn-on of 300 $A/\mu s$. For continuous use the actual di/dt should be limited to a value significantly below this, typically around 10 $A/\mu s$ in LCC applications. Generating this commutating voltage with a single SM operating in the region of 2 kV would require a commutating inductance of 200 μH, significantly above the required size for dV/dt snubbering ($\sim$ 20 μH), and was found to result in thyristor turn-off losses in the region of 20 J per turn-off event. A dedicated turn-off SM that operates at a lower voltage could be included within each PG, however this would result in additional conduction losses, as well as a single point of failure for the entire PG. The following subsection details a proposed differential voltage technique that allows smaller commutating voltages to be generated, which results in a significantly lower required commutating inductance size and an order of magnitude reduction in turn-off losses.

A. Differential Voltage Generation

The use of a full SM voltage to control the turn-on and turn-off of the PG thyristors results in a requirement for a relatively large inductor to be included in each PG, as well as turn-off losses in the region of 20 J. An alternative method

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of controlling the PG thyristor turn-on and turn-off would be to use the difference between two SM voltages to generate the required commutating voltage. By inserting one SM in a positive direction and another in the negative direction the differential voltage between the two SM capacitor voltages could be placed across the thyristors. This concept is illustrated in Fig. 6a. This may allow commutating voltages in the region of 100-200 V to be used, lessening the required size of the commutating inductor, and decreasing the thyristor turn-off losses. This method of generating the commutating voltage is applicable to any PG structure with at least one bipolar SM type. The correct differential voltage could be achieved by actively discharging a SM prior to firing the thyristors.

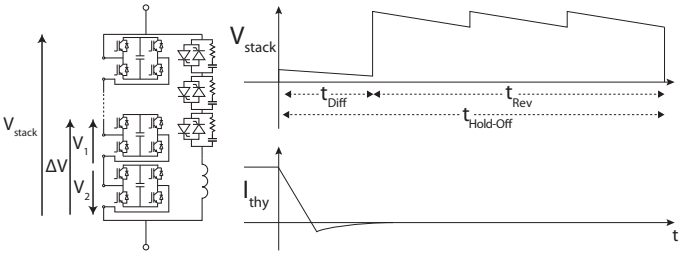

Fig. 6. a) Intermediate SM commutating voltage generation. b) PG thyristor turn-off procedure showing a period of differential voltage being applied, followed by whole SM voltages in rotation, causing the sharp changes in applied stack voltage.

As discussed in Section II, the hold-off time applied to the thyristors may have to be in the region of 1 ms. The SMs generating this reverse voltage will be in the current path of the arm current, resulting in them either being charged or discharged. Holding the differential pair in the current path for the entire hold-off time will not be feasible unless a very large SM capacitor is used. The proposed solution to this is to use the differential voltage for a period t_{Diff}, long enough to commutate the current back into the SM branch and recover the stored charge within the thyristors, and then use the stack of SMs to place a larger reverse voltage across the thyristors for a period t_{Rev}, which comprises the remainder of the hold-off period. Because the stored charge within the thyristors should be mostly evacuated this should result in only minor additional turn-off losses. To limit the voltage deviation of the SM used to generate the reverse voltage, the duty could be rotated between different SMs. The proposed turn-off procedure is illustrated in Fig. 6b, and is detailed in the following paragraphs, which give a step-by-step description of the proposed PG thyristor turn-on and turn-off procedure. Each paragraph has its own accompanying figure, shown in Fig. 7 showing the state of the SMs, as well as the current path through the PG. The steps are given assuming the upwards facing thyristors are to be fired.

a) SMs Conducting: Thyristors are turned off and the arm current is conducting through the SMs. The SMs are free to generate any requested voltage from the controller. The thyristors block the voltage generated by the SMs.

b) Turn-On - Step 1: All SMs apart from the SM that will be used as the lower voltage SM in the differential pair (SM_L) are bypassed. SM_L is inserted into the current path in order to discharge its capacitor voltage so that the correct difference voltage can be achieved. During this period the output voltage of SM_L (V_L) appears across the thyristors.

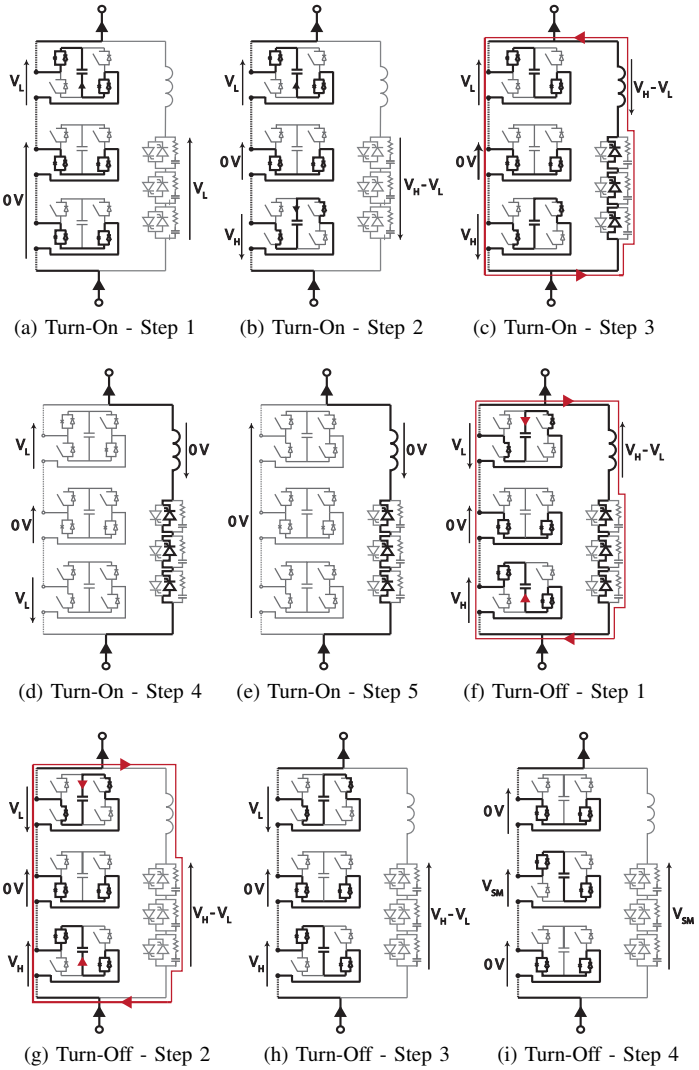

Fig. 7. Turn-On and turn-off control of PG thyristors using two SMs to generate a differential voltage - Black lines indicate that the arm current is flowing through that branch, grey indicates that there is no current. Red lines show circulating current within the PG.

c) Turn-On - Step 2: When the target voltage of SM_L has been achieved, the SM which is used as the higher voltage SM in the difference pair (SM_H) is switched from a bypass state to a blocked state. Its output voltage (V_H) is dependent on the arm current direction and is such that it opposes the current flow. As SM_L is inserted so that it is discharging its capacitor, the output voltages V_L and V_H are of opposite polarity. A forward voltage (with respect to the upwards facing thyristors) corresponding to $V_H - V_L$ is applied across the thyristors. During this period the difference voltage will increase due to the charging/discharging action of the arm current. This results in SM_H increasing in capacitor voltage and SM_L decreasing in capacitor voltage. To limit this, the firing pulse for the thyristor should be sent shortly after the thyristors are forward biased by this step.

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d) Turn-On - Step 3: The upwards facing thyristors are sent gate pulses. The voltage across them collapses and the difference voltage ($V_H - V_L$) now appears across the commutating inductor. This voltage drives a circulating current around the path shown in red, driving the arm current from the SM branch into the thyristor branch. The di/dt through the thyristors is determined by the magnitude of the difference voltage and the commutating inductor size. SM_H and SM_L will continue to charge/discharge while the current commutates.

e) Turn-On - Step 4: The current in the SM path is forced through zero. Some reverse current due to recovery of the diodes within the SMs may be expected. The blocked SM (SM_H), which has a higher capacitor voltage than the SM that is inserted in a negative polarity (SM_L), outputs a voltage which opposes any current flow. The overall SM path is effectively open-circuited and the arm current flows wholly through the thyristor branch.

f) Turn-On - Step 5: SM_L is then blocked for the remainder of the period when the thyristors conduct the arm current, this is done in preparation for the turn-off procedure. SM_H could then either remain blocked or set into bypass. All other SMs within the arm are kept in a bypass state.

A SPICE simulation of this turn-on procedure (apart from Step 5) is shown in Fig. 8. The behaviour of the diodes within the blocked SM were modelled using the parameters for a similarly sized high power diode given in [20]. From time 0-50 μs the SMs are conducting the arm current and the thyristor assembly is in a blocked state. Time 50-250 μs corresponds to step 1, where SM_L is being actively discharged in order to achieve the correct differential voltage. Once this has been achieved SM_H is blocked (step 2) while SM_L remains generating a positive voltage, resulting in the differential voltage between the SMs forward biasing the thyristors (Time 250-300 μs). At t=300 μs (step 3) the thyristors are fired and the current is forced from the SM branch into the thyristor branch. The initial di/dt is low ($\sim$4 A/μs) and increases once the inductor is driven into saturation. As the current reaches zero the diodes within SM_H, which is in a blocked state, will undergo reverse recovery.Some oscillation in the output voltage of the blocked SM can be expected at this point as its diodes recover. As the thyristors will have been fired by this point this transient voltage will appear across the commutating inductance. When the diodes recover SM_H outputs a voltage which opposes the voltage generated by SM_L. The resulting net voltage generated by the stack at this point is zero and the arm current flows wholly through the thyristor assembly (step 4).

g) Turn-Off - Step 1: After conducting the arm current for some period of time the decision to commutate the PG thyristors is made from a centralised controller. The SM with the higher capacitor voltage, SM_H, is switched with an output polarity that will drive a circulating current around the red path shown, driving the current from the thyristors and back into the SM path. The SM with the lower capacitor voltage SM_L remains blocked and so outputs a voltage which opposes any current flow. A difference voltage corresponding to $V_H - V_L$ is imposed across the commutating inductor. The thyristor current is driven through zero and continues

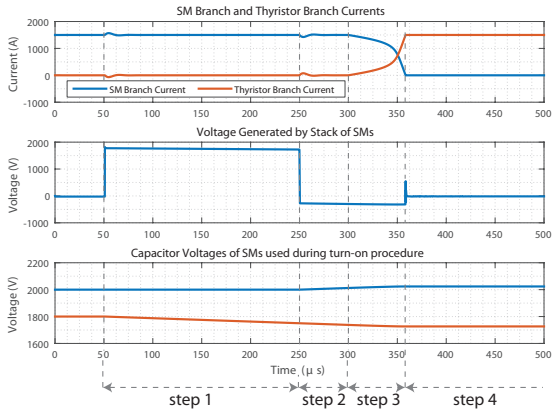

Fig. 8. Thyristor turn-on process when using differential voltage generation. Commutating inductor is a 30 μH saturable inductor with a 200 A saturation characteristic.

negative until the thyristor junctions recover their reverse voltage blocking capability. The voltages of the SMs used to impose the difference voltage starts to converge due to the charging/discharging action of the arm current.

h) Turn-Off - Step 2: The thyristor junctions recover and the commutating voltage $V_H - V_L$ is now across the thyristors, while the remainder of the stored charge within the thyristor junctions is recovered. The SMs conduct the arm current plus the reverse recovery current from the thyristors, which continues to circulate around the red path.

i) Turn-Off - Step 3: The stored charge within the thyristors is recovered (approximately 300 μs after SM_H is switched) and the arm current is wholly conducting through the SM path. The thyristors remain reverse biased.

j) Turn-Off - Step 4: A larger reverse voltage can be imposed across the thyristors for the remainder of the turn-off period to ensure it fully turns off. As the stored charge has mostly been recovered by this point the larger reverse voltage can be applied without a large penalty in terms of turn-off losses. This also allows another SM to be used apart from the pair used to generate the differential voltage. After the thyristors have been held reverse biased for a sufficient time (an additional 300-700 μs depending on the thyristors characteristics) the turn-off process has been completed. The PG is now able to use its SMs to generate an output voltage.

A SPICE simulation of the turn-off of the thyristors, with variation in the size of the commutation inductor, is shown in Fig. 9. The behaviour of the diodes within the blocked SM were modelled using the parameters for a similarly sized high power diode given in [20]. The thyristors are commutated by a small differential voltage (step 1) generated by two SMs in the parallel stack (t=100 μs). This commutates the current from the thyristors back into the SM path. The magnitude of the differential voltage decreases due to the charging/discharging action of the arm current. The current through the thyristors reverse as they recover. When the thyristor junctions regain their reverse blocking capability the differential voltage generated by the SMs appears across the thyristors (t=210 μs, step 2). The current in the thyristors then decays to zero (step 3). After the thyristors have been commutated a large reverse voltage

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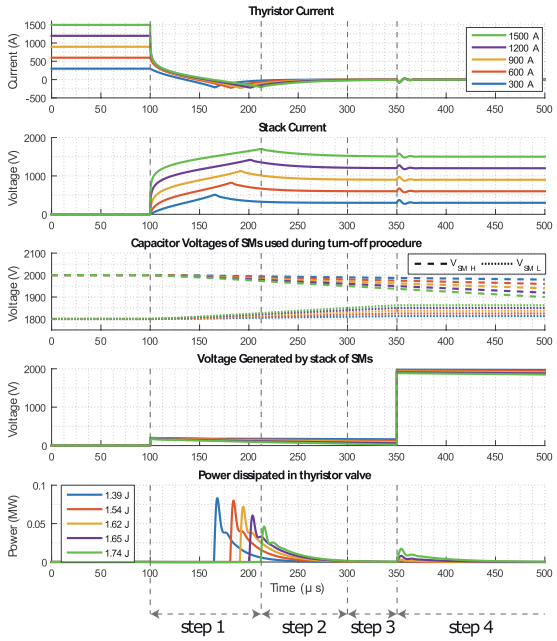

Fig. 9. Thyristor turn-off using differential voltage generation. Differential voltage is set to 200 V. Commutating inductor is a 30 μH saturable inductor with a 300 A saturation characteristic. Step intervals are shown lining up to the 1500 A case. Thyristor reverse-recovery losses are shown colour-coded for each case in the last sub-plot.

is applied across the thyristors (t=0.3 ms) for the remainder of the thyristor hold-off time (step 4). This is done to ensure the thyristors fully turn-off and regain their forward voltage blocking capability. Following this point the duty of which SM is used to hold the thyristor assembly reverse biased could be rotated between SMs, in order to limit their deviation in voltage. The losses incurred within the thyristor assembly with an arm current magnitude of 1500 A is 1.7 J, significantly below the loss incurred when a full SM is used to commutate the thyristors (∼22.5 J) and comparable to the turn-off loss that may be expected in a single high-power IGBT turning off at full load.

The operation of a PG within a PG augmented MMC, using differential voltage generation, as simulated in simulink, is shown in Fig. 10. No reverse recovery effects are seen because the limitations of the thyristor models within simulink. Prior to firing the thyristor an SM is actively discharged so that the target differential voltage can be achieved. The thyristor is then forward biased and then fired. The thyristor then conducts the arm current for several milliseconds. At turn-off the thyristor is commutated by applying a differential voltage from two of the SMs. After the thyristor current has been commutated and the reverse recovery process completed, the differential pair of SMs are switched to zero and other SMs are rotated in duty in order to keep the thyristor valve reverse biased. After the hold-off period is finished the turn-off procedure has completed and the PG is free to generate a voltage using its SMs. The SM capacitor voltages can be seen to be well controlled, with one tending to stay below the others due to the thyristor turn-off strategy employed.

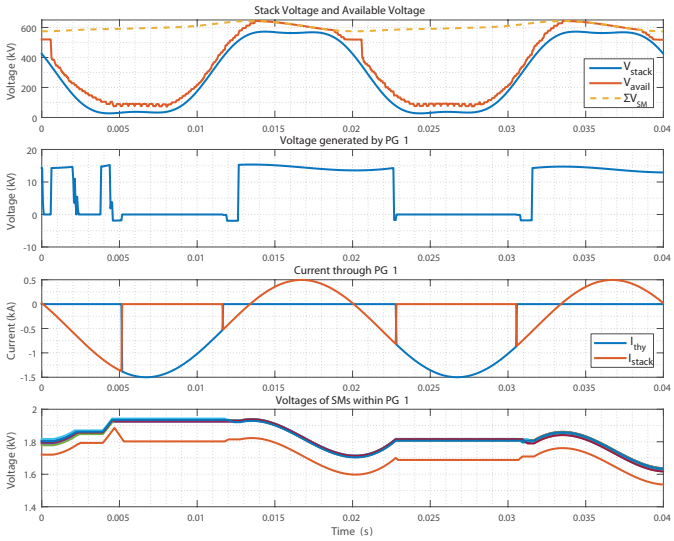

Fig. 10. Overall PG turn-on & turn-off process within an Augmented MMC using proposed differential voltage generation technique simulated in Simulink. V_{avail} is given by the sum of the SM voltages within PGs that do not have active thyristors.

V. Converter Topologies

This section will examine what converter topologies are best suited to be augmented with PGs. Because the thyristor branch within each PG has a significantly lower forward voltage drop in comparison to the SM branch, it is desirable for a PG augmented converter to be capable of utilising this bypass branch as much as possible, however this can only be done when the SMs within that PG are not required to generate a voltage output. To achieve the highest PG thyristor utilisation, and so maximize the efficiency benefits of the PG concept, it is desirable for the overall stack of PGs within the converter to be required to generate a low voltage (i.e. allow most PGs within the stack to bypass themselves through their thyristor branch) when the current flowing through the stack is high, and only generate a high voltage (i.e. most PGs required to use their SMs to generate a voltage output) when the current flowing through it is low.

An emphasis in this study is placed upon converter topologies which are capable of blocking AC current contribution to DC side faults, though it should be acknowledged that PGs could be used to augment non DC fault tolerant converter topologies. The topologies examined in this section are based upon the Modular Multilevel Converter (MMC) [1] and the Extended Overlap Alternate Arm Converter (EO-AAC) [9], [21]. The two topologies examined based upon the MMC are a PG augmented variant of a full-bridge MMC (A-MMC), and a PG augmented variant of the Hybrid MMC variant [3] (AH-MMC), which combines FB and HB-SMs to achieve DC fault tolerance. The AH-MMC is assumed to have a 50:50 split of FB and HB-SMs within each PG.

A toplogy based upon the EO-AAC was also investigated. The EO-AAC is a hybrid topology which combines director switches (series semiconductor switches) and a stack of FB-SMs within each arm in an effort to achieve a VSC with DC fault tolerance, high efficiency and low volume. The EO-AAC

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achieves this while eliminating the six-pulse ripple in the DC current inherent to the previous iterations of the AAC [8]. In the EO-AAC, the third harmonic voltage that is imposed upon the converters voltage waveform was chosen as part of an optimization to improve the efficiency of the converter, by optimizing the required ratio of director switches to FB-SMs within the arm, whilst still retaining DC fault ride through capability [21]. This wave-shape was found to result in poor utilisation of the PG thyristors. Because of this, a variant of the EO-AAC which is operated with a more standard third harmonic modulation was investigated, which was found to result in greater thyristor utilisation, counteracting the power-loss penalty of more required SMs. To reflect the usage of more standard third harmonic injection, as well as the use of PGs, this converter is called the Augmented Trapezoidal Alternate Arm Converter (AT-AAC). It was found possible to eliminate the director switch within this topology, with alternate arm action achieved through current control, without impacting the overall converter efficiency.

The design specifications for the three considered topologies are given in Table. II. The PG design specification given in Table. I is used. The AT-AAC can be seen to require more IGBTs than either of the variants based upon the MMC, this due to the higher AC voltage that the EO-AAC operates at.

TABLE II
SPECIFICATIONS OF THE CONSIDERED CONVERTER TOPOLOGIES. DEVICE QUANTITIES ARE GIVEN PER CONVERTER ARM. % INCREASE IS GIVEN RELATIVE TO A HALF-BRIDGE MMC.

	A-MMC	AH-MMC	AT-AAC
Rated Power	900 MW	900 MW	900 MW
DC Voltage	300 kV	300 kV	300 kV
AC Voltage (L-L RMS)	367 kV	367 kV	489 kV
SM Capacitor	9.6 mF	9.6 mF	6 mF
Rated Voltage of PG Stack (pu)	1	1	1.15
Num. of PGs	42	42	48
Num. of SMs per PG	8	8	8
Num. of SMs (% Increase)	336 (0%)	336 (0%)	384 (14.3%)
Total Num. of IGBTs (% Increase)	1344 (100%)	1008 (150%)	1536 (228%)
Total Num. of Thyristors	252	252	288

The voltage and current waveforms of the three considered converter topologies are given in Fig. 11. As both the A-MMC and the AH-MMC will have identical voltage and current waveforms simulation results from only the A-MMC are shown. The stack voltage of the A-MMC is low when the arm current is at its peak, indicating that there is good potential for having a significant number of PGs within the valve stack utilize their thyristor branch. However at other parts of the cycle, particularly when the stack voltage is high, there is still current flowing in the arm. The alternate arm action of the AT-AAC results in the arm current being at its maximum when the stack voltage is close to zero, while the arm current is zero during the portion of the cycle that the stack voltage is at its maximum. This indicates significant opportunity to utilize the PG thyristors in this topology. One of the metrics that has been devised for comparing the PG augmented converters is the thyristor utilisation ratio, (ϕ_{thy}), which is introduced here. The thyristor utilisation ratio is used as a measure of how much the thyristor path through each PG is used relative to the path through the stack of sub-modules. It can be calculated as by $\phi_{thy} = \frac{\overline{|I_{thy}|}}{\overline{|I_{stack}|}}$.

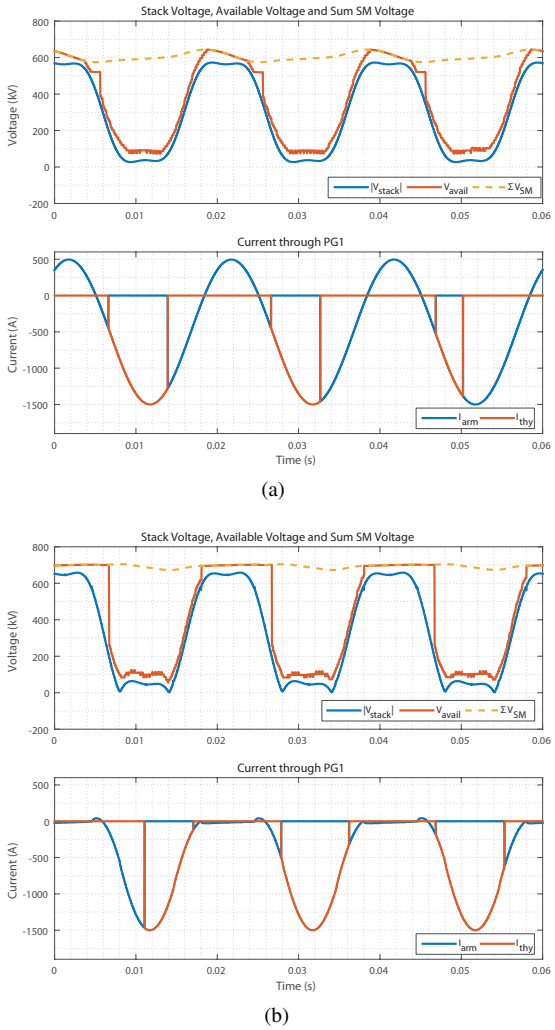

Fig. 11. Stack voltage showing available voltage (indicating PG usage) and current through a single PG. a) A-MMC/AH-MMC b) AT-AAC

Power-loss estimates for the three considered converter topologies operating at rated inverting power are given in Table III. The losses for each topology with the use of the PG thyristors disabled ($\phi_{thy} = 0$) are also given. IGBT conduction, IGBT switching and thyristor conduction losses are estimated using the method presented in [22], assuming the use of a 3.3 kV 1.5 kA IGBT [23]. Values for snubber losses (0.1 J per SM switching event) and thyristor turn-off losses (2 J per thyristor valve turn-off event), assuming the use of the proposed differential voltage technique for turn-on and turn-off of the PG thyristor valves, are taken from the results presented in Sections. III & IV. Turn-on losses for the Infineon T2871N thyristor are assumed to be 2 J/kA, using the data provided for a similarly rated thyristor given in [24].

For each converter the loss reduction (IGBT conduction losses) achieved through the use of the PGs dominates the additional losses associated with the inclusion of the thyristor bypass branch. Both MMC derived topologies show thyristor utilisation values of 0.55, with the A-MMC achieving power-losses that would be expected in the half-bridge MMC and the AH-MMC showing power-losses of below 0.4%. The AT-AAC variants exhibit higher thyristor utilisation values (∼0.7)

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TABLE III
POWER-LOSS ESTIMATES (IN % RATED POWER) FOR THE CONSIDERED TOPOLOGIES OPERATING AT RATED INVERTING POWER. RESULTS ARE GIVEN ASSUMING THE USE, AND NON-USE (ϕ_{thy}=0) OF THE PG THYRISTORS. LOSS REDUCTION GIVEN IN COMPARISON TO A HALF-BRIDGE MMC.

	A-MMC		AH-MMC		AT-AAC	
ϕ_{thy}	0	0.55	0	0.55	0	0.720
IGBT Conduction	0.726	0.273	0.543	0.205	0.602	0.153
IGBT Switching	0.094	0.101	0.093	0.101	0.069	0.080
Thyristor Conduction	0	0.048	0	0.048	0	0.046
Thyristor Turn-On	0	0.019	0	0.019	0	0.018
Thyristor Turn-Off	0	0.003	0	0.003	0	0.004
Snubber	0	0.019	0	0.007	0	0.006
Overall Loss	**0.818**	**0.451**	**0.636**	**0.382**	**0.670**	**0.307**
Loss Reduction	**-79%**	**1.3%**	**-39.2%**	**16.4%**	**-46.6%**	**32.8%**

with subsequent greater reduction in the IGBT conduction losses within the converter. Power losses close to 0.3% are seen for the AT-AAC, an approximate 30% reduction in losses in comparison to the HB-MMC, while achieving DC fault tolerance. This is achieved because the voltage wave-shape of this topology allows higher utilisation of the PG thyristors in comparison to the A-MMC and AH-MMC, resulting in overall lower power-losses despite the increased number of required PGs within each stack. Thyristor utilisation values and power-losses for each converter at several set-points are given in Fig. 12. The converters can be seen to retain their low power-loss values when operating at different power-factors. A slight reduction in PG utilisation, with subsequent impact on power-losses, can be seen at inductive power-factors. This is caused by the increased phase shift between the converter voltage and current waveforms.

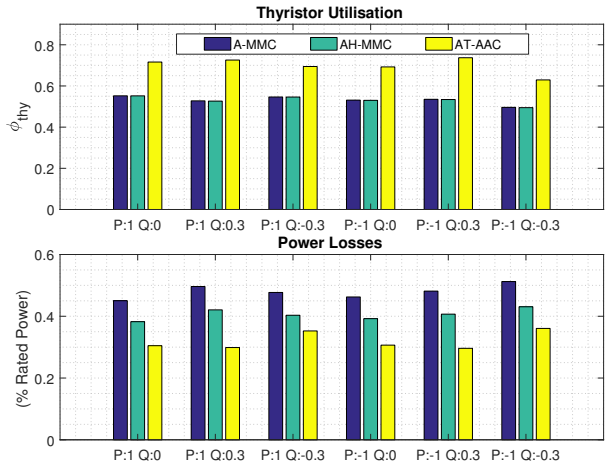

Fig. 12. Thyristor utilisation and power losses of the considered converter topologies at several apparent power set-points. Powers are given in per-unit values and and given referenced to the grid side of the converter transformer.

VI. DYNAMIC RESPONSE TO FAULT SCENARIOS

During steady-state operation it has been found possible to maintain the available voltage within each stack of PGs (given by the sum of the SM voltages within the PGs that do not have either conducting thyristors, or thyristors going through the turn-off process) above the voltage demand from converters current controller by using a modulation technique based upon PS-PWM [25]. The requirement to enforce a hold-off time (of up to 1 ms) on each PG during the turn-off of the PG thyristors, during which the voltage capability of that PG must be restrained, will have an impact on the dynamic response of the converter, limiting its ability to respond during the very initial portion of a fault scenario.

To investigate the potential impact of this, a fault study examining four fault scenarios was carried out using the AT-AAC, which is chosen as the preferred topology due to its low steady-state losses. The AC system was modelled as a voltage source connected to the converter through an impedance giving a short circuit ratio of 2.5 and an X/R ratio of 15. The DC system is modelled as an ideal voltage source connected to the converter's DC bus through a 150 km distributed parameter cable model. The inception angle of each fault was varied by $\frac{\pi}{6}$ intervals referenced to the voltage waveform at the primary of the converter transformer. Both rectifying and inverting conditions were considered. The peak fault current experienced during the four tested AC and DC fault scenarios is given in Table. IV. The highest fault currents can be seen to occur during the line to line transformer fault and the pole to pole DC fault. The peak over-current in the case of the line-to-line AC fault is 2112 A, approximately 1.3 times the peak current under steady-state conditions. This is considered within the transient capabilities of the IGBTs considered [26].

TABLE IV
PEAK CURRENTS EXPERIENCED IN FAULT STUDY

Fault Case	Pre-Fault Power (pu)	Peak Current	Fault Inception Angle
Three Phase Fault	-1	1746	$\frac{5\pi}{6}$
Single Line to Ground Fault	-1	1611	$\frac{10\pi}{6}$
Line to Line Fault at Transformer	-1	2112	$\frac{8\pi}{6}$
DC Pole to Pole Fault	1	1990	$\frac{11\pi}{6}$

Simulation results in Matlab/Simulink of an AT-AAC riding through the worst case pole-to-pole DC fault identified are given in Fig. 13. The fault occurs at t=0.1 s. The DC voltage quickly collapses and oscillates due to ringing in the DC cable. The converter's controller detects the DC fault and initiates the turn-off procedure for all PGs that have active thyristors. At the same time, the converter drops its active power set-point. The utilisation of the PGs limits the converters dynamic response at the start of the fault, resulting in a partial loss of current control. This can be seen with an over-current occurring in the converter, reaching peak values in the region of 1.3 pu. After the PG turn-off procedure has completed the converter regains its full voltage capability and full current control is restored. The DC current is then driven to zero by the converter. The converter remains connected to the AC system throughout the fault and is capable of acting as a STATCOM during this time.

VII. CONCLUSION

This paper has introduced Power-Groups (PGs), a modular multilevel structure of SMs that contains a low impedance thyristor bypass branch, which can be used to bypass the SMs when the PG is not required to generate a voltage output. Simulation results indicate that PGs have the potential to allow

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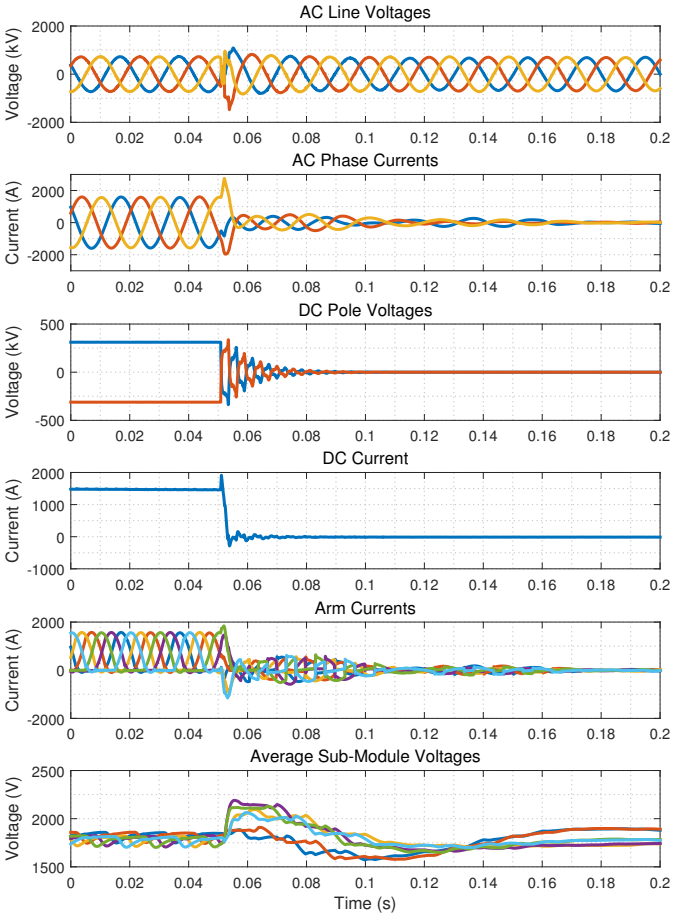

Fig. 13. AT-AAC riding through a pole-to-pole DC fault occurring at t=0.05 s.

voltage source converters with power losses close to 0.3% of rated power to be achieved, while retaining full independent P/Q control, high quality AC and DC current waveforms and tolerance to DC side faults. The inclusion of thyristors within a multilevel voltage source structure introduces numerous challenges in how the structure can be operated while respecting the operating limitations of the thyristor devices themselves. Methods of limiting the dV/dt stress placed across the thyristor valve, as well as methods of controlling the turn-on and turn-off of the thyristor valves with low losses and low required size of the series commutation inductor included within each PG have been presented. The requirement to hold the thyristor valve within each PG reverse biased during the turn-off period results in a significant delay in how quickly the voltage capability of the SMs within each PG can be regained. This impacts both during steady-state operation where a controller capable of anticipating the voltage demand from the current controller must be implemented, and during transient situations where it limits the ability of the converter to respond during the initial portion of a fault. This results in some unavoidable over-currents flowing through the converter at the fault inception. The worst case over-currents identified in a fault study reach magnitudes of approximately 1.3 pu. This is considered within the Safe Operating Area capability of the IGBTs considered for the design [26], and so is not considered an impediment to the practical realisation of the converter.

The Augmented Trapezoidal Alternate Arm Converter (AT-AAC) is considered the most promising topology identified, due to the low power losses that can be achieved while still achieving DC fault tolerance (∼30% lower than the half-bridge MMC). The Augmented Hybrid Modular Multilevel Converter (AH-MMC) also shows promising efficiencies. The AT-AAC requires significantly more semiconductor devices, as well as SMs, thyristor valves and associated ancillary equipment in comparison to non fault blocking topologies such as the half-bridge MMC and other fault tolerant designs such as the Hybrid MMC or Extended Overlap Alternate Arm Converter, however the power-losses achieved with this converter are significantly lower than these non-augmented topologies. The additional capital cost associated with this increase may be offset by the combination of a significant reduction in power-losses, the cost of which typically dominates the capital cost associated with implementing DC fault tolerant converters [27], and a reduction in overall systems costs that a DC fault tolerant converter may enable, such as the replacement of DC circuit breakers with fast dis-connectors.

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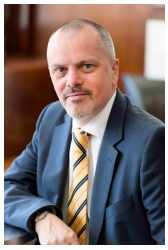

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David R. Trainer recieved his Bsc (Hons) and Ph.D. degrees from Staffordshire Polytechnic, UK, in 1985 and 1991 respectively. Between 1985 and 1998 he worked for GEC on the development of advanced thyristor valves for HVDC power transmission and later pioneered the use of GTO based modular multilevel converter (M2C) technology for reactive power compensation. In 1998, David joined Goodrich working on the development of electric actuation systems for civil and defence aerospace. In 2004 he joined Rolls-Royce to support more electric engine development in the strategic research centre. In 2008, David joined Alstom to work on the development of high power voltage source converters for HVDC power transmission, leading the development of new converter technologies.

Konstantin Vershinin graduated with degree in Applied Physics and Mathematics from Moscow Institute of Physics and Technology, Moscow, Russia in 1998. He has received his PhD degree in power semiconductor devices in 2006 from Emerging Technology Research Centre, Leicester, UK. He has more than 10 years experience in developing of new semiconductor devices and associated processes. He has been involved in development of Clustered IGBT for a range of voltages and oxide flanked MOSFET device for 100V applications. He has joined Alstom in 2014 to work on the next generation of HVDC VSC and LCC valves and new HVDC converter topologies. Currently he is the leading Disruptive System Technologies team at GE's Grid Solutions. He has published more than 50 papers and contributed to 10 patents.