Dimensioning and Modulation Index Selection for the Hybrid Modular Multilevel Converter

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Abstract

The Hybrid MMC, comprising a mixture of full-bridge and half-bridge sub-modules, provides tolerance to DC faults without compromising the efficiency of the converter to a large extent. The inclusion of full-bridges creates a new freedom over the choice of ratio of AC to DC voltage at which the converter is operated, with resulting impact on the converter's internal voltage, current and energy deviation waveforms, all of which impact the design of the converter. A design method accounting for this, and allowing the required level of de-rating of nominal sub-module voltage and up-rating of stack voltage capability to ensure correct operation at the extremes of the operating envelope is presented. A mechanism is identified for balancing the peak voltage that the full-bridge and half-bridge sub-modules experience over a cycle. Comparisons are made between converters designed to block DC side faults and converters that also add STATCOM capability. Results indicate that operating at a modulation index of 1.2 gives a good compromise between reduced power losses and additional required sub-modules and semiconductor devices in the converter. The design method is verified against simulation results and the operation of the converter at the proposed modulation index is demonstrated at laboratory-scale.

I. Introduction

The Half-Bridge (HB) Modular Multilevel Converter (MMC) delivers a high-power voltage source converter with high efficiency and controllability [1]. However it remains weak to DC-side faults because of its inability to generate a negative voltage within its stacks of sub-modules

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(SMs), and therefore inability to control the fault current through the anti-parallel diodes [2] of each SM. If DC fault tolerance is a required feature of the converter, as it may be in overhead line applications or multi-terminal networks, then this issue could be solved by replacing the HB sub-modules (SMs) with Full-Bridge (FB) SMs. However this leads to a significant increase in the overall power losses within the converter, assuming the same modulation index is used [3]. An interesting compromise between these options is a hybrid design [4], in which each arm of the converter contains a stack of SMs that contains a mixture of HB and FB-SMs. By including a sufficient number of FB-SMs within each arm, the converter could be designed to be DC fault tolerant without compromising the overall efficiency of the converter to the same extent that a wholly FB design would. This Hybrid MMC design in illustrated in Fig. 1.

Other options for achieving DC fault tolerance include designing the converter with different sub-module arrangements, such as the Clamp-Double-Sub-Module (CD-SM) [5], Semi-Full-Bridge [6], Diode Clamp Sub-Module (DC-SM) [7] and Clamp Single Sub-Module (CS-SM) [8]. Other hybrid converter topologies, with different operating principles to the MMC, such as the Alternate Arm Converter [9] and the AC-side Cascaded H-Bridge Converter [10] have also been proposed to address this issue. In addition to these other options for preventing AC side fault current contribution to DC faults have been presented, such as the bypass thyristor based methods presented in [11] and [12].

The inclusion of FB-SMs within the converter arm means that the converter's output voltage is no longer constrained by the DC pole voltage (i.e $\pm\frac{V_{DC}}{2}$) [13], allowing the converter to be designed to over-modulate (i.e m $>$ 1) its output during normal operation. As the modulation index (m) (which defines the ratio of the peak AC phase voltage to DC pole voltage) at which the converter operates is increased, the maximum voltage that each arm of the converter must be capable of generating increases, leading to an increase in the overall required voltage rating of the stack, with more semiconductor devices required in the conduction path. At the same time, the AC component of the arm current is reduced leading to a reduced RMS current flowing through each converter arm for a given P/Q set-point. Because of these changes in the current and voltage waveforms, the overall energy deviation of the stacks of SMs within the converter are also impacted. This then has an impact on how each SM is rated, and how the overall voltage capability of stack of SM is chosen so that the converter is capable of operating across its entire P/Q specification.

The possibility of designing the Hybrid MMC to over-modulate its output, and all of the

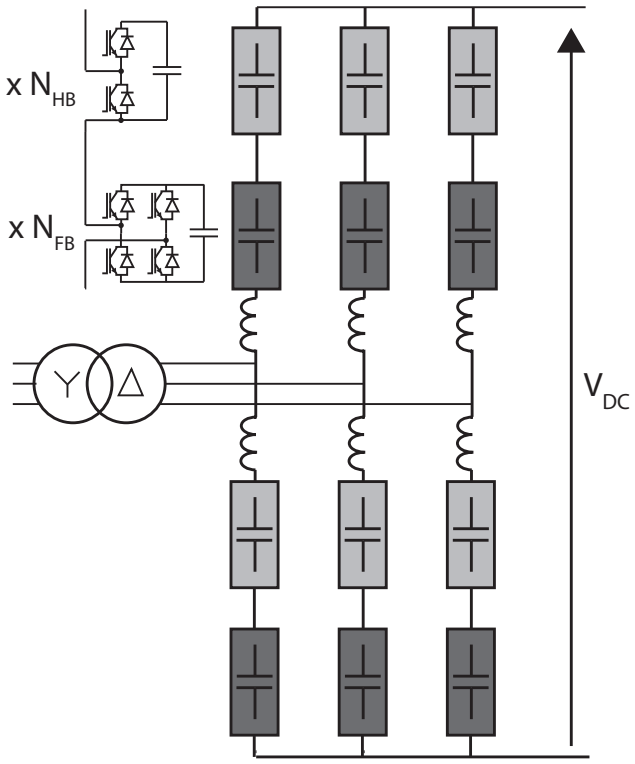


Fig. 1. Hybrid Modular Multilevel Converter

impacts that this will have on its dimensioning has received some attention [6], [13], [14], but a full investigation into what modulation index results in the highest efficiencies has not yet been performed. In [13], the design of the Hybrid MMC, considering operation at modulation indexes of 0.8163 and 1.633 was investigated. Modulation indices between these two values were not considered, but an expression for the required number of FB-SMs to block the AC side contribution to a DC fault was derived. Issues with voltage divergence between the FB and HB-SMs at higher modulation indexes were identified. In [15] the authors consider Hybrid MMC designs with a varying modulation index, as well as the design impact of requiring the converter to operate with a reduced DC voltage during adverse weather conditions in overhead line applications. The impact of the modulation index on the converters energy deviation, with subsequent impact on the design of the converter is neglected. In addition no modulation index is identified as preferable from a power-losses perspective. In [14] analytical expressions for the energy deviation and sub-module capacitor voltage ripple of full-bridge converters were presented as a function of the converters modulation index. The authors propose the use of a modulation index of 1.4 because this was found to result in the elimination of the fundamental component

within the SM capacitor voltage ripple. In [6], an MMC design using Semi-Full-Bridge SMs was presented, but efficiency results were not presented. Following the lead in [14], the authors show experimental results of the converter operating at a modulation index of 1.4. In [16] a method for charging of the SMs during AC side start-up of the converter was presented. An expression for the capacitor ripple voltage was derived as a function of the modulation index. In [17] the design of Hybrid MMCs using various different SM topologies was investigated. However, the analysis was performed assuming a relatively low modulation index of 0.81 in all cases. Other works have focused on the control of Hybrid MMC [18] and its DC fault ride through capability [16], [19] as well as reliability aspects of the design [20]. Other multilevel converter topologies have also been designed to over-modulate their output. The Alternate Arm Converter has been designed to operate at a modulation index of $\frac{4}{\pi}$ (≈ 1.27) as this results in a net zero deviation in the stored energy within the converter over a cycle.

This paper presents full design investigation including analysis of the impact that the choice of modulation index has on the required de-rating of the SMs below their peak rated voltage, the required number of SMs and the efficiency. In Section II, a difficulty with the design is identified where the peak voltage reached by the FB and HB-SMs within the Hybrid MMC at higher modulation indexes do not balance. A solution to this issue is also proposed. In Section III, derivations of the internal voltage, current and energy deviation waveforms of the converter as a function of the modulation index. In Section IV the expressions for the voltage and energy deviation waveforms are employed in a methodology which allows a Hybrid MMC to be designed for a given P/Q specification with a given SM design is presented. The method outputs the nominal voltage at which each SM should be operated, and the required total number of HB-SMs and FB-SMs. The method is extended to the case where the Hybrid MMC is required to be capable of operating as a STATCOM while connected to a shorted DC bus. In Section V, the design method is used to investigate what modulation index gives the highest efficiency. A sweep of designs through a range of modulation indices is performed, examining the required increase in the number of SMs, the ratio of FB-SMs to HB-SMs and the overall converter efficiency. In Sections VI and VII the design methodology is verified against both simulation and lab-scale experiment.

II. Peak Voltage Balancing Mechanism

The Hybrid MMC has a functional limit [21] on the maximum modulation index at which it can operate before the ratio of FB to HBs must be increased past the level required to give DC fault blocking capability. This is because only the FB-SMs are capable of generating the negative portion of the stack voltage waveform, and the different duties of the FB-SMs and HB-SMs results in their energy. At higher modulation indexes it becomes impossible for the SM voltage balancing mechanism to re-balance the imbalance generated during the negative portion of the stack voltage cycle. This leads to an overall energy divergence between FB-SMs and HB-SMs.

One design issue related to the balancing problem that has not been reported is that while it still may be possible to balance the energy content of the FB and HB portions of the arm over each cycle, it may not be possible to do this by the time the overall energy deviation of the stack of SMs reaches its maximum. This condition would result in an imbalance between the peak voltage that the FB-SMs and HB-SMs reach, which may require further de-rating of the nominal SM voltage below the peak rated SM voltage. This would require an increase in the overall required number of sub-modules, and reduction in converter efficiency as a consequence [22]. This problem is illustrated in Fig. 2 for three Hybrid MMC designs at different modulation indexes. It should be noted that the average value each set of SMs can differ, even though the voltage balancing mechanism is attempting to bring the voltage deviation between individual SMs to a minimum.

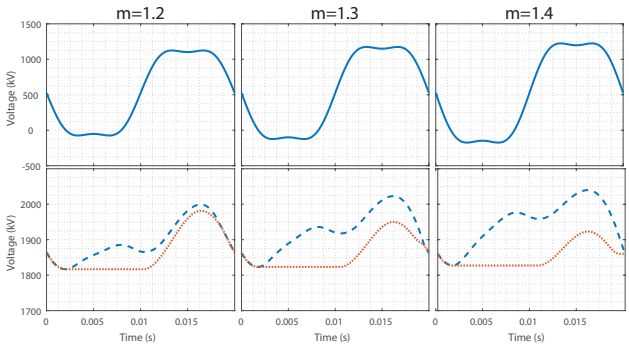


Fig. 2. Average FB-SM and HB-SM voltages in a Hybrid MMC assuming ideal voltage balancing with variation in modulation index. Top: Stack voltage. Bottom: Average FB-SM voltage (dashed), average HB-SM voltage (dotted)

To mitigate this problem a closed loop controller, shown in Fig. 3, has been developed which

adjusts the SM voltages sent to a sorting algorithm based voltage balancing mechanism. To achieve this the controller acts upon the measured error of the peak voltage reached by the average of all SMs, and the peak voltage reached by the average of the HB SMs. This error is passed to a discrete integral controller, which is triggered once per cycle. This integral controller outputs a adjustment factor, ΔV_{adjust}. This adjustment factor adjusts a normalisation factor for the HB-SMs, which is calculated by subtracting ΔV_{adjust} from $V_{\text{SM}_{\text{nom}}}$, while the FB-SMs are normalised by $V_{\text{SM}_{\text{nom}}}$. This has the effective action of causing the SM balancing mechanism, which is based upon a sorting algorithm [32], to preferentially select/de-select the HB-SMs over the FB-SMs. The voltage balancing mechanism is applicable where the overall energy content within the stack of SMs is regulated independently of the SM voltage balancing mechanism and modulation, such as in the controller presented in [31].

The proposed controller only acts upon the voltages passed to SM voltage balancing mechanism during portions of the cycle when P_{stack} is negative (i.e SM capacitors are being discharged), while during portions of the cycle where P_{stack} is positive, un-modified normalised SM voltages are passed to the voltage balancing mechanism. Doing this ensures that the voltage balancing mechanism operates on the actual SM voltages when the SMs are approaching their peak value, allowing effective voltage balancing to take place at this point, limiting any overshoot of individual SMs above the peak average value.

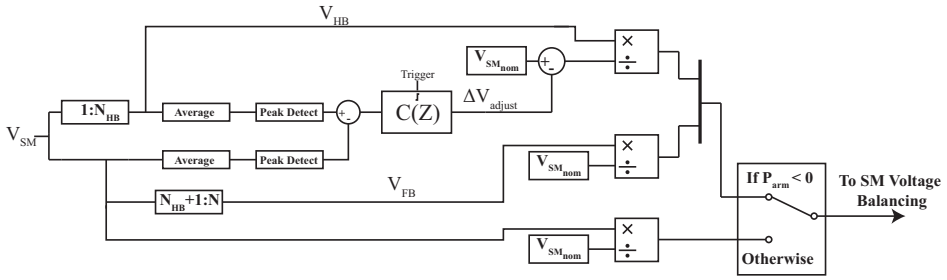


Fig. 3. Peak voltage balancing controller

The operation of this controller is illustrated in Fig. 4, for a Hybrid MMC operating at a modulation index of 1.45, operating at rated rectifying power and 0.3 pu capacitive reactive power. The controller is activated at t=0.04 seconds. Before this an imbalance between the peak FB and HB voltages can be seen, with the FB-SMs reaching higher peak voltages. When the controller is activated the nominal set-points of the FB-SMs and HB-SMs are quickly adjusted,

and the peak voltages reached equalised. The overall average SM voltage within the stack can be seen to be unaffected by the operation of the proposed peak balancing controller.

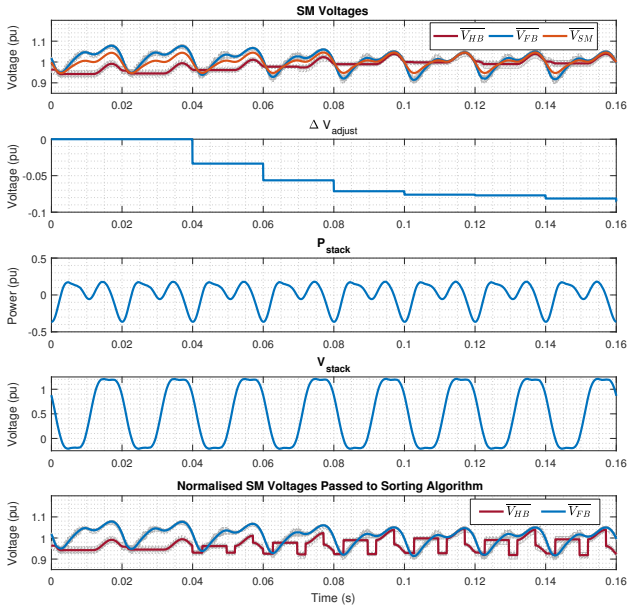
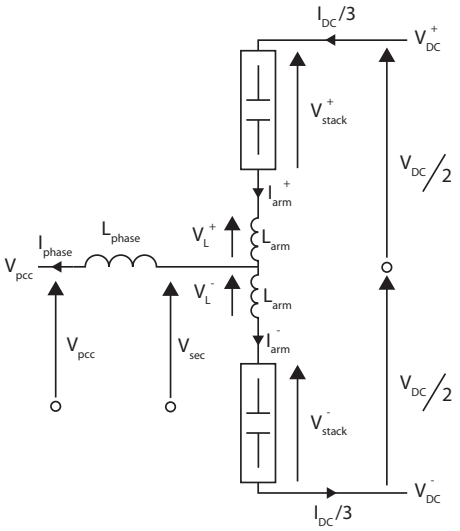


Fig. 4. Peak voltage balancing mechanism acting to balance the peak voltage reached by the SMs. From Top: Average SM voltages. Per unit value of ΔV_{adjust}. Power generated by stack of SMs. Voltage generated by stack of SMs. SM voltages passed to sorting algorithm based voltage balancing mechanism.

III. Converter Waveform Derivation

A single phase diagram of an MMC interfaced to an AC system through a transformer is shown in Fig. 5, where L_{phase} is the leakage reactance of the converter transformer, and L_{arm} are the arm inductors. The leakage inductance of a transmission scale transformer is significant, in the region of 0.14 pu [22]. The voltage rise across the converter transformer can therefore not be ignored when calculating the internal voltage waveforms within the converter. In addition, any P/Q set-point calculation should be referenced to the converter's Point of Common Coupling (PCC) with the AC grid, rather than at the converter terminals.

In this work, it is chosen to define modulation index (m) of the converter as the ratio between the magnitude of the nominal AC phase voltage at the PCC and the nominal DC pole voltage magnitude. The voltage at the PCC can be written as (1), where K_{AC} is a scalar used to represent any variation in the AC voltage around its nominal value ($K_{AC} = \frac{V_{AC}}{V_{AC(nom)}}$).



(a)

Fig. 5. Single Phase Representation of a Modular Multilevel Converter

$$V_{\text{pcc}}(\omega t) = mK_{\text{AC}}\frac{V_{\text{DC}}}{2}sin(\omega t_{pcc}) \tag{1}$$

Assuming that any circulating current is well controlled, the arm inductors represent zero impedance to the DC side, and appear in parallel on the AC side. The points at the top of the upper arm inductor and at the bottom of the lower arm inductor are therefore equipotential [23]. To simplify the analysis it is useful to exploit this fact and do the analysis based on a virtual AC point (V_{c}), that represents the voltage at this equipotential point. The voltage at the this virtual point, V_{c} can be expressed using the per unit system as in (2).

$$V_{\text{c}_{\text{pu}}} = K_{\text{AC}} + \frac{\left|S_{\text{pcc}_{\text{pu}}}\right|^*}{K_{\text{AC}}}j(X_{\text{phase}_{\text{pu}}} + \frac{X_{\text{arm}_{\text{pu}}}}{2}) \tag{2}$$

The voltage at V_c can then expressed as in (3), where the value of K_{c} is given by $\left|V_{\text{c}_{\text{pu}}}\right|$.

$$V_{\text{c}}(wt) = mK_{\text{c}}\frac{V_{\text{DC}}}{2}\sin(\omega t) \tag{3}$$

To calculate the phase current, it is also useful to calculate the AC side power as measured at V_c. This can be calculated as in (4).

$$\overline{S_{\text{c}}} = \overline{V_{\text{c}}} \times \overline{I_{\text{phase}}}^* \tag{4}$$

The currents flowing through the converter can then be derived based upon the converter's P/Q set-point and the AC voltage magnitude, in this analysis both referenced to V_{c}.

The phase current, I_{phase}, can be given as in (5), where ϕ_{c} is given by the angle of $\overline{S_{\text{c}}}$.

$$I_{\text{phase}}(\omega t) = \frac{4}{3}\frac{|S_{\text{c}}|}{mK_{\text{c}}V_{\text{DC}}}\sin(\omega t - \phi_{\text{c}}) \tag{5}$$

The DC current can be expressed as in (6), where K_{DC} is a scalar used to represent any deviation of the DC voltage from its nominal value (V_{DC}).

$$I_{DC} = \frac{|S_{\text{c}}|\,cos(\phi_{\text{c}})}{K_{\text{DC}}V_{\text{DC}}} \tag{6}$$

In an MMC operating under balanced conditions the phase current is split evenly between the upper and lower arms, whilst the DC current is divided equally between all three phases of the converter. The arm current flowing through the upper arm of a phase leg can then be expressed as in (7).

$$I_{\text{arm}}(\omega t) = \frac{2}{3}\frac{|S_{\text{c}}|}{mK_{\text{c}}V_{\text{DC}}}sin(\omega t - \phi_{\text{c}}) + \frac{|S_{\text{c}}|\,cos(\phi_{\text{c}})}{3K_{\text{DC}}V_{DC}} \tag{7}$$

The voltage generated by the upper stack of SMs within the converter, V_{stack}, assuming the use of third harmonic injection, can be written as (8), with the relative magnitude of the third harmonic given by a scalar K_{3rd}.

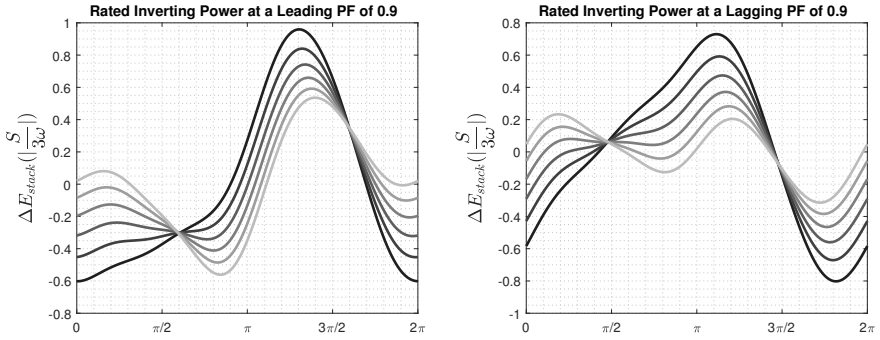
$$V_{\text{stack}}(\omega t) = K_{\text{DC}}\frac{V_{\text{DC}}}{2} - \left(mK_{\text{c}}\frac{V_{\text{DC}}}{2}\sin(\omega t) + K_{\text{3rd}}mK_{\text{c}}\frac{V_{\text{DC}}}{2}\sin(3\omega t)\right) \tag{8}$$

The power exchange of the stack can then be determined as a product of the arm current and the stack voltage, given in (9). Integrating this stack power allows the exchange of energy between the stack and the AC and DC systems, ΔE_{stack}, to be derived (10) [24].

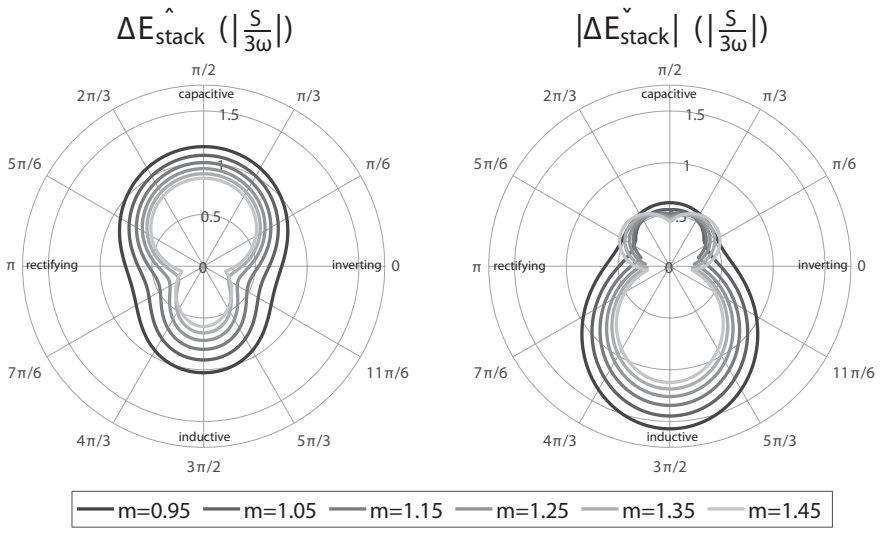
$$\begin{aligned} P_{\text{stack}}(\omega t) = \frac{|S_{\text{c}}|}{3}\Bigg(&\frac{K_{\text{DC}}}{K_{\text{c}}m}\sin(\omega t - \phi_{\text{c}}) \\ &+ \frac{1}{2}\cos(\phi_{\text{c}}) - \sin(\omega t)\sin(\omega t - \phi_{\text{c}}) \\ &- \frac{mK_{\text{c}}}{2K_{\text{DC}}}\cos(\phi_{\text{c}})\sin(\omega t) - K_{\text{3rd}}\sin(3\omega t)\sin(\omega t - \phi_{\text{c}}) \\ &- \frac{K_{\text{3rd}}mK_{\text{c}}}{2K_{\text{DC}}}\cos(\phi_{\text{c}})\sin(3\omega t)\Bigg) \end{aligned} \tag{9}$$

$$\Delta E_{\text{stack}}(\omega t) = \frac{|S_{\text{c}}|}{3\omega}\Bigg(- \frac{K_{\text{DC}}}{mK_{\text{c}}}\cos(\omega t - \phi_{\text{c}}) + \frac{1}{4}\sin(2\omega t - \phi_{\text{c}}) + \frac{mK_{\text{c}}}{2K_{\text{DC}}}\cos(\omega t)\cos(\phi_{\text{c}}) - \frac{K_{\text{3rd}}}{4}\sin(2\omega t + \phi_{\text{c}}) + \frac{K_{\text{3rd}}}{8}\sin(4\omega t - \phi_{\text{c}}) + \frac{K_{\text{3rd}}mK_{\text{c}}}{6K_{\text{DC}}}\cos(3\omega t)\cos(\phi_{\text{c}})\Bigg) \quad (10)$$

~~The maximum and minimum energy deviation of the Hybrid MMC, with variation in modulation index~~ The variation in stack energy deviation at two different power-factors, as well as maximum and minimum values around the P/Q envelope are illustrated in Fig. 6. The energy deviation values have been normalised, as noted in the figure. The max energy deviation, which is linked to the peak voltage that the SMs will reach [25] can be seen to reduce for all power angles with an increasing modulation index. The minimum energy deviation can be seen to decrease with m for inductive power factors, but increase a little for capacitive power factors.



(a) Normalised energy deviation waveforms at rated inverting power at a power factor of 0.9.



(b) Normalised peak and minimum energy deviation of the H-MMC with variation in the modulation index and power angle.

Fig. 6. Variation in the stack energy deviation with modulation index.

IV. Design of the Hybrid MMC for a Given P/Q Specification

The P/Q capability of Modular Multilevel Converters is limited by: (i) the peak rated voltage of the SMs, (ii) the stack voltage limit, (iii) the over-modulation limit (i.e the stack must not attempt to generate a negative voltage) and (iv) the arm current limit [22], [26]. In the Hybrid MMC, the over-modulation limit is removed due to the presence of the FB-SMs within each arm, with the sum FB and HB-SM voltage defining a positive stack voltage limit, and the sum FB-SM voltage defining a negative stack voltage limit.

When dimensioning an MMC, it is desirable to include the minimum number of SMs required in order to maximise the converter's efficiency. This must be done while respecting the operational

limits of each SM, in terms of their peak rated voltage, while ensuring the stack of SMs always has enough voltage available to retain control over the arm current. In this work, it is assumed that the set-point for the nominal SM voltage is the same under all operating conditions. Further optimisations to the design could be made through the use of techniques presented in [27], though these are not considered in this paper.

This section details a methodology which allows a multilevel converter to be designed for a given P/Q specification, given a particular SM design. The variables assumed to be known are the peak rated SM voltage ($V_{\text{SM}}^{\text{max}}$) and the SM capacitor size (C). The method described here finds the nominal SM voltage, and the overall required number of SMs (N) (given by the total number of FB and HB-SMs) that is required for the converter to operate across a given P/Q specification during normal operating conditions. The cases in which the converter must be capable of operating while connected to a shorted DC bus is considered, and an expression that gives the required ratio (K_{FB}) of FB-SMs to overall number of SMs (N) is derived.

1) Peak Sub-Module Voltage Limit: To make the best utilisation of the SMs, and so maximise the efficiency of the converter, the nominal SM voltage should be chosen so that the voltage rating of the SM ($V_{\text{SM}}^{\text{max}}$) should be reached only under the worst case operating condition for steady-state operation [22]. To solve for this condition, it is useful to assume that the SMs are all tightly controlled around their instantaneous mean value, and then solve for the peak rated mean SM voltage [22]. This assumption has been found to be valid for the case of the Hybrid MMC if a mechanism to balance the peak voltage reached by the FB-SMs and HB-SMs, such as the one presented in Section II, is present. The point of the cycle where the instantaneous mean SM voltage reaches its peak within the arm corresponds to the peak positive energy deviation of the stack [25]. The nominal energy within an SM can therefore be expressed as in (11), as the energy in the SM when it is at $V_{\text{SM}}^{\text{max}}$, minus the peak positive energy deviation of the arm (under the worst case specified operating condition) divided by the number of SMs.

$$E_{\text{SM}_{\text{nom}}} = \frac{1}{2} C V_{\text{SM}}^{\text{max}2} - \frac{\Delta \hat{E_{stack}}}{N} \tag{11}$$

Equating (11) and the expression $E_{\text{SM}_{\text{nom}}} = \frac{C}{2} {V_{\text{SM}_{\text{nom}}}}^2$ for the nominal SM energy and then rearranging for the nominal SM voltage gives (12).

$$V_{\text{SM}_{\text{nom}}} = \sqrt{V_{\text{SM}}^{\text{max}2} - \frac{2\Delta \hat{E_{stack}}}{NC}} \tag{12}$$

2) Stack Voltage Limit: The maximum voltage that each converter stack is capable of generating is given by the sum of the SM capacitor voltages within the stack. This voltage is a time varying value due to the energy deviation of the stack over each cycle. When dimensioning the converter, it must be ensured that the converter has sufficient voltage capability to meet the voltage demand at all operating points. At the same time it is desirable to limit the amount of SMs included within the stack to ensure high efficiency. Some safety margins on the stack voltage capability should also be considered in order to allow for disturbances to the energy levels (and hence voltage capability) within the converter during fault conditions. In this work it was found to be useful to specify this safety margin in terms of energy. The energy safety margin, E_{safety}, represents the amount of energy by which a converter stack can be perturbed downwards, and still be capable of generating all specified P/Q set-points across all AC grid conditions. For the case of the Hybrid MMC, two energy safety margins are considered, one based upon the positive arm voltage capability E^{+}_{safety} and the other on the negative arm voltage capability E^{-}_{safety}.

The stored energy within the converter stack, assuming the energy safety margin has been depleted, can also described by sum of the energy within the SMs at their nominal voltage, plus the deviation of the stored energy within the stack, $\Delta E_{stack}(\omega t)$, given by (10), minus the safety margin, E^{+}_{safety}. This is expressed in (13).

$$E_{\text{stack}_{\text{safe}}}(\omega t) = N\frac{1}{2}CV^{2}_{\text{SM}_{\text{nom}}} + \Delta E_{\text{stack}}(\omega t) - E^{+}_{\text{safety}} \tag{13}$$

Assuming the overall deviation in voltage between SMs is relatively small, the instantaneous maximum available voltage within the stack, considering the safety margin, can be calculated as in (14).

$$V_{\text{avail}_{\text{safe}}}(\omega t) = \sqrt{\frac{2NE_{\text{stack}_{\text{safe}}}(\omega t)}{C}} \tag{14}$$

When operating at its design limit in terms of voltage capability, an MMC will be utilising the voltage capability of all of the SMs within each stack of the converter, assuming the energy content of the stack has been depleted by its safety margin. Fig. 7 illustrates this point. The available voltage within the stack, considering the safety margin, can be seen to intersect the stack voltage at one point during the cycle, denoted ωt_{crit}.

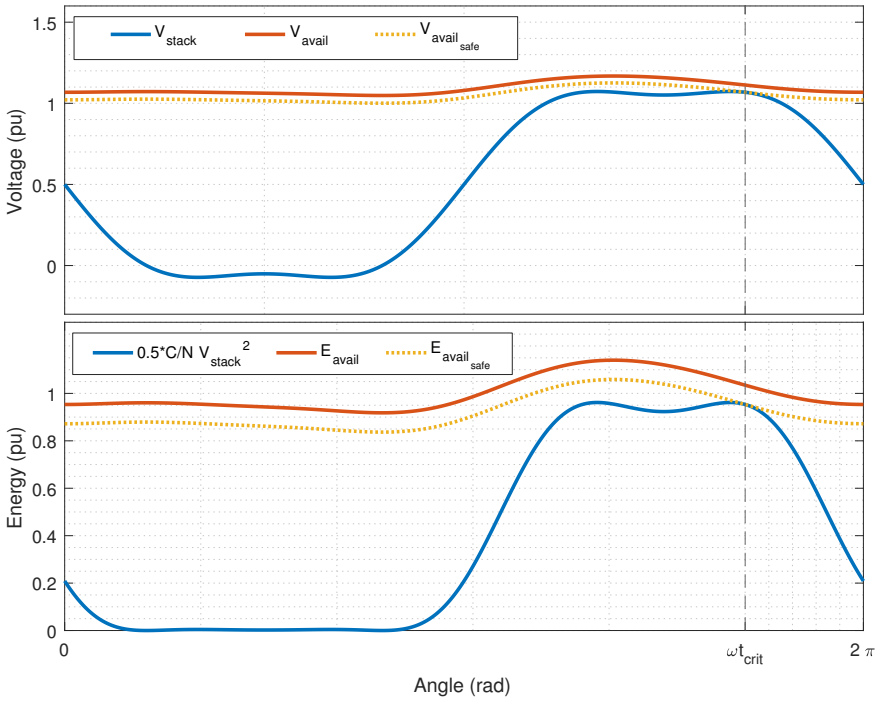


Fig. 7. Stack voltage and arm energy levels when the converter is operating at its voltage limit. Top: Stack voltage, available voltage and available voltage with safety margin. Bottom: Instantaneous required energy to meet stack voltage demand, stack available energy, stack available energy with safety margin.

At this critical angle, the instantaneous stack voltage will equal the total available voltage within the stack. The stack voltage at the critical angle can therefore be be linked to the available voltage within the stack by (15). This can be rearranged in terms of the energy stored within the stack at this point to give (16).

$$V_{\text{stack}}(\omega t_{\text{crit}}) = V_{\text{avail}_{\text{safe}}}(\omega t) = \sqrt{\frac{2N E_{\text{stack}_{\text{safe}}}(\omega t)}{C}} \tag{15}$$

$$E_{\text{stack}}(\omega t_{\text{crit}}) = \frac{1}{2}\frac{C}{N} V^2_{\text{stack}}(\omega t_{\text{crit}}) \tag{16}$$

~~The stored energy within the converter stack, assuming the energy safety margin has been depleted, can also be described as the sum of the energy within the SMs at their nominal voltage, plus the deviation of the stored energy within the stack, $\Delta E_{stack}(\omega t)$, given by (10), minus the safety margin, E^{+}_{safety}. This is expressed in (13).~~

Equations (16) and (13) can be equated to give (17), which is only valid at the critical angle. The unknown terms within this equation are the number of SMs (N), and the nominal SM voltage ($V_{\text{SM}_{\text{nom}}}$).

$$\frac{1}{2}\frac{C}{N}V_{\text{stack}}(\omega t_{\text{crit}})^2 = N\frac{1}{2}CV_{\text{SM}_{\text{nom}}}{}^2 + \Delta E_{\text{stack}}(\omega t_{\text{crit}}) - E^{+}_{\text{safety}} \tag{17}$$

The exact location of the critical angle is dependent on the level of energy storage within the converter, as governed by both N and $V_{\text{SM}_{\text{nom}}}$ and is closely related to the point at which the energy is lowest, but the voltage demand highest. Taking (17) and dividing both sides by the expression for the nominal energy ($N\frac{1}{2}CV^2_{\text{SM}_{\text{nom}}}$) gives (18).

$$\frac{V^2_{stack}(\omega t_{\text{crit}})}{N^2V^2_{SM_{nom}}} = 1 + \frac{\Delta E_{\text{stack}}(\omega t_{\text{crit}}) - E^{+}_{\text{safety}}}{N\frac{1}{2}CV_{SM_{nom}}} \tag{18}$$

Rearranging this expression gives (19).

$$V_{stack(nom)} = NV_{SM_{nom}} = V_{stack}(\omega t_{\text{crit}})\sqrt{\frac{1}{1+\frac{\Delta E_{\text{stack}}(\omega t_{\text{crit}})-E^{+}_{\text{safety}}}{N\frac{1}{2}CV^2_{SM_{nom}}}}} \tag{19}$$

The critical point is the point which maximises (19), i.e maximises the required voltage capability within the stack. When first solving for the critical angle an estimate for the nominal energy (E^{est}_{nom}), given by $N\frac{1}{2}CV^2_{\text{SM}_{\text{nom}}}$, within the converter can be made. The critical angle can then be found from (20). To ensure the critical angle has been found, the entire design process can be iterated with the value of E^{est}_{nom} updated based on the previous results. This has been found to converge within 1-2 iterations of this process.

$$\omega t_{crit} = \arg\max_{\omega t}\left\{V_{stack}(\omega t)\sqrt{\frac{1}{1+\frac{\Delta E_{\text{stack}}(\omega t)-E^{+}_{\text{safety}}}{E^{est}_{nom}}}}\right\} \tag{20}$$

3) Solving for N and V_{SM}: The converter design must be done while simultaneously solving for the conditions on the peak rated sub-module voltage limit and the stack voltage limit. This can be done by substituting (12) into (17). Grouping terms gives the second order polynomial expression (21). Solving for the roots of (21) and then choosing the positive root that satisfies the condition: $V_{\text{SM}_{\text{nom}}} \leq V^{\text{max}}_{\text{SM}}$, gives the required number of SMs within the arm. The nominal energy within a single SM can then be calculated from (11), which then allows the nominal SM voltage to be solved using (12).

$$N^2\left(\frac{C}{2}V_{\text{SM}}^{\max 2}\right) + N\left(- \Delta\hat{E_{stack}} + \Delta E_{\text{stack}}(\omega t_{\text{crit}}) - E_{\text{safety}}^{+}\right) - \frac{C}{2}V_{\text{stack}}(\omega t_{\text{crit}})^2 = 0 \quad (21)$$

To design for a given P/Q specification, the required value of N can be checked for each outer point of the P/Q specification, with the values of $V_{\text{stack}}^{\text{crit}}$ and ΔE^{crit} recalculated for each operating point and using the maximum value of $\Delta\hat{E_{stack}}$ across the P/Q specification. The required number of SMs can then be taken as the resulting worst case value of N.

A. Rating for Blocked Operation during DC Faults

If the converter is designed to simply block the AC side current contribution to a fault on the DC side then the FB portion of the stack can be sized according to the maximum AC line voltage, following the analysis presented in [21]. The number of required FBs, N_{FB}, within each arm is then given by the rating of the FB stack, divided by the nominal SM capacitor voltage. The number of FBs N_{FB} can then be given by (22).

$$N_{\text{FB}} = \frac{\sqrt{3}}{2}\frac{m\hat{K_{\text{AC}}}V_{\text{DC}}}{V_{\text{SM}_{\text{nom}}}} \quad (22)$$

B. Rating for DC Fault Ride Through & STATCOM Operation

The negative voltage capability of each stack of SMs is given by the sum of the capacitor voltages of the FB-SMs within the stack. If the converter needs to be rated to perform a DC fault ride through (i.e., retain current control throughout the fault), as well as provide STATCOM capability when the DC bus is shorted, then the sizing of the FB portion of the stack can be carried out in a similar manner to the overall stack so that neither the peak SM voltage limit or the stack voltage limit are breached under the specified operating envelope. In general the stack voltage limit has been found to be the limiting factor, and so the design under this assumption is given here.

In this case the number of FB-SMs must be chosen so that the FB-SMs have sufficient voltage capability to ensure operation under the worst case specified operating condition. As with the positive voltage capability some safety margin (E_{safety}^{-}) should also be applied to the negative voltage capability to account for disturbances to the overall energy content of the FB-SMs. As with the positive voltage capability this safety margin can be specified in terms of energy. Under the assumption that the same capacitor and nominal voltage are used for both the FB-SMs and

HB-SMs, then the ratio K_{FB} also describes the ratio of the nominal energy stored within the FB-SMs, to the nominal energy stored within the overall stack. In this case then the value of K_{FB} can then be found by adapting (17) for the DC Fault (DCF) case. This is given in (23).

$$\frac{1}{2}\frac{C}{K_{\text{FB}}N}V_{\text{stack}}^{\text{DCF}}(\omega t_{\text{crit}})^2 = K_{\text{FB}}N\frac{1}{2}CV_{\text{SM}_{\text{nom}}}{}^2 + \Delta E^{\text{DCF}}(\omega t_{\text{crit}}) - E^{\text{-}}_{\text{safety}} \tag{23}$$

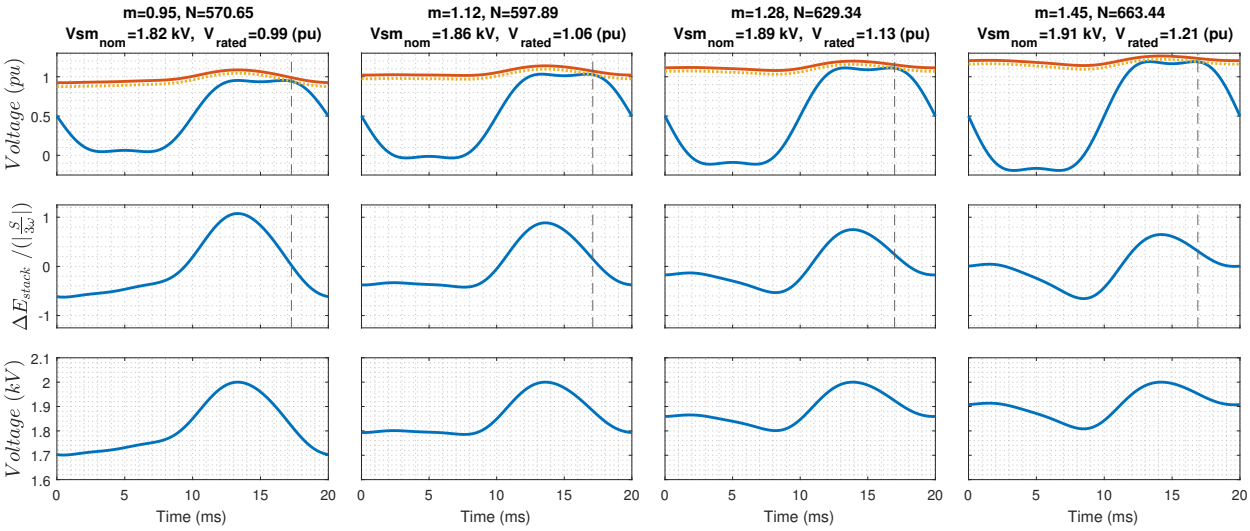
This can be re-arranged in terms of K_{FB}, into the form of a second order polynomial, which is given in (24). The required value of K_{FB} can be found by taking the positive root of this expression. The worst case can be found by sweeping the outer design specifications for STATCOM operation during DCF conditions.

$$K_{\text{FB}}^2(NV_{\text{SM}_{\text{nom}}})^2 + K_{\text{FB}}(NV_{\text{SM}_{\text{nom}}})^2\Big(\frac{\Delta E^{\text{DCF}}(\omega t_{\text{crit DCF}}) - E^{\text{-}}_{\text{safety}}}{N\frac{1}{2}CV_{\text{SM}_{\text{nom}}}{}^2}\Big) - V_{\text{stack}}^{\text{DCF}}(\omega t_{\text{crit DCF}})^2 = 0 \tag{24}$$

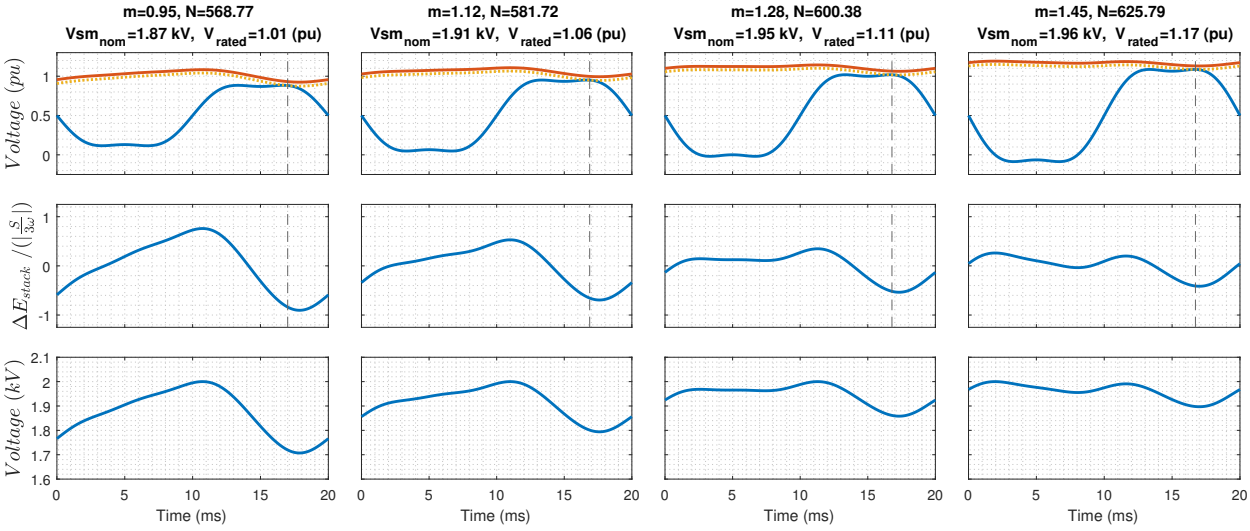
V. Design Analysis

Solving for the required number of SMs (N) within the converter, using (21), requires the the peak energy deviation of the stack, and the stack voltage and energy deviation at the critical point to be found. Figure 8 illustrates how these values vary with the converters modulation index, and how they impact the design of the overall converter when considering operation at leading and lagging power-factors. For illustrative purposes each design in this plot considers only a single set-point with no AC voltage variation. As the modulation index increases the energy deviation waveform the stack changes considerably for both leading and lagging operation. When examining lagging power-factors, it can be seen that the critical point occurs when the energy deviation is approaching its nadir value, meaning that the overall available voltage within the stack is also approaching its nadir. As the modulation index increases this nadir value for a given set-point decreases. From design perspective this results in a lessening in the requirement to increase the rated voltage of the overall stack (given by the product of N and V_{SM_nom}) above the value of the stack voltage at the critical point. For leading power factors this effect is less pronounced as the critical point occurs when the energy deviation is at a positive value (i.e the voltage capability within the stack at that point is above its nominal value).. At lower modulation indexes the required value of N is broadly equal for operation at both leading and lagging power-factors. However, as the modulation index increases the design burden for leading power-factors becomes considerably more pronounced than that for lagging power-factors. This

is because of the decreasing value of the energy deviation of the critical point for lagging power-factor operation. In addition the peak energy deviation at lagging power-factors is below that at a leading power-factor. This results in a higher allowable peak average SM voltage, further reducing the overall required value of N.



(a) Design for Rated Inverting Power at a Leading Power Factor of 0.9



(b) Design for Rated Inverting Power at a Lagging Power Factor of 0.9

Fig. 8. Variation in the required values of N and $V_{SM_{nom}}$ with modulation index. Designs are done considering only single set-points and no variation in AC voltage. Top: Stack Voltage, Available Voltage and Available Voltage considering the energy safety margin. Middle: Normalised energy deviation of the stack. Bottom: Average SM Voltage. The dashed line in the upper two sub-plots shows the location of the critical point.

To investigate the design of the Hybrid MMC considering realistic design specifications for P/Q capability and AC voltage variation a detailed design sweep ~~of a Hybrid MMC designed~~

using the methodology presented in the Section IV was carried out for three SMs capacitor sizes. A 9 mF SM capacitor was chosen as the base case capacitor as this SM capacitor size results in a half-bridge MMC design (at m=0.96) that has an energy storage equivalent to 33.8 kJ/MVA, which is in line with industrial estimates of required energy storage [26]. SM capacitors of 7 mF and 11 mF, corresponding to energy storage equivalents at m=0.96 of 26.8 kJ/MVA and 41 kJ/MVA respectively, were chosen to give some variance around the base case value. The inputs to the design script are given in Table. I. The P/Q specification used is taken from the GB grid code requirements for voltage source converters [28]. It calls for the converter to be capable of generating 0.3/-0.5 pu reactive power (capacitive reactive power given as positive), whilst at ± 1 pu active power (inverting power given as positive) over a $\pm 5\%$ variation in AC voltage. The DC voltage is assumed to be well controlled to its nominal value.

TABLE I
CONVERTER DESIGN SPECIFICATION

Design Inputs	
Rated Power	1.575 GW
Modulation Index	1.2
Q at Rated Power	0.3/-0.5 pu
Q under DC Fault Conditions	0.3/-0.5 pu
DC Voltage	+-525 kV
AC Voltage Variation	+-5%
Peak SM Voltage	2000 V
E_{safety}	3 kJ/MVA
$E_{\text{safety}_{\text{FB}}}$	3 kJ/MVA
Transformer Leakage Reactance	0.14 pu
Arm Inductor	0.1 pu

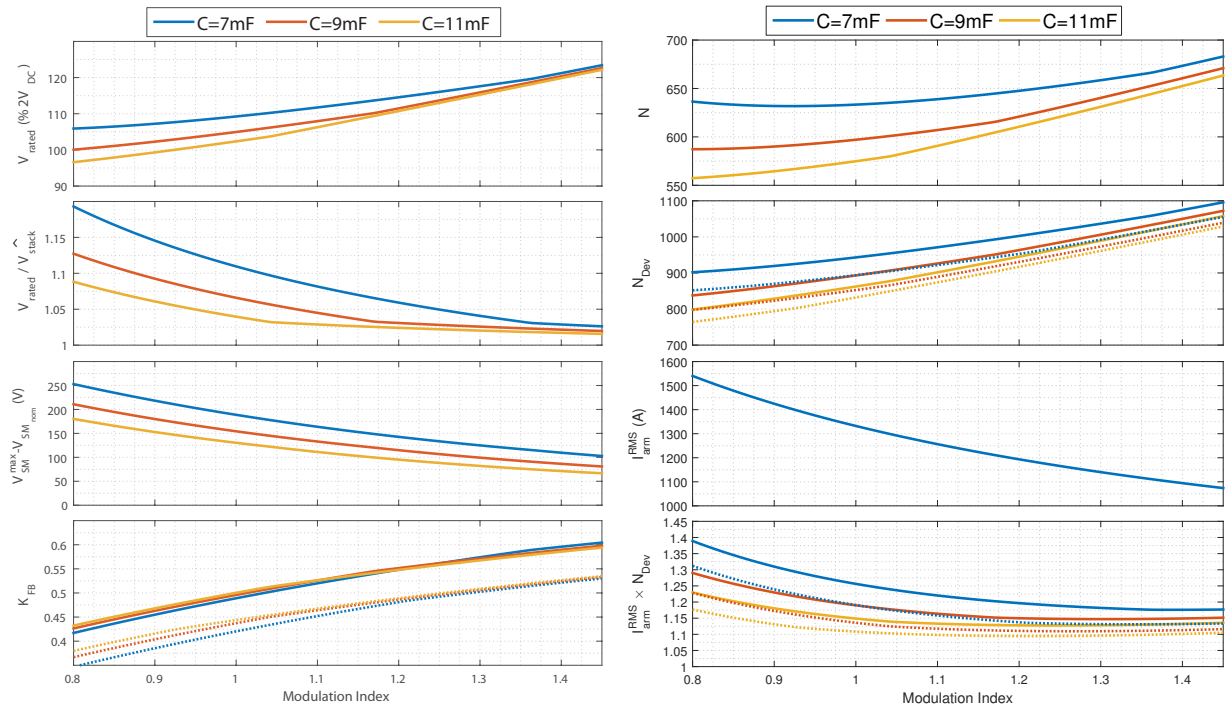
The results from a design sweep, with variation in the modulation index from 0.8 to 1.45, for the three SM capacitor sizes are shown in Fig. 9. This illustrates how the modulation index that the converter operates at impacts the overall design. A maximum modulation index of 1.45 was considered the Hybrid MMC experiences issues in divergence in energy between the FB and HB SMs if the modualtion index is increased mcuh beyond this point [13], [15]. As the modulation index is increased, the rated voltage of the stack (shown at top left (a)(i) and given by the product

of N and $V_{SM_{nom}}$) can be seen to increase for all three capacitor sizes. The required number of SMs (N) to achieved this rated voltage (shown at the top right (b)(i)) however can be seen to be approximately constant from $m \approx 0.8$ to $m \approx 1.05$, despite the increased required voltage rating of the stack. Past $m \approx 1.2$ the required number of SMs increases at a shallow rate for all three capacitor sizes considered. This shallow increase is caused by the reduced energy deviation of the stacks of SMs as the modulation index is increased, as illustrated in Fig. 6. This has two major impacts on the converter design, which offset the need for more SMs. The first impact is shown in Fig. 9(a)(ii), showing the required ratio of the rated stack voltage to the peak stack voltage demand in order to operate without breaching the specified safety margins. This reveals a sharp decline from $m \approx 1$ to $m \approx 1.2$, with the effect more pronounced with the smaller SM capacitor sizes. The second factor is shown in Fig. 9(a)(iii) and shows the required de-rating applied to each SM to ensure it does not exceed its peak voltage rating. This also reduces as m increases, resulting in greater utilisation of each SM. These factors combine to reduce the required increase in SMs as the modulation index increases. At lower modulation indexes there can be seen to be a large variation in the required value of N with the SM capacitor size, this variation can be seen to reduce as the modulation index is increased.

The value of K_{FB}, shown in the bottom sub-plot of Fig. 9a can be seen to increase as the modulation index increases. There is an approximate 0.05 difference between the designs that are required to simply block the DC fault (shown in dashed lines), and those that are required to perform STATCOM operation while the DC bus is shorted (shown in solid lines). At m=1 the value of K_{FB} is close to 0.45, increasing to 0.6 at m=1.45. K_{FB} is seen to vary little with the SM capacitor size. ~~For designs which are required to simply block the fault current, the required value of K_{FB} is approximately 0.07 below that of the designs required to operate as a STATCOM.~~

Conduction losses dominate the power-losses within modular multilevel converters at HVDC scale. To make an estimate of the expected power-losses, the number of devices (1 for each HB-SM, 2 for each FB-SM) within the conduction path (N_{Dev}) can be calculated using $N_{\text{Dev}} = N \times (1 + K_{FB})$. This is shown in Fig. 9b(ii). The RMS current flowing through the arm ($I_{\text{stack}}^{\text{RMS}}$), which is same for all designs, decreases as the modulation index is increased due to the reduced AC current component flowing through the converter arms. The product of $I_{\text{arm}}^{\text{RMS}}$ and N_{Dev}, is used as an indicator of the expected power-losses within the converter, and is shown in the last sub-plot of Fig. 9b(iv). This shows a significant decrease as the modulation index is increased

from 0.8 to 1.2. From 1.2 to 1.4 it is relatively level, with a slight upwards trend observed as the modulation index increases past 1.4. This indicates that most of the power-loss reduction benefits that may be achieved by designing the Hybrid MMC to over-modulate are achieved by operating with a modulation index of 1.2, with little further reduction after this point.



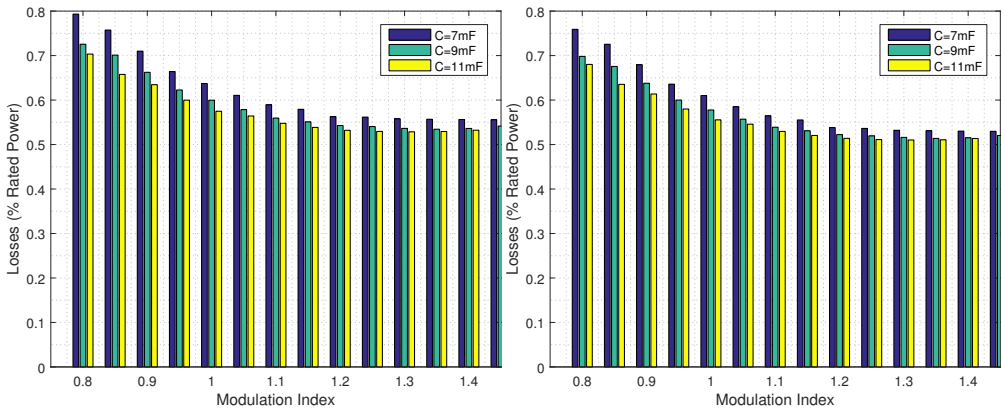
(a) (b)

Fig. 9. Hybrid MMC design variation with modulation index. a) From top: Rated voltage of arm (% DC pole to pole voltage), ratio of V_{rated} to $\hat{V_{stack}}$, required de-rating of nominal sub-module voltage from peak voltage rating, ratio K_{FB} of FB-SMs to HB-SMs. b) From top: Number of SMs (N), Number of devices in the current path (N_{Dev}), RMS Arm current at rated inverting power, product of RMS arm current and N_{Dev}. Solid lines show rating for STATCOM operation, dashed lines show rating for blocked operation.

Efficiency estimates for Hybrid MMC designs were undertaken for the choices of SM capacitor size, using time domain simulation models of the Hybrid MMC implemented in Matlab/Simulink, and with stepped changes of 0.05 in modulation index. Power-losses were estimated using the method presented in [29] and the results of this are shown in Fig. 10. The IGBT used was a 3.3 kV 1500 A device from ABB semiconductors [30]. As noted in [15], the decreasing AC current magnitude as the modulation index increases opens up the possibility of uprating the converters power rating, as the peak current rating of the IGBTs used will not be fully exploited. In a practical system the level to which this would depend on the limitations of the DC cable

or overhead line that the converter is connected to. Alternatively a smaller IGBT could be used at higher modulation indexes, however this would likely negate the efficiency gains achieved by increasing the modulation index, and so is considered undesirable. Efficiency results, assuming the use of the same IGBT in all cases, show a relatively sharp decrease in the overall losses as design is moved into the over-modulation region. Most of the gain in efficiency is achieved by a modulation index of 1.2, with only small further gains beyond this.

At lower modulation indexes there is noticeable variation in the power-losses with the SM capacitor choice, with designs with larger SM capacitors showing lower losses. This difference is reduced, though not eliminated, as the modulation index is increased. This indicates that a SM capacitor which may be an undesirable choice, for power-loss reasons, for use in a design at lower modulation indexes may be a more viable as a choice in an over-modulating design. The reduced cost associated with a smaller capacitor size could also offset some of the increased capital cost associated with the increased number of SMs.



(a) (b)

Fig. 10. Variation in estimated losses in a H-MMC designed with a 9 mF SM capacitor with the modulation index a) Rating for STATCOM operation during DC faults b) Rating for DC fault blocking

To illustrate the design options which exist with the Hybrid MMC, with associated penalties in terms of number of SMs, semiconductor device count and power-losses, a comparison was undertaken between designs at m=0.96 and m=1.2, and a half-bridge MMC design at m=0.96. The results of this comparison are given in Table. II. The modulation index for the under-modulating designs was chosen so that their stack voltage under the worst case operating condition (rated power, rated capacitive reactive power, maximum AC voltage) still leaves a 5% margin in converter voltage with respect to the DC voltage. For Hybrid MMC designs that

TABLE II
CONVERTER DESIGN COMPARISON

	Half-Bridge MMC	Hybrid-MMC	Hybrid-MMC	Hybrid-MMC	Hybrid-MMC
V_{DC}	±525 kV	±525 kV	±525 kV	±525 kV	±525 kV
V_{AC} (Line to Line RMS)	617 kV	617 kV	617 kV	772 kV	772 kV
Modulation Index (m)	0.96	0.96	0.96	1.2	1.2
DC Fault Strategy	NA	Block	STATCOM	Block	STATCOM
C	9 mF	9 mF	9 mF	9 mF	9 mF
Nominal SM Voltage	1.836 kV	1.836 kV	1.836 kV	1.882 kV	1.882 kV
Total number of SMs per arm	589	589	589	625	625
Number of Half-Bridges per arm	589	338	297	320	277
Number of Full-Bridges per arm	0	251	292	305	348
Number of IGBTs per arm	1178	1680	1762	1860	1946
Nominal Energy Storage (kJ/MVA)	34	34	34	37.95	37.95
% Power Loss at Rated Inverting Power	0.4462	0.5889	0.6097	0.5148	0.5365

are capable of STACOM operation, power-loss reductions in the region of 12% (corresponding to 0.065% of rated power) can be seen when moving from a design at m=0.96 to a design with m=1.2. The required increase in the overall number of SMs to achieve this is approximately 6%, with an approximate 10% increase in the required number of IGBTs (because of the increased ratio of FB-SMs to HB-SMs). Similar power-loss reductions and required increases in number of SMs are seen in the cases where the converter is designed to block. Rating the converter to be capable of operating as a STATCOM, rather than blocking during a fault, carries a power-loss penalty of approximately 0.02% of rated power, and an approximate 4.5% increase in the required number of IGBTs. The most efficient DC fault tolerant design in this group (m=1.2, rated to block) incurs a power-loss that is approximately 15% higher than the HB MMC design.

A P/Q capability graph of a Hybrid MMC with a 9 mF SM capacitor operating at m=1.2 is shown in Fig. 11 to illustrate the overall P/Q capability of the Hybrid MMC operating at this modulation index. In a HB-MMC the limiting factor on the stack voltage limit is typically at a set-point of full rated power plus full rated inductive power-factor, while the peak SM voltage limit is reached at rated power, rated capacitive power-factor [22]. In over-modulating Hybrid MMC it has been found that both of these limits occur at full rated power plus full rated capacitive reactive power. This is in line with the energy deviation plots shown in Fig. 6

which showed an increase in the stack energy deviation nadir magnitude as the modulation index increases at capacitive power-factors, with a reduction in this nadir magnitude seen at inductive power-factors. The current limit shown is taken as the minimum required current limit to allow an equivalently rated converter designed at a modulation index of 0.96 to function. Overall the converter exhibits significant reactive power capabilities, as well as some over-head margin in terms of active power capability, due to the reduced AC component in the arm current, which could be exploited..

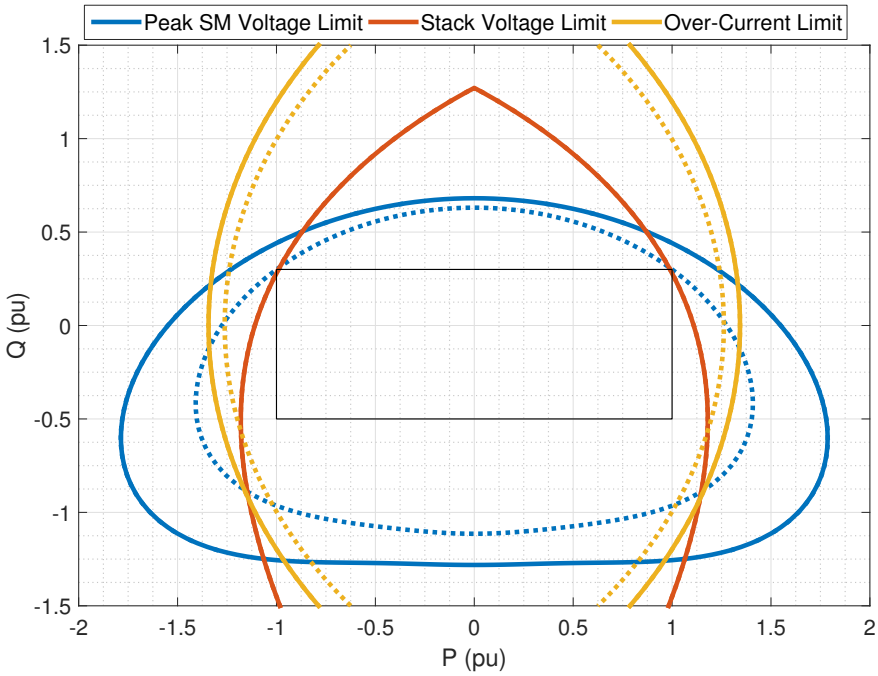


Fig. 11. P/Q capability graph of Hybrid MMC with a 9mF SM capacitor designed to operate at a modulation index of 1.2. Solid lines show limit at AC voltage 105% nominal, dashed lines show limits at AC voltage 95% nominal

This section has examined how the modulation index that the Hybrid MMC is operated impacts the overall design. It has been found that the reducing energy deviation as the modulation index increases results in better utilisation of each sub-modules rated peak voltage, plus a reduced requirement on the overall voltage rating of the stack. These factors combined with the reducing AC current magnitude cause a reduction in power-losses in the converter, the majority of which are accrued by a modulation index of 1.2.

VI. Simulation Results

A detailed simulation model of a Hybrid MMC was implemented in MATLAB/Simulink and was configured to operate at a modulation index of 1.2 and operate as a STATCOM during DC faults. The specification for the converter is the same as those given in Table II, with the additional circuit values given in Table I. The converters controller uses an LQR current controller with energy management system that ensures the correct energy levels are maintained within each converter arm [31]. Voltage balancing of SMs within each stack is achieved using a tolerance band method, similar to the one described in [32]. Separate sorted lists are generated for positive and negative voltages, to account for the inability of the HB-SMs to contribute to neagtive voltage genration.

The four outer corners of the P/Q specification were tested at both extremes of the AC voltage variation. Results from the converter when operating during inverting operation are given in Figure. 12. In the results inverting active power and capacitive reactive power are defined as positive. At P:1 Q:0.3 pu at 105% nominal voltage, shown in Fig. 12a, the peak average SM voltage can be seen (label: A) to intersect the design value of 2000 V. At P:1 Q 0.3 pu at 95% nominal voltage, shown in Fig. 12a, the stack voltage can be seen to intersect (label:B) with the safety margin applied to the overall available voltage within the stack. At the other two operating conditions, given in Fig. 12b and 12c, the stack voltage and peak average SM voltage stay below the specified limits. This is in agreement with the P/Q capability graph shown in Fig. 11.

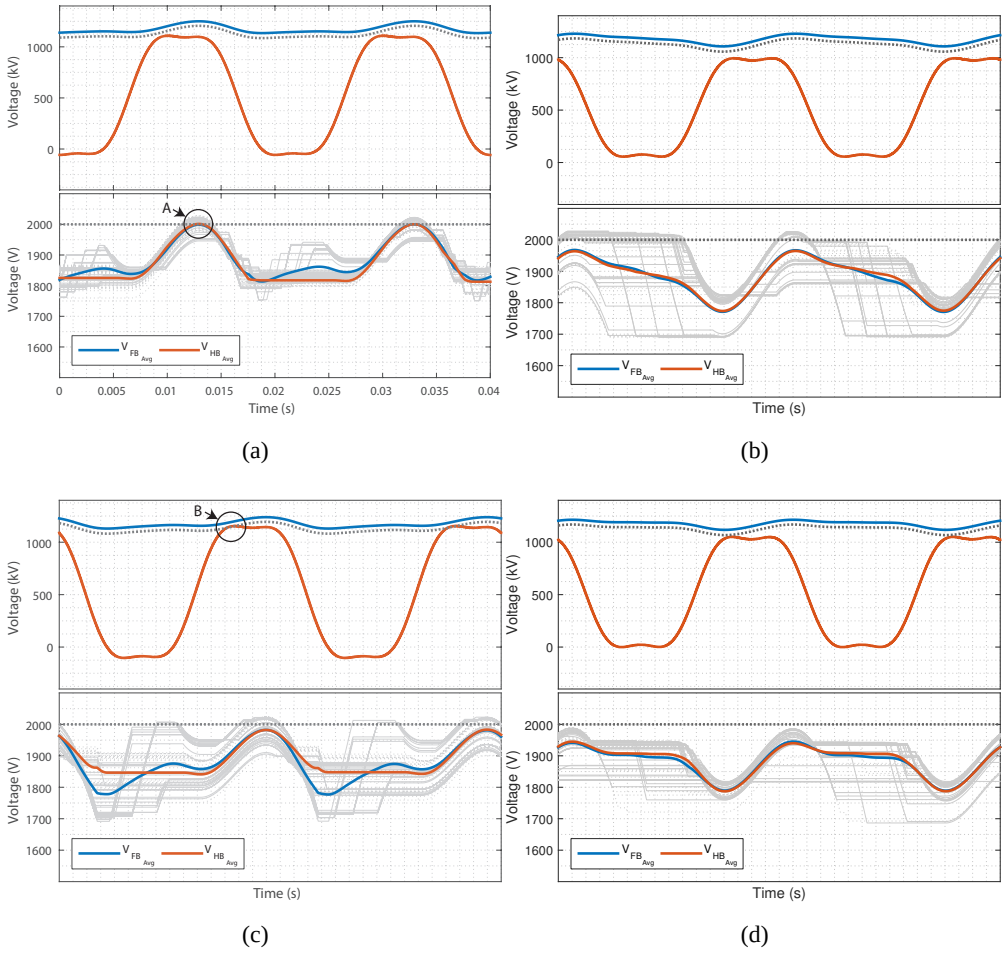


Fig. 12. Hybrid MMC simulation verification. Top: stack voltage, moving average of stack voltage, sum SM capacitor voltage, design safety limit (dashed line. Middle: SM Voltages (dashed) and mean SM voltage (solid). Bottom: arm current a) P: 1 Q: 0.3 AC Voltage: 95% b) P: 1 Q: -0.5 AC Voltage: 95% c) P: 1 Q: 0.3 AC Voltage: 105% d) P: 1 Q: -0.5 AC Voltage: 105%

VII. Experimental Results

To verify the design methodology presented, as well as verifying the operation of the converter at a modulation index of 1.2, a Hybrid MMC was dimensioned and tested using a lab-scale multilevel converter. The experimental results are carried out at lab-scale, with a multilevel converter that contains 10 SM per arm that can be configured as either full-bridges or half-bridges. the experimental work was carried out to validate the analytical work against un-modelled factors as well as practical control limitations. A picture of the lab-scale converter is given in Fig. 13. Further details of the lab-scale converter, as well as the system used for emulating DC fault tests are provided in [33]. The converters controller is similar to the one used for the simulation results within the previous section, and is implemented on an Opal-RT OP5600 real-time simulator.

(a) (b)

Fig. 13. Multilevel Converter Demonstrator a) Front view of cabinet b:) Array of sub-modules

Because the lab-scale converter has only 10 SMs per arm, each of which can be configured as either a FB-SMs or HB-SMs, it was not possible to do the experiment using a design with $K_{\text{FB}} = 0.55$ and a modulation index of 1.2. A sweep of design inputs, using the methodology presented in Section IV, with variation in the SM capacitor, DC voltage and peak rated SM voltage was undertaken. By tightening the AC voltage variation on the P/Q capability to 0% a solution was found with a required number of SMs close to 10, and a required number of FBs close to 5. The inputs and outputs from the design is given in Table. III.

The converter was run using the parameters from the table above, with the values of N and N_{FB} rounded to 10 and 5 respectively. Two outer points of the P/Q specification were tested during steady-state operation. Results from each run are given in Fig. 14. The SM voltages were logged using the OPAL-RT controllers data acquisition system. The arm current and stack voltage of the upper arm of phase A were logged with an oscilloscope using a current probe and differential voltage probe. A moving average of the measured stack voltage was generated and overlaid on the measured stack voltage. The converter can be seen to be operating close to its design limits in both set-points tested, with the mean SM voltage reaching slightly above the 170 V design target during rectifying operation with positive reactive power. At rectifying operation with inductive reactive power the stack voltage can be seen to intersect the safety margin applied to the total available voltage within the stack with good approximation. This intersection occurs

TABLE III

DESIGN INPUTS AND SOLUTION

Design Inputs		Design Solution	
Rated Power	15 kW	N	9.932
m	1.2	N_{FB}	5.095
Q at Rated Power (pu)	0.3/-0.5	Nominal SM Voltage	162 V
Q under DCF (pu)	0.3/-0.5	Nominal Energy Storage	40.2 kJ/MVA
SM Capacitor	770 uF	Rated Voltage of Arm	1.609 kV
DC Voltage	725 V	Rated Voltage of FBs	0.825 kV
AC Voltage (RMS L-L)	1066 V		
AC Voltage Variation	+-0%		
Peak SM Voltage	170 V		
E^{+}_{safety}	3 kJ/MVA		
E^{-}_{safety}	3 kJ/MVA		
Transformer Leakage Reactance	6 mH		
Arm Inductor	23.5 mH		

at an inductive power factor, rather than a capacitive one as discussed in the previous section. This occurs as the dimensioning of the experimental converter was done without any variation in the AC voltage magnitude.

The converter was also tested with a pole to pole DC fault scenario, generated using a 10 Ω fault impedance and chopper IGBT. The results from this test are shown in Fig. 15. Prior to the fault the converter was set to generate -1 pu active power and 0.3 pu reactive power. When the DC fault is detected the converters controller is set to drop its active and reactive power set-point, and then ramp back up to its reactive power set-point after one cycle. The converter can be seen to retain current control throughout the fault, quickly driving the arm current to zero once the fault is detected, and then ramping up to its reactive power set-point. The filtered moving average of the stack voltage can be seen to be move slightly past the safety margin, but still below the overall available voltage within the arm during STATCOM operation under DC fault conditions. This is because the fault results in some disturbance to the energy levels within the converter. Such disturbances can be expected and are one of the reasons why the energy safety margin was included within the design specification. In addition, the lab-scale converter has 5 FB sub-modules, whereas the design called for 5.095 and so the rated negative voltage

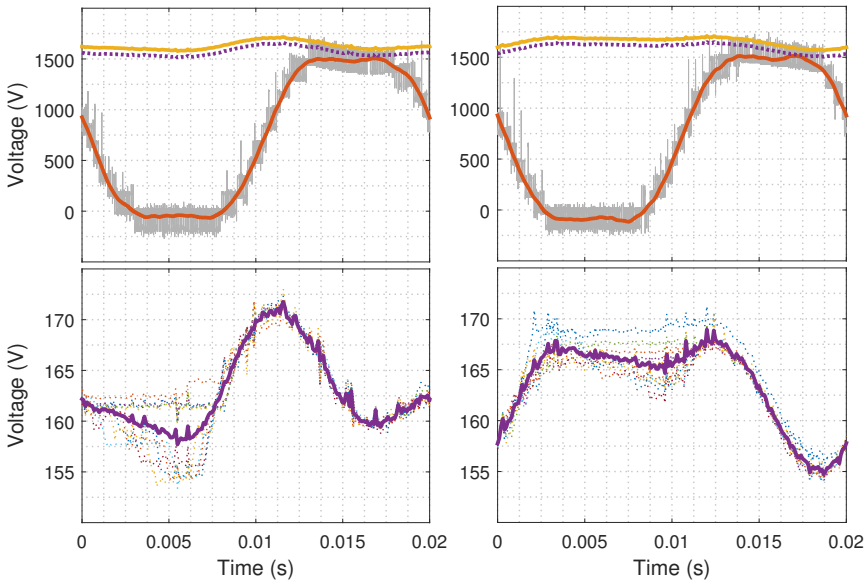


Fig. 14. Hybrid MMC simulation verification. Top: stack voltage (grey), moving average of stack voltage (orange), sum SM capacitor voltage (yellow), and design safety limit (dashed line). Middle: SM Voltages (dashed) and mean SM voltage (solid). Bottom: arm current a) P: -1 Q: 0.3 - converter limited by Peak Sub-Module Voltage Limit b) P: -1 Q: -0.5 - converter limited by Stack Voltage Limit

capability of the arm is therefore slightly below the required level given by the design method.

~~During the DC fault the converter periodically attempts to recharge the DC bus by injecting a small amount of active power into the DC system. When the fault is cleared the controller detects a rise in the DC voltage when it injects active power. The controller then actively recharges the DC bus voltage and ramps back to its pre-fault set-point. The SM voltages are well controlled during the fault, with a slight disturbance to their levels at point of fault inception and during the re-charge stage. The converter retains current control throughout the fault.~~

~~A close up of the DC fault results is given in Fig.~~ 15 ~~focusing on the internal converter currents and voltages in the upper arm of phase A the 5 cycles following the fault inception. The filtered moving average of the arm voltage can be seen to be moving slightly past the safety margin, but still below the overall available voltage within the arm. This is because the fault results in some disturbance to the energy levels within the converter. Such disturbances can be expected and are one of the reasons why the energy safety margin was included within the design specification. In addition, the lab-scale converter has 5 FB sub-modules, whereas the design called for 5.095 and so the rated negative voltage capability of the arm is therefore slightly below the required~~

~~level given by the design method.~~

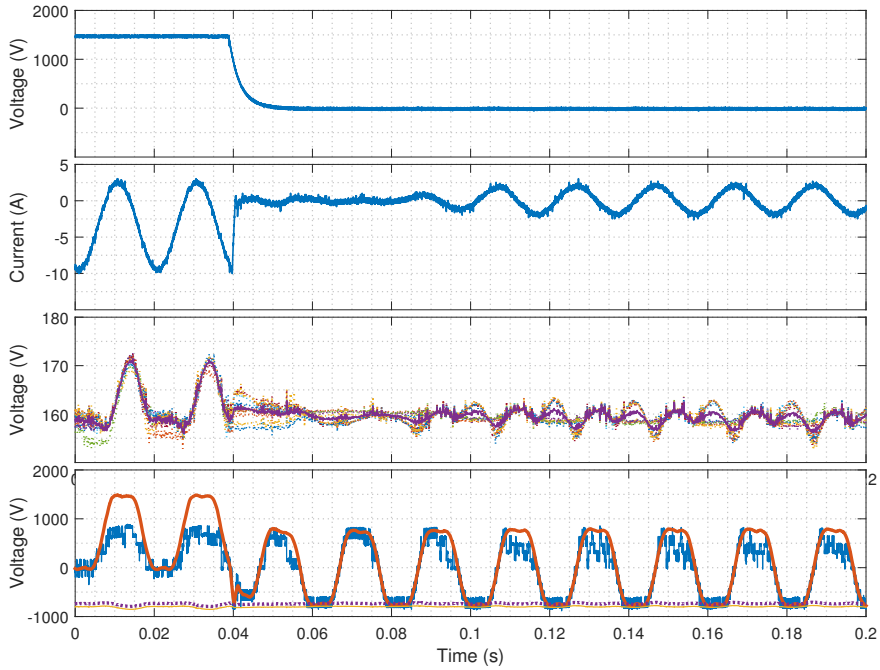


Fig. 15. Experimental results of Hybrid MMC being subjected to a pole-to-pole DC fault, followed by a ramp to 0.3 pu reactive power while the DC bus is shorted. Results are shown for the upper arm of Phase A. Top: DC pole. Top Middle: Arm current. Top Bottom: SM voltages (dashed) and mean SM voltage (solid) Bottom: moving average filtered overall stack voltage, stack voltage generated by FBs, available negative voltage and safety margin

VIII. Conclusion

The ability of the Hybrid MMC to offer tolerance to DC faults without the efficiency penalty of the full-bridge MMC is known. With the Hybrid MMC there is a choice over the ratio of AC to DC voltage at which the converter should operate. This choice impacts not only the required voltage rating of each stack, but also the required ratio of full-bridge to half-bridge sub-modules in order to achieve DC fault tolerance. At the same time the choice of ratio of AC to DC voltage impacts the converters internal voltage, current and energy deviation waveforms, which have an impact on the required amount of de-rating applied to each sub-module, as well as the required up-rating of the overall voltage capability of each stack of sub-modules. This paper has described and verified a design process that, for a given P/Q specification and given modulation index, gives the required number of sub-modules, the required de-rating applied to each sub-module and the required ratio of full-bridge sub-modules to the overall required

number of sub-modules. This method is then used to perform a sweep of Hybrid MMC designs, with variation in the modulation index. It is found that increasing the modulation index past 1 gives an initial improvement in efficiency but diminishing returns occur such that a nominal modulation index of 1.2 is the preferred choice. In comparison to a Hybrid MMC design that does not over-modulate, the reduction in semiconductor power losses is approximately 10% and the required increase in the number of sub-modules is 6% (corresponding to a 10% increase in the number of IGBTs). Designing the Hybrid MMC to be capable of operating as a STATCOM under DC fault conditions carries a further design penalty.

The design method was verified with a time-step simulation of a 1.5 GW, $\pm$525 kV converter to demonstrate that key design parameters are within limits at the extreme of the specified operating range. The design was also verified in terms of limitations of a practical real-time controller with a 15 kW, $\pm$750 V laboratory-scale converter. ~~and, in particular, fault ride-through with a DC-side fault demonstrated.~~

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