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High-Efficiency MOSFET-based MMC Design for LVDC Distribution Systems

Y. Zhong
Siemens Wind Power Ltd,
Keele, UK
yanni.zhong@siemens.com

N. Roscoe, D. Holliday
Department of Electronic and
Electrical Engineering
University of Strathclyde,
Glasgow, UK

T.C. Lim,
Supply Design Ltd, Rosyth,
UK

S.J. Finney
Department of Electronic and
Electrical Engineering
University of Edinburgh,
Edinburgh, UK

Abstract -- **LVDC distribution networks have the potential to release larger capacity without having to upgrade the existing cables. One of the main challenges of LVDC networks is the extra customer-end DC-AC conversion stage. This paper proposes and evaluates a 5-level Si MOSFET-based MMC as a promising alternative to the conventional 2-level IGBT-based converter. This is due to the comparatively higher efficiency, power quality and reliability, and reduced EM emissions. A comprehensive analysis of a Si MOSFET 5-level MMC converter design is performed to investigate the suitability of the topology for LVDC applications. Detailed theoretical analysis of the 5-level MMC is presented, with simulated and experimental results to demonstrate circuit performance. To suppress the AC circulating current, especially the dominant 2nd harmonics, this paper presents a double line-frequency PI with orthogonal imaginary axis control method. Comparison of simulation and experimental results with those for double line-frequency PR control shows that the proposed PI controller has better performance. In addition, it is simpler to implement and more immune to sampling/discretisation errors.**

Index Terms--**Converter Design, Current Suppression Control, DC-AC, LVDC, MMC, PI with Orthogonal Imaginary Axis, PR.**

I. Nomenclature

LVDC – Low-voltage direct current
MMC – Modular multilevel converter
PI – Proportional integral   PR – Proportional resonant
SM – Submodule   SR – Synchronous rectification

II. Introduction

The concept of LVDC distribution has been proposed and has, in recent years, drawn increasing attention. This is because existing low-voltage AC power distribution networks face challenges from increased load demands in combination with rapid deployment of new technologies [1, 2]. In particular, the number of high-capacity power electronic interfaces, such as electric vehicle chargers and embedded PV generation, have increased significantly [3-5]. LVDC networks are able to provide increased capacity without the need to upgrade existing cables [6, 7].

Due to the existence of widespread AC loads, the additional power losses and EMI issues caused by the conventional 2-level IGBT-based converter would become one of the main challenges of LVDC networks. To improve the efficiency, power quality and reliability, as well as to reduce the EM emissions, this paper proposes a modified MMC topology for a customer-end DC-AC conversion stage, and a thorough converter design.

MMC is a promising topology but it has not been applied previously in low-voltage (LV) applications. Comparisons between MMC and 2-level converters for LV applications are distinctly different to those for high-voltage (HV) applications for two reasons: (1) the wide range of available device technologies at LV, and (2) the design requirements imposed by the applications are very different. Hence, theoretical analysis and experimental validation are presented in this paper to investigate the advantages and disadvantages of applying MMC to LVDC DC/AC conversion. At LV, MMC cell voltage is low enough for Si MOSFET and GaN HEMT to be used instead of IGBTs, potentially reducing the conduction loss dramatically [7, 8]. In addition, for LV MMC, the use of MOSFETs means that R_{dson} can be significantly reduced through parallel connection, and synchronous rectification, bringing very low conduction loss.

Wide-bandgap devices such as SiC and GaN are expected to replace Si devices and improve efficiency in 2-level converters as well as MMC. By comparing different converter topologies, including IGBT 2-level, SiC MOSFET 2-level, GaN HEMT MMC and Si MOSFET MMC, it has been concluded that an Si MOSFET 5-level MMC with 4 parallel-connected MOSFETs is a promising alternative topology to replace the conventional 2-level IGBT-based converter [8, 9].Total converter efficiency is compared in Fig. 1, and has previously been discussed in detail [9]. Modelling losses for parallel connection is less accurate due to variations in threshold voltage. The first device to turn on discharges C_{ds} and C_{gd} in all parallel devices, incurring more loss than if all devices were to turn on simultaneously. During C_{gd} discharge in an off device, the discharging current tends to slow C_{gs} charging, thus further spreading out turn-on times. Hence, measured loss for 4 parallel devices is greater than calculated loss. Loss in a single MMC module with 4 parallel IRFP4668 devices was measured using heatsink temperature rise, and this measured loss has been combined with calculated passive losses and included in Fig. 1. Regarding passive component loss, both MMC and SiC 2-level converters have

uncertainties. Although MMC submodule electrolytic capacitor loss would be a dominating factor as the number of parallel-connected devices increases [8], if volume is not of great concern, film capacitors can almost eliminate capacitive loss. The single-phase, 2-level converter requires a large DC-side capacitor, which is subject to large 2nd harmonic currents leading to high loss. Calculations for 2-level converters show that the AC-side inductance incurs loss of over 250W due to high RMS current on the output of the single-phase converter. In addition, SiC brings issues with potential EMI [10, 11].

IGBT total converter efficiency is calculated by summing semiconductor losses [12] with 2-level converter passive filter losses [9] giving 93.6%. For the 5-level Si MOSFET MMC, efficiency is improved and is predicted to be 97.2% [12], offering improved reliability through cooler operation. Using measured loss, efficiency is 96.7%. It is also possible for MMC to provide redundancy for failure management, thus the reliability can be further improved [13]. In addition, MMC with appropriate arm current control has no need for an input filter allowing the use of smaller AC filters, low switching losses, better output waveform quality and the ability to prevent capacitor discharging current [14-16].
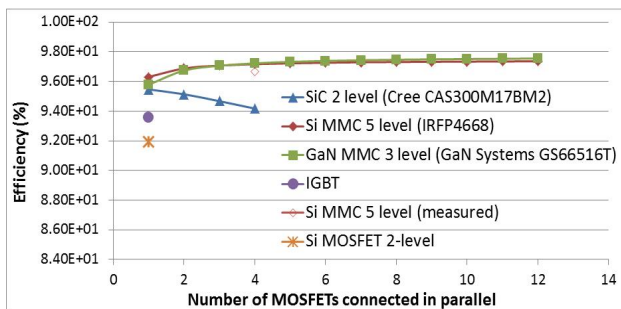

Fig. 1. Efficiency comparison for two phase-leg Si MOSFET 5-level MMC, GaN 3-level MMC, SiC 2-level, Si MOSFET 2-level and IGBT 2-level converters at 10 kW, 10 kHz, 600 V_{dc}, M=0.57 and unity power factor.
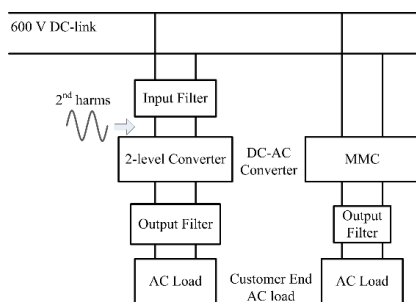

Fig. 2. DC network with single-phase customer-end AC loads.

Fig. 2 shows an example DC network with single-phase AC loads supplied through conventional 2-level and MMC converters. Unlike the 3-phase converter where the 2nd harmonic current will be cancelled in the DC side, the conventional single-phase inverter will suffer from enhanced 2nd harmonics. This harmonic current will circulate in the filter capacitor resulting in losses, and similar losses will also be exhibited in the LV MMC. However, the inherent energy storage of the MMC allows control and elimination of this harmonic circulating current without the need of a bulky input filter.

This investigation examines the applicability of single-phase MMC for LV applications, where a key consideration is elimination of the 2nd harmonic from the DC input current. Much research has studied the suppression of AC circulating current in HV MMC. Proportional resonant (PR) control is often adopted because it has high gain at selected frequencies and it can be applied to both single and 3-phase converters [17, 18]. To eliminate multiple harmonics, a multi-frequency PR controller (parallel-connected PR controllers at 2nd, 4th, 6th, and 8th order harmonics) are recommended [18]. The PR controller is 2nd order, meaning that DSP implementation may be difficult when many parallel-connected PR controllers are required. PI control in the line-frequency reference frame [19] has a limited gain, especially at the dominating 2nd harmonic. A repetitive-plus-PI control strategy, where the repetitive compensator is added to track the error and eliminate multiple harmonics, was therefore presented [20]. Another PI controller for 3-phase MMC, based on the double line-frequency, negative-sequence rotational coordinate frame, has also been presented [21].

In selecting the circulating current control method for an LV MMC application, simplicity, feasibility and effectiveness are the main concerns. Additionally, because the 2nd harmonics dominate the circulating current, two methods based on double line-frequency, namely PR control and PI with orthogonal imaginary axis control, were selected for comparison using simulations and experiments. Other effective control methods, such as repetitive-plus-PI control and multi-frequency PR control, are not considered for this LV application because of their increased complexity, and controllers such as the PI controller based on the negative-sequence rotational coordinate frame are not selected because they are not suitable for single-phase operation [17–21]. Among the selected controllers, the PR controller is a commonly used method based on previously reported research [17, 18]. The single-phase double line-frequency PI controller proposed in this paper is a novel modified control method based on [21]. The novelty is that while [21] uses dq transformation for 3-phase, this paper introduces an orthogonal imaginary axis to generate a rotating frame for single-phase MMC. The differences between the proposed PI control method and [19, 20] are that the reference frame rotating at double the line frequency enables the novel PI controller proposed here to achieve zero steady-state error at 100 Hz, whilst [19] constantly has this steady-state error and [20] adopted a repetitive compensator to track this error.

To investigate the suitability of single-phase MMC for LVDC distribution networks applications, detailed parameter sizing is presented in this paper. The contribution regarding capacitor sizing is the derivation of an equation for the zero-crossing points and energy deviation for single phase MMC. In contrast to HV MMC applications, an output filter is

required for LV MMC. Another contribution is therefore the output filter sizing equations for single-phase LV MMC.

Whist efficiency is a significant benefit offered by MMC in LVDC applications, this is not explored in this paper since it has been examined fully in previous publications [7, 8]. Dynamic current sharing between the four parallel-connected devices has little impact because of the relatively low switching frequency of each device [8]. Therefore, parallel-connection will not be further considered in this paper.

This paper is organised as follows. Section III presents the parameter sizing of MMC and the output filter design. To suppress the 2nd order harmonics in the circulating current, both PR, and PI with orthogonal imaginary axis controllers are designed in Section IV. Output voltage regulation is also introduced to maintain waveform quality of output voltage. Experimental results for 5-level MMC are presented in Section V.

III. MOSFET MMC DESIGN

Since the application of MMC in LV is different in HV and the circulating current property is different for single-phase than for 3-phase, a comprehensive analysis is carried out in this section.

A 2-phase-leg MMC topology and the average model of a single-phase MMC are presented in Fig. 3 and Fig. 4 respectively [22, 23]. Each SM contains two MOSFETs and one capacitor which acts as an energy storage component that may be inserted in the series path or bypassed according to the switching state of the MOSFETs [24]. Additionally, to simplify the sizing procedure, the following assumptions are made:

1) The current suppression control eliminates all harmonics and the remaining circulating current (i_{diff}) only has a DC component I_{dc}.
2) All capacitors and all switches are identical.
3) SM capacitor voltages are instantaneously balanced.

In Fig. 4, output voltage V_{ao} and current i_{ao} are assumed sinusoidal with lagging phase angle φ, and are given by (1) and (2), where M is the modulation index.

$$V_{ao} = M \cdot \sin \omega t \cdot \frac{V_{dc}}{2} \tag{1}$$
$$i_{ao} = I_{ao} \sin(\omega t - \varphi) \tag{2}$$

According to [21] and assumption 1, the upper and lower arm currents i_{au} and i_{al} can be expressed as (3) and (4), where I_{dc} is the DC component of i_{diff} in one phase leg.

$$i_{au} = i_{diff} + \frac{i_{ao}}{2} = I_{dc} + \frac{i_{ao}}{2} \tag{3}$$
$$i_{al} = i_{diff} - \frac{i_{ao}}{2} = I_{dc} - \frac{i_{ao}}{2} \tag{4}$$

The use of multilevel modulation allows the generation of low-distortion output voltage without the need for a bulky output harmonic filter or high switching frequency [25]. In this section, the output waveform quality will be analysed and the output filter designed.
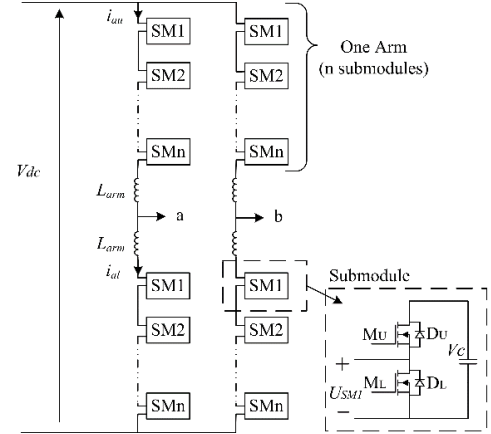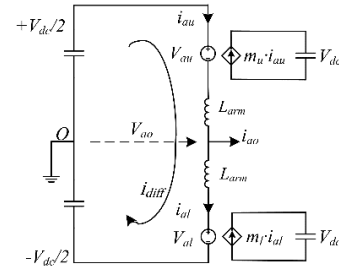

Fig. 3. 2-phase-leg n-level MMC.

Fig. 4. Average model of a single-phase MMC.

A. Submodule Capacitor Sizing

The MMC relies on charged SM capacitors to build up the output AC voltage. The capacitances should be minimised, whilst maintaining voltage fluctuation within ±10% of the nominal value [26]. In this section, the capacitor value is obtained based on its maximum energy deviation. The symbols used in the analysis are defined as follows:

- V_C is the average submodule capacitor voltage.
- V_{C_nom} is the nominal SM capacitor voltage.
- ΔV_{max} is the maximum voltage difference in p.u.

Level-shifted SPWM modulation, specifically phase opposition disposition (POD), is exploited to generate a sinusoidal output waveform. The cumulative upper and lower arm voltages, V_{au} and V_{al}, can be expressed as (5) and (6) respectively, in which m_u and m_l describe the switching actions in the upper and lower arms respectively.

$$V_{au} = m_u \cdot V_{dc} = \left(\frac{1}{2} - \frac{1}{2}M \cdot \sin \omega t\right) \cdot V_{dc} \tag{5}$$
$$V_{al} = m_l \cdot V_{dc} = \left(\frac{1}{2} + \frac{1}{2}M \cdot \sin \omega t\right) \cdot V_{dc} \tag{6}$$

The average energy stored in one arm, E_{arm}, and peak-to-peak energy deviation, ΔE_{arm}, are given by (7) and (8).

$$E_{arm} = \frac{n}{2} \cdot C_{sub} \cdot V_C{}^2 \tag{7}$$
$$\Delta E_{arm} = \frac{n}{2} \cdot C_{sub} \cdot \left[V_{C_{nom}}(1 + \Delta V_{max})\right]^2 - \frac{n}{2} \cdot C_{sub} \cdot \left[V_{C\_nom}(1 - \Delta V_{max})\right]^2 \tag{8}$$

The minimal SM capacitance, C_{sub}, can be derived as (9).

$$C_{sub} = \frac{\Delta E_{arm}}{2n \cdot V_{C\_nom}^2 \cdot \Delta V_{max}} = \frac{n \cdot \Delta E_{arm}}{2V_{dc}^2 \cdot \Delta V_{max}} \quad (9)$$

Apparent power, $|S|$, is given by (10), and by combining it with (3) and (5), the instantaneous power flow into the upper arm can be derived by (11), in which P is real power to the MMC and $\cos\varphi$ is the power factor.

$$|\bar{S}| = \frac{P}{\cos\varphi} = \frac{V_{dc} \cdot 2I_{dc}}{\cos\varphi} \quad (10)$$

$$\begin{aligned} p_{arm-up}(t) &= V_{a1}(t) \cdot i_{au}(t) \\ &= |\bar{S}| \frac{1}{4M}(1 - M\sin\omega t) \cdot [M\cos\varphi + 2\sin(\omega t - \varphi)] \end{aligned} \quad (11)$$

Energy stored in one arm can be obtained by integrating power with respect to time. By integrating $P_{arm\_up}(t)$ between $t1$ and $t2$, where $t1$ and $t2$ are the zero crossing points of P_{arm_up} (Fig. 5), the peak-to-peak energy variation can be calculated (Fig. 6). The symbolic solution for ΔE_{arm} is given by (14). The symbolic equations are the contributions of this paper.

$$t1 = \frac{1}{\omega}[\varphi - \sin^{-1}(0.5M\cos\varphi)] \quad (12)$$

$$t2 = \frac{1}{\omega}[\pi + \varphi + \sin^{-1}(0.5M\cos\varphi)] \quad (13)$$

$$\begin{aligned} \Delta E_{arm} &= \int_{t1}^{t2} P_{arm-up}(t)\,dt \\ &= \frac{|\bar{S}|}{\omega} \cdot \frac{1}{M}\left(1 - \frac{1}{4}M^2\cos^2\varphi\right)^{1.5} \end{aligned} \quad (14)$$
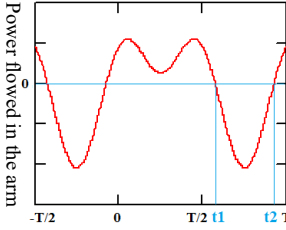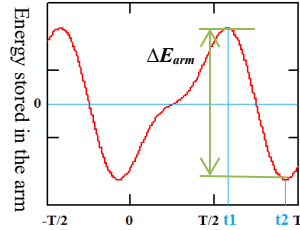

Fig. 5. Power flow through the arm   Fig. 6. Energy stored in the arm.

The maximum ΔE_{arm} occurs when $\cos\varphi=0$, i.e. zero real power, and is given by (15). Additionally, a lower value of M would lead to a higher energy deviation.

$$\Delta E_{arm-max} = \frac{|\bar{S}|}{\omega} \cdot \frac{1}{M} \quad (15)$$

Therefore, the minimum cell capacitance required for the single-phase MMC is given by (16).

$$C_{sub} = \frac{n \cdot |\bar{S}|}{2\omega \cdot M \cdot V_{dc}^2 \cdot \Delta V_{max}} \quad (16)$$

According to (16), the required capacitance for a 5-level 2-phase-leg 10 kW 600 V_{dc} / 240 V_{ac} MMC is 3.18 mF. The Matlab simulation of Fig. 7 shows that SM capacitor voltages in one phase leg are well balanced and that the voltage ripple is $\pm7.5\%$, which is within the $\pm10\%$ distortion limit.

B. Arm Inductor Sizing

In MMC, the function of the arm inductors (L_{arm}) is to limit the circulating current which results from the voltage difference u_{diff} between the DC side voltage and the voltage in one phase-leg. In some applications, such as HVDC system,

arm inductors are also a key to limiting the DC fault current [27]. In this study, the main consideration is the circulating current constraint.
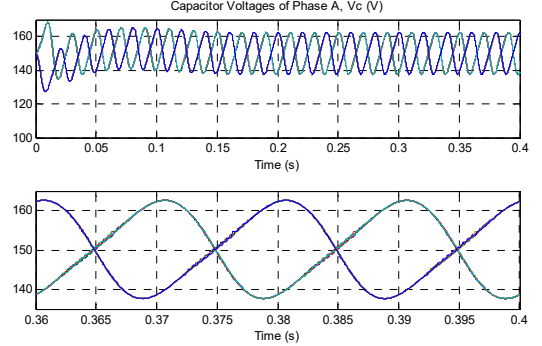

Fig. 7. Capacitor voltages for a 4 SM per arm 5-level 2-phase-leg MMC with 3.3 mF SM capacitance.

Voltage difference u_{diff} can be given by (17) [28]. Its maximum value can subsequently be derived as (18).

$$\begin{aligned} u_{diff} &= \frac{V_{dc} - (v_{au} + v_{al})}{2} = \frac{n}{8C_{sub}}\left\{-\frac{3}{4\omega}M \cdot I_{ao} \cdot \right. \\ &\left. \sin(2\omega t - \varphi) + \frac{1}{\omega}M^2 I_{dc} \cdot \sin(2\omega t)\right\} \\ &= \frac{n \cdot I_{dc}}{8\omega C_{sub}} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2\varphi} \cdot \sin(2\omega t - \theta) \end{aligned} \quad (17)$$

where $\theta = \tan^{-1}\left(\frac{3\tan\varphi}{M^2 - 3}\right)$.

$$u_{diff\_max} = \frac{n \cdot I_{dc}}{8\omega C_{sub}} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2\varphi} \quad (18)$$

The peak-to-peak value of the circulating current at the switching frequency can be given by (19).

$$I_{pp} = \frac{u_{diff}}{L_{arm}} \cdot \Delta T \quad (19)$$

Since the largest ΔT would be T_S, the largest I_{pp} can be expressed as (20).

$$\begin{aligned} I_{pp\_max} &= \frac{u_{diff\_max}}{L_{arm}} \cdot T_S \\ &= \frac{n \cdot I_{dc} \cdot T_S}{8\omega L_{arm} C_{sub}} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2\varphi} \end{aligned} \quad (20)$$

I_{pp_max} is limited into 5% of DC side current I_d in this study.

$$I_{pp\_max} = 0.05I_d = 0.1I_{dc} \quad (21)$$

Given this, the required L_{arm} should be at least

$$L_{arm} = \frac{5n}{4\omega C_{sub}f_s} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2\varphi} \quad (22)$$

By applying (22), $L_{arm} = 1.5$ mH is required for the 10 kW 2-phase-leg 5-level MMC with 600 V_{dc} and 240 V_{ac}. The Matlab simulation results for arm currents and DC input current are presented in Fig. 8, which shows that the DC current ripple is 4.7% and meets the current limitation.
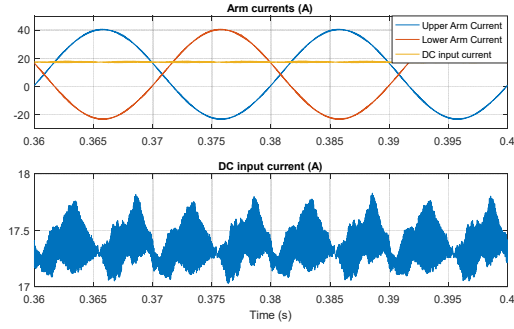
Fig. 8. Simulation results of arm currents and circulating current in a 2-phase-leg 5-level MMC (V_{dc}=600 V, V_{out}=240 V, 10 kW, L_{arm}=1.5 mH).

C. Output Filter Design

In established HV MMC applications, large numbers of SMs are required to support the DC voltage. This large SM number permits use of low switching frequency 'staircase' modulation with minimal distortion and no filter requirement. However, the LV MMC investigated in this paper uses relatively few SMs, necessitating the use of PWM rather than the common low-frequency modulation. Therefore, the filter design is specialised for MMC in LVDC.

As shown in Table 1, for a 10 kW 600 V_{dc} / 240 V_{ac} 10 kHz MMC with level-shifted SPWM modulation, a small output filter is required when fewer than 13 levels are used, in order to meet the 5% distortion limit.

Table 1 THD analysis of output voltage and current for MMC with different numbers of levels, (10 kW, 10 kHz, 600 V_{dc} / 240 V_{ac}, 0.95 power factor, level-shifted SPWM modulation)

MMC Levels	Output Current THD	Output Voltage THD
5-level	0.48%	16.05%
7-level	0.65%	10.39%
9-level	0.59%	7.72%
11-level	0.59%	5.78%
13-level	0.45%	4.47%

A large filter inductance L would increase converter volume and cost significantly, whilst a large capacitance C would draw large current from the converter, increasing switching device stresses. Selecting L and C therefore requires a design trade-off.

The gain of a passive LC filter at cut-off frequency ω_n is infinite, whilst a parallel damped filter has a significantly damped gain at ω_n. This allows a higher bandwidth and better noise suppression for the feedback control. Fig. 9 presents the equivalent circuit of an MMC with a parallel damped filter. The upper and lower arm inductances L_{arm} in one phase can be regarded as connected in parallel, and to serve as part of the output filter. The series-connected resistor R_f and capacitor C_{f2} are connected in parallel with capacitor C_{f1}. The purpose of resistor R_f is to reduce the output peak impedance of the filter at the cut-off frequency. Capacitor C_{f2} blocks the

low frequency component of the input voltage and reduces power dissipation in the filter resistance [29].
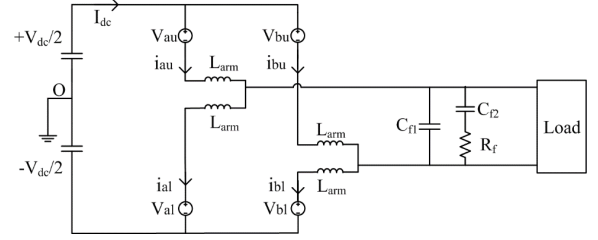

Fig. 9. Equivalent circuit of 2-phase-leg MMC with parallel damped filter.

The transfer function and cut-off frequency for the parallel damped filter are given by (23) and (24) respectively.

$$G_{filter} = \frac{C_2 Rs + 1}{C_1 C_2 LR s^2 + (C_1 + C_2) L s^2 + C_2 Rs + 1} \tag{23}$$

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{24}$$

For low-voltage MMC, only a capacitor is needed to complete the output filter. For example, the output voltage THD for a 10 kHz, 5-level MMC (with parameters listed in Table 2) is 16.05% without an output filter. The FFT analysis shown in Fig. 10(a) indicates the high distortion appears as sidebands centered around multiples of the switching frequency. Therefore, the cutoff frequency of the filter needs to be lower than the switching frequency. The impedance of capacitor C_{f2} should be lower than R_f at the resonant frequency, while its capacitance should be higher than C_{f1} so that the cutoff frequency of the main filter will not be affected [29].

The FFT analysis shown in Fig. 10(a) suggests a 20 kHz harmonic dominates. By setting the cut-off frequency equal to 10% of 20 kHz and applying (24), a parallel damped filter with C_{f1}=200 nF can be selected. The optimum damping resistance R_f and capacitance value C_{f2} are given by (25) and (26) [29], which results in C_{f2}=800 nF and R_f=86.6 Ω.

$$R_f = \sqrt{\frac{L_{arm}}{c_{f1}}} \tag{25}$$

$$C_{f2} = 4C_{f1} \tag{26}$$

The output spectrum shown in Fig. 10(b) indicates that the filter can meet the 5% distortion target.

Table 2 Circuit parameters for 2-phase-leg 5-level MMC

Input Voltage	600 V	Output Voltage	240 V
Modulation Index	0.57	Output Current	43.86 A_{rms}
Arm Inductance	1.5 mH	SM Capacitance	3.3 mF
Power Factor	0.95	I_{dc}	16.67 A
Real Power	10 kW	Load R_L	5.19 Ω
Switching Frequency	10 kHz	Load L_L	5.46 mH

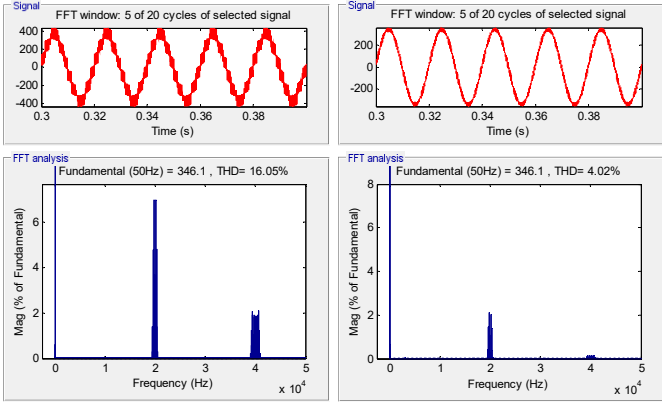(a) without output filter (b) with parallel damped filter

Fig. 10.   FFT analysis of 5-level 2-phase-leg MMC output line voltage.

IV. MOSFET MMC CONTROL STRATEGIES

The difference between the DC-link voltage and the sum of the arm voltages leads to a circulating current, which increases converter power loss. For single-phase converters, the circulating current is a serious issue as the 2nd harmonic from each arm sums at the DC side. For LVDC networks with significant single-phase loading, this 2nd harmonic may result in larger cable loss or even network malfunction. Conventional converters address this issue by the use of passive input filters with associated losses and the risk of system resonance. The internal capacitance of the LV MMC structure permits active elimination of these harmonics resulting in a near DC input current. In this section, both the basic conventional PR control, and double-line frequency PI control with orthogonal imaginary axis, are designed and compared. Voltage regulation is also introduced to maintain output voltage during changing load conditions.

A. Current Suppression Control

1) Generation of 2nd Harmonic Current

Based on the average model shown in Fig. 4, the capacitor current in each SM can be given by the product of switching action and arm currents i_{au} and i_{al}, as shown in (27) and (28).

$$i_{cu}(t) = i_{au} \cdot m_u$$
$$= (I_{dc} + \frac{I_{ao}}{2}\sin(\omega t - \varphi)) \cdot \left(\frac{1}{2} - \frac{1}{2}M \cdot \sin\omega t\right) \tag{27}$$

$$i_{cl}(t) = i_{al} \cdot m_l$$
$$= \left(I_{dc} - \frac{I_{ao}}{2}\sin(\omega t - \varphi)\right) \cdot \left(\frac{1}{2} + \frac{1}{2}M \cdot \sin\omega t\right) \tag{28}$$

Equation (29) is derived from (27), which shows that i_{cu} can be expanded to DC, fundamental and 2nd harmonics of the grid frequency. In steady state, the DC component of capacitor current should be zero. Therefore, the average upper arm capacitor current can be expressed as the sum of fundamental-frequency and 2nd harmonic components as shown in (30).

$$i_{cu}(t) = \frac{1}{2}\left(I_{dc} - \frac{M}{4}I_{ao}\cos\varphi\right) - \left[\frac{M}{2}I_{dc} \cdot \sin\omega t - \frac{1}{4}I_{ao}\sin(\omega t - \varphi)\right] + \frac{M}{8}I_{ao}\cos(2\omega t + \varphi) \tag{29}$$

$$i_{cu}(t) = -i_c^{(1)}(t) + i_c^{(2)}(t) \tag{30}$$

where $i_c^{(1)}(t) = \frac{M}{2}I_{dc} \cdot sin\omega t - \frac{1}{4}I_{ao}\sin(\omega t + \varphi)$,

and $i_c^{(2)}(t) = \frac{M}{8}I_{ao}\cos(2\omega t + \varphi)$.

Similarly, lower arm capacitor current is given by (31).

$$i_{cl} = i_c^{(1)}(t) + i_c^{(2)}(t) \tag{31}$$

The nth harmonic of capacitor ripple voltage is the product of the corresponding capacitor reactance at $n\omega$ and the nth harmonic of capacitor current. As shown in (32), $\Delta u_C^{(n)}(t)$ denotes the nth harmonic of capacitor voltage and can be represented by $V_n\sin n\omega t$.

$$\Delta u_C^{(n)}(t) = \frac{i_c^{(n)}(t)}{jn\omega C} \to V_n\sin n\omega t \tag{32}$$

Hence, the total capacitor ripple voltage at fundamental and 2nd harmonic frequencies for upper and lower cells can be represented as ΔV_{cu} and ΔV_{cl} respectively.

$$\Delta V_{cu} = -V_1\sin\omega t + V_2\sin 2\omega t \tag{33}$$
$$\Delta V_{cl} = V_1\sin\omega t + V_2\sin 2\omega t \tag{34}$$

Therefore, the ripple voltage across the SM terminals is:

$$\Delta V_{au} = m_u \cdot \Delta V_{cu} =$$
$$(\frac{1}{2} - \frac{M}{2} \cdot \sin\omega t) \cdot (-V_1\sin\omega t + V_2\sin 2\omega t) \tag{35}$$

$$\Delta V_{al} = m_l \cdot \Delta V_{cl} =$$
$$(\frac{1}{2} + \frac{M}{2} \cdot \sin\omega t) \cdot (V_1\sin\omega t + V_2\sin 2\omega t) \tag{36}$$

Ripple voltage across the phase is given by (37).

$$\Delta V_a = \Delta V_{au} + \Delta V_{al} =$$
$$2 \cdot (\frac{M}{2} \cdot \sin\omega t \cdot V_1\sin\omega t + \frac{1}{2}V_2\sin 2\omega t) \tag{37}$$

This means that DC phase leg ripple voltage contains only a 2nd harmonic component, which will produce a 2nd harmonic circulating current ripple.

$$i_{diff-ac} = I_{diff}\sin(2\omega t + \theta) \tag{38}$$

In a 3-phase application, assuming a balanced load, the DC-side ripple current is given by (39), which indicates that the current in the DC side will not have a 2nd harmonic component.

$$\Delta I_{dc-3ph} = i_{diffa-ac} + i_{diffb-ac} + i_{diffc-ac}$$
$$= I_{diffa}\sin(2\omega t + \theta) + I_{diffb}\sin(2(\omega t + 120^o) + \theta)$$
$$+ I_{diffc}\sin(2(\omega t + 240^o) + \theta) \tag{39}$$
$$= I_{diffa}[\sin(2\omega t + \theta) + \sin(2\omega t + \theta + 240^o)$$
$$+ \sin(2\omega t + \theta + 120^o)] = 0$$

For a 2-phase-leg inverter, however, instead of cancelling each other, the 2nd harmonic components will be doubled in the DC-side current, as shown in (40).

$$\Delta I_{dc} = \Delta i_{diff_a} + \Delta i_{diff_b}$$
$$= I_{diff_a}\sin(2\omega t + \theta) + I_{diff_b}\sin(2(\omega t + 180^o) + \theta) \quad (40)$$
$$= 2I_{diff_a}\sin(2\omega t + \theta)$$

The DC-side current harmonics will increase transmission power losses and could potentially lead to DC network malfunction. The current circulating between phases will increase the semiconductor power losses, which may reduce efficiency and lead to overrating of devices. An input filter is often required for a conventional 2-level converter (Fig. 2), which stops the 2nd harmonic energy from being transmitted to the DC side. In contrast, MMCs feature distributed SM capacitance, where circulating current suppression control can be used to compensate the common-mode voltage by inserting and bypassing the required number of SMs.

2) Rationale for Current Suppression Control

Assumption 1 in Section III is not applicable since there are even harmonic components in the circulating current i_{diff} [28, 30]. Therefore, upper and lower arm currents are re-written as (41) and (42), and i_{diff} can be derived as (43).

$$i_{au} = i_{diff} + \frac{i_{ao}}{2} \quad (41)$$
$$i_{al} = i_{diff} - \frac{i_{ao}}{2} \quad (42)$$
$$i_{diff} = \frac{i_{au}+i_{al}}{2} \quad (43)$$

i_{diff} is generated by the voltage difference between V_{dc} and phase voltage. Before designing the current suppression controller, it is important to derive this voltage difference. According to Fig. 4, (44) and (45) can be obtained according to Kirchhoff's voltage law, where R represents the parasitic ohmic losses. The output voltage v_{ao} can be derived as the difference of (44) and (45), as presented in (46).

$$\frac{V_{dc}}{2} - v_{au} - Ri_{au} - L_{arm}\frac{di_{au}}{dt} - v_{ao} = 0 \quad (44)$$
$$\frac{V_{dc}}{2} + v_{ao} - Ri_{al} - L_{arm}\frac{di_{al}}{dt} - v_{al} = 0 \quad (45)$$
$$v_{ao} = \frac{-v_{au}+v_{al}}{2} + \frac{1}{2}Ri_{ao} + \frac{L_{arm}}{2}\frac{di_{ao}}{dt} \quad (46)$$

Equation (47) defines e_a as the differential mode component of the arm voltages, and illustrates that e_a controls the output current i_{ao} directly, i.e. controls the output power.

$$e_a = \frac{-v_{au}+v_{al}}{2} \quad (47)$$

By adding (44) and (45), and combining with (43), (48) can be derived.

$$V_{dc} - (v_{au} + v_{al}) = 2Ri_{diff} + 2L_{arm}\frac{di_{diff}}{dt} \quad (48)$$

As given by (49), u_{diff} denotes half of the voltage difference between the DC-side voltage and the sum of the upper and lower arm voltages. It shows that common-mode arm voltage u_{diff} gives rise to the circulating current (Fig. 11), which indicates that the control of i_{diff} can be realised by regulating u_{diff} [18]. The current control block diagram is shown in Fig. 12.
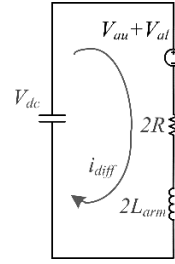

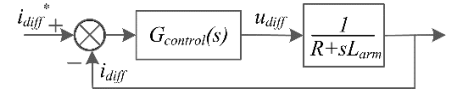Fig. 11. Equivalent circuit of circulating current.

Fig. 12. Current suppression control block diagram (i_{diff} is the feedback signal and i_{diff}* is the reference).

$$u_{diff} = \frac{V_{dc} - (v_{au} + v_{al})}{2} = Ri_{diff} + L_{arm}\frac{di_{diff}}{dt} \quad (49)$$

By substituting (47) into (49), the references for the upper and lower arm voltages are given by (50) and (51) [21].

$$v_{au}^* = \frac{V_{dc}}{2} - e_a - u_{diff} \quad (50)$$
$$v_{al}^* = \frac{V_{dc}}{2} + e_a - u_{diff} \quad (51)$$

e_a is generated by the main PWM controller to control the output voltage and power. u_{diff} is the voltage difference generated by the current suppression controller to suppress the circulating current.

3) Current Suppression Controllers

▪ **PR Control**

The standard proportional integral (PI) controller functions adequately for DC quantities. For single-phase AC, however, a PI controller introduces a residual constant error [31]. In contrast, a PR controller can achieve zero steady-state error at a certain operating frequency [32] due to its infinite gain, as shown in the Bode plot in Fig. 13. Additionally, the PR controller has a very narrow bandwidth, which ensures the controller only affects circulating current at a certain frequency. A PR controller is designed at 100 Hz to eliminate the 2nd harmonic circulating current.

The transfer function of the PR controller is given by (52).

$$G_{PR}(s) = K_P + \frac{K_r s}{s^2 + \omega_n^2} \quad (52)$$

where K_P and K_r are the proportional and resonant gains respectively, and ω_n is the resonant frequency.
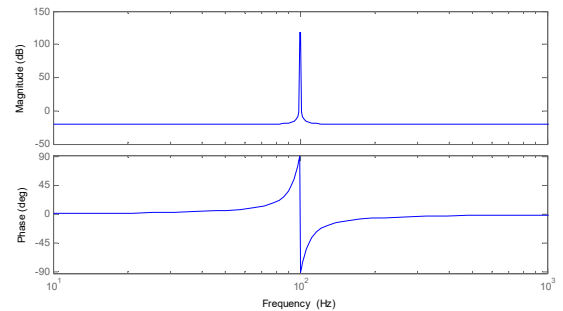

Fig. 13. Bode plot of PR controller at 100 Hz resonant frequency.

As shown in Fig. 14, half the sum of the arm currents is the circulating current i_{diff}. Then the high pass filter (5 Hz cut-off frequency) filters out the DC component leaving only harmonics (i_{diff_ac}), among which the 2nd harmonic dominates. The 2nd order harmonic current reference ($i^*_{diff\_ac}$) is set to zero and compared with i_{diff_ac}. Their difference is fed into a PR controller, which generates an infinite gain and achieves zero-steady state error at 100 Hz. The output u_{diff} is then subtracted from the arm voltage modulation references in (50) and (51) in order to compensate the voltage variations of the submodule capacitors.
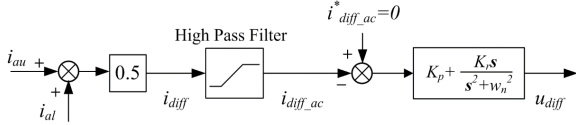

Fig. 14. PR control block for circulating current suppression.

Simulation results for a 10 kW 5-level 2-phase-leg Si MOSFET MMC are shown in Fig. 15. The figure shows that with the PR controller, the 2nd harmonic in the circulating current is almost eliminated and the arm currents are composed of a 50 Hz sine wave with a DC offset. With 1.5 mH arm inductance, the input DC current ripple is 4.2% which is within the 5% current distortion limit.
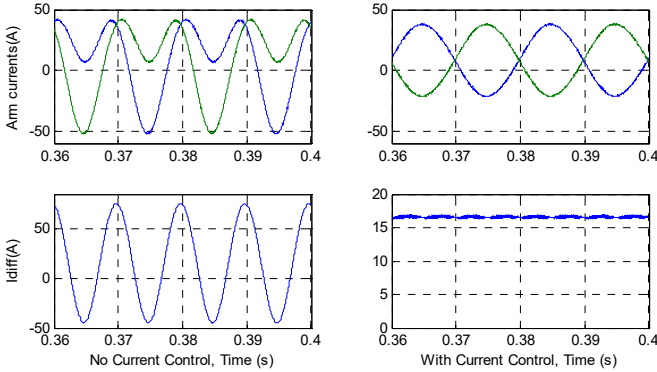

Fig. 15. Simulation results for arm currents and circulating current in a 5-level 2-phase-leg Si MOSFET MMC, without and with PR current control. (V_{dc}=600 V, V_{out}=240 V, 10 kW, L_{arm}=1.5 mH).

- **PI Control with Orthogonal Imaginary Axis**

DQ transformation is commonly used in three-phase systems, where AC signals are transformed to a two-axis, stationary (αβ) frame, then into a rotating (dq) reference frame where the signals are converted to DC quantities. Thereby, a PI controller can be adopted to achieve zero steady-state error. However, for a single-phase system, in order to apply dq transformation and achieve zero steady-state error, a fictitious phase must be created to generate an orthogonal plane [33]. There are many ways to generate the virtual axis from a single-phase signal, such as shifting the AC signal by 90° [34], or applying a first-order, all-pass filter phase shifter [35], or a second-order generalised integrator [36].

In this study, the orthogonal axis is generated by delaying the real signal by 90° (Fig. 16 (a)). The real current is i_{diff} after the high-pass filter, in which the 2nd harmonic dominates. The stationary αβ coordinate can be transformed to the dq coordinate system rotating at 100 Hz through the Park Transformation (53).
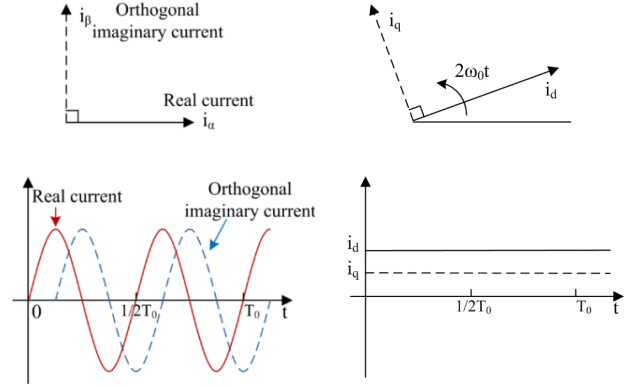
(a) Two phase stationary (αβ) frame   (b) Two phase rotary (dq) frame
Fig. 16. Reference frames for Park Transformation: T_0 is the fundamental time period and the real current is the 2nd harmonic component.

As shown in the control block diagram of Fig. 17, two DC quantities, i_d and i_q, are generated after the Park Transformation. Reference signals i^*_d and i^*_q are set to zero to eliminate the input harmonic signal. A PI controller is then applied to ensure a zero steady-state error. Although i_q is imaginary and does not exist practically, the PI control action has been realised in the dq reference frame. The compensation, however, is only applied to the real signal, i.e. only u_{diff} will be used for (50) and (51).

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (53)$$

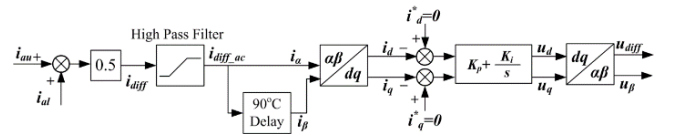where $\omega t = 2(2\pi/T_0)t$ in this application.

Fig. 17. PI current suppression control block diagram with imaginary orthogonal axis.

Simulation results for a 10 kW 5-level 2-phase-leg Si MOSFET MMC are shown in Fig. 18. With a PI controller, the 2nd harmonic in the circulating current is almost eliminated. Similar to the PR controller, PI controlled input DC current ripple is 4.2%.

B. Output Voltage Regulation

The voltage regulation is designed to stabilise the output voltage for varying load conditions. When the load current changes, the voltage drop across the arm inductors and filter will change, which gives rise to an error between the output voltage v_o and the output voltage reference v^* (Fig. 19). For single-phase AC, a PR controller with 50 Hz resonant

frequency is adopted because it can provide zero steady-state error [29]. Parameters for the overall control schematic blocks shown in Fig. 19 are listed in Table 3.
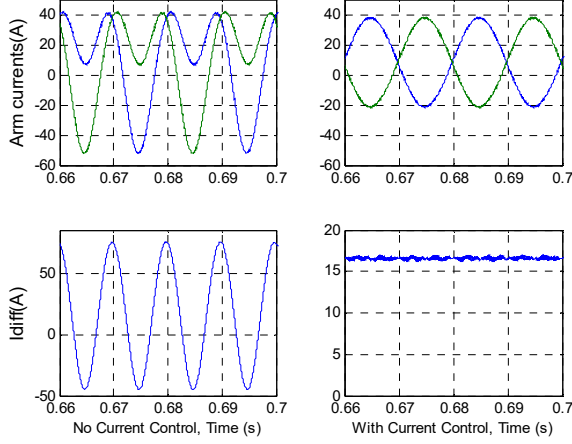

Fig. 18. Simulation results for arm currents and circulating current in a 5-level 2-phase-leg Si MOSFET MMC, without and with PI current control. (V_{dc}=600 V, V_{out}=240 V, 1.5 kW, L_{arm}=1.5 mH).

The PR controller generates the 50 Hz fundamental control signal for the MMC. For example, (54) shows the relationship of inverter output v_{inv} and DC-side voltage in a single-phase-leg MMC, where M and Θ are generated by the PR controller according to the arm inductance, filter impedance and the error between v_o and v^*. To simplify the mathematics, the filter is assumed to be a passive LC filter.

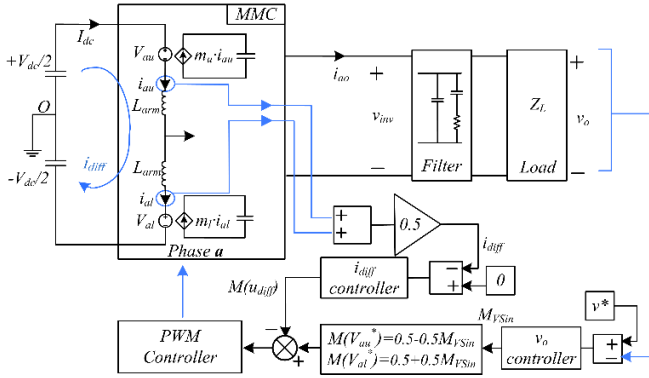$$V_{inv} = M_{Vsin} \cdot V_{dc} = M\sin(\omega t + \theta) V_{dc} \qquad (54)$$

Fig. 19. Overall control schematic blocks of MMC.

Table 3 Parameters for the MMC overall control schematic

v_o	Output load voltage
v^*	Output voltage reference
v_{inv}	Inverter output
Z_L	Load impedance
M_{Vsin}	Output modulation signal of voltage controller
$M(V_{au})$	Upper arm modulation signal
$M(V_{al})$	Lower arm modulation signal
$M(u_{diff})$	Compensating signal of circulating current suppression control

Based on Fig. 19, the impedance of C_f in parallel with Z_L is expressed by (55). The inductance is the sum of half the arm inductance ($L_{arm}/2$) and the filter inductance. Hence v_o and v_{inv} are related according to (56), where γ is the angle difference between v_o and v_{inv}.

$$Z_o = C_f // Z_L = \frac{Z_L}{1+j\omega C_f Z_L} \qquad (55)$$

$$v_o = \frac{Z_o}{j\omega(\frac{L_{arm}}{2}+L_f)+Z_o} \cdot v_{inv} = |Z|e^{j\gamma} v_{inv} \qquad (56)$$

Equation (57) is derived by substituting (54) into (56). M and Θ are calculated by evaluating the amplitude and phase angle of (57), as shown in (58) and (59) respectively.

$$\hat{V}_o \sin\omega t = |Z| \cdot M \cdot \sin(\omega t + \theta + \gamma) \cdot V_{dc} \qquad (57)$$

$$M = \frac{\hat{V}_o}{|Z| \cdot v_{dc}} \qquad (58)$$

$$\theta = -\gamma = \tan^{-1}\frac{\omega R_L(\frac{L_{arm}}{2}+L_f)}{F \cdot |Z_L|^2 + \omega X_L(\frac{L_{arm}}{2}+L_f)} \qquad (59)$$

where $\hat{V}_o$ is the peak output voltage, and $Z_L = R_L + jX_L$ is the load impedance.

F is a factor relating the arm inductance and filter parameters, and Z refers to the impedance proportion that defines the voltage sharing, as shown in (60) and (61).

$$F = 1 - \omega^2 C_f \left(\frac{L_{arm}}{2} + L_f\right) \qquad (60)$$

$$Z = \frac{F \cdot |Z_L|^2 + \omega X_L(\frac{L_{arm}}{2}+L_f) - j\omega R_L(\frac{L_{arm}}{2}+L_f)}{F^2 \cdot |Z_L|^2 + 2\omega X_L(\frac{L_{arm}}{2}+L_f) \cdot F + \omega^2(\frac{L_{arm}}{2}+L_f)^2} \qquad (61)$$

The PR controller is able to generate M and Θ automatically to compensate the output voltage error. Fig. 20 shows the simulation results for a 5-level MMC, where the output power changes from 500 W to 10 kW at t=0.2 s.
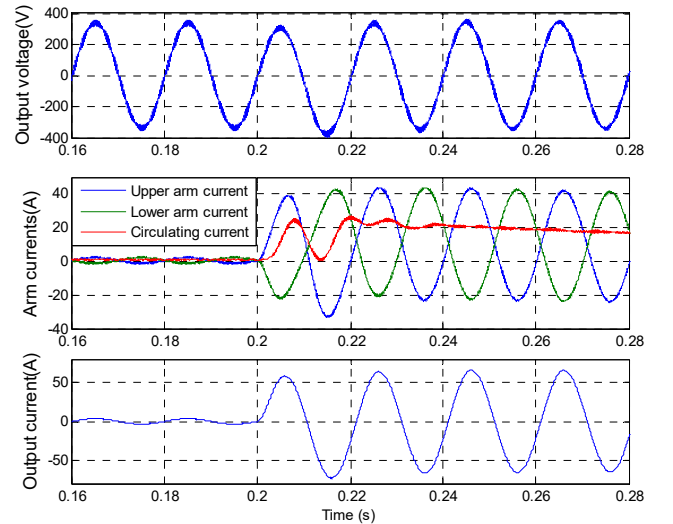

Fig. 20. Voltage and currents waveforms for a 10 kW two-phase-leg 5-level MMC when the load is increased at t=0.2 s.

The results indicate that the output voltage v_o can be stabilised during the transition from almost no load to the full-load condition. Arm currents and output current undergo

a sudden increase at t=0.2 s, and the arm currents are stable and free from 2nd harmonic distortion. The FFT analysis shows that the total harmonic distortion (THD) of the output voltage and current are 3.98% and 0.46% respectively, thus indicating very high quality output power.

V. EXPERIMENTAL RESULTS AND ANALYSIS

A MOSFET-based single-phase-leg 5-level MMC test rig was built to verify the two current suppression control methods.

A. Hardware Setup

The MMC prototype consists of 4 SMs in one arm, a TI F28335 digital signal processor (DSP) and voltage and current transducers, as shown in Fig. 21. The 5-level single-phase-leg MMC circuit diagram is shown in Fig. 22 and its signal process is shown in Fig. 23. Eight SM capacitor voltage signals and two currents signals are detected by the voltage and current transducers. The ten feedback signals from the transducers are sent to the interface circuits, which provide isolation. The DSP implements current suppression control with a 10 kHz overall switching frequency. Eight PWM signals are generated to control the SMs, with complimentary circuit boards to create complimentary signals from these eight signals with a 2 μs dead-time for each power MOSFETs.
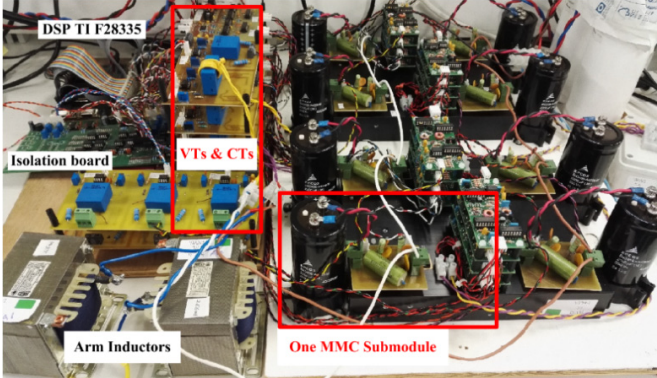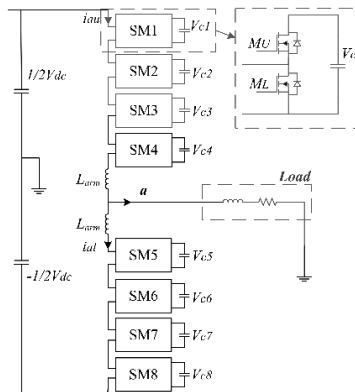

Fig. 21. Single-phase-leg 5-level MMC prototype.

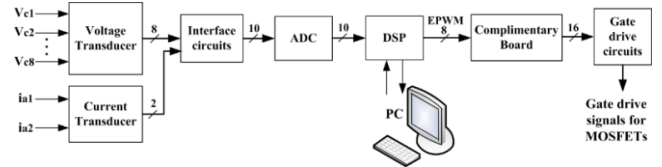

Fig. 22. Test rig topology: 5-level single-phase-leg MMC.

Fig. 23. 5-level single-phase-leg MMC signal process.
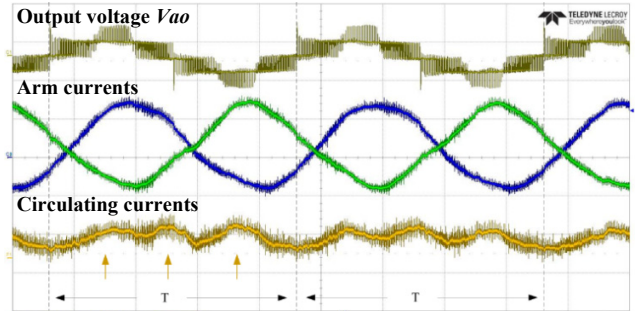
B. Experimental Results

Table 4 lists the experimental parameters for the single-phase-leg 5-level MMC. Two different current suppression control strategies, PR control and PI control with orthogonal imaginary axis, are applied and results are shown in Fig. 24.

Table 4 Experimental parameters for the single-phase-leg 5-level MMC

Submodule capacitance	3.3 mF	Arm inductance	1.5 mH
Snubber capacitance	5.6 nF	Snubber resistance	3.3 Ω
Switching frequency	10 kHz	Input DC voltage	150 V
Load resistance	8.9 Ω	Load inductance	12.5 mH

The two current suppression controllers were designed assuming perfect balanced SM capacitances. Their simulation results were proved to be equally effective, as shown in Fig. 15 and Fig. 18. However, as shown in Fig. 24, the experimental results for both control methods show the presence of circulating current components that are not predicted by the initial simulation. Compared to the tuned PR second harmonic current controller, the rotating frame PI controller gives a superior level of performance. Fig. 24(a) also shows that with PR control the circulating current contains fundamental and third harmonic components.

(a) With PR current suppression control
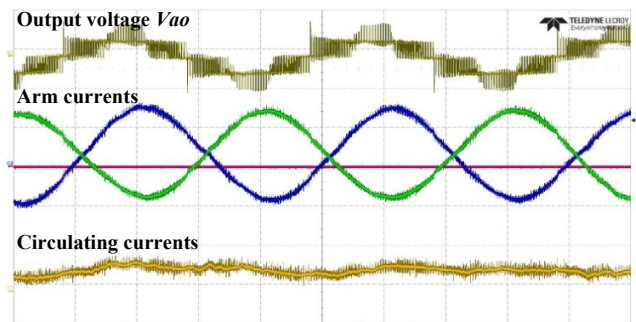
(b) With PI current suppression control

Fig. 24. Experimental waveforms for single-phase-leg 5-level MMC (V_{ao}: 100 V/div; Currents: 2 A/div).

A number of issues have been identified which can result in degraded performance of the circulating current controller. First of all, in the Matlab simulation, all the submodules are identical. However, in the test rig there is device-to-device deviation of SM capacitance. The standard capacitor tolerance is ±20% [37]. The nth harmonic capacitor voltage $\Delta u_C^{(n)}(t)$ in (32) will not be the same for upper and lower arms because of different C values, i.e. the amplitudes of nth harmonic capacitor voltages V_n are different for upper and lower voltages. Therefore, ripple voltage across the phase leg can be rewritten as (62).

$$\Delta V_a = \Delta V_{au} + \Delta V_{al} = \frac{1}{2}(V_{1l} - V_{1u})\sin\omega t + \frac{1}{2}\cdot$$
$$[M(V_{1u} + V_{1l})\sin^2\omega t + (V_{2u} + V_{2l})\sin 2\omega t] + \frac{M}{2}\cdot \quad (62)$$
$$(V_{2l} - V_{2u})\sin\omega t \sin 2\omega t$$

There are fundamental and 3rd harmonic components in the ripple voltage across one phase, which will result in unbalanced arm currents and give rise to odd harmonics in the circulating current.

To further investigate the effects of capacitance variation, a worst-case capacitance deviation between upper and lower arms, i.e. -20% less capacitance in the upper arm and +20% more capacitance in the lower arm, was assumed.
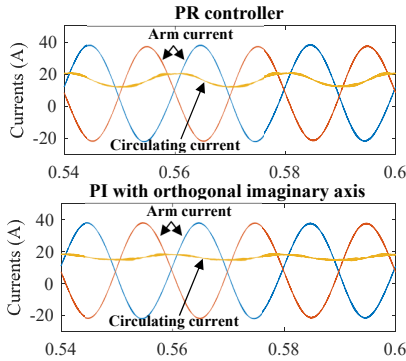

Fig. 25   Simulated arm and circulating currents with mismatched capacitance under PI and PR control.

(a) 2nd harmonic PR control   (b) PI with orthogonal imaginary axis
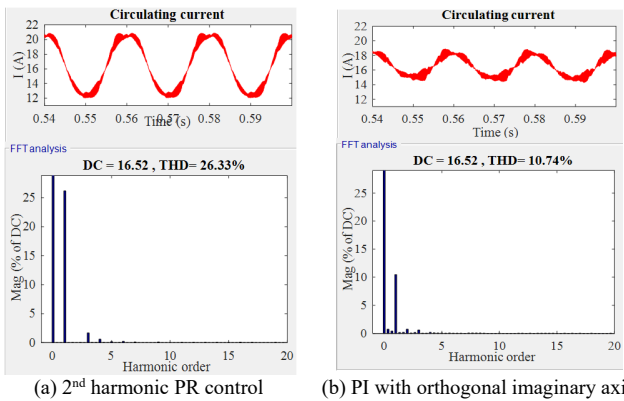
Fig. 26   FFT analysis of circulating current with mismatched capacitance under PI and PR control.

Fig. 25 and Fig. 26 respectively show the resulting simulated arm and circulating current waveforms and their FFT analysis under both PR and PI with orthogonal imaginary axis control schemes. The figures show that the PI with orthogonal imaginary axis controller performs better than the PR controller, having a THD of approximately half of that of the PR scheme.

C.   Improved Circulating Current Control Models

The original PR and PI with orthogonal imaginary axis control options are two variants of narrow bandwidth controllers designed to eliminate the predicted 2nd harmonic. This approach allows the 'natural' DC current to flow, controlling AC components to zero. For both control approaches, however, practical results and FFT analysis indicate the presence of other harmonic components in the circulating current resulting from capacitor mismatch. Amongst the techniques that could be employed, the addition of parallel-connected control stages is a simple means of suppressing these additional harmonic components. Additional PI controllers with orthogonal imaginary axes rotating at frequencies chosen to control the harmonic components may be connected in parallel. Similarly, PR controllers with carefully selected resonant frequencies which coincide with and therefore suppress the undesired harmonic current components may also be connected in parallel.

(1) Parallel-connected PR controllers

Parallel-connected PR controllers with resonances at the fundamental, 2nd, 3rd and 4th harmonic frequencies were designed as shown in (63).

$$G_{PR}(s) = K_P + \sum \frac{K_{rh}\cdot s}{s^2 + (h\cdot\omega_0)^2}, \quad h = 1,2,3,4 \quad (63)$$

where ω_0 denotes the fundamental frequency and h is the harmonic order.

(2) Parallel-connected PI controllers

In this improved controller, two PI controllers with dq reference frames rotating at 100 Hz and 50 Hz are connected in parallel.

Simulation results for the modified PR and PI control schemes operating under conditions of capacitance mismatch are presented in Fig. 27.

The FFT analysis shown in Table 5 illustrates that the modified controllers can improve the circulating current, with the THD attributed to all of the examined frequency components being significantly reduced in comparison to the original control topologies. In contrast to the simulation results presented in Fig. 26 where the PI control scheme outperformed the PR scheme with regard to THD, the parallel-connected PR controller exhibits superior performance to that of the parallel-connected PI scheme. This may be attributed to the two additional control frequencies introduced by the parallel-connected PR approach.
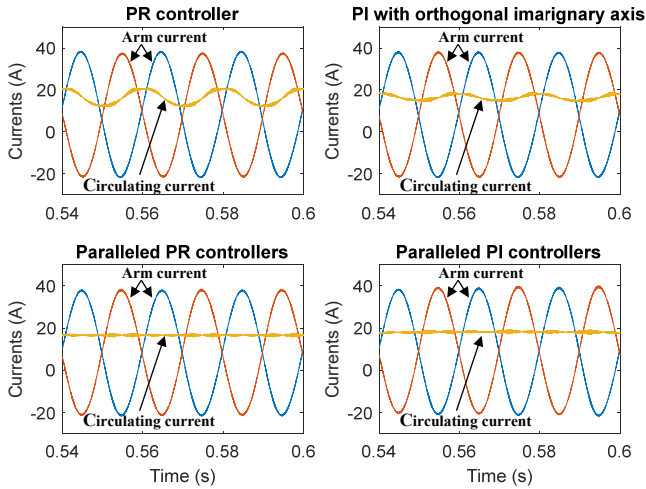
Fig. 27 Current simulation waveforms under capacitance mismatch with improved controllers

Table 5 THD analysis of circulating current under different control methods

	PR	Parallel-connected PR	PI	Parallel-connected PI
Total THD	26.33 %	1.98 %	10.74 %	2.24 %
Fundamental	26.19 %	0.03 %	10.47 %	0.3 %
2nd harmonic	0.02 %	0.01 %	0.76 %	0.44 %
3rd harmonic	1.69 %	0.02 %	0.61 %	0.23 %
4th harmonic	0.59 %	0.06 %	0.19 %	0.1 %

D. Analysis of Experimental Results

Comparing the two original control methods, the superior performance of the PI controller can be attributed to two factors. Firstly, the PI controller has a larger bandwidth. For example, after the Park Transformation at 100 Hz, the third harmonic signal is converted into either 50 Hz or 250 Hz. The PI controller still has certain gains at these two frequencies that might help to suppress the harmonics. However, the PR controller has a very narrow bandwidth as presented in Fig. 13, which has no effect on other frequency harmonics. This is verified by the simulation results shown in Fig. 26.

Another reason for the difference between these two controllers is the discretisation method used when implementing the controller in the DSP. Zero-order hold (ZOH) is employed for both controllers. For systems with time delays in feedback loops, the ZOH method leads to an approximate discretisation rather than an exact discretisation [38]. The PR controller is second-order and its implementation requires a relatively high sampling frequency. It is therefore more sensitive to discretisation errors. In contrast, for the first-order PI controller, the ZOH method is able to provide better accuracy [39].

In conclusion, for practical single-phase LV MMC, a PI controller with an orthogonal imaginary axis performs well and is simple to implement. If further improved performance is required, a parallel-connected PR controller with resonances at the fundamental, 2nd, 3rd and 4th harmonic frequencies, or a parallel-connected PI controller with rotary frames at the fundamental and 2nd harmonic frequencies were

proposed and were shown, through simulation studies, to be effective.

VI. CONCLUSION

Detailed design of a 5-level Si MOSFET-based MMC for LVDC distribution applications has been presented. General equations for a 2-phase-leg MMC to enable sizing of the SM capacitance and arm inductance were presented based on SM voltage oscillation and DC-side current variation requirements respectively. Simulation results showed that a small output filter is required when an MMC with fewer than 13 levels is used to meet a 5% voltage distortion limit. A parallel damped filter with a 200 nF capacitor was accordingly designed for the 5-level MMC.

The 2nd harmonic component in the circulating current is a severe problem as it doubles in amplitude at the DC-side for 2-phase-leg converters, leading to increased converter and DC cable losses. To suppress 2nd harmonic current, double line-frequency PI with orthogonal imaginary axis control was designed and compared with double line-frequency PR control. Simulation results showed that performance of the two controllers was comparable. However, experimental results for a 5-level MMC hardware prototype showed that circulating current contains odd harmonic components due to the device-to-device deviation of SM capacitance. Experimental results presented showed that the PI with orthogonal imaginary axis controller has superior harmonic suppression performance when compared to the PR controller. The first-order PI controller is less susceptible to discretisation errors introduced during DSP implementation, increasing its reliability. Additionally the increased bandwidth of the PI controller in comparison to the PR approach makes it more effective in improving current THD. The second-order PR controller is more sensitive to discretisation errors as well as requiring a relatively high sampling frequency. Therefore, PI with orthogonal imaginary axis control is recommended for LV MMC applications. To further improve current suppression performance, a parallel-connected PR controller with resonances at the fundamental, 2nd, 3rd and 4th harmonic frequencies, or a parallel-connected PI controller with dq reference frames rotating at the fundamental and 2nd harmonic frequencies may be employed.

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