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Improvement of Boron Doping in SiGe Raised Sources and Drains for FD-SOI Technology by Carbon Incorporation

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Selective epitaxial growth (SEG) of highly boron-doped SiGe (SiGe:B) is a key step to realize Raised Source and Drain (RSD) for applications in SiGe-based microelectronic devices. This paper is devoted to the optimization of boron dopant profiles in SiGe RSD. For this purpose Fully-Depleted Silicon-On-Insulator (FD-SOI) blanket and patterned wafers are considered. We show that, in both situations, a weak carbon incorporation increases the dopant level and flattens the boron profile in the RSD. Finally experimental conditions for optimal RSD fabrication are reported.

Introduction

In semiconductor industry, the continuous scaling reduction of CMOS components improves devices performances and reduces manufacturing cost. However, the electrostatic control of the channel must be very accurate. To address this requirement, a promising option for the technical nodes beyond 14 nm is based on Fully-Depleted Silicon-On-Insulator (FD-SOI) technology, using ultra-thin SOI films (less than 10 nm) on which Raised Source and Drain (RSD) are formed by selective epitaxial growth (SEG) of highly boron-doped SiGe [1] [2].
CMOS component functioning depends on different properties of the RSD including the quality of the selective epitaxial growth and the distribution of dopants inside the RSD.
Recently we have proposed an efficient low-temperature cleaning method optimized for further selective epitaxial growth of RSD on FD-SOI substrates [3]. In this paper we are now interested in the optimization of the dopant profile in the SiGe:B RSD. For this purpose we report on the impact of the FD-SOI surface preparation on the dopant profile, and on the influence of C incorporation in the doping properties. More precisely we show that on blanket wafers a carbon incorporation improves the dopant properties (dopant level and dopant profile) inside a thin SiGe:B layer. On this basis we will search optimized conditions that allow to in similar improvements on patterned wafers used in real conditions.

Experimental methods

In [3, 4] we explored wet cleans (as HF-last, and HFRCA), industrial dry cleaning (SiCoNi) and a combination of wet and dry cleanings to improve the surface state of FD-SOI wafers. More precisely we showed that a combination of HFRCA, Siconi and low-temperature baking is the most suitable cleaning method to reach a clean FD-SOI surface optimized for subsequent RSD epitaxial growth. A part of this work is devoted to an

analysis of the impact of these cleaning methods on the doping profile inside the RSD. The cleaning methods we have used have been described in ref. [3] but are also synthetically reported in table I.

The selective epitaxial growth of SiGe:B and SiGe films on such cleaned surfaces has been realized with Epi 300 Centura setup from Applied Materials® using reduced pressure (RP) chemical vapor deposition (CVD) [5]. The epitaxial layers grow in the temperature range of 550 - 700 °C at 10 Torr with SiH_2Cl_2 and SiH_4 gases for SiGe:B and SiGe channel growth. The precursor gases for germanium and boron incorporation are GeH_4 and B_2H_6. Moreover, HCl and H_2 have been used as carrier and etchant gases, respectively. Both SiGe:B and SiGe:B(RSD)/SiGe(channel) epitaxial layers were investigated on SOI blanket and pattern wafers.

The dopant profiles are analyzed by Secondary Ion Mass Spectrometry SIMS developed by CAMECA IMS instrument.

Table I. Description of the different wet and plasma cleaning used in this work.

Type	Products	Process
SC1 (or **APM** Ammonium Peroxide Mixture)	**NH_4OH** (ammoniac) then DI water	**Removing particles** SC1 oxide and deoxidation simultaneously. This has the effect of oxidize the silicon as the basis particles, and then "reject" the particles by electrostatic repulsion during the deoxydation. The effectiveness of SC1 may be increased with the addition of an action Physics : (*megasonic or Spray: not used in your case)*
SC2 *(or **dHCl** for diluted HCl)*	**HCl** (Hydrochloric acid) then DI water	**Removing of metal contamination** SC2 dissolved metals. In the case, we will in fact dilute HCl (H_2O_2 not used but single wafer tool).
HF (***HF-Last***)	**HF** (Hydrofluoric acid) then DI water then N_2-blow dry	**Deoxidation** Isotropic and selectively. Only the diluted HF (0.25 to 2%) will be used in cleaning recipes: selectively etching the oxide.
RCA	***SC1*** **then *SC2***	**Chemical oxide**
HF-RCA	**HF** **then *SC1*** **then *SC2***	Process used when the plates must be cleaned and deoxidizing.
SiCoNi	**NH_4F plasma**	**Deoxidation** An in-situ dry chemical cleaning technology has been developed and integrated to RT-CVD tool [3, 6, 7].

Results and Discussion

I. B dopant profile on blanket wafers: surface cleaning and C incorporation impact

The SiGe:B film (thickness = 8 nm) has been deposited on a Si(001) surface or a SiGe epitaxial film previously cleaned with HF last, Siconi, HF last+SiCoNi, or HFRCA+SiCoNi processes. Fig.1a shows the boron profiles measured in the SiGe:B film grown on Si(001) whereas Fig. 1b shows the boron profiles in the SiGe:B film grown on SiGe.

For SiGe:B/Si(001), Fig.1a shows that whatever the cleaning method the boron concentration is not homogeneous but exhibits an interfacial excess. Notice that weak differences exist according to the surface preparation. For instance, the interfacial excess is slightly higher with a sole HF-Last cleaning than with HF-RCA+SiCoNi cleaning.

For SiGe:B/SiGe, Fig. 1b shows again an interfacial excess of boron. However in this case the cleaning process influences more the boron profile than previously. More precisely, the combination HF-RCA+Siconi cleaning only produces a weak interfacial effect in agreement with previous results that showed that HF-RCA+SiCoNi cleaning optimizes (reduces) the residual roughness of FD-SOI surfaces [3].

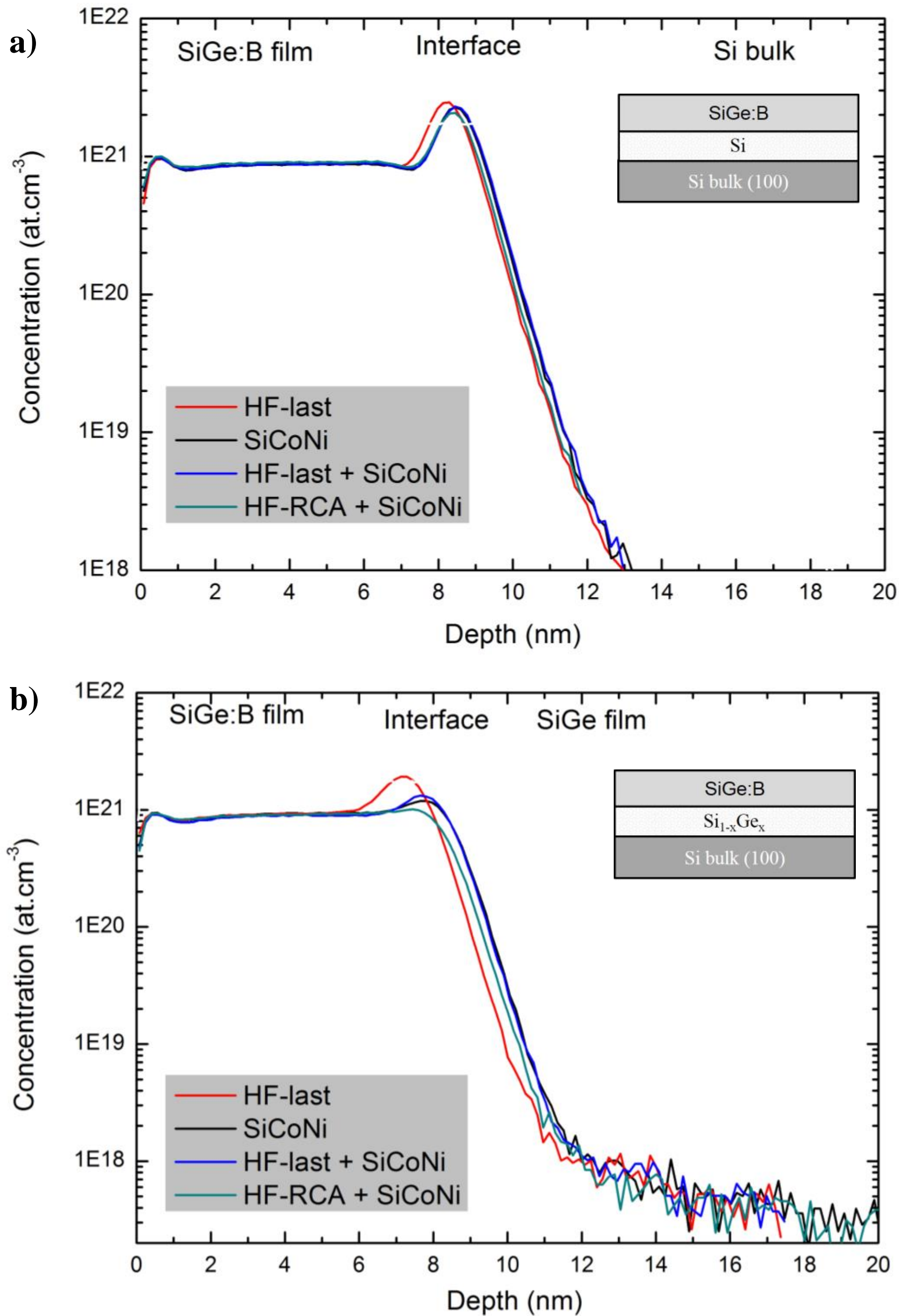

Figure 1. SIMS depth profiles of the boron atoms grown on blanket wafers with different surface preparation on (a) Silicon and (b) SiGe epitaxy.

Fig.2 shows the boron profile recorded in SiCoNi-cleaned SiGe:B/SiGe after carbon incorporation of (~1%) during the RSD epitaxy. Two main effects of the carbon incorporation are clearly shown: (i) an increase of the average doping level (roughly $2x10^{21}$ instead of $9x10^{20}$ at.cm^{-3}) and (ii) the complete vanishing of the interfacial peak we attribute to substitutional C that reduces B diffusion. Notice that all incorporated

boron atoms do not participate to the electrical doping. For 2.10^{21} at.cm^{-3} of boron, thermal activation actually leads to 3.10^{20} at.cm^{-3} of active (substitutional) boron (see table II).

Table II. Relative percentage of active, substitutional and total boron concentration.

Samples	Active [B]	Substitutional [B]	Total [B]	Ge (%)
Measured by	**MBIR**	**XRD**	**SIMS**	**Ellipsometry**
(at.cm^{-3})	2.7 10^{20}	8.210^{20}	1,64 10^{21}	34,7

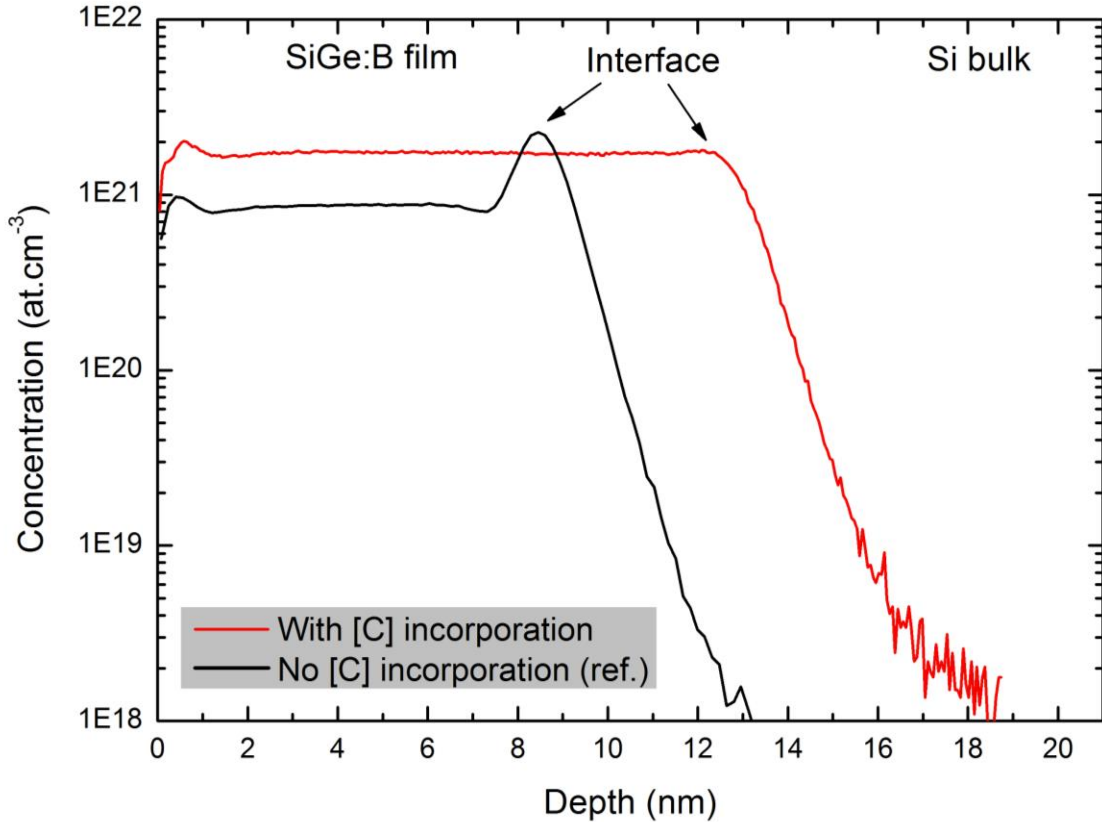

Figure 2. SIMS depth profiles of the boron atoms grown on blanket wafers with adding [C] and SiCoNi clean.

II. Optimization of C incorporation in case of patterned wafers

Since C incorporation widely improves the doping properties on blanket wafers, we now intend to transfer the process to patterned wafers, and more precisely to find the best experimental conditions to reach a high doping level with homogeneous Boron concentration (flat profile) in RSD epitaxially grown on patterned wafers.

Fig.3 shows the boron profiles recorded using high or low B_2H_6 flow conditions respectively. Increasing the B_2H_6 flow degrades the doping profile and greatly increases the interfacial boron peak. Fig.3 also evidences that C incorporation widely improves the profile concentration in both situations of low and high B_2H_6 flow.

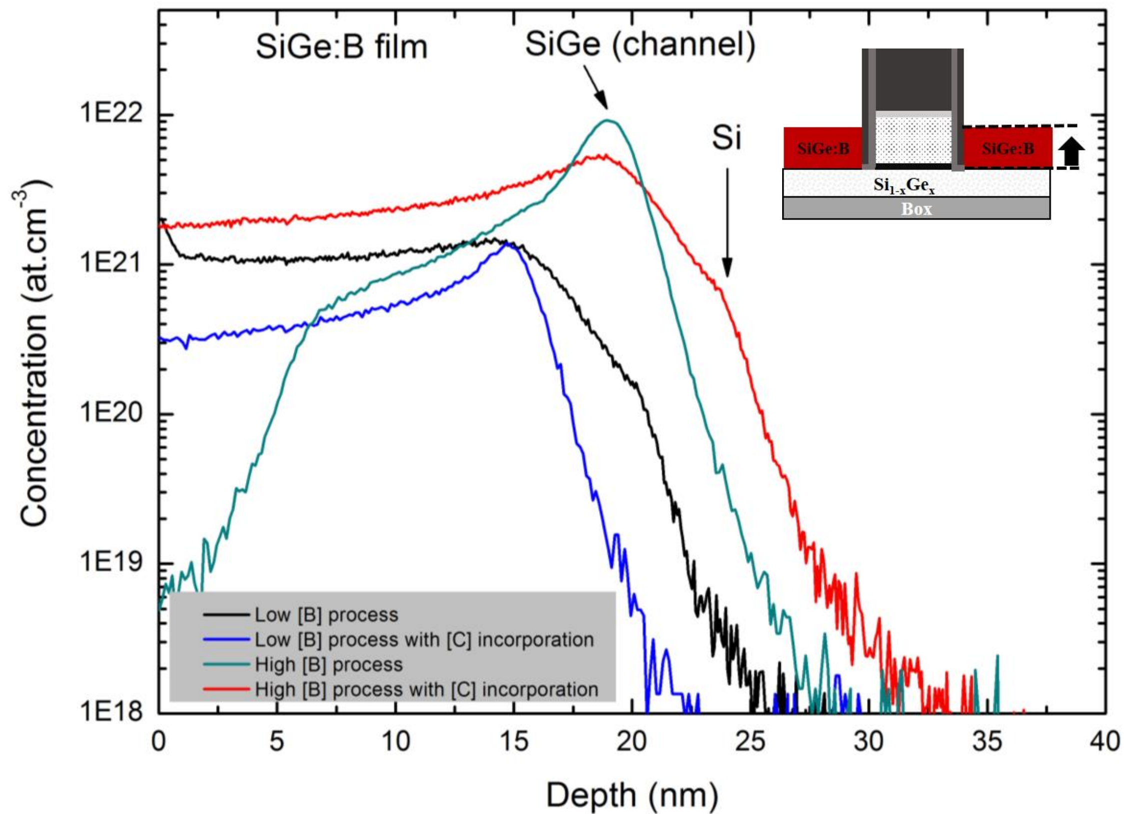

Figure 3. Boron SIMS profiles in SiGe:B film grown on pattern wafers with and without carbon addition for two conditions doping levels. The surface cleaning is combination HF-last + SiCoNi.

We have also measured the effect of a high or a low C incorporation and the impact of a seed layer (0.5nm thick SiGe) on the boron profiles. As shown in Fig 4, low as well as high C incorporation flatten the boron profile but a higher level of doping results from the higher C concentration. However, a certain amount of B diffuses into the channel and even in the SOI substrate. Such un-wanted effect may have a negative impact on the devices performances. A proposed solution is to block boron penetration by incorporating a certain amount of H_2 or N_2 near the SiGe/SOI interface [8].

Fig.4 also shows the impact of classical Dynamical Surface Annealing (DSA) [9, 10] or conventional high temperature spike annealing [11] used for dopant activation. We recover our main previous results due to C incorporation: disappearance of the interfacial accumulation of B and increase of the dopant level. It is important to notice that the dopant activation annealing does not degrade the doping (neither the doping level nor the boron profile).

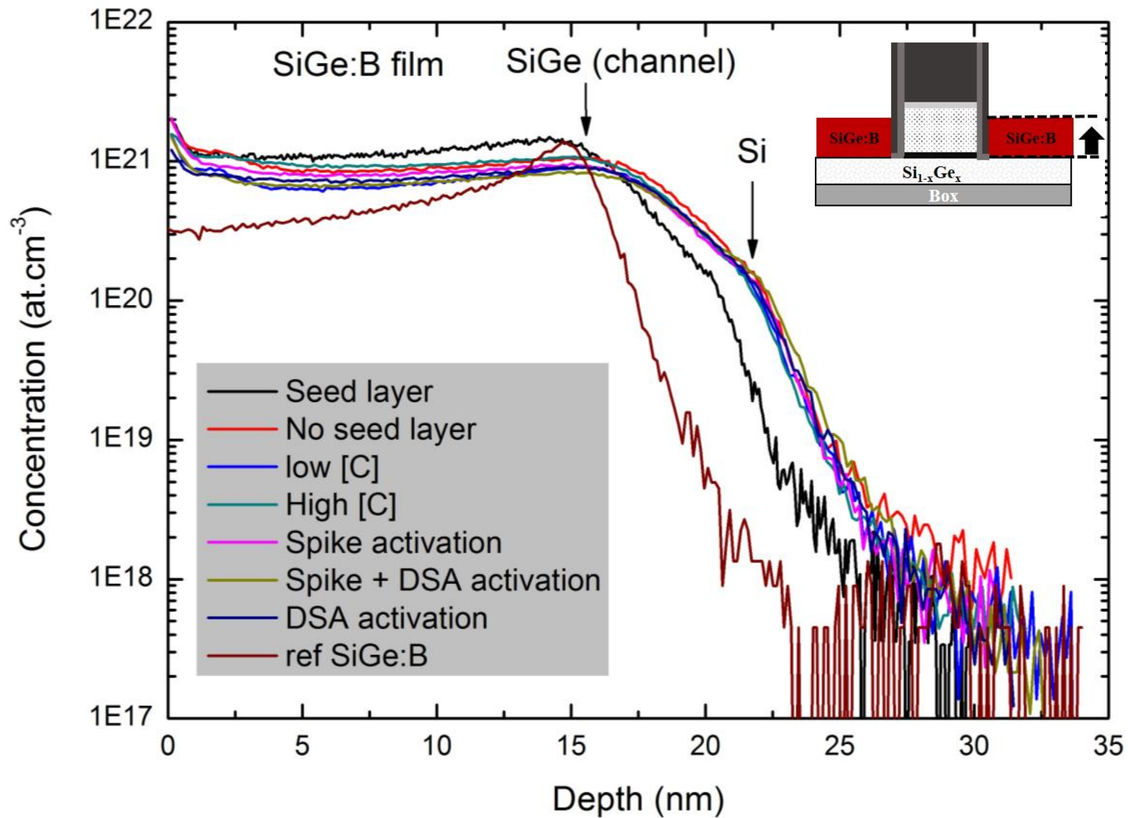

Figure 4. Boron SIMS profiles in SiGe:B film grown on pattern wafers with different doping levels and process methods. We also report, for comparison, a reference profile recorded without any c incorporation (ref SiGe:B)

III. Quality of epitaxially grown Raised Source and Drains

The quality of the epitaxial growth has been characterized by measuring, by AFM, the surface roughness at the end of the epitaxial process and by recording SEM and TEM images of the RSD.

Figure 5 shows the RMS height variation of epitaxial surfaces that result from the different studied processes: the surface roughness is greater for low C incorporation than for high C incorporation and the RMS increases with the B_2H_6 flow. On the other hand dopant activation processes do not significantly affect the surface roughness that remains comparable to that of the SiGe:B reference sample. The best surface roughness is thus reached with high [C] and after spike activation. Obviously the amount of C incorporated in the device is limited by its influence on the electronic properties. A good compromise seems to be a carbon amount in the range 0.5% - 1.5%.

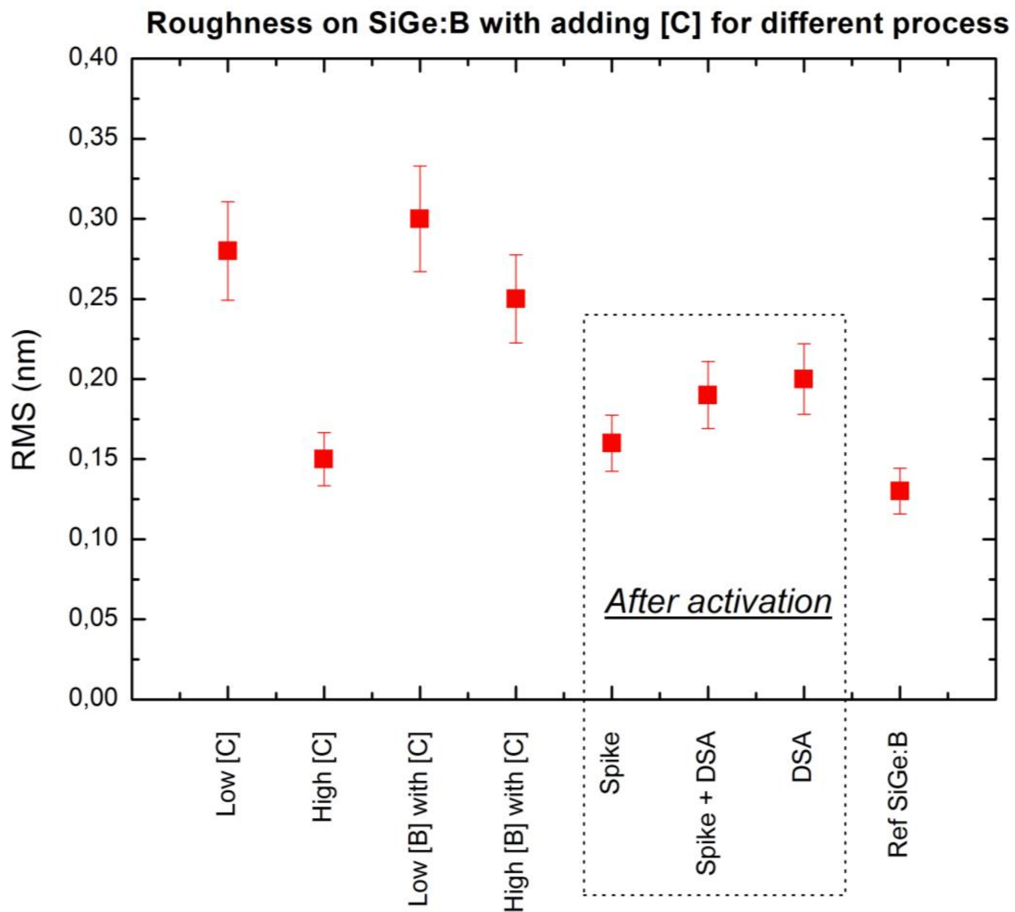

Figure 5. 30 µm x 30 µm atomic force microscopy images associated for different epitaxy process. RMS value on different SiGe:B for different epitaxy process and after activation. RMS value reference (no adding [C]) is 0.14 nm.

Figure 6 shows top view SEM images of SiGe:B film structure grown on patterned wafers using high [C] incorporation and spike dopant activation.

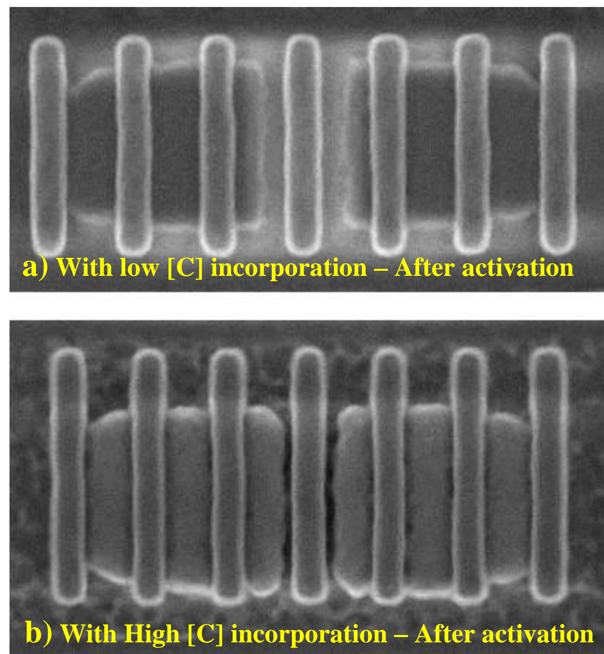

Figure 6. Top view SEM images of patterned wafers with adding [C], a) RSD Low [C] (after dopant activation), b) RSD High [C] (after dopant activation). Notice that the high carbon concentration reduces the SEG illustrated by the lower quality of the isolation central zone.

Figure 7 shows a x-TEM image of a CMOS device with $Si0_{.72}Ge_{0.28}$:B Raised Source and Drain ([B] > 8.0 10^{20} $at.cm^{-3}$) grown on a SiGe channel. The RSD has no facet and no visible defects and thus validates our procedure.

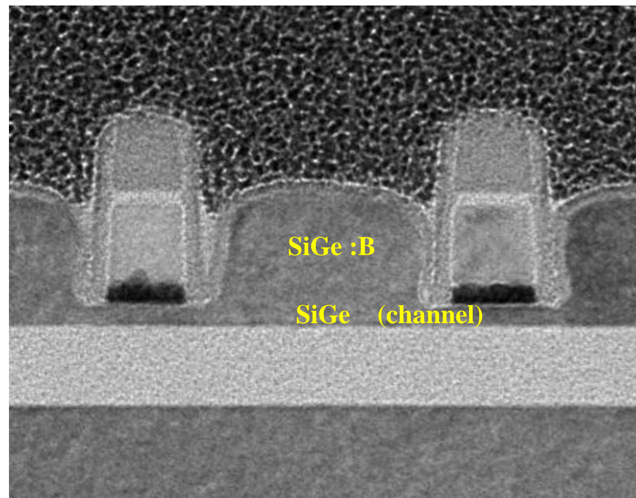

Figure 7. x-TEM image of selective SiGe:B with adding [C] epitaxial film grown on $Si_{0.72}Ge_{0.28}$ channel on patterned wafer.

Conclusion

In ref [3] we proposed a surface cleaning process that enables a subsequent good epitaxial quality of RSD. In this paper we show (i) how the surface cleanings may influence the

dopant profile in the RSD and (ii) that C incorporation rises the doping level and improves its homogeneity. Combining optimized pre-cleaning methods described in ref [3] with C incorporation, high B_2H_6 flux and spike activation of dopants described in the present work enable us to fabricate CMOS devices of high electronic quality. Electric characterizations are reported in a forthcoming paper.

Acknowledgments

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References

1. N. Loubet, T. Adam, M Raymond, Q. Liu, K. Cheng, R. Sreenivasan, A. Reznicek, P. Khare, W. Kleemeier, V. Paruchuri, B. Doris, R. Sampson, *Thin Solid Films* **520**, p.3149-3159 (2012).
2. J. M. Hartmann, V. Benevent, A. André, C. Sirisopanaporn, M. Veillerot, M. P. Samson, S. Barraud, Z. Essa, and B. Sermage, *ECS Journal of Solid State Science and Technology*, 3 (11) p.382-390 (2014).
3. M. Labrot, F. Cheynis, D. Barge, P. Müller, M. Juhel, *Applied Surface Science* **371**, p.436–446 (2016).
4. M. Knotter, *Handbook for Cleaning for Semiconductor Manufacturing: Fundamentals and Applications*. In: Karen A. Reinhardt, Richard F. Reidy (Eds.), Wiley, 2011 (April).
5. W. W. Wu, S. L. Cheng, S. W. Lee, and L. J. Chen, *J. Vac. Sci. Technol. B*, **21**, p.2147-2150 (2003).
6. H Yang, X Lu, CT Kao, M Chang – *US Patent* 7,780,793 (2010).
7. R Arghavani, CT Kao, X Lu - *US Patent* 7,955,510 (2011).
8. Z. Ma, J. Chen, Z. Liu, J. Krick, Y. Cheng, C. Hu, P. Ko, *IEEE, Electron device letters* **Vol 15 (3)**, p.109-111 (1994).
9. Y.-W. Chen, *17th IEEE International Conference on Advanced Processing of Semiconductors*, 2209.
10. C. Ortolland, E. Rosseel, N. Horiguchi, C. Kerner, S. Mertens, J. Kittl,E. Verleysen, H. Bender, W. Vandervost, A. Lauwers, P. P. Absil, S. Biesemans, S. Muthukrishnan, S. Srinivasan, A. J. Mayur, R. Schreutelkamp, and T. Hoffman, *IEDM Tech. Dig.*, p.23-26, (2009).
11. W. Lercha, S. Paul, J. Niess, S. McCoy, J. Gelpey, F. Cristiano, F. Severac, P. Fazzini, A. Martinez-Limia, P. Pichler, H. Kheyrandish, D. Bolze, *Materials Science and Engineering B,* **154–155**, p.3-13 (2008).