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Design of Low Power Vedic Multiplier Based on Reversible Logic

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ABSTRACT
Reversible logic is a new technique to reduce the power dissipation. There is no loss of information in reversible logic and produces unique output for specified inputs and vice-versa. There is no loss of bits so the power dissipation is reduced. In this paper new design for high speed, low power and area efficient 8-bit Vedic multiplier using Urdhva Tiryakbhyam Sutra (ancient methodology of Indian mathematics) is introduced and implemented using Reversible logic to generate products with low power dissipation. UT Sutra generates partial product and sum in single step with less number of adders unit when compare to conventional booth and array multipliers which will reduce the delay and area utilized, Reversible logic will reduce the power dissipation. An 8-bit Vedic multiplier is realized using a 4-bit Vedic multiplier and modified ripple carry adders. The proposed logic blocks are implemented using Verilog HDL programming language, simulation using Xilinx ISE software.
Keywords: Reversible Logic gates, Ripple carry Adder, Urdhva Tiryagbhyam Sutra, Vedic Mathematics.

I. INTRODUCTION

As the technology improves, the requirement also changes so the complexity of design. Power consumption has become the centre of attention for digital system design. Landauer's principle [1] states that in the irreversible logic the heat coming from computation was due to the destruction of information (wiping out bits of information) but not due to the processing of bits. Landauer showed that for every bit of information that is erased during an irreversible logic computation KTln2 joules of heat energy is generated, where K is the Boltzmann constant and T is the temperature in Kelvin at which the system is operating. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works like multiplication, convolution, Fourier calculations, and signal processing the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components.

A computation in which no information is lost is known Reversible and the gates used in designing are called reversible gates. This new approach of designing using reversible logic gates which reduces the power dissipation and improves system response time. Bennett[2] showed that in order to avoid energy dissipation in a circuit it must be built from reversible circuits. Reversible logic ensures zero information loss and low power dissipation. This is so because reversible computation does not require erasing any bit of information and consequently it does not dissipate any energy for computation.

Thus, Reversible logic circuits avoid energy loss by not computing the computed information by recycling the energy in the system. In the design of reversible circuits, two restrictions should be considered; firstly, Fan-out is not permitted and secondly, Feedback from gate outputs to inputs is not permitted. Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa. So, there is a one-to-one mapping between input and output vector. In an n-output reversible gate, the output vectors are permutations of the numbers 0 to 2n - 1.

Multiplication is most importance in Digital Signal Processing like Image and speech Processing. To implement the hardware module of Discrete Fourier, Cosine and Sine Transformations; large numbers of complex multipliers are required. There are so many novel designs and algorithms are projected multiplier design is always a challenging task and optimization required. The use of Vedic mathematics reduces the calculation compared to other multiplier design. Vedic mathematics is methodology of arithmetic rules that allow simple and effective speed implications. It provides some effective algorithm that can be applied in complex computation. Vedic mathematics was remade from the antiquated Indian scriptures (Vedas) by "Sri Bharati Krishna Tirtha" (1884-1660) after his exploration on Vedas. He developed 16 sutras and 16 upa sutras after broad research in "Atharva Veda". It has been discovered that Urdhva Tiryakbhayam is the most proficient among these. The proposed 8-bit multiplier is based on the "Urdhva Tiryakbhayam(UT)*"* sutra (algorithms). Urdhva Tiryakbhayam means "vertically and crosswise". Vedic multiplier also reduces transistor count in multiplier which is also an additive feature, improves the compactness of the system. This implementation requires TG, PG, and HNG

reversible gates as a whole improves the efficiency of the digital systems.

The paper organization follows: In section II, reversible logic and gates are discussed. Vedic Multiplication and sutra is discussed in section III. Proposed methodology for Vedic multiplier is in section IV. In Section V, RTL Design implementation of module using XilinxISE14.5. Section VI, has results and discussion. Finally, conclusion is given in Section VII.

II. REVERSIBLE LOGIC AND GATES.

Reversible logic is a promising computing design which presents a method for constructing computers with no heat dissipation. Reversible logic is the one of the upcoming technology used to reduce the heat generation due to the information loss. In reversible logic the computation process is reversible, i.e time-invertible. An *n*×*n* reversible circuit consists of *n* inputs and *n* outputs with mapping of each input pattern to a unique output pattern assignment and vice versa. Optimization and performance parameters of reversible logic are Garbage outputs (GO) which do not contribute to the reversible logic realization of the design. Quantum cast (QC) refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count (NG) is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions.

Features and design constrain of reversible logic.

- Reversible logic has an equal number of inputs and outputs.
- Fan-out is not allowed.
- Feedback paths are not allowed.
- Every output that is not used in the circuit is a garbage signal.
- The number of constants at the inputs of the gates should be kept as low as possible.

Basic reversible gates used in design are listed below

1. Feynman Gate (FG)

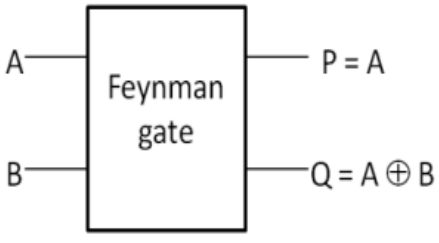

Fig.1. Feynman Gate

Feynman gate is a 2*2 reversible gate as shown in figure 3.2. The input vector is I (A, B) and the output vector is O(P, Q) and outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

2. Toffoil Gate (TG)

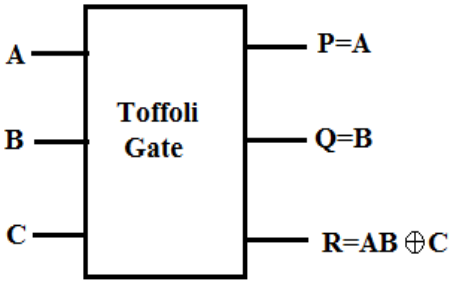

Fig.2. Toffoli Gate

Toffoli Gate is 3*3 gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕ C. Quantum cost of a Toffoli gate is 5. It is used to realize AND function; it is also used for realizing XOR function.

3. Peres Gate (PG)

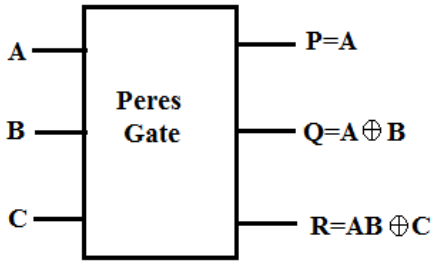

Fig.3. Peres Gate

In 3*3 Peres gate, the input vector is I (A, B, C) and output vector is O (P, Q, R). The output is given by P = A, Q = A⊕ B and R=AB⊕ C. Quantum cost of a Peres gate is 4. It is used for realization of half adder, Xor and And function.

4. HNG Gate.

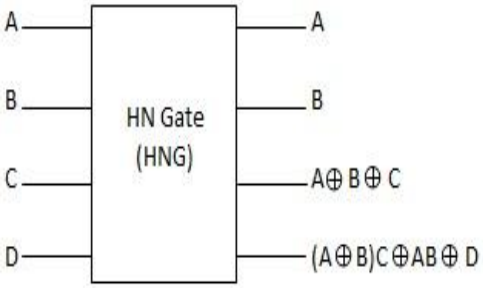

Fig.4. HNG Gate

It is a 4x4 bit gate and its quantum cost is six. The input vectors are I= (A, B, C, D) and output vectors are O= (A, B, A⊕B⊕C, (A⊕B)C⊕AB⊕D). It is used for designing full adders. HNG gate produces sum and carry in the same and thereby reduces the gate count and garbage outputs.

III. VEDIC MULTIPLIER

Vedic mathematics reduces the calculation compared to other multiplier design. Vedic mathematics is methodology of arithmetic rules that allow simple and effective speed implications. It provides some effective algorithm that can be applied in complex computation.

Urdhva Tiryakbhayam Sutra

The proposed 8-bit multiplier is based on the "Urdhva Tiryakbhayam(UT)*"* sutra (algorithms). UrdhvaTiryakbhayam means "vertically and crosswise". This UT sutra is a recognize from "Sthapatya- Veda" (book on construction and structural modeling as well as building designs), which is an upa-veda (supplement) of "Atharva Veda". These sutra have been traditionally used for multiplying two decimal number. This sutra also applied for the binary number to make the proposed algorithm suitable for the digital system. It is very simple compare to the conventional method of multiplication. Urdhva Tiryakbhyam Multiplication Algorithms is generalized multiplication formula applicable to all cases of multiplication. It means "Vertically and Crosswise" method. The digits at the two ends of the line are multiplied and the resultant output is added with the previous carry. When there are more lines involve in one step, all the results are added with the previous carry. The least significant digit of the number thus obtained after adding acts as one of the result digits and the rest act as the carry for the next step. Initially the carry bit is taken to be as zero. It is faster and easier than other algorithms like array and booths algorithms. For a "NxN" multiplier, it requires "NxN" AND gates, "Nx(N-2)" full adders and 'N' half adders. But Vedic multiplier requires only (N-1) adders. Figure 4 shows the steps involve in 4-Bit Vedic multiplier.

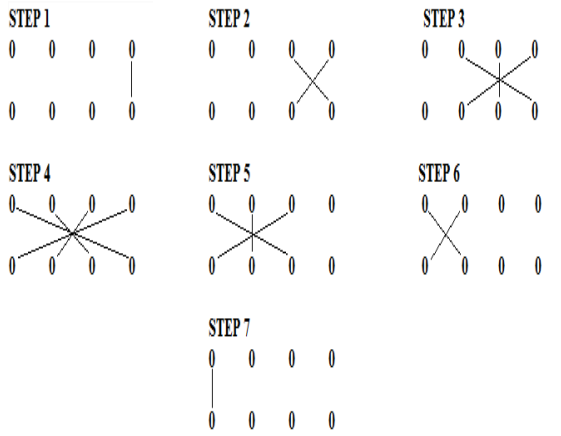

Fig.4. Vedic multiplication steps

For 3-bit binary number (110) and (011) multiplication using UT algorithm is shown in the figure 5.

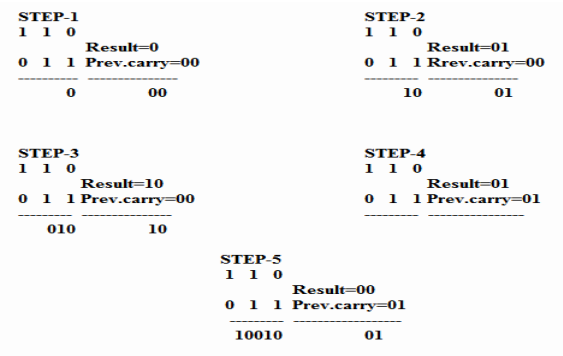

Fig.5. Multiplication of 3-Bit binary numbers using UT algorithm.

The digits at the two ends of the line (cross and vertical lines) are multiplied and the result is added with the previous carry. If there are more lines in one step, all the results are added with the previous carry if generated. The least significant digit of the numbers thus obtained after adding acts as one of the result digits and the rest of numbers act as the carry for the next step, where zero carry is considered as an initial condition. This algorithm is also true for the decimal numbers also.

IV. PROPOSED ARCHITECTURE.

The proposed 8x8 reversible vedic multiplier multiply two binary numbers and give 16-bit binary output. Peres gate and Feynman gates are used for designing the multiplier. The beauty of UT architecture is the generation of partial products and additions are done concurrently. The proposed vedic multiplier is design using reversible 2x2 and 4x4 vedic multiplier as its sub unit. Proposed 2x2, 4x4 and 8x8 vedic multiplier are describe below.

❖ **2x2 Vedic Multiplier**

It has two 2-bit binary number ***A*** and ***B*** as input and 4-bit number ***S*** as output. Where ***A*** =a1a0 and ***B*** =b1b0 let output is ***S*** =s3s2s1s0 and c1and c2 are the carry generated in s1 and the s2, which is shown in the figure 6.

Output is given as:

s0 = a0b0;

s1 = a1b0 + a0b1;

s2 = c1 + a1b1;

s3 =c2;

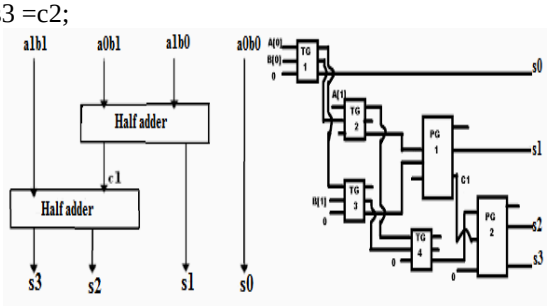

Fig.6. 2x2 Vedic multiplier using TG and PG gates.

There are four TG and two PG gates are used in realizing 2x2 Vedic multiplier. Total six reversible gates are used in this implementation. Number of constants and number of garbage values is six and quantum cost is 28. This implementation looks same as array and booth multiplier, So 2-bit Vedic multiplier does not give much advantage over other methods but 4x4 and 8x8 does.

❖ 4x4 Vedic Multiplier

The 4x4 bit binary vedic multiplier can be implemented using four 2x2 bit vedic multiplier unit. Let 4x4 multiplications having input A= a3a2a1a0 and B= b3b2b1b0 and the output the multiplication result is F= F7F6F5F4 F3F2F1F0. Using the fundamentals of UT sutra, taking two bits at a time and using four 2x2 multipliers, 4-bit binary multiplication will be calculated. The 4x4 vedic multiplier is shown in the figure 7.

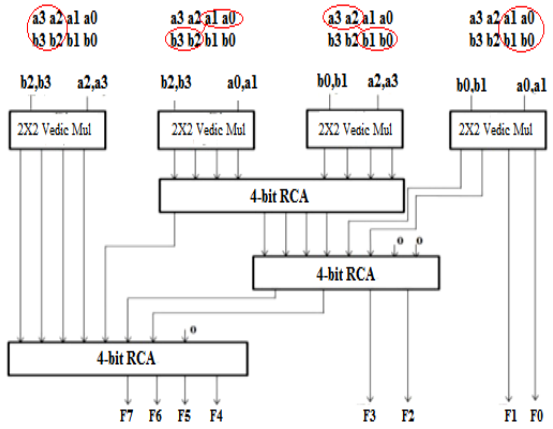

Fig.7. 4x4 Vedic multiplier

This design consists of four 2x2 vedic multiplier, and three 4-bit ripple carry adder circuit. This purposed design reduces the delay because it has property of concurrency. It has quantum cost of 144, constant input is 32 and garbage output is 44. The proposed 4x4 vedic multiplier has less quantum cost, constant inputs and garbage value as compare to design proposed in [4],[5]and [6] This design is used for implementing the proposed 8x8 vedic multiplier.

❖ 8x8 Vedic Multiplier

The proposed 8x8 vedic multiplier block diagram is shown in the figure 8. It is easily implanted using four 4x4 vedic multiplier and three 8-bit ripple carry adder. This makes the design of this proposed 8x8 multiplier very simple and efficient compare to the array and booth type multipliers. All the multipliers are made using PG and TG reversible gates. And RCA is design using HNG gates. So the designs are reversible in nature. It has quantum cost of 720.

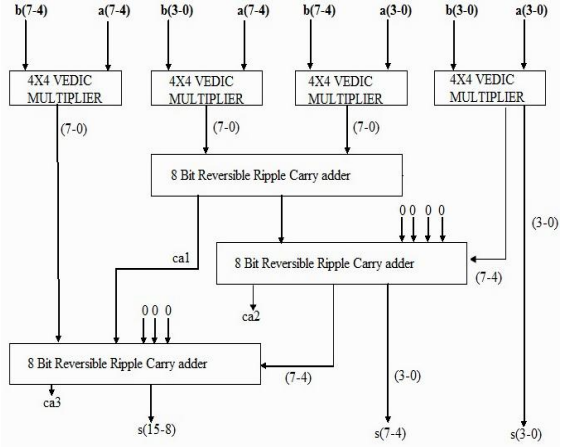

Fig.8. Proposed 8x8 Vedic multiplier.

❖ 8-bit Reversible Ripple Carry Adder

Reversible adder is proposed using HNG gate. In HNG gate if fourth input, D is made constant zero and inputs is given through A and B and carry to third input C then it act as reversible one bit full adder and output is taken from R and S respectively.

The proposed 8-bit reversible adder is form using HNG gate having two 8-bit inputs and a carry which is propagate from the list significant bit (LSB) to most significant bit (MSB) also known as ripple carry adder. The size of the reversible ripple carry adder is very small and it is very simple to design, so normally ripple carry adders are used for cascading. Each HNG gate act as one bit full adder so total eight HNG gates are required to built 8-bit ripple carry adder. Output is represented as S0-S7 and 'g' is the garbage. The 4 bit ripple carry adder is made with same HNG gate. In proposed adder total 16 garbage values are produced and having quantum cost of 48. The proposed reversible 8-bit ripple carry adder is shown in the figure 9.

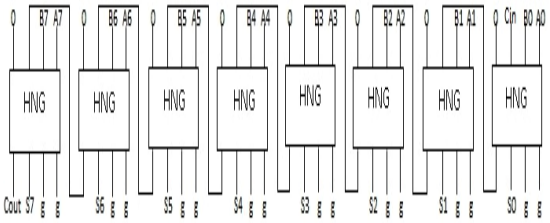

Fig.9. Proposed 8-Bit RCA using HNG Gate.

V. RTL DESIGN AND IMPLEMENTATIOM

The design architectures are written in VHDL language using Xilinx ISE 14.5 tool. The VHDL codes are simulated using ISIM tool present in the Xilinx and are implemented on Spartan LX45 board. The RTL design of 8x8 vedic multiplier and 8-bit ripple carry adder are as shown in figure 10 and 11 respectively.

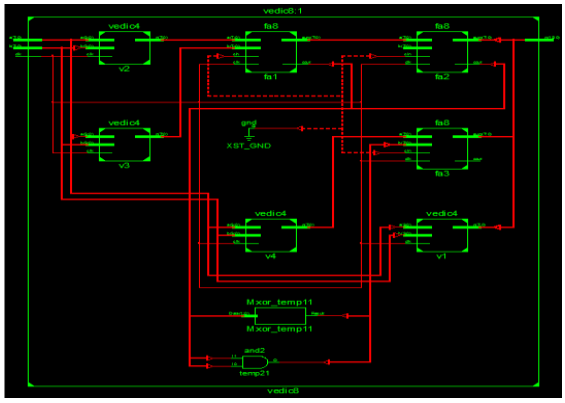

Fig.10. RTL of Proposed 8x8 Vedic multiplier

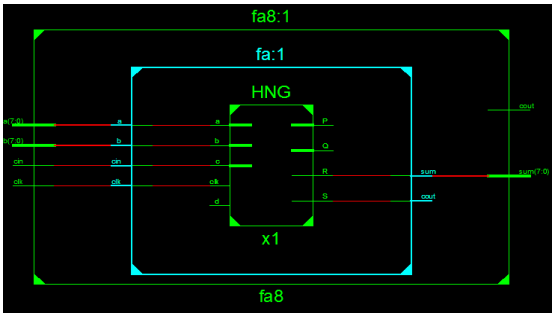

Fig.11. RTL of Proposed 8-bit RCA.

RTL (Resister Transfer Level) description describes a circuit's registers and the sequence of transfers between these registers but does not tell about the hardware used to carry out these operations. It is use to determine the size and number of registers used.

VI. RESULTS AND DISCUSSIONS

All the blocks are modeled using Verilog HDL. The simulation results of the proposed design are verified using Xilinx ISE ISim. This achieves functional verification of the conceptual design which enables the developer to synthesize ('compile') their designs, perform timing analysis.

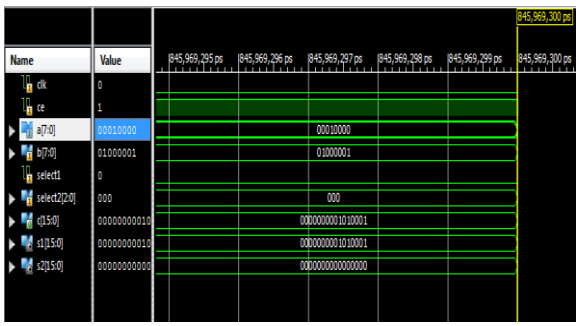

Fig.12. Simulation result of 8-bit RCA.

Time delay and power comparisons between proposed 8-bit reversible, non reversible and [8] adders were observed and compared and tabulated in Table 1.

Table 1. Time and Power Comparisons of proposed logic.

Parameters	**Irreversible RCA**	**Ref. [8]**	**Proposed Reversible RCA**
Time Delay (ns)	11.2 ns	7.88 ns	7.4 ns
Power (mw)	0.047	0.0114	0.0102

The above observations shows that the proposed reversible ripple carry adder is time and power efficient than irreversible logics and the design proposed in [8].

Fig.13. Simulation Result of 8x8 Vedic Multiplier

Comparison between 8-bit Reversible Vedic multiplier with the conventional multiplier (Booth) and reversible multiplier [8] in terms of parameters like time delay, power consume and area utilized are shown in the table 2.

Table 2. Comparison of Multiplier designs.

Parameters	Conv. Booth Multiplier	Ref [8]	Proposed Multiplier
Time Delay	27.72ns	21.44ns	20.249ns
Power (mw)	0.430mw	0.299mw	0.278mw
Area (no. slice LUTs.)	171	--	108

The proposed 8-bit reversible multiplier is more efficient and optimized than the conventional 8-bit booth multiplier and design proposed in [8].

The power dissipation, speed and the area utilization in terms of LUT is improved by 35.35%, 26.94% and 36.8% respectively with respect to conventional booth multiplier. Also proposed design has 5.5% power and 7% speed improvement over design [8]. The improvement in power dissipation is achieved by the 3*3 reversible gates, which are the fundamental blocks of the proposed design but in [8], Viswanath and Ponni utilized 4*4 gate (TSG).

The proposed Low power Reversible Vedic multiplier and conventional booth structure are implemented using VHDL programming language, simulated and synthesized using Xilinx ISE 14.5 and get implemented using Spartan xc6slx45-2csg324 FPGA kit.

VII. CONCLUSION

This paper presents the Urdhva Tiryakbhayam Vedic Multiplier realized using reversible logic gates. First a basic 2x2 UT multiplier is designed and implemented using PG and TG reversible gates. And this 2x2 UT multiplier block is cascaded to obtain 4x4 multiplier with the ripple carry adders which were required for adding the partial products were constructed using HNG gates and this 4x4 is used to construct proposed 8x8 Vedic multiplier design with 8-bit reversible ripple carry adder using HNG gate to add the partial product in single step.

The fast, low power and area efficient reversible logic based adder and Vedic multipliers with lower hardware complexity are integrated and resulted that the power dissipation and speed of operations of proposed design is reduced when compared with the other design. Less number of adders in the Vedic multiplier reduces the area and power dissipation and increases the operation speed. The proposed logic are implemented using Verilog HDL programming language, simulated and synthesized using Xilinx ISE 14.5i software. The synthesized output resulted that the proposed technique consumes approx the 35% of less power, area of 36% less and the 26% of higher performance compared to conventional circuit and 5% of less power and 7% speed over [8].

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