Energy Efficient High Port Count Optical Switches

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To my loving parents

To my Cambridge era

Declaration

I hereby declare that this dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration except as declared in the Preface and specified in the text.

It is not substantially the same as any that I have submitted, or, is being concurrently submitted for a degree or diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text. I further state that no substantial part of my dissertation has already been submitted, or, is being concurrently submitted for any such degree, diploma or other qualification at the University of Cambridge or any other University or similar institution except as declared in the Preface and specified in the text.

This dissertation contains less than 65,000 words including appendices, bibliography, footnotes, tables and equations and has less than 150 figures.

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Abstract

The advance of internet applications, such as video streaming, big data and cloud computing, is reshaping the telecommunication and internet industries. Bandwidth demands in datacentres have been boosted by these emerging data-hungry internet applications. Regarding inter- and intra-datacentre communications, fine-grained data need to be exchanged across a large shared memory space.

Large-scale high-speed optical switches tend to use a rearrangeably non-blocking architecture as this limits the number of switching elements required. However, this comes at the expense of requiring more sophisticated route selection within the switch and also some forms of time-slotted protocols. The looping algorithm is the classical routing algorithm to set up paths in rearrangeably non-blocking switches. It was born in the electronic switch era, where all links in the switches are equal. It is, therefore, not able to accommodate loss difference between optical paths due to the different length of waveguides and distinct numbers of crossings, and bends, leading to sub-optimal performance.

We, therefore, propose an advanced path-selection algorithm based on the looping algorithm that minimises the path-dependent loss. It explores all possible set-ups for a given connection assignment and selects the optimal one. It guarantees that no individual path would have a sufficiently substantial loss, therefore, improve the overall performance of the switch. The performance of the proposed algorithm has been assessed by modelling switches using the VPI simulator. An 8×8 Clos-tree switch demonstrates a 2.7dB decrease in loss and 1.9dB improvement in IPDR with 1.5 dB penalty for the worst case. An 8×8 dilated Beneš shows more than 4 dB loss reduction for the lossiest path and 1.4 dB IPDR improvement for 1 dB power penalty. The improved algorithm can be run once for each switch design and store its output in a compact lookup table, enabling rapid switch reconfiguration.

Microelectromechanical systems (MEMS) based optical switches have been fabricated with over 1,000 ports which meet the port count requirements in data centre networks. However, the reconfiguration speed of the MEMS switches is limited to the millisecond to microsecond timescale, which is not sufficient for packet switching in datacentres. Opto-electronic devices, such as Mach-Zehnder Interferometers (MZIs) and semiconductor optical amplifiers (SOAs)

with nanosecond response time show the potential to fulfil the requirements of packet switching. However, the scalability of MZI switches is inherently limited by insertion loss and accumulated crosstalk, while the scalability of SOA switches is restricted by accumulated noise and distortion.

We, therefore, have proposed a dilated Beneš hybrid MZI-SOA design, where MZIs are implemented as 1×2 or 2×1 low-loss switching elements, minimising crosstalk by using a single input, and where short SOAs are included as gain or absorption units, offering either loss compensation or crosstalk suppression though adding only minimal noise and distortion. A 4×4 device has been fabricated and exhibits a mere 1.3dB loss, an extinction ratio of 47dB, and more than 13dB IPDR for a 0.5dB power penalty. When operating with 10 Gb/s per port, 6pJ/bit energy consumption is demonstrated, delivering 20% reduced energy consumption compared with SOA-based switches. The tolerance of the current control accuracy of this switch is very broad. Within a 5 mA bias current range, the power penalty can be maintained below 0.2 dB for 8 dB IPDR and 12 mA for 10 dB IPDR with a penalty less 0.5 dB. The excellent crosstalk and power penalty performance demonstrated by this chip enable the scalability of this hybrid approach. The performance of 16×16 port dilated Beneš hybrid switch is experimentally assessed by cascading 4×4 switch chips, demonstrating an IPDR of 15 dB at a 1 dB penalty with a 0.6 dB power penalty floor. In terms of switches with port count larger than 16×16, the power penalty performance has been analysed with physical layer simulations fitted with state-of-the-art data. We assess the feasibility of three potential topologies, with different architectural optimisations: dilated Beneš, Beneš and Clos-Beneš. Quantitative analysis for switches with up to 2048 ports is presented, achieving a 1.15dB penalty for a BER of 10^{-3}, compatible with soft-decision forward error correction.

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List of Abbreviations

ASE	Amplifier Spontaneous Emission
AWG	Array Wave Grading
BER	Bit Error Rate
CW	Continuous Wave
EDFA	Erbium-Doped Fibre Amplifier
InP	Indium phosphide
IPDR	Input Power Dynamic Range
MEMS	Micro-Electro-Mechanical System
MZI	Mach-Zehnder Interferometer
MMI	Multi-Mode Interference
MQW	Multi Quantum Well
NRZ	Non-Return to Zero
OEO	Optical-Electrical-Optical
OSNR	Optical Signal to Noise Ratio
PD	Photodiode
PC	Polarisation Controller
PRBS	Pseudo-Random Bit Sequences
QCSE	Quantum Confined Stark Effect
QD	Quantum Dot
QW	Quantum Well
SNR	Signal to Noise Ratio
SOA	Semiconductor Optical Amplifier
TE	Traverse electric
TM	Traverse Magnetic
VOA	Variable Optical Attenuator
WDM	Wavelength Division Multiplexing

List of Publications

1. **M. Ding**, A. Wonfor, R. V. Penty, I. H. White, “Advanced Path-Selection Algorithm for Rearrangeably Non-Blocking Integrated Optical Switches” in IEEE/OSA Journal of Optical Communications and Networking (in submission)
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3. I. White, **M. Ding**, A. Wonfor, Q. Cheng, and R. Penty, "High Port Court Switch Architectures for Data Center Applications," in Advanced Photonics 2017 (IPR, NOMA, Sensors, Networks, SPPCom, PS), OSA Technical Digest (online) (Optical Society of America, 2017), paper NeW1B.2.
4. R. V. Penty, **M. Ding**, A. Wonfor, and I. H. White, "Scaling of Low Energy InP SOA Based Switches," in Advanced Photonics 2017 (IPR, NOMA, Sensors, Networks, SPPCom, PS), OSA Technical Digest (online) (Optical Society of America, 2017), paper PM4D.3.
5. **M. Ding**, A. Wonfor, Q. Cheng, R. V. Penty, and I. H. White, "Scalable, Low-Power-Penalty Nanosecond Reconfigurable Hybrid Optical Switches for Data Centre Networks," in Conference on Lasers and Electro-Optics, OSA Technical Digest (online) (Optical Society of America, 2017), paper JW2A.135.
6. **M. Ding**, A. Wonfor, Q. Cheng, R. V. Penty, I. H. White, "Dilated 4×4 Hybrid MZI-SOA Switch with Relaxed Active Bias Control" European Conference on Integrated Optics (ECIO), Eindhoven, Netherland, 2017, paper T4.3.
7. **M. Ding**, A. Wonfor, Q. Cheng, R. V. Penty and I. H. White, "Emulation of a 16×16 optical switch using cascaded 4×4 dilated hybrid MZI-SOA optical switches," 2017 Optical Fiber Communications Conference and Exhibition (OFC), Los Angeles, CA, 2017, pp. 1-3.

8. S. Zhu, A. Wonfor, A. Quarterman, N. Bamiedakis, **M. Ding**, R. V. Penty, I. H. White, “Unidirectional Operation of a Monolithically Integrated Mode locked Semiconductor Ring Laser” European Conference on Integrated Optics (ECIO), Warsaw, Poland, 2016, paper o-42.
9. **M. Ding**, A. Wonfor, Q. Cheng, N. Bamiedakis, R. V. Penty, I. H. White, “Low-Energy, Dilated 4x4 Hybrid MZI-SOA Cross-point Optical Switch”, European Conference on Integrated Optics (ECIO), Warsaw, Poland, 2016, paper o-39.
10. Q. Cheng, **M. Ding**, A. Wonfor, J. Wei, R.V. Penty, I.H. White, The feasibility of building a 64 × 64 port count SOA-based optical switch, in Proc. Photonics in Switching 2015, Florence, Italy (2015), pp. 199–201.
11. I. H. White, **M. Ding**, Q. Cheng, A. Wonfor and R. V. Penty, "Advanced photonic routing sub-systems with efficient routing control," 2015 17th International Conference on Transparent Optical Networks (ICTON), Budapest, 2015, paper Tu.A3.1.
12. **M. Ding**, Q. Cheng, A. Wonfor, R. V. Penty, I. H. White, “Routing Algorithm to Optimise Path-Dependent Loss for Rearrangeably Non-Blocking Integrated Optical Switches”, Semiconductor and Integrated OptoElectronics (SIOE), Cardiff, Wales, UK, 2015
13. **M. Ding**, Q. Cheng, A. Wonfor, R. Penty, and I. White, "Routing Algorithm to Optimize Loss and IPDR for Rearrangeably Non-Blocking Integrated Optical Switches," in CLEO: 2015, OSA Technical Digest (online) (Optical Society of America, 2015), paper JTh2A.60.

Chapter 1 Introduction

1.1 Optical Communications

The ever-increasing network traffic driven by fast-growing video streaming, file sharing and cloud computing and big-data applications requires networks with a higher and higher transmission bandwidth [1]. It was forecasted by Cisco [2] that the total internet traffic would reach 278 Exabytes per month in 2018 (Figure 1.1) with a compound annual growth rate (CAGR) of 24 percent from 2016 to 2021.

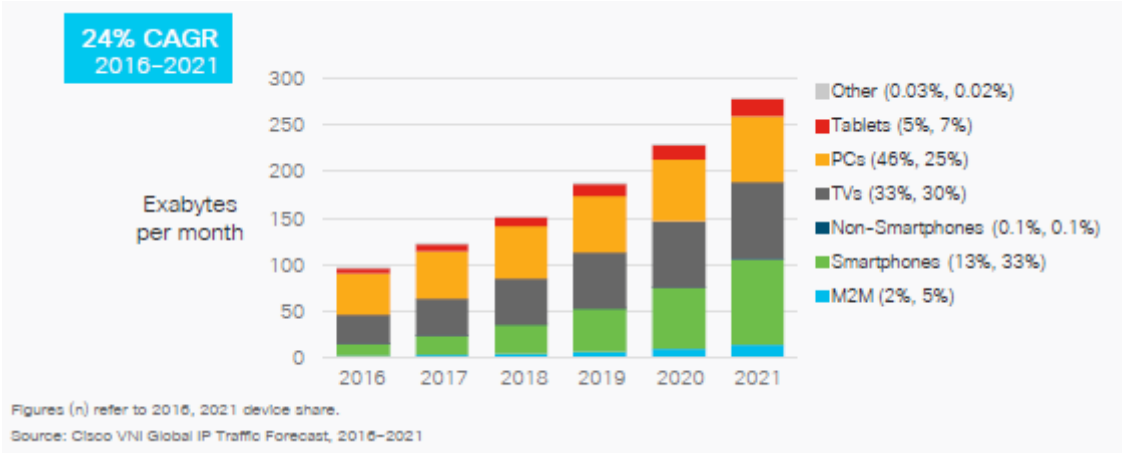

Figure 1.1– Global IP traffic growth in exabytes per month [2]

Optical communication has demonstrated the outstanding capability and is believed to be an attractive solution to the explosive growth of internet traffic.

- Low transmission loss of optical fibres (lower than 0.2dB/km at wavelengths around 1550nm)
- Near-zero distortion
- Small size
- Immune to electromagnetic waves

- More than THz bandwidth with Wavelength Division Multiplexing

1.2 Photonic Switches

With the development of optical communication technologies, the communication networks evolve from simple point-to-point links to much complicated optical networks with crossovers. In optical networks, the signals at each node should be able to be routed and delivered to any other nodes [3]. For instance, if a node at one access network needs to deliver a message to a node in another access network (Figure 1.2), the devices at the intersection between Access/Aggregation networks can route date from any input port to the desired output port. These devices are called switches.

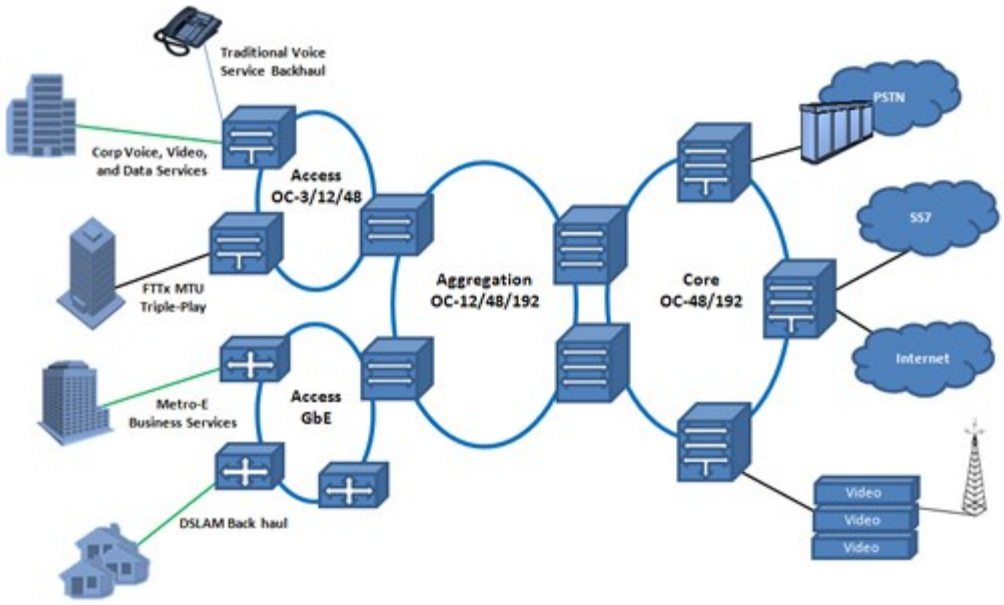

Figure 1.2– Network topology [4]

The majority of signal switching within optical networks is realised by converting signals from the optical domain to the electrical domain and using electronic switches to do the data routing. However, there is a growing issue for electronics switches. Since the data rate of electronic transceivers is currently limited to around 40Gb/s [5], it is far less than the capacity of optical links (more than 10Tb/s). Hence, high-date-rate optical links usually include tens to hundreds of wavelength channels in order to reach a high aggregated data rate. Each channel, however,

requires its own Optical/Electrical (O/E) and Electrical/Optical (E/O) conversion devices. A large amount of O/E and E/O devices are required for the signal switching. Moreover, electronic devices are usually designed with data-rate limits, the upgrade of the system requires the replacement of the most of the electronic devices, rising the overall cost. Additionally, as electronic switches route signals at the bit level, they result in high-energy consumption. Nowadays, the internet consumes about 1% to 1.9% of the total electrical power consumption around the world [6] with more than 10% of it is from routers and switches [7]. This number is continuously growing with the soaring access rate. Routers and switches are predicted to be the majority energy consumption elements in the internet after 2020 [7][8] [7].

Therefore, energy-efficient switches are in demand for future optical networks. Data switching in the optical domain, without the need of O/E conversion, has attracted much attention due to its characteristics [9]:

- It is data-rate independent, which switches signals at packet and flow level regardless of date rates.
- No O/E and E/O conversion devices are required, reduce the energy consumption.

The implementation of the optical switches is able to extend the reach of the tremendous bandwidth from the optical fibre links to the network switching nodes. The optical end-to-end bandwidth can then enable the wavelength based services and applications. Optical switching is regarded as a key enabling component for the future communication systems [10]. However, there are still challenges to design reliable large-scale fast-reconfiguration optical switches. This thesis is to explore the methods to design and implement the high-port-count low-energy-consumption optical switches.

1.3 Thesis Scope

Bandwidth demands in datacentres are doubling every 12-15 months owing to the recent massive development of cloud computing [11]. Current data centre networks use electronic packet routers and optical transceivers to interconnect servers with a multi-stage folded Clos architecture [12]. The cost, energy consumption and cabling complexity increase significantly

with an increasing number of nodes in the network. Optical switches have the potential to replace the electronic switches and some optical transceivers currently used in this approach and meet the size and bandwidth demands of future data centre networks. The data centre networks in production today connect 100,000 servers [12]. Connecting all servers with a monolithic switch able to respond on nanosecond timescales is currently impractical, but using optical switches to connect electronically-aggregated racks can dramatically reduce the cost and complexity of the networks. Given 50 servers per rack, 2,000 port switches would be required to connect 100,000 servers in a data centre. As small messages are exchanged across a large shared memory space in data centres, nanosecond response time is required to fulfill the requirements of packet switching.

This thesis studies the feasible approach to implement optical switches in data centres. To fulfill the requirment for intra- and inter-datacentre communications, suitable optical switching technologies should feature high port court, nanosecond response times, low power consumption, low noise-figures, low crosstalk and low loss [13] with adaptive control scheme.

Chapter 2 studies a range of optical switching technologies: such as MEMS, thermo-optics, liquid crystal, acousto-optics, electro-optics and semiconductor optical amplifiers (SOAs). Some of them are mature technologies with commercialised products which have been implemented in optical networks. Among these optical switching technologies, semiconductor optical amplifiers (SOAs) and Mach Zehnder Interferometers (MZIs) demonstrates nanosecond timescale reconfiguration time, which is essential for intra- and inter-datacentre communications. The fundamental knowledge of SOAs and MZIs are, therefore, studied. Operation principles, carrier density, heterostructure and quantum-well structure of SOAs are explained. The construction and matrix equations of MZIs are also discussed.

Chapter 3 reviews switch architectures and routing algorithms. A number of notations are used to describe input/output ports, sub-switches, stages, and connection assignments. The common notations of switching networks are explained at the beginning of the chapter. Large optical switches are constructed by connecting 2×2 basic switch elements with various network architectures. There are trade-offs between different architectures in terms of the total number of building blocks and the blocking characteristic. Multi-stage architectures require routing

algorithms to select the middle-stage sub-networks to set up paths for the given connection assignments. The looping algorithm is the classical routing algorithm which has been proposed for Base 2 switches. It is also extended to all Beneš, Clos and dilated Beneš architectures.

Chapter 4 proposes an advanced path-selection algorithm. As the looping algorithm might lead to paths with the unnecessarily large loss, the advance path-selection algorithm explores all possible set-ups for a given connection assignment and selects the optimal one. It guarantees that no individual path would have a sufficiently considerable loss, therefore, improve the overall performance of the switch. The advanced routing algorithm has also been extended to all Beneš, Clos and dilated Beneš architectures.

Chapter 5 investigates a hybrid optical switch design approach, which includes MZIs as the switching elements and short (and hence low power) SOA elements as both gain and absorption elements to enable both loss compensation and crosstalk suppression. The dilated Beneš scheme is adopted to suppress the crosstalk further. A 4×4 switch with this hybrid design approach has been fabricated using a generic foundry, demonstrating -47dB crosstalk ratio and a 14dB input power dynamic range (IPDR) for a penalty less than 0.5dB. When operating with 10 Gb/s per port, 6pJ/bit energy consumption is demonstrated, delivering 20% reduced energy consumption compared with SOA-based switches. The tolerance of the current control accuracy of this switch is very broad. Within a 5 mA bias current range, the power penalty can be maintained below 0.2 dB for 8 dB IPDR and 12 mA for 10 dB IPDR with a penalty less 0.5 dB.

Chapter 6 further studies the scalability of the hybrid switch. The performance of a dilated Beneš 16×16 port dilated hybrid switch is experimentally assessed by cascading 4×4 switch chips, with an IPDR of 15 dB at a 1 dB penalty with a 0.6 dB power penalty floor being demonstrated. In terms of switches with a port count larger than 16×16, the power penalty performance can be simulated with physical layer simulations fitted using experimental data. A few topologies with hybrid MZI-SOA building blocks have the potential to build low-power-penalty large-port-count switches. We assess the feasibility of three potential topologies, with different architectural optimisations: dilated Beneš, Beneš and Clos-Beneš. Quantitative

analysis for switches with up to 2048 ports is presented, achieving a 1.15dB penalty for a BER of 10^{-3}, compatible with soft-decision forward error correction.

Chapter 7 summarises the advanced-algorithm and hybrid-design approaches to improve the performance of large-scale integrated switches. The outlook for the future work including the feedback loop to control MZI bias, the four hierarchical control layer and quantum secure router are discussed in the end.

1.4 Novel Contributions

The main contributions of this thesis are listed below:

- An advanced path-selection algorithm is proposed and evaluated using physical layer simulations. It guarantees that no individual path would have a sufficiently considerable loss, therefore, improve the overall performance of the switch.
- For the first time, a monolithically integrated lossless active active-passive 4×4 switch with hybrid MZI-SOA building components is demonstrated. A wide IPDR of 14 dB with penalties less than 0.5 dB is achieved.
- The control current tolerance of the hybrid switch is demonstrated. Within a 5 mA bias current range, the power penalty can be maintained below 0.2 dB for 8 dB IPDR
- A 16×16 hybrid MZI-SOA switch is emulated by cascading two 4×4 chips. A wide IPDR of 15 dB at a 1 dB penalty with a 0.6 dB power penalty floor is demonstrated.
- The quantitative analysis for switches with up to 2048 ports is presented using physical layer simulations fitted using experimental data. For the first time, a Clos-Beneš MZI-SOA based switch with a hybrid fibre-integration approach achieves a record 2048 port count with 1.15 dB.

Chapter 2 Optical Switching Technologies

2.1 Introduction

There are a variety of optical switching technologies available and attracting much attention. Some of them are mature technologies with commercialised products which have been implemented in optical add-drop multiplexers (OADM) and protection networks. The technologies are discussed in Section 2.2.

Among optical switching technologies, semiconductor optical amplifiers (SOAs) and Mach Zehnder Interferometers (MZIs) demonstrate nanosecond timescale reconfiguration time. The fast reconfiguration time is important for latency-sensitive-data exchange within data centres. These two technologies, therefore, are believed to be key enabling technologies for future inter- and intra-datacentre networks. They are implemented in the switch designs included in this thesis. The fundamental theory of SOAs and MZIs are discussed in Section 2.3 and Section 2.4, respectively.

2.2 Optical Switching Technologies

A few optical switching technologies have been widely studied. In this section, the performance of the switching technologies listed below is discussed and compared. The key optical switching characteristics, such as reconfiguration time, insertion loss, distortion and crosstalk are analysed.

- Micro-Electro-Mechanical System Switches
- Thermo-Optic Switches
- Acousto-Optic Switches
- Liquid Crystal Switches

- Electro-Optic Switch
- Semiconductor Optical Amplifiers (SOAs)

2.2.1 Microelectro-Mechanical Systems (MEMS) Switches

MEMS devices are mechanically integrated circuits which utilise tiny reflective surfaces to redirect the input light beams to the assigned output ports or the other corresponding reflective surface [14]. MEMS switching technologies are classified into two categories: two-dimensional (2-D) MEMS and three-dimensional (3-D) MEMS.

Figure 2.1a shows the top view of a 2-D MEMS device. The microscopic mirrors make a 45˚ angle to the input light beam in order to redirect the light to output ports at the bottom. The switching functionality is obtained by changing the position of the mirrors:

- When a mirror is activated to the up position, it moves into the path of a beam and redirects the input beam to one of the output ports.
- When all the mirrors below the path of a beam stay in the down position, the light passes through the switch matrix and is dropped.

This mirror matrix is arranged in a crossbar configuration to achieve non-blocking cross-connection [15]. The switch blocking characteristic is explained in details in Chapter 3. The trade-off for the simple control method of the crossbar layout is the large optical loss and low scalability. As the number of ports increases, the optical path length also grows which leads to a larger amount of optical loss. Meanwhile, the number of mirrors required grows dramatically, increasing the cost and complexity of fabrication.

In contrast, the 3-D MEMS technology needs fewer mirrors for large-port-count switches. As shown in Figure 2.1b, each input/output port has its dedicated mirror which is able to tilt freely about two axes [16]. An optical path between an input port and an output port is established by tilting the corresponding mirrors simultaneously. A switch with over 1000 ports has been realized with 3-D MEMS [17].

A drawback of the 3-D MEMS technology is that the angle and position of each mirror need to be placed accurately. Otherwise, a huge amount of loss and crosstalk occur. The switch,

therefore, is vulnerable to external disturbance or drift. A feedback control system can be implemented to adjust the mirrors. It, however, increases the cost and complexity of the system.

The switching functionality of MEMS switches is achieved by moving the mirrors. The beam-steering technology limits its response time to the order of 10 milliseconds. Recently, the reconfiguration speed of modest port count MEMS-based switches has been improved to the sub-microsecond level by adopting Silicon photonics [18]. This had a compact 7×7 mm^2 footprint for a 64×64 port count and also has achieved better than -65 dB extinction ratio.

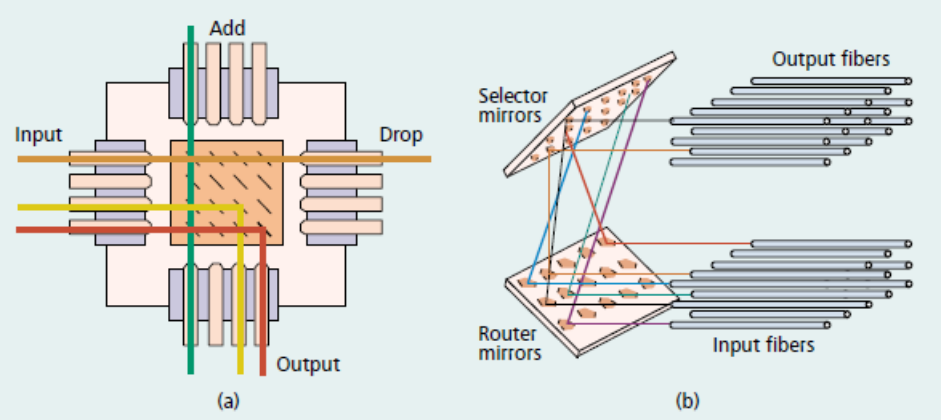

Figure 2.1 a) 2-D MEMS technology b) 3-D MEMS technology [19]

2.2.2 Thermo-optic Switches

Thermo-optical switches utilise the temperature-sensitive optical characteristic of certain materials to tune the optical signal. The typical thermo-optic switches are based on Mach-Zehnder interferometers (MZI) [20]. The details of MZI theory is discussed in Section 2.4.

Figure 2.2 shows the structure of a thermo-optical MZI. It is capable of switching signals between two inputs and two outputs. Two 3dB couplers are included in it to split input signals and merge output signals. Two arms of it have the same length. The refractive index of the arm material varies with the temperature [21]. Heating one arm of the interferometer will change its refractive index which leads to a phase difference between the two arms. Consequently, the interference can be made constructive or destructive by controlling the temperature between the two arms. Therefore, the output power ratio between the two output ports is varied.

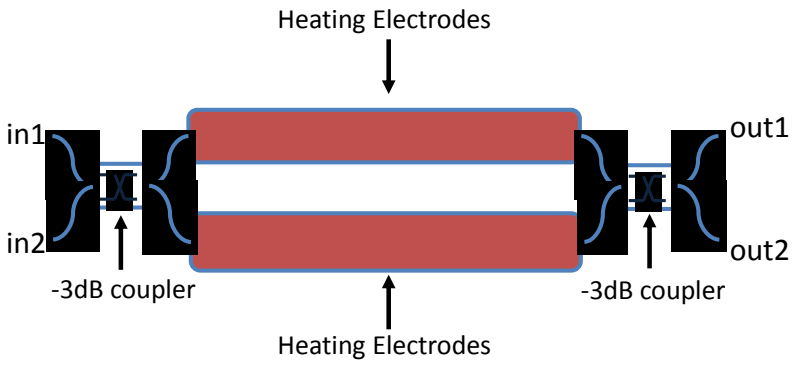

Figure 2.2 2x2 thermal-optic MZI switch schematic [22]

One of the drawbacks of the thermo-optic MZI switch is the high-energy consumption caused by the power-hungry temperature controller. Additionally, as it based on MZI, it has the issues caused by the MZI structure. It is difficult to make the 3 dB coupler exactly balanced, and the lengths of two arms may be mismatched. These lead to crosstalk between two output ports, degrading the optical performance.

Thermo-optic switches can also be based on Micro-ring Resonators as shown in Figure 2.3. The ring resonator is a closed loop coupled to input and output waveguides. Light with certain wavelengths can build up intensity over multiple round trips due to constructive interference. The only light at the resonant wavelength coming from the input waveguide passes through the ring and reaches the output waveguide, other waveguides are reflected. The ring resonator thus functions as a filter here. The resonant wavelength can be adjusted by changing the refractive index of the ring waveguide, which is realised by varying the temperature. The switching function is, therefore, achievable by tuning the temperature:

- Light at the resonant wavelength enters from the in1. Without tuning the resonant wavelength in the ring waveguides, the injection light is coupled into the upper ring and exits from the out1.
- With temperature adjustment, the resonator wavelength is shifted away from the signal's carrier wavelength. The light, therefore, propagates through the waveguide and exits at out2.

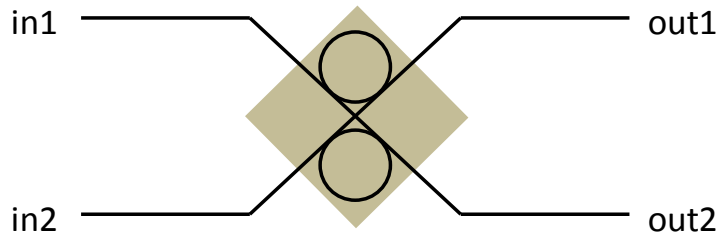

Figure 2.3 2x2 Thermal-optic micro-ring resonator switch schematic [23]

Single-order micro-ring resonators are vulnerable to wavelength variation and fabrication mismatch. Higher-order resonators improve the operating bandwidth, improving tolerance to fabrication variations. More complex wavelength locking loops, however, are required.

2.2.3 Acousto-optic Switches

Acousto-optical switches utilise the interaction between sound and light (called the acousto-optic effect) to tune optical signals. Figure 2.4 shows a schematic of a 2×2 acousto-optic switch. It is composed of two polarization beam splitter and two parallel waveguides.

When a surface acoustic wave is created and travels in the same direction as the optical signal in the waveguides, it forms the equivalent of a moving grating due to the acousto-optic effect [24][25]. The equivalent of a moving grating can be phase-matched to an optical signal at certain wavelengths. In this situation, the polarisation of the phase-matched optical wave is turned 90°, either from the TM (Transverse Electric) to the TE (Transverse Magnetic) mode or vice versa. An example is shown below with an input signal from the upper port.

- The input signal is split into the TM and TE mode. With the surface acoustic wave, the polarization of the signals in two arms is rotated by 90°. Two signals then combine at the second polarization splitter and exit at the upper port.
- Without the surface acoustic wave, the polarisation of two signals is maintained. The two signals, therefore, combine at the lower port.

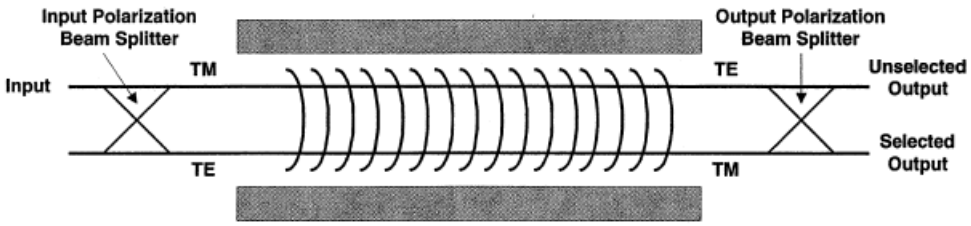

Figure 2.4 Schematic of a 2x2 acousto-optic switch [26]

The acousto-optic switch is able to switch multi-wavelength signals by applying several surface acoustic waves with different frequencies simultaneously. Acousto-optic switches, however, are not able to achieve high switching speed as it is limited by the speed of the sound wave.

2.2.4 Liquid-Crystal Switches

Liquid crystals change the polarization state of incident light when an electric field is applied to them [27]. Liquid-crystal switches utilise this characteristic to switch light between terminals. Figure 2.5 shows a schematic of a 1×2 liquid-crystal switch. It consists of birefringent plates at input/outputs, a liquid-crystal modulator and a polarization beam splitter.

As the birefringent plates have different refractive indexes along two axes, they are used to manipulate the polarization of light to desired states [28]. The liquid crystal modulator rotates the polarizations of light passed through it. The rotating degrees of light depends on the voltage applied to it. The polarization beam splitter allows the signal with certain polarization pass through it and reflects the signal with orthogonal states. The operation detail is described below.

- Without applying a voltage bias, the polarization of the input signals is not changed by the liquid-crystal modulator. The signals then pass through the polarization beam splitter and arrive at Output #1.
- With certain electrical field over the liquid crystal, the polarization of the input signals is rotated to the orthogonal states. The signal is then reflected by the polarization beam splitter and exits at Output #2.

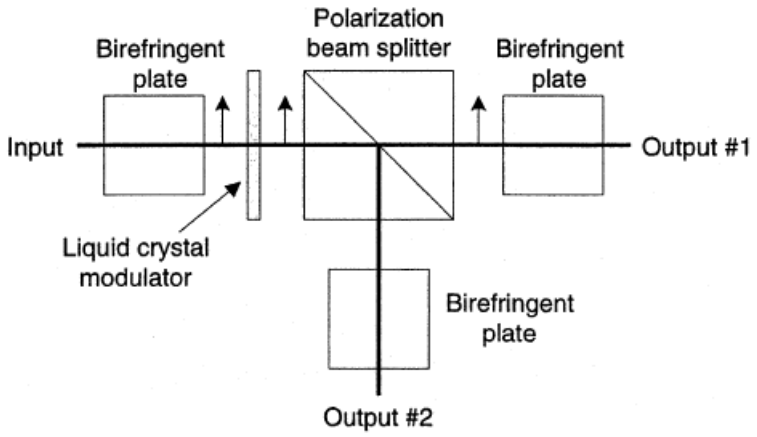

Figure 2.5 1x2 Liquid-crystal optical switch [26]

The liquid-crystal switch demonstrates reliable optical performance as there are no moving parts in the device (compared with MEMS switches). It is, however, sensitive to ambient temperature. Temperature controllers might be required, increasing the energy consumption and cost of the system.

2.2.5 Electro-Optic Switches

Both Electro-optic switches based switches utilise electrical signal to change optical properties of the material. This approach ensures the nanosecond reconfiguration time. Figure 2.6 shows an electro-optic MZI switch. Its schematic is similar to a thermo-optic MZI switch. It consists of two multi mode interferences (MMI) to split incoming signals into two arms and combine them together. The refractive index or optical absorption coefficient of the arm material can be changed by an external electric field [29] or an injection current [30]. The refractive index and optical absorption coefficient are related to each other via the Kramers-Kronig relations.

The electro-optic switching process can be triggered by a number of electro-optic effect. The Pockels effect changes or produces birefringence in the optical medium [31]. The Pockels effect is also known as the linear electro-optic effect as the birefringence is proportional to the external electric field. The response time of the change of the refractive index is below picoseconds. The switching speed of the devices based on the Pockels effect is usually limited by the RC time constant. The Pockels effect appears in semiconductor crystals which lack a centre of symmetry and dielectric substances. Lthium Niobate is the widely used material based

on Pockels effect and exhibits fast switching speed owing to its small dielectric constant [32]. The Kerr effect is also a change in the refractive index of a material in response to an applied electric field [33]. Compared with Pockels effect, in the Kerr effect, the refractive index change is proportional to the square of the field. Polar liquids, such as nitrotoluene and nitrobenzene exhibit very large Kerr constants. Glass cells filled with one of these liquids are used to modulate light. Voltages as high as 30kV might be required to achieve transparency, much higher can the operating voltage for the Pockels effect. The Franz-Keldysh effect and QCSE are used for Electro-absorption modulation. The Franz-Keldysh effect is a change in optical absorption in uniform, bulk semiconductors when an electric field is applied [34]. The QCSE requires quantum well structures. In QCSE, the increasing electric field shift the electron states to lower energies and shift the hole state to higher energies, which reduce the permitted light absorption frequencies and the refractive index changes accordingly[35].

The optical phase is then changed by the applied voltage or current. By varying the phase difference between the two arms, the signals can be combined constructively or destructively at the output MMI and here the light can be switched from on output port to the other. Similar to other switches based on the MZI structure, Electro-optic MZI switches suffer from poor crosstalk due to imperfect coupler split ratio and loss mismatch within the arms. Electro-optic MZIs are core components used to build the switches in the thesis. The theory is discussed in detail in Section 2.4.

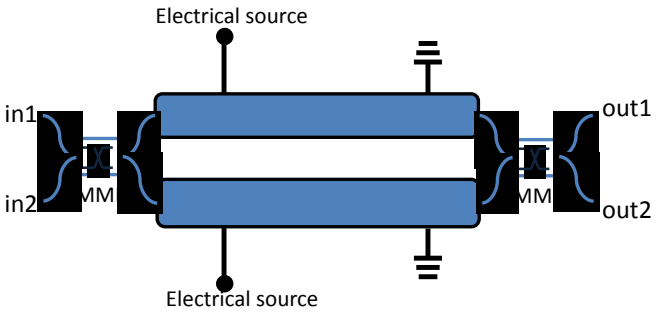

Figure 2.6 Schematic of a 2x2 electro-optic MZI switch

2.2.6 Semiconductor Optical Amplifiers

Figure 2.7 shows a schematic of a 2×2 SOA switch. The 2×2 SOA switch adopts a broadcast-and-select architecture [35]. Between every input terminal and output terminal, there is an SOA. The function of the SOA is a gate. When the SOA is pumped with current, the carrier density in it is built up to allow amplification. It compensates the loss from other passive components. If the SOA is not pumped, it absorbs the incoming light and cuts off the signal [37]. As shown in Figure 2.7, the second and third SOAs are pumped, and here the signal from first input goes to the second output and the light injected into the second input passes to the first output. SOA-based switches with larger port count can be constructed by cascading SOA gating elements [38]. Large size switches, however, suffer from accumulated amplified spontaneous emission (ASE) noise and saturation-induced distortion [39][40]. The theory is explained in Section 2.3.

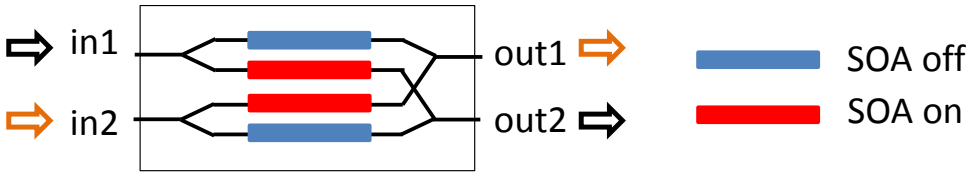

Figure 2.7 Schematic of a 2x2 SOA switch

The capability of integrated photonic circuits has demonstrated rapid advances recently. The integrated optical circuits reduced the coupling loss between components and ease the calibration. Additionally, they can be easily combined with to electric control circuits, realising small-footprint high-performance optical systems. The integrated switch with electro-optic MZI and SOA based on InGaAsP/InP or silicon foundries have attracted much attention. The switch design discussed in this thesis includes both MZIs and SOAs with an InGaAsP/InP foundry.

2.2.7 Summary of Switch Technologies

The switch technologies discussed above can be used for different applications depends on their properties. The major switch applications are listed below.

Protection Switching: In this application, switches are used to switch the signal to the backup fibre links in case the primary links are not working. Usually, 2x2 switches with millisecond transition time are used.

Optical Cross-Connects (OXCs): OXCs are the basic devices to route optical signals within optical networks or systems. Optical switches are used in OXCs to reconfigure light paths. Switch technologies with both fast and slow transition times can be used in OXCs

Optical Add-Drop Multiplexers (OAMs): OAMs are used to add or drop specific wavelength channels in the WDM signals. Wavelength sensitive switches are required in this application.

Packet Switching: In terms of inter- and intra-datacentre communications, fine-grained data need to exchange across a large shared memory space. Switches with nanosecond reconfiguration time are potential candidates for this application.

The properties and applications of each switch technologies are summarised in

Table 2.1.

Table 2.1 Summary of switch technologies

Technology	Transition Time	Scalability	Advantages	Disadvantages	Application
MEMS	0.9 μs to 10 ms [18]	≤1100×1100 [17]	Simple control method	Large-scale switches have long optical path and great number of mirrors	OXCs, OADMs
Thermo-Optic	≥90 μs [21]	≤32×32[41]	Small Size	High-energy consumption; High optical loss	OXCs, OADMs
Liquid Crystal	Milliseconds	~2×2	No moving part, reliable optical performance	Sensitive to the ambient temperature	Protection, OADMS
Acousto-Optic	~300ns[41]	~2×2	switching several different wavelengths simultaneously	Small port count	Protection
Electro-Optic	~4 ns[42]	≤32×32[43]	Low power consumption; No ASE noise	Certain level crosstalk; High insertion losses;	OXCs, OADMs Packet Switching
SOA	≥2 ns [36]	≤16×16 [40]	Gain controlled via bias current; Small size and convenient for optoelectronic integration	ASE Noise during amplification process; Gain-induced distortion	OXCs, OADMs Packet Switching

In summary, although optical switches based on MEMS, thermo-optics, liquid crystal and acousto-optics are able to route large volume of data in parallel with millisecond reconfiguration time. They are suitable for circuit switches in optical networks to deliver delay insensitive long messages.

Electro-optic switches and SOA-based switches demonstrate nanosecond reconfiguration time, which is qualified for routing packetized data with datacentres. The scalability of these switches, however, is much worse than MEMS switches. The accumulated crosstalk, insertion loss, ASE noise and distortion degrade the performance of large size switches. In this thesis, different approaches have been made to enhance the performance of these fast reconfiguration switches.

2.3 Fundamentals of Semiconductor Optical Amplifiers

2.3.1 Basic Structure and Operation Principles

SOAs operate as gating elements in optical switches. An SOA can be seen as a laser diode with suppressed residual facet reflectivity [44][45]. Figure 2.8 shows a schematic of an SOA.

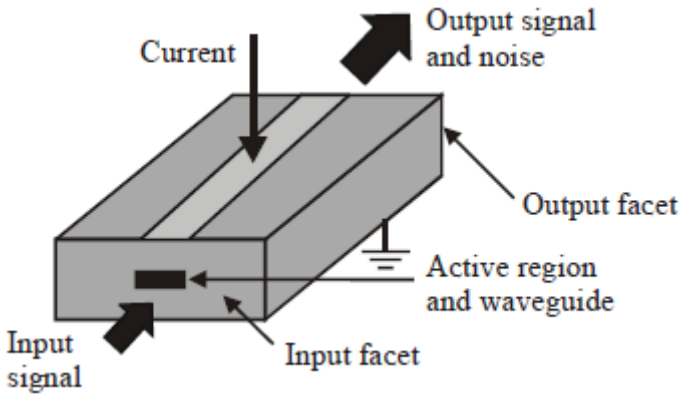

Figure 2.8 Schematic diagram of an SOA [46]

SOAs are built from III-V group semiconductor materials. The band gap of the active region is smaller than that of the surrounded regions. When a current is injected into the SOA, the input optical signal is amplified within the active region by stimulated emission (Figure 2.9).

However, at the same time, a certain number of electrons move from the conduction band to the valence band spontaneously and emit photons (spontaneous emission). This spontaneous emission is not correlated with the input signal but is added to the output signal as noise. The noise occurring within the amplification process is amplified spontaneous emission (ASE). When the probability of stimulated emission is greater than stimulated absorption, the SOA offers optical gain. To build up the probability of stimulated emission, more carriers need to be in the conduction band than the valence band (population inversion) [48].

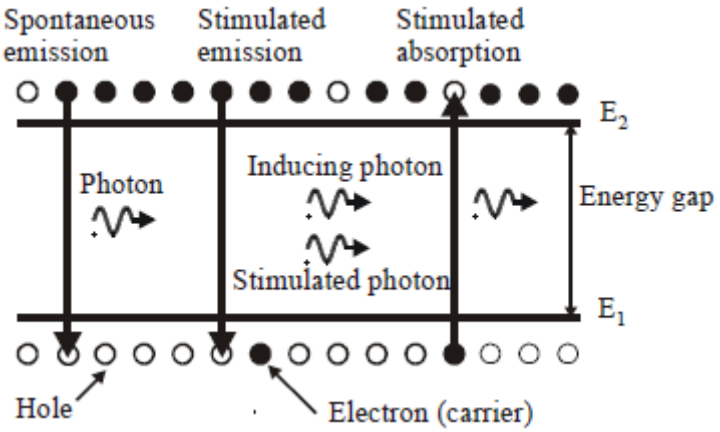

Figure 2.9 Spontaneous and simulated processes in a two-level systems [46]

The optical properties of SOAs are strongly determined by the active region carrier concentration. The theory behind the carrier density is first discussed in the following section. The structure of the heterojunctions making up the SOA is then explained. SOAs usually adopt a quantum-well structure to reduce the noise and increase the gain and saturation power. The quantum-well theory is also included in the next section. The carrier population in the active region of SOAs can be modelled by the equations and are also described. The noise-induced distortion and amplifier noise analysis are put in the appendix.

2.3.2 Carrier Density

The carrier density in the active region is determined by two properties of the semiconductor material, the probability of electrons at energy states and the density of the states.

Electrons are fermions (which have half-integer spin) and governed by the Pauli Exclusion Principle that no two fermions can co-exist in an identical energy state. The probability that an energy state is occupied by an electron at a given temperature is determined by the Fermi function f(E), Equation (2.1).

$$f(E) = \frac{1}{e^{\frac{E-E_F}{kT}} - 1} \tag{2.1}$$

Where E is the given energy level, k is Boltzmann's constant, T is the absolute temperature, and E_f is the Fermi level. kT is often known as the thermal energy and takes a value of 0.026 eV at 300K [47].

Fermi level is the term used to describe the top of the collection of occupied electron energy levels at 0k, absolute zero temperature. Therefore, at 0K, all the occupied energy states are below the Fermi level. As shown in Figure 2.10, for intrinsic semiconductors, the Fermi level is halfway between the valence and conduction bands. In doped semiconductors, the Fermi level is shifted by the doping impurities. In n-type material, the Fermi level is near the top the band gap so the electrons can be easily excited into the conduction band at a higher temperature. By contrast, in p-type material, the Fermi level is near the bottom of the band gap, allowing the excitation of holes into the valence band at a higher temperature.

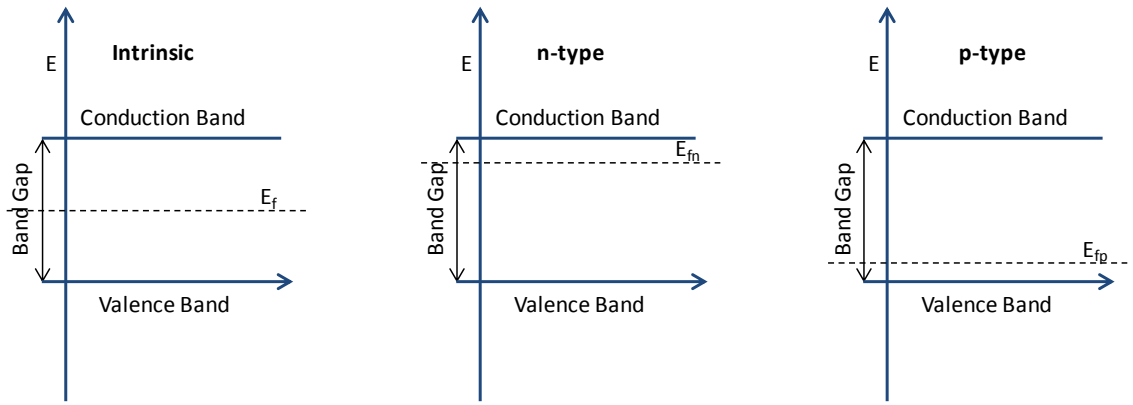

Figure 2.10 Fermi level for intrinsic, doped n-type and doped p-type semiconductor

The probability of electrons at an energy state, f(E), is also determined by the temperature. With a higher temperature, some of the energy states above the Fermi level are available to

electrons. With sufficient temperature, a fraction of the electrons can reach the conduction band. The probability of occupancy of energy levels by electrons, called Fermi-Dirac distribution of an intrinsic material at different temperatures is shown in Figure 2.11.

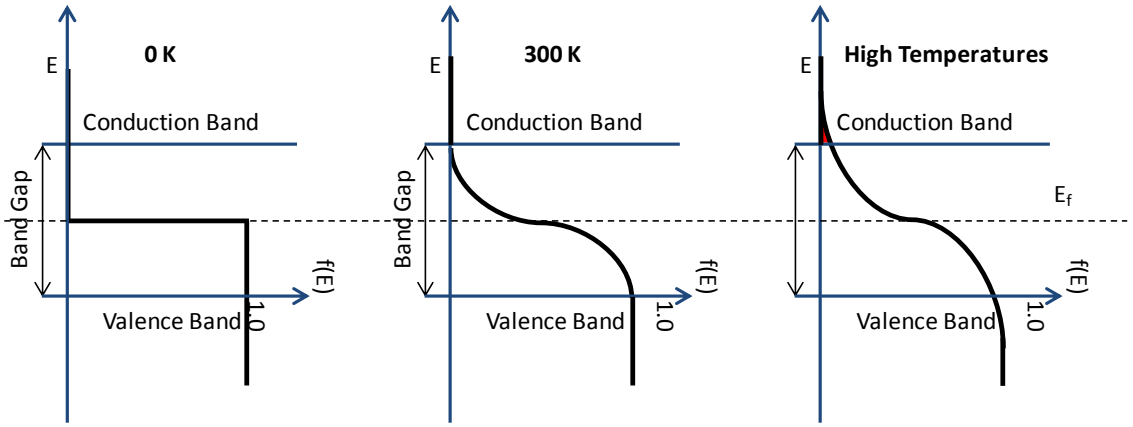

Figure 2.11 Fermi Dirac distribution of electrons at different temperatures

To calculate the number of electrons in the conduction band, the number of available energy states is also required in addition to the probability of electrons in the energy states. In bulk materials, the density of states is given by Equation (2.2)[48].

$$\rho(E) = \frac{8\sqrt{2}\pi m^{3/2}}{h^3}\sqrt{E - E_C} \tag{2.2}$$

where h is the Planck constant, m is the effective mass of an electron in the conduction band, E_C is the energy level at the border between band gap and conduction band [48].

The population of conduction band then can be calculated from the density of the states and the probability of occupation of the states as shown in Equation (2.3).

$$n(E) = f(E)\rho(E) = \frac{1}{e^{\frac{E-E_F}{kT}} - 1}\frac{8\sqrt{2}\pi m^{3/2}}{h^3}\sqrt{E - E_C} \tag{2.3}$$

Figure 2.12 shows the way that electron population of conduction band is calculated from the probability of occupation of the states and the density of the states. The orange shadowing is the probability of occupation of states, while the grey shadowing is the number of available

energy states. The actual population is then calculated by timing two above terms, which is shown as the red shadowing in the end.

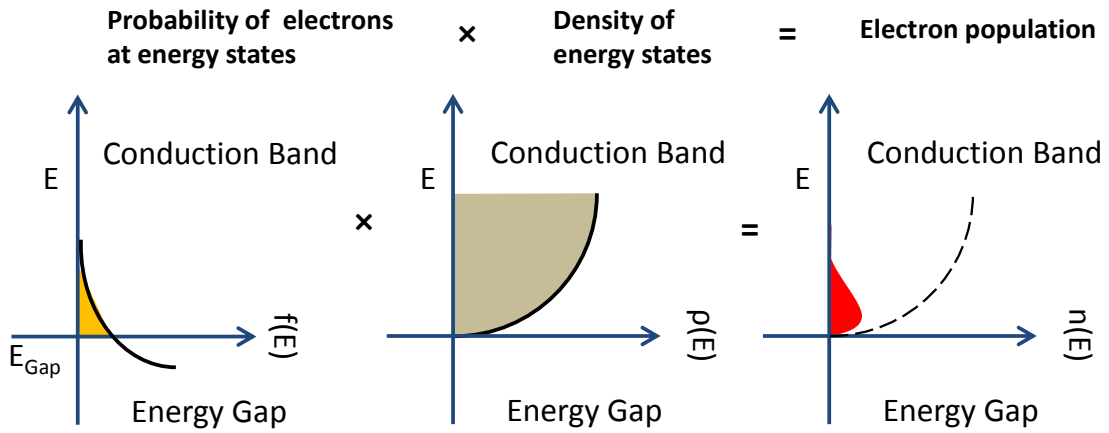

Figure 2.12 Calculating the electron population from the probability of occupation of the states and the density of energy states

2.3.3 Double Heterostructure

Doping semiconductor materials can shift the Fermi level towards either conduction band or valence band. In order to design a laser diode or SOA, the p-n junction must be heavily doped. In this case, the Fermi level of the n-type region lies in the conduction band whereas the Fermi level of the p-type region also shifted into the valence band.

In thermal equilibrium, the extra electrons which reach the conduction band in the n-type region diffuse across the junction and combine with holes in the p-type region. As space charge builds up, a depletion region is created, preventing further electrons transferring to p-type region. As shown in Figure 2.13a, the p-n junction is in thermal equilibrium. More electrons from the n-region cannot move into the p-type region because they are repelled by the negative ions on the edge of the p-type region and attracted by the positive ions in the n-type region. A forward bias on the junction can assist electrons to overcome the space charge in the depletion region. Electrons will flow across the depletion region in this case as shown in Figure 2.13b.

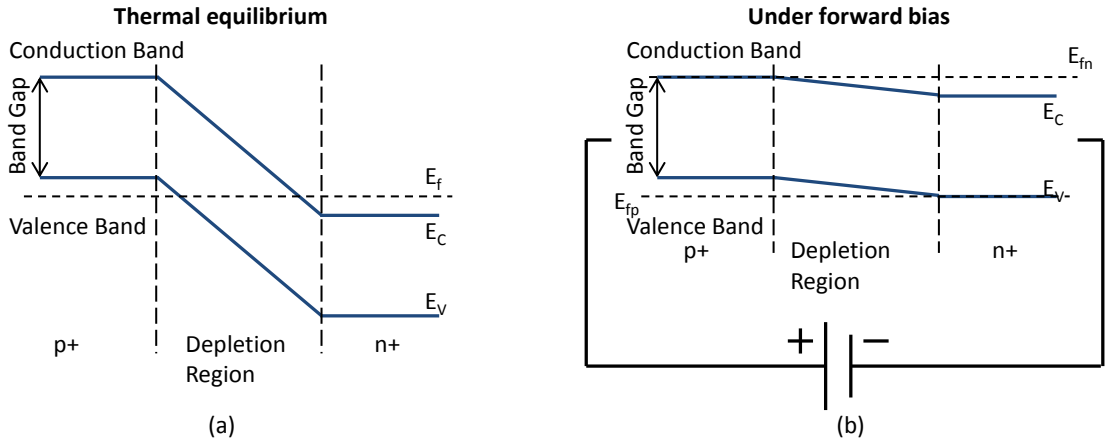

Figure 2.13 Schematic of energy bands for a P-N junction (a) in thermal equilibrium and (b) under forward bias

In Figure 2.13 Figure 2.13b, both electrons and holes exist in the depletion region. The recombination of electrons and holes generate photons. The recombination can be enhanced by adopting a heterojunction structure. A thin layer (intrinsic or lightly doped) of material with a narrower band gap is inserted between the p-type and n-type regions (Figure 2.14). Electrons and holes are confined in the thin layer due to the band gap discontinuity, allowing a higher carrier density to be achieved. The thin layer also has a higher refractive index compared to the surrounding layers. The layer, therefore, provides optical confinement, acting as a dielectric waveguide.

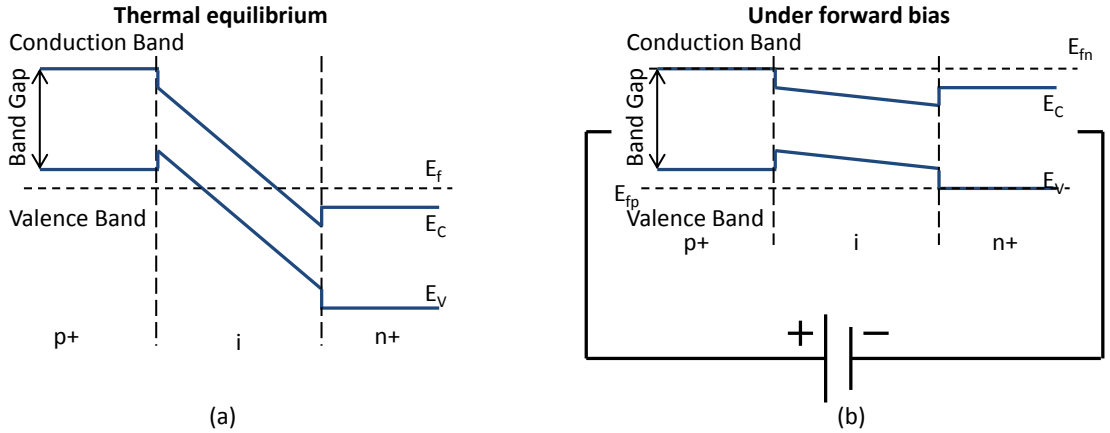

Figure 2.14 Schematic of energy bands for a double heterojunction (a) in thermal equilibrium and (b) under forward bias

2.3.4 Quantum-Well

The idea of the quantum devices is to modify the density of states, reducing the number of translational degrees of freedom for carriers and hence improving the optical performance of the devices [49][50].

In terms of quantum well devices, a thin "well" layer is surrounded by two "barrier" layers with a higher band gap. Both electrons and holes see lower energy in the "well", that is why it is called quantum well As the layer is so thin (about 100Å, 40 atomic layers), the fact that the electron and hole are waves cannot be neglected. The allowed states in this structure correspond to standing waves perpendicular to the layers. The electronic energy is, therefore, quantized in the system.

The basic characteristic of a quantum well can be explained by a "particle in a box" model. Figure 2.15 shows a "finite well" case, the barriers on either side of the quantum well have a finite height. The tunnelling penetration is considered in this case. The case can be simplified by assuming the barriers are infinitely high. The wave functions, therefore, much be zero at the walls of the quantum well [51].

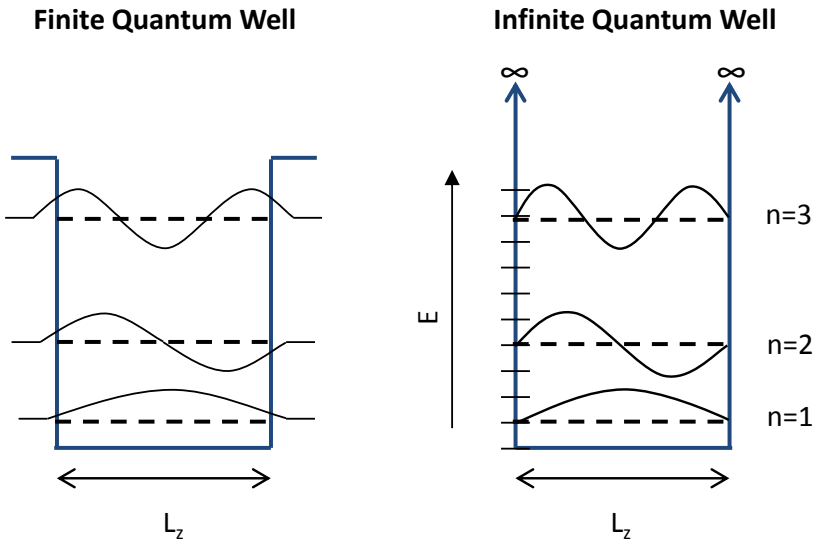

Figure 2.15 Schematic of a finite and infinite quantum-well with wave functions

L_z is the width of the quantum well. The available electrons' and holes' wavelengths are, therefore, given by Equation (2.4).

$$\lambda = \frac{2L_z}{n} \qquad (n = 1, 2, 3, 4 \ldots) \tag{2.4}$$

The momentum of these particles is calculated by substituting the above equation into the DeBroglie relationship as shown in Equation (2.5).

$$p = \frac{h}{\lambda} = \frac{nh}{2L_z} \qquad (n = 1, 2, 3, 4 \ldots) \tag{2.5}$$

The kinetic energy associated with the *nth* quantum state for a particle in an infinite box is then given by Equation (2.6).

$$E_n = \frac{1}{2}mv^2 = \frac{p^2}{2m} = \frac{n^2h^2}{8m{L_z}^2} \qquad (n = 1, 2, 3, 4 \ldots) \tag{2.6}$$

m is the effective mass of electrons or holes. The energy between the lowest energy level in conduction band and the highest energy level in the valence band is as shown in Figure 2.16 is given by Equation (2.7)[48].

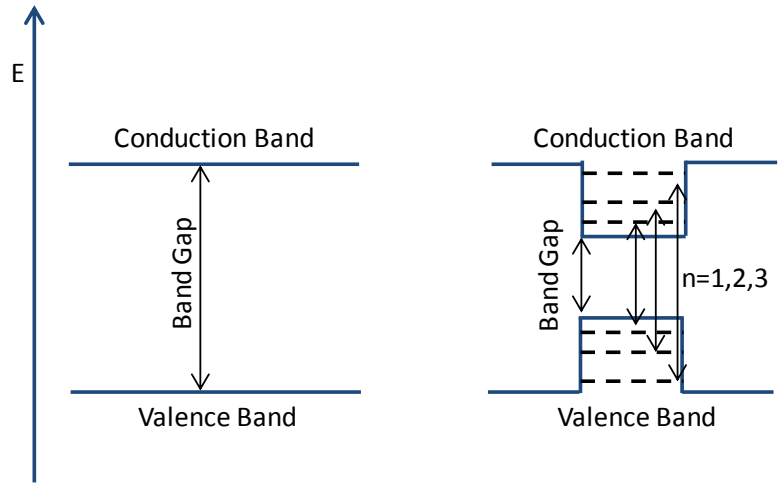

Figure 2.16 Schematic of energy bands for bulk structure and quantum-well structure

$$E_n \approx E_g + \frac{h^2}{8L^2}\left(\frac{1}{m_c} + \frac{1}{m_h}\right) \tag{2.7}$$

where m_c and m_h are the effective masses of the conduction band and valence band, respectively [48]. Although this equation is oversimplified, it indicates an important characteristic of the bound states for particles, the smaller the confinement, the larger the emitted photon energy.

Figure 2.17 compares the density of states in the bulk structure and the quantum-well structure. Carriers have 3-dimensional freedom in bulk structures while it is restricted to 2-dimensional freedom in quantum-well structures. Carriers can still move freely in the directions parallel to the layers. The carriers in a confined state, there, can have any amount of kinetic energy due to in-plane motion in the quantum well. They have energy greater than or equal to the simple discrete confined –state energy.

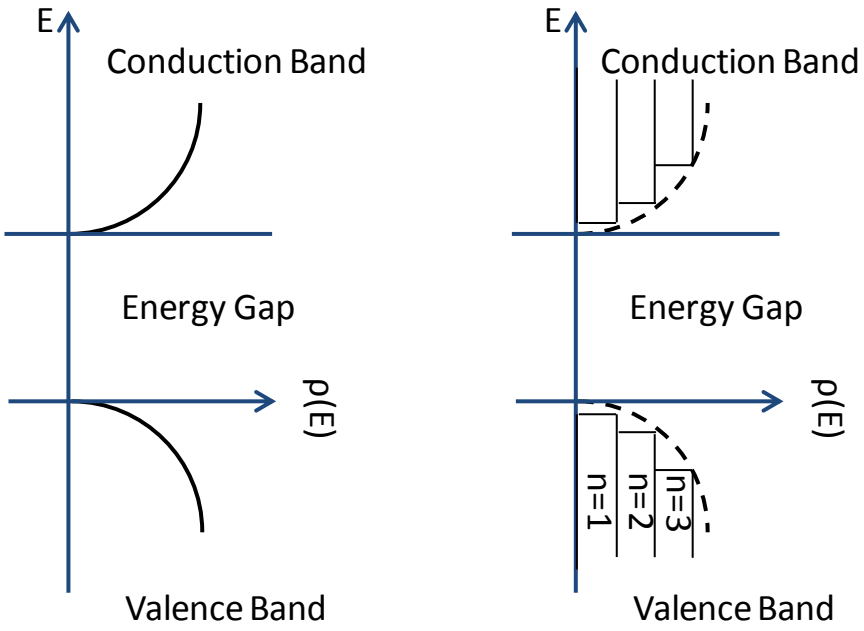

Figure 2.17 Density of states for bulk structure and quantum-well structure

2.3.5 SOA Rate Equations

The rate equations govern the dynamics of the amplification process in the active region of the semiconductor optical amplifiers. Approximations are made to simplify the carrier rate equation. The width and thickness of the active region are assumed generally small. The amplifier length is assumed much larger than the diffusion length. The carrier density is nearly uniform along the transverse dimension, and hence an average value is used in the approximation, and carrier diffusion is neglected. The carrier density in the active region is then given by the rate equation (2.8).

$$\frac{\partial N}{\partial t} = \mathrm{R_p(t)} - \mathrm{R_{st}(t)} - \mathrm{R_n(t)} \tag{2.8}$$

where N is the carrier density [52] [53]. $R_p(t)$ is the external pumping density rate of the injection current, increasing the population in the active region. $R_{st}(t)$ is the stimulated emission density rate, converting electrons to photons. $R_n(t)$ is the spontaneous recombination density rate.

Equation (2.9) describes the external pumping density rate.

$$\mathrm{R_p(t)} = \frac{\mathrm{I}}{\mathrm{qV}} \tag{2.9}$$

where I is the injection current, q is the charge of an electron, and V is the volume of the active region. The stimulated emission density rate is given by the Equation (2.10).

$$\mathrm{R_{st}(t)} = \frac{\mathrm{g(N)}}{\mathrm{h\nu}} |\mathrm{A}|^2 \tag{2.10}$$

where g(N) is the optical gain coefficient, v is the light frequency. hv, therefore, is the energy of a photon. A is the slowly-varying envelope associated with the optical pulse, and $|A|^2$ represents intensity. g(N) is defined by Equation (2.11).

$$\mathrm{g(N)} = \Gamma\alpha(\mathrm{N} - \mathrm{N_0}) \tag{2.11}$$

where Γ is the confinement factor, α is the differential gain (unit: meter squared), N_0 is the carrier density required for transparency. The no-radiation spontaneous recombination is given by Equation (2.12).

$$R_n(t) = \frac{N}{\tau_c} \tag{2.12}$$

where τ_c is the spontaneous carrier lifetime. The rate equation can, therefore, be rewritten as Equation (2.13). It also shows the carrier density in a steady state, where $\partial N/\partial t=0$.

$$\begin{gathered} \frac{\partial N}{\partial t} = \frac{I}{qV} - \frac{\Gamma\alpha|A|^2}{h\nu}(N - N_0) - \frac{N}{\tau_c} \\ \frac{I}{qV} = \frac{\Gamma\alpha|A|^2}{h\nu}(N - N_0) + \frac{N}{\tau_c} \quad (\frac{\partial N}{\partial t} = 0) \end{gathered} \tag{2.13}$$

2.4 Fundamentals of Mach-Zehnder Interferometers

2.4.1 Basic Structure and Mechanism

A Mach Zehnder Interferometer utilises the phase difference between signal arms and combines them either constructively or destructively at the corresponding output ports [55]. As shown in Figure 2.18, the MZI contains two 2x2 couplers and two phase modulators. The incoming optical signal is split into two branches at the first 2x2 coupler [56]. The phase modulators introduce different phase variations between the two branches. Interference occurs when two signals recombine at the second 2x2 coupler and this can be changed from destructive to constructive by controlling the phase modulators. Hence the power can be switched between the two output ports.

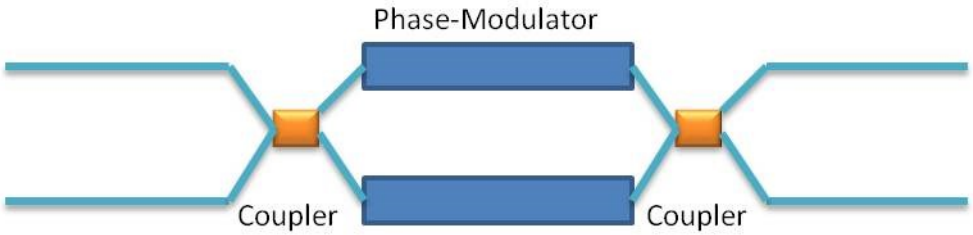

Figure 2.18 Schematic of MZI

2.4.2 2×2 Coupler

A 2×2 coupler is made of two waveguides. They are close enough to each other and overlapped over an interaction region as shown in Figure 2.19.

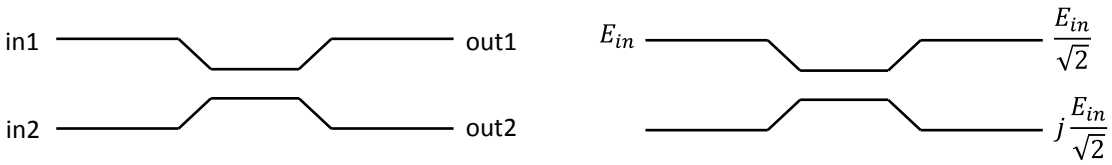

Figure 2.19 2x2 Coupler (a) Schematic (b) 3dB 2x2 Coupler [57]

The electric field in a 2×2 couple is defined by the Equation (2.14).

$$\frac{d\boldsymbol{E}(z)}{dz} = jK\boldsymbol{E}(z) \tag{2.14}$$

where z is the coupling length. E is the electrical field at two outputs, which is defined by Equation (2.15).

$$\boldsymbol{E}(z) = \begin{bmatrix} E_1(z) \\ E_2(z) \end{bmatrix} \tag{2.15}$$

And K is the coupling coefficient. It is defined by Equation (2.16).

$$K = \begin{bmatrix} 0 & \kappa \\ \kappa & 0 \end{bmatrix} \tag{2.16}$$

By using a scattering matrix, the output signal can be expressed by input signal as shown in Equation (2.17).

$$\begin{bmatrix} E_1(z) \\ E_2(z) \end{bmatrix} = \exp(jKz) \begin{bmatrix} E_1(0) \\ E_2(0) \end{bmatrix} = \begin{bmatrix} \cos(\kappa z) & \mathrm{jsin}(\kappa z) \\ \mathrm{jsin}(\kappa z) & \cos(\kappa z) \end{bmatrix} \begin{bmatrix} E_1(0) \\ E_2(0) \end{bmatrix} \tag{2.17}$$

For the 3dB coupler as shown in Figure 2.19(b), the input power is equally split into two output ports. Equation (2.18) is derived from Equation (2.17). The first solution with minimum z is obtained.

$$\begin{aligned} \cos^2(\kappa z) &= \sin^2(\kappa z) \\ \kappa z &= \frac{\Pi}{4} \end{aligned} \tag{2.18}$$

Equation (2.19) is then obtained with the first solution of κz.

$$\begin{bmatrix} E_1(z) \\ E_2(z) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} \begin{bmatrix} E_1(0) \\ E_2(0) \end{bmatrix} \tag{2.19}$$

With incoming optical field, E_{in}, at the first input port, both outputs are reduced in power by 3 dB and the second output has a 90 degrees phase shift.

$$\begin{bmatrix} E_1(z) \\ E_2(z) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} \begin{bmatrix} E_{in} \\ 0 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} E_{in} \\ jE_{in} \end{bmatrix} \tag{2.20}$$

2.4.3 Phase modulators

The phase modulator in each arm introduces a phase shift into the signals. It is achieved by changing the refractive index of the material. As the phase velocity of light in the waveguide is determined by the refractive index, the phase shift, therefore, is determined by the refractive index. The refractive index can be modified by either reverse biased voltage (depletion mode) or forward bias current (current injection mode).

The QCSE-based MZI is one of the reverse biased MZIs [58][59]. QCSE in quantum-well structure shows high electro-refraction and electro-absorption. In QCSE, The external electric field has effect on the light absorption/emission spectrum or emission spectrum of a quantum

well. When the external electric field is not applied, electrons and holes within the quantum well only occupy states within a discrete set of energy sub-bands. Only discrete frequencies of light can be absorbed or emitted. With increasing electric field shift the electron states to lower energies and shift the hole states to higher energies, which reduce the permitted light absorption frequencies and the refractive index changes accordingly [35]. The external electric field also shifts electrons and holes to opposite sides of the well, reducing the recombination efficiency. The potential barriers around the quantum well limits the spatial separation between the electrons and holes, which in turn make the excitons possible even under the influence of an electric field.

The QCSE-based phase modulators operate like capacitors, only consuming energy during transitions [60]. However, the in-band electro-absorption loss is currently inevitable, leading to intensity imbalance between two arms, which in turn causes the crosstalk.

2.4.4 MZI-based Switch

By introduction different phase shifts in two arms, the optical power at output ports can be controlled. Figure 2.20 shows two couplers connected together via a differential phase shift ϕ.

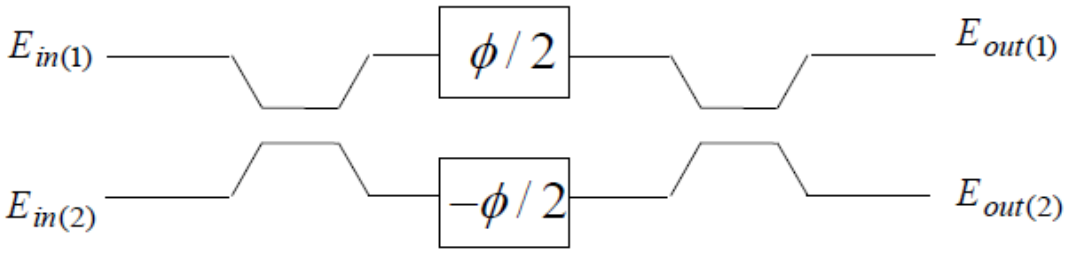

Figure 2.20 Schematic of Mach Zehnder modulator [57]

Equation (2.21) is derived to express the output electric field at two output ports.

$$\begin{bmatrix} E_{out(1)} \\ E_{out(2)} \end{bmatrix} = j \begin{bmatrix} \sin(\frac{\phi}{2}) & \cos(\frac{\phi}{2}) \\ \cos(\frac{\phi}{2}) & -\sin(\frac{\phi}{2}) \end{bmatrix} \begin{bmatrix} E_{in(1)} \\ E_{in(2)} \end{bmatrix} \tag{2.21}$$

With optical power only from first input power and zero phase difference between two arms. All power goes to the second output port with 90 degrees phase shift.

$$\begin{bmatrix} E_{out(1)} \\ E_{out(2)} \end{bmatrix} = j \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} E_{in} \\ 0 \end{bmatrix} = j \begin{bmatrix} 0 \\ E_{in} \end{bmatrix} \tag{2.22}$$

It can be noticed that the output signal power at both ports varies sinusoidally with the phase difference ϕ as shown in Equation (2.23) and (2.24).

$$\frac{E_{out}}{E_{in}} \propto \sin(\frac{\phi}{2}) \tag{2.23}$$

$$\frac{E_{out}}{E_{in}} \propto \cos(\frac{\phi}{2}) \tag{2.24}$$

That means if the phase difference shifts 180 degrees, the input signal can be totally directed from one output port to the other.

In ideal Mach Zehnder Modulators, perfect 3 dB splitters and phase modulators with equal length are assumed. Output extinction is complete in this case as calculated by above equations. In real devices, it is difficult to make the 3dB couplers exactly balanced and the lengths of two arms may be mismatched. Those factors lead to an imbalanced power between the two arms of the MZI, which introduces crosstalk to the output signal. The typical crosstalk of current commercial MZIs is -10 dB to 20 dB, restricting the scalability of MZI-based switches.

2.5 Conclusions

This chapter first reviewed the optical switching technologies. MEMS, thermo-optic, liquid crystal and acousto-optic switches have been studied to construct optical switches. MEMS switches are notable and have been available both as research demonstrations and in commercial products. Routing between more than 1000 ports has been demonstrated with low insertion loss. However, this type of cross-connect uses beam-steering technology which limits its response time to the millisecond and microsecond time scale. They are, therefore, suitable

for circuit switches in optical networks. Electro-optics switches (MZI) and SOA-based switches have demonstrated nanosecond reconfiguration time, which makes them suitable for routing packetized data with datacentres.

The basic operation of SOAs and MZIs was described in this Chapter. The operating principles, carrier density, heterostructure and quantum-well structure of SOAs were explained. The Dynamics of the amplification process in the active region of the SOA is governed by the rate equations. The beat noise between signal and spontaneous emission contributes to the noise at the detectors. An MZI is made of two 2x2 couplers and two phase modulators. The electric field at the output ports is governed by the matrix equations discussed in this chapter.

The noise and gain-saturated distortion limit the scalability of SOA-based switches while the crosstalk and loss degrade the performance of large-scale MZI-based switches. Different approaches have been made to mitigate those effects and increase the port count of fast-reconfiguration switches and these will be described later in the thesis.

Chapter 3 Fundamentals of Switch Architectures and Algorithms

3.1 Introduction

High-port-count switching networks are crucial required in both data centres and core networks to accommodate traffic considerable number of users. Most of the switching networks are constructed from 2×2 basic switching elements with various technologies mentioned in the last Chapter. The 2×2 basic switching elements are called building blocks in this approach [61]. A number of switch architectures have been proposed to scale up the size of switches by connecting 2×2 building blocks [62]. There are trade-offs between different architectures in terms of the total number of building blocks, the number of stages and the complicity of algorithms.

In this chapter, the common notation in switching networks is explained at the beginning [63]. Switching networks can be broadly categorised into two groups: blocking and non-blocking. Non-blocking architectures are required for most of inter- and intra-datacentre networks. In terms of non-blocking architectures, there are strictly, wide-sense and rearrangeably non-blocking networks. The last two architecture need less basic building blocks but require routing algorithm. Classical routing algorithms are discussed at the end of the chapter.

3.2 Notations

The switching networks discussed in this chapter connect N inputs to N outputs in an arbitrary manner. Inputs and outputs are numbered In#1, In#2, … , In#N and Out#1, Out#2, … , Out#N from top to bottom.

The building blocks between inputs and outputs can be numbered by their stages. Stages are numbered 1, 2, … , n from left to right as shown in Figure 3.1. Stage 1 is also referred as the input stage, and Stage n is called the output stage. The number of stages required depends on the architecture of the switch. The tree architecture only has one stage regardless of the number of port counts, switching on and off the signal with a single gate. Clos networks have n=3 stages, regardless of the number of inputs/outputs [64]. In contrast, a N×N Beneš network (discussed in 3.3.6) has $n=2\log_2 N-1$ stages and a N×N dilated Beneš (discussed in 3.3.7) switch has $n=\log_2 N$ stage.

Multi-stage switching networks are constructed by sub-switches with the smaller port count. The number of port count of input and output stage (Stage 1 and n) sub-switch in most research is 2^t where t is an integer. In this chapter, we consider the switching fabric with 2^t-port-count sub-switches, which is referred to as a base 2^t switch. The number of the sub-switch needed per stage is denoted by r. The value of $r=N/2^t$ depends on the size of the sub-switches. Sub-switches are numbered 0, 1, … , r from top to bottom as shown in Figure 3.1.

Figure 3.1 shows a Base 2 Beneš switch with the denotation of inputs/outputs, the number of stages and sub-switches.

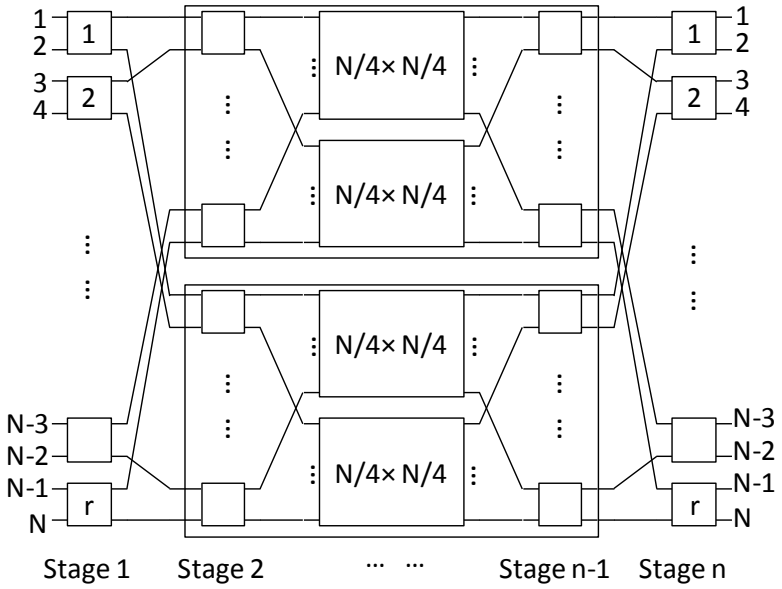

Figure 3.1– N×N base 2 Beneš switch with denotation

The connection assignment between input and output ports can be denoted by Π as shown in Equation (3.1) The corresponding output terminal of input port x is denoted by $\pi(x)$. The corresponding input terminal of the output port y is denoted by $\pi^{-1}(y)$ as shown in Equation (3.2). We shall consider only network states where all inputs and outputs are engaged for the algorithms in this chapter. This is sufficient since these states include all others. Such a state between all inputs and outputs is called a full assignment.

$$\Pi = \begin{pmatrix} 1 & 2 & 3 & \dots & N \\ \pi(1) & \pi(2) & \pi(3) & \dots & \pi(N) \end{pmatrix} \tag{3.1}$$

$$\Pi^{-1} = \begin{pmatrix} \pi^{-1}(1) & \pi^{-1}(2) & \pi^{-1}(3) & \dots & \pi^{-1}(N) \\ 1 & 2 & 3 & \dots & N \end{pmatrix} \tag{3.2}$$

An odd port and its next even port are called dual to each other. The dual of input x (output $\pi(x)$) is denoted as $\sim x$ ($\sim\pi(x)$). When links are set up in a switching network, x and its dual $\sim x$ are connected to different sub-switches at the next stage.

Signal paths are created via switching networks by setting up connections between sub-switches in adjacent stages. Each method to realize a connection assignment is called a set-up. The switching networks considered in this chapter have a symmetrical architecture. To create a set-up, the connections are made from the sub-switches from two sides (stage 1 and stage n) to adjacent sub-switches at the more inner stages.

3.3 Switch Architecture

Large scale-optical switches are required for next-generation optical networks. Large-port-count optical switches are built by cascading a number of basic switching elements with certain switch architectures. A few key characteristics are considered when selecting the switch architecture [16]:

Blocking/Non-Blocking: If any connection assignments are able to be realised in a switch, architecture, this architecture is called a non-blocking architecture. This non-blocking characteristic might have conditions depending on the architecture. If certain connection

assignments are not able to be set up with a switching network, this network is blocking. Details of blocking/non-blocking architectures are described in Chapter 3.3.1.

Number of switching elements: Large-scale optical switches comprise substantial basic switching elements. The number of switching elements has a relatively large variation among different switch architectures. The number of switching elements determines the cost, the complexity of control and the ease of fabrication. It is, therefore, a key characteristic to be considered when designing switches.

Loss uniformity: Paths are set up between corresponding input and output ports. They might consist of a different number of switch elements and various lengths of optical links. The accumulated loss among different paths in the same switch, therefore, can be different. Uniform loss is preferred for optical switches, offering uniform performance across all paths. Loss uniformity can be achieved with either special switch design or advanced algorithms. An advanced path-selection algorithm proposed in this thesis is discussed in Chapter 4.

Number of crossovers: Integrated optical circuits are promising technology in recent years, offering compact systems with high performance. Optical switches fabricated on integrated optical chips use waveguides to connect switching gates. Unlike integrated electronic circuits, where the crossovers of metal wires can be avoided by fabricating metal wires at different layers, in integrated optics, all the waveguides usually only can be made within a single layer, and these waveguide crossovers are inevitable. The crossovers lead to crosstalk and optical loss. Hence, it is also desirable to minimise the number of crossovers for a given switch design.

3.3.1 Blocking Characteristics

One of the key characteristics of blocking/non-blocking switches is the **Blocking State**. Figure 3.2 shows a blocking state in a 4×4 Beneš switch. 2 of 4 corresponding input-output pairs are connected in the demonstrated state with the assignment shown in Equation (3.3).

$$\Pi = \begin{pmatrix} 1 & 2 & 3 & 4 \\ 4 & \pi(2) & \pi(3) & 1 \end{pmatrix} \tag{3.3}$$

Links from In#1 to Out#4 and from In#4 to Out#1 are set up (bold lines). With the current state, it is impossible to connect any idle input port to any idle output port. For instance, In#2 cannot be connected to Out#2 via any available path. Although there are other states in which this connection is achievable, certain links are not able to be set up in the current state. States with this characteristic are defined as blocking states.

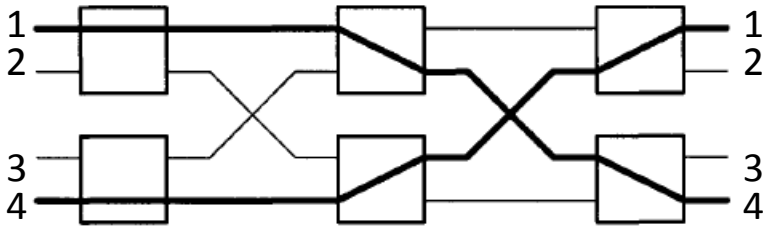

Figure 3.2– Blocking state in a 4×4 Beneš architecture

The blocking and non-blocking characteristics are defined by the occurrence of blocking states:

- **Blocking switches:** the blocking states cannot be avoided by any arrangement of connections.
- **Non-blocking switches:** Every combination of connections is able to be realised.

The non-blocking switches are further categorised into four classes:

- **Strict-sense non-blocking switches:** Any idle input ports can be connected to any idle output port, regardless of the current state and path selection algorithm.
- **Wide-sense non-blocking switches:** Any pair of idle input and output ports can be connected following a certain path selection algorithm, regardless of the current state.
- **Rearrangeably non-blocking switches:** Any pair of idle input and output ports can be connected. However, some existing connections need to be reassigned to alternative connecting paths.
- **Repackably non-blocking switches:** this is similar to the rearrangeably non-blocking switch, but the rearrangement of existing connection is implemented each time after one of the existing connections is terminated [66]. The purpose of this design is to increase the loading of the most used middle-stage switches, leaving the less loaded middle-stage switches free for new connections.

The first three architectures are widely studied and therefore discussed in detail in this chapter. The different number of building blocks required to build large-port-count switches with these three architectures. Generally, the strict sense non-blocking architecture requires the largest number of building blocks, then the wide sense non-blocking architecture. The rearrangeably non-blocking architecture needs the least number of building blocks.

The number of building blocks required for strict sense non-blocking switches increases exponentially with the port count. The rearrangeably non-blocking architecture, therefore, attracts a lot of research interest since it constructs a given-size large-port-count switch with the smallest number of building blocks. Although the existing connections need to be cut off and moved to alternative paths, the connection re-setting up can be done within guard bands between data packets to mitigate the loss of data during switching events.

In this chapter, a number of well-known switch architectures are introduced and compared. They are categorized into two main groups:

1) Single-stage Switch Fabrics
    - Crossbar [67][68]
    - Tree [69][70]
2) Multi-stage Switch Fabrics
    - Clos [64]
    - Banyan [71]
    - Beneš [65]
    - Dilated Beneš [72]

In terms of single-stage switches, both Crossbar and Tree architectures are strict sense non-blocking. The Clos architecture can be strict sense, wide sense or rearrangeably non-blocking depending on the number of middle-stage sub-switches. The Banyan architecture is, however, a blocking architecture. It is the cornerstone of Beneš architectures. Half of a Beneš network with the centre stage is a Banyan-type architecture. Half of the dilated Beneš network with one more adjacent stage is also a Banyan-type.

3.3.2 Crossbar Architecture

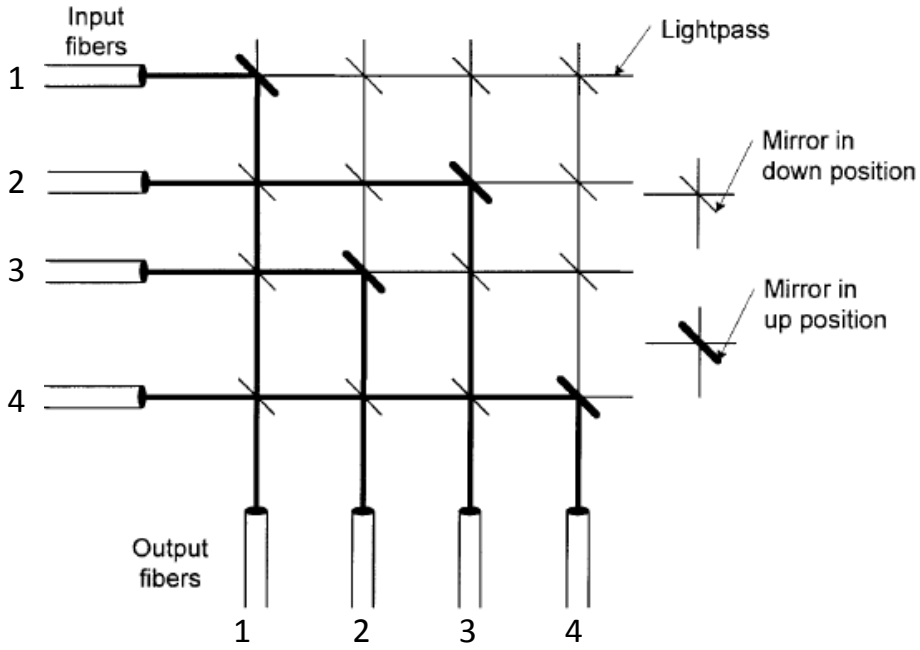

Figure 3.3– A 4x4 Crossbar switch with micro mirrors [61]

The crossbar architecture is widely used in electronic switches and MEMs optical switches. This topology can be seen as a matrix with rows (for inputs) and columns (for outputs) joined by cross points. In optical switches, micro mirrors are usually used as cross points [73]. As discussed in Section 2.1.1

- When a mirror is activated to the up position, it moves into the path of a beam and redirects the input beam to one of the output ports.
- When all the mirrors below the path of a beam stay in the down position, the light passes through the switch matrix and is dropped.

The crossbar architecture is strict-sense non-blocking, and thus easy to control (no routing algorithm required). However, for a N×N crossbar switch, the number of cross points (switching gates) required is N^2. Consequently, the number of required cross points for large-port-count switches will be extremely high.

The other concern for crossbar switches is the path-dependent insertion loss. As shown in Figure 3.3, the optical paths between different pairs of input and output ports have distinct lengths. The link between In#4 and Out#1 is the shortest one with smallest passive loss, while the link connection In#1 and Out#4 suffers the largest insertion loss.

3.3.3 Tree Architecture

The tree type architecture is a single-stage broadcast-and-select fabric. Between every input port and output port, there is a switching gate. A common switching gate is the semiconductor optical amplifier (SOA). In the ON state, it not only passes the signal through the gate but also amplifies the signal power to compensate the passive loss of the broadcast fabric. In the OFF state, it attenuates the signal power to turn off the signal at the switching gate.

Figure 3.4 shows 2×2 and 4×4 tree architecture switches. In the 2×2 switch, an input broadcasts into 2 branches, which are connected to switching gates [74]. Each switching gate is then connected to the corresponding output port. The signal from the input port, therefore, can be sent to any output port by turning on the corresponding switching gate. The 4×4 tree architecture [75][76] also can be built using 2×2 switches (as building blocks).

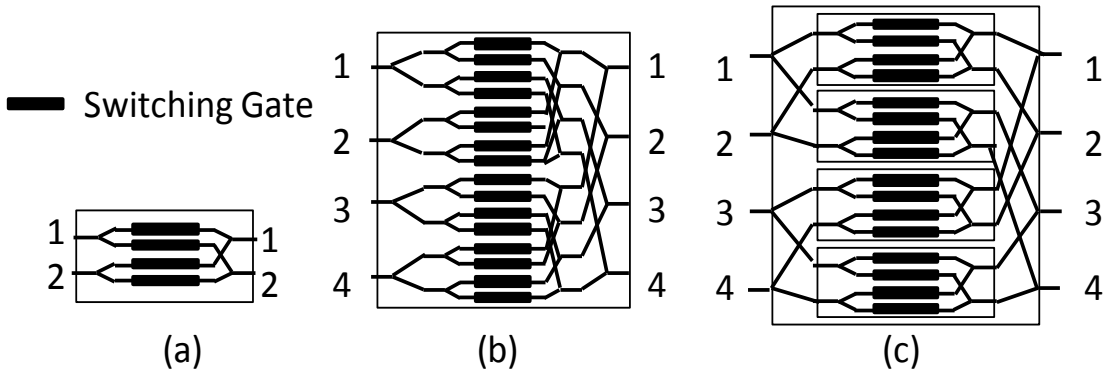

Figure 3.4 (a) 2x2, (b) 4x4 tree architecture, (c) 4x4 architecture built by 2x2 switches

The advantage of the tree architecture is that it only has one stage, greatly simplifying the control of the switch. However, similar to cross bar switches, the number of switching gates required grows geometrically with the port count. A N×N tree architecture switch consists of N^2 switching gates or $N^2/4$ 2×2 building blocks. For unsymmetrical N×M switches, the number

of required gating elements is N×M. High-port-count tree architecture switches, therefore, required a large number of switching gates. It leads to unpractical large footprints in integrated photonic circuits. Additionally, as shown in Figure 3.4, splitters and combiners are used to construct the broadcast and select network. The total number of splitters and combiners, SC, required for a N×N tree-architecture network is shown in Equation (3.4).

$$SC = 2 \times \log_2 N \tag{3.4}$$

Each of them introduces at least 3 dB loss into the system. The accumulated loss for a high-port-count switch is considerable. Gain from the SOA is used to compensate the loss. However, amplified spontaneous emission (ASE) noise and distortion are also enhanced with the increase of gain, degrading the signal performance [77].

3.3.4 Clos Architecture

The Clos architecture is the classical architecture for three-stage switches [64]. It can be strict-sense, wide -sense or rearrangeably non-blocking depending on the design of the switch.

Here, the number of the middle-stage switches is denoted as m, and the number of input ports of a first-stage sub-switch (or output ports of a last-stage sub-switch) is denoted as d. The size of the first-stage switches is, therefore, d×m (it is m×d for last-stage switches). The values of m and d determine the blocking characteristic of the Clos architecture:

- Strict-sense non-blocking: $m \geq 2d - 1$ (Figure 3.5)
- wide-sense non-blocking: $\frac{3d}{2} \leq m \leq 2d - 1$ (Figure 3.6)
- Rearrangeably non-blocking: $d \leq m \leq \frac{3d}{2}$ (Figure 3.7)

Figure 3.5, 3.6 and 3.7 show 16×16 architectures with strict sense, wide sense and rearrangeably non-blocking characteristics, respectively. Each of three 16×16 architectures has 4 first-stage sub-switches. The number of input ports of a first-stage sub-switch is 4 (d=4) for all three switching architectures. The number of middle-stage switches, therefore, determines the blocking characteristics of the switching fabrics.

- Strict-sense non-blocking (m=7, d=4): $m \geq 2d - 1$ (Figure 3.5)
- wide-sense non-blocking (m=6, d=4): $\frac{3d}{2} \leq m \leq 2d - 1$ (Figure 3.6)
- Rearrangeably non-blocking(m=4, d=4): $\leq m \leq \frac{3d}{2}$ (Figure 3.7)

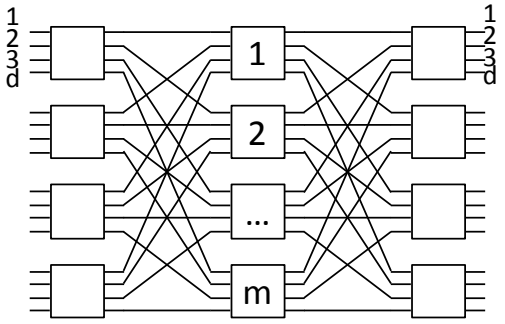

Figure 3.5 16x16 Clos architecture – strict sense non-blocking

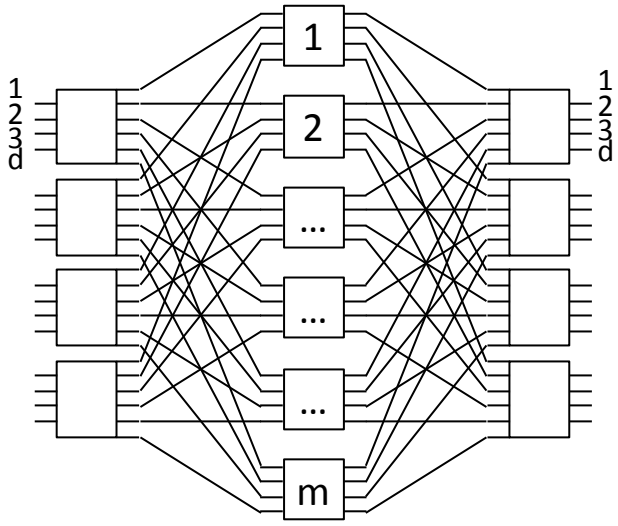

Figure 3.6 16x16 Clos architecture – wide sense non-blocking

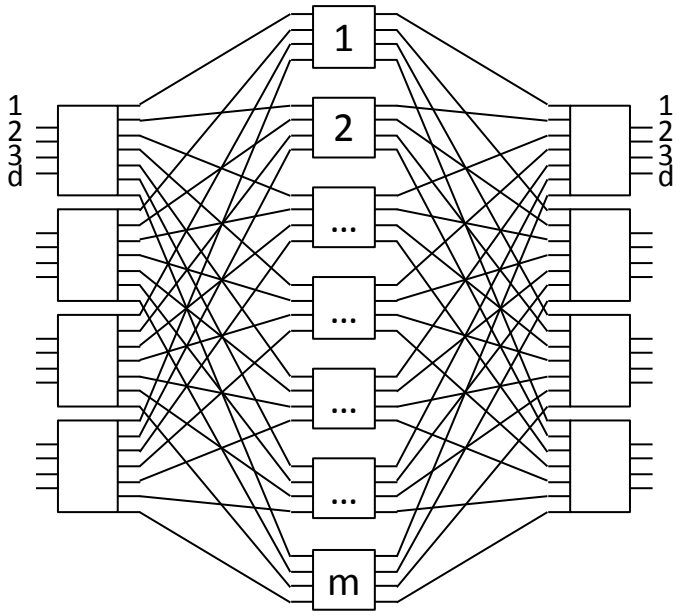

Figure 3.7 16x16 Clos architecture – rearrangeably non-blocking

It should be noted that all sub-switches in the discussion above are assumed strict-sense non-blocking. If any sub-switch is wide-sense or rearrangeably non-blocking in a strict-sense non-block Clos architecture, the non-blocking characteristic of the whole switching fabric will be degraded to wide-sense or rearrangeably non-blocking, respectively. The non-blocking characteristic is always same with the lowest non-blocking characteristic of all hierarchical levels.

3.3.5 Banyan-type Architecture

The Banyan-type architecture [71] is the only blocking architecture discussed in this chapter. Although it is rarely implemented in the modern data exchange networks, it is the cornerstone of widely used Beneš architecture.

Generally, a N×N Banyan switch can be constructed from sub-switches with a variety of sizes. The number of stages of a N×N Banyan architecture with d×d sub-switches is shown in Equation (3.5) [71].

$$n = \log_d N \tag{3.5}$$

The most important characteristic of the Banyan-type architecture is its packing scheme: the network can be redrawn by reordering sub-switches in the same stage without changing the way the sub-switches were interconnected between themselves [78][79][80][81]. With this packing scheme, different 8×8 Banyan-type structures can be obtained as shown in Figure 3.8. An original Banyan switch is shown in Figure 3.8a with all sub-switches numbered. The reverse Banyan switch (Figure 3.8b) is constructed by swapping sub-switches 2 and 3 in all stages. The Baseline switch (Figure 3.8c) is obtained by exchanging switches 2 and 3 in the first stage.

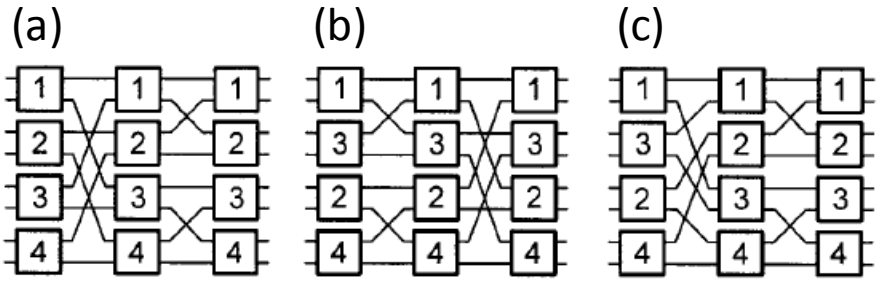

Figure 3.8 (a) Banyan (b) Reverse Banyan and (c) Baseline [61]

This topology can be constructed recursively. A N×N switch is constructed by two N/2×N/2 switching fabrics with an additional stage connecting the two parts of the switching fabric together. The Banyan-type switches have these following properties, which are still valid in the architectures based on Banyan-type switches.

- **Buddy property**: If a sub-switch r1 at stage n is connected with r3 and r4 at stage n+1, r3 and r4 are also connected with the same switch r2 at stage n. For instance, in an 8×8 Banyan network (Figure 3.8a), sub-switches 1 and 3 at stage 1 are connected with sub-switches 1 and 3 at stage 2. They are kept separated with other sub-switches through the first two stages. The signals are only "mixed" among themselves.
- **Imprimitive network**: the buddy property can be extended to more than two stages. The signals which are only "mixed" among themselves over a certain number of stages define a set of imprimitivity. The corresponding part of the network is termed as an imprimitive network. Banyan-type networks are imprimitive networks, which allow their packing scheme.

- **Exclusive connection**: there is one and only one possible link between each input port and each output port.
- **Self-routing**: the route in the switching fabrics can be determined by the number assigned output ports. Figure 3.9c shows the self-routing in a 16×16 baseline switch. The number of output ports is renumbered from 0 here as they need to be converted to binary numbers. The number of the assigned output ports in binary is added to packets with the most significant bit at first position. The number of digits is equal to the number of stages. Each bit controls the corresponding 2×2 building block in different stages. The most significant bit controls the building block at Stage 1. As shown in Figure 3.9a & b, if the bit is 0, the signal is directed to the upper output, and vice verse. For example, the packet from In#0 is sent to Out#8 (1000 in binary).
    - In#1 → Stage 1: lower output(1) → Stage 2: upper output (0) → Stage 3: upper output(0) → Stage 4: upper output (0) → Out#8

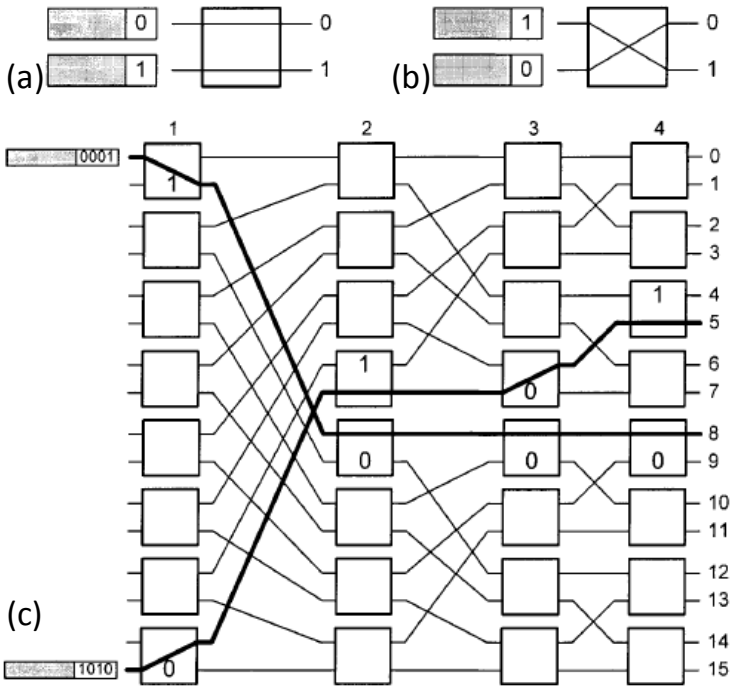

Figure 3.9 (a)(b) Self-routing control in a 2×2 building block (c) Self-routing in a 16×16 Banyan-type network [61]

Other binary networks, such as Reverse Banyan and Baseline (Figure 3.8 b & c), can be obtained from Banyan architecture by reordering sub-switches in stages without changing the way switches were interconnected between themselves. This makes Banyan architectures have self-routing ability [82].

3.3.6 Beneš architecture

The Beneš architecture [65] can be seen as a rearrangeably non-blocking Clos architecture entirely constructed by 2x2 basic switching elements as shown in Figure 3.10. The Beneš architecture is constructed recursively by using N/2×N/2 Beneš switches as middle-stage sub-switches until 2x2 middle-stage sub-switches are reached.

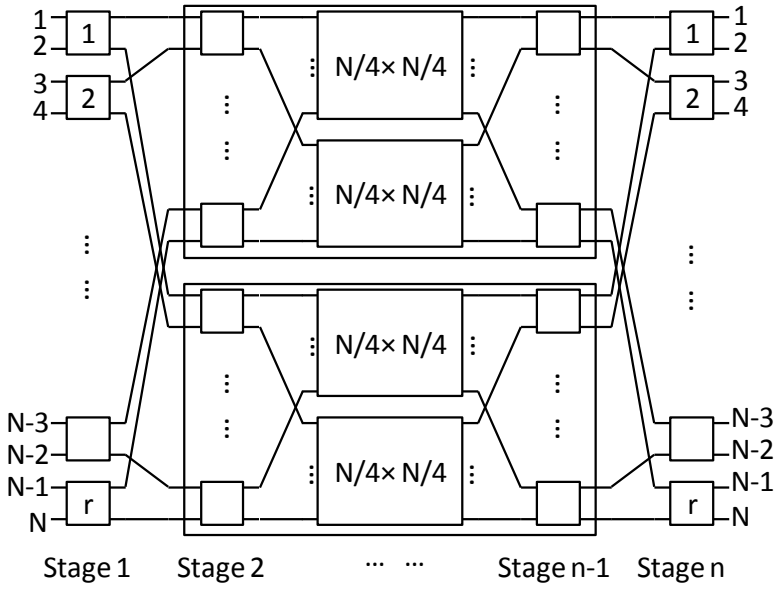

Figure 3.10 Beneš architecture – Recursive construction [65]

The total number of stages is calculated by Equation (3.6)

$$n = 2 \times \log_2 N - 1 \tag{3.6}$$

This equation is similar to the Equation (3.5), which calculates the number of stages for Banyan-type switches. As shown in Figure 3.11, half of a Beneš network with the centre stage

is a Baseline architecture. Therefore, the number of stages of a Beneš doubles that of a Baseline architecture and minuses one.

The properties of Banyan-type networks, therefore, can also apply to Beneš networks. The sub-switches can be re-ordered to achieve certain special characteristics. The self-routing property can be implemented to direct the signal from the select middle-stage sub-switch to the assigned output port.

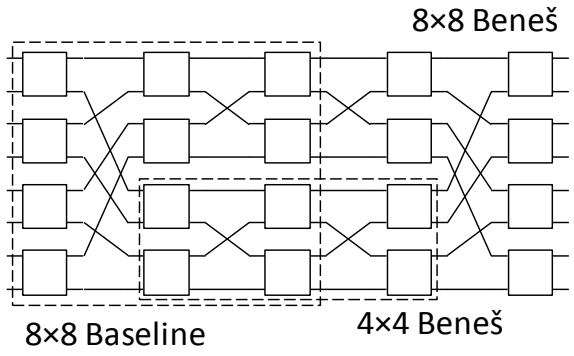

Figure 3.11 8×8 Beneš architecture

The number of 2×2 building blocks required for a N×N Beneš switch is shown in Equation (3.7). The number of stages, n, times the number of building blocks per stage is the number of building blocks required to construct the switch.

$$B = N \times \log_2 N - \frac{N}{2} \tag{3.7}$$

This number is much smaller than that of the tree architecture. The disadvantage of this design, compared with the tree architecture, is the cascaded stages. The noise and crosstalk from the switching gates are accumulated with an increasing number of stages.

3.3.7 Dilated Beneš architecture

Crosstalk is one of the issues that limit the scalability of optical switches. When two signals share a gating element, such as Mach Zehnder Interferometers, undesired coupling from one path to the other results in crosstalk. The switch crossover within each 2×2 building block can, therefore, cause crosstalk between two incoming signals. For a Beneš network with a full

assignment, to support all N paths through the network, every 2×2 building block has two active inputs. The accumulated crosstalk from cascaded building blocks is a limiting factor of large-scale switches.

The dilated Beneš architecture has been proposed to ensure no building blocks carry more than one active path [72]. The crosstalk within building blocks is, therefore, negligible, which enhances the scalability of the dilated Beneš architecture. An 8x8 Ti: $LiNbO_3$ switch has been fabricated with dilated Beneš architecture, demonstrating low crosstalk performance [83].

The recursive construction of a N×N dilated Beneš switch is shown Figure 3.12. Both the first stage and last stage are N 2×2 building blocks. Only one input (output) is connected to the input (output) terminal to ensure there is only one active path through a 2×2 sub-switch. Two sub-networks with N×N ports are used as middle stages. Only half of the inputs and outputs are active at any time, which means a N×N sub-network is technically a N/2×N/2 dilated Beneš network. Every 2×2 switch at the input- and output-stage of the N/2×N/2 dilated Beneš networks has only one active input and output, respectively. N/2×N/2 dilated Beneš sub-networks are constructed recursively until 2×2 dilated Beneš sub-networks are reached. A 2×2 dilated Beneš network is constructed by two stages of building blocks as shown in Figure 3.13.

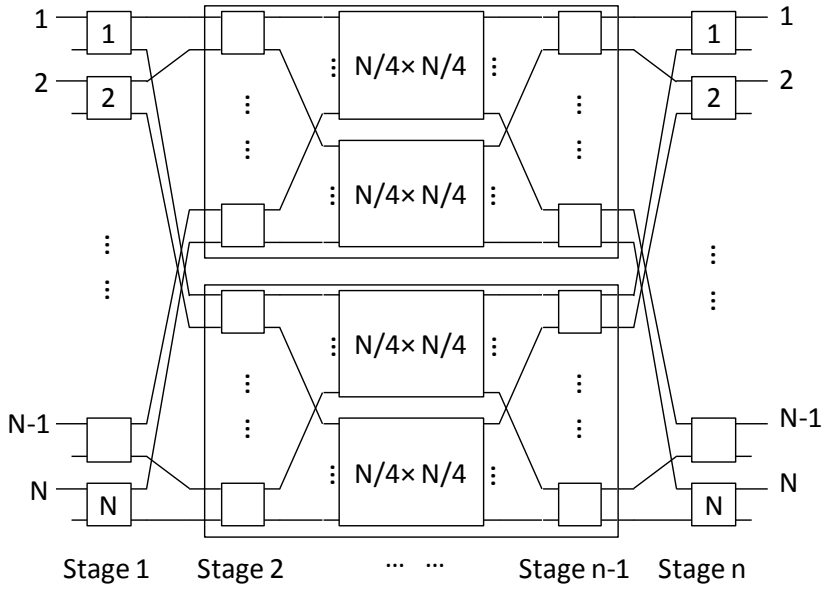

Figure 3.12 Dilated Beneš architecture – Recursive construction [72]

Similar to the Beneš architecture, the dilated Beneš architecture is also rearrangeably non-blocking. The total number of stages required for a N×N Dilated Beneš architecture is calculated by Equation (3.8). A dilated Beneš architecture needs one more stage than a Beneš architecture with an exactly same size [Equation (3.5)].

$$n = 2 \times \log_2 N \tag{3.8}$$

The number of 2×2 building blocks required for a N×N Dilated Beneš architecture is calculated in Equation (3.9). It almost doubles the number of building blocks required for a Beneš architecture with the same size because each 2x2 building block at input/output-stage only has one fixed active input/output.

$$B = 2 \times N \times \log_2 N \tag{3.9}$$

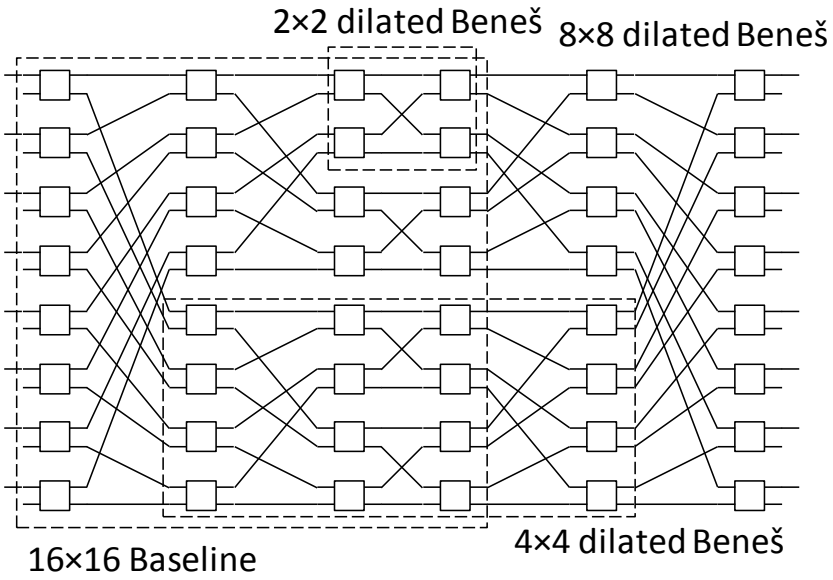

Figure 3.13 8×8 Dilated Beneš architecture [72]

As shown in Figure 3.13, half of the dilated Beneš network with one more adjacent stage is a Baseline network. The properties of Banyan-type networks, therefore, can also apply to dilated Beneš networks.

Special layouts of the dilated Beneš can be constructed by re-ordering the sub-switches in same stages (Kabacinski, Modified dilated Benes networks for photonic switching 1999). Figure 3.14a shows a modified 8×8 dilated Beneš obtained by re-ordering sub-switches in stage 2 and 5. The modified network can be entirely constructed by 2x2 dilated Beneš switches and the shuffle networks between them are identical. It might ease the design and fabrication of integrated dilated Beneš switches.

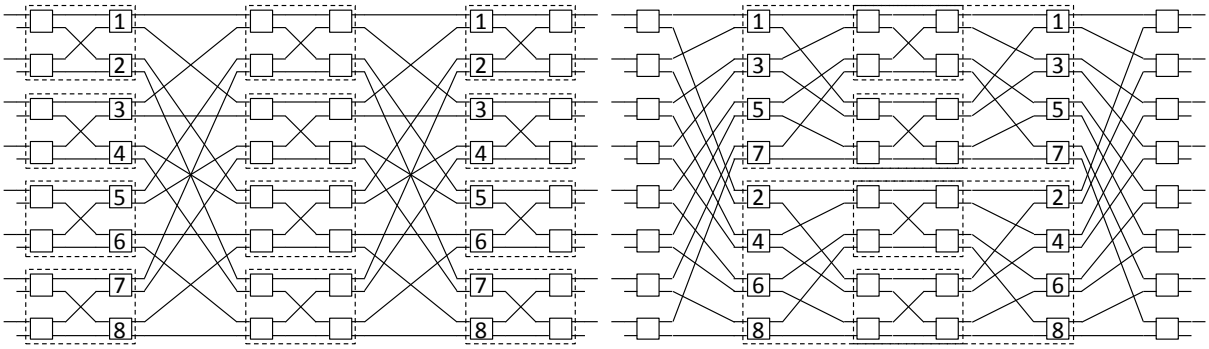

Figure 3.14 a) Modified 8x8 dilated Beneš switches b) Original 8x8 dilated Beneš switches

3.3.8 Optical Switch Architecture Summary

The key characteristics of the all switch architectures discussed above are summarised in Table 3.1.

Table 3.1 Summary of switch architectures

Architecture	Blocking Characteristics	Number of Stages	Number of Building Blocks
Crossbar	Strict sense non-blocking	1	--
Tree	Strict sense non-blocking	1	$\frac{N^2}{4}$
Clos	Depends on the number of middle-stage switches	3	$2 \times m \times n + \frac{m \times n^2}{d^2}$*
Banyan	Blocking	$\log_2 N$	$\frac{N}{2} \times \log_2 N$
Beneš	Rearrangeably non-blocking	$2 \times \log_2 N - 1$	$N \times \log_2 N - \frac{N}{2}$
Dilated Beneš	Rearrangeably non-blocking	$2 \times \log_2 N$	$2 \times N \times \log_2 N$

*Assume the sub-switches are tree-architecture switches

The single-stage architectures (Crossbar and Tree architectures) only require one stage. The accumulated crosstalk and other effects are therefore very low. Additionally, as a strict-sense non-blocking architecture, a routing algorithm is not required. For those reasons, they are, therefore, potential candidates for small-scale optical switches (smaller than 8×8 port count). The number of building blocks of the tree architecture, however, increases exponentially with the port count. Switches with more than 8×8 port count tend to used rearrangeably non-blocking architecture to minimise the number of building blocks required. Figure 3.15 shows the number of building blocks required for each architecture, which also indicates the footprint of each designs.

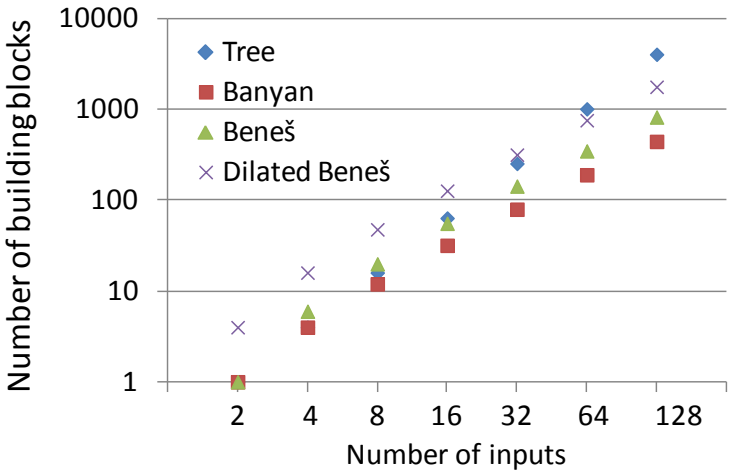

Figure 3.15 Number of building blocks as a function of the number of inputs

Figure 3.16 shows the number of stages required for each architecture. The path loss is mainly determined by the number of stages and the design of the shuffle network. Although, the tree architecture only has one stage, the size of the broadcast and select network grows geometrically with the number of ports. The Beneš architecture required one less stage than and dilated Beneš architecture. The complexity of the Beneš increase from the inner stage to the outer stages, while the shuffle network for dilated Beneš architecture has the same complexity, which leads to substantial loss for large-size switches. There are trade-offs when selecting the architecture of the switches, especially for large-size switches, which are discussed in Chapter 6.

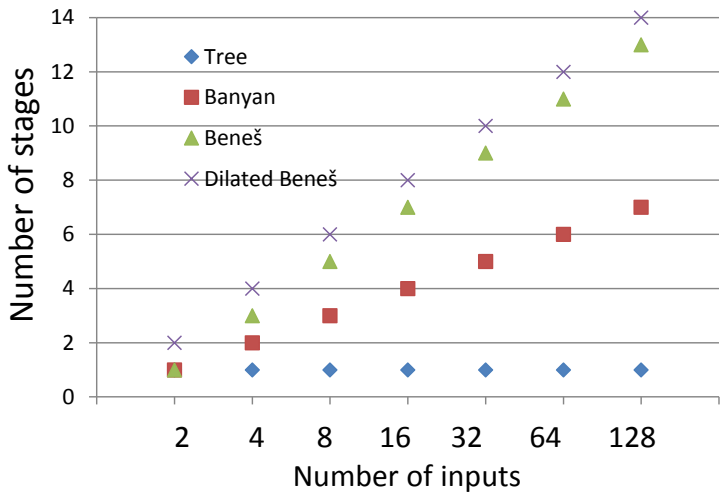

Figure 3.16 Number of stages blocks as a function of the number of inputs

There is a trade-off between the blocking characteristic and number of building blocks. For instance, a rearrangeably non-blocking Clos architecture requires fewer building blocks compared with a strict/wide sense non-blocking Clos network. More complex routing algorithms, however, are needed to set up paths through the rearrangeably non-blocking Clos architectures. A trade-off also exists between the crosstalk performance and the number of building blocks. The dilated Beneš architecture almost doubles the number of building blocks compared with the Beneš architecture, while greatly reducing the crosstalk. For large-scale optical switches, the dilated Beneš architecture arguably demonstrates the most balanced performance in terms of the number of building blocks, the number of stages and crosstalk performance. In this thesis, we, therefore, study the characteristics and performance of the dilated Beneš architecture in detail.

3.4 Routing Algorithm

When a switching network receives a connection assignment, the paths between the corresponding input and output ports need to be set up. In strict sense non-blocking architectures, such as tree and crossbar architectures, there is one and only one possible link between each input port and each output port. Setting up connections requires no routing algorithm. Switching the exclusive gating element links the assigned input and output ports.

Blocking architectures, such as Banyan-type networks, might not be able to realise the given connection assignments. In terms of achievable connection assignments, no routing algorithm is required as there is only one possible link between each input and output port.

Multi-stage architectures, such as Clos, Beneš and dilated Beneš architectures, require a routing algorithm to set up paths. Basically, a connection is set up via a middle-stage sub-switch/sub-network in multi-stage non-blocking architectures. A link between a pair of input and output can be realised by any available middle-stage sub-switch.

Several **path searching algorithms** can be used to check the availability of middle-stage sub-switch and assign an available sub-switch to the new connection:

- **Random Algorithm:** Check the middle-stage sub-switches randomly and set up the connection via any available sub-switch.
- **Sequential Algorithm:** Check the availability of middle-stage sub-switches from top to bottom and assign the link via the first available sub-switch.
- **Round-robin Algorithm:** from the sub-switch next to the one used to route the last connection, check the availability of sub-switches from top to bottom and set up the connection via the first available sub-switch.
- **Cyclic Static Algorithm:** a middle-stage sub-switch is able to route more than one signal. This algorithm checks the availability of the sub-switches which routes the last connection. If it is fully assigned, it checks the next middle-stage sub-switch.
- **Save-the-unused Algorithm:** it avoids routing signals via any empty middle-stage sub-switches. It randomly routes signals via sub-switches with existent connections.
- **Packing Algorithm:** this has a similar concept to the save-the-unused algorithm. It routes a new connection via the busiest but available middle-stage sub-switches.

In the above path searching algorithms, if all middle-stage sub-switches are assessed, and no available path is found, the switch is in a blocking state. Rearrangeably non-blocking architectures are especially vulnerable with path searching algorithms and can easily end up with the blocking state. To mitigate the blocking state, rearrangement algorithms, such as Paull's matrix has been proposed to rearrange the existent links and make available middle-stage sub-switches for new connections. Other approaches consider the entire given connection

assignment and set up all links together [84][85][86][87][88][89][90]. The looping algorithm has been proposed set-up connections in the Base 2 switching networks [91]. It is also extended to All Beneš, Clos [92] and dilated Beneš architectures [72]. The looping algorithm and its extended algorithms, therefore, are discussed in this chapter.

3.4.1 Looping Algorithm

The looping algorithm is the classic routing algorithm which was proposed for electrical switching networks [91]. The original algorithm was proposed for base 2 switching networks in which the first- and last-stage sub-switches have the 2×2 port count (details have been explained in 3.2 Notation).

The looping algorithm sets up paths from the Stage 1 and Stage n 2×2 sub-switches via middle-stage sub-networks. The links can be established via either upper or lower middle networks. As the Stage 1 and Stage n are composed of 2×2 sub-switches, the two terminals on the same 2×2 sub-switch are dual to each other (details have been explained in 3.2 Notation). They are connected to different N/2×N/2 middle networks in set-ups.

The steps of the looping algorithm are shown by Algorithm 3.1. This takes a full connection assignment as input and starts the connection from the In#1. It links the In#1 to its corresponding output port $\pi(1)$ via the upper middle network. It then links $\sim\pi(1)$, the dual of $\pi(1)$, to its corresponding input port $\pi^{-1}(\sim\pi(1))$ via the lower middle network. After that, it checks whether $\sim\pi^{-1}(\sim\pi(1))$, the dual of $\pi^{-1}(\sim\pi(1))$, is input port #1. If it is, the algorithm completes a loop and searches for the next unconnected input terminal from top to bottom to start another loop. If it is not, it continues this linking procedure until it reaches the beginning port of the loop. This algorithm takes a number of loops to connect all inputs and outputs.

Algorithm 3.1 Looping algorithm

Input: A full connection assignment

1: Find a not connected input terminal x and set $x_0=x$. If all input terminals are connected, exit the algorithm.

2: Connect x_0 to $\pi(x_0)$ through the *upper* middle sub-network

3: Connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *lower* middle sub-network

4: If $\sim\pi^{-1}(\sim\pi(x_0)) = x0$, go to **line 1**, else set $x_0=\sim x_1$ and go **line 2**

Figure 3.17 shows a set-up established with the looping algorithm. It is an 8×8 Clos-tree switching network. Stage 1 and Stage 3 consists of four 2×2 sub-switches. Stage 2 (middle stage) has two 4×4 tree-architecture switches, which are the middle sub-networks. It receives the connection assignment shown in Equation (3.10).

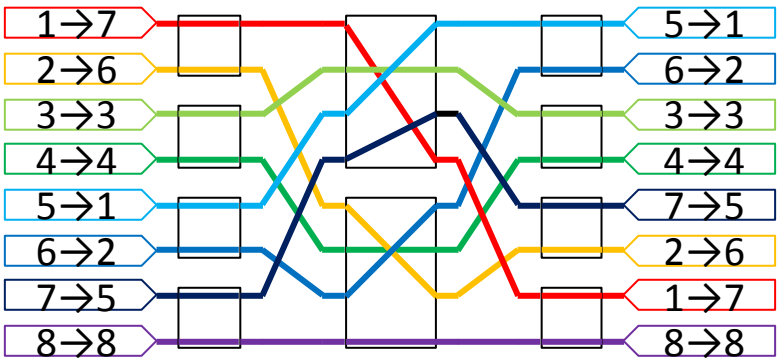

Figure 3.17 8×8 Clos-tree switch set-up

$$\Pi = \begin{pmatrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \\ 7 & 6 & 3 & 4 & 1 & 2 & 5 & 8 \end{pmatrix} \tag{3.10}$$

The looping algorithm takes three loops to set up all links in this switching network.

Loop 1: In#1→ (Upper)→ Out#7→ Out#8→ (Lower)→ In#8→ In#7→ (Upper)→ Out#5→ Out#6→ (Lower)→ In#2→ In#1

Loop 2: In#3→ (Upper)→ Out#3→ Out#4→ (Lower)→ In#4→ In#3

Loop 3: In#5→ (Upper)→ Out#1→ Out#2→ (Lower)→ In#6→ In#5

In terms of networks with rearrangeably non-blocking middle-stage sub-networks, the looping algorithm can be implemented to set up paths from the outer layer to the inner layer in a recursive way.

The looping algorithm always regulates the first link of each loop via the upper middle network. The looping algorithm was designed for electronic switches which assume that all paths are

equal. In optical circuits, the links are distinguished with each other as they consist of different length and numbers of waveguides, bends and crossings. Adopting the looping algorithm without modification in optical switches might lead to sub-optimal performance.

3.4.2 Extended Looping Algorithm

The looping algorithm for Base 2 switches can be extended to Base 2^t switches [92]. In a Base 2^t switching network, there are 2^t middle networks. Figure 3.18 shows a Base 4 switch with 16 ports. It contains four middle networks. The looping algorithm decides the link between each input/output port via one of the four middle networks.

In the middle stage (Stage 2), the sub-switch 1 and 2 are marked as the upper middle network group, the sub-switch 3 and 4 are called the lower middle network group. With a given connection assignment, the extended looping algorithm shown in Algorithm 3.2 is run to divide the total set of assignment into two parts. Each part is connected with different groups of the middle network. Then, the extended looping algorithm is applied to each part individually. In each part of the assignment, a middle network from the corresponding group is selected for each link. In this Base 2^t example, we have $2^t = 4$, $t = 2$. For a switching network with larger t, this composite procedure can be repeated until each port is assigned with a dedicated middle network.

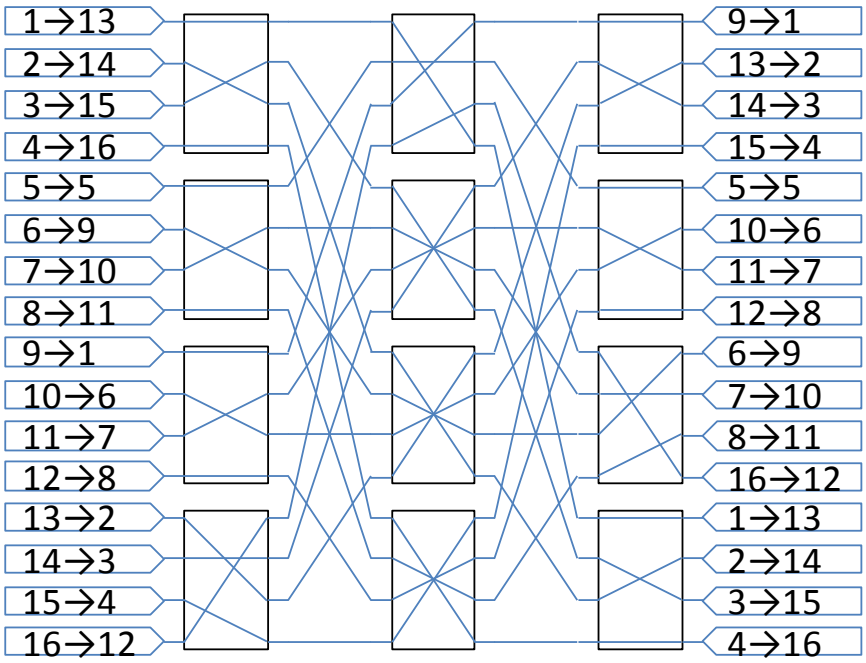

Figure 3.18 16×16 Clos-tree switch set up by the extended looping algorithm

Algorithm 3.2 Extended looping algorithm

Input: A full connection assignment

1: Find a not connected input terminal x and set $x_0=x$. If all input terminals are connected, exit the algorithm.

2: Connect x_0 to $\pi(x_0)$ through the *upper* middle network (group)

3: Connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *lower* middle network (group)

4: If $\sim\pi^{-1}(\sim\pi(x_0)) = x0$, go to **line 1**, else set $x_0=\sim x_1$ and go **line 2**

The connection assignment applied to the 16×16 Clos-tree network is given in Equation (3.11).

$$\Pi = \begin{pmatrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16 \\ 13 & 14 & 15 & 16 & 5 & 9 & 10 & 11 & 1 & 6 & 7 & 8 & 2 & 3 & 4 & 12 \end{pmatrix} \quad (3.11)$$

For the routing at the middle network group level, four loops are taken to assign input/output ports to a middle network group.

Looping at the middle network group level:

Loop 1: In#1→ (Upper Group)→ Out#13→ Out#14→ (Lower Group)→ In#2→ In#1
Loop 2: In#3→ (Upper Group)→ Out#15→ Out#16→ (Lower Group)→ In#4→ In#3
Loop 3: In#5→ (Upper Group)→ Out#5→ Out#6→ (Lower Group)→ In#10→ In#9→ (Upper Group)→ Out#1→ Out#2→ (Lower Group)→ In#13→ In#14→ (Upper Group)→ Out#3→ Out#4→ (Lower Group)→ In#15→ In#16→ (Upper Group)→ Out#12→ Out#11→ (Lower Group)→ In#8→ In#7→ (Upper Group)→ Out#10→ Out#9→ (Lower Group)→ In#6→ In#5
Loop 4: In#11→ (Upper Group)→ Out#7→ Out#8→ (Lower Group)→ In#12→ In#11

After assigning the middle network group to every port, the given assignment is also divided into two parts. Each part of the assignment is associated with a middle network group. The middle network group is then considered as a switch with the half size of the original 16×16 network. The original port numbers in the 16×16 switch are converted to new port numbers in the virtual 8×8 switches by Equation (3.12). The new port number is the least integer that is greater than or equal to the half of the original port number. The ceiling function in computer languages is used to get the number.

$$\mathrm{subN} = \lceil \mathrm{N} \rceil \tag{3.12}$$

After converting the port numbers, the algorithm is applied to each middle network group to assign a dedicated middle-stage switch to each link.

Looping within the first middle network group:
Loop 1: In#1/subIn#1→ (Upper)→ Out#13/subOut#7→ Out#15/subOut#8→ (Lower)→ In#3/subIn#2→ In#1/subIn#1
Loop 2: In#5/subIn#3→ (Upper)→ Out#5/subOut#3→ Out#7/subOut#4→ (Lower)→ In#11/subIn#6→ In#9/subIn#5→ (Upper)→ Out#1/subOut#1→ Out#3/subOut#2→ (Lower)→ In#14/subIn#7→ In#16/subIn#8→ (Upper)→ Out#12/subOut#6→ Out#10/subOut#5→ (Lower)→ In#7/subIn#4→ In#5/subIn#3

Looping within the second middle network group:
Loop 1: In#2/subIn#1→ (Upper)→ Out#14/subOut#7→ Out#16/subOut#8→ (Lower)→ In#4/subIn#2→ In#2/subIn#1

Loop 2: In#6/subIn#3→ (Upper)→ Out#9/subOut#5→ Out#11/subOut#6→ (Lower)→ In#8/subIn#3→ In#6/subIn#3

Loop 3: In#10/subIn#5→ (Upper)→ Out#6/subOut#3→ Out#8/subOut#4→ (Lower)→ In#12/subIn#6→ In#10/subIn#5

Loop 4: In#13/subIn#7→ (Upper)→ Out#2/subOut#1→ Out#4/subOut#2→ (Lower)→ In#15/subIn#8→ In#13/subIn#7

Similar to the looping algorithm for Base 2 switches, the first link of each run of the looping algorithm is always regulated via the upper middle network (group). The established set-up might lead to paths with unnecessarily large loss or crosstalk.

3.4.3 Dilated Beneš Looping Algorithm

A dilated Beneš scheme demonstrates good crosstalk performance. Dilated Beneš switches constructed entirely by dilated 2×2 building blocks and attracts much attention recently due to the ease of design and fabrication [72]. As shown in Figure 3.19, a 2×2 dilated building block contains four 2×2 switches. Although the 2×2 dilated building block has four inputs and four outputs, only one of each pair will be on at a time which means the outer input and output ports function as 1×2 and 2×1 switching elements. With this design, the crosstalk within the dilated 2×2 building blocks is negligible, enabling the scalability of optical switches.

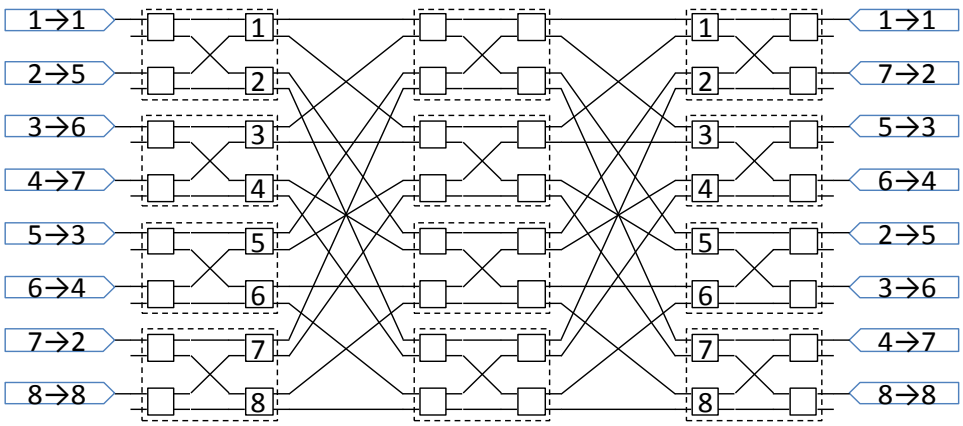

Figure 3.19 8×8 dilated Beneš switch with a given connection assignment

In order to route signals via the dilated Beneš network in a clear way, the architecture needs to be redrawn (Figure 3.20) to show a recursive architecture similar to a Base 2 switching network. As half of the dilated Beneš is a Banyan interconnection scheme, the properties of a Banyan switch also applies to the dilated Beneš scheme. Its re-packing scheme, therefore, can be used to redraw the dilated Beneš networks. Figure 3.20 is obtained by reordering sub-switches in stage 2 and 5 without changing the way switches were interconnected between themselves.

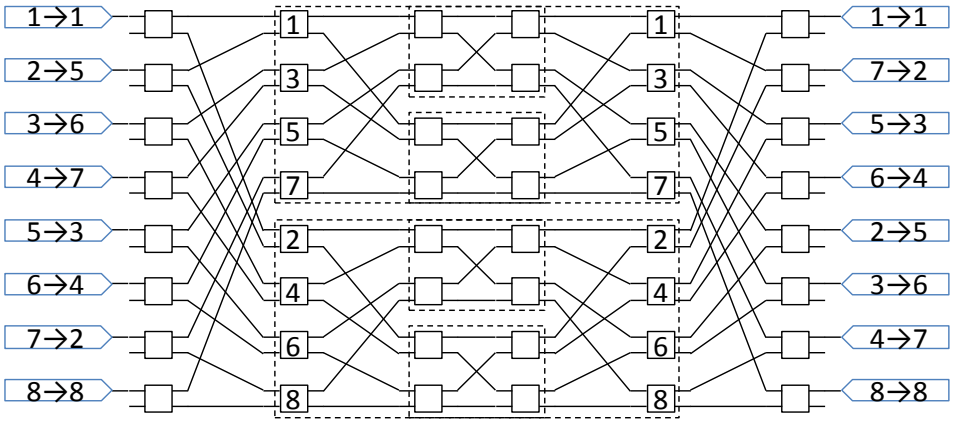

Figure 3.20 Modified 8×8 dilated Beneš switch

The routing algorithm for the dilated Beneš network is also the looping algorithm shown in Algorithm 3.1. Exactly same with the Base 2 switches, Algorithm 3.1 links the input and output ports for a N×N switch via either upper or lower middle sub-network. After selecting the middle sub-networks, the next step is to apply the algorithm recursively to set up the link within the N/2×N/2 middle networks until the 2×2 networks are reached. The previous step ensures every 2×2 switch at the input- and output-stage of the N/2×N/2 networks has only one active input and output, respectively. The two middle sub-networks therefore also have a dilated Beneš scheme. The looping algorithm is, therefore, able to be applied to the two middle networks. As the dilated Beneš network is recursively constructed, the looping algorithm is able to select links from the outer stage to the inner layer in a recursive way.

The dilated Beneš network in Figure 3.20 has the connection assignment shown in Equation (3.13).

$$\Pi = \begin{pmatrix} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \\ 1 & 5 & 6 & 7 & 3 & 4 & 2 & 8 \end{pmatrix} \tag{3.13}$$

It is 8×8 dilated Beneš network. Each of first and last stage consists of eight 1×2 or 1×2 sub-switches. 4×4 dilated Beneš sub-networks are placed at the centre stage. Firstly, the looping algorithm needs to apply to select a 4×4 sub-network for each connection.

Looping to assign path to 4×4 middle-stage sub-network

Loop 1: In#1→ (Upper)→ Out#1→ Out#2→ (Lower)→ In#7→ In#8→ (Upper)→ Out#8→ Out#7→ (Lower)→ In#4→ In#3→ (Upper)→ Out#6→ Out#5→ (Lower)→ In#2→ In#1

Loop 2: In#5→ (Upper)→ Out#3→ Out#4→ (Lower)→ In#6→ In#5

After assigning 4×4 middle-stage sub-networks to all connections, each 4×4 sub-network has its own new assignment. The algorithm is then applied again to each 4×4 network to choose a 2×2 sub-network for each connection.

Looping to assign path in the upper 4×4 middle-stage sub-network

Loop 1: In#1/subIn#1→ (Upper)→ Out#1/subOut#1→ Out#3/subOut#2→ (Lower)→ In#5/subIn#3→ In#8/subIn#4→ (Upper)→ Out#8/subOut#4→ Out#6/subOut#3→ (Lower)→ In#3/subIn#2→ In#1/subIn#1

Looping to assign path in the lower 4×4 middle-stage sub-network

Loop 1: In#2/subIn#1→ (Upper)→ Out#5/subOut#3→ Out#7/subOut#4→ (Lower)→ In#4/subIn#2→ In#2/subIn#1

Loop 2: In#6/subIn#3→ (Upper)→ Out#4/subOut#2→ Out#2/subOut#1→ (Lower)→ In#7/subIn#4→ In#6/subIn#3

After assigning a dedicated 4×4 and 2×2 sub-network to each connection, the set-up is established in the modified 8×8 dilated Beneš network shown in Figure 3.20. The building blocks are then reordered with the defined bar or cross state to building the set-up for the given layout. The final set-up for the dilated Beneš network is shown in Figure 3.21.

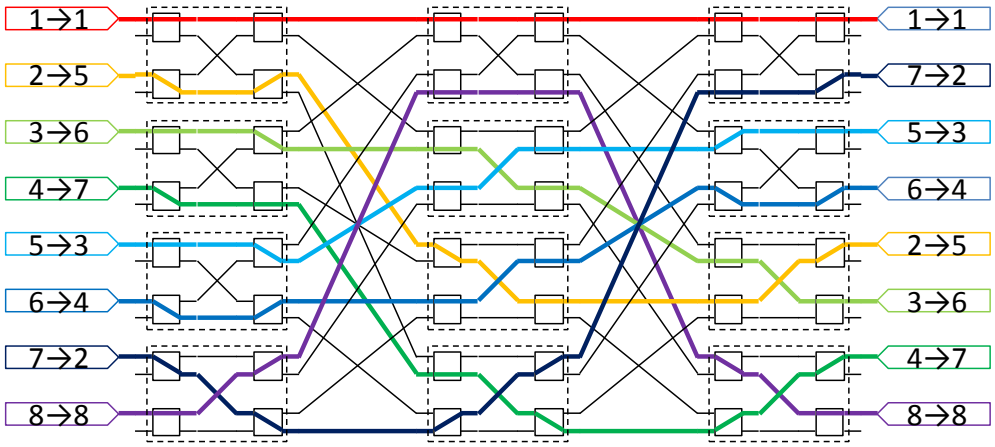

Figure 3.21 8×8 dilated Beneš switch set up by the looping algorithm

3.4.4 Conclusions

Multi-stage architectures require routing algorithms to select the middle-stage sub-networks to set up paths for the given connection assignments. Path searching algorithms are straightforward methods to find the available middle-stage sub-switches for connections. They are vulnerable with rearrangeably non-blocking architecture and might be ended up with a blocking state.

Routing algorithms for rearrangeably non-blocking architectures have been proposed to consider the entire given connection assignment and set up all links together, avoiding the blocking state.

The looping algorithm is the classical routing algorithm which has been proposed for Base 2 switches. Beneš architectures along with Clos architectures with 2×2 sub-switches at first- and last-stage can be applied to the looping algorithm. It has also been extended to Base 2^t switches. The dilated Beneš networks also can be set up with the looping algorithm by modifying the network layout. The computational complexity of these algorithms is summarised in Table 3.2.

Table 3.2 Summary of routing algorithms [91][94][72]

Algorithm	**Computational Complexity for a Single Level**	**Computational Complexity for the Whole Switch***
Looping Algorithm for N×N Base 2	$O(N)$	$O(N \times (\log_2 N - 1))$
Looping Algorithm for N×N Base 2^t	$O(N \times t)$	$O(N \times (\log_{2^t} N - 1))$
Looping Algorithm for N×N dilated Beneš	$O(N)$	$O(N \times (\log_2 N - 1))$

*The switch is entirely constructed by 2×2 or $2^t \times 2^t$ sub-switches

A common issue for the looping algorithm and its modified versions is that they always regulate the first link of each loop via the upper middle network. It works well with electronic networks as all links are equal. With integrated optical networks, links have different losses from waveguides, bends and crossings. The set-up established by the looping algorithm might lead to paths with an unnecessarily large loss, which comes with sub-optimal performance. These algorithms are then modified to explore all possible set-ups for a given connection assignment and choose the optical one. These modified algorithms have been proposed within this thesis and are discussed in details in Chapter 4.

Chapter 4 Advanced Routing Algorithms

4.1 Introduction

Large-scale high-speed optical switches usually compensate for the loss of waveguides, splitters and combiners with optical amplification so that the switches can operate nearly lossless. Multi-stage rearrangeably non-blocking architectures are widely adopted for large-scale optical switches. Several alternative paths can be set up between a pair of input and output in non-blocking architectures.

Consideration of the chosen route of any signal through the switch is thus important. Unnecessarily long paths through the switch can increase the optical losses of waveguides, crossings and bends which must be compensated for by increasing optical gain, at the expense of increased ASE noise. Mitigating the unnecessarily long paths in the switch can improve the output optical signal quality and enlarge the input power dynamic range (IPDR).

The looping algorithm has been proposed to set-up paths for a given connection assignment. It was born in the electronic switch era, where all links in the switches are equal. It does not accommodate loss difference between optical paths due to the different length of waveguides and varying numbers of crossings and bends and thus will lead to a sub-optimal performance in terms of output OSNR and Q factor. It, therefore, is necessary to update the looping algorithm to adapt for the physical variations in optical switches. Several modified looping algorithms were proposed to reduce the time taken for this process [93][94], to optimize crosstalk performance [95] and to self-route the switch [96]. However, to our knowledge, no algorithm has been designed specifically to optimize the path loss and IPDR.

In this chapter, we, therefore, propose an advanced path-selection algorithm based on the looping algorithm that minimizes the path-dependent variation. It explores all possible set-ups with a given connection assignment and selects the optimal one [97]. It guarantees that no

individual path would have a sufficiently considerable loss, therefore, improve the overall performance of the switch. The advanced routing algorithm has also been extended to Base 2^t switches and dilated Benes switches. The implementation methods for each advanced routing algorithm are also discussed in this chapter.

4.2 Advanced Looping Algorithm for Base 2 Switches

The looping algorithm always regulates the first link of each loop via the upper middle network regardless of the loss of the paths. Figure 4.1(a) is a simplified schematic of the switch (even the schematic is symmetric, the layout of the switch is more complicated and not symmetric). shows the links established by the looping algorithm in an 8×8 Clos-tree switch with the given connection assignment shown in Equation (3.10) [98]. The steps in the looping algorithm and the given connection assignment are explained in detail in Chapter 3.4.1.

Figure 4.1(b) shows the set-up in an integrated optical switch. The bends, crossings and different length waveguides can be clearly seen in the layout of the integrated optical switch. The bold dark blue link from In#7 to Out#5 shows the worst case. This path, however, requires a higher level of gain from the cascaded SOAs, which in turn reduces the optical signal to noise ratio (OSNR) due to the additionally induced ASE noise.

In order to avoid those unnecessary long paths with a large loss, an advanced routing algorithm has been proposed to search for an optimal set-up with the minimized path-dependent loss. Basically, the advanced routing algorithm is a modified looping algorithm, exploring all possible set-ups by linking the first connection in each loop via either upper or lower middle network. It then finds the optimal set-up by considering the all path loss in the integrated optical switch.

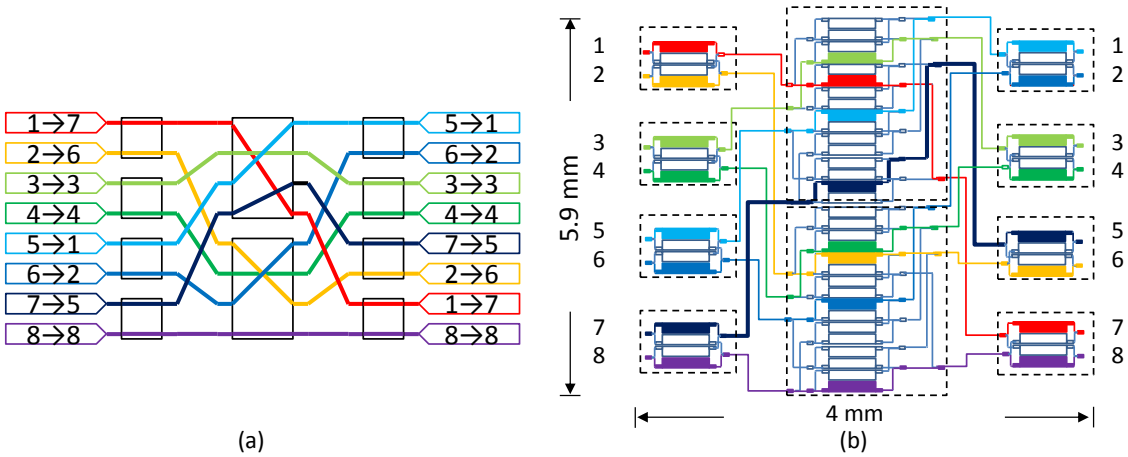

Figure 4.1 8×8 Switch set up by the looping algorithm shown in (a) schematic (b) layout

The steps of the advanced routing algorithm are shown in Algorithm 4.1. The first part of it is the looping algorithm. The looping algorithm is run to calculate how many loops are required to set up the switch for the given connection assignment. The number of loops is denoted by L. As the first link in each loop can be established via either the upper or lower middle switch. The total number of all possible set-ups is 2^L, which is denoted by *SetUp* as shown in Equation (4.1).

$$\mathrm{SetUp} = 2^{\mathrm{L}} \tag{4.1}$$

Then, the detailed link arrangement of each setup is created by enumerating all possible set-ups by establishing the first connection via either the upper or lower middle switch. Each set-up is assigned a number from 0 to *SetUp-1*. The number is then converted to an L-digit binary number to utilise the nature of binary number to mark the state of the first link for each of the L loops. The binary number is denoted as *sBinary*. *sBinary* is labelled from the most significant bit (MSB) to the least significant bit (LSB) as *sBinary[1]* to *sBinary[L]*. If the bit is 0, the loop links the first connection via the upper middle network. If the bit is 1, the first connection of that loop is via the lower middle network. All possible set-ups can be constructed by linking each loop according to *sBinary*. The algorithm can be implemented recursively to rearrangeably non-blocking sub-networks in the inner layer to explore all possible set-ups in a similar way.

Algorithm 4.1 Advanced routing algorithm

Input: A full connection assignment

1: Set L=0

2: Find a not connected input terminal x and set x_0=x. If all input terminals are connected, go the **line 6**.

3: Connect x_0 to $\pi(x_0)$ through the *upper* middle sub-network

4: Connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *lower* middle sub-network

5: If $\sim\pi^{-1}(\sim\pi(x_0)) = x0$, increase L by 1 and go to **line 2**, else set x_0=$\sim x_1$ and go the **line 3**.

6: $SetUp$=2^L

7: Set s = 0

8: Reconstruct the links

9: Convert s from decimal to an L-digit Binary number *sBinary*

10: Label *sBinary* from MSB to LSB as *sBinary[1]* to *sBinary[L]*

11: Set b = 1

12: Find a not connected input terminal x and set x_0=x.

13: if *sBinary [b]* = 0, then Connect x_0 to $\pi(x_0)$ through the *upper* middle sub-network and connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *lower* middle sub-network

14: if *sBinary [b]* = 1, Connect x_0 to $\pi(x_0)$ through the *lower* middle sub-network and connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *upper* middle sub-network

15: If $\sim\pi^{-1}(\sim\pi(x_0)) \neq x_0$ set x_0=$x_1$and go the **line 13**.

16: If $\sim\pi^{-1}(\sim\pi(x_0)) = x_0$, increase b by 1.

17: If $b > L$, go to **line 18**, else go to **line 12**.

18: Save the set-up, reconstruct the link, and increase s by 1.

19: If $s \geq SetUp$, exit the algorithm, else got the **line 8**.

After creating all set-ups for the connection assignment, the optimal set-up for a given integrated switch design is evaluated by a weighting mechanism. Three possible selections are considered.

- Accepting an outcome if the maximum unamplified path loss is below a threshold value
- Computing the root mean square path loss for all states and choosing the lowest outcome
- Examine the maximum individual path loss in each set of connections and choosing the connection set which exhibits the lowest overall maximum individual path loss.

This last option has been chosen to guarantee that no individual path would have an extremely large loss.

4.2.1 Evaluation Model

A comprehensive layout with various lengths of waveguides and numbers of crossings and bends are adopted here to evaluate the advanced routing algorithm. Physical-layer parameters (Table 4.1) measured in the experiments [99][100] are used to calculate the path loss.

Table 4.1 Loss parameters

Component	Loss
Waveguide	8 dB/cm
Crossing	0.2 dB
Bend	0.5 dB
MMI Coupler	0.5 dB
Transition Element	1 dB

A path between an input port and an output port consists of five parts.

- Path within a 2×2 input-stage sub-switch
- First shuffle network between input-stage sub-switches and middle-stage sub-switches
- Path within a 4×4 middle-stage sub-switch
- Second shuffle network between output-stage sub-switches and middle-stage sub-switches

- Path within a 2×2 output-stage sub-switch

The path-loss difference within the 2×2 sub-switch is negligible. The passive components in 2×2 sub-switch introduce 7.64 dB regardless of the bar or cross state. The losses in the first and second shuffle network are calculated (Table 4.2&Table 4.3). The loss introduced by passive components in 4×4 middle-stage sub-switch is shown in Table 4.4.

Table 4.2 Loss of the first shuffle network [dB]

	Upper Middle-stage Sub-Switch	**Lower Middle-stage Sub-Switch**
First-Stage Sub-Switch #1	1.7	4.4
First-Stage Sub-Switch #2	2	3.3
First-Stage Sub-Switch #3	3.1	2.2
First-Stage Sub-Switch #4	3.6	1.7

Table 4.3 Loss of the second shuffle network [dB]

	Upper Middle-stage Sub-Switch	**Lower Middle-stage Sub-Switch**
Last-Stage Sub-Switch #1	1.8	3.7
Last-Stage Sub-Switch #2	2.9	2.6
Last-Stage Sub-Switch #3	3.9	1.7
Last-Stage Sub-Switch #4	3.9	1.5

Table 4.4 Passive loss within middle-stage 4×4 sub-switch [dB]

	Out#1	**Out#2**	**Out#3**	**Out#4**
In #1	17	16.2	16.1	17.4
In #2	18.5	17.4	17.3	18.3
In #3	18.2	17	19.7	16.3
In #4	21.4	19.8	19.3	15.5

All possible set-ups and their path losses for this layout are then evaluated. It requires three loops to set up the all the links, L=3, as discussed in Chapter 3. The total number of set-ups, *SetUp,* is therefore 2^L=8. Algorithm 4.1 enumerates connections for each set-up. All path losses

for each set-up are calculated with the above physical-layer parameters. The maximum individual path loss in each set-up is examined. The optimal set-up is then chosen from these 8 options (Figure 4.2). The unnecessarily long path (bold dark blue link) in Figure 4.1 is avoided in the optimal set-up. The path with the overall maximum individual path loss in the optimal set-up has been minimized.

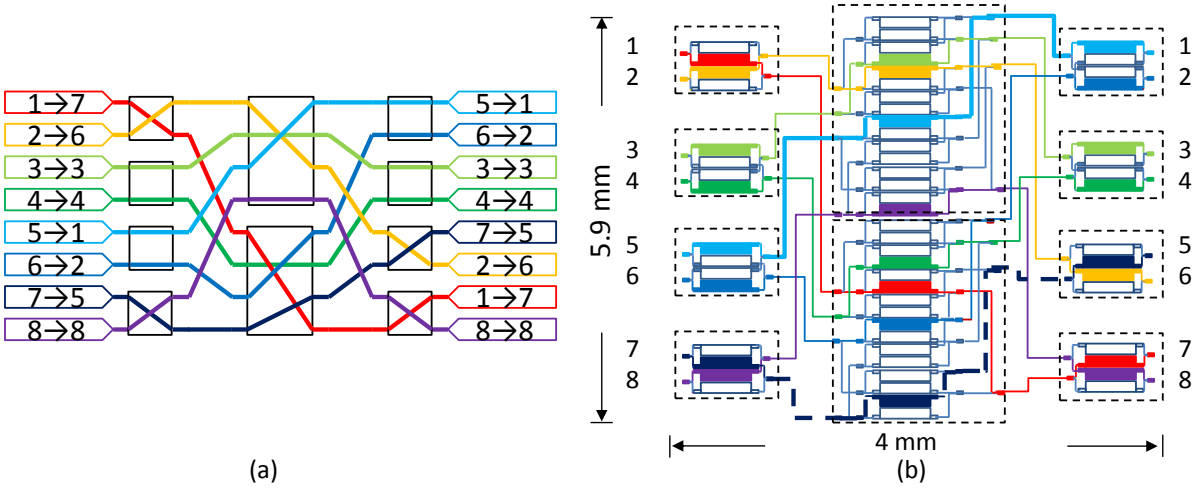

Figure 4.2 8×8 Switch set up by the advanced routing algorithm shown in (a) schematic (b) layout

4.2.2 Look-up Table Approach

The computational complexity of the chosen algorithm is $O(2^L \times N)$, where N is the network size. It, however, requires high-speed processor if we use on-the-fly computation. Running the advanced routing algorithm off-line and storing its output of each assignment in a look-up table can enable fast switch reconfiguration.

The size of the look-up table, however, inevitably increases exponentially with the number of the inputs of the switching network. In this switch with 8×8 port count, there are 8! = 40320 possible full connection assignments. The size of the look-up table will be a practical issue.

In order to reduce the size of the look-up table, a permutation matrix method is adopted here. We use a matrix with r rows and r columns (r is the number of the first-/last-stage sub-switches as explained in Chapter 3) to represent the connections in a connection assignment (Table 4.5)

[cite Neiman]. Rows and columns correspond to the first- and last-stage sub-switches. The matrix is defined as Equation (4.2).

$$H_r^{(d)} = \left[h_{i,j} = \begin{cases} k, & \text{if there are k connections between subSwtiches} \\ 0, & \text{if there is no connection between subSwitches} \end{cases} \right] \tag{4.2}$$

Here, rather than considering the connections between input and output ports, we consider the connections between input- and output-stage sub-switches. The maximal number of connections between two sub-switches is equal to the number of inputs of a sub-switch. Table 4.5 shows the connection matrix for the given assignment shown in Figure 4.2.

Table 4.5 Connection matrix between first-/last-stage sub-switches

	Last-stage Sub-switch #1	**Last-stage Sub-switch #2**	**Last-stage Sub-switch #3**	**Last-stage Sub-switch #4**
First-stage Sub-switch #1	0	0	1	1
First-stage Sub-switch #2	0	2	0	0
First-stage Sub-switch #3	2	0	0	0
First-stage Sub-switch #4	0	0	1	1

We only consider full connection assignments where all inputs and outputs are engaged for the algorithms in this chapter. This is sufficient since these states include all others. The connection matrix of a full connection assignment has the following characteristics shown in Equation (4.3) and Equation (4.4).

$$\sum_{i=1}^{r} H[i;j] = d \tag{4.3}$$

$$\sum_{j=1}^{r} H[i;j] = d \tag{4.4}$$

The sum of any row or column is the number of inputs of a sub-switch, d. All possible connection matrixes then can be enumerated. The number of all possible connection matrixes is much smaller than the connection assignments. Taking the 8×8 Clos-tree switch as an example, the number of connection matrixes is 282 while the number of connection assignments is 40320.

In 2×2 sub-switches, such as the first-/last-stage sub switches in this design, the loss difference between the bar and cross connection are negligible compared with the loss in the shuffle networks between stages. Therefore, the assignments, which share the same connection matrixes, can be grouped together. Since first- and last-stage sub-switches are non-blocking, it is sufficient to say the connection is set up between two sub-switches.

This method dramatically cuts the size from the look-up table from 8! =(40320) to 282. It is therefore practical to adopt an off-line algorithm and a look-up to enable fast reconfiguration.

4.2.3 Loss and Power Penalty Evaluation

These advanced routing algorithms for different switch architectures have been evaluated by examining the loss reduction of the link with overall maximum individual path loss. The loss difference between the best set-up and the worst set-up of all connection matrixes is shown in Figure 4.3.

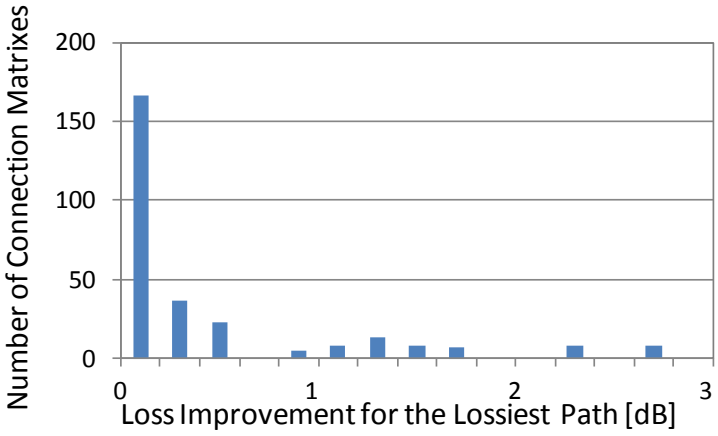

Figure 4.3 The loss improvement for the lossiest path for the 8×8 Clos-tree switch

Figure 4.3 shows the loss improvement of the lossiest path for all 282 connection matrixes between input- and output-stage sub-switches in the 8×8 Base 2 switch. Those 282 connection matrixes contain all possible connection assignments between individual input and output ports. Although most switch connection maps are not significantly changed by the algorithm, eight have a loss reduction exceeding 2.7dB, which is very significant with this switch design.

The example discussed in Figure 4.1 and Figure 4.2 has one of those eight connection matrixes. The worst-case path (In#7 to Out#5) with 42.1dB loss shown by the bold dark link in Figure 4.1 has been avoided. The path with the maximal individual loss (In#6 to Out#2) in Figure 4.2 has 31.8 dB loss, 2.7 dB lower than the set-up from the original routing algorithm.

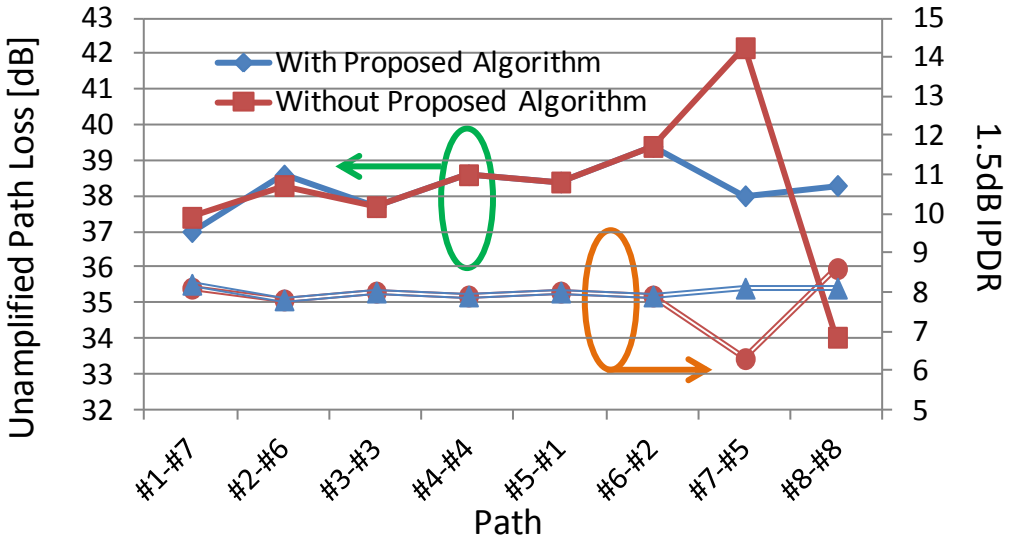

Figure 4.4 Detailed loss and IPDR of each path for the set-ups shown in Figure 4.1 and Figure 4.2

The optical performance improvement for this connection map has been evaluated by simulating IPDR (Input Power Dynamic Range) for all paths with and without the algorithm using the photonic simulation software VPI. The performance of link is marked by the IPDR with a penalty less than a certain value. The power penalty is the difference of the power required at the receiver to achieve a constant 10^{-9} BER in the presence and absence of the switch is the power penalty. More information about IPDR is discussed in Chapter 5.3.3. The simulation applies a 10Gbps NRZ (Non-Return to Zero) injected optical signal and an injection current of 30mA for all SOA elements. Figure 4.4 shows the loss and IPDR improvement for

each path. The average path performance doesn't see much improvement because the weighting mechanism adopted here is to minimise the maximum individual path loss in order to guarantee that no individual path would have an extremely outstanding large loss and bad performance. The path #In7-Out#5 with overall smallest IPDR has been avoided. With the proposed advanced routing algorithm, the new lossiest path In#6-Out#2 show 1.9dB IPDR improvement for power penalties less than 1.5dB, which means within a range of 1.9 dB in terms of input power, the power penalty of the link is below 1.5 dB. The loss variation among all paths is less than 2.4 dB. The IPDR values for all paths differ by less than 0.4dB.

4.3 Advanced Looping Algorithm for Base 2^t Switches

Figure 4.5 shows the set-up established by the extended looping algorithm. Similar to the looping algorithm for Base 2 switches, as the first link of each run of the looping algorithm is always regulated via the upper middle network (group), the established set-up might lead to paths with unnecessarily large losses. Here the bold purple path from In#16 to Out#12 has the greatest passive component losses caused by the broadcast-and-select splitters, long waveguides, bends and crossings.

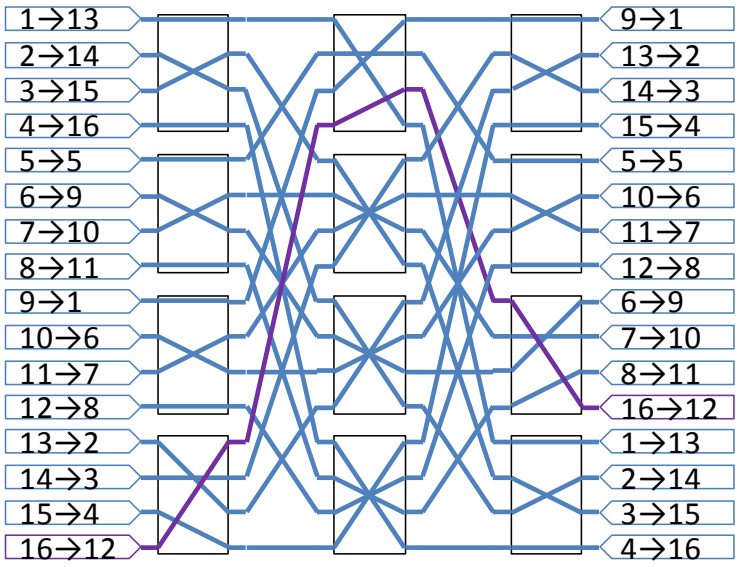

Figure 4.5 Unnecessary long path in a 16×16 Clos-tree switch set up by the extended looping algorithm

The advanced routing algorithm is then proposed to explore all possible set-ups and find the optimal set-up with minimized path-dependent loss [101]. Unlike the extended looping algorithm, four middle-stage switches are not divided into the upper middle switch group and the lower switch group. All possible combinations of switch groups have been explored to ensure any middle switch is put in the same group with any other middle switch. Additionally, the first connection in each loop is regulated via both possible middle switches (switch groups).

Figure 4.6 shows the flowchart of the algorithm for Base 4 networks. The Algorithm 4.2 is first applied to enumerate all possible set-ups between two middle-stage switch groups. Then, within each group of the middle networks, the Algorithm 4.2 is applied again to enumerate all possible set-ups. The constituents of each middle-stage switch group are then defined. There are three possible cases as shown in Table 4.6. All combinations of the set-up of two parts of networks are then enumerated to explore all possible set-ups of the whole network. For Base 2^t switches with a larger value of t, this composite procedure can be repeated until each port is assigned with a dedicated middle switch.

Table 4.6 Middle-stage group constituents [dB]

	1st Middle-stage Group	**2nd Middle-stage Group**
Case 1	Switch 1 & 2	Switch 3 & 4
Case 2	Switch 1 & 3	Switch 2 & 4
Case 3	Switch 1 & 4	Switch 2 & 3

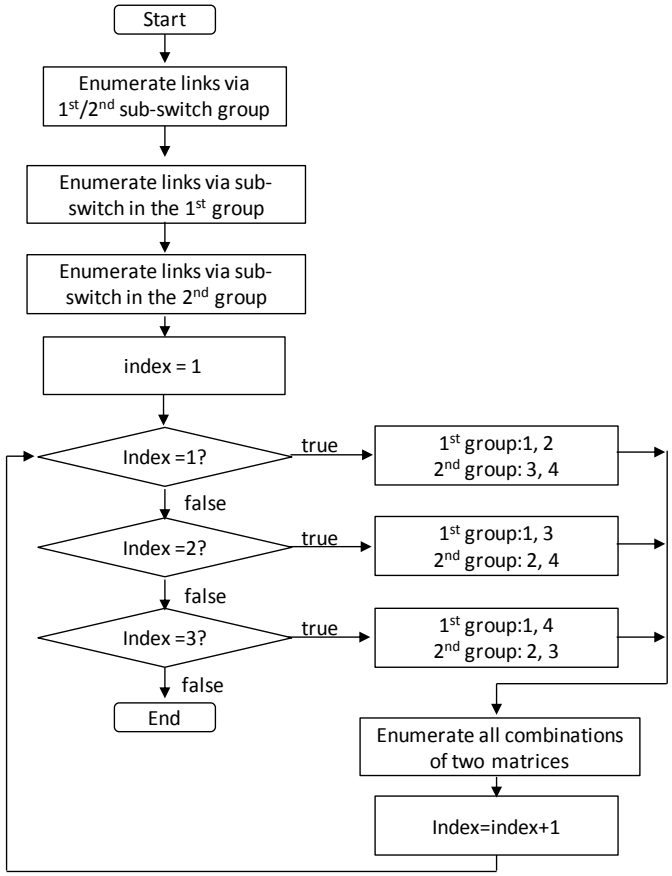

Figure 4.6 Flowchart of the algorithm for Base 4 switches

Algorithm 4.2 Advanced routing algorithm

Input: A full connection assignment

1: Set L=0

2: Find a not connected input terminal x and set x_0=x. If all input terminals are connected, go the **line 6**.

3: Connect x_0 to $\pi(x_0)$ through the *1st* middle network (group)

4: Connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *2nd* middle network (group)

5: If $\sim\pi^{-1}(\sim\pi(x_0)) = x0$, increase L by 1 and go to **line 2**, else set x_0=$\sim x_1$ and go the **line 3**.

6: $SetUp$=2^L

7: Set s = 0

8: Reconstruct the links

9: Convert s from decimal to an L-digit Binary number *sBinary*

10: Label *sBinary* from MSB to LSB as *sBinary[1]* to *sBinary[L]*

11: Set $b = 1$

12: Find a not connected input terminal x and set $x_0=x$.

13: if *sBinary [b]* = 0, then Connect x_0 to $\pi(x_0)$ through the *1st* middle network (group) and connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *2nd* middle network (group)

14: if *sBinary [b]* = 1, Connect x_0 to $\pi(x_0)$ through the *1st* middle network (group) and connect $\sim\pi(x_0)$ to $\pi^{-1}(\sim\pi(x_0))$ through the *2nd* middle network (group)

15: If $\sim\pi^{-1}(\sim\pi(x_0)) \neq x_0$ set $x_0=x_1$and go the **line 13**.

16: If $\sim\pi^{-1}(\sim\pi(x_0)) = x_0$, increase b by 1.

17: If $b > L$, go to **line 18**, else go to **line 12**.

18: Save the set-up, reconstruct the link, and increase s by 1.

19: If $s \geq SetUp$, exit the algorithm, else got the **line 8**.

4.3.1 16×16 Evaluation Model

In terms of the connection assignment shown in Figure 4.5, this requires four loops, L=4, to assign middle switching network groups each terminal. The total number of set-ups at middle-switching-network-group level is therefore 2^L=16 according to Equation (4.1).

For each group, the Algorithm 4.2 is applied again to explore all set-ups. The total number of set-ups in this Base 4 switch is calculated by Equation (4.5). *L_1stGroup* and *L_2ndGroup* represent the number of loops required within the 1st and 2nd group, respectively. These two numbers vary with the set-ups at middle-switching-network-group level. Within each set-up at the switch-group level, there are three possible combinations of middle switching network group as shown in Table 4.6.

Table 4.7 shows the detailed calculation of the total set-ups for the given assignment.

$$set\_up = \sum_{s=1}^{2^L} (3 \times 2^{L\_1stGroup} \times 2^{L\_2ndGroup}) \quad (4.5)$$

Table 4.7 Total number of set-ups [dB]

#Set-up (Group Level)	$2^{L\_1stGroup}$	$2^{L\_2ndGroup}$	Combinations (=$3\times2^{L\_LOWER}\times2^{L\_upper}$)
#1	4	16	192
#2	4	16	192
#3	16	4	192
#4	16	4	192
#5	4	16	192
#6	4	16	192
#7	16	4	192
#8	16	4	192
#9	4	16	192
#10	4	16	192
#11	16	4	192
#12	16	4	192
#13	4	16	192
#14	4	16	192
#15	16	4	192
#16	16	4	192
Total			3072

There are 3072 set-ups for the given connection assignment. The optimal set-up with lowest overall maximum individual path loss is then selected based on the layout of the switch. A comprehensive 16×16 layout (Figure 4.7) is adopted here to evaluate the performance of the advanced algorithm. Physical-layer parameters shown in Table 4.1 are used to calculate the loss of each path.

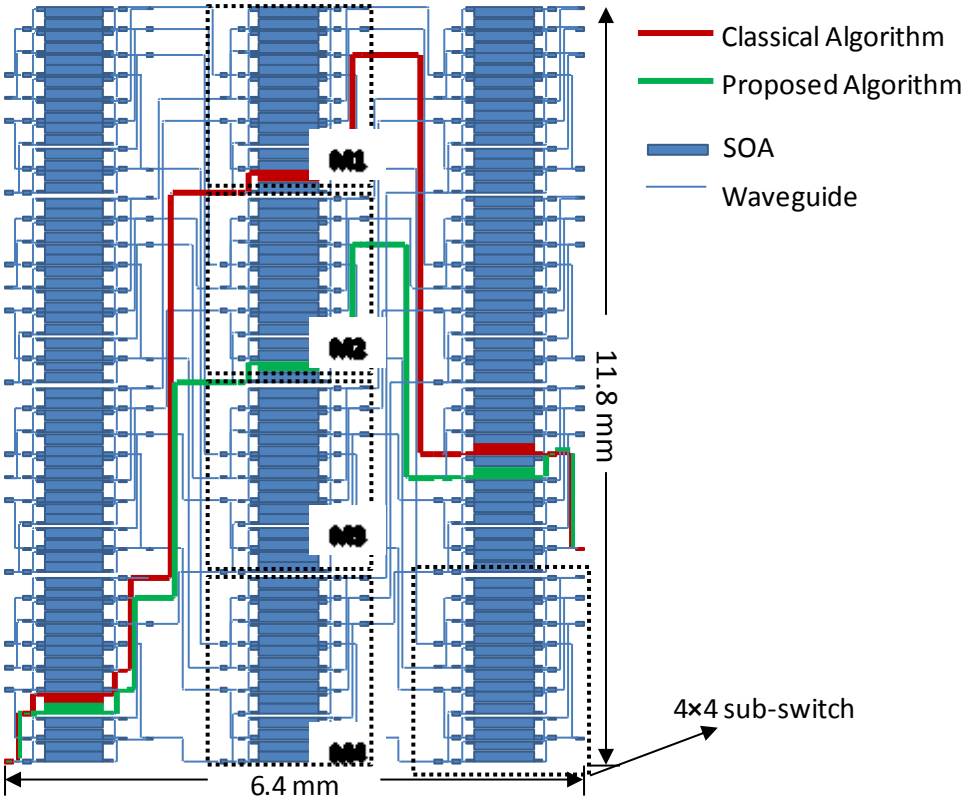

Figure 4.7 Layout of a 16×16 Clos-tree switch with the worst-case path set up by the looping algorithm and the advanced routing algorithm

A path between a pair of input and output terminals consists of five parts.

- Path within a 4×4 input-stage sub-switch
- Shuffle network between input-stage sub-switches and middle-stage sub-switches
- Path within a 4×4 middle-stage sub-switch
- Shuffle network between and middle-stage sub-switches and output-stage sub-switches
- Path within a 4×4 output-stage sub-switch

The losses in the two shuffle networks are identical (Table 4.8). The loss introduced by passive components in 4×4 middle-stage sub-switch is same with the 4×4 switches shown Table 4.4.

Table 4.8 Loss of the shuffle network [dB]

	Middle-stage Switch #1	**Middle-stage Switch #2**	**Middle-stage Switch #3**	**Middle-stage Switch #4**
First-stage Sub-switch #1	2.6	5.2	7.8	9.3
First-stage Sub-switch #2	3.6	3.4	5.6	6.7
First-stage Sub-switch #3	6.2	3.9	3.3	4
First-stage Sub-switch #4	8.3	5.6	2.9	1.9

The computational complexity of the algorithm is O(*SetUp*×N). Running the algorithm off-line and storing the optimal set-up for each assignment is also a practical way to enable fast reconfiguration. There are, however, 16! = 20.9 trillion possible full connection assignments between input and output terminals.

The size of the look-up table can be reduced by using the permutation matrix method discussed in Section 4.2.2. By considering the connections between input- and output-stage 4×4 switches, the size of the look-up table is trimmed to 10147. If the path-dependent loss within the input- and output-stage 4×4 sub-switches is much smaller than the path-dependent loss within the shuffle network, the permutation matrix can be adopted. This method is best suited for switches with small-scale input- and output-stage sub-switches. For networks with large-scale input- and output-stage sub-switches, on-the-fly computation might be necessary.

Figure 4.8 shows the optimal set-up established by the advanced routing algorithm by comparing the path loss between input- and output-stage 4×4 sub-switches. The unnecessarily long path with 35.5 dB loss between In#16 and Out#12 in Figure 4.5 has been avoided. The newly established path between In#16 and Out#12 is marked as a dashed purple line in Figure 4.8. The path with the overall maximum individual loss in this new set-up is between In#14 and Out#3 (solid green line), which has a reduced 32.3 dB loss compared to the original set-up.

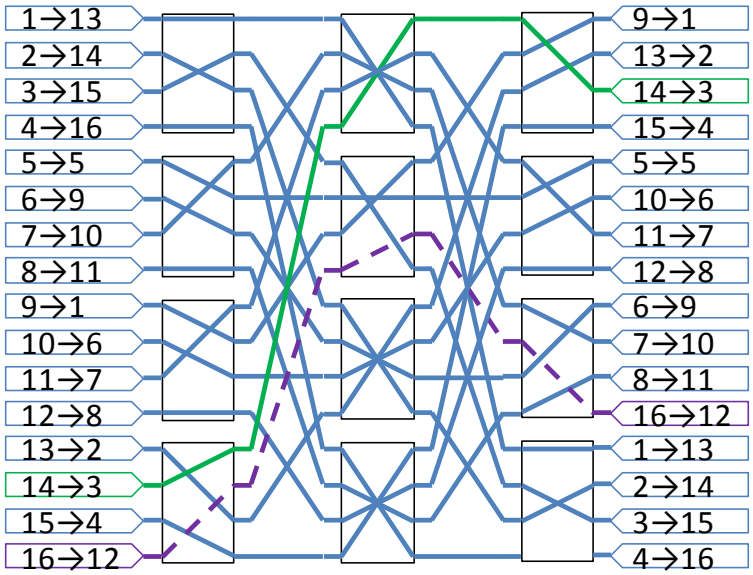

Figure 4.8 16×16 Clos-tree switch set up by the advanced routing algorithm

This advanced routing algorithm is also evaluated by examining the loss improvement for the link with overall maximum individual path loss. Figure 4.9 shows the loss improvement of the lossiest path for all 10147 connection matrixes between input- and output-stage sub-switches in the 16×16 Base 4 switch. Those 10147 connection matrixes contain all possible connection assignments between individual input and output terminals. Around 2000 connection maps have a significant loss reduction exceeding 3dB.

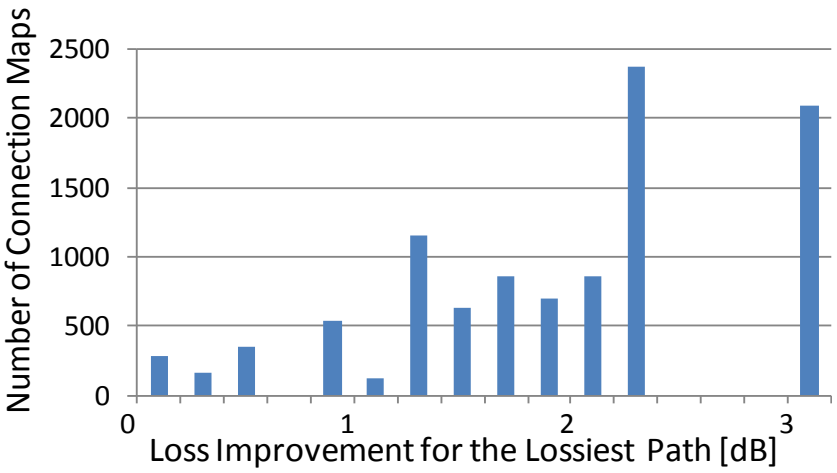

Figure 4.9 The loss improvement for the lossiest path for the 16×16 Clos-tree switch

The example discussed in Figure 4.5 and Figure 4.8 has one of those 2000 connection matrixes. A 3.15 dB loss improvement has been demonstrated for the path with the maximum individual loss. Figure 4.10 shows the loss of each path for two set-ups.

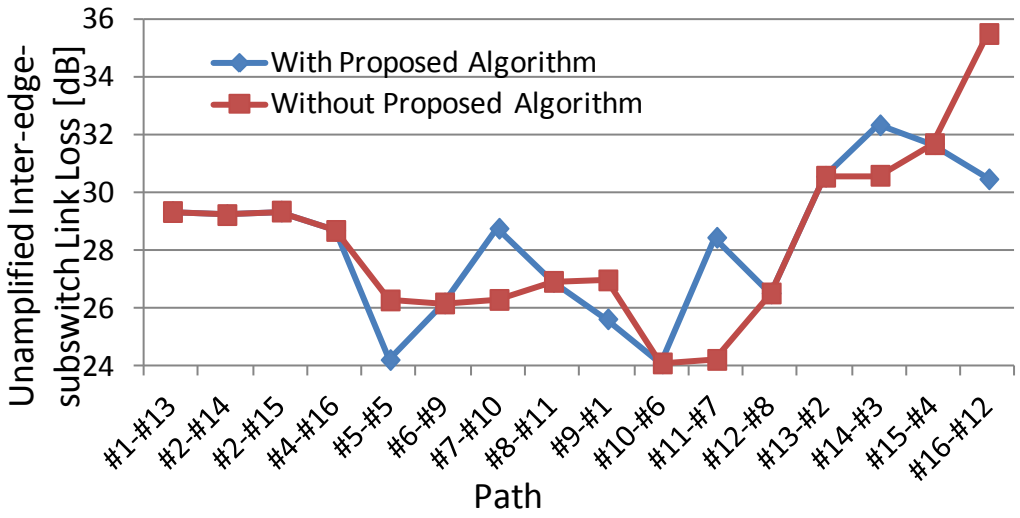

Figure 4.10 Detailed loss of each path (between first- and last-stage sub-switches) for the set-ups shown in Figure 4.5 and Figure 4.8

However, in this switch design, this loss improvement between the input- and output-stage sub-switches is of the same magnitude with the loss difference within 4×4 sub-switches (2.6 dB variance). Therefore, considering the loss improvement between the input- and output-stage sub-switches is not sufficient with this switch design, computing the loss between individual terminals is necessary in this case.

4.4 Advanced Looping Algorithm for Dilated Beneš Switches

Figure 4.11 shows a dilated Beneš switch set up by the looping algorithm. The details of the Algorithm and explanation are described in Section 3.4.3. Similar to Base 2 and Base 2^t switches, the classical looping algorithm might lead to unnecessarily long paths. The link between In#8 and Out#8 is routed via a sub-optimal middle-stage switch in this set-up.

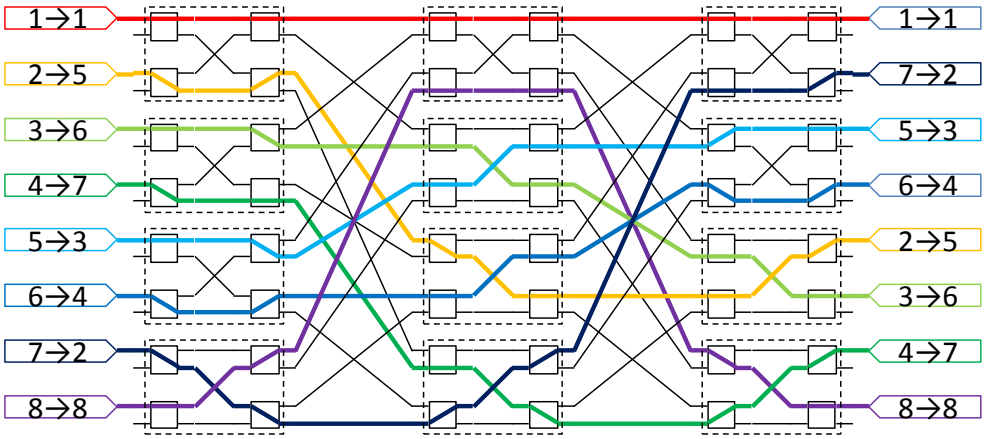

Figure 4.11 8×8 dilated Beneš switch set up by the looping algorithm

In order to estimate the performance of routing algorithms for dilated Beneš switches, we propose a hybrid component method for this dilated Beneš scheme as shown in Figure 4.12. Both Mach-Zehnder Interferometers (MZIs) and Semiconductor Optical Amplifiers (SOAs) are included in a 2×2 sub-switch. Here, MZIs are used as the main switching elements. Both outputs of an MZI are linked to short SOA components. Once the signal is routed to an output, the corresponding SOA is turned on in order to compensate for the loss from other passive components. The SOA connected to the other output is in the OFF state and suppresses crosstalk.

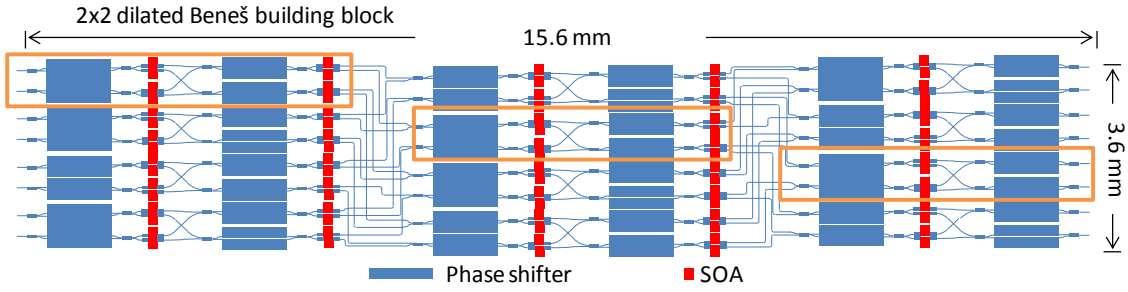

Figure 4.12 Layout of a8×8 Dilated Beneš switch

Physical-layer parameters shown in Table 4.1 are also used to calculate the loss of each path. A path between any input port and any output consists of five parts.

- Path within a 2×2 input-stage dilated Beneš building block
- First shuffle network between the input stage and the middle stage

- Path within a 2×2 middle-stage dilated Beneš building block
- Second shuffle network between the middle stage and the output stage
- Path within a 2×2 output-stage dilated Beneš building block

The loss within a 2×2 dilated Beneš building block is 11.7 dB in the bar state and 12.4 dB in the cross state. Table 4.9 and Table 4.10 show the path loss within the first and second shuffle network.

Table 4.9 Loss of the first shuffle network [dB]

	Middle-stage Switch #1	**Middle-stage Switch #2**	**Middle-stage Switch #3**	**Middle-stage Switch #4**
First-stage Sub-switch #1	1.5	2.9	4.2	5.7
First-stage Sub-switch #2	3.3	3	3.2	4.1
First-stage Sub-switch #3	4.4	3.3	2.6	2.8
First-stage Sub-switch #4	6.2	4.5	3.2	1.6

Table 4.10 Loss of the second shuffle network [dB]

	Middle-stage Switch #1	**Middle-stage Switch #2**	**Middle-stage Switch #3**	**Middle-stage Switch #4**
First-stage Sub-switch #1	1.6	3.2	4.5	6.2
First-stage Sub-switch #2	2.8	2.6	3.3	4.4
First-stage Sub-switch #3	4.1	3.2	3	3.3
First-stage Sub-switch #4	5.7	4.2	2.9	1.5

The advanced routing algorithm in Algorithm 4.1, therefore, is used to explore all possible set-ups by enumerating all possible links from outer stages to inner layers and find the optimal set-up with the minimised path-dependent loss.

The total number of set-ups in this Base 4 switch is calculated by Equation(4.6). L is the number of loops required to determine the first-level middle sub-network. L_upper and L_lower

represent the number of loops required within upper and lower sub-network, respectively. These two numbers vary with the set-ups at first level.

$$set\_up = \sum_{s=1}^{2^L} (2^{L\_upper} \times 2^{L\_lower}) \tag{4.6}$$

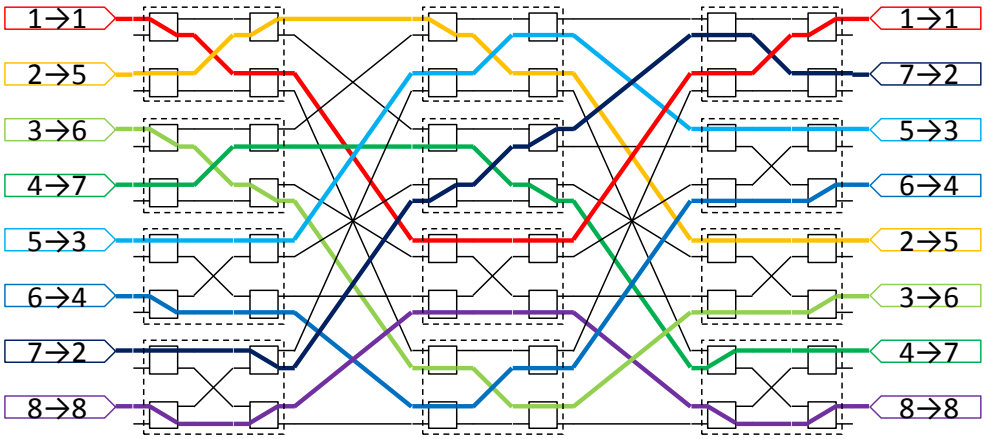

Figure 4.13 8×8 Dilated Beneš switch set up by the advanced routing algorithm

Figure 4.13 shows the optimal set-up where the path with large loss is avoided. The loss of the link between In#8 and Out#8 is 45.6 dB in this design while all other links have loss around 40 dB.

The off-line processing and storing method is also adopted for dilated Beneš switches. The 0.7 dB loss between bar and cross states of the 2×2 dilated building blocks are insignificant compared with the loss in shuffle networks between stages. The permutation matrix method is, therefore, can be used to trim the size of the look-up table. By only considering the path between input-stage and output-stage dilated Beneš building block, the assignments sharing the same connection matrix can be grouped together to cut down the size of the look-up table. The size look-up table is cut from 8! =(40320) to 282282.

Figure 4.14 shows the loss improvement of the lossiest path for all connection matrixes between input- and output-stage 2×2 dilated building blocks. 18 of 282 connection maps show more than 4 dB loss reduction.

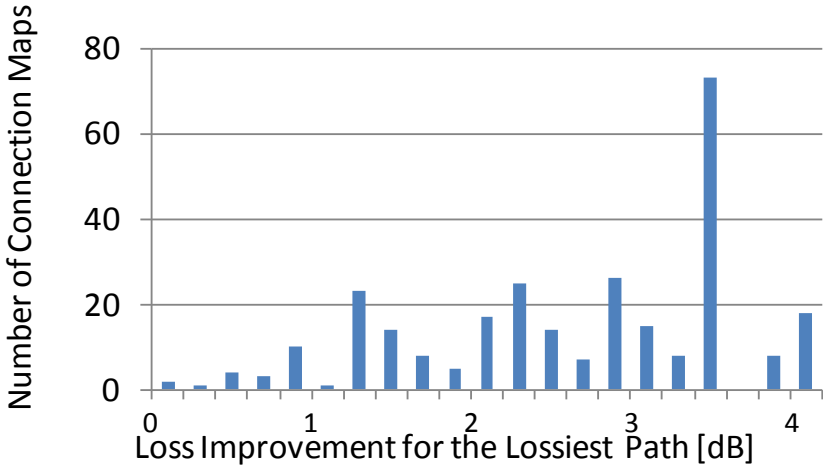

Figure 4.14 The Loss improvement for the lossiest path for the 8×8 dilated Beneš switch

The example discussed in the Figure 4.11 and is one of those 18 connection maps and demonstrates 4.13 dB reduction. The best set-ups store with those 282 connection maps, therefore, can provide optical set-ups for all possible connection assignments.

Figure 4.15 shows the loss between input- and output-stage 2×2 dilated building blocks for each link in Figure 4.11 and Figure 4.13. The variance among all paths has been reduced from 6.7 dB to 0.5 dB.

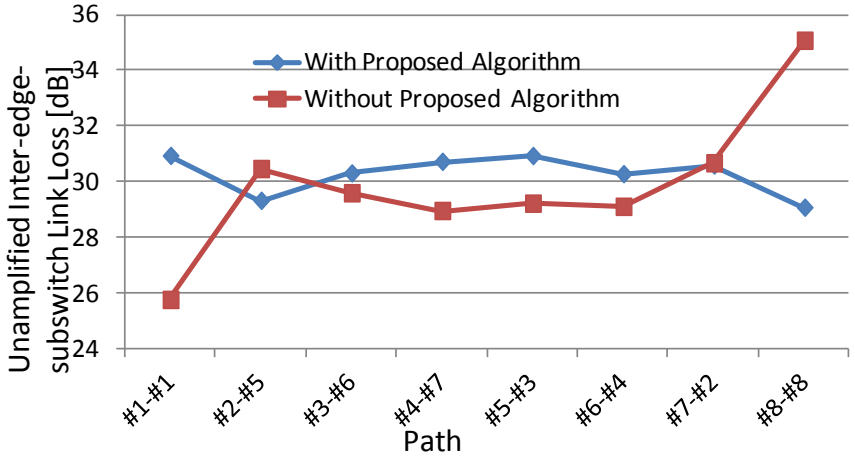

Figure 4.15 Detailed loss of each path (between the first- and last-stage 2×2 dilated sub-switches) for the set-ups shown in Figure 4.16 and Figure 4.17

To evaluate the optical performance improvement with the advanced routing algorithm, the loss of the entire path from input to output is required. The average unamplified path loss between the bar stage and cross state within a 2×2 dilated building block is used. This is 12.05 dB for the input-stage dilated building blocks. The output-stage dilated building blocks have a 9.45 dB average unamplified loss since they are shorter and only have one stage of SOAs.

The VPI simulator is also used here to simulate the IPDR performance of the links. 10Gbps NRZ (Non-Return to Zero) injected optical signal is applied. The IPDR for a 1 dB power penalty for the lossiest path has been reduced from 25.3 dB to 23.9 dB as shown in Figure 4.18.

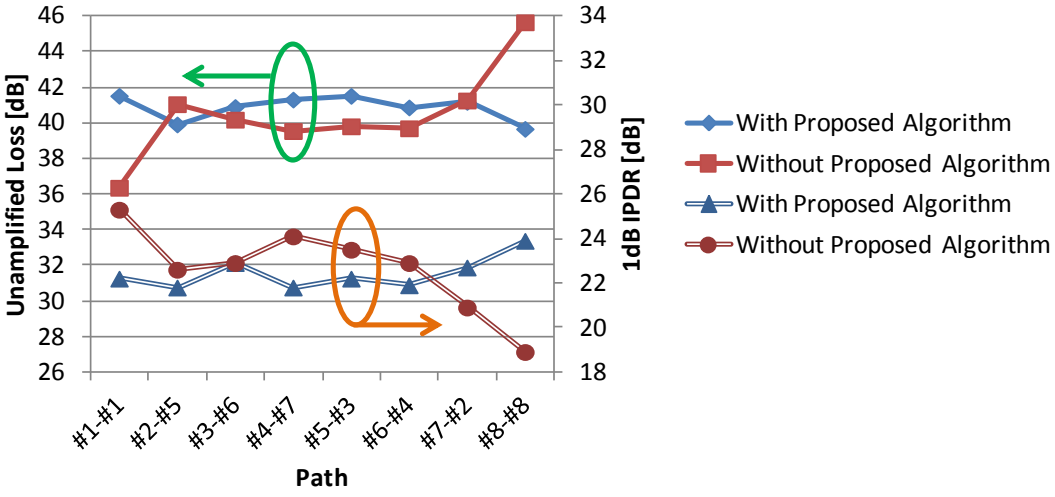

Figure 4.18 Detailed loss and IPDR of each path for the set-ups shown in Figure 4.1 and Figure 4.2

4.5 Conclusions of Advanced Routing Algorithms

The advanced routing algorithms developed here explore all possible set-ups for a given connection assignment and select the optimal set-up to mitigate the unnecessarily long path. The advanced routing algorithms for all three switching networks (Base 2, Base 4 and dilated Beneš) regulate the first connection in each loop via either the upper or lower middle network rather than always the upper middle network. The optimal set-up then can be selected based on the layout of switches.

It, however, a requires high-speed processors to construct all set-ups and calculate the optimal one with on-the-fly computation. Running the advanced routing algorithm off-line and storing its output of each assignment in a look-up table is a practical way to enable fast switch reconfiguration. The look-up table, however, has considerable size as it is the factorial of the number of input ports. If the path dependent loss within the input- and output-stage sub-switches is insignificant compared with shuffle networks, the size of look-up table can be greatly reduced by only considering the permutation between input- and output-stage sub-switches.

The loss and IPDR show a significant improvement by using the algorithm. An 8×8 Clos-tree switch demonstrates a 2.7dB decrease in loss and 1.9dB improvement in IPDR with 1.5 dB penalty for the worst case. An 8×8 dilated Beneš shows more than 4 dB loss reduction for the lossiest path and 1.4 dB IPDR improvement for 1 dB power penalty. The improvement by using the algorithm is predicted to be more significant with increasing switch size.

Chapter 5 Monolithic 4×4 Hybrid MZI-SOA Switch

5.1 Introduction of InP-Based Switches

Recent rapid advances in the capability of InP-based integrated photonic circuits have attracted much attention. A full range of optical components, including lasers, modulators, amplifiers and receivers can be produced in InGaAsP/InP foundries [102]. Hundreds of components per chip resulting in complex operations have been demonstrated using this approach.

Within such a platform, SOAs [103], MZIs [104][105] and ring resonators [106] can be used as switching elements. Ring resonator-based switches offer power-efficient solutions for optical switching. Higher-order ring resonators demonstrated good performance in terms of bandwidth, though only by implementing more complex wavelength locking loops [106]. However, optical loss is still an issue that restricts the scalability. SOA-based switches are generally built based on a broadcast-and-select architecture [107][108]. Splitters and combiners are implemented to assemble fan out and fan in networks [109]. The attenuation of OFF-state SOAs absorbs the signal and enhances the extinction ratio [110]. The gain from the ON-state SOAs is able to compensate the intrinsic 3 dB loss from each 2-way splitter/combiner and excess loss from other passive components. The number of splitters/combiners and the total length of passive waveguides on each path increases with the size of the switch, and thus a higher level of gain is required to compensate for the growing loss as the switch size increases. However, SOAs introduce ASE noise and signal distortion and increase the switch power penalty. As the port count reaches 16×16, a 4.9 dB penalty [111] and a 1.8-5.5 dB penalty for different paths has been reported [112].

MZI-based switches on the other hand in principle do not suffer from intrinsic loss but instead suffer from poor crosstalk due to imperfect coupler split ratio and loss mismatch within the arms. Large MZI-based switches can be built by cascading MZI elements, but the accumulated crosstalk will limit the scalability. Moreover, MZI-based switches suffer from the passive loss which in part also limits their size.

In this thesis, a hybrid approach has been adopted. SOAs are integrated with MZI switches to compensate for the passive loss and to reduce the MZI crosstalk. Each MZI is used as a 1×2 or 2×1 low-loss switching element in a dilated Beneš architecture in order to mitigate the crosstalk further. The design, fabrication, characterisation and control of an integrated hybrid MZI-SOA 4×4 switch are discussed in this chapter.

5.2 Design and Integration of the 4×4 Hybrid MZI-SOA Switch

5.2.1 Switch Design

Both MZIs and SOAs are included in this hybrid design [113][114]. Here, MZIs are used as the main switching elements to avoid the intrinsic 3 dB loss from splitters/combiners in broadcast-and-select SOA-based switches. As shown in Figure 5.1 both outputs of an MZI are linked to short SOA components. Once the signal is routed to an output, the corresponding SOA is turned on in order to compensate for the loss from other passive components. The SOA connected to the other output is in the OFF state and therefore suppresses crosstalk.

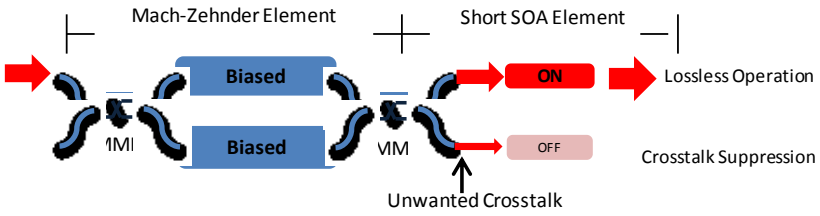

Figure 5.1 Basic operation scheme of the hybrid MZI-SOA switch

A hybrid dilated Beneš scheme has been proposed to reduce the crosstalk further[113][101]. As shown in Figure 5.2, it includes four 2×2 hybrid building blocks within a dilated Beneš architecture. A 2×2 dilated Beneš building block contains four MZIs and eight SOAs. Although

it has four inputs and four outputs, only one of each pair will be on at a given time which means the outer input and output elements function as 1×2 and 2×1 low-loss switches, respectively.

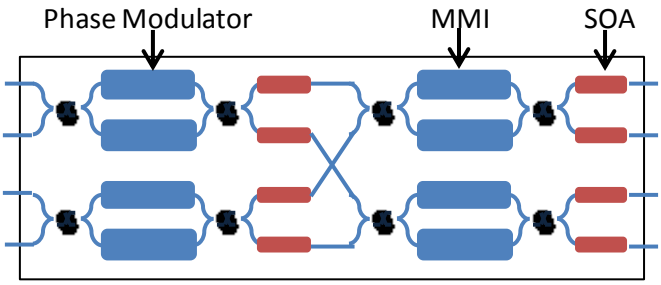

Figure 5.2 Schematic of a dilated Beneš hybrid 2×2 building block

Figure 5.3 shows the schematic of the 4×4 dilated hybrid switch which is constructed using two cascaded 2×2 dilated building blocks [116]. It has a modified dilated Beneš architecture. It can be converted back to the original dilated Beneš architecture by reordering the 2×2 sub-switches at Stages 2 and 3. The reason to adopt this modified dilated Beneš architecture is to increase the size of the basic building blocks, easing the design and fabrication.

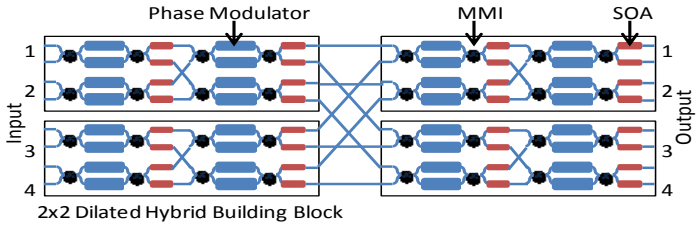

Figure 5.3 Schematic of a dilated Beneš hybrid 4×4 switch

The chip was fabricated on a multi-project wafer [102]. A chip size of 4 mm × 6 mm was allocated to this project. The design of the 4×4 switch shown in Figure 5.3 cannot fit into this allocated chip size. The layout of the switch, therefore, was amended to fit into to allocated area as shown in Figure 5.4. The details of the fabrication parameters are discussed in the next section.

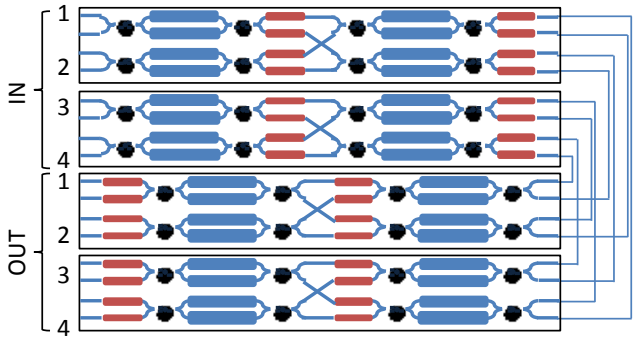

Figure 5.4 Schematic of a folded 4×4 dilated beneš hybrid switch.

5.2.2 Fabrication in a Generic Foundry

The 4×4 hybrid switch chip was fabricated in an open access generic InGaAsP foundry within the EU FP7 PARADIGM project [117][118]. In this approach, predefined and standardised optical components, such as phase modulators, SOAs and waveguides were adopted to construct photonic integrated circuits (PICs) [121-136].

Figure 5.5 shows the cross-section view of the Multiple Quantum Well (MQW) epitaxial structure and the passive waveguide. The detailed compositions of MQW of the platform are confidential. Further information is possibly provided by contacting EuroPic and Oclaro [135].

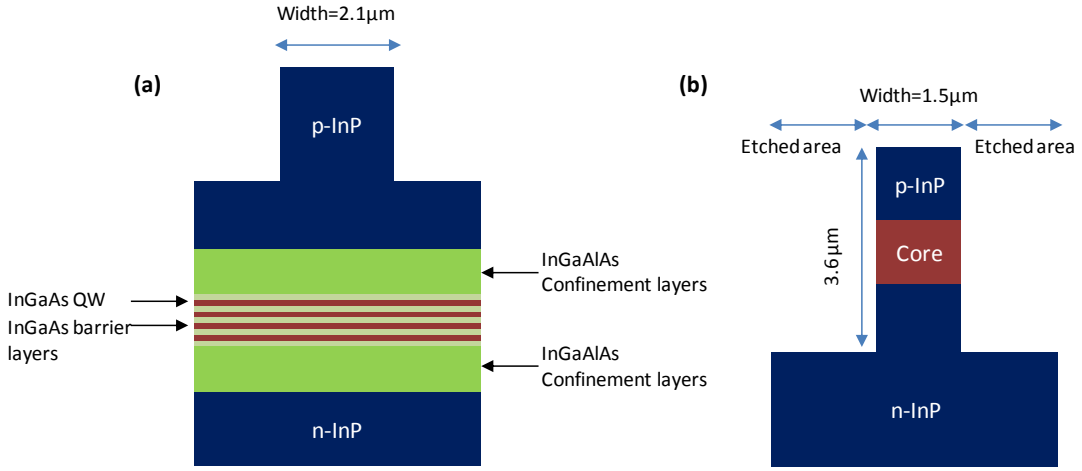

Figure 5.5 Cross-section view of (a) the MQW epitaxial structure and (b) The passive waveguide [135]

SOAs are shallow-etched waveguides with MQW active regions. The SOA waveguide width is 2.1 μm. The length is variable from a minimum of 50 μm. They can only be defined along a direction perpendicular to the major flat. The structure is optimised by the foundry to provide optical gain for TE polarization. A bond-pad area with a width of 175 μm is defined around the SOA sections. Strong-to-weak (deep-etched to shallow-etched) waveguide transition elements are required between strong passive waveguides (deep-etched waveguides) to SOA section. 100 μm long waveguide transition elements have been implemented in this design to reduce reflections.

Strong passive waveguides have a deep-etched waveguide geometry. The core region is a single bulk layer. The waveguide was defined by etching trenches on both of the sides. 1.5 μm ridge width was applied in this design. The default trench width is 10 μm, which means the separation between two waveguides needs to be larger than 10 μm.

Phase modulators within the MZIs have the p-contact on the top of the waveguide, allowing refractive index tuning for phase shifting. The core region is an MQW structure that provides efficient EO modulation through the QCSE. This component is controlled by reversed biased voltage. Compared with carrier injection phase shifters, no energy is consumed in the static state, ensuring low power consumption for this hybrid approach.

Figure 5.6 shows the design layout and a photograph of the fabricated chip. Within a 4 mm × 6 mm allocated sector, the switch layout was folded to fit into the area. As a result, the four input and four output ports were placed at the same edge of the chip, and the folded shuffle network was located at the opposite end of the chip. The facet of the input and output waveguide terminals is anti-reflection coated.

The length of the chip, however, is still not enough if all phase modulators are 1000 μm long. The length of some of the modulators has been slightly adjusted to 900 μm to fit the chip design. Those 1000 μm and 900 μm long QCSE phase modulators are connected with waveguides and multimode interference (MMI) couplers to construct the MZIs.

230 μm long SOAs were placed after each MZI to compensate for the loss and suppress crosstalk. Longer SOAs (250 μm) were connected to the shuffle network to compensate for its excess loss.

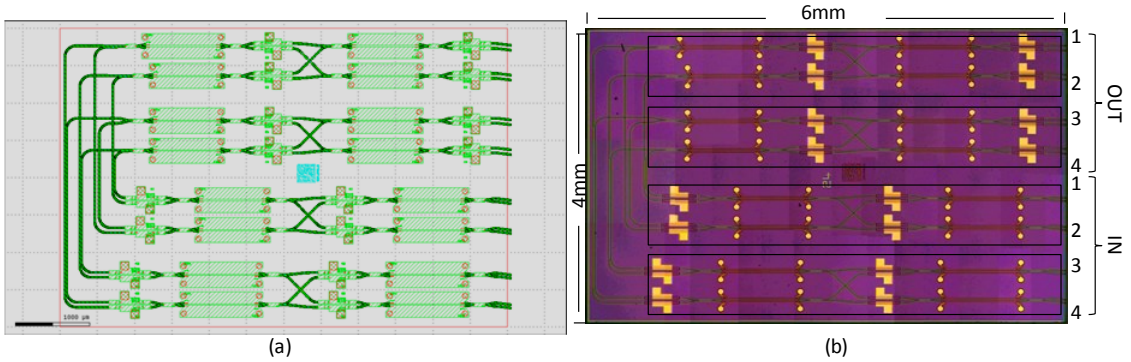

Figure 5.6 (a) Switch layout and (b) Photo of a fabricated switch

5.3 Characterisation of the 4×4 Hybrid Switch

To characterise the performance of the switch chip, the chip needs to be die-bonded to a sub-mount to have a good ground connection. Each component is then wire bonded to copper pads. By adjusting the voltage and current on these copper pads, the MZIs and SOAs on the chip can be controlled.

Since there are no spot size converters (SSCs) at the input and output waveguide for this particular switch due to the limited chip size, a single mode fibre's spot size does not match that of the waveguides on the chip. Lensed fibres are therefore used in this experiment to convert the spot size and effectively couple light in and out of the chip. The spot size of the lensed fibre used in this experiment is 2.5 microns. The coupling loss between the lensed fibre and the chip is 7.5 dB. It was measured by comparing the measured optical power from a broad-area detector and a lensed fibre.

The design of the sub-mount is shown in Figure 5.7a. Since the waveguides are fabricated at an angle of 7° to the facet normal to further reduce the optical reflections in this design, the lensed fibre needs to be aligned 23° to the facet normal shown Figure 5.7b. This design of the

sub-mount reduces the complexity of the fibre coupling. Aligning the fibre with both top and bottom edge ensure the correct angle of the lensed fibre.

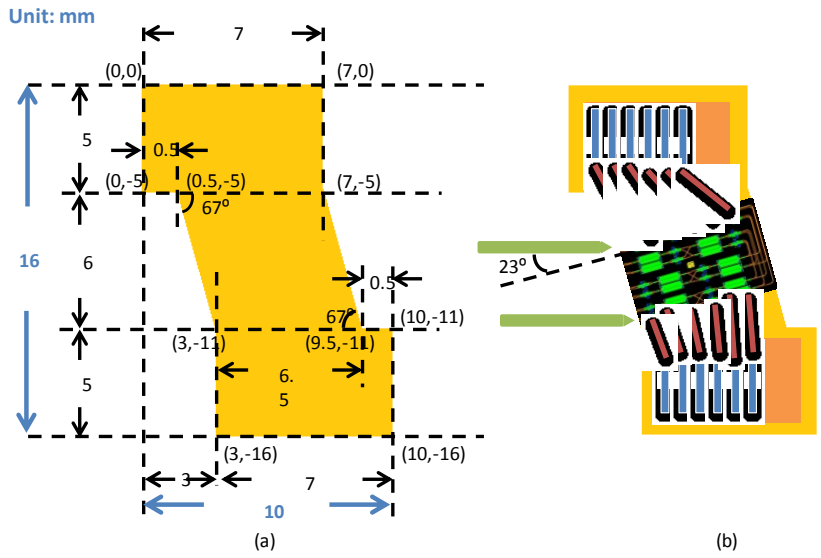

Figure 5.7 (a) Design of the sub-mount and (b) Sub-mount with switch chip and copper pads

Experimental characterisation has been performed by mounting the chip on a thermo-electric cooler (TEC) to maintain a temperature of 20°C. Figure 5.8 shows the experimental setup of the chip. The chip on the sub-mount is placed at the top of an experimental stage. Two lensed fibres are used to couple light in and out of the chip. The copper pads wire bonded with SOAs and MZIs are connected with D connectors. Cables from voltage sources and current sources can be easily plug in the D connectors and control the switch.

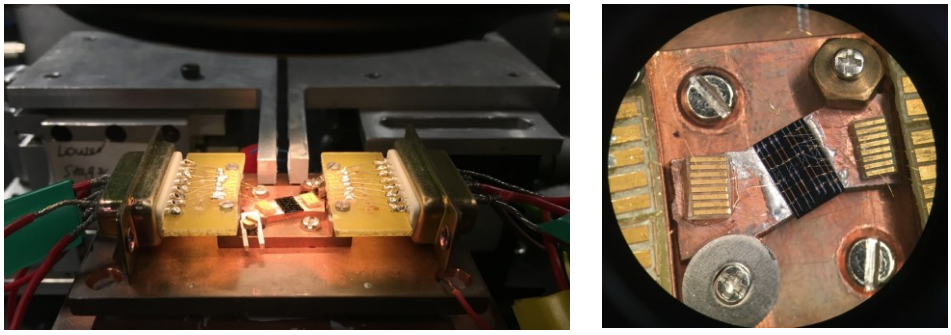

Figure 5.8 (a) Switch chip under test and (b) Top view of the chip under test

5.3.1 Static Characterisation

The ASE spectrum of the SOA at the output port was tested initially. A lensed fibre was aligned with an output port to collect the light coming out the SOA, which is 230 µm long and biased at 15 mA. An Optical Spectrum Analyser (OSA) with 0.1 nm resolution in wavelength was connected with the other end the lensed fibre. Figure 5.9 shows the spectrum of the ASE noise.

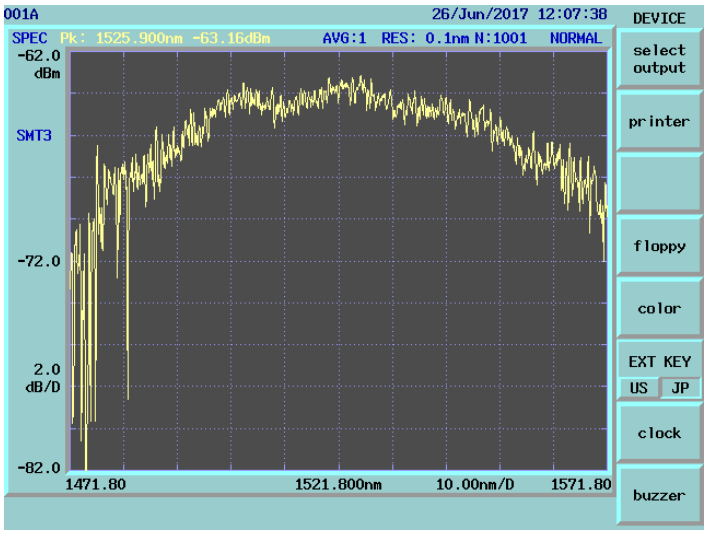

Figure 5.9 ASE spectrum of 230 µm SOA biased at 15 mA (0.1 nm resolution in wavelength)

As the optimum operating wavelength is determined by the SOA gain performance, the SOA components were characterised first. A tunable laser was used to inject a continuous wave (CW) signal into the current. Four SOAs on the path were connected with current sources, and both arms of four MZIs were controlled by the voltage sources. All SOAs and MZIs were biased with optimal current and voltage, respectively (details of the optimal current and voltage is discussed in this section and section 5.3.2). The gain peak was found to be at 1535.9 nm with a 3 dB bandwidth of 22.5 nm. The gain curve is shown in Figure 5.10.

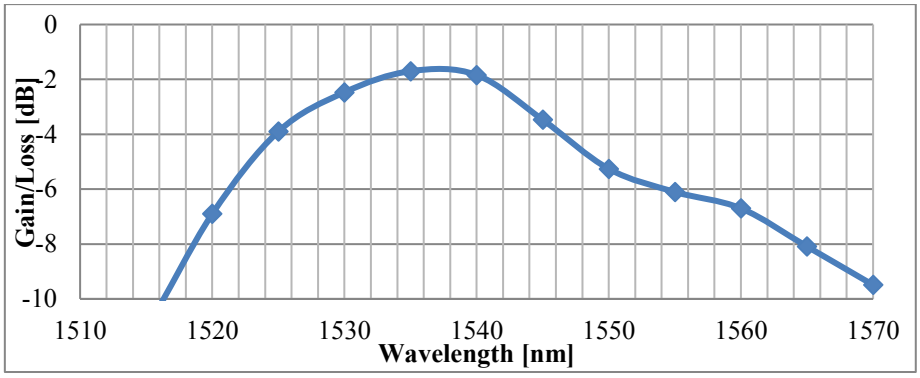

Figure 5.10 On-chip gain/loss at different wavelength

The Optical Signal to Noise Ratio (OSNR) of the chip was then measured with 0.1 nm resolusion. An optical input with different power was injected into the chip. -25 dBm, -20 dBm, -15 dBm, -10 dBm on-chip input power result in OSNR of 22 dB, 27.5 dB, 32.5 dB, 37.5 dB (Figure 5.11).

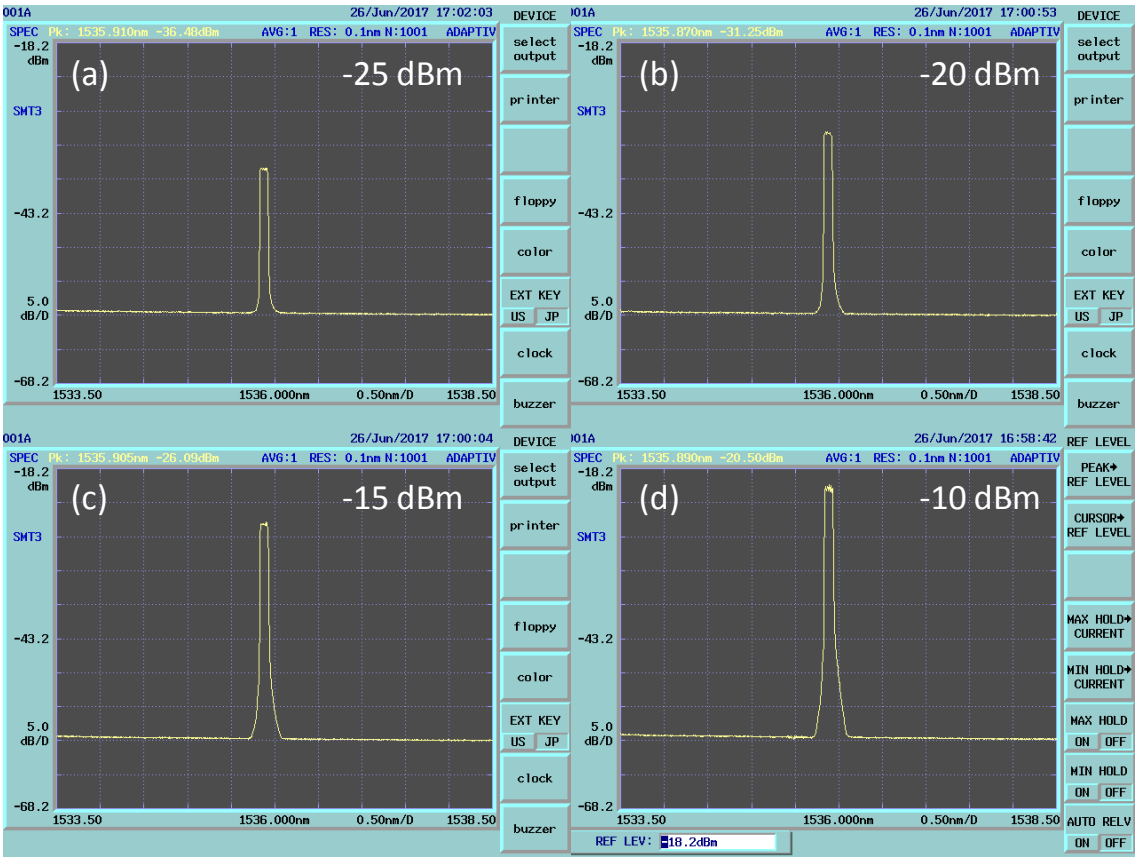

Figure 5.11 OSNR (0.1 nm resolution in wavelength) for on-chip input power at (a) -25dBm (b) -20dBm (c) -15 dBm (d) -10 dBm

The gain/absorption performance of SOAs on the chip was then characterised. The transparency currents of the SOAs with two different lengths were determined first.

A junction-voltage technique was adopted here to measure the material transparency current[136]. An input optical signal is able to, due to stimulated absorption or emission, induce a change in carrier density in the active region. It leads to a voltage drop across the diode. At material transparency, the stimulated absorption is exactly balanced by stimulated emission and the voltage drop goes to zero. The polarity of the voltage drop changes sign at the transparency current. Therefore, a modulated input beam and lock-in amplification are usually adopted to sensitively detect the polarity sign flip and the transparency current.

As shown in Figure 5.12, the tunable laser was directly modulated with a 10 MHz sinusoidal signal. The SOA under the test was connected to a bias Tee. DC bias was provided by the current source and the RF port was monitored to measure the phase and amplitude of RF signal

stimulated by the modulated inject optical signal using a lock-in amplifier. The SOA here acts as a detector which indicates the operating status under different DC bias current. Increasing the bias current from zero, the SOA operates in absorption, transparency and amplification mode. The SOA acts as an absorber without DC bias and the increasing bias current reduce the absorption until the material transparency potion is reached, where a 180^0 phase change occurs and the power of the detected RF signal reaches a minimum. Further increased injection carriers will cause population inversion and contribute to amplification.

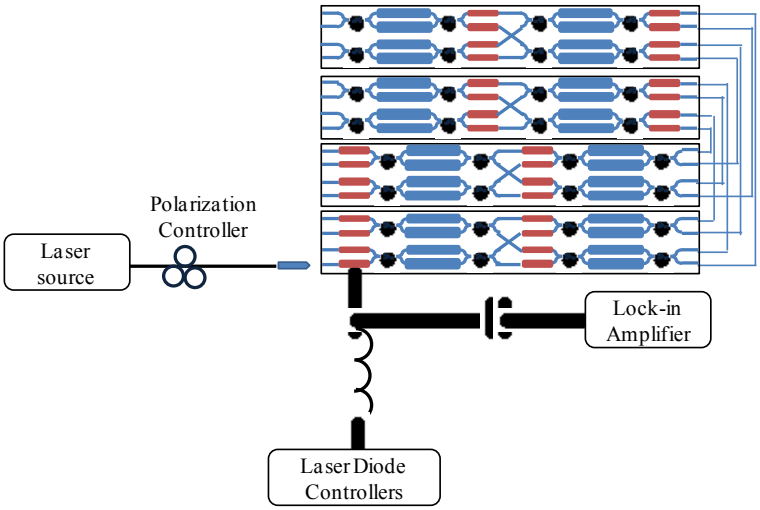

Figure 5.12 Experiment setup for transparency current measurement

As shown in Figure 5.13a, the transparency current of the 230 μm long SOA was found to be 3.7 mA. The 250 μm long SOA is not at the edge of the chip. To measure the transparency current of the 250 μm long SOA, the other two SOAs between the measured SOA and the edge of the chip were biased at the transparency current. Figure 5.13b shows the 4.2 mA transparency current of the 250 μm long SOA. The amplitude of the RF signal was reduced because of the increasing passive loss between the SOA and the edge of the chip.

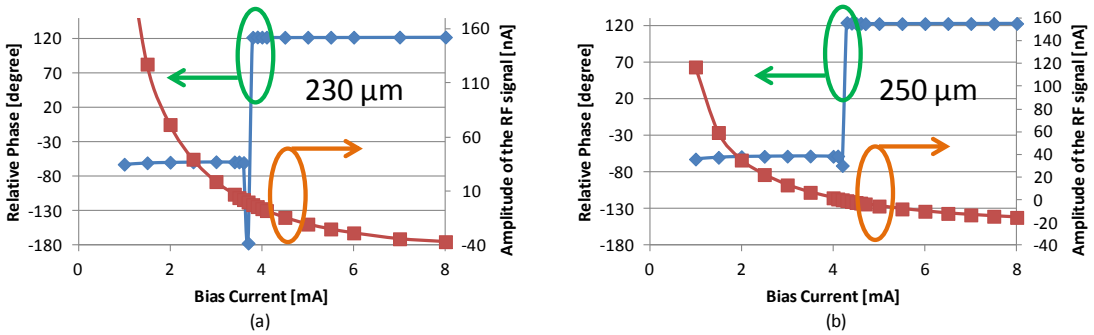

Figure 5.13 The monitored amplitude and phase of the detected signal as a function of bias current for (a) 230 µm and (b) 250 µm long SOA

The gain performance of individual SOAs was then characterised by biasing the other three SOAs in a path at the transparency current and by varying the bias current of the measured SOA. Figure 5.14 shows the gain versus current for SOA for both 230 and 250 µm lengths. 15mA/17mA bias current were chosen for the 230/250 µm long SOAs to provide 5/6.3dB gain respectively to compensate for the loss of the passive components. Around 15 dB attenuation was introduced by SOAs with both lengths when they are in the OFF state.

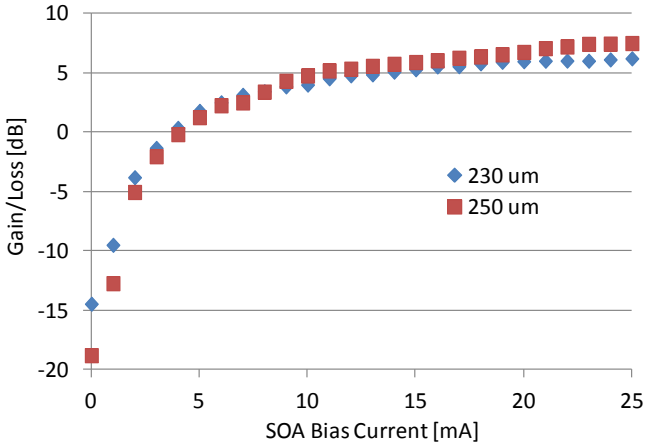

Figure 5.14 SOA (230/250µm) gain versus bias current

Figure 5.15 shows the power budget of an ON state path, which exhibited a 1.3 dB overall loss [137]. 23.9 dB loss was introduced by the passive components on the chip: optical waveguides (6 dB/cm), S-bends (0.2 dB), circular bends (0.2 dB), MMIs (0.5 dB), 900 µm long phase modulators (1 dB) and 1000 µm long phase modulators (1.2 dB), waveguide transition elements (1 dB). The estimated component-level loss was found by a combination

of experimental measurements. The four SOAs provided 22.6 dB gain to compensate the passive loss and achieve almost lossless operation. The excess loss from the folded shuffle network was compensated by the additional gain from the 250 μm SOA.

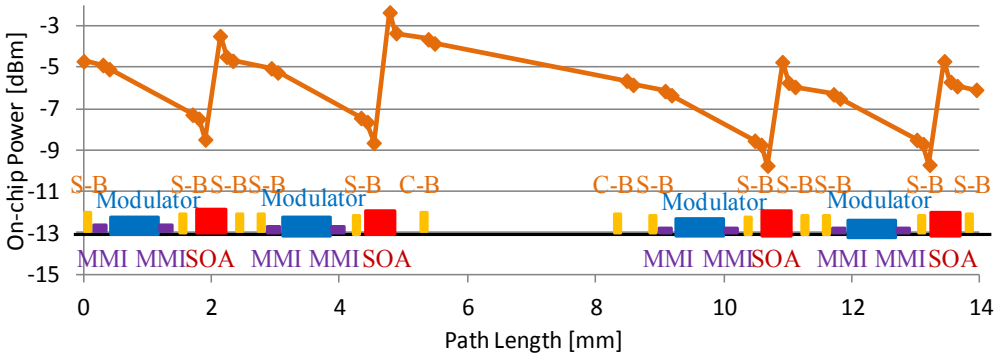

Figure 5.15 On-chip power budget of a path

5.3.2 Switching Performance Characterisation

To assess the switching performance of the 4×4 switch, the switching curve of each individual MZI need to be measured. Here, to accurately measure the switching curve of individual MZIs, the absorption property of SOAs is utilised. As shown in Figure 5.16, the SOA is connected to a current meter. It works as a photodiode, so the output power of the MZI can be measured. A 1535.9 nm (where the SOAs have the peak gain) laser source was used to generate the optical input to maximise the output power. As the foundry provides SOA structures optimised to provide optical gain for TE polarization, a polarisation controller is required before the input of the switch to ensure TE polarisation. The two arms of the MZI were reversed biased by a voltage source. The extinction ratio in terms of the arm bias voltages was then measured.

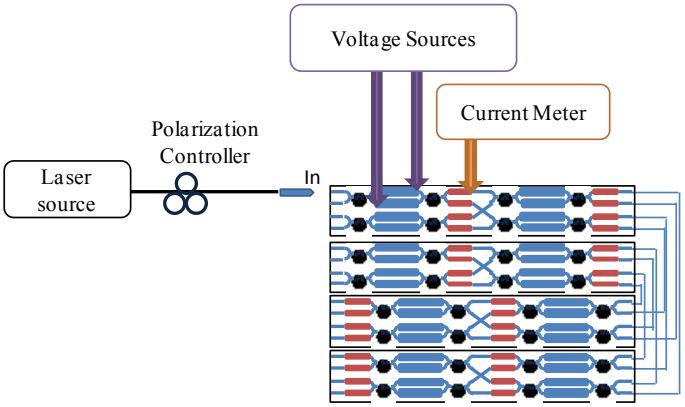

Figure 5.16 Experiment setup for MZI switching curves measurement

The switching curves of the other MZIs, which are not at the edge of the chip, can be measured in the same way. The SOAs between the measured the MZIs and the input port were biased at the transparency current. The MZIs in between them were biased at the optimal point with the largest output. The 3D switching curves of five MZIs are shown in Figure 5.17.

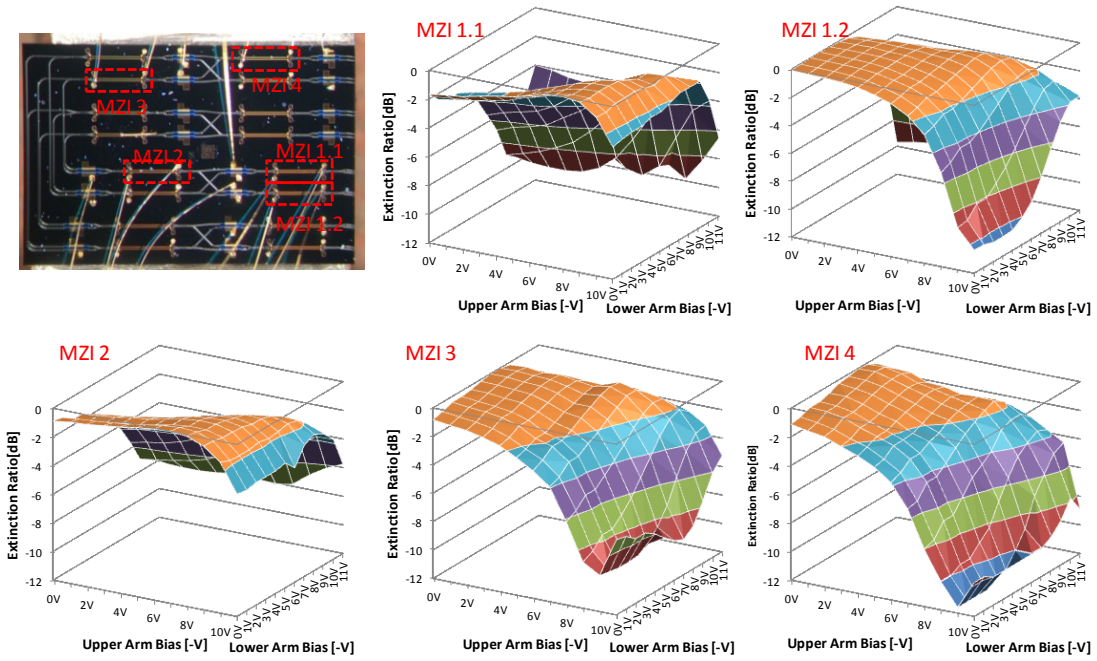

Figure 5.17 Switching curves of MZIs in terms of both arms

To prevent damaging the chip and extend the lifespan of the switch, the voltage applied to the phase shifters should be minimised. Therefore, the applied voltage sweeping is aborted as soon as both peak value and bottom value have been appeared.

In the switching operation, to ease the complexity of the control, one arm of the MZI is biased at an optimal voltage ensuring the maximal optical output, and the other arm is biased with varying voltage. The 3D switching curves are then analysed to extract 2D switching curves with an arm fixed at an optimal voltage.

Figure 5.18 shows the 2D switching curves for five MZIs. It shows the peak and bottom value of a switching curve. These MZIs feature a V_π of around 9 V. The extinction ratio of a single MZI is within the range of -11 to -8 dB.

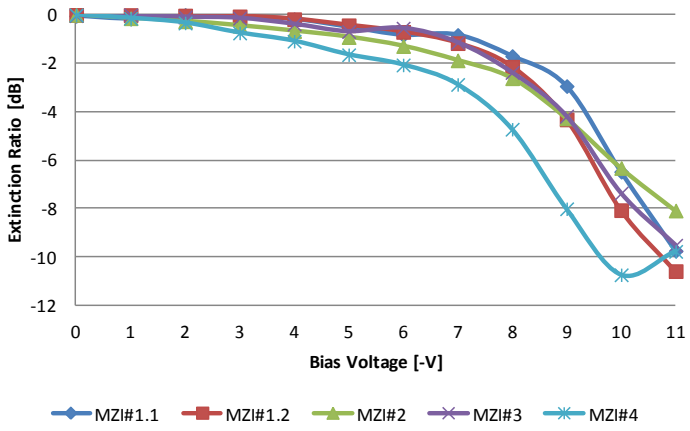

Figure 5.18 Switching curves of MZIs with one arm biased by an optimal voltage

The switching performance of the switch was then measured by assessing the crosstalk between two adjacent input ports. As shown in Figure 5.19, a CW laser source was implemented with a polarization controller, and an optical spectrum analyzer (OSA) was used to measure the output power of the switch. The light was injected into two inputs in turn to characterise the switching performance/crosstalk ratio of each path. The corresponding MZIs were biased to tune the output power between the minimum value to maximum value. The corresponding SOA on each path was turned on and off to reduce the crosstalk ratio further. Other SOAs and MZIs were biased at constant current/voltage.

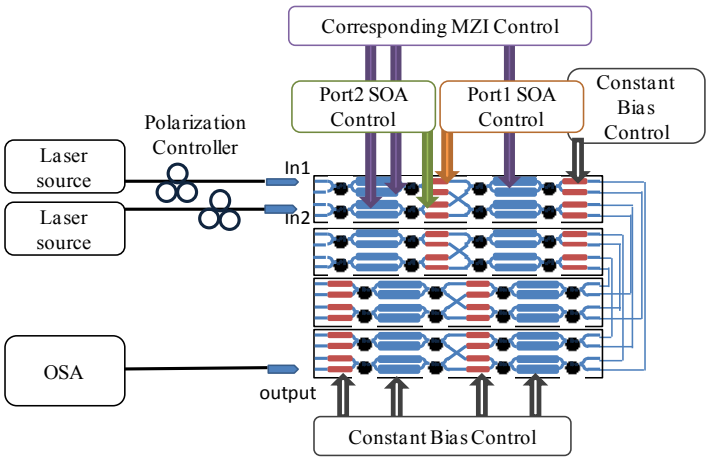

Figure 5.19 Testbed for the dilated building block switching curve measurement

The crosstalk ratio of a single MZI on this chip only can achieve at most -11 dB. The relatively poor crosstalk performance mostly results from the loss mismatch between the two phase modulator arms and imperfect MMI split ratio, limiting the scalability of switches based on MZIs. The dilated Beneš architecture, as discussed at the beginning of this chapter greatly improves the crosstalk performance. As shown Figure 5.20, the crosstalk is roughly doubled to -27 dB as indicated by the blue line with diamond symbols and green line with triangle symbols. By switching the bias of the SOA between 0 mA and 15 mA, the crosstalk ratio is enhanced by more than 20 dB. As a result, -47 dB and -50 dB crosstalk for Ports 1 and 2, respectively, are demonstrated. This 20 dB improvement comes from the difference between the 5 dB gain of SOA in the ON-state and the 15 dB attenuation of the OFF-state. This dilated design plus the SOA thus ensures an excellent crosstalk regardless of imperfect fabrication processes.

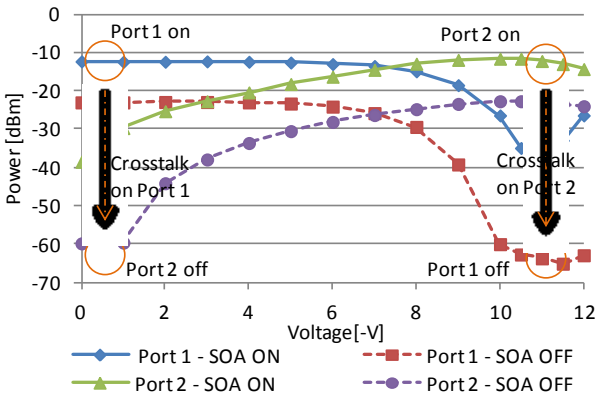

Figure 5.20 Switching curves of the 4×4 chip between two inputs and one output.

The dynamic switching operation was characterised by switching a given output-edge MZI between cross and bar states and turning the corresponding SOA on and off. A Stanford delay generator was used for the experiments. For SOAs alone, the rise time is 3ns and fall time is 2 ns (10% - 90%).

By turning the MZI and corresponding SOA simultaneously, the transition time of a switching unit can be measured. As shown in Figure 5.21, 6 ns rise time and 3 ns fall time has been recorded for a hybrid switching unit.

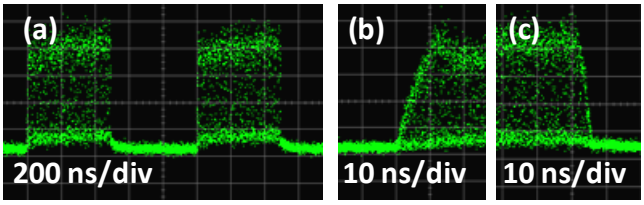

Figure 5.21 (a) Dynamic switching operation of the switch, (b) Rising edge and (b) Falling edge

5.3.3 Power Penalty and Relaxed Active Control

We assess both SNR impairments and non-saturated distortion with the chip by measuring the power required at the receiver to achieve a constant 10^{-9} BER relative to the case without the switch – the power penalty. The power penalty of a path (coloured purple) is assessed by using the testbed shown in Figure 5.22. A laser source with a wavelength of 1535.9 nm and a Mach-Zehnder modulator (labelled in Figure 5.22) driven by a 10 Gb/s non-return-to-zero (NRZ) signal with 2^{31}-1 pattern length Pseudo-Random Binary Sequence (PRBS) was used to generate the optical input to the chip. An Erbium-doped Fibre Amplifier (EDFA) was placed after the Mach-Zehnder modulator to compensate the loss from the modulator and coupling loss from the following lensed fibre. A variable optical attenuation was connected with the EDFA to vary the input optical power. 10% of the optical power was transmitted to a power meter for the mentoring purpose. A polarisation controller is required before the input of the switch to ensure TE polarisation.

The output is characterized using an optical pre-amplified and filtered receiver for Bit Error Rate (BER) measurements. The EDFA is used here to compensate the 7 dB coupling loss from lensed fibre, the 2.5 dB excess loss from the variable attenuator and 1 dB loss from the 10:90 coupler. The filter was used to reduce the ASE noise from the EDFA. The measurement also can be done without the filter by measuring the power penalty with and without the optical chip for each input power level and calculating the difference between them [138]. Similar results have been demonstrated using the two measurement methods.

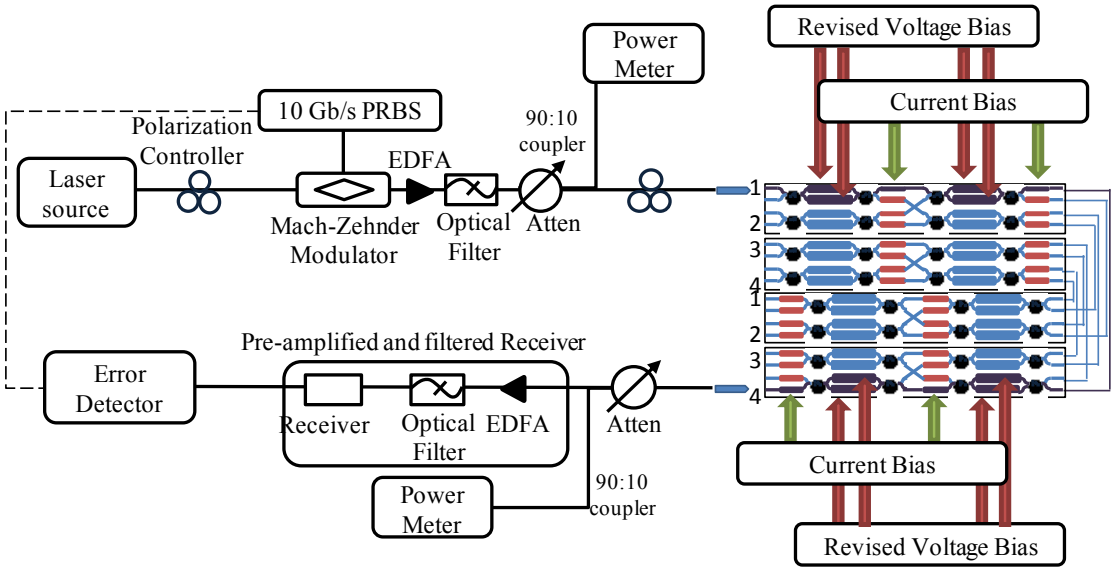

Figure 5.22 Experiment setup for BER measurement

The received input power can be adjusted by varying the loss of the VOA on the receiver side. A lower BER is achieved with higher received input power. The BER versus received input power for the back-to-back operation where the switch was replaced by a fibre was also measured, The power difference required at the receiver to achieve a constant 10^{-9} BER in the presence and absence of the switch is the power penalty as shown in Figure 5.23.

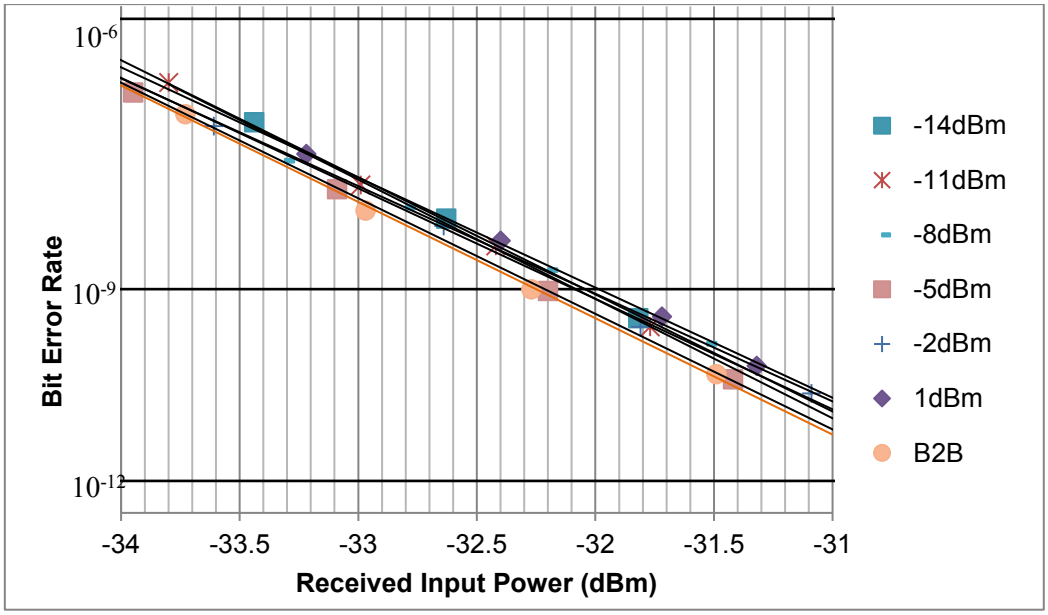

Figure 5.23 BER versus received input power for the 4×4 switch

Input Power Dynamic Range (IPDR) of an optical switch gives the input power range within which an optical switch can be operated under a certain low power penalty [139]. This switch demonstrates an IPDR of 13 dB for a penalty less than 0.5 dB with a penalty floor at 0.05 dB as shown in Figure 5.25.

The corresponding eye diagrams for on-chip optical input powers at -14 dBm and 2 dBm are also recorded. The power penalty builds up in the low input power region owing to the degraded optical signal-to-noise ratio (OSNR), which is the ratio between the signal power and the noise power within a valid bandwidth. For the high input power, the optical performance is limited by the saturation-induced distortion.

For multi-stage SOA networks, it has been previously demonstrated in [141] that active power monitoring and bias control can extend the IPDR. In this experiment, optimum bias control currents in the range from 3.6 mA to 20 mA for the first-stage 230 µm long SOA and from 5.6 to 22 mA for the second-stage 250 µm long SOA are selected to minimise power penalty as the input power is varied, as shown in Figure 5.24. The bias to the second-stage SOA is chosen to be 2 mA higher than first-stage SOA [142]. Other SOAs are biased at 15 mA.

The extended IPDR is also shown Figure 5.25 with the corresponding eye diagrams for optical input power at -14 dBm and 2 dBm. The IPDR for a power penalty of less than 0.5 dB has been extended by at least 4 dB by implementing the active bias control. The power penalty improvement is more significant at high powers because there is less amplifier-induced distortion as the SOA bias currents are lower.

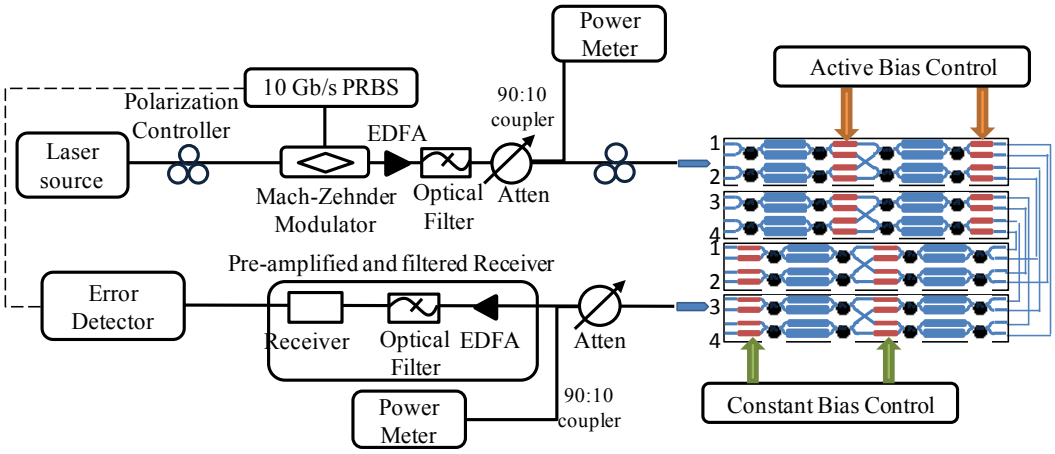

Figure 5.24 Experiment setup for active bias control

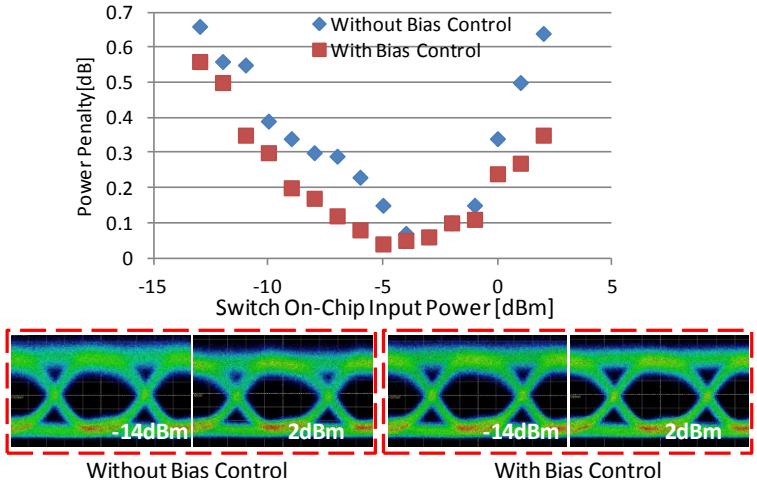

Figure 5.25 Power penalty as a function of switch on-chip input power and eye diagrams

Output power variation is a problematic issue which may lead to signal degradation in subsequent components [143]. It is highly desirable to be able to configure the switch circuit dynamically in order to maintain a constant switch output power for a range of input powers. Controlling the bias current of the first/second-stage SOAs can also effectively maintain the

output power. Figure 5.26 shows the static transfer function of the switch with and without current control. A fixed output power at -6 dBm is achieved for a range of 10 dB input power.

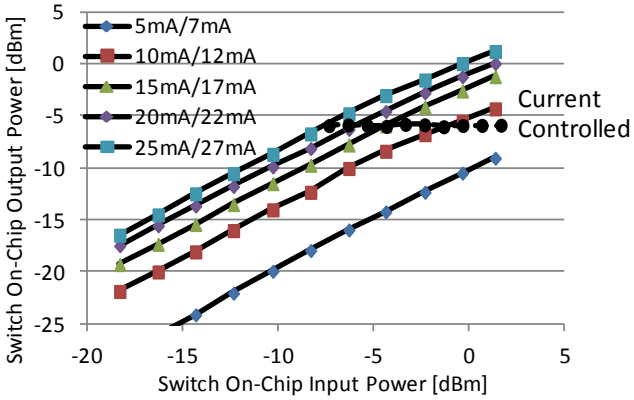

Figure 5.26 Static transfer functions of the switch for constant and biased control

The tolerance of the controlled current also needs to be studied [144]. The power penalty of the switch was measured with a range of on-chip input power and a range of bias currents for the first/second-stage SOAs. The second-stage SOA is 2 mA higher than first-stage SOA. Figure 5.27 shows a detailed penalty map as a function of both on-chip input power and bias current. The tolerance of the current control accuracy of this switch is very broad. Within a 5 mA bias current range, the power penalty can be maintained below 0.2 dB for 8 dB IPDR and within a 12 mA range 10 dB IPDR with a penalty less 0.5 dB has been achieved. The active control, therefore, can be implemented easily.

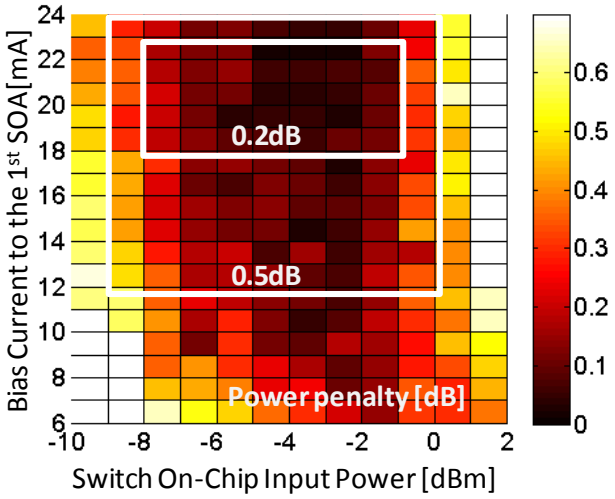

Figure 5.27 Power penalty map as a function of the on-chip input power and SOA bias current

5.4 Discussion and Conclusions

5.4.1 Energy Consumption

Low energy consumption is a merit of optical switches relative to their electronic counterparts particularly at high throughput. Compared with electronic switches, the power consumption of optical switches has been significantly reduced as there are no opto-electronic (OE) and electro-optic (EO) conversion. The hybrid MZI-SOA switches show further lower energy consumption compared with conventional SOA-based switches.

In terms of fixed current operation for this chip, the 230 μm and 250 μm SOAs are biased at 15 mA and 17 mA respectively, and both of them have a forward voltage of 1 V. Therefore they consume 15 mW and 17 mW respectively.

Conventionally, a 50 Ω matched impedance is used to drive each phase modulator to eliminate electrical reflections. In this work, the matched impedance is not used to reduce the power consumption. As the transmission line from drivers to the chip is less than 60 cm, the electrical propagation time is much less than switching period, and the reflections from terminations are not a significant concern. The MZIs are reverse biased and act as capacitors. Each MZI has a capacitance of around 0.5 pF. In order to estimate the power consumption, we assume a bit rate

of 10 Gb/s, a packet length of 10^4 bits and hence a switching rate of 1MHz. Since no energy is consumed unless the MZI is switched, each consumes around 5 μW, and so the energy consumed by the MZIs is thus negligible compared to the SOAs.

Therefore, a path through the switch has 62 mW power consumption and a fully loaded 4×4 requires 250 mW. When operating with 10 Gb/s per port, the energy efficiency is 6pJ/bit and. Compared with the SOA-based switches cited at the beginning of this Chapter, where a 4×4 chip consumes 310 mW [110], this hybrid approach delivers 20% reduced energy consumption.

5.4.2 Integrated Polarisation-Diversity

Polarisation controllers are required for this chip since the SOA structures in the foundry have been optimised to provide optical gain for TE polarisation. For situations where polarisation controllers cannot be used, such as when the input polarisation is varying, an integrated polarisation-diversity scheme is a possible solution. The design of the chip should be adjusted to adapt to this case. Two identical switches can be placed in parallel on the chip. In front of one of the switches, a polarisation rotator can be fabricated to provide 90-degree polarisation rotation. A splitter is also placed in front of two switches to split optical input evenly into two switches, and a combiner is fabricated after two switches to combine outputs together. With this scheme, input light with all kinds of polarisations can be switched, and polarisation controllers can be omitted.

5.4.3 Conclusions

Recent rapid advances in the capability of InP-based integrated photonic circuits have attracted much attention. A full range of optical components, including lasers, modulators, amplifiers and receivers can be produced in InGaAsP/InP foundries [102]. Hundreds of components per chip have been demonstrated using this approach. Table 5.1 summarises the performance of a selection of InGaAsP/InP-based switches in chronological order, placing this work in the context of the state of the art. Key switching metrics, such as gain/loss, crosstalk, power penalty floor and IPDR, are highlighted and compared.

SOAs, MZIs and ring resonators can be used as switching elements. Ring resonator-based switches offer power efficient solutions for optical switching. Higher-order resonators demonstrated good performance in terms of bandwidth, though only by implementing more complex wavelength locking loops [106]. However, optical loss is still an issue that restricts the scalability. SOA-based switches are generally built based on a broadcast-and-select architecture. Splitters and combiners are implemented to assemble fan out and fan in networks. The attenuation of the OFF-state SOAs absorbs the signal and enhances the extinction ratio. The gain from the ON-state SOAs is able to compensate the intrinsic 3 dB loss from each 2-way splitter/combiner and excess loss from other passive components. The number of splitters/combiners and the total length of passive waveguide on each path increases with the size of the switch, and thus a higher level of gain is required to compensate for the growing loss as the switch size increases. However, SOAs introduce ASE noise and signal distortion and increase the switch power penalty. As the port count reaches 16×16, a 4.9 dB penalty [111] and a 1.8-5.5 dB penalty for different paths is reported [112].

Table 5.1 Selected state-of-the-art of Indium Phosphide based optical switches

Port Count	**Architecture**	**Switching gate**	**On-chip gain/loss [dB]**	**Crosstalk [dB]**	**Power penalty floor at 10Gb/s[dB]**	**IPDR at 10Gb/s [dB]**	**Group**
1×8	Tree	SOA	>+17.5	<-44.4	0	20.5(<0.5dB)a	S. Tanaka et al, 2009 [107]
1×8	Tree	SOA	-3	-	0.4	-	H. Wang et al, 2009 [108]
4×4	N-stage Planar	SOA	-20.4 to -1.5	<-40	1.2	-	A. Albores-Mejia et al, 2010 [109]
16×16	Clos-tree	SOA	0 to +2	-	1.8 to 5.5	-	A. Wonfor et al, 2011 [111]
16×16	Clos-tree	SOA	-30 to -17.2	-18 to -30	4.9	-	R. Stabile et al, 2012 [112]
4×4	Tree	SOA	+5.8 to +7.5	-	0.45	12(<1dB)a	K. Wang et al, 2012 [110]

4×4	N-stage Planar	MZI	-	<-20	0	-	N. Koyama et al, 2013[104]
8×8	N-stage Planar	MZI	-	<-20	0	-	H. Kouketsu et al, 2014 [105]
8×8	Clos-tree	SOA	+3.7 to +7.7	-	0.7	14.5(<1dB)a	Q. Cheng et al, 2015 [103]
4×4	Cross point	Ring resonator	-20.5 to -5.9	-	2.1	-	R. Stabile et al, 2016 [106]
4×4	Dilated Beneš	MZI+SOA	>-1.3	<-47	0.05	14(<0.5dB)a	This work

The size of conventionally MZI-based switches is inevitably restricted by the accumulated crosstalk and loss owing to cascaded MZIs and a considerable number of passive components. Using SOAs as switching gates elements can ensure constant is a solution to maintain the output optical power by utilising the gain from amplifiers, but suffer from the ASE noise and distortion associated with the gain.

Therefore, a combination of two switching technologies is adopted in this chapter by implementing MZIs as switching gates and SOAs to compensate the passive loss. The almost lossless operation is demonstrated even in the longest path with an only 1.3dB loss. A dilated Beneš architecture is implemented to avoid the crosstalk within the MZIs. A -47dB crosstalk ratio is demonstrated with the dilated Beneš approach. Unlike SOA-based switches, the SOAs implemented in this design are relatively short, 230/250μm, and are driven with low injection current, 15/17mA, as they do not need to provide large gain to compensate the inherent splitter/combiner loss. The ASE noise and non-saturated distortion are then substantially reduced, and this ensures a low-power-penalty performance. A 14dB IPDR for a penalty less than 0.5dB is demonstrated. The IPDR performance has been further improved by actively controlling the injection current. The tolerance of the current control accuracy of this switch is very broad. Within a 5 mA bias current range, the power penalty can be maintained below 0.2 dB for 8 dB IPDR and 12 mA for 10 dB IPDR with a penalty less 0.5 dB. The active control, therefore, can be implemented easily.

The excellent crosstalk and power penalty performance demonstrated by this chip enable the scalability of this hybrid approach. The performance of large-scale hybrid switches is assessed in the next Chapter. The performance of 16×16 port dilated hybrid switch is assessed by cascading 4×4 switch chips. In terms of switches with the larger port count, quantitative analysis is conducted using physical layer simulations fitted using experimental data.

Chapter 6 Experimental Emulations and Simulations for Large Scale Switches

6.1 Introduction

Optical switches have the potential to replace the electronic switches and many of the optical transceivers currently used in the data centre folded Clos architecture and meet the size and bandwidth demands of future data centre networks [11][12][145]. The data centre networks in production today can connect as many as 100,000 servers [146]. Connecting all servers with a monolithic switch able to respond on nanosecond timescales is currently impractical, but using optical switches to connect electronically-aggregated racks could dramatically reduce the cost and complexity of the networks [147]. Given 50 servers per rack, 2,000 port switches would be required to connect all the racks in a data centre as shown in Figure 6.1.

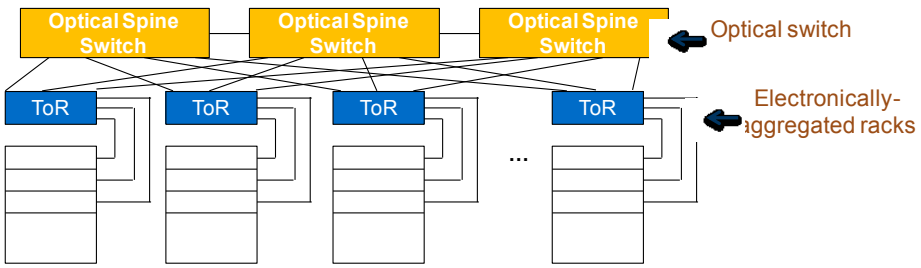

Figure 6.1 Data centre structure with optical switches connecting electronically-aggregated racks [148]

MEMS based optical switches have been fabricated with over 1,000 ports which meet the port count requirements [17]. However, MEMS switches have response times of the order of a millisecond which is not sufficient for some applications in datacentres, such as small message exchange across a large shared memory space. Opto-electronic devices, such as Mach-Zehnder Interferometers (MZIs) and semiconductor optical amplifiers (SOAs) with nanosecond response time have the potential to fulfil the requirements of packet switching. To allow

increased port count, we have proposed a novel scalable hybrid MZI-SOA approach with a dilated Beneš architecture. A 4×4 switch chip has demonstrated a 14dB IPDR for a penalty less than 0.5dB discussed in Chapter 5.

In this Chapter, the scalability of the hybrid dilated Beneš by cascading the 4×4 chips is investigated. The emulated 16×16 switch has demonstrated a record IPDR of 15 dB at a 1 dB penalty with a 0.6 dB power penalty floor. The experimental details and results are discussed in Section 6.2.

In terms of switches with a port count larger than 16×16, the power penalty performance can be simulated with physical layer simulations fitted using experimental data. A few topologies with hybrid MZI-SOA building blocks have the potential to build low power penalty large port count switches. We assess the feasibility of three potential topologies, with different architectural optimisations: dilated Beneš, Beneš and Clos-Beneš. Quantitative analysis for switches with up to 2048 ports is presented in Section 6.3.

6.2 Experimental Emulation for 16×16 Port Hybrid Switch

6.2.1 Design and the Testbed

Large-port-count hybrid switches can be constructed from smaller switch elements by implementing a dilated Beneš architecture [149]. As shown in Section 5.2.1, a 4×4 dilated Beneš switch contains four 2×2 dilated Beneš building blocks with each path containing two cascaded elements. Thirty-two 2×2 dilated Beneš building blocks in total are required to build a 16×16 switch. Each path goes through four 2×2 dilated Beneš blocks as shown in Figure 6.2. A path in a 16×16 switch can, therefore, be emulated by cascading two 4×4 switch chips [116].

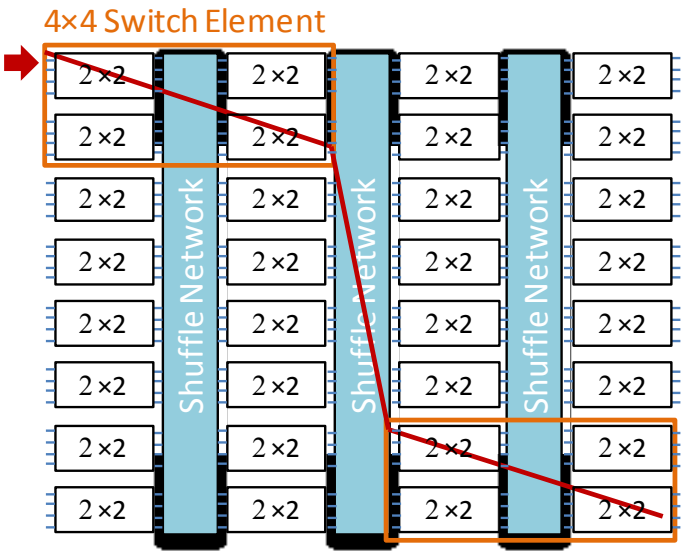

Figure 6.2 Schematic of emulated 16×16 switch

The emulated 16×16 switch has been assessed by measuring the power penalty. Figure 6.3 shows the experimental test-bed of the emulated 16×16 switch. A laser source with a wavelength of 1535.9 nm followed by a Mach-Zehnder modulator driven by a 10 Gb/s non-return-to-zero (NRZ) signal with 2^{31}-1 pattern length PRBS was used to generate the optical input to the chip. An EDFA was placed on the transmitter side to compensate the loss from the Mach-Zehnder modulator, the intrinsic loss of the VOA and the coupling loss from the lensed fibre. Two lensed fibres were used to connect two chips by coupling light out of the first chip and into the second chip. An EDFA was placed between two the chips to compensate the coupling loss. The total loss between the chips was adjusted to 1.5 dB, which represents the average loss within an integrated 16×16 shuffle network. The output was assessed by an error detector. Another EDFA was placed here to compensate the loss from the VOA and the lensed fibre.

All three EDFAs in the testbed were followed with a filter to reduce the ASE noise from the EDFAs. The measurement was also done without the filter by measuring the power penalty with and without the optical chip and calculating the difference between them [138]. Similar results were demonstrated using the two measurement methods.

The Back-to-Back performance was been measured by omitting two chips and lensed fibres from the system and connecting the transmitter part with the middle part and the receiver part.

The power penalty was then recorded as the difference in received power required achieving a BER of 10^{-9} in the presence and absence of the switch.

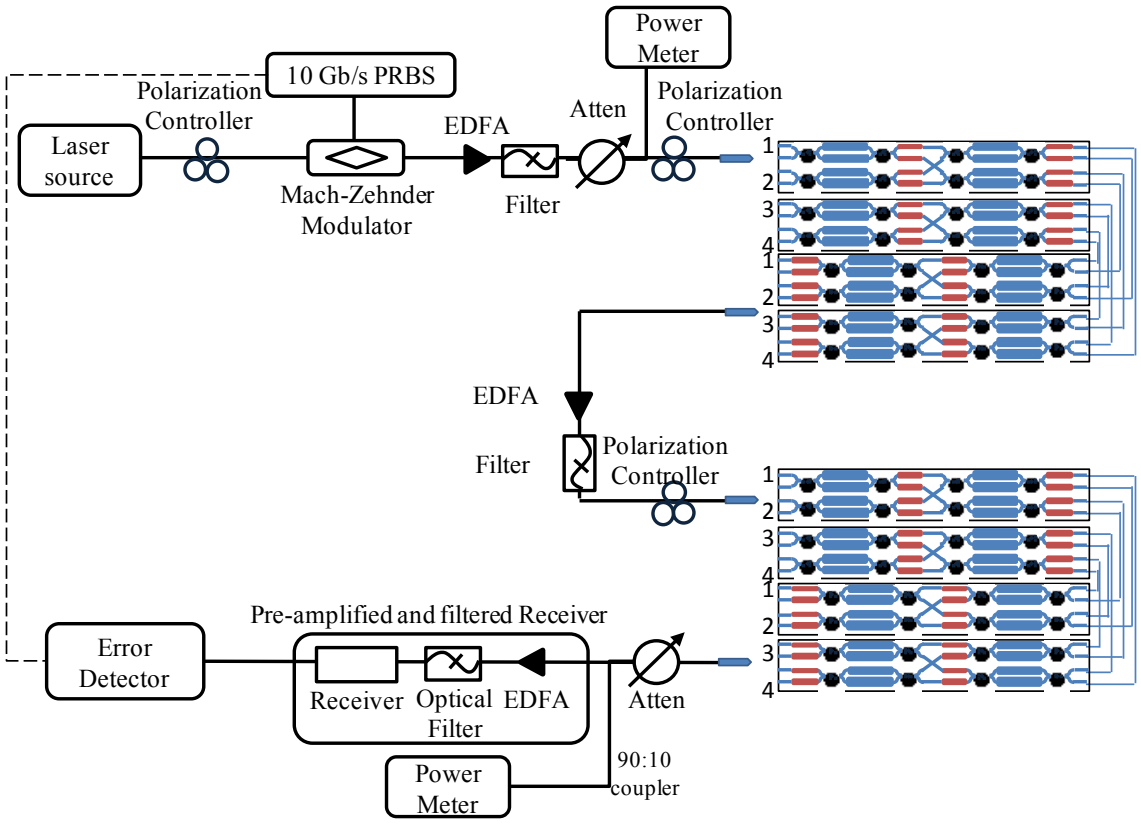

Figure 6.3 Experiment setup for cascaded measurement

6.2.2 Performance and Discussions

The two 4×4 switch chips used to build the 16×16 switch were also assessed individually. Both of them exhibited an IPDR of more than 13dB with a power penalty of less than 0.5dB. The emulated 16×16 switch has demonstrated a wide 15 dB IPDR for less than 1dB penalty as shown in Figure 6.4. A 0.6 dB power penalty floor has also demonstrated. The degradation of the performance compared with a single chip is due to the accumulated ASE noise and saturation induced distortion from more SOAs.

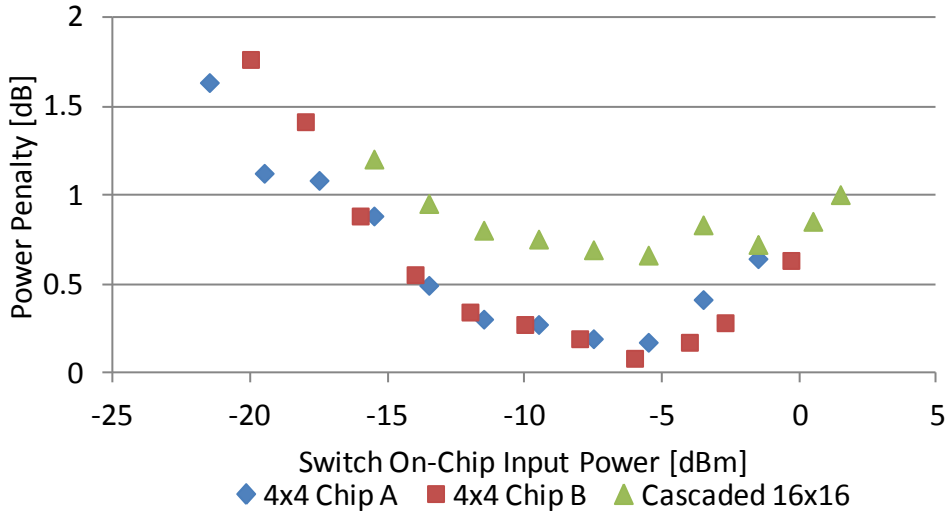

Figure 6.4 Power penalty as a function of switch on-chip input power for two 4×4 switch chips and the emulated 16×16 switch

While the switch state is in constant, the matched impedance in the driving circuit still results in power consumption. Therefore, similar to the individual 4×4 chips discussed in Section 5.4.1, a matched impedance is not implemented in the driving circuit as this would result in a constant power consumption Each path of the 16×16 switch requires 124mA for all eight SOAs. With a forward voltage of 1.0V, a fully loaded 16×16 switch consumes 1.980W. This corresponds to 12.4pJ/bit at a bit rate of 10 Gb/s. Compared with the active-passive SOA switches reported at the beginning of the last Chapter where an emulated 16x16 switch consumes 3.5W [150], the hybrid approach exhibits 43% lower-energy consumption.

This low-power-penalty low-energy-consumption performance enables further scaling up of this hybrid switch. The emulation of switches with larger port counts, however, is not possible due to lack of equipment limitation. Quantitative analysis by simulation for switches with more than 16×16 port count is presented in the next section.

6.3 Simulations for Switch with Up to 2048 Port Count

6.3.1 Hybrid Switch Design Methodologies

Figure 6.5 shows a N×N hybrid MZI-SOA switch with a dilated Beneš architecture. This hybrid dilated Beneš has been explained in details in Section 5.2.1. In this design, MZIs are used as 1×2 or 2×1 port low-loss switching elements, minimizing crosstalk by having a single input [72]. A short SOA is linked to each output of MZI. Once the signal is routed to an output, the corresponding SOA is turned on in order to compensate for the loss from other passive components. The SOA connected to the other output is in the OFF state and suppresses crosstalk. With a full connection assignment, only half of the waveguides route signal and half of SOAs are in the ON state.

The total number of cascades2×2 hybrid building blocks, which consists of an MZI and two short SOAs, is calculated using Equation (6.1). The total number of building blocks required for a N×N switch is shown in (6.2).

$$n = 2 \times \log_2 N \tag{6.1}$$

$$B = 2 \times N \times \log_2 N \tag{6.2}$$

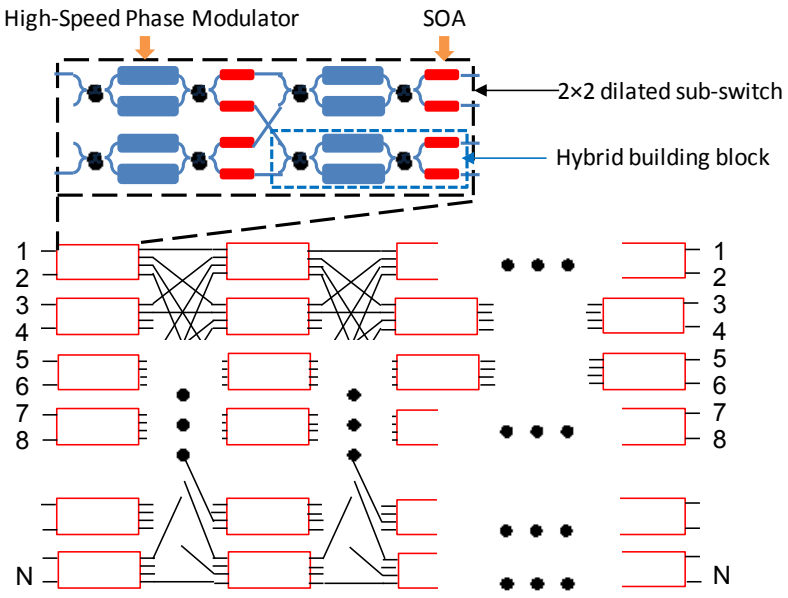

Figure 6.5 Building block and schematic of the scalable dilated Beneš network

where n is the number of cascades, N is the port counts and B is the total number of building blocks. This design significantly reduces the crosstalk introduced by building blocks. The loss from the required passive shuffle networks, however, grows substantially with increasing port count, which is likely to greatly degrade the performance of the large-port-count switches.

Figure 6.6 shows a N×N hybrid switch using a Beneš topology. As described in Section 3.3.6, the Beneš architecture can be constructed recursively by using N/2×N/2 Beneš switches as middle-stage sub-switches until 2x2 middle-stage sub-switches are reached. Here the MZIs are used as 2×2 switching elements, and short SOAs are included to compensate the loss. The number of cascades of 2×2 hybrid building blocks required for a N×N port-count Beneš switch is shown in Equation (6.3) [65]. The number of building blocks required is calculated by Equation (6.4).

$$n = 2 \times \log_2 N - 1 \tag{6.3}$$

$$B = N \times \log_2 N - \frac{N}{2} \tag{6.4}$$

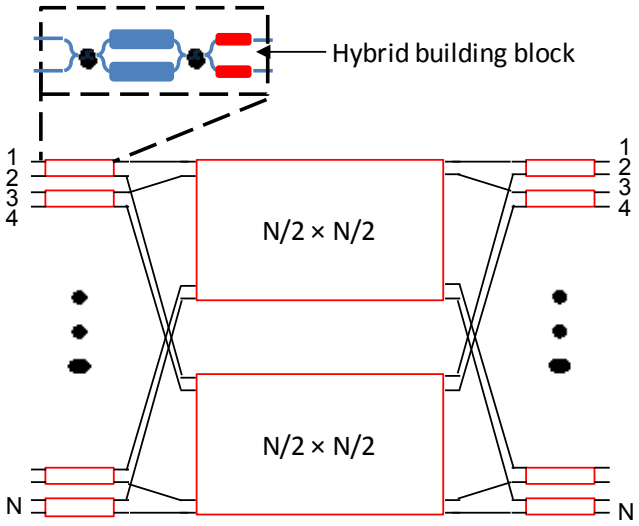

Figure 6.6 Building block and schematic of the scalable Beneš network

Compared with the dilated Beneš architecture, the crosstalk introduced by the building blocks cannot be mitigated, but the number of building blocks required is substantially reduced. The loss of the shuffle networks reduces from the outer layers to the inner layers.

Figure 6.7 shows a N×N hybrid switch using the Clos-Beneš architecture. The sub-switches adopt the Beneš architecture and are inter-connected with the Clos architecture. Each Beneš sub-switch is constructed using 2×2 hybrid building blocks. Beneš sub-switches in the first and last stage have a size of d×d. The middle-stage sub-switches have a size of N/d × N/d. The total number of cascaded 2×2 hybrid building blocks in a path is shown in Equation (6.5) [64], and the total number of building blocks required in Equation (6.6).

$$n = 2 \times \log_2(d \times N) - 3 \tag{6.5}$$

$$B = N \times \log_2(d \times N) - \frac{3 \times N}{2} \tag{6.6}$$

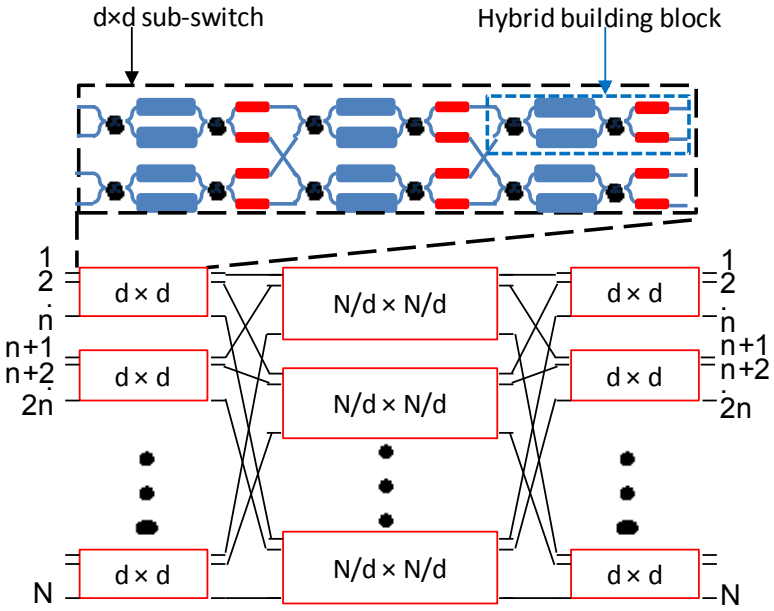

Figure 6.7 Building block and schematic of the scalable Clos-Beneš network

Similar to the switches using the Beneš architecture, this design has lower immunity to the MZI-induced crosstalk. The full-size shuffle networks between the sub-switches account for a large fraction of loss. The loss from the shuffle network within the Beneš sub-switches is much smaller than the inter-sub-switch shuffle network.

Table 6.1 summarises the number of stages and building blocks of these three topologies. The loss in the switch is introduced by the passive components in the 2×2 hybrid building blocks and by the waveguides in the shuffle networks. The accumulated loss is one of the significant factors determining the performance of the switch.

The Dilated Beneš architecture has the lowest number of building blocks but potentially the largest loss from the shuffle networks for large-scale switches. Clos-Beneš architecture, however, has the most cascaded 2×2 hybrid building blocks but relatively shorter waveguides, especially for large-port-court switches. The quantitative analysis of the total accumulated loss and optical performance is presented in the next section.

Table 6.1 Summary of switch architectures

Architecture	Number of Stages	Number of Building Blocks
Dilated Beneš	$2 \times \log_2 N$	$2 \times N \times \log_2 N$
Beneš	$2 \times \log_2 N - 1$	$N \times \log_2 N - \frac{N}{2}$
Clos-Beneš	$2 \times \log_2(d \times N) - 3$	$N \times \log_2(d \times N) - \frac{3 \times N}{2}$

6.3.2 Quantitative Evaluation

The accumulated loss from all passive components for each topology with different port count has been calculated with the state-of-the-art loss parameters available in the foundry as shown in Table 6.2.

Table 6.2 State-of-the-art loss parameters

Component	Loss
Passive Waveguide	-1dB/cm [102]
Waveguide 2x2 MMI	-0.2dB [115]
Phase modulator	-0.5dB [115]
SOA Transition Element	-0.3dB [115]
S-bend / C-bend	-0.1dB [117][151]
Waveguide Crossing	-0.05dB [117]

We investigate the performance of switches with port count ≥ 128. Figure 6.8a shows the average accumulated losses for each topology.

The dilated Beneš topology has the largest overall unamplified loss. The switch with 128 ports exhibits 77.3 dB accumulated loss and the switch with 256 ports has 139.8 dB loss. The loss from the waveguides in the shuffle networks accounts for most of the accumulated loss. The

waveguides loss soars with the port count and inevitably leads to a considerable amount of loss in dilated Benes switch.

The Beneš topology and Clos-Beneš topologies demonstrate similar overall loss for the same switch size. A Clos-4×4Beneš switch has 4×4 Beneš sub-switches in its first and last stages. The size of middle-stage sub-switches varies with of the size of the whole switch. The 128×128 port-count Beneš switch shows 45.6 dB loss. For both the Beneš and Clos-Beneš topologies, the passive loss from the 2×2 building blocks dominates the overall loss of the switch port count equal or smaller than 256. For switches with greater than 256 port count, the loss from the shuffle networks dominates.

The loss mismatch between two phase modulator arms and imperfect MMI split ratio leads to crosstalk between two signals within an MZI. The planar design of switch inevitably leads to waveguide crossings. 90° tapered crossings are reported and used on many platforms to reduce the possible crosstalk between two waveguides. The state-of-the-art crosstalk parameters used for the quantitative analysis are shown in Table 6.3.

Table 6.3 State-of-the-art crosstalk parameters

Component	Crosstalk
MZI	-30dB [152]
Waveguide Crossing	-45dB [153]

The aggregate crosstalk in those switches has also been evaluated (Figure 6.8b). We assume the crosstalk from the MZIs and waveguides is coherent in phase, which results in the worst case. The dilated Beneš topology is designed with the purpose to minimise crosstalk. Hence, the dilated 128 port Beneš switch shows an excellent -21.2 dB crosstalk compared with the other topologies. The dilated Beneš switch topology with more than 512 ports, however, shows worse performance compared with other topologies. This is caused by increasing number of crossings in the shuffle network. The 1024 port dilated Beneš switch has nine shuffle networks, and each shuffle network has 320 active crossings (only half of the crossings are active in the dilated Beneš topology). The Beneš and Clos-Beneš topologies demonstrate similar aggregate

crosstalk with the same switch size with the Beneš topology showing a slightly smaller aggregate crosstalk. The Clos-Beneš Switches with larger size sub-switches show higher aggregate crosstalk because of a greater number of MZIs.

6.3.3 Penalty Evaluation

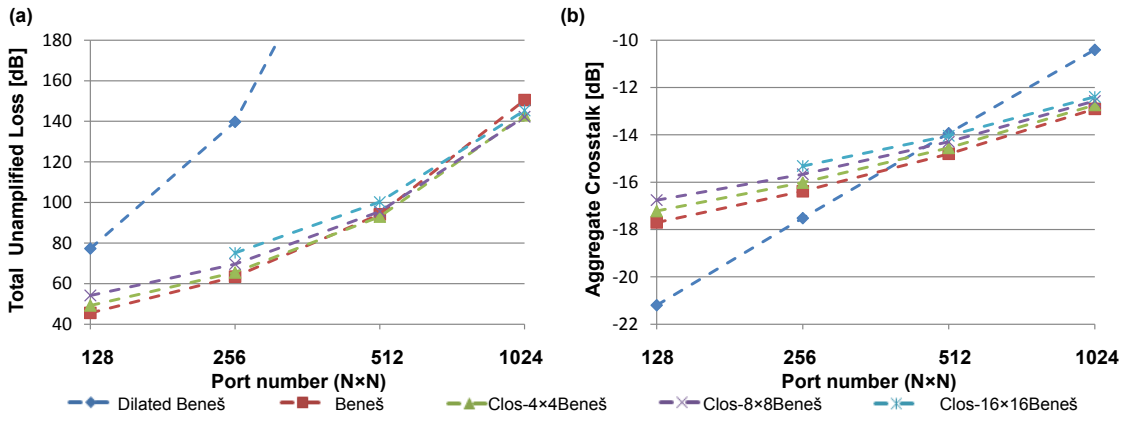

Figure 6.8 (a) Accumulated average loss from passive component and (b) Aggregate crosstalk from MZIs and waveguide crossings of hybrid switches with different topologies as a function of port number

The power penalties of these hybrid switch designs can be evaluated using the commercial VPI simulator with parameters fitted from experimental data [154]. Figure 6.9 shows the modelling schematic of a 128×128 Clos-4×4Beneš Switch. The power penalties were studied with 10Gb/s single-channel NRZ input signals. VOAs are used to represent the loss from passive components. The aggregate crosstalk is represented by a crosstalk source which is not correlated with the signal. Power penalties were recorded at bit error rates of 10^{-9}, 10^{-5} and 10^{-3}, corresponding to the operation with no Forward Error Correction (FEC), hard decision and soft decision FEC, respectively.

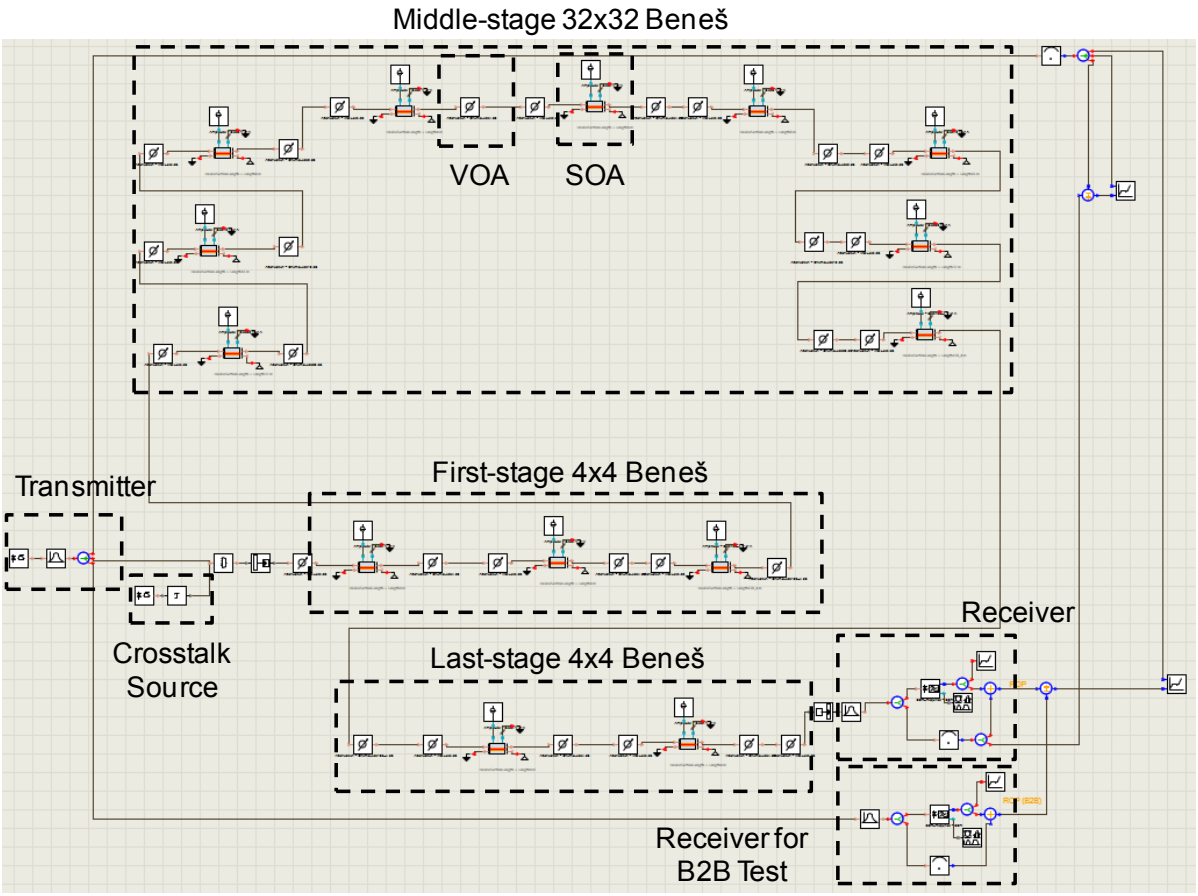

Figure 6.9 Modelling schematic of a 128×128 Clos-4×4Beneš switch

Figure 6.10 shows the power penalty floor of all topologies with bit error rates at 10^{-9}, 10^{-5} and 10^{-3}. The 128 port dilated Benes based switch can operate with a moderate power penalty of 1dB without FEC. Scaling the switch beyond this introduces higher penalties, mandating the use of FEC. A 256 port dilated Beneš switch exhibits a 1.28dB and 0.73 dB penalties with hard and soft decision FEC, respectively. Larger dilated Beneš switches exhibit more than 3 dB penalty even with soft decision FEC.

≤256 port count Beneš and Clos-Beneš topologies demonstrate higher power penalties. 512 port count switches can be achieved with these topologies. The Beneš switches show the lowest penalty between the two but the difference is insignificant. Clos-Beneš Switches with larger size sub-switches show the largest penalty.

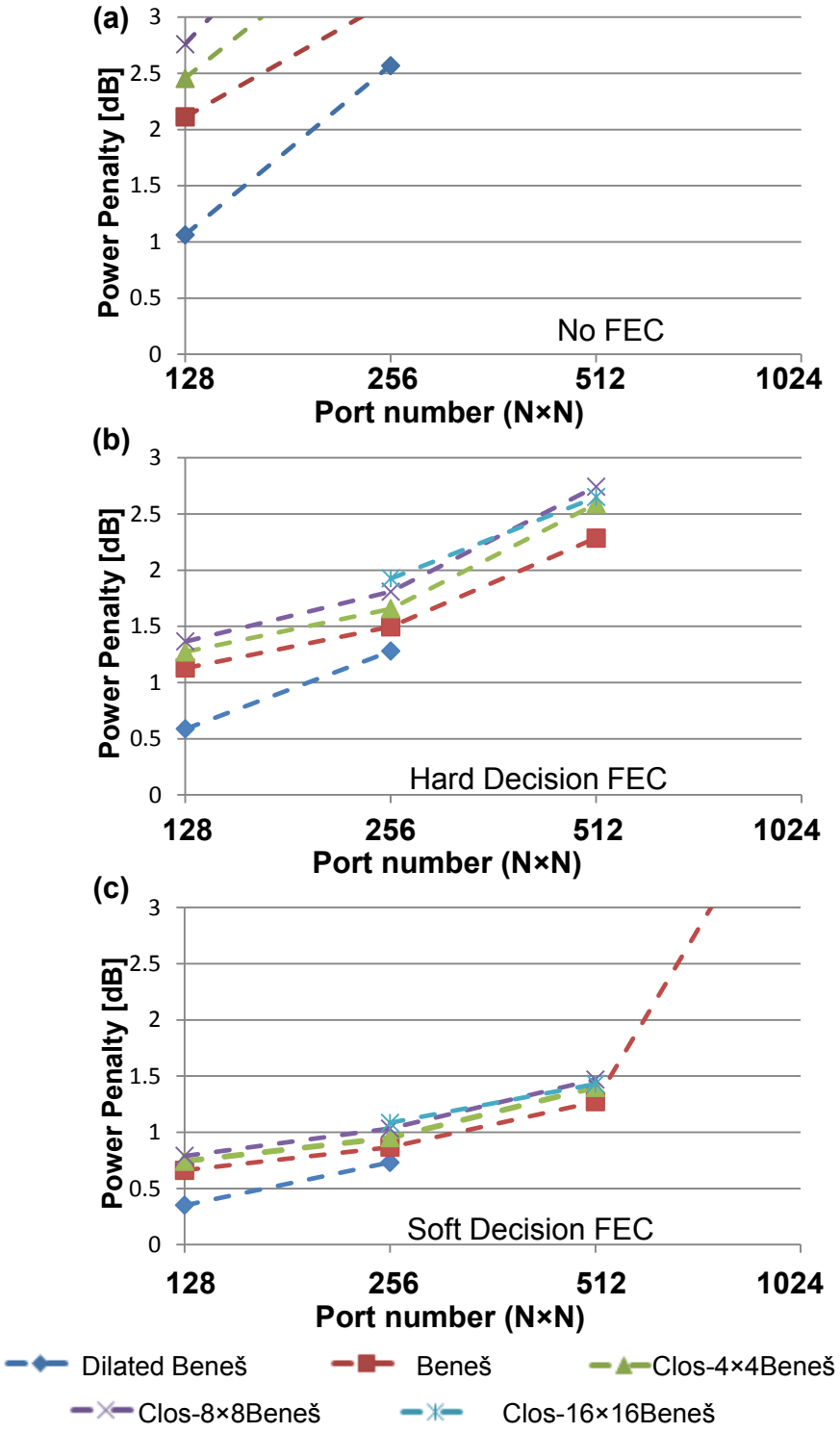

Figure 6.10 Power penalty floor of hybrid switches with different topologies as a function of port number for (a) No FEC BER=10^{-9} (b) Hard decision FEC BER=10^{-5} and (c) Soft decision BER=10^{-3}

6.3.4 Fibre Interconnect

It was noted in the previous section that the major shuffle networks between the Beneš sub-switches account for a large fraction of the switch loss. Table 6.4 shows the average loss introduced by the large shuffle network for Clos-Beneš switches.

Table 6.4 Average loss introduced by major shuffle network in Clos-Beneš networks

Structure	128	256	512	1024
Clos-4x4Beneš	4.1dB	8.1dB	16.1dB	32.1dB
Clos-8x8Beneš	4.4dB	8.8dB	17.6dB	35.2dB
Clos-16x16Beneš	N/A	9dB	18.2dB	36.6dB

With increasing switch size, the loss from the large shuffle network reaches a substantial level. The shuffle network in a Clos-16×16 Beneš introduces 36.6 dB loss into the link. This loss needs to be compensated by the gain from SOAs which reduces the optical signal to noise ratio (OSNR) due to the additional ASE noise.

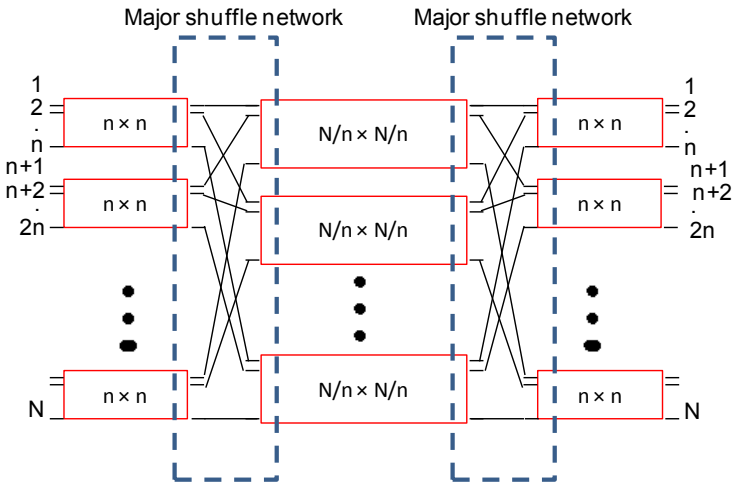

Figure 6.11 Major shuffle network in Clos-Beneš networks

One of the purposes of optical integration is to eliminate the coupling loss between discrete components. The loss introduced by integrated waveguides, however, is much larger than the coupling loss. Hence, in terms of very large size port count optical switches, rather than

fabricating all components on a monolithic chip, using fibre ribbons to interconnect the sub-switches mitigates the loss from the large shuffle networks as shown in Figure 6.11. Hence, 0.5 dB chip-to-fibre coupling loss is assumed.

Figure 6.12a shows the average accumulated loss for the Clos-Beneš switches with inter-sub-switch fibre links along with the results from the integrated topologies. The switches with fibre links show a reduced loss, especially for switches with a larger port count.

The shuffle networks constructed by fibre ribbons do not have any crossings and hence there is no crosstalk introduced by the shuffle networks. The aggregate crosstalk, therefore, is substantially reduced as shown in Figure 6.12b.

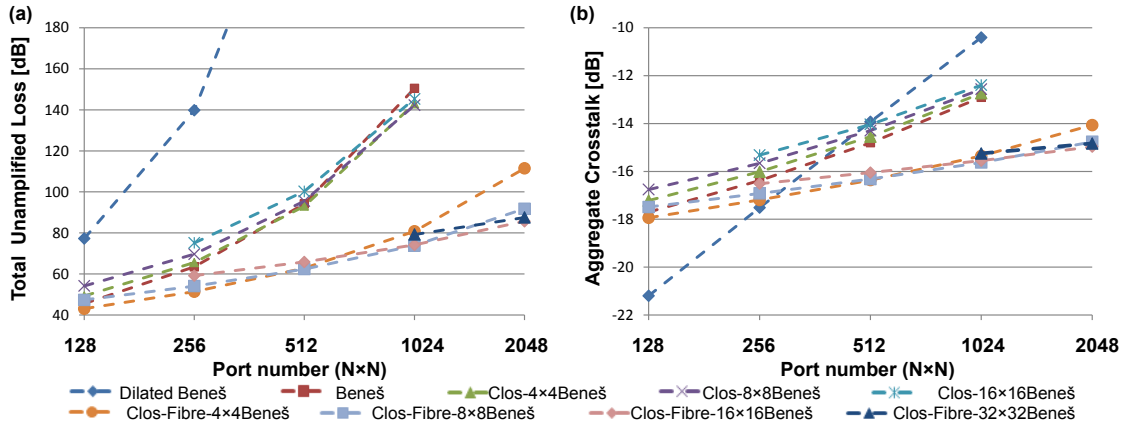

Figure 6.12 (a) Accumulated average loss from passive component and (b) Aggregate crosstalk from MZIs and waveguide crossings of hybrid switches with additionally topologies as a function of port number

6.3.5 Switches with 2048 Port Count

The VPI simulator has also been used to evaluate the power penalties of these Clos-Beneš switches with fibre interconnects. The power penalty floors of all previous and modified topologies are shown in Figure 6.13.

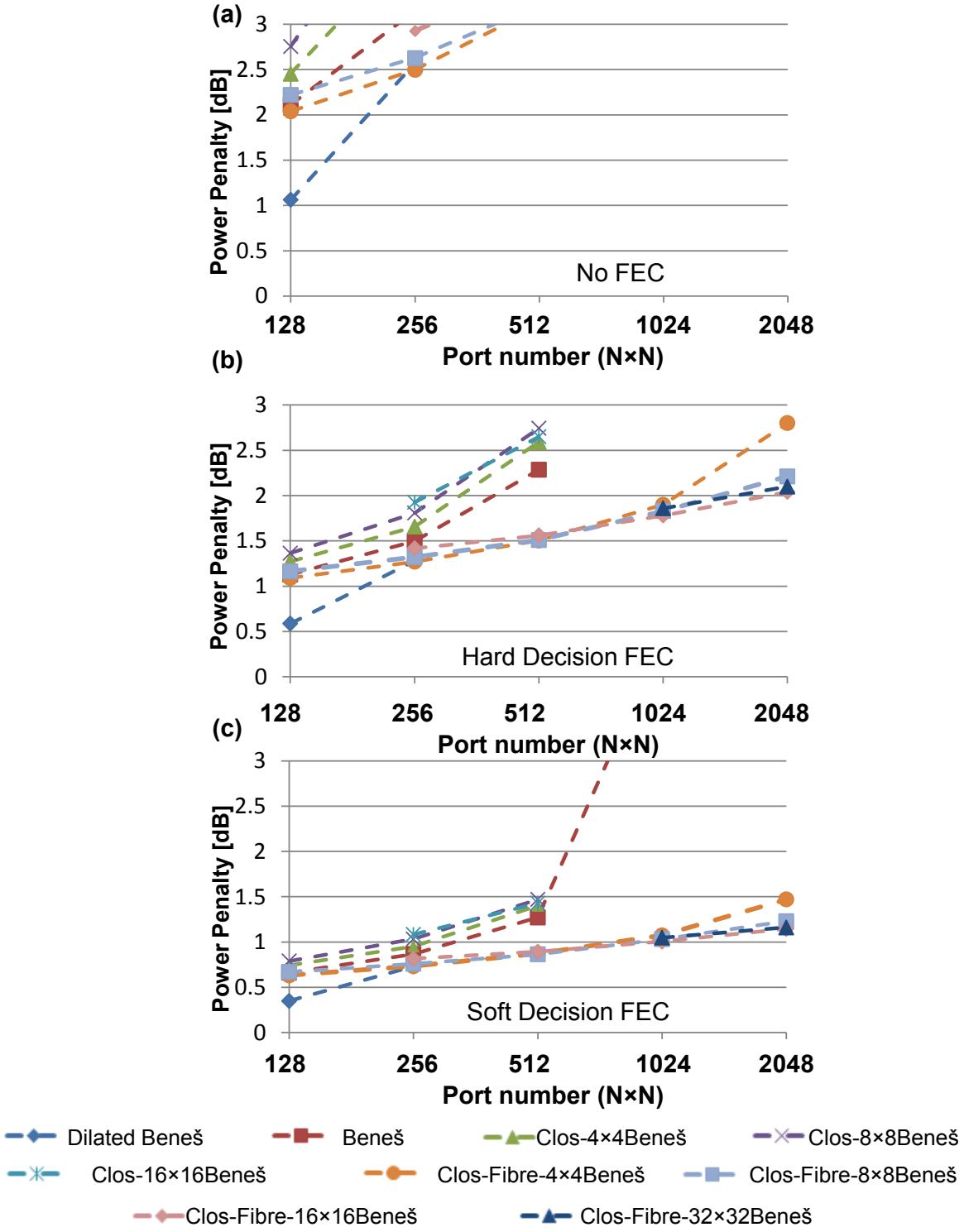

Figure 6.13 Power of hybrid switches with additional different topologies as a function of port number for (a) No FEC BER=10^{-9} (b) Hard decision FEC BER=10^{-5} and (c) Soft decision BER=10^{-3}

2048 port switches are shown to be feasible all Clos-Fibre-Beneš designs with 4×4, 8×8, 16×16 and 32×32 port count sub-switches. Clos-Fibre-Beneš topologies with the larger first and last stage sub-switches demonstrate better power penalty performance. Using three stages of sub-switches, with port counts of 32×32, 64×64 and 32×32 respectively and operating with hard decision FEC, a power penalty of 2.1 dB is predicted. If soft-decision FEC is allowed, then 2048 ports can be achieved in the fibre interconnect based Clos-Benes architecture with a power penalty of 1.16dB. This again uses similarly sized sub-switches of 32×32, 64×64 and 32×32 ports.

In these larger switches, the dominant impairments come from waveguide loss. The use of a Clos architecture with similarly sized sub-switches minimizes the waveguide loss within each sub-switch. Furthermore using fibre ribbons within the inter sub-switch interconnects further minimizes loss. This has the added benefit of reducing the maximum size and complexity of the largest single photonic integrated circuit, improving fabrication yield and control complexity of the sub-switches. This is the reason why the 32×32, 64×64 and 32×32 switch performs better than a 4×4, 512×512, 4×4 port sub-switch alternative.

6.4 Conclusions

The excellent crosstalk and power penalty performance demonstrated by the 4×4 chip enables the scalability of the hybrid approach. The scalability of the hybrid dilated Beneš design has been experimental assessed by cascading the 4×4 chips. A 16×16 switch has been emulated by two 4×4 chips. An IPDR of 15 dB with lower than 1 dB penalty and 0.6 dB power penalty floor has been demonstrated.

The performance of hybrid switches with larger than 16×16 port count has been analysed with physical layer simulations fitted with state-of-the-art fabrication data. The feasibility of three potential topologies, with different architectural optimisations: dilated Beneš, Beneš and Clos-Beneš, has been assessed. The Clos-Beneš structure with a hybrid fibre-integration approach, which includes 32×32 chips as input/output sub-switches and 64×64 chips as the middle stage switches, achieves 2048 ports with a 1.15dB penalty for a BER of 10^{-3}, compatible with soft-decision forward error correction. The use of inter-sub-switch fibre connection eliminates the

waveguide loss from full-size shuffle networks. Using the Clos-Beneš architecture with similarly sized sub-switches minimizes the waveguide loss within each sub-switch and eases the complexity of fabrication.

Chapter 7 Conclusions and Future Work

7.1 Summary

The advance of internet applications, such as video streaming, big data and cloud computing, reshapes the telecommunication and internet industries. Bandwidth demands in datacentres have been boosted by those emerging data-hungry internet applications. These applications place considerable requirements on datacentre interconnection networks which must exchange fine-grained communication signals between nodes at high data-rates. Currently, optical fibre point to point links and electronic switching fabrics are used to realise the switched interconnect. At each optical/electrical interface, the signal is generated or detected, and often multiplexed or demultiplexed. Each wavelength division multiplexed (WDM) channel requires its own opto-electronic (OE) and electro-optic (EO) conversion which consumes a substantial amount of energy. In terms of performance scaling, the aggregate capacity of electronic switch chips is not keeping up with intra-datacentre traffic. For next generation intra-datacentre networks, optical switching fabrics are promising candidates to allow low power and low-latency communication.

A range of optical switching technologies, such as MEMS, thermo-optics, liquid crystal and acousto-optics have been studied. MEMS switches are notable and have been available both as research demonstrations and in commercial products. 3D MEMS-based switches have been realized with over 1000 ports, and can also provide wavelength- and polarization-independent operation with low insertion loss. However, this type of cross-connect uses beam-steering technology which limits its response time to the order of 10 milliseconds; this is not fast enough for packet switching in datacentres. Recently, the reconfiguration speed of modest port count MEMS-based switches has been improved to the sub-microsecond level by adopting Silicon photonics. This had a compact 7×7 mm^2 footprint for a 64×64 port count and also has achieved

better than -65 dB extinction ratio. However, sub-microsecond reconfiguration time still only accommodates latency-insensitive data migrations.

For advanced data-centre applications, suitable optical switching technologies should feature nanosecond response times. Electro-optic and SOA-based switches demonstrate the capability to switch signals at nanosecond timescale. SOA-based switches can be fabricated on III-V materials, such as InGaAsP/InP. The platform enables the integration of both active and passive optical components. SOAs can compensate for the insertion loss of the passive components, offer lossless operation. However, high port court SOA-based switches are extremely challenging since accumulated amplified spontaneous emission (ASE) noise and gain-saturated distortion substantially degrade the system performance as the total required SOA gain grows. Electro-optic Mach Zehnder modulators noiseless operation and can be fabricated with silicon-photonics and III-V materials. The MZIs which adopt the reversely biased phase modulator demonstrate low-power consumption, as energy is only required during transitions. However, imperfect coupler split ratio and loss mismatch within the arms lead to poor crosstalk with the MZIs. Limited crosstalk performance around -20dB is featured by the integrated MZIs. Large MZI-based switches built by cascading MZI elements inevitably suffer from the accumulated crosstalk.

Large optical switches are constructed by connection 2×2 basic switch elements with network architectures. There are trade-offs between different architectures in terms of the total number of building blocks and the blocking characteristic. The number of building blocks required for constructing strict/wide sense non-blocking switches increases exponential with the port count of switches. In contrast, rearrangeably non-blocking architectures require fewer building blocks. More complex routing algorithms, however, are needed to set up paths via the switch. In terms of different kinds of rearrangeably non-blocking architectures, the trade-off also exists between the crosstalk performance and the number of building blocks. The dilated Beneš architecture almost doubles the number of building blocks compared with Beneš architecture, while greatly reducing the crosstalk. For large-scale optical switches, dilated Beneš architecture demonstrates the most balanced performance in terms of the number of building blocks, the number of stages and crosstalk performance.

Multi-stage rearrangeably non-blocking architectures require routing algorithms to select the middle-stage sub-networks to set up paths for the given connection assignments. The looping algorithm is the classical routing algorithm which has been proposed for Base 2 switches. It is also extended to all Beneš, Clos and dilated Beneš architectures. However, there is a common issue for the looping algorithm - they always regulate the first link of each loop via the upper middle network. It works well with electronic networks as all links are equal. With optical integrated networks, links have different losses from waveguides, bends and crossings. The set-up established by the looping algorithm might lead to paths with an unnecessarily large loss, which comes with sub-optimal performance.

In Chapter 4, we, therefore, propose an advanced path-selection algorithm based on the looping algorithm that minimizes the path-dependent loss. It explores all possible set-ups for a given connection assignment and selects the optimal one. It guarantees that no individual path would have a sufficiently large loss, therefore, improve the overall performance of the switch. It, however, requires high-speed processors to construct all set-ups and calculate the optimal one with on-the-fly computation. Running the advanced routing algorithm off-line and storing its output of each assignment in a look-up table is a practical way to enable fast switch reconfiguration. The look-up table, however, has an inevitable considerable size as it is the factorial of the number of input ports. If the path dependent loss within input- and output-stage sub-switches is insignificant compared with shuffle networks, the size of look-up table can be greatly reduced by only considering the permutation between input- and output-stage sub-switches. For an 8×8 Clos-tree switch, all 40302 connection assignments can be trimmed to 282 connection matrixes. It is therefore practical to adopt an off-line algorithm and a look-up to enable fast reconfiguration. For the 8×8 switch layout shown in Chapter 4, eight connection matrixes demonstrate a loss reduction exceeding 2.7 dB for the lossiest path. The optical performance has been assessed by using the VPI simulator, 1.9 dB IPDR improvement for penalties less than 1.5dB is demonstrated. In terms of 16×16 Clos-tree switch, the size of the look-up table can be reduced from 20.9 trillion to 10147 by using the permutation matrix method. The loss improvement between the input- and output-stage sub-switches has a significant loss reduction exceeding 3dB. However, in this 16×16 switch design, this loss is of the same magnitude with the loss difference within 4×4 sub-switch (2.6 dB variance).

Therefore, considering only the loss improvement between the input- and output-stage sub-switches is not sufficient with this switch design, computing the loss between individual terminals is necessary in this case. In terms of the 8×8 dilated Beneš switch layout, the 0.7 dB loss between bar and cross states of the 2×2 dilated building blocks are insignificant compared with the loss in shuffle networks between stages. The permutation matrix method is, therefore, can be used to trim the size of the look-up table to 282. 18 of 282 connection maps show more than 4 dB loss reduction for the lossiest path. The IPDR with 1 dB power penalty for the lossiest path has been reduced by 1.4 dB.

In chapter 5, a hybrid approach has been adopted to include MZIs as the switching elements and short (and hence low power) SOA elements as both gain and absorption elements to enable both loss compensation and crosstalk suppression, enhancing scalability [7]. Crosstalk in this hybrid approach is further reduced by using a dilated Beneš scheme. A 4×4 hybrid switch has been fabricated using a generic foundry within the EU FP7 PARADIGM project. The chip is constructed by using predefined generic building elements, such as SOAs, phase modulators and waveguides, to enable the reliable design, layout and fabrication of photonic integrated circuits. The almost lossless operation is demonstrated even in the longest path with an only 1.3dB loss. A -47dB crosstalk ratio is demonstrated with the dilated Beneš approach. A 14dB IPDR for a penalty less than 0.5dB is also demonstrated. The IPDR performance has been further improved by actively controlling the injection current. The tolerance of the current control accuracy of this switch is very broad. Within a 5 mA bias current range, the power penalty can be maintained below 0.2 dB for 8 dB IPDR and 12 mA for 10 dB IPDR with a penalty less 0.5 dB. The active control, therefore, can be implemented easily. When operating with 10 Gb/s per port, the energy efficiency is of the chip 6pJ/bit, delivering 20% reduced energy consumption compared with SOA-based switches.

The excellent crosstalk and power penalty performance demonstrated by this chip enable the scalability of this hybrid approach. The scalability of large-scale hybrid switches is assessed in Chapter 6. The performance of 16×16 port dilated hybrid switch is experimentally assessed by cascading 4×4 switch chips. The emulated 16×16 switch has demonstrated a record IPDR of 15 dB at a 1 dB penalty is achieved with a 0.6 dB power penalty floor. It demonstrates 12.4pJ/bit at a bit rate of 10 Gb/s, 43% lower than the energy consumption of SOA-based

switches. In terms of switches with a port count larger than 16×16, the power penalty performance has been analysed with physical layer simulations fitted with state-of-the-art data. In addition to dilated Beneš, we have also assessed the scalability of two other potential topologies: Beneš and Clos-Beneš. The MZI-SOA switch in a Clos-Beneš structure with a hybrid fibre-integration approach, which includes 32×32 chips as input/output sub-switches and 64×64 chips as middle-stage switches, achieves 2048 ports with a 1.15dB penalty for a BER of 10^{-3}, compatible with soft-decision forward error correction. The use of inter-sub-switch fibre connection eliminates the waveguide loss from full-size shuffle networks. Using Clos-Beneš architecture with similarly sized sub-switches minimizes the waveguide loss within each sub-switch and eases the complexity of fabrication.

To conclude, this thesis studies the advanced-algorithm and hybrid-design approach to improve the performance of large-scale integrated switches. It opens a route towards the design, implementation and control of high-port-count optical switches.

7.2 Future Work

A few next-step research ideas have been already been proposed and discussed or even modelled and tested. The feedback loop has been proposed to precisely control the bias of the MZI and in turn minimize the crosstalk. Early-stage simulations have been done and discussed. The hierarchical control layer is the proposed solution for the future switch control circuit. A fully functional switch system can be constructed by implementing the hierarchical control layer into the control circuits. The research of the hybrid optical switch for the quantum communication has already been conducting. The modelling of the quantum switch has been built and proof-of-concept test-beds have also been constructed.

In addition to those approaches, the redundancy of the switch also can be studied. When a number of building blocks are not functioning, the modified architectures or control algorithms might keep the switch still functioning.

7.2.1 Feedback Loop to Control MZI Bias

The dilated Beneš architecture demonstrates excellent crosstalk performance, regardless of imperfect coupler split ratio and loss mismatch within two arms. It, however, almost doubles the number of building blocks compared with Beneš architecture to achieve the same port count. The cost of the fabrication is larger, and the fabrication yield is inevitably lower.

Figure 7.1 shows another potential method to reduce crosstalk value without using dilated Beneš architecture. The crosstalk ratio can be reduced by actively adjusting the DC bias of phase modulators. Before the operation with data, the switch goes through a calibration phase, where the offset voltage of phase modulators is measured. The SOAs following the MZIs are utilised as power meters here. The offset voltage maximises the power at the corresponding port and minimises the power at the other port. The details of the calibration are listed below.

1. A training single (CW wave) is routed from In#1 to Out #2.
2. In an ideal case, all power is expected to be received at Out#2. In real case, certain amount of signal power goes to Out#1
3. Two SOAs detect the powers going to Out#1 and Out#2.
4. The photocurrent is measured by current meters.
5. The control circuits then adjust the bias voltages of two phase modulators in order to maximise the power at Out#2 and minimise the power at Out#1.
6. The optical bias voltages are then recorded and used in the following operation.

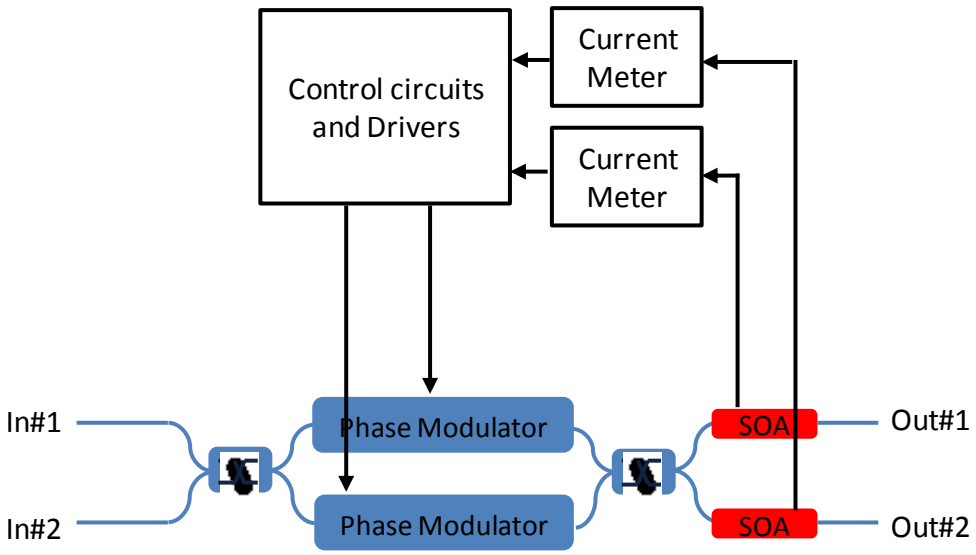

Figure 7.1 Mach-Zehnder modulator with feedback loop

7.2.2 Four Hierarchical Control Layer

Control circuits and drivers are needed to bias the corresponding SOAs and MZIs to set up paths for the given connection assignments [155]-[168]. In terms of large-size optical switches, they usually adopt a hybrid architecture, such as Clos-Beneš. The connections need to be set up first between Beneš sub-switches and then within the Beneš sub-switches. The bias voltage/current for SOAs and MZIs also needs to be adjusted [169][170].

To manage the complexity of the control functions for large-size rearrangeably non-blocking switches, a layered control [171] is proposed. As shown in Figure 7.2, four hierarchical control layer are implemented to set up paths.

- Arbiter – allocating transmission slots for the given connection assignment
- Routing Table - Clos – setting up connection between Beneš sub-switches
- Routing Tables - Benes – determining the set-ups within Benes sub-switches
- MZI & SOA Controllers – adjusting the bias for individual SOAs and MZIs

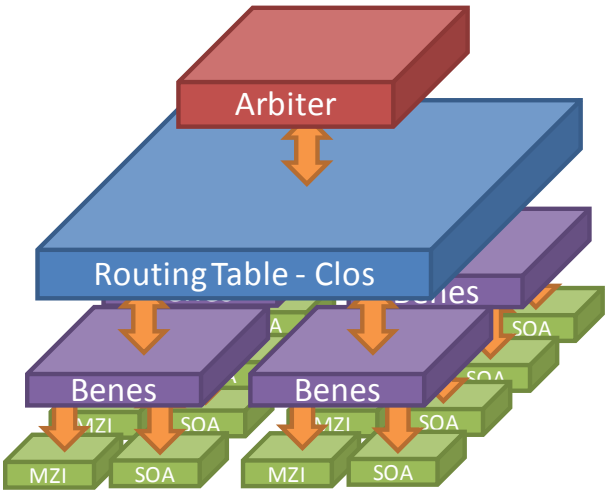

Figure 7.2 Four hierarchical control layer

The bias voltage and current in the MZI & SOA controllers are adjusted in the calibration phase and implemented in the operation phase:

Phase #1: Calibration – all paths are sequentially tested. The appropriate biases for MZIs and SOAs to achieve lossless and lower penalty operation are determined and stored in the MZI and SOA controllers

Phase #2: Operation – the MZI & SOA controllers set the appropriate bias for individual elements based on allocated routes.

7.2.3 Hybrid Optical Switch System for Quantum Communication

Quantum key distribution (QKD) links have attracted much research interest recently [172]. The QKD links between two parties have been demonstrated and implemented [173]. To extend the secure communication between multiple users, the idea of quantum secured routes (QSR) are proposed [174]. The QSR routes both classical and QKD signals simultaneously (Figure 7.3). In terms the link between the transmitter/receiver and the router, the classical and QKD signals are multiplexed together [175], trimming the cost of fibre instalment [176]. In this coexistence scheme, the classical signal and QKD signals are placed at different transmission band to mitigate the effect of Raman scattering on the weak QKD signal [177]. These two signals are de-multiplexed by the QKD drop filter and routed separately by different

parts of the switch on the QSR chip. The hybrid switch presented in this thesis is used to route classical signals due to its lossless, low-penalty, low-energy-consumption and high-reconfiguration-speed characteristics. Individual wavelengths in the classical channel can be routed separately in this design. The QKD signal is very weak and sensitive to noise. The ASE noise introduced by SOAs will critically damage the QKD signal. The pure MZI switch is then adopted to route the QKD signals. The switched classical and QKD signals are combined at QKD add filters and transmitter to the receivers.

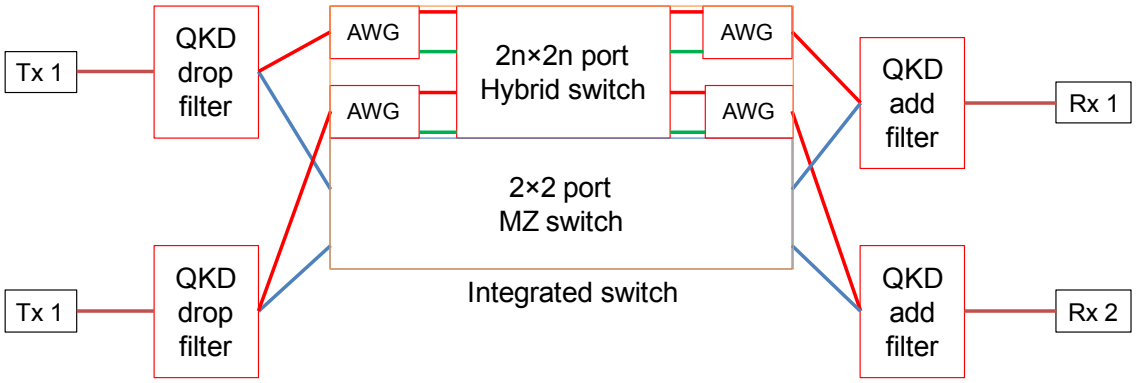

Figure 7.3 Schematic of a quantum secured router

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Appendix

A1. Gain-Induced Distortion

Ultra short optical pulses are adopted in the current communication system. As the input pulse width is comparable to the carrier lifetime in SOAs, the saturated gain has time to recover before the trailing edge of the pulse. This leads to gain-induced distortion in SOAs.

It is useful to separate the amplitude and phase of the pulse to study the pulse propagation as shown in Equation (A.4).

$$A = \sqrt{P}\exp(i\phi) \tag{A.1}$$

where A is the slowly-varying envelope associated with the optical pulse as described in the previous section, and $|A|^2$ represents intensity. P and ϕ are the instantaneous power and the phase of the propagating signal, respectively. Based on the photon rate equation, gain coefficient and the wave equation for the propagation of the electromagnetic field in the active region, the following Equations (A.2), (A.3) and (A.4)(A.4) can be derived from pulse propagating along the length of z.

$$\frac{\partial P}{\partial z} = (g - \alpha_{int})P \tag{A.2}$$

$$\frac{\partial \phi}{\partial z} = -\frac{1}{2}\alpha g \tag{A.3}$$

$$\frac{\partial g}{\partial \tau} = -\frac{g - g_0}{\tau_c} - \frac{gP}{\tau_c P_s} \tag{A.4}$$

where α_{int} is the internal loss, α is the linewidth enhancement factor [178][179], g_0 is the unsaturated small signal gain, P_s is the saturation power and τ is the reduced time measured in a reference frame moving with the pulse. Equation (A.5)

$$\tau = t - z/v_g \tag{A.5}$$

where v_g is the group velocity. Equation (A.6) defines P_s. The saturation power above with the SOA is heavily saturated.

$$P_s = \frac{h\nu\sigma_m}{\Gamma\alpha\tau_c} \tag{A.6}$$

where σ_m is the cross section area of the active region. The small signal gain [52] is defined by Equation(A.7).

$$g_0 = \Gamma\alpha N_0 \left(\frac{I}{I_0} - 1\right) \tag{A.7}$$

I_0 is the current required for transparency, as defined by Equation (A.8).

$$I_0 = \frac{qVN_0}{\tau_c} \tag{A.8}$$

As shown in Equation (2.13), the increase of optical input power reduces the carrier density. The weakened carrier density leads to lower optical gain as shown by Equation (2.11).

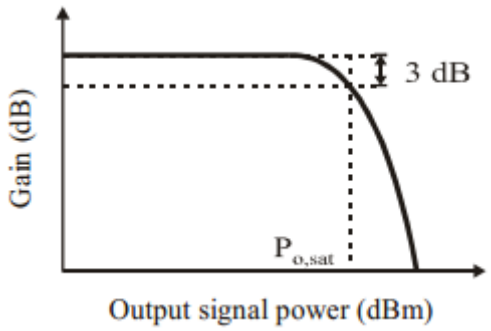

Figure A.1 Typical SOA gain vs output power [46]

Figure A.1 shows a typical SOA gain versus the output optical power. In the low power region, the gain almost keeps constant as the optical power is increased. The optical gain slowly drops with the increasing optical power. When the signal power is larger than the saturation power, the SOA is heavily saturated and gain reduction becomes significant.

In communication systems, square-wave input signals with a pulse width around a hundred picoseconds (corresponding to 10Gbit/s non-return-to-zero {NRZ} signal) are required to be amplified to extend the covering distance. If the amplification is linear, the shape of amplified pulses will be a replica of the input pulses. In practice, the patterning effect caused by nonlinearities are observed. [180][181][182][183]. The leading pulse saturates the SOA and reduces the gain for the trailing edge. The typical distorted output waveforms are shown in Figure A.2

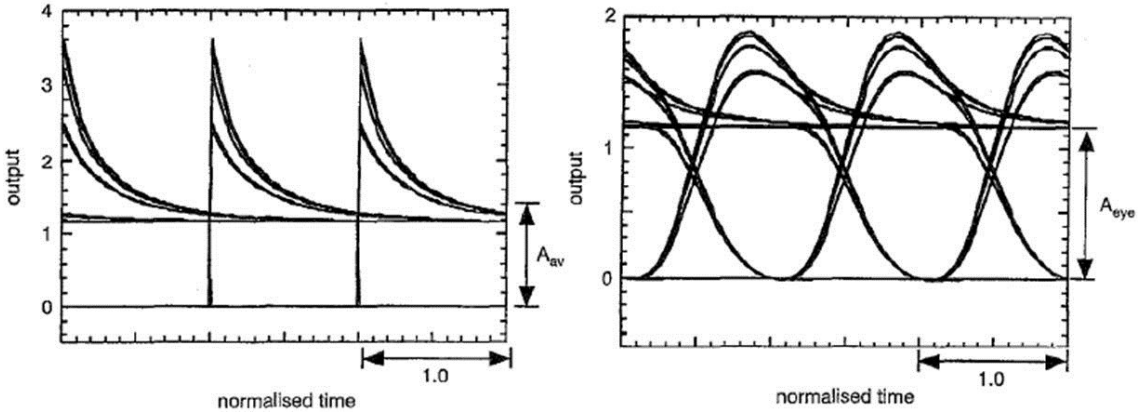

Figure A.2 SOA gain saturation (a) Waveforms at SOA output (b) Waveforms after a fifth-order Bessel filter [184]

Waveforms with different bit patterns suffer a different level of distortion.

- ✧ A stream with a long run of OFF bits before ON bits: The carrier density completely recovers during the long series of OFF bits. Therefore, the leading edge of ON bits has a huge gain. After that, the accumulated carriers in the SOA are depleted, and the gain returns to a saturated value.
- ✧ A stream with a short period of OFF bits before the ON bits: The carrier density cannot be built up during the short period of OFF bits. The leading edge of the ON bits is only slightly saturated.

The patterning effect can be reduced by using special coding schemes. Figure 0.3 shows the optical signal waveforms at the SOA output and the filtered output for the Manchester format [185]. The boosted gain at the leading edge of the pulse is smaller than that with NRZ modulation. This is because the OFF bits do not continue in the Manchester format and the carrier density is not able to be built up substantially.

It can also be noticed that the eye opening in the second half of one-bit period is larger than that in the first half. The reason is the carrier density has more time (at least half bit period) to recover.

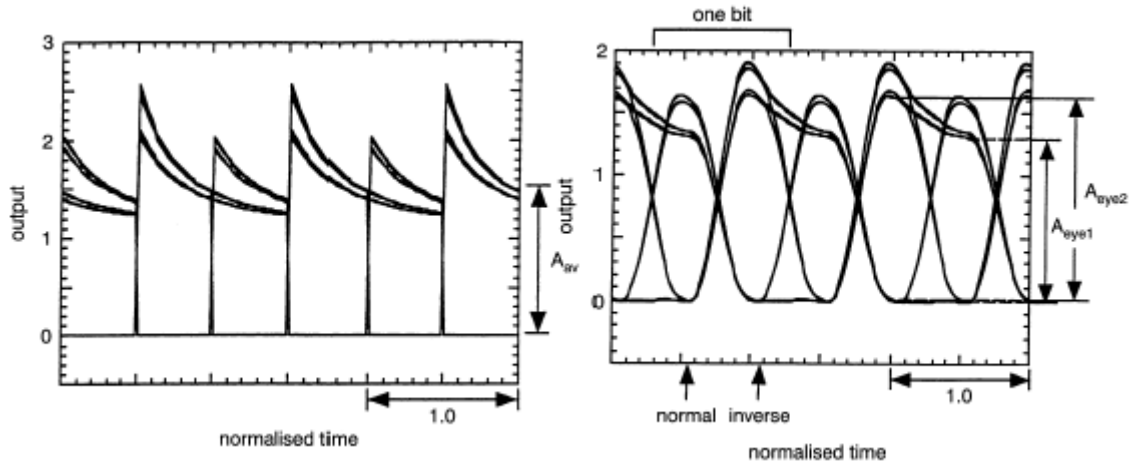

Figure 0.3 Signal waveforms for Manchester format a) at SOA output b) after a fifth-order Bessel filter [184]

A.2 Amplifier Noise Analysis

Optical gain is achieved by stimulated emission in the SOA. The spontaneous emission in the SOA is, however, inevitable and leads to the amplified spontaneous emission (ASE) noise. The spontaneous emission power produced by an SOA is given by Equation (A.9).

$$P_{sp} = N_{sp}hv(G-1)B_o \tag{A.9}$$

where P_{sp} is the spontaneous emission power, n_{sp} is the spontaneous emission factor, which is 1 for an ideal amplifier and ranges from 1.4 to 4 depending on the injection current and operating wavelength [186]. G is the optical gain, and B_o is optical bandwidth. It can be noticed that, with a constant optical bandwidth, reducing the optical gain is the only method to minimise the ASE noise.

The optical power is detected by a photodetector at the receiver end of the system. The detected current, I, is given by the square of the electric field of the optical signal (square law detector), E, as shown in Equation (A.10).

$$I = R|E|^2 = R(E \cdot E^*) = R \cdot P \tag{A.10}$$

where R is the photodetector responsivity and P is the received optical power. When the electric field consists of signal components at different frequencies, the components beat with each other. The Equation (A.11), (A.12) and (A.13) give an example that a photodetector receives two signals with optical carrier frequencies at ω_1 and ω_2.

$$E_1 = |E_1|e^{-j\omega_1 t} \tag{A.11}$$

$$E_2 = |E_2|e^{-j\omega_2 t} \tag{A.12}$$

$$I = R|E_1 + E_2|^2 = R(|E_1|^2 + 2|E_1||E_2|\cos([\omega_1 - \omega_2]t) + |E_2|^2) \tag{A.13}$$

The second term in the Equation (A.13) represents the beating between two signals.

In the following noise analysis, the optical powers are written in their current equivalent. Unity responsivity is also assumed. The photocurrent equivalent of the spontaneous emission power is given by Equation (A.14).

$$i_{sp} = \frac{P_{sp}e}{hv} = N_{sp}q(G-1)B_o \tag{A.14}$$

The detected signal power is given by Equation (A.15).

$$S = (GI_s\eta_{in}\eta_{out}L)^2 \tag{A.15}$$

where I_s is the photocurrent equivalent of the input power of the SOA, η_{in} is the amplifier input coupling efficiency, η_{out} is the amplifier output coupling efficiency, and L is the optical loss between the amplifier and the detector. The total noise, N_{tot}, is given by Equation (A.16)(A.16).

$$N_{tot} = N_{shot} + N_{s-sp} + N_{sp-sp} + N_{th} \tag{A.16}$$

N_{shot} is the shot noise, $N_{s\text{-}sp}$ is the signal-spontaneous beat noise, $N_{sp\text{-}sp}$ is the spontaneous-spontaneous beat noise, and N_{th} is the thermal noise. Only the noise which falls within the electrical bandwidth of the receiver, B_e, contributes to the noise in the detected current. Equation (A.17), (A.18), (A.19) and (A.20) calculate the noise for these terms.

$$N_{shot} = 2B_e q\eta_{out} L(GI_s\eta_{in} + I_{sp}) \tag{A.17}$$

$$N_{s-sp} = 4GI_s\eta_{in}{\eta_{out}}^2 I_{sp} L^2 \frac{B_e}{B_o} \tag{A.18}$$

$$N_{sp-sp} = \left(I_{sp}\eta_{out}L\right)^2 \frac{B_e}{{B_o}^2}(2B_o - B_e) \tag{A.19}$$

$$N_{th} = {I_{th}}^2 \tag{A.20}$$

I_{th} is the equivalent photocurrent of thermal noise power.

Two performance measures, the Q factor and the Bit Error Rate (BER) are commonly used for the detected signals. Q factor is given by Equation (A.21).

$$Q = \frac{\sqrt{S(1)} - \sqrt{S(0)}}{\sqrt{N_{tot}(1)} + \sqrt{N_{tot}(0)}} \tag{A.21}$$

S(1) and S(0) and $N_{tot}(1)$, $N_{tot}(0)$ are the signal and total noise for bit 1 and bit 0, respectively. BER is given by Equation (A.22). It is assumed that the Gaussian noise is dominant. A BER of 10^{-9} requires a Q of 6 [54].

$$BER = \frac{1}{\sqrt{2\pi}} \frac{\exp\left(-\frac{Q^2}{2}\right)}{Q} \tag{A.22}$$