Low-Power 56 Gb/s NRZ Microring Modulator Driver in 28 nm FDSOI CMOS

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***Abstract*—High speed optical interconnects require low-power compact electro-optical transmit modules comprising driver circuits and optical modulators. This paper presents a low power 56 Gb/s non-return-to-zero CMOS inverter based driver in 28 nm fully depleted silicon-on-insulator CMOS driving a 46 GHz silicon photonic microring modulator. The driver delivers 1 Vpp to the microring modulator from a 75 mVpp input while only consuming 40 mW (710 fJ/bit at 56 Gb/s). The realized transmitter shows 4 dB extinction ratio when running of a 1 V supply voltage. Transmission experiments up to 2 km of single mode fiber show a bit-error-ratio less than $1 \cdot 10^{-9}$ at 56 Gb/s.**

***Index Terms*—28 nm, broadband amplifier, CMOS inverter, driver, FDSOI CMOS, silicon photonic microring modulator, transmitter**

I. Introduction

DATA centers keep on requiring faster transceivers to sustain the continuous growth in intra data center communication. The need for faster optical interconnects is identified by the roadmaps of multiple standarization bodies such as the Ethernet Alliance, the Optical Internetworking Forum (OIF) and Infiniband. The low power consumption, low capacitance and small footprint of microring modulators make these devices ideal for densely integrated, low power transmitters in data centers [1]. CMOS-based drivers are well suited for this application and with the recent CMOS technologies it becomes feasible to design and deploy low power CMOS-based transceivers (1-2 pJ/bit power efficiency) with data rates above 40 Gb/s [2]–[5]. To enable these data rates in CMOS, non-return-to-zero (NRZ) inverter based driver topologies are often chosen [2], [3], [6], [7]. Although they can operate very fast, CMOS inverters are limited in drive voltage being typically the supply voltage (Vdd) due to transistor breakdown. For the most recent CMOS nodes, this is close to 1 V. Most modulators require more voltage swing to have an extinction ratio (ER) close to their maximum. Increasing the drive voltage beyond the breakdown voltage of the transistors is typically accomplished by adopting different (inverter-based) topologies: cascoded inverter, driving both anode and cathode or the pseudo-differential inverter. With the cascoded inverter [2], [6], the drive voltage is increased beyond the breakdown voltage by stacking multiple transistors on top of each other. The cascoded inverter requires an extra level shifted input, often generated by a high-speed level shifter or an RC bias-tee. The level shifter introduces extra complexity, while the bias-tee limits the low frequency cut-off. In [3] and [7] both nodes of the ring modulator are driven to increase the maximum drive voltage from 1 Vpp to 1.5 Vpp. By using a pseudo-differential inverter output driver, an output voltage of twice the supply voltage is obtained [6], [8]. However, this requires a proper way to reverse bias the modulator, e.g. with an on chip bias-tee. Here, rather than trying to achieve the maximum possible extinction ratio, we deliberately limit the drive voltage such that the microring can be driven from a conventional CMOS inverter. This eliminates any risks of incidentally exceeding the breakdown voltage of the driver transistors while also reducing power consumption (which scales quadratically with drive voltage). Although sacrificing ER, sufficient optical budget is still available to support transmission over 2 km of fiber.

Another problem with the conventional CMOS inverter drivers is that they are, without modification, not capable of amplifying small incoming signals. The small-signal bandwidth (BW) of the CMOS inverter is typically much smaller than the large-signal BW. However, when the input signal is generated from other chips in the system, e.g. in chip-to-module standards, the input amplitude will most of the time be much lower than e.g. 1 Vpp, requiring additional amplification in the driver. Our proposed driver therefore also features a high gain inverter based broadband amplifier to amplify the low swing input signal to full swing Vdd.

First, we start by describing the co-integrated microring modulator. Next, we analyze the broadband inverter based amplifier and discuss the design choices and simulation results. The third section covers the electro-optical transmission experiments.

II. Silicon photonic microring modulator

In this work we used a C-band microring modulator fabricated in imec's Silicon Photonics (SiPh) platform [1]. Static measurement, of this microring modulator are shown in Fig. 1.

This microring has a Q-factor of ∼2500 with a modulation efficiency of 40 pm/V. The low Q-factor ensures the required high-speed operation of the microring, albeit with a lower ER than a high Q ring. According to the S_{21} measurement, the ring

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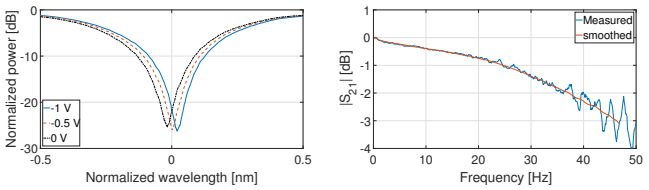


(a) (b)

Fig. 1. Measured microring characteristics: (a) static transmission spectra and (b) S_{21}

has 46 GHz small-signal 3 dB BW. The microring has a junction capacitance around 22 fF. In [1], the large-signal dynamic behavior has been verified with a signal swing of 1.5 Vpp and a bias voltage of -0.25 V. An ER of 6.6 dB was reported at 50 Gb/s by using a 50 Ω terminated 67 GHz RF probe and signal generator. In this work, 1 Vpp was the evident drive voltage, since this is the nominal supply voltage in the chosen 28 nm fully depleted silicon on insulator (FDSOI) CMOS technology. For this 1 Vpp drive voltage the ring modulator has an ER of 4.7 dB (measured with RF probe and signal generator in [1]). To evaluate the optical budget under these conditions, we calculated the insertion loss (IL) from Fig. 1. With a calculated IL of -11 dB, an assumed 10 dBm laser power and 5 dB loss due to edge couplers and waveguides, we calculate an optical modulation amplitude (OMA) of -6 dBm. This OMA is 4 dB above the -10 dBm required by state-of-the-art receivers to achieve a BER $\leq 1{\cdot}10^{-12}$ with an assumed photodiode responsivity of 0.8 A/W [9]. Moreover, this margin increases from 4 dB to 7 dB when using KP-FEC ($2{\cdot}10^{-4}$). In a future microring design, improved p-n junction design can reduce ring modulator IL by 4-5 dB at the expense of slightly reduced BW (still $>$ 35 GHz), giving e.g. an OMA of -2 dBm.

III. CMOS DRIVER ARCHITECTURE

High-speed optical modulators are often driven using current-mode logic (CML) amplifiers loaded with termination resistors. In such driver topologies, a large amount of static power is dissipated in the termination resistors and the differential amplifiers are always on irrespective of whether a 1 or a 0 is transmitted. As microrings are very small (compared to the electrical wavelength of the highest signal frequency) and have a very small lumped capacitance, they can be driven directly from CMOS inverters. CMOS inverters dissipate significantly less power than conventional drivers, because the power dissipated is largely dynamic and increases linearly with increasing bit rate. In addition, when using the same supply voltage, the output swing (which is equal to the supply voltage) of a CMOS inverter stage is larger than that of a CML stage with the same supply voltage. Given that the ER specification is fulfilled, we can focus on optimizing the driver for power and speed rather than drive voltage.

Transferring the signal onto the modulator is one challenge, however, receiving a clean signal from one electrical chip (e.g. an FPGA transceiver) at the input of the transmitter, is also becoming more difficult at high bit rates. Due to printed circuit board (PCB) transmission line losses, the effective signal applied to the transmitter module can be much lower than e.g. 1 Vpp and an additional amplification step in the driver is required. However, in CMOS processes, amplifying at high bit rates ($>$ 40 Gb/s) becomes challenging, even in the most recent CMOS nodes. The conventional unmodified CMOS inverter has a low ($<$10 GHz) small-signal BW, that is not high enough to amplify the incoming 50 Gb/s signal. A common solution to this is to use a CMOS inverter with shunt-shunt feedback, also known as the CMOS inverter transimpedance amplifier (TIA). To achieve high gain, a TIA inverter should be driven from a high impedance at its input and loaded with a high impedance at its output [10]. Due to the feedback, however, a TIA inverter has a low input impedance and low output impedance, therefore reducing the achievable gain when cascading several TIA inverters as in [2]. Therefore we propose the alternative topology shown in Fig. 2. The first 2 stages are inverter TIAs, dimensioned such that the input impedance is equal to 50 Ω [10]. To increase the input matching bandwidth, a commonly known broadband matching technique is used by adding a series inductor of 200 pH in front of the input TIA. Active input matching gives a high matching bandwidth while still providing gain. Unlike in [2], stage 3 is now a classic inverter without any feedback. Conventional inverters have a high input impedance and (for the same transistor size) an output impedance that is several times higher than the inverter TIA with feedback resistor. This implies that the fourth stage is driven from a relatively high impedance and is loaded with the high input impedance of the output inverter. This helps to significantly increase the achievable gain. Moreover, note that stage 3 and stage 4 resemble a Cherry-Hooper amplifier [11], for which it is known that the impedance mismatch helps to simultaneously achieve high gain and high bandwidth. Fig. 3 demonstrates how the proposed topology benefits in gain from loading an inverter TIA with conventional CMOS inverters. The gain of a single inverter TIA loaded with inverters is 6 dB higher, making it possible to have less stages to achieve the same gain and hence reducing power consumption. As in [2] inductive peaking using shunt and series inductors is then used to increase the small-signal bandwidth to 30 GHz. The series inductance due to wire bonding or flip chip bonding also adds to the inductive peaking and should be taken into account. In the design process, we used 100 pH (for flip chip bonding). The amplifiers in the chain were also sized to have low group delay variation and jitter (Fig. 3).

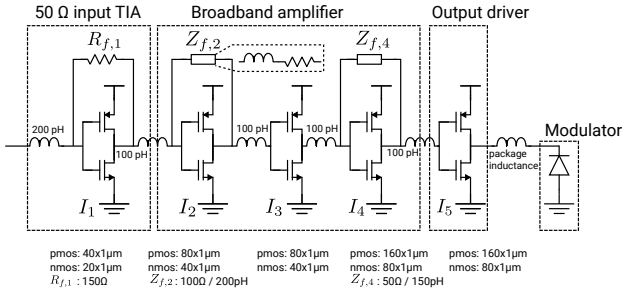
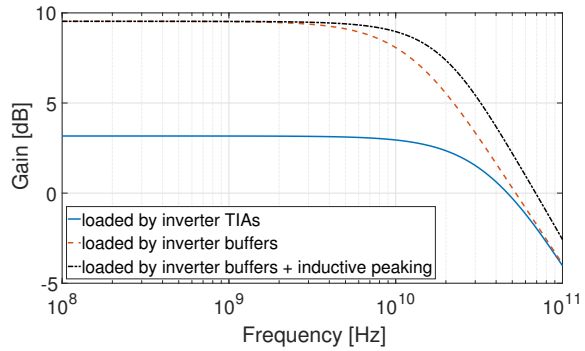
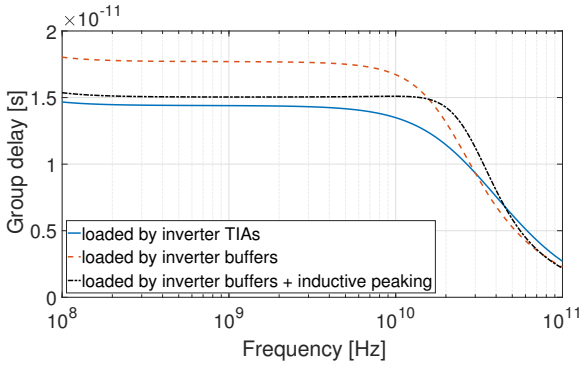


Fig. 2. The CMOS driver architecture

The broadband amplifier in combination with the input TIA has a post-layout simulated small-signal gain of 22 dB



(a)



(b)

Fig. 3. Simulated effect (a) amplitude and (b) group delay of a single inverter TIA stage in a full inverter TIA chain or with an inverter TIA chain where every inverter TIA is surrounded by inverter buffers

with 30 GHz bandwidth, which means that any signal larger than 100 mVpp at the input of the driver results in 1 Vpp voltage swing at the input of the output inverter I_5. The output inverter then works in its large-signal regime and its effective bandwidth increases significantly beyond the small-signal value. To confirm this experimentally, we measured the large-signal S-parameters, see Fig. 4. As expected, the large-signal bandwidth increases from 25 GHz at an input voltage of 110 mVpp to 44 GHz with an input voltage of 1 Vpp. The large-signal BW of the driver further increases beyond 100 mVpp input voltage thanks to the fact that the stages of the broadband amplifier and eventually the input TIA also start to operate in their large-signal regime. The large-signal gain decreases because any input swing larger than 100 mVpp gives rise to a limiting output voltage of 1 Vpp.

IV. Electro-optical experiments

We assembled the silicon photonic microring and CMOS driver on a test PCB (Fig. 5). The electrical and photonic dies are placed very close to each other to minimize the wirebond inductance.

The light is coupled into and out of the optical chip by two grating couplers. We used a tunable laser to find the optimal (maximum eye opening) wavelength (1549.310 nm) for the microring instead of a heater to ease testing. The laser power was set to 12 dBm and we estimate the optical power going in the microring to be around 6 dBm due to grating coupler losses. The modulated light leaves the optical

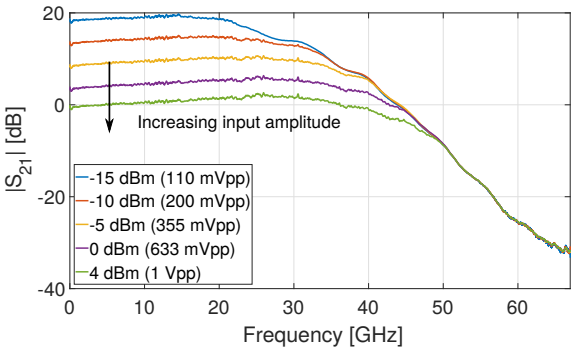


Fig. 4. Large-signal electrical S-parameter measurements of the driver

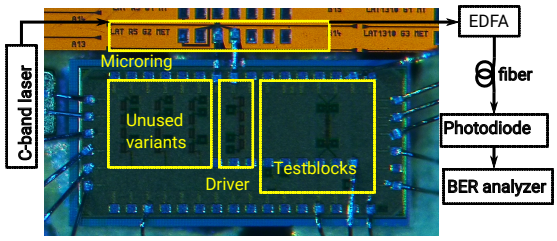
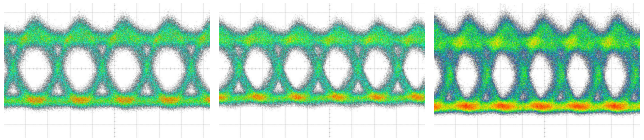


Fig. 5. Photograph of the electrical CMOS chip bonded to optical chip

chip through a second grating coupler and was amplified with an erbium-doped fiber amplifier (EDFA) to compensate for the losses in the two grating couplers and to overcome the reduced sensitivity due to the lack of a suitable high-speed transimpedance amplifier. There was no optical tunable filter to filter the amplified spontaneous emission noise from the EDFA available at the time of measuring. The resulting optical signal was coupled into a photodiode which has a responsivity of 0.6 A/W and a bandwidth of 50 GHz. The power into the photodiode was 8 dBm. The high speed electrical input of the driver chip was probed with a 50 GHz RF probe and all other DC connections are wire bonded to the PCB. The microring modulator is reverse biased with the average DC output voltage ($\mathrm{Vdd}/2 = 0.5\,\mathrm{V}$) of the CMOS inverter output stage.

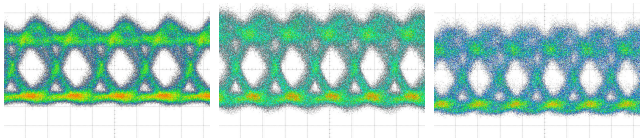
Fig. 6 and Fig. 7 show the measured optical eye-diagrams at respectively 50 Gb/s, 56 Gb/s and 60 Gb/s (PRBS $2^9 - 1$, a choice limited by the measurement equipment). The eyes are clearly open even after 2 km of single mode fiber. A small amount of overshoot is visible in the rising edge, which is due to the bondwire in the assembly. The reason why there is less or no peaking in the falling edge is that the overshoot is attenuated by the ring transmission curve. We achieved an extinction ratio of 4 dB, which is close to the value obtained in [1]. The measured IL at this ER is -11.5 dB.

Fig. 8 shows real-time (with a real-time bit-error ratio analyzer) measured bit-error ratio's (BER) for different fiber lengths and bit rates. The transmitter is back-to-back error free ($\mathrm{BER} \leq 1 \cdot 10^{-12}$) for 50 Gb/s for input voltages down to 75 mVpp. A higher input amplitude doesn't degrade the reported BER curves. For 56 Gb/s, the BER is $2 \cdot 10^{-11}$. After 2 km, the BER is roughly 10 times larger and 60 Gb/s transmission is still below KP-FEC ($2 \cdot 10^{-4}$). To have relevant measurements, we ensured that at least 10 errors were made before capturing



(a) (b) (c)

Fig. 6. Measured (a) 50 Gb/s, (b) 56 Gb/s and (c) 60 Gb/s back to back eye diagrams of the optical transmitter. (10 ps/division, (a) and (b) = 45 mV/division, (c) = 32 mV/division)



(a) (b) (c)

Fig. 7. Measured (a) 50 Gb/s, (b) 56 Gb/s and (c) 60 Gb/s eye diagrams of the optical transmitter after 2 km of fiber. (10 ps/division, (a) and (b) = 45 mV/division, (c) = 32 mV/division)

the BER. For the listed BER $= 1 \cdot 10^{-13}$, no errors were found for $1 \cdot 10^{14}$ bits. To show the speed limitation of the used BER analyzer, we have included its electrical back-to-back BER in Fig. 8 as a reference. In these link experiments, we used a 50 Ω matched photodiode instead of a TIA. With edge couplers and a TIA, no EDFA would have been needed in the electro optical experiments.

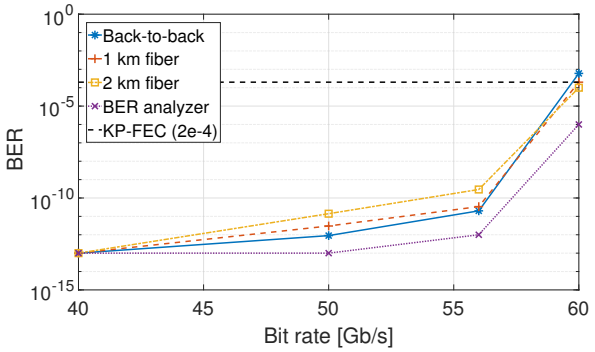


Fig. 8. BER vs bit rate for different fiber lengths

Table I presents a comparison of our work with other CMOS modulator drivers, which shows that the proposed driver has a good figure of merit (FOM), defined as power consumption / bit rate, while accepting an input signal amplitude down to 75 mVpp.

V. Conclusion

In this paper, we proposed and analysed a high gain, low power transmitter with a silicon photonics microring modulator and a CMOS driver. The driver uses a combination of inverter TIAs and normal CMOS inverters to provide 22 dB gain with a large BW. The driver is capable of driving the ring modulator at 56 Gb/s starting from an input signal as low as 75 mVpp with a power consumption of 40 mW (710 fJ/bit at 56 Gb/s). We showed link experiments with the fabricated assembly up to 60 Gb/s. The optical extinction ratio of the measured transmitter assembly is 4 dB.

TABLE I
Comparison of reported CMOS modulator drivers (bit rate $>$ 40 Gb/s)

Ref.	Process	Bit Rate (Gb/s)	Input Swing* (mV)	Output Swing (V)	Power (mW)	FOM** (pJ/bit)
[2]	28 nm SOI	40	< 10	5.2	292	7.3
[2]	28 nm SOI	60	-	4.3	318	5.3
[3]	28 nm	50	900	1-1.5	31	0.61
[4]	45 nm SOI	40	890	2	178	4.45
This work	28 nm SOI	56	75	1	40	0.71

*: minimum input swing to have full output swing at reported bit rate
**: FOM = power consumption / bit rate

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