Power analysis and Conditional Expectation of CMOS Sensors

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Abstract

Our research currently focusing on image sensors predominantly the sensors implemented using CMOS (Complementary Metal Oxide Semiconductor) technology. These sensors designated as CMOS sensors which were introduced after CCD (Charge-coupled Devices) sensors since CCDs having some drawbacks in terms of its power and making cost compared to CMOS sensors. The most prominent feature of the CMOS sensors is that they can work at low voltage. CMOS sensors need only one supply voltage but CCDs require three to four which makes the cost of the CMOS sensor very low compared to CCD. In this context we concentrated on power consumption of CMOS sensors and corresponding regression analysis applied to obtain the linearity between the input voltage and the power consumed by the sensor in different technical environments. Further research includes the testing of these sensors in terms of their response with respect to the input voltage levels, temperature effects, noise and the conditional expectation among them. Along with that we are computing the parameters in order to characterize the sensor in according with the physical and the logical effects.

Introduction

A wide dynamic range CMOS image sensor that can capture a scene containing both bright and dark areas is highly desirable for applications including automobile driver aids, security cameras and consumer products. Numerous approaches have been proposed to expand the dynamic range of CMOS image sensors. Most of these can be divided into one of three principal groups. The first group convert photocurrents into a time-to-saturation signal by integrating a comparator in each pixel [1]. However, this approach increases the pixel area with the result that these pixels are at a disadvantage when costs must be controlled or reduced whilst increasing pixel count. The second more evolutionary group samples the photocurrent several times within one or more integration periods and then synthesizes the wide dynamic range image . The main disadvantage of these systems is the cost of the processing needed to synthesize the final image. The last group realizes a logarithmic compression of the input photocurrent to the output voltage using the current-voltage characteristics of MOSFETs working in weak inversion . The small maximum output swing (typically 0.3V) and responsivity (50mV/decade) of these pixels make them vulnerable to both fixed pattern and temporal noise.

Furthermore, although the continuous output available from these pixels can be an advantage in some applications, it means that these pixels are slow to respond to a sudden decrease in photocurrent. The ideal pixel should combine the speed of response of an integrating pixel with the dynamic range compression of logarithmic pixels. This can be achieved using a comparator within each pixel to vary the effective integration time of the pixels so that the output voltage is proportional to the logarithm of the photocurrent . However, the large pixel size and low fill factor resulting from the use of an in-pixel comparator makes it impractical for most applications. To overcome these problems a novel wide dynamic range CMOS Image sensor technique has been developed.

Dynamic range

Dynamic range quantities the ability of a sensor to adequately image both high lights and dark shadows in a scene. It is defined as the ratio of the largest non- saturating input signal to the smallest detectable input signal.

Largest non- saturating signal given by

$$i_{\max} = \frac{qQ_{\text{sat}}}{t_{\text{int}}} - i_{dc},$$

Smallest detectable input signal defined as standard deviation of input referred noise under dark conditions

$$i_{\min} = \frac{q}{t_{\text{int}}}\sqrt{\frac{1}{q} i_{dc} t_{\text{int}} + \sigma_r^2}$$

Thus dynamic range is

$$\text{DR} = 20\log_{10}\frac{i_{\max}}{i_{\min}} = 20\log_{10}\frac{\frac{qQ_{\text{sat}}}{t_{\text{int}}} - i_{dc}}{\frac{q}{t_{\text{int}}}\sqrt{\frac{1}{q} i_{dc} t_{\text{int}} + \sigma_r^2}}$$

Extended Dynamic range

To increase dynamic range we need to increase i_{max} and/or decrease $i_{min.}$ I_{max} Increases as integration time is decreased and I_{min} decreases as integration time is increased.

To increase dynamic range need to spatially `adapt' pixel integration times to illumination such as short integration times for pixels with high illumination and long integration times for pixels with low illumination. Integration time can't be made too long due to saturation and motion.

Regression Analysis on Power per Pixel

Regression Statistics	
Multiple R	0.282990996
R Square	0.080083904
Adjusted R Square	-0.073235445
Standard Error	3600.596912
Observations	8

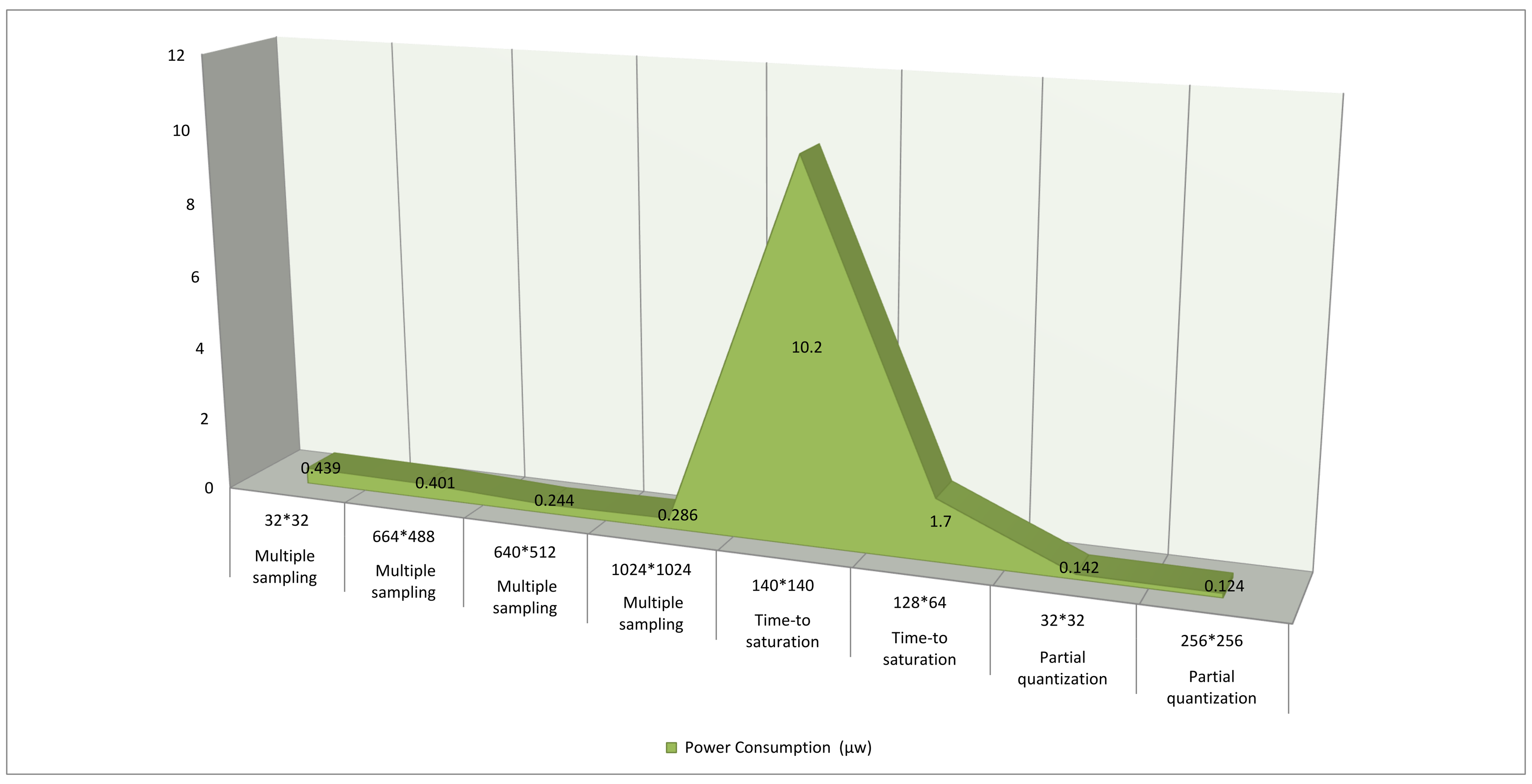
ANOVA

	df	SS	MS	F	Significance F
Regression	1	6771693.278	6771693	0.522334	0.497040058
Residual	6	77785788.72	12964298		
Total	7	84557482			

	Coefficients	Standard Error	t Stat	P-value	Lower 95%	Upper 95%	Lower 95.0%	Upper 95.0%
Intercept	2670.448916	1858.33043	1.437015	0.200744	-1876.721829	7217.61966	-1876.721829	7217.61966
Image Size	-2.684359165	3.71421029	-0.72273	0.49704	-11.77270432	6.403985995	-11.77270432	6.403985995

RESIDUAL OUTPUT

Observation	Predicted Calculated Power (nw)	Residuals
1	2584.549422	-2145.549422
2	888.0344301	-487.0344301
3	952.4590501	-708.4590501
4	-78.33486919	364.3348692
5	2294.638632	7905.361368
6	2326.850942	-626.8509425
7	2584.549422	-2442.549422
8	1983.252969	-1859.252969



Conclusion

The power consumption of two major wide dynamic range CMOS imaging sensors is studied in this paper with respect to image size in pixels. The power consumption is analytically derived and verified using HSPICE simulations. The power analysis shows that WDR CISs consume much higher power than conventional 3T-APS CISs. For CISs with large imaging array, the CIS power consumption is dominated by the driving of column buses.

References

[1].S. Kavusi, A. El Gamal, Quantitative study of high dynamic range image sensor architectures, Proc. SPIE 5301 (2004) 264–275.