Experimental Studies on Germanium-Tin P-Channel Tunneling Field Effect Transistors

Von der Fakultät Informatik, Elektrotechnik und Informationstechnik der Universität Stuttgart zur Erlangung der Würde eines Doktors der Ingenieurwissenschaften (Dr.-Ing.) genehmigte Abhandlung

Vorgelegt von
Erlend Granbo Rolseth
aus Trondheim, Norwegen

Hauptberichter:	Prof. Dr. habil. Jörg Schulze
Mitberichter:	Prof. Dr. rer. nat. Joachim Knoch
Tag der mündlichen Prüfung:	22.08.2017

Institut für Halbleitertechnik der Universität Stuttgart
2017

Contents

Zusammenfassung **10**

Summary **13**

Chapter 1 Introduction **15**

1.1 Searching for a New Energy Efficient Switch 15

1.2 A Brief History of Germanium in Complementary Metal-Oxide-Semiconductor Technology 16

1.3 History of the Tunneling Field Effect Transistor 18

1.4 Theoretical Background 20

1.4.1 Power Consumption of a Logic Element 21

1.4.2 Tunneling Field Effect Transistor: Operating Principles 23

1.4.3 Zener Tunneling Current 24

1.4.4 Subthreshold Swing of Tunneling Field Effect Transistors 26

1.4.5 Leakage Current Mechanisms in Tunneling Field Effect Transistors 28

1.5 Tunneling Field Effect Transistors: State-of-the-Art 32

1.5.1 Material System Considerations for Tunneling Field Effect Transistor Design 32

1.5.2 Geometry Considerations for Tunneling Field Effect Transistor Design 35

1.6 Thesis Overview 36

Chapter 2 Vertical Tunneling Field Effect Transistor Device Fabrication and Data Acquisition 40

2.1 Molecular Beam Epitaxy 40

2.1.1 Molecular Beam Epitaxy Growth Process 41

2.1.2 Doping in Molecular Beam Epitaxy Systems 42

2.1.3 Molecular Beam Epitaxy Growth of Germanium on Silicon 43

2.1.4 Molecular Beam Epitaxy Growth of Germanium-Tin 45

2.1.5 Molecular Beam Epitaxy Growth of Germanium/Germanium-Tin P-Channel Tunneling Field Effect Transistors 46

2.2 Vertical Gate-All-Around Device Fabrication of Germanium Based Tunneling Field Effect Transistors 48

2.2.1 Mesa Structuring in Gate-All-Around Fabrication Process of Germanium Based Tunneling Field Effect Transistors 49

2.2.2 Gate Formation in Gate-All-Around Fabrication Process of Germanium Based Tunneling Field Effect Transistors 50

2.2.3 Isolation and Contacting in Gate-All-Around Fabrication Process of Germanium Based Tunneling Field Effect Transistors 52

2.3 Data Acquisition and Processing 53

Chapter 3 Germanium-Tin P-Channel Tunneling Field Effect Transistors: the Effect of Tin-Content in Germanium-Tin Channel 56

3.1 Introduction 56

3.2 Layer Growth and Device Fabrication 57

3.3 Results and Discussion 59

3.3.1 Influence of Tin-Content in Channel on Leakage Current in Germanium-Tin Tunneling Field Effect Transistors 60

3.3.2 Influence of Tin-Content in Channel on Subthreshold Swing of Germanium-Tin Tunneling Field Effect Transistors 66

3.3.3 Influence of Tin-Content in Channel on Drive Current of Germanium-Tin Tunneling Field Effect Transistors 68

3.4 Conclusion 71

Chapter 4 Germanium-Tin P-Channel Tunneling Field Effect Transistors: Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface .. 72

4.1 Introduction 72

4.2 Layer Growth and Device Fabrication 73

4.3 Results and Discussion 74

4.3.1 Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface on Leakage Current 75

4.3.2 Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface on Drive Current 78

4.4 Conclusion 80

Chapter 5 Source Doping Concentration Variation in Germanium P-Channel Tunneling Field Effect Transistors 82

5.1 Introduction 82

5.2 Layer Growth and Device Fabrication 83

5.3 Results and Discussion 84

5.3.1 Influence of Source Doping Concentration on Leakage Current in Germanium Tunneling Field Effect Transistors 84

5.3.2 Temperature Dependence of Germanium P-Channel Tunneling Field Effect Transistors with Varying Source Doping Concentration 87

5.3.3 Influence of Source Doping Concentration on Subthreshold Swing in Germanium P-Channel Tunneling Field Effect Transistors 89

5.3.4 Influence of Source Doping Concentration on Drive Current in Germanium P-Channel Tunneling Field Effect Transistors 94

5.4 Conclusion 95

Chapter 6 Source Doping Profile Tuning in Germanium P-Channel Tunneling Field Effect Transistors through Molecular Beam Epitaxy Antimony Pre-Buildup 97

6.1 Introduction 97

6.2 Layer Growth and Device Fabrication 98

6.3 Results and Discussion 99

6.4 Conclusion 103

Chapter 7 Electrical Characterization of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors Passivated through Post Plasma Oxidation 104

7.1 Introduction 104

7.2 Layer Growth and Device Fabrication 105

7.3 Results and Discussion 105

7.3.1 Capacitance-Voltage Characteristics of Post Plasma Oxidized Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors 106

7.3.2 Current-Voltage Characteristics of Post Plasma Oxidized Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors 113

7.3.3 Temperature Dependency of the Current-Voltage Characteristics of Post Plasma Oxidized Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors 116

7.4 Conclusion 119

Chapter 8 Impact of Sulfur Passivation on the Electric Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors ... 121

8.1 Introduction 121

8.2 Layer Growth and Device Fabrication 121

8.3 Results and Discussion 122

8.3.1 Influence of Sulfur-Passivation on the Capacitance-Voltage Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors 122

8.3.2 Influence of Sulfur-Passivation on the Current-Voltage Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors 125

8.4 Conclusion 127

Concluding Remarks 129

Appendix: The Metal-Oxide-Semiconductor System 132

References 144

Acknowledgements 155

Curriculum Vitae 157

Acronyms and abbreviations

ALD	Atomic layer deposition
BHF	Buffered hydrofluoric acid
BTBT	Band-to-band tunneling
DIBT	Drain induced barrier thinning
EOT	Equivalent oxide thickness
FGA	Forming gas annealing
GIDL	Gate induced drain leakage
HF	High frequency
ICP-RIE	Induced coupled plasma-reactive ion etching
IHT	Institut für Halbleitertechnik
IL	Interfacial layer
ITRS	International technology roadmap for semiconductors
LF	Low Frequency
MBE	Molecular beam epitaxy
ML	Monolayer
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
NDR	Negative-differential-resistance
QCE	quantum confinement effect
RT	Room temperature
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
SRH	Shockley-Read-Hall
TAT	Trap-assisted tunneling
TMA	Tri-methyl-aluminum
VS	Virtual substrate
A	Device area
C_D	Depletion capacitance

C_M	MOS capacitance
C_P	Measured capacitance
C_S	Semiconductor capacitance
D	Mesa diameter
D_{it}	Interface state density
$d_{channel}$	Channel thickness
d_{ox}	Oxide thickness
E_G	Bandgap
I_{ON}	Drive current
I_{OFF}	Leakage current
J_A	Area leakage current density
J_P	Perimeter leakage current density
k_B	Boltzmann constant
N_A	Acceptor doping concentration
N_D	Donor doping concentration
N_S	Source doping concentration
n_i	Intrinsic carrier concentration
P	Device perimeter
p_i	Background doping concentration
q	Elementary charge
R_S	Series resistance
SS	Subthreshold swing
T	Measurement temperature
T_{sub}	Substrate temperature
V_{DS}	Drain-Source voltage
V_{FB}	Flatband voltage
V_G	Gate-source voltage
V_{stress}	Presoaking voltage
W_D	Depletion width
w_G	Gate width
x	Sn-content
ξ	Electric field
ε_o	Vacuum permittivity
ε_r	Relative permittivity

ε_S	Semiconductor permittivity
τ	Lifetime
λ	Tunneling barrier width

Al	Aluminum
Al_2O_3	Aluminum oxide
B	Boron
Ge	Germanium
GeO_x	Germanium oxide
GeSn	Germanium-tin
H_2O_2	Hydrogen peroxide
S	Sulfur
Si	Silicon
SiO_2	Silicon oxide
SiGe	Silicon-germanium
Sb	Antimony
Sn	Tin

Zusammenfassung

In den letzten Jahren zeigte sich ein wachsendes Interesse an Bauelementkonzepten wie Tunnel-Feldeffekttransistoren (TFETs), die auf dem quantenmechanischen Tunneln basieren. Der TFET konkurriert in Bezug auf Geschwindigkeit, Leistung und Fläche direkt mit dem Metall-Oxid-Halbleiter-Feldeffekttransistor (MOSFET). Der Injektionsmechanismus in TFET ist ein Band-zu-Band-Tunnel- (BTBT-) Strom, und der potentielle Vorteil des TFET liegt in seinen steilen Strom-Spannungs (IV) -Unterschwellwertcharakteristiken, die nicht wie im MOSFET durch die 60 mV / Dekade bei Raumtemperatur begrenzt sind. TFETs könnten bei niedrigen Versorgungsspannungen zwar potentiell besser arbeiten, aber die experimentellen Realisierungen dieses Bauelements bleiben noch hinter den Erwartungen zurück. Insbesondere ist eine Verbesserung des On-Stroms notwendig, um den MOSFET hinsichtlich seiner Leistungsfähigkeit zu übertreffen.

In dieser Arbeit wurden verschiedene Strategien zur Verbesserung der Leistungsfähigkeit von p-Kanal Germanium (Ge) TFETs experimentell untersucht. Modifikationen des Halbleitermaterials und Dotierungsprofile werden mit dem Ziel, die Tunnelwahrscheinlichkeit zu erhöhen und hohe On-Ströme zu erreichen, untersucht. Hierzu wurden vertikale TFETs konzipiert, hergestellt und charakterisiert. Die vertikalen Halbleiterstrukturen selbst wurden mittels Molekularstrahlepitaxie (MBE) hergestellt, und die vertikalen Bauelemente wurden unter Verwendung eines GAA- (Gate-all-around) -Geometrie-Herstellungsprozesses hergestellt.

Es wird gezeigt, dass der On-Strom (I_{ON}) effektiv durch die Einführung von Germanium-Zinn (GeSn) in den Kanal erhöht werden kann. Ein sukzessiver Anstieg von I_{ON} wird beobachtet, wenn der Zinn (Sn) -Gehalt x in einem Germanium-Zinn ($Ge_{1-x}Sn_x$) -Kanal von x = 0 % auf x = 2 % und x = 4 % erhöht wird. Dies liegt an der Verringerung der Bandlücke in $Ge_{1-x}Sn_x$ mit steigendem Sn-Gehalt, was die Tunnelwahrscheinlichkeit effektiv erhöht. Ferner wurde experimentell ermittel, dass, wenn die Schichtdicke von $Ge_{0,96}Sn_{0,04}$ auf 10 nm begrenzt ist, die genaue Positionierung dieser $Ge_{0,96}Sn_{0,04}$-Schicht relativ zum Source-Kanal-Übergang des TFETs deutliche Auswirkungen auf die Kennlinien des Bauelements hat: Ein hoher I_{ON} wird erreicht, wenn sich diese Schicht vollständig innerhalb des Kanals befindet, während der Leckstrom (IOFF) reduziert wird, wenn diese Schicht vom Kanal in die Source verschoben wird. Eine Schwierigkeit beim Einbau von $Ge_{1-x}Sn_x$ in die p-Kanal-Ge-TFETs ist, eine hohe epitaxiale Qualität beizubehalten, wenn der Sn-Gehalt erhöht wird. Zusammen mit der Verringerung der Bandlücke wird gezeigt, dass das Einbringen von Sn die I_{OFF}- und

Subschwellenschwingung (SS) der Bauelemente durch erhöhte Shockley-Read-Hall (SRH) -Erzeugung und Trap-Assisted-Tunneling (TAT) -Ströme verschlechtert. Dies stellt die Machbarkeit einer akzeptablen Leistung mit GeSn als Kanalmaterial in Frage. Basierend auf den Ergebnissen werden einige Verbesserungsstrategien diskutiert.

Es wurde herausgefunden, dass die Variation der Source-Dotierungskonzentration in p-Kanal-Ge-TFETs mit Gate-Source-Überlappung hauptsächlich die Unterschwellencharakteristika der Bauelemente beeinflusst. Eine höhere Steilheit wird mit zunehmender Dotierstoffkonzentration in der Source-Region erzielt. Es wird angenommen, dass diese Korrelation ein Ergebnis von TAT in der Source-Gate-Überlappungsregion ist. Im Gegensatz zu Ergebnissen aus veröffentlichten Simulationsstudien konnte für die untersuchten Dotierungsgrade keine Auswirkung der Dotierstoffkonzentration auf I_{ON} identifiziert werden.

Eine MBE-Vorbelegungsstrategie von Antimon (Sb) wird untersucht, um steile Source-Dotierungsprofile in vertikalen p-Kanal-Ge-TFETs zu erhalten. Es ist ersichtlich, dass für eine Sb-Vorbelegung von 1/20 Monolagen (ML) sowohl I_{ON} als auch SS verbessert sind. Dies wird dadurch erklärt, dass die Ausbreitung der Tunnelbarriere in die Source-Region reduziert wird, was zu einer Erhöhung der Tunnelwahrscheinlichkeit und Verbesserung der Bandpassfilterung führt. Die Verstärkung von I_{ON} ist gering, aber die Vorbelegung lässt sich ohne Mehraufwand in den TFET-Herstellungsprozess integrieren und kann leicht mit anderen Strategien zur Verstärkung der On-Ströme von TFETs kombiniert werden. Die Ergebnisse deuten auch darauf hin, dass eine optimale Vor-Aufbau-Dotierung existiert.

In dieser Arbeit werden auch das Aluminiumoxid (Al_2O_3), das als Gateoxid verwendet wird, und das Ge / Al_2O_3 / Al-System untersucht. Eine Germaniumoxid (GeOx) -Passivierung durch Post-Plasma-Oxidation und eine Schwefel (S) -Passivierung durch wässrige Ammoniumsulfit-Lösungsbehandlung werden durch die Herstellung und elektrische Charakterisierung von MOS-Kondensatoren untersucht. Für die mit GeO_x passivierte Probe wird eine Hysterese und eine Verschiebung der Flachbandspannung durch Akzeptor-Traps im Oxid erklärt. Eine allgemeine Parallelverschiebung der Kapazitäts-Spannungs- (C-V) -Kurve zu positiven Gate-Spannungen ist Indikator für ortsfeste negative Ladungen und ein O-reiches Al_2O_3. Es wird vorgeschlagen, dass diese O-reichen Regionen durch die Nach-Plasma-Oxidationsbehandlung induziert werden könnten. Temperaturabhängige Strom-Spannungs (I-V) -Kennlinien zeigen einen Schottky-Emissionsprozess als Haupttransportmechanismus durch das Oxid bei niedrigen elektrischen Feldern an.

Es wird beobachtet, dass der Effekt der S-Passivierung der Ge-Oberfläche sowohl die C-V-Hysterese als auch den Leckstrom in der Region mit niedrigem E-Feld reduziert. Die gemessenen Oxidkapazitäten zeigen auch, dass dies nicht auf Kosten einer Oxidverdickung geht.

Summary

Recent years have shown a growing interest in device concepts based on quantum mechanical tunneling. The tunneling field effect transistor (TFET) is a device that competes directly with the metal-oxide-semiconductor field effect transistor (MOSFET) in terms of speed, power and area. The drive current injection mechanism in TFETs is a band-to-band tunneling (BTBT) current and the promise of the TFET lies in its steep subtreshold current-voltage (I-V) characteristics, which is not restricted by the MOSFET's 60 mV/dec limit at room temperature. TFETs could perform better at low supply voltages, but improvement of the drive current is necessary to outperform the MOSFET.

In this work different device tuning strategies for the p-channel germanium (Ge) TFET are studied. Modifications involving the semiconductor material and doping profiles are investigated with the aim of increasing the tunneling probability and achieving high drive currents. This investigation has been conducted through designing, fabricating and characterizing the vertical TFET structures. Vertical semiconductor structures were grown by means of molecular beam epitaxy (MBE), and the vertical devices were fabricated using a gate-all-around (GAA) geometry fabrication process.

It is shown that the drive current (I_{ON}) can be effectively increased by the introduction of germanium-tin (GeSn) in the channel. A successive increase in I_{ON} is seen when increasing the tin (Sn)-content, x, in a germanium-tin ($Ge_{1-x}Sn_x$) channel from x = 0 % to x = 2 % and x = 4 %. This is due to the lowering of the bandgap, which effectively increases the tunneling probability. Furthermore, it is found that when $Ge_{0.96}Sn_{0.04}$ is confined within a 10 nm delta-layer, TFET device performance can be tuned by shifting the position of this layer at the source-channel interface. A high I_{ON} is achieved when this layer is completely inside the channel, while the leakage current (I_{OFF}) is reduced when this layer is shifted from the channel and into the source. A complicating factor with incorporating $Ge_{1-x}Sn_x$ in the p-channel Ge TFETs is found to be the difficulty of maintaining a high epitaxial quality when increasing the Sn-content. Together with the lowering of the bandgap, this is shown to degrade the I_{OFF} and subthreshold swing (SS) of the device through increased Shockley-Read-Hall (SRH) generation and trap-assisted tunneling (TAT) currents. This further calls into question the feasibility of achieving acceptable performance with GeSn as channel material. Based on the results, some device performance strategies are discussed.

Varying the source doping concentration in p-channel Ge TFETs with gate-source overlap is found to mainly influence the subthreshold characteristics of the devices. Steeper

subthreshold characteristics is found with increasing source doping concentration. This correlation is believed to be a result of TAT in the source-gate overlap region. Contrary to results from published simulation studies, no effect of varying the source doping concentration on I_{ON} could be distinguished for the doping levels investigated.

A MBE pre-buildup technique of antimony (Sb) is investigated as a means to achieve steep source doping profiles in vertical p-channel Ge TFETs. It is seen that for a Sb pre-buildup concentration of 1/20 monolayer (ML), both I_{ON} and SS is improved. This is explained by that the extent of the tunneling barrier into the source region is reduced, leading to an increase of the tunneling probability and improvement of the band pass filtering. The boost in I_{ON} is small, but the pre-buildup technique imposes no extra load onto the TFET fabrication process and can easily be combined with other strategies for boosting the drive current for TFETs. The results also suggests that an optimal pre-buildup doping exists.

In this work also the aluminum oxide (Al_2O_3), which is used as gate oxide, and the $Ge/Al_2O_3/Al$ system is studied. A germanium oxide (GeO_x)-passivation achieved through post-plasma oxidation and a sulfur (S)-passivation achieved through an aqueous Ammonium sulfite solution treatment, are both investigated through the fabrication and electrical characterization of MOS-capacitors. For the sample passivated with GeO_x, a hysteresis and a shift in the flatband voltage is explained by acceptor traps in the oxide. A general parallel shift of the capacitance-voltage (C-V)-curve towards positive gate voltages indicates fixed negative charges and an O-rich Al_2O_3. It is suggested that these O-rich regions could be induced by the post plasma oxidation treatment. Temperature dependent current-voltage (I-V)-characteristics indicate a Schottky emission process as the main transport mechanism through the oxide at low electric fields.

The effect of S-passivation of the Ge surface is seen to reduce both the C-V hysteresis and the leakage current in the low E-field region. The measured oxide capacitances also reveal that this does not come at the expense of a thicker equivalent oxide thickness (EOT).

Chapter 1 Introduction

1.1 Searching for a New Energy Efficient Switch

At the time of writing there are over 3 billion smartphone users in the world. Projections are made that those numbers will exceed 6.4 billion by the year 2021[1]. It is no exaggeration to say that the market of electronic devices has, and is continuing to, exhibit a unique growth, not seen the likes of in many other industries. The growth is partly a result of the improvement achieved for each new electronic device generation. Due to the new features and capabilities of the newest device generation, electronic devices are often acquired at a more frequent rate than the actual service lifetime of the devices. To keep up with this rapid development, however, considerable requirements are forced onto the electronic switches i.e. transistors, responsible for doing the job. Scaling down the transistors dimensions, has been the successful strategy used for over five decades to accomplish this task. This strategy has allowed to increase the transistor count on the chip, and hence increasing a processors computational power. For a long time scaling did also result in more energy efficient as well as faster switches. This made miniaturization a very advantageous approach. As the nanometer technology needed to realize these switches has grown extremely complex and expensive, we are now also seeing other reasons for why the scaling is becoming less advantageous than before. The devices are being pushed hard against their theoretical limits. This has made increasing the transistor count, but at the same time reducing the power consumption of each single transistor, a very difficult task. For a consumer this leads to some worrisome outlooks if not taken care of. Imagine if your *portable* electronic device needs constant recharging. It takes away its intended practicality. If the device, due to excessive power dissipation, is too hot to handle, this also limits its usefulness. In trying to solve this problem, scientific virtue and engineering ingenuity is called for. A new energy efficient switch is needed.

In this thesis an electronic switch that is based on quantum mechanical tunneling is presented. This device, the tunneling field effect transistor (TFET), takes advantage of the peculiar phenomenon that electrons can pass through a barrier if it is made sufficiently thin. Switching between on and off with the aid of tunneling has been shown to consume much less energy than other devices. A TFET could hence potentially outperform the existing and transistor era's long lived work horse, the metal-oxide-semiconductor field effect transistor (MOSFET), in terms of both speed and power as well as area. The TFET has, however, its own challenges to overcome before it can be accepted by the industry. Although the current flow

can be controlled in a very energy efficient way, the existence of a barrier still significantly reduces the current carrying-capacity. As a result the drive currents of TFETs is inferior to today's transistors. Solving this problem sets the backdrop for this thesis.

1.2 A Brief History of Germanium in Complementary Metal-Oxide-Semiconductor Technology

Germanium (Ge) is considered an exciting candidate for high-performance scaled complementary metal-oxide-semiconductor (CMOS) technology. Compared to silicon (Si), Ge has a smaller bandgap and higher and better balanced bulk hole and electron mobilities (see Table 1). This gives Ge the potential of replacing Si as the material of choice, as the computer technology is pushed up against the physical limitations of miniaturization. Although attracting much interest in the last decades for its exciting attributes, the emergence of Ge in the semiconductor technology is more of a revival. Ge actually has a history in the semiconductor industry as long as the industry itself. It was the earliest semiconductor pursued by the Bell Laboratories at the beginning of the transistor era [2]. Numerous breakthroughs in the field of semiconductor engineering have Ge in the leading role: the first commercial transistor [3], the first integrated circuit [4] and the first demonstration of a tunneling diode [5] to mention a few. However, in the history of the MOSFET and what evolved into the successful CMOS technology, Si has played the instrumental role. In addition to its abundance, one of the most important reasons for pursuing Si was because of the superior interface it formed with silicon oxide (SiO_2) and the high quality thermal oxide [6]. Due to the thermal instability and chemical reactivity of germanium oxide (GeO_2) with water, the Ge/GeO_2 system on the other hand was considered unfit for field effect devices. Ge was hence sidelined in the beginning years of the CMOS technology. Looking back at the computer chip era and dominance of the CMOS technology in the electronics industry today, one can understand the Si choice.

Table 1 Properties of Si and Ge at 300 K. After [31].

Semiconductor	Lattice constant (Å)	Indirect bandgap (eV)	Direct bandgap (eV)	Mobility (cm^2/Vs)		Relative permittivity $\varepsilon/\varepsilon_0 = \varepsilon_r$	Intrinsic carrier concentration (cm^{-3})
				μ_n	μ_p		
Si	5.43	1.12	3.4	1450	500	11.9	$1 \cdot 10^{10}$
Ge	5.65	0.66	0.8	3900	1900	16.0	$2 \cdot 10^{13}$

Between the 60's and beginning of the 80's the main focus of the CMOS technology was scaling down the well-functioning Si/SiO_2 system, rigorously following the scaling trend predicted by Gordon E. Moore [7]. Little attention was therefore given to alternative materials investigations during this period. This was, however, about to change. Although the scaling and miniaturization strategy was immensely fruitful and effective, concern were being voiced [8] about the physical and geometrical limitations awaiting in the near future. Also the cost due to the demands and constraints on the production facilities that came with the continued scaling, was growing with a worrisome rate [9]. This eventually led to the appearance of Ge in the field in the mid 80's. The accomplishment of low-temperature (< 700 °C) epitaxial growth of Si, allowed the effective joining of Si and Ge into silicon-germanium (SiGe) alloys [10]. SiGe alloys found its uses as channel material [11], but first and foremost as relaxed SiGe buffers for strained Si MOSFETS [12, 13]. Through strain or through alloying with Ge, an effectiv increase in carrier mobility compared to unaltered Si is achieved. SiGe therefore represented an alternative approach to improving device performance other than device dimension shrinking. Noteworthy industry breakthroughs followed. IBM was first out, revealing their SiGe technology in 1989, and a decade later introducing it into the industry's first standard, high-volume SiGe chip [14]. Intel followed soon after by introducing SiGe in their 90 nm process generation [15]. At the time SiGe had been introduced and accepted by the somewhat conservative semiconductor industry, the research community was eager to investigate the next natural step. Due to the high mobility of charge carriers, all Ge devices could potentially provide improved performance even compared to advanced strained Si and SiGe layers [2]. All Ge FETs devices were fabricated, characterized and reported [16, 17, 18]. Now, an extra focus was put on the major problem facing Ge based field effect devices in the first place: the unfavorable surface properties.

Simultaneously as Ge was being introduced into the field, the CMOS scaling and device shrinking also started demanding very thin SiO_2 gate oxides thicknesses, t_{ox}. For very thin oxides, $t_{ox} < 4$ nm, however, quantum mechanical tunneling through the oxide becomes a serious issue. In the beginning of the 2000's the leakage current through the SiO_2 gate oxide started increasing 100 fold for each process generation [19]. The solution to this problem was found in high-κ dielectrics, which in this context are defined as insulators that have a higher relative permittivity than SiO_2. They could offer a larger physical thickness, but with the same equivalent capacitance as that of a much thinner SiO_2 layer. Although concern were voiced about introducing a new high-κ material into the gate stack and the CMOS technology, by 2007 both Intel [19] and IBM [20] had announced that they would replace SiO_2 with the high-κ

material hafnium oxide (HfO_2) for the 45 nm process generation. Now with the departure from SiO_2 as gate oxide of choice, the importance of the superior Si/SiO_2 semiconductor-oxide system became redundant. From this point of view, the argument of sticking with Si as a channel material lost its significance.

Which material system and device concept will eventually replace the Si MOSFET, is yet to be determined, as many exciting device concepts and new materials have entered the race [21]. The first experimental demonstration of an all Ge CMOS circuit with an Al_2O_3 gate oxide has recently been reported [22]. But also a recently presented TFET using Ge as a source material has gained attention due to its extremely steep turn-on characteristics [23]. Both of these two maybe marking, in separate ways, the beginning for a new or alternative era for the CMOS technology. However, one can expect Ge to be a major influential player, as creative scientist and engineers struggle to sustain Moore's Law in the years that lie ahead.

1.3 History of the Tunneling Field Effect Transistor

The history of the tunneling field effect transistor, can be traced all the way back to 1952 and a work conducted by O. M. Stuetzer [24]. In an experimental study, he demonstrated a surface conductivity control when an electrode (Gate) was placed in the neighborhood of a pn-junction. The device, which he named *junction fieldistor*, contained the basic elements of a TFET. This device also demonstrated both n-type and p-type transistor behavior, depending on the positioning of the gate electrode with respect to the pn-junction. This is a unique characteristic of the TFET. The reported surface conductivity control was, however, not attributed to quantum mechanical tunneling. This having the natural explanation that tunneling in semiconductors at the time was not yet an established concept. It is true that the idea of electrons traveling from one energy band to another, had been theorized by Clarence Zener already in 1934 [25]. However, the theory of Zener was derived to explain the electrical breakdown of dielectrics. It was later found that Zener's breakdown theory was applicable also for semiconductors. *Zener tunneling* and *Zener effect* were later introduced and are today commonly used terms to describe the tunneling in reverse biased pn-junctions.

A tunneling breakthrough came in 1958, when Leo Esaki reported on a new phenomenon in heavily doped Ge pn-junctions [5]. He discovered an anomalous current-voltage (I-V) characteristic in the forward direction. A negative differential resistance (NDR) region was observed, were the current decreased with increasing voltage bias. Esaki was able to explain the behavior by electron band-to-band tunneling (BTBT). Simplified band diagram schematics explaining the I-V characteristics of such a junction are shown in Figure 1. The discovery later

earned Esaki the 1973 Nobel Prize in physics [26]. Together with the theoretical work of Evan O. Kane [27, 28], Esaki's discovery laid the foundation for a better understanding of tunneling in semiconductor structures.

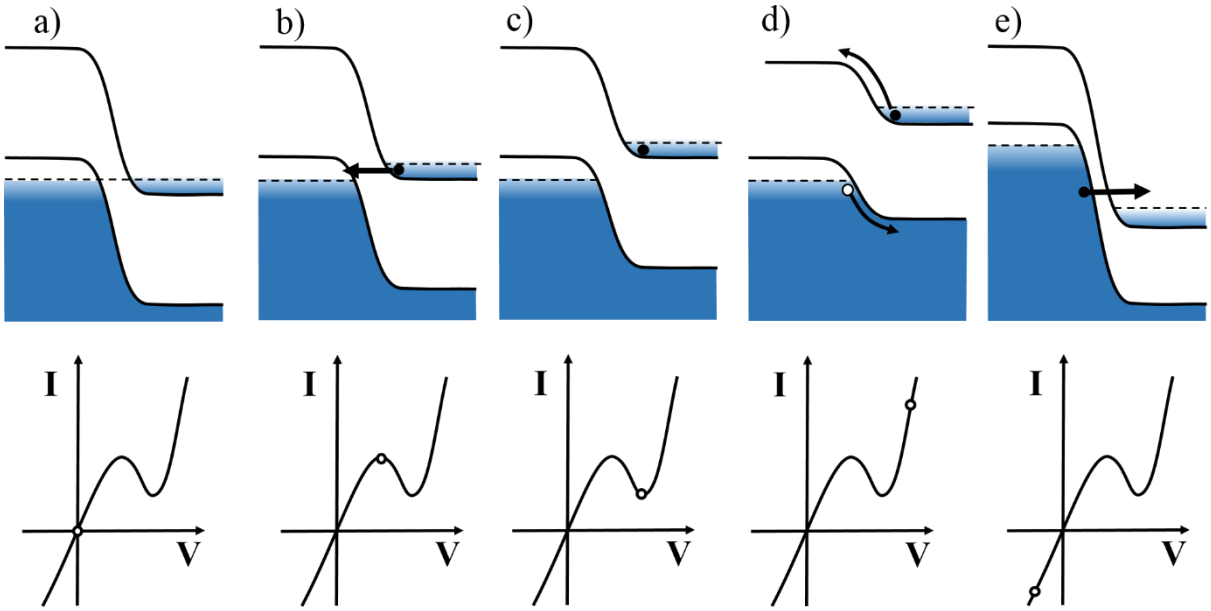

Figure 1 Simplified band diagrams and the corresponding I-V characteristics explaining the current flow in a tunnel diode for different voltage biases. **a)** Thermal equilibrium, zero bias. No current is flowing. **b)** For a small forward voltage bias, electrons in the conduction band of the degenerate n-region tunnel into empty states in the valence band of the p-region. **c)** At higher positive bias the tunneling current decreases as the overlap of the energy bands is reduced and leading to a NDR. **d)** Diffusion current dominate at high forward bias. **e)** For negative bias electrons tunnel from valence band and into the conduction band. This is often referred to as Zener tunneling. After [29].

The tunnel diode, sometimes referred to as *Esaki diode*, was also introduced into the industry. It showed great promise as an oscillator and switching element at high frequencies [30]. Other conventional semiconductor devices would, however, in the course of time outperform and replace the tunnel diode for these functional areas [31]. The tunnel diode was therefore pushed into niche markets. In the fields of semiconductor science and engineering, the BTBT phenomenon continued to fascinate. Although it took some time, this eventually led to the appearance of new device concepts. The first three terminal devices actively addressing and taking advantage of the BTBT phenomenon was proposed by Quinn et al. in 1978 [32]. Their n-MOSFET structure with a heavily doped p-source was designed to yield information about subband splittings of the surface inversion layer. A transistor device concept, with the similar structure as that of Quinn was proposed by Baba [33]. This device was given the name *surface tunnel transistor* (STT). In addition to gallium-arsenide (GaAs) which was used in the

first STT, also Si [34], Si-on-insulator [35] and indium-gallium-arsenide ($In_{0.53}Ga_{0.47}As$) [36] STTs were demonstrated in the course of the 1990's. Many of the early three terminal tunneling devices were focusing on the forward characteristics, and controlling the NDR of the tunnel diode with a gate. However, the Si STT demonstrated by Reddick and Amartunga in 1995 [37], also showed the BTBT current under reverse bias could be controlled. The first vertical Si TFET was proposed and fabricated by Hansch et al. in 2000[38].

In the early 2000's the TFET's potential as a low-power switch became recognized. This followed the realization that the I-V characteristics in the subthreshold region of a TFET was not restricted by the MOSFET's 60 mV/dec subthreshold swing limit at room temperature [39]. This interest got further vitalized by the experimental demonstrations of a devices surpassing this limit by Appenzeller et al. in 2004 [40]. Many groups had at this time directed their focus on the TFET, and soon after more sub 60 mV/dec TFETs were demonstrated [41, 42].

With the attention given due to the obvious potential of the TFET, the challenges of the device became more and more evident towards the end of the 2000's. Although showing great off-state and turn-on characteristics, the drive current was still inferior to that of a MOSFET. The favorable steep turn-on characteristics were also only demonstrated in a narrow and low current regime. The recent years of TFET research, has been revolving around how best to tackle these problems. As with most scientific and engineering challenges, many different solutions have been proposed. In this rapidly advancing field, a wide variety of TFETs, with different material systems and device geometries, are represented in the published TFET studies.

The current status and state-of-the-art of TFETs, is given in the end of this chapter. Some theoretical background will, however, first be given. This can be useful in order to better understand the ideas behind the different TFET concepts, as well as the work presented in this thesis.

1.4 Theoretical Background

The TFET, like the MOSFET, is a three terminal electronic switch. When a voltage is applied between the drain and source contacts, the current flow between them is controlled by the voltage applied to a third terminal, the gate. Both p- and n-channel TFETs are realizable. This offers complementary TFET technology for logic operations, analogous to CMOS technology. TFETs can also be incorporated in industrial CMOS process flow, without additional process steps. The TFET bears a strong resemblance to the MOSFET in this regard. A fundamental difference, with respect to the MOSFET can, however, be found in the mechanism with which

the gate controlled current is flowing and turned on and off. This gives the TFET some unique advantages. In this chapter the operating principles of a TFET will be explained. Both the TFETs potential and challenges will be highlighted.

Understanding the function of a TFET require some basic understanding of energy band theory for semiconductors. The reader is directed to introductory books on the topic like those of Sze and Ng [31] and Schroeder [43], as this topic is too extensive to cover here. Information about the MOS capacitor system and the field effect is contained in Appendix.

1.4.1 Power Consumption of a Logic Element

The TFET is regarded as a candidate for replacing the MOSFET due to its low power operation capabilities. It is therefore natural to start by looking at the power dissipation in digital CMOS circuit, which is given by the following expression [44]:

$$P_{tot} = C_L \cdot V_D^2 \cdot f \cdot \alpha + I_{SC} \cdot V_D + V_D \cdot I_{OFF}. \quad (1)$$

Here, the first term represents the switching component and describes the power dissipated when switching between the on and off state. It is the product of a load capacitance, C_L, the supply voltage, V_D, the clock frequency, f, and an activity factor, α. The second term is the short circuit term when both p-MOSFET and n-MOSFET are simultaneously active and a short circuit current I_{SC} is flowing. The third term is the static power consumption. This term describes the power dissipated due to the presence of a non-zero leakage current, I_{OFF}, when the transistor is turned off. When examining (1) it is clear that the most effective way of reducing the power dissipation would be to reduce V_D. A reduction of V_D should, however, not compromise the drive current in the on-state of the transistor, I_{ON}. Transistors in integrated circuits work together, and the output of one stage of transistors can be used as input of the next stage. In this case the time it takes to charge C_L depends directly on I_{ON}. I_{ON} therefore determines the maximum speed of the circuit. This means that reducing I_{ON} in most cases leads to unacceptable increase in delay time and result in slow operation.

From these requirements an important characteristic of the transistor should be introduced: its rate of current change with respect of the applied gate voltage. This figure of merit is often quantified by the subthreshold swing (SS). The SS is a measure of how much voltage needs to be applied to the gate terminal to induce a change in drain current by one order of magnitude. The average SS of a transistor can be defined as [45]:

$$S_{avg} = \frac{V_D}{\log\left(\frac{I_{ON}}{I_{OFF}}\right)}. \quad (2)$$

The ideal switch would have a step function response, where SS → 0 mV/dec. However, the physics involved in the switching process, in addition to the technological challenges incurred when fabricating an ideal device, prevents this limit from being reached. For a MOSFET, a theoretical limit exist for the lowest achievable SS. This limit originates from the switching mechanism and the thermal injection process of charge carriers over the gate controlled barrier (see Figure 2a). At room temperature this limit is 60 mV/dec [31]. The consequence of this limit for the SS when scaling the voltage V_D is seen in Figure 2 b. As I_{ON} should remain constant, V_D-scaling of a MOSFET leads to a parallel shift of the transfer characteristics (green) with respect to the initial characteristics (black). This leads to at least a tenfold increase in I_{OFF} for every 60 mV of V_D reduction. The static power dissipation in (1) therefore increases when reducing V_D.

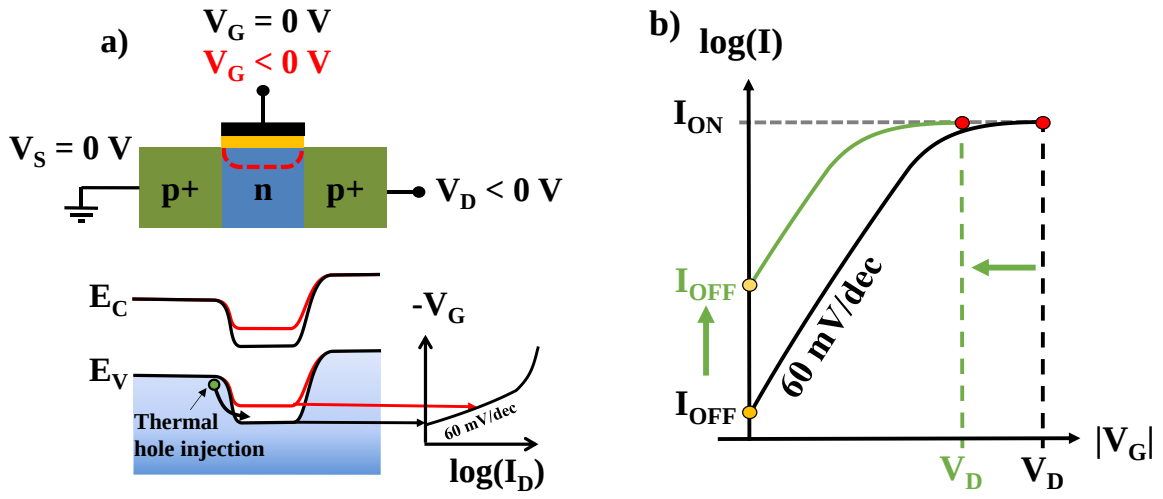

Figure 2 a) Schematic illustration of a p-type MOSFET. The energy band diagrams are shown below for two different gate biases. The thermal injection of holes from source into the channel, limits the SS to 60 mV/dec at room temperature. **b)** V_D scaling of the MOSFET. A tenfold increase in I_{OFF} results for every 60 mV reduction of V_D. The static power dissipation as a results increases.

The inability to surpass this limit is starting to make its presence, as MOSFETs approaching the 60 mV/dec SS limit are already in the market. This has intensified the search for what is referred to as *steep slope* switches: switches with SS < 60 mV/dec (see Figure 3a). One of these proposed switches is the TFET.

1.4.2 Tunneling Field Effect Transistor: Operating Principles

The TFET as a device concept is based on a reversed biased pin diode and the tunneling phenomenon, which was briefly introduced in section 1.3. When the TFET is turned on, the TFET behaves like a tunneling diode in reverse bias mode. A current flows when electrons tunnel from valence band and into the conduction band. This BTBT mechanism, often referred to as *Zener tunneling*, is hence used to attain a drive current in TFETs. However, to prevent this current from flowing in the off-state, the TFET structure differs from the tunneling diode by an intrinsic or lightly doped region which is sandwiched between the high n- and p-doped regions. This region blocks the tunneling current by widening the tunneling barrier. It therefore ensures a low I_{OFF}. To enable to switch between the on and off states, the intrinsic region is gated and serves as the channel region. When applying a gate bias, the energy bands in the channel region are manipulated through the field effect. At sufficient gate bias the energy bands overlap and Zener tunneling is engaged. A p-channel TFET with the corresponding band diagram schematics is shown in Figure 3b. At the onset of tunneling, an ideal TFET shows a very steep I-V relationship which is not physically limited to the 60 mV/dec MOSFET limit at room temperature.

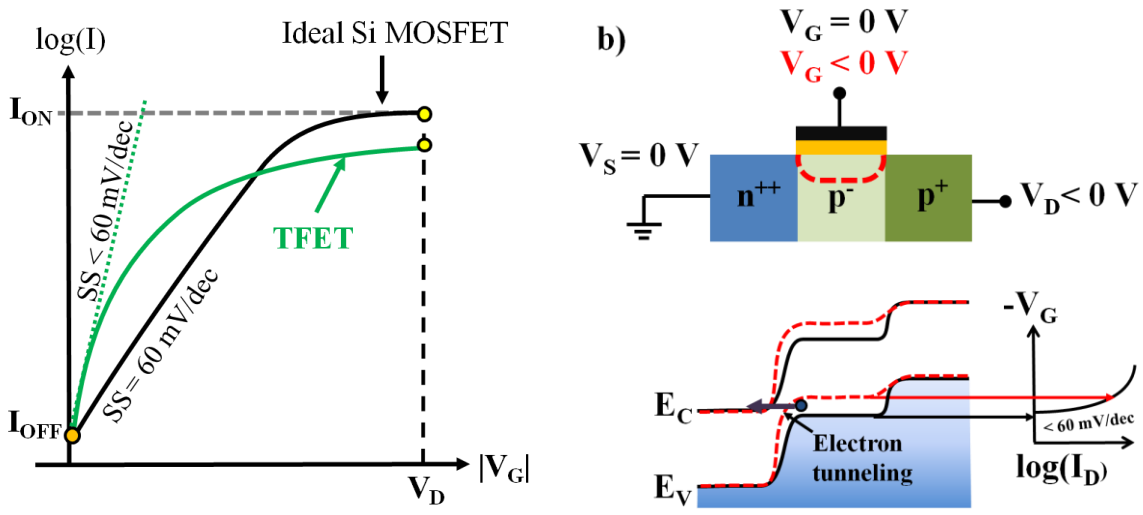

Figure 3 a) A TFET can have a SS < 60 mV/dec at room temperature and therefore offer the possibility of scaling the supply voltage without increasing the leakage current. The I_{ON} of today's TFETs are, however, still inferior to the MOSFET. b) Schematic illustration of a p-channel TFET structure. The energy band diagrams are shown below for two different gate biases. The injection mechanism for a TFET is BTBT of electrons (indicated with an arrow). The BTBT current is activated above a certain gate voltage corresponding to when the channel valence band is above the source conduction band. This switching mechanism offers the potential of steep slope IV-characteristics.

Both p-channel and n-channel TFET have similar pin diode structures. Asymmetric doping profiles, where source doping is higher than the drain doping, should however be used to suppress tunneling at the drain-channel interface [46]. A TFET with symmetric doped pin layer will exhibit ambipolar behavior, since applying a gate bias with opposite polarity can create a tunneling junction and induce current flow at the drain-channel interface. This ambipolarity can also lead to increased leakage current also for zero gate bias. Other suggested device strategies for reducing the tunneling at the drain-channel interface includes structures with gate-drain underlap [47], heterogeneous gate oxide [48] and heterojunction TFETs [49].

1.4.3 Zener Tunneling Current

To analyze the Zener tunneling current in a TFET, one first has to find an expression for the BTBT probability at the channel-source interface. Tunneling of an electron through the forbidden energy gap is analogous to a particle tunneling through a potential barrier. The potential barrier across a pn-junction can be approximated by a triangle, see Figure 4. The height of the barrier equals the bandgap E_G of the semiconductor and tunneling width d is proportional to the tunneling screening length, λ. The tunneling screening length is composed of two components, $\lambda = \lambda_{dop} + \lambda_{ch}$. The length λ_{dop} is the part which is extended into the source region. λ_{dop} therefore depends on the doping abruptness as well as the doping level.

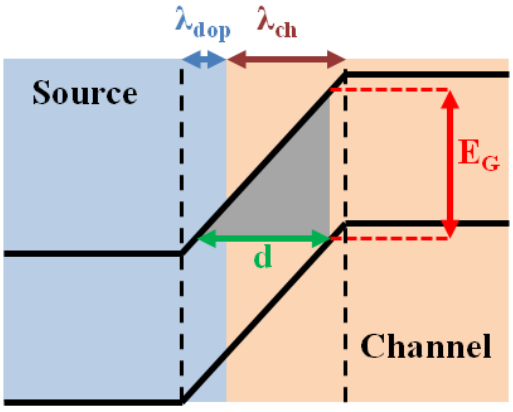

Figure 4 The tunneling barrier at the channel-source interface can be approximated by a triangular barrier (gray area). The height of the tunneling barrier equals the materials bandgap E_G. The spatial width of the tunneling junction is determined by the sum of the screening length in the source λ_{dop} and the channel λ_{ch}, respectively.

In general a high source doping will reduce λ_{dop}. The length λ_{ch} is the part of the width of λ extended into the channel and is strongly dependent on the electrostatic control of the gate. The

tunneling probability through a triangular barrier with a uniform electric field ξ can be given by the Wentzel-Kramers-Brillouin (WKB) approximation [31]:

$$T_{WKB} \approx \exp\left(-\frac{4\cdot\sqrt{2\cdot m^{*}\cdot E_G^3}}{3\cdot q\cdot\hbar\cdot\xi}\right). \tag{3}$$

Here m^{*} is the reduced effective mass, which averages both the electron and hole effective masses. In (3) a high electric field, low effective mass and narrow bandgap is assumed so that the effect of the transverse energy states on the tunneling probability can be neglected [50]. Only electrons within a certain energetic interval, $\Delta\Phi$, contribute to current flow (see Figure **5**). The TFET is therefore said to work as an energy filter, only allowing electrons within $\Delta\Phi$ to flow.

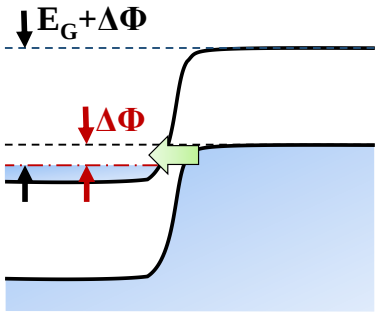

Figure 5 Band diagram of a p-channel TFET with a degenerate n-type source doping in the on-state. Only electrons within the interval $\Delta\Phi$ contribute to the current flow. From the figure one can see that the degeneracy in the n-region, although reducing the tunnel barrier, also reduces $\Delta\Phi$ and can hence limit the current flow.

Now with an expression for the tunneling probability, the total current density can be found by integrating over the energy interval $\Delta\Phi$:

$$J = \frac{2\cdot q}{h}\cdot T_{WKB}\int_0^{\Delta\Phi}[f_S(E)-f_D(E)]dE. \tag{4}$$

Here $f_{S,D}(E)$ is the source and drain fermi-dirac distribution functions, respectively. Through rigorous manipulation of (4) the following result is obtained for the tunneling current [28, 31, 50]:

$$J = \frac{\sqrt{2 \cdot m^*} \cdot q^3 \cdot \xi \cdot \Delta\Phi}{8 \cdot \pi^2 \cdot \hbar^2 \cdot \sqrt{E_G}} \exp\left(- \frac{4 \cdot \sqrt{2 \cdot m^* \cdot E_G^3}}{3 \cdot q \cdot \hbar \cdot \xi} \right). \quad (5)$$

The electric field ξ in this expression can be approximated by:

$$\xi \approx \frac{E_G}{q \cdot d} \approx \frac{E_G + \Delta\Phi}{q \cdot \lambda}. \quad (6)$$

As a major challenge for TFETs is its low tunneling current, the expression in (5) is used as the starting point for many of the TFET performance tuning strategies and state-of-the-art TFETs, which will be reviewed at the end of this chapter. In general, we see from (5), that to increase the current, the exponential term should be made close to unity. With respect to material properties, this necessitates a low bandgap as well as low effective mass. Similarly, the tunneling width λ should be minimized in order to ensure a high transparency of the tunneling barrier.

The indirect tunneling from band-to-band in semiconductors like Si and Ge, requires phonon-assistance to conserve the momentum of the process. Although derived for direct semiconductors, the analytical expression in (5) has been shown to be in good agreement with measured reverse biased heavily doped Ge pn-junctions [51]. The phonon assistance needed for indirect semiconductors, however, significantly lowers the tunneling probability.

Note that (5) does not contain any thermal energy term ($k_B \cdot T/q$), and has therefore a weak temperature dependence, mainly originating from the temperature dependence of E_G. The phonon-assistance needed for indirect tunneling, however, introduces an additional temperature dependence in indirect semiconductors compared to direct semiconductors.

1.4.4 Subthreshold Swing of Tunneling Field Effect Transistors

The SS has already been briefly introduced, and is the parameter most often used to quantify the steepness of the transfer characteristics for a field effect devices. It is defined as:

$$SS = \left(\frac{d\log(I_{DS})}{dV_G} \right)^{-1}, \quad (7)$$

where I_{DS} is the drain-source current, V_G the gate voltage and SS is given in mV/dec. The SS of a TFET is one of the attributes which makes it such an interesting device concept. For a MOSFET the I_{DS}-V_G relationship is well known and SS is given by [31]:

$$SS_{MOSFET} = \ln(10)\cdot\left(\frac{k_B\cdot T}{q}\right)\cdot\left(1+\frac{C_D}{C_{OX}}\right). \quad (8)$$

Here C_D is the depletion layer capacitance and C_{OX} the oxide capacitance. (8) represents the ideal SS, where interface defects and other unidealities degrading the SS are not considered. The C_D/C_{OX} term can be minimized by reducing the oxide thickness. If excellent electrostatic control of the gate is achieved, this term can be neglected, and the minimum obtainable SS for a MOSFET becomes:

$$SS_{MOSFET} = \ln(10)\cdot\left(\frac{k_B\cdot T}{q}\right) \sim 60\ \text{mV/dec} \quad (9)$$

at room temperature.

An expression for the SS of a TFET can be found through taking the derivative of (5):

$$SS=\left(\frac{\partial\log(J_{DS})}{\partial V_G}\right)^{-1} = \ln(10)\cdot\left(\frac{1}{\Delta\Phi}\cdot\frac{\partial\Delta\Phi}{\partial V_G}+\frac{\xi+b}{\xi^2}\cdot\frac{\partial\xi}{\partial V_G}\right)^{-1}. \quad (10)$$

Where:

$$b=\frac{4\cdot m^{*1/2}\cdot E_G^{3/2}}{3\cdot q\cdot\hbar}. \quad (11)$$

We see that there are two terms in the denominator of (10) which should be maximized to achieve a low SS. These terms can be thought to represent two different switching mechanisms [52]. The first term is dominant if the tunneling probability is close to unity and changes little with respect to gate voltage. For a TFET with good electrostatic control we have:

$$\frac{\partial\Delta\Phi}{\partial V_G} \sim q. \quad (12)$$

The SS originating from this term therefore reduces to:

$$SS \approx \frac{\ln(10)}{q}\cdot\Delta\Phi. \quad (13)$$

In this expression, SS increases linearly with V_G and allow for vanishing SS for $\Delta\Phi \rightarrow 0$. This is in contrast to the MOSFET, where SS is almost completely independent of gate voltage.

When having an energy band diagram in mind, this switching mechanism can be thought of as the vertical shift of the energy bands and the band overlap dependence of V_G.

The second term in (10) is dominating if the tunneling probability is small, but varying rapidly with gate voltage. In this case, the switching mechanism is due to gate voltage manipulation of the tunneling width and the junction electrical field (horizontal movement of energy bands). This can be calculated to [53]:

$$SS \approx \ln(10)\cdot \frac{3\cdot q\cdot \hbar\cdot(\Delta\Phi+E_G)^2}{4\cdot\lambda\cdot\sqrt{2\cdot m^*}\cdot E_G^{3/2}}. \tag{14}$$

Due to the quadratic $(\Delta\Phi+E_G)$ dependence, we can see that the expression for SS in (14) changes more rapidly with gate voltage than the term in (13). It also does not vanish for $\Delta\Phi \rightarrow 0$, but can be made small through tuning the parameters λ, E_G and m^*. Comparing (14) and (5) we, however, see that there exists a tradeoff between achieving steep SS and high I_{ON}, with respect to λ and m^*.

The SS in (13) allows for a larger gate voltage range for which SS < 60 mV/dec, compared to (14). When designing a device, this type of switching is therefore the more attractive of the two. In practice, however, the two contributions are coupled and cannot be engineered independently.

1.4.5 Leakage Current Mechanisms in Tunneling Field Effect Transistors

In an ideal switch, no current flows when it is in the off-state. Real devices, on the other hand, will always exhibit some degree of carrier conduction. Different types of transport mechanisms can contribute to leakage currents in TFETs. The type of contributions present and their magnitude depend on the material, device structure and geometry as well as temperature and biasing conditions. In the following section the most common leakage current mechanisms will be introduced.

1.4.5.1 Diffusion Current

Ideally the leakage current of a TFET should be dictated by the diffusion current of the reverse biased diode. An expression for the saturated diffusion current is given by [31]:

$$J_0 = q\cdot\left(\frac{D_p}{L_p\cdot N_D}+\frac{D_n}{L_n\cdot N_A}\right)\cdot n_i^2. \tag{15}$$

Here D_p and L_p are the diffusion constant and diffusion length for holes in the n-region, and D_n and L_n are the diffusion constant and diffusion length for electrons in the p-region. The diffusion current under reverse bias is almost completely independent of drain-source bias. As both source and drain doping levels are high, the diffusion barrier for a TFET is very high. This usually ensures a very low diffusion current at room temperature for TFETs. The quantities D, L and n_i are all temperature dependent, and the temperature dependence of the diffusion current is given by [31]:

$$J(T) \propto T^{\gamma/2} \cdot \left[T^{3/2} \cdot \exp\left(-\frac{E_G(T)}{2 \cdot k_B \cdot T}\right)\right]^2 = T^{3+\gamma/2} \cdot \exp\left(-\frac{E_G(T)}{k_B \cdot T}\right). \quad (16)$$

Here γ is an integer. In the last expression in (16) the temperature dependence of the polynomial term is negligible compared to the exponential term. Diffusion currents therefore have a temperature dependence with activation energy close to bandgap, $E_A \sim E_G$. At high temperatures diffusion currents usually become dominant due to this strong temperature dependence.

1.4.5.2 Shockley-Read-Hall Generation Current

Crystal defects either in the bulk or at the surface can constitute trap states within the forbidden bandgap of the semiconductor. These trap states allow generation of electron-hole pairs to take place within the depletion region (see Figure 6) and contribute to a current flow. The generation rate, U_{SRH}, can be described by Shockley-Read-Hall theory [54, 55]. U_{SRH} is maximized for trap levels with energy E_t close to the intrinsic fermi level E_i, $E_t = E_i$. These midgap trap states are therefore the most effective generation centers. Considering only these traps an expression for the generation rate is given by [31]:

$$U_{SRH} = -\left(\frac{\sigma_p \cdot \sigma_n \cdot v_{th} \cdot N_t}{\sigma_n \cdot (1+n/n_i) + \sigma_p \cdot (1+p/n_i)}\right) \cdot n_i = -\frac{n_i}{\tau_g}. \quad (17)$$

Here N_t is the number of traps, v_{th} is the thermal velocity and $\sigma_{p,n}$ is the electron and hole capture cross sections, respectively. τ_g is the expression inside the brackets and is the generation carrier lifetime. The total generation current is proportional to the diode depletion layer width W_D:

$$J_{ge} \approx q \cdot U_{SRH} \cdot W_D = -\frac{q \cdot n_i}{\tau_g} \cdot W_D. \quad (18)$$

As W_D is dependent on the applied reverse bias, it is expected that:

$$J_{ge} \propto \sqrt{\Psi_{bi} - V}\,, \tag{19}$$

for abrupt junctions. Here Ψ_{bi} is the junction built in potential. The temperature dependence of SRH generation current is governed by the temperature dependence of n_i, if the generation lifetime is a slowly varying function of temperature:

$$J_{ge}(T) \propto n_i(T) \sim T^{3/2} \cdot \exp\left(-\frac{E_G(T)}{2 \cdot k_B \cdot T}\right). \tag{20}$$

The activation energy of a SRH leakage current is therefore close to half the materials bandgap E_G.

1.4.5.3 Tunneling Leakage Currents

The tunneling of electron through the bandgap used as drive current mechanism in TFET can also contribute to significant carrier transport in the off state, especially for devices with short intrinsic channel region and poor electrostatic gate control of the body. Leakage current due to Zener tunneling can be described by a similar expression as to that given in (5).

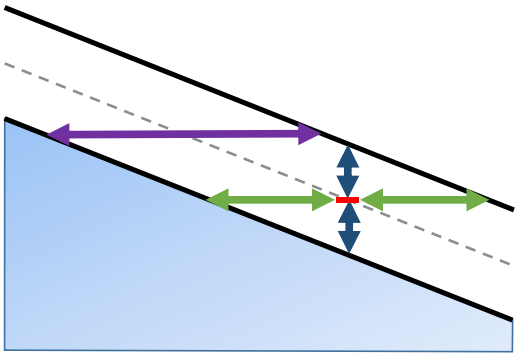

Figure 6 Band diagram showing different leakage current mechanisms. When traps are present in the bandgap, both SRH scattering processes involving mid gap traps (blue arrow), and TAT events (green arrow) increases. A SRH process has a strong temperature dependence, while tunneling process has a strong electric field dependence. When the channel width is small and the electrostatic gate control of the body is poor, BTBT (purple arrow) can take place even in the off state of the transistor.

Traps can also lead to increased tunneling currents due to trap assisted tunneling (TAT). TAT is the tunneling between energy bands and trap states within the bandgap (see Figure 6). The two leakage mechanisms, SRH and TAT, often take place simultaneously. The combined leakage current due to these two mechanism can be described by the Hurkx model [56]. In this model the SRH constant, U_{SRH}, in (18) is replaced by U_{trap}:

$$U_{trap} = (1+\Gamma)\cdot U_{SRH}. \qquad (21)$$

Here Γ is the electric field enhancement factor, which is given by the integral:

$$\Gamma = \frac{E_T}{k_B \cdot T} \int_0^1 \exp\left(\frac{E_T}{k_B \cdot T} \cdot u - \frac{4}{3} \cdot \frac{\sqrt{2 \cdot m^*} \cdot E_T^{3/2}}{q \cdot \hbar \cdot |\xi|} \cdot u^{3/2} \right) du. \qquad (22)$$

Here ξ is the electric field and E_T is the trap energy level, which equals $E_G/2$ for midgap traps. At low electric fields Γ is close to zero and the current is simply given by (18). At high electric fields the tunneling events will dominate as Γ increases.

The temperature dependence of a TAT process is dependent on which of the two processes, tunneling or SRH, is dominating. At low electric fields, the SRH mechanism is usually dominating which as explained above results in an activation energy equal to $E_G/2$. It can, however, become significantly lower when tunneling is dominating at higher electric fields.

As tunneling has a strong electrical field dependence, everything that modulates the electrical field can alter the leakage tunneling rate. For TFETs with short channels and poor electrostatic control of the gate, a dependence of tunneling leakage with the drain-source bias can be seen. This effect is often referred to as drain induced barrier thinning (DIBT), and is due to the modulation of the drain-to-source tunneling barrier width with respect to the drain-source bias.

1.4.5.4 Gate Oxide Leakage Currents

Gate oxide leakage is a shared problem for most field effect devices with aggressively scaled MOS systems. Ideally the energy barrier by the insulating gate oxide should be so large that they prevent the free flow of carriers from the metal to the semiconductor or vice versa. In real insulators on the other hand some degree of carrier conduction will be present at sufficiently high electrical field or temperature. Especially tunneling through the oxide has become a problem as the oxide thickness is scaled down to meet the requirements of modern CMOS technology. The gate oxide leakage can be suppressed by increasing the physical oxide thickness. This however degrades the gate control, as it reduces the total MOS gate capacitance. To omit this problem high-κ materials, materials with dielectric constant larger than that of SiO_2, $\kappa > \kappa_{SiO2} = 3.9$, have become standard in CMOS technology. More information of the leakage current in a MOS-capacitor system is given in Appendix.

1.4.5.5 Gate Induced Leakage Currents and Ambipolarity

Gate induced leakage currents are due to tunneling events taking place in the drain region or at the drain-channel interface of the device. Tunneling at the drain-channel interface, is a unique and often encountered problem for the TFET. This is often referred to as *ambipolar leakage* and is a consequence of the similar pin structures of p- and n-channel TFETs. The gate voltage does not only modulate the source-channel barrier, but also the drain-channel barrier can be altered to the extent where tunneling is allowed.

For devices with a gate-drain overlap, tunneling can also take place in the accumulation layer formed inside the drain. For a certain gate bias the energy bands in this region are bent to the extent that tunneling is allowed. Tunneling taking place in this region is often referred to as gate induced drain leakage (GIDL). GIDL is not unique for the TFET, and has for a long time been known to contribute to leakage current in MOSFETs[57, 58]. Gate induced leakage currents, both ambipolar leakage and GIDL, leads to a distinct *ambipolar* behavior. For a p-type device this means that the drain current increases with positive voltage, and that the drain current increases for negative voltage for an n-type device, respectively. Gate induced leakage currents can also lead to an elevated leakage floor when no gate bias is applied.

The terms ambipolar leakage and GIDL are often used interchangeably, as they both refer to leakage currents induced by the gate. It can however be useful to differ between them as different design approaches might be needed to suppress the two.

1.5 Tunneling Field Effect Transistors: State-of-the-Art

In the above sections the operating principles of a TFET was explained, and expressions for the BTBT drive current, SS and different leakage current mechanisms was given. It is now time to take a look at how one, with this knowledge, best should proceed when engineering a TFET to meet the requirements of the international technology roadmap for semiconductors (ITRS)[59]. At the moment there exists no scientific consensus with regards to this, and a large variety of strategies and TFET concepts have evolved. What follows is therefore an overview of some performance boosters and the state-of-the-art TFETs.

1.5.1 Material System Considerations for Tunneling Field Effect Transistor Design

As has been previously stated, the potential of the TFET lies in its steep subthreshold characteristics. This allows for a much needed supply voltage reduction for the next generations of electronic devices. The gate voltage dependence of the SS for a TFET (see (13) and (14) in

section 1.4.4), leads to that the tunneling current exhibit an early saturation at higher gate voltages. As a consequence I_{ON} of TFETs are, to date, low compared to those of MOSFETs. Increasing I_{ON}, without degrading SS and I_{OFF}, is therefore the TFETs biggest challenge, and a major obstacle for realizing TFETs as viable candidates to replacing MOSFETs.

When focusing on increasing I_{ON}, the expression for the BTBT current (see (5) in section 1.4.3), can be used as a starting point for finding an optimal TFET semiconductor material. This expression states that the materials energy bandgap, E_G, and the reduced effective mass, m^*, and tunneling width λ should be minimized to increase the tunneling current. The first two parameters depend solely on the material system, while λ can be influenced by several parameter, like doping profiles, geometry and gate capacitance [60]. Due to the large bandgap and large carrier mass, Si can in this regard be considered an unideal TFET material. Si TFETs are, however, still the most studied. The know-how, excellent quality and availability of Si is superior to that of any other semiconductor. Of the TFETs that experimentally have demonstrated SS < 60 mV/dec, Si TFET, stands for the largest portion of these reported devices[61]. Experimental studies do however agree with predictions, as Si TFETs exhibit overall low I_{ON}[62, 63, 64]. Of the group IV materials, SiGe and Ge are more interesting. They can easily be integrated on a Si-platform and make it into mass production, but have a reduced bandgap and reduced effective mass with respect to Si. Demonstrated SiGe TFETs[65] and Ge TFETs [66] also show considerably higher I_{ON} compared to Si TFETs. These materials still suffer the same major problem as Si, namely that they are indirect semiconductor materials. In order for electrons to tunnel between bands misaligned in momentum-space, they must also absorb energy from vibrations in the crystal. This significantly lowers the tunneling probability. Potential of group IV materials for TFET, however, lies in direct bandgap transition engineering through strain[67] or through alloying with Sn[68].

Group III-V semiconductors materials such as InGaAs[69], have the advantage that they are direct semiconductors and as a result show considerably higher tunneling currents than those of Si TFETs. Using the mix of two group III-V compounds creating staggered gap heterojunctions, like InGaAs/GaAsSb[70] and AlGaSb/InAs[71], have demonstrated the highest tunneling currents so far, with I_{ON} comparable to that of current MOSFETs. The high currents is a result of the natural overlap between bands which leads to that less voltage is needed to turn these devices on. Group III-V materials are still a bit too exotic for mass production in logic chips. That larger companies like Intel are looking into these materials for the use in MOSFETs [72] , is, however, a sign for that this might only be a temporary showstopper.

Although a bias toward group III-V seems to have evolved for the n-channel TFET, this is not the case for the less studied p-channel TFET. Here the low conduction band density of states is a limiting factor for III-V materials [73]. Finding one single material that is suited for complementary TFET, which is a must if TFETs should be implemented in logic chips, is therefore another problem facing TFETs. Some have suggested that a future complimentary TFET element can consists of both types of material, i.e. group IV material for a p-channel and a group III-V material for n-channel TFET, respectively [74].

Materials that have attracted recent interest are 2D materials like transition metal dichalcogenides and graphene [75]. These offer high electron tunneling efficiency through a broken-gap band alignment and a low I_{OFF} through band gap engineering of drain material. Even though these materials are at a very early stage, TFETs have already been demonstrated [23, 76].

When choosing a material with the sole purpose of increasing the tunneling current, one can run into trouble. Especially with bandgap engineering, the tradeoff due to increase of leakage current with lowering of the bandgap becomes a problem. The above referred to III-V staggered bandgap heterojunction TFETs and also low bandgap Ge and GeSn TFETs [77], which show high I_{ON}, also exhibit high leakage currents and poor I_{ON}/I_{OFF}-ratio. These devices have not been able to demonstrate SS < 60 mV/dec. This is not only due to low bandgap, but also a consequence of the low quality of these material. Crystal defects, both in the bulk at the surface, increase SRH and TAT leakage currents. With respect to material quality, TFETs are said to require a much higher degree of perfection than previous electronic devices [78]. Novel materials, that are predicted to show excellent TFET characteristics, often lack technological experience. This is thought to be the main reason for the large gap between the experiments and the much more optimistic theoretical predictions of TFETs, which often neglects nonidealities [61].

The drain and source doping profiles are other material parameters which can be tuned to improve device performance. The source doping profile and level determines the tunneling barrier width λ, while the drain doping profile affects the electrical field and ambipolarity. A high and abrupt source doping is needed to ensure a small depletion width in the source. A source doping abruptness of less than 4 nm/dec is needed to maximize I_{ON} [50]. However, degeneracy limits the number of electrons available for tunneling and can reduce I_{ON}.

The gate oxide material is important to ensure a good electrostatic control of the gate. Both a higher I_{ON} and a lower SS can be obtained by increasing the gate oxide capacitance[79]. The problem of having a high oxide capacitance, but on the same time preventing gate oxide

leakage, is thanks to the advances in MOSFET technology, solved by implementing high-κ oxides. Some common high-κ oxides are HfO_2, Al_2O_3 and ZrO_2. Many semiconductor/high-κ surfaces, however, suffer from very high interface trap densities (D_{it}), which prevents low SS of being achieved [48]. Surface passivation chemistry has therefore become an essential part of the work in improving future TFETs.

1.5.2 Geometry Considerations for Tunneling Field Effect Transistor Design

In order to improve TFET performance, geometry and device design is also important in order to utilize the material system at hand. In bulk TFETs, a trade-off exist between achieving high on-currents and small values for SS. 1D systems, achieved with nanowire geometries, and 2D crystals have been proposed as ideally suited for realizing TFETs with high I_{ON} and low SS [53, 80]. In nanowire geometries the electrical gate field penetrate the entire body and therefore represents the ideal electrostatic gate control. In this devices a pn-structure is often used and the positional dependence of the gate with respect to the junction is used to separate the p-channel and n-channel TFETs. The gate metal is chosen to deplete the channel in the off state, an *intrinsic* region is then achieved electrostatically. Achieving 1D and 2D systems is, however, technologically challenging, and not realizable for all materials. Scaling down to the atomic level also introduces a problem of variability, where placement and concentration of dopant atoms and interface roughness can significantly change the electrical properties [81].

In addition to reducing body thickness, well aligned gates are a key technological challenge. Both unintentional gate-underlap and overlap can have serious deteriorating effects on the TFET performance [82].

Having an intentional source-gate overlap has been shown to boost drive currents in Si [83] and SiGe [84] TFETs. In this case tunneling does not only takes place at the source channel interface, but also inside the gate overlapped source region.

Channel length is another design consideration. A channel reduction can reduce the channel resistance and hence increase I_{ON}[85]. TFETs are less prone to short channel effects compared to MOSFETs, as the barrier height is not affected by a channel reduction. Direct source-to-drain tunneling leakage, however, is a problem for TFETs with very short channels and poor electrostatic gate control of the body. These devices often exhibit DIBT, where the leakage current is a strong function of the drain-to-source voltage.

Many considerations must be made when the optimal material system and design of TFETs are discussed. In most cases tuning parameters are entangled and will affect each other. This very often leads to tradeoffs. It is also expected that an additive combination of performance

boosters, simultaneously optimizing many parameters, are needed to achieve TFETs compatible with modern MOSFETs [60]. The recently reported ATLAS TFET [23] is a good example of the complexity which one might expect to see more of in the future. This device has a two dimensional TFET geometry with molybdenum disulfide as channel material and a highly doped Ge as source material. It has demonstrated a record SS of 3.9 mV/dec and an average of 31.1 mV/dec for over four decades of drain current at room temperature. The I_{ON} of this device is however two orders of magnitude below the ITRS requirement [59].

1.6 Thesis Overview

This thesis details four approaches for performance tuning of p-channel TFETs. The focus of these approaches is mainly given to bandgap and doping profile engineering of the group IV materials Ge and GeSn. These materials are realizable on a Si platform, but have lower bandgaps compared to Si, which is favorable for improving I_{ON}. Some device design aspects are also considered, as the influence of having a gate-source overlap region in the vertical TFET structures is studied. The TFET are studied through the fabrication and subsequent electrical characterization. Area and temperature dependence is also considered and used to separate different leakage current contributions, and to evaluate and predict scaling trends.

In addition, two experiments investigate the passivation methods for the Ge surface through the fabrication and electrical characterization of Ge/Al_2O_3 MOS capacitors.

A short description and overview of each of the remaining chapters will now be given.

Chapter 2 - Vertical Tunneling Field Effect Transistor Device Fabrication and Data Acquisition

The TFETs presented in this work were all fabricated in the clean room at IHT Stuttgart. In this chapter the details of the device fabrication and procedures will be described. First some information of the molecular beam epitaxy (MBE) system and growth of group IV semiconductor materials is given. A second part of this chapter gives a walkthrough and a detailed scheme of the gate-all-around (GAA) fabrication process used after epitaxial growth to attain measurable TFET devices. Some information of the data acquisition and processing is also enclosed in the end of this chapter.

Chapter 3 - Germanium-Tin P-Channel Tunneling Field Effect Transistors: the Effect of Tin-Content in Germanium-Tin Channel

The effect of implementing the low bandgap material germanium-tin ($Ge_{1-x}Sn_x$) in Ge p-channel TFETs is presented in Chapter 3. At the onset of this thesis, there existed no published experimental or simulation studies of $Ge_{1-x}Sn_x$ TFETs. The prediction of achieving a direct group IV semiconductor through alloying Ge with Sn [86] had, however, gained considerable momentum, and the potential of incorporating the material in TFETs was not only considered by our group. The first demonstration of a $Ge_{1-x}Sn_x$ TFET was presented in 2013 by Yang et al. [87]. The handful of published studies on $Ge_{1-x}Sn_x$ TFETs so far, are all similar with respect to its goal, namely the prospect of increasing the tunneling probability and drive currents through bandgap engineering. With the focus on vertical structures, where the pin layer structures are achieved by means of MBE, and through examining the bulk and surface current properties, the study presented in this chapter gives new relevant information on the potential and challenges of the $Ge_{1-x}Sn_x$ material system.

It is shown that I_{ON} successively increases with increasing Sn-content in the channel. A successively increase in bulk leakage currents is also reported, which is concluded to stem from bandgap reduction and degraded crystal quality. Area dependence on the electrical characterization predicts improved SS with increased Sn-content by further downscaling.

Chapter 4 - Germanium-Tin P-Channel Tunneling Field Effect Transistors: Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface

In this chapter the $Ge_{1-x}Sn_x$/Ge heterojunction TFET design space introduced in Chapter 3 is further explored, through looking at the positional placement of a 10 nm $Ge_{0.96}Sn_{0.04}$-δ-layer at the source-channel interface. With the assumption that the leakage current can be reduced when the $Ge_{0.96}Sn_{0.04}$ is confined within in a δ-layer, this experiment aims to investigate how this layer should be positioned at the source-channel interface to maximize I_{ON}. The area and temperature dependence on the electrical characterization is reported.

Chapter 5 - Source Doping Concentration Variation in Germanium P-Channel Tunneling Field Effect Transistors

In Chapter 5 the effect of varying the source-doping concentration in Ge p-channel TFETs with source gate-overlap is presented. In TFETs with gate-source overlap it is assumed that two type of tunneling currents contribute to I_{ON}, namely tunneling at the source-channel interface,

point-tunneling, and tunneling in the gate overlapped source region, *line-tunneling.* For these TFETs, the source doping concentration can become an important tuning parameter with respect to improving I_{ON}, as its magnitude is expected to affect these current contributions in different ways.

Simulations presented by Vandenberghe et al. [88] have suggested that an optimal doping concentration exist for TFETs with gate-source overlap. The study presented in this chapter is, however, the first which experimentally investigates the effect of varying the source doping concentration in Ge TFETs. Contrary to the simulations, little effect of the source doping concentration on I_{ON} is observed. The SS, on the other hand, can be seen to improve with increasing source doping concentration.

Chapter 6 - Source Doping Profile Tuning in Germanium P-Channel Tunneling Field Effect Transistors through Molecular Beam Epitaxy Antimony Pre-Buildup

TFETs require very abrupt source doping profiles to maximize I_{ON}. A well-known method for achieving steep doping profiles with MBE is through a pre-buildup doping technique [89]. With this technique doping segregation, which is the main cause of doping profile smearing in MBE, is compensated.

In the study presented in this chapter, this method is for the first time implemented in the fabrication scheme of vertical TFETs. The effect of varying the Sb monolayer (ML) buildup concentration on the electrical characterization of these devices is studied through three samples. Small improvements both in terms of I_{ON} and SS can be seen for a Ge p-channel TFET with 1/10 ML Sb concentration.

Chapter 7 - Electrical Characterization of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors Passivated through Post Plasma Oxidation

A good surface quality is essential for not degrading the TFET's SS, I_{ON} and I_{OFF} through interface traps. As high-κ/Ge surfaces in general have a high D_{it}, improved Ge surface passivation methods are necessary for future Ge based TFETs. In Chapter 7 a post plasma oxidation passivation method of the Ge surface is investigated through the fabrication and electrical characterization of $Ge/Al_2O_3/Al$ on Si-substrate MOS capacitors. The post plasma oxidation is performed with the aim of creating a germanium oxide (GeO_x) interfacial layers between the Ge and Al_2O_3.

This passivation method was implemented in the fabrication scheme of the TFETs presented in this thesis, and the electrical characteristics provide supplementary information of the Ge

surface quality, which is relevant to these studies.

Chapter 8 - Impact of Sulfur Passivation on the Electric Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

Sulfur (S) has emerged as an attractive candidate for passivation of the Ge surface. S-passivation, has also been implemented in the fabrication scheme for $Ge_{1-x}Sn_x$ based field effect devices [90]. Passivating Ge- and $Ge_{1-x}Sn_x$ interfaces through S is, however, relatively new with the first experiments performed less than a decade ago [91]. More experimental studies are therefore called for, in order to better assess its potential as a standardized passivation method for Ge based devices.

In this chapter, S-passivation of the Ge surface is studied through the fabrication and electrical characterization of Ge/Al_2O_3 MOS capacitors. It is shown that the S-passivation reduces the leakage current for low electrical fields and reduces the C-V characteristic hysteresis. This does not come at the expense of a thicker equivalent oxide thickness.

Chapter 2 Vertical Tunneling Field Effect Transistor Device Fabrication and Data Acquisition

The devices investigated and presented in this thesis were all fabricated in the clean room at IHT Stuttgart. The device fabrication process itself can be divided into two main parts: (I) the epitaxial growth of the semiconductor layer structures and (II) the process of transforming the layer structure into vertical GAA field effect devices. These two parts are the subject for the first two sections in this chapter, respectively. In the third section information of the electrical measurements, data acquisition and data processing are given.

2.1 Molecular Beam Epitaxy

For the optimal device performance of a TFET, many requirements have to be fulfilled with respect to the semiconductor structure. Abrupt and high concentration doping profiles are especially important. Additionally a high crystalline quality is needed to avoid high leakage currents and degradation of the device performance. In this work MBE was used to grow the semiconductor layer structures. MBE is a form of physical vapor deposition process, where deposition onto a crystalline substrate is conducted under ultrahigh vacuum (UHV) conditions. Compared to other epitaxial growth methods, MBE is unique in the way that it allows deposition at very low substrate temperature, controlling growth reproducibility to atomic monolayer dimension and the ability of real time monitoring of the growth process itself.

Figure 7 shows an example of the schematics of a standard equipped MBE chamber. The substrate is positioned in the top of the chamber, facing down towards the effusion cells and electron beam evaporators positioned at the bottom of the chamber. The substrate temperature is controlled by a radiation heater positioned above it, radiating the backside of the wafer.

A very important requirement for successful MBE growth is keeping the substrate surface clean from contaminants. When a substrate surface is contaminated, the crystal information is lost for the impinging atoms. This may result in everything from crystalline defects to polycrystalline, or in the worst case, amorphous growth [22]. To avoid this, UHV conditions are necessary to ensure minimal background vapor. The necessity of UHV conditions also leads to a mean-free path of the atoms longer than the dimensions of the MBE chamber. Atoms therefore form a beam, as they move from their source and onto the substrate without collisions inside the chamber.

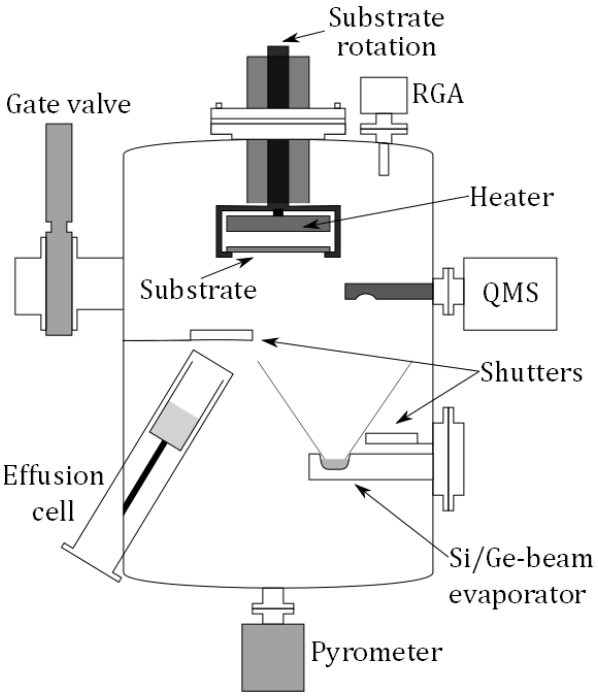

Figure 7 Schematics of a MBE chamber showing the main components. The substrate is positioned at the center in the upper part of the chamber, and faces downward towards the effusion cells and e-beam evaporation. The substrate temperature is controlled by a radiation heater situated above. A residual gas analyzer, a quadrupole mass spectrometer and a pyrometer are examples of measurement devices that allow real time monitoring, as well as control, of the growth process.

2.1.1 Molecular Beam Epitaxy Growth Process

A well collimated beam of the required constituents is achieved through electrical heating of their respective evaporation sources. In this work an electrical beam evaporator was used for Si and effusion cells were used for Ge and Sn, respectively. A calibrated beam supports a constant flux of atoms impinging onto the substrate. From here the MBE growth process itself is dominated by the substrate surface kinetics of atoms, or molecules, reacting with the top atomic layer of the substrate [92]. The surface kinetics of the MBE process can be described by the interaction between three states (I-III): (I) Free atoms impinging onto the surface. (II) Adsorbed atoms, *adatoms*, which stick to the surface, but are mobile on the substrate surface. (III) Atoms that are incorporated into the crystal. The second state is especially important as it enables the atoms to move to the crystal lattice positions, as opposed to random positions, and the substrate crystal structure is preserved. Epitaxial growth takes place when an atom goes from the process adsorption (I) → (II), followed by incorporation (II) → (III). However the processes desorption (II) → (I), and detachment (III) → (II), as well as reflection (I) → (I), can also take place. The different rates of all of these processes depends on the surface temperature, beam flux and material properties (e.g. sticking coefficient and ionization energy). A natural

requirement for epitaxial growth is that the rate of incorporation must be higher than rate of detachment and desorption. When this condition is fulfilled, high temperatures are usually necessary for good crystal quality. In MBE processes, substrate temperatures close to or below half the melting point of the material are common [92].

2.1.2 Doping in Molecular Beam Epitaxy Systems

In MBE, doping is achieved by simultaneously incorporating dopant atoms during growth. For group IV semiconductors arsenic (As), phosphorous (P) and antimony (Sb) are the most common n-type dopants, while boron (B), aluminum (Al), gallium (Ga) and Indium (In) are common p-type dopants. The choice of which dopant element to use is based on different criteria. Important is the solubility of the dopant material in the matrix crystal, the ionization energy, its vapor pressure, diffusibility and the general handling of the material (e.g. toxicity). Properties for different dopants are shown in Table 2.

Table 2 Properties of dopants.

Dopant	Type	Solubility in Si [211]	Solubility in Ge [211]	Ionization energy (eV) [31]	Temperature for $P = 1.3 \cdot 10^{-4}$ Pa (K) [212]
B	p	0.8	17	0.045	1773
Al	p	0.002	0.073	0.067	1093
Ga	p	0.008	0.087	0.072	953
In	p	$4 \cdot 10^{-4}$	0.001	-	-
P	n	0.35	0.08	0.045	353
As	n	0.3	0.02	0.054	433
Sb	n	0.023	0.003	0.039	623

In the MBE system used in this work B and Sb are used as p- and n-type dopant, respectively. B is the obvious choice for p-type dopant, as it has the highest solubility and lowest ionization energy. Sb is used as n-type dopant. Although Sb has a lower solubility than both P and As, the vapor pressure of these other two elements is very high. This makes dopant control difficult, as well as it leads to chamber memory effects and higher background doping [92]. In addition, P and As are both extremely toxic, which makes handling an issue.

For TFETs abrupt and high level doping concentrations are required. The MBE technique allows epitaxial growth at low temperatures in regimes were dopant diffusion is negligible. For MBE growth surface segregation is the dominant mechanism for doping profile smearing. Especially for Sb, segregation in both Si and Ge must be appropriately taken into consideration [93]. Surface segregation describes the situation of when it is more energetic favorable for an atom to stay mobile on the surface than it is to be incorporated into the crystal matrix. With a constant dopant beam flux, the mismatch between incorporation and adsorption causes a buildup of dopant adatoms. Only after reaching a certain adatom concentration, does the number of dopants incorporated into the crystal matrix equal the number of dopants delivered by flux. Different techniques can be used to suppress dopant profile smearing resulting from surface segregation. *Co-evaporation* describes growth where the direct incorporation of dopants takes place. This technique requires that the substrate temperature is lowered to the point where segregation is negligible. A substrate temperature lowering usually introduce more point defects into the layer and can degrade the crystal quality [92]. It hence represents a tradeoff. Another technique, often used when sharp doping profiles and high doping concentration are required, is *pre-buildup*. In the pre-buildup technique, the dopant adatoms concentration are pre-adjusted while the growth of the matrix material is temporarily arrested [89]. A high initial adatom concentration will compensate the surface segregation and provide a steady-state doping process.

Other MBE doping techniques include solid phase epitaxy [94] and direct- and secondary ion-implantation [92].

2.1.3 Molecular Beam Epitaxy Growth of Germanium on Silicon

In this work Si <100> wafers were used as substrates for the Ge based TFET devices. Although Ge substrates are available, they are often much more expensive and less durable than the Si alternative. For integration purposes, which is an important requirement when considering the TFET, Si substrates are hence the only viable option. A complicating factor by using Si substrates is, however, the heteroepitaxial growth of Ge on Si. As Ge has a lattice constant, a_{Ge}, which is 4 % larger than the lattice constant of Si, a_{Si} (see Table 1 in section 1.2), Ge will experience a compressive strain when grown directly on Si. Strain can significantly alter the electrical properties of a material, by changing its bandgap, effective mass and carrier mobilities [95]. The epitaxial growth of perfect dislocation-free strained Ge, where Ge has taken on the lattice parameter of Si, is known as pseudomorphic growth (see Figure 8b). This type of growth will continue until a critical thickness of stability is reached [96]. This thickness

corresponds to the stage in the growth process where the first dislocation is formed, releasing some of the built in strain (see Figure 8c)[1]. The relaxation through dislocation formation will usually continue until the lattice constant of Ge is reached. A dislocation consists of one segment that is perpendicular to the growth direction, these are referred to as *misfit dislocations*. At the two ends of a misfit dislocation one finds segments that thread upwards to the substrate surface (60° on the <111> plane for growth on <100> substrates) [97]. These latter are referred to as threading dislocations. Although necessary for relaxation, dislocations represents defects in the crystal which could constitute trap states within the bandgap of the material. A certain number of traps, N_T, can be found per length of dislocations (a value of traps per length is found in [98], with $N_T = 10^6$ cm^{-1} for SiGe material systems). Traps can significantly deteriorate the performance of electronic devices, and are therefore very undesirable.

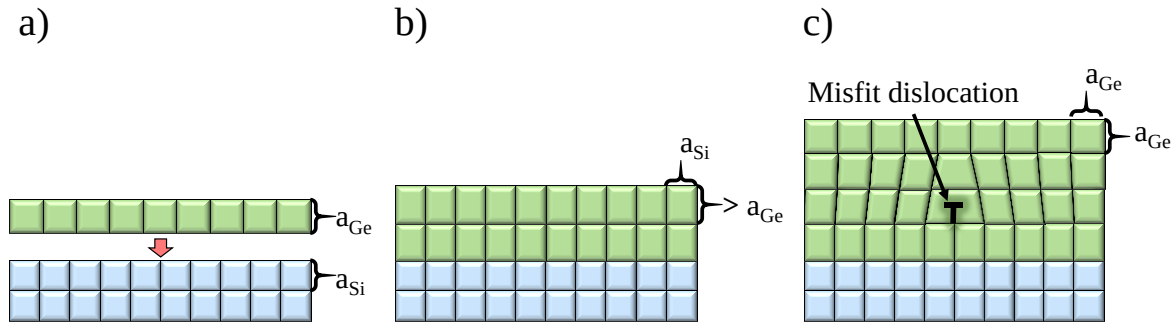

Figure 8 a) Heteroeptixial growth of Ge on Si can be problematic due to the lattice mismatch between Si and Ge, $a_{Ge} > a_{Si}$. **b)** Pseudomorphic growth of Ge. Here the grown Ge takes on the lattice constant of Si. Strain is effectively built into the grown crystal structures. **c)** Strain is relieved through the formation of misfit dislocations.

A method of controlling the defect formation for the active layers of Ge grown on Si is through the formation of a Ge virtual substrate (VS). In addition to the bulk Si substrate the VS consists of a relaxed buffer layer. The purpose of such a buffer layer, is to form a misfit dislocation network which is fully contained within the VS itself. In this way the lattice constant mismatch is adjusted and the misfit dislocation formation is limited for the successively grown Ge layers. The ideal VS should also have a limited number of threading dislocations interfering with the active layers grown above the buffer. For integration, as well as reduced heat dissipation, a low thickness of the buffer layer is preferred [99]. The SiGe buffer technology has been crucial for the high mobility strained Si, SiGe and Ge channel MOSFETs [100].

[1] This is a simplified picture of the growth process. For the Ge on Si system the built-in strain is released through the formation of three dimensional islands. After these islands has been formed, misfit dislocations are formed at the interface of these islands, and the surface again becomes smooth with continued growth. This is known as Stranski-Krastanov growth [213].

The Ge VS used for the devices presented in this work is unique by that it is consists of a very thin buffer layer, d_{buffer} = 100 nm. The buffer layer is formed by the epitaxial growth of Ge direct on Si at a substrate temperature of T_{sub} = 330 °C. After the deposition of Ge on Si, the growth process is temporarily arrested. The strain is then adjusted through a high temperature annealing step at a substrate temperature of T_{sub} = 810 °C, with a duration of five minutes. During this step the misfit dislocation segments are extended and the threading dislocations glide to the edge of the wafer were they are less likely to interfere with the active epitaxial layer grown onto the buffer [97].

2.1.4 Molecular Beam Epitaxy Growth of Germanium-Tin

The MBE growth of $Ge_{1-x}Sn_x$ can be considered a relatively new discipline. Although a handful of groups conducted $Ge_{1-x}Sn_x$ MBE studies in the late 80's and early 90's[101, 102, 103, 104, 105], the significant share of MBE-$Ge_{1-x}Sn_x$ studies has been conducted during the last decade. The promise of a group IV direct bandgap material through incorporating Sn into $Ge_{1-x}Sn_x$, has attracted considerable interest to $Ge_{1-x}Sn_x$ for optoelectronic uses [106]. A direct and low bandgap material is also interesting for TFETs, due to the prospect of significantly increasing the BTBT probability and hence the drive current[107]. Due to the large lattice mismatch of 14.7 % between α-Sn and Ge, and the low solid solubility of 1 % of Sn in Ge, a lot of experimental effort is currently directed towards the epitaxial growth of $Ge_{1-x}Sn_x$ [108, 109, 110]. The epitaxial growth of $Ge_{1-x}Sn_x$ usually has to be performed at very low temperatures (typically T_{sub} < 200 °C), to suppress segregation and phase separation of Sn [111]. Simultaneously obtaining high Sn-content and achieving high crystal quality at these low temperatures is the major challenge for $Ge_{1-x}Sn_x$ grown by means of MBE.

In this work the $Ge_{1-x}Sn_x$ was grown on Ge, and is used in the active layer of the TFET structures. $Ge_{1-x}Sn_x$ has a larger lattice constant than Ge. Like the heteroepitaxial growth of Ge on Si, the growth of $Ge_{1-x}Sn_x$ on Ge will therefore introduce a compressive strain in the $Ge_{1-x}Sn_x$ layers (analogous to Figure 8b). The expected critical thickness of $Ge_{0.96}Sn_{0.04}$ (the highest Sn-content used in this work), is, however, thicker than the $Ge_{1-x}Sn_x$ layer thickness used[112]. It is therefore assumed that all grown $Ge_{1-x}Sn_x$ layers reported in this work is pseudomorphic biaxially strained with respect to the underlying Ge. This compressive strain increases the separation between the indirect and direct band edges, compared to fully relaxed $Ge_{1-x}Sn_x$. The predicted crossover of the indirect and direct bandgap as a function of Sn-content and strain is a matter of ongoing debate, but a recent experimental study have shown a that the crossover concentration is x ~ 9 % for fully relaxed $Ge_{1-x}Sn_x$ [113]. For pseudomorphic $Ge_{1-x}Sn_x$ on Ge,

a Sn-content of at least x = 17 % has been proposed [114], but some have also argued that no indirect-direct transition can be obtained with the external compressive strain arising from the Ge-substrate[115].

2.1.5 Molecular Beam Epitaxy Growth of Germanium/Germanium-Tin P-Channel Tunneling Field Effect Transistors

Bellow follows a description of the growth procedure for Ge/ $Ge_{1-x}Sn_x$ p-channel TFETs as it was performed in this work.

A high temperature (T_{sub} > 900 °C) surface cleaning step [116] is performed before growth. This is performed to ensure an initial clean surface and remove the native oxide, which is essential for high quality epitaxial growth. As explained in 1.4, the TFET has a pin diode layer structure. For a p-channel TFET the p-region serves as a drain and the n-region as a source, respectively. For the vertical devices presented here the buried layer serves as the drain, and top layer as the source. The growth therefore starts with the heavily p-doped drain regions. The first layer is a Si buried layer. This layer serves as a contact layer as well as it reconstructs the crystal surface, covers remaining surface contaminants and ensures a smooth surface for successive growth. The thickness of this layer can be reduced by using heavily p-doped substrates. In which way the substrate itself serves as contact layer. The drain region continues with the growth of the Ge VS buffer layer which was described above in section 2.1.3. As the VS is a part of the drain region, the drain current has to flow through it during operation. This buffer layer therefore ads to the total series resistance. The Ge VS is heavily p-doped as a measure to reduce the resistance of this layer. Due to the high annealing temperature needed to form the Ge VS, it is essential that the pin layer structure is grown in this order. Sb-doped Ge cannot be annealed at temperatures above 500 °C due to the strong diffusion of Sb in Ge[117].

On the Ge VS, a relaxed Ge drain region is grown. This region is, after device fabrication, overlapped by the gate electrode. A very thick drain layer might enhance gate induced drain leakage currents. Except for this, the thickness of this layer is not a critical parameter with respect to the TFET device performance, and can be adjusted to control the total mesa height. The drain doping level N_A should be lower than the source doping level to suppress ambipolar leakage [46]. The doping concentration in this layer should therefore be chosen based on this criteria. For the all devices presented in this work a drain doping of $N_A = 1 \cdot 10^{18}$ cm^{-3} was used. This doping concentration was either constant in the entire Ge drain region, or a doping gradient was used. A doping gradient was achieved by adjusting the effusion cell temperatures to pre-calibrated set values during growth. During the growth, the doping concentration is reduced

from the initial high doping concentration of the Ge VS to the $N_A = 1 \cdot 10^{18}$ cm^{-3} doping at the channel interface. The advantage of this doping strategy is that it avoids growth interruption, which can allow incorporation of background impurities.

The intrinsic channel region is grown next. For the MBE system used in this work, an unintentional p-type background doping is present. This p-type doping concentration has been established from C-V measurements of pin diode structures to be $p_i \sim 1 \cdot 10^{16}$ cm^{-3} for Ge, and $p_i \sim 1 \cdot 10^{17}$ cm^{-3} for $Ge_{1-x}Sn_x$ with x = 4.2 % Sn-content [118]. A background doping of $p_i = 7 \cdot 10^{16}$ cm^{-3} has been established from C-V measurements of Al_2O_3/Ge MOS capacitors (results are given in Chapter 7). For growth of $Ge_{1-x}Sn_x$ in the channel region of the TFET, a growth temperature of T_{sub} = 160 °C was used to avoid surface segregation. In this work, the influence of the channel thickness, t_{ch}, on the TFET device performance was investigated. Different channel thicknesses was used in the different experiments. The range of channel thickness was varied between a minimum of t_{ch} = 50 nm, and a maximum of t_{ch} = 200 nm.

The n-doped source region is the final step in the growth process. This region starts with a highly n-doped Ge layer. The source doping profile is a critical parameter for TFETs, because the channel-source interface represents the position where BTBT takes place. To achieve abrupt source profiles with low surface segregation, this region is grown at low temperatures (T_{sub} = 160 °C). The effect of varying the source doping concentration on the TFET is the topic of Chapter 5, while implementation of a Sb-pre-buildup with different pre-buildup ML concentrations is the topic of Chapter 6. These topics are discussed in more detail in these chapters, respectively. The influence of the source layer thickness on the device performance is not primarily of any great importance. It can become influential, if a gate-source overlap exists. In the devices presented here the entire Ge source region is overlapped by the gate. Gate induced tunneling currents in this overlap region can affect the drive current as well as the subthreshold swing of the TFET. This will be shown in Chapter 5. Because of Fermi level pinning, Al and n-doped Ge contacts show a rectifying behavior [119]. A heavily Sb-doped Si cap layer is therefore grown as a final layer as part of the source region to ensure an ohmic top contact.

A MBE layer schematic of a vertical Ge TFET is shown in Figure 9. Information on the exact layer structure for each experiment is given in each chapter.

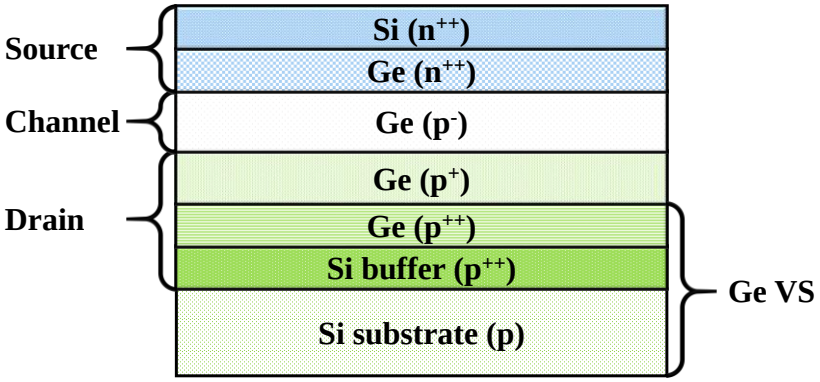

Figure 9 MBE layer schematic for vertical Ge TFETs.

2.2 Vertical Gate-All-Around Device Fabrication of Germanium Based Tunneling Field Effect Transistors

After MBE growth vertical TFETs were fabricated using a GAA fabrication process. The process flow of the fabrication process and device schematics at the different stages in the process are shown in Figure 10. This device fabrication process was initially developed at IHT Stuttgart by Daniel Hähnel, but further process development was performed during the work on this thesis. This thesis' contribution to the device fabrication process involves passivation methods for the Ge/Al_2O_3 interface and downscaling of the gate oxide thickness. In addition, a photolithography mask was developed for the contact windows of the devices.

A fabricated 35 mm x 35 mm chip contains in total 3600 transistors with area to perimeter ratios varying between A/P = 0.78 µm^2 / 3.14 µm (smallest) to A/P = 100 µm^2 / 40 µm (largest). Both circular and square shaped mesas are provided by the mask layout. Through using electron beam lithography and additional process steps, mesas with diameters < 100 nm can be attained through this GAA fabrication process [77]. For the TFETs presented in this thesis, however, only normal photolithography was used. This had the advantage of being a more robust process, less time-consuming and producing a higher number of working transistors. A finished chip also contains circular diode structures, without gate electrode structures. These structures allow for additional electrical characterization of the MBE layers, without the influence of a gate field.

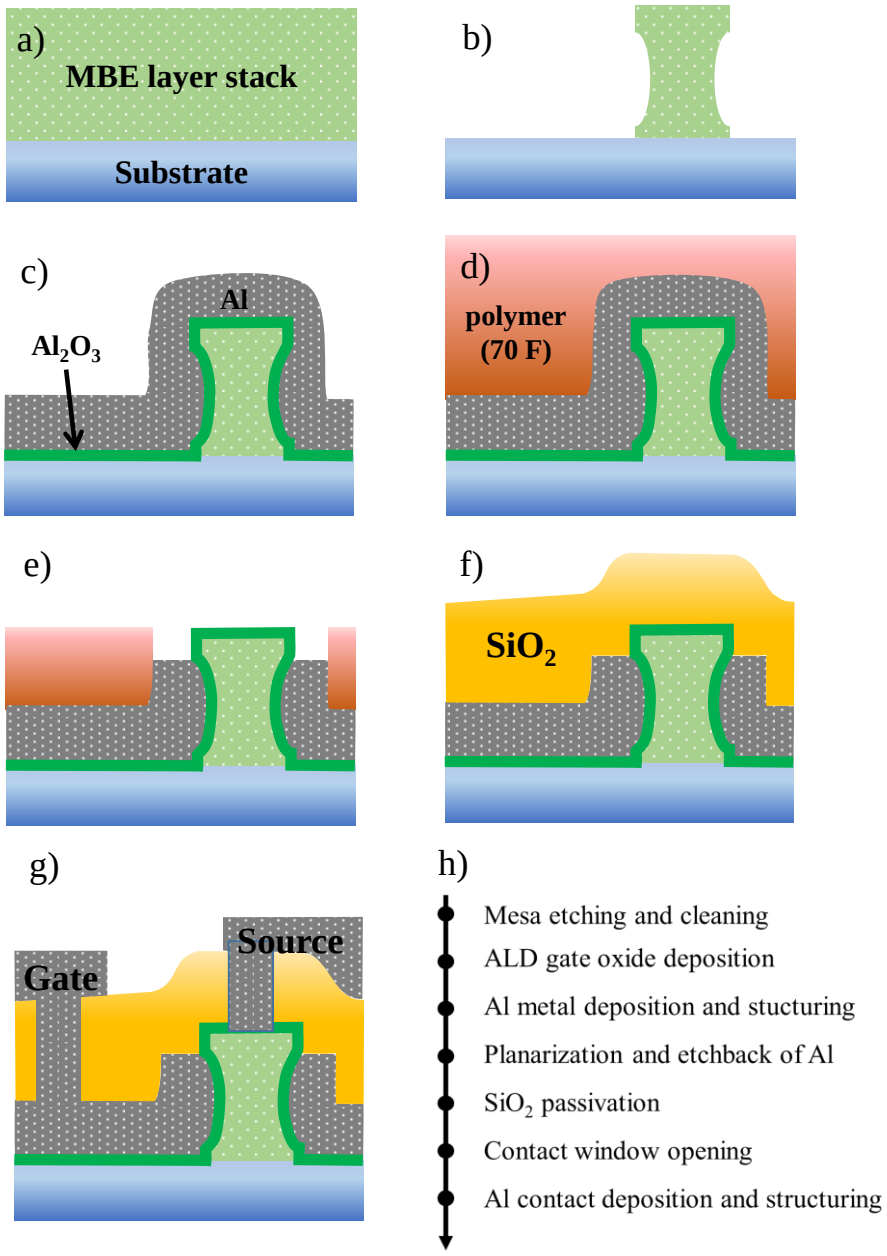

Figure 10 Schematics of the GAA TFET fabrication scheme at different stages in the fabrication process. **a)** Starting point is the grown MBE layer stack. **b)** After etching of the mesa. **c)** After gate electrode formation. **d)** Planarazation with spin-on-polymer. **e)** After etchback of Al. **f)** After SiO_2 passivation. **g)** Finalized transistor. **h)** Process flow.

2.2.1 Mesa Structuring in Gate-All-Around Fabrication Process of Germanium Based Tunneling Field Effect Transistors

The GAA process starts with photolithography and the dry anisotropic etching of the transistor mesa in an induced-coupled-plasma reactive ion etching (ICP-RIE) system. Cl_2 and HBr are used as process gases. The mesa is etched down to the buried Si contact layer. This is

confirmed through end-point detection surveillance. A consequence of dry etching Ge, and especially $Ge_{1-x}Sn_x$, is that it induces a buried layer surface roughness (see Figure 11). A peak-to-valley difference of as much as 50 nm for the buried layer surface after mesa etching, has been measured with a surface profiler. Due to the gate-substrate overlap (see Figure 10) an increased surface roughness can increase gate-oxide leakage and reduce device reliability.

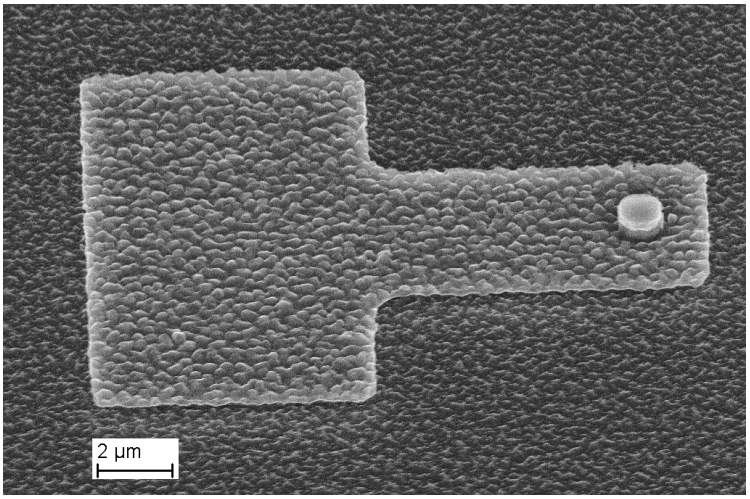

Figure 11 SEM image of a GeSn TFET after gate formation. A distinct surface roughness results from dry etching of Ge and GeSn.

Dry mesa etching is followed by resist removal and DI water diluted hydrogen peroxide (H_2O_2) solution and hydrofluoric acid cleaning steps. H_2O_2 selectively etches Ge [120], and also $Ge_{1-x}Sn_x$. After these steps the Ge and $Ge_{1-x}Sn_x$ regions of the mesa are therefore slightly under etched (See Figure 10b). Scanning electron microscopy (SEM) images presented in [77] show that the under etching is ~ 30 nm. This under etching is, however, beneficial for the later back etching of the gate Al covering the top contact. It ensures a defined gate-source overlap and makes the back etching less critical. A microscopy image of a transistor after mesa etching is shown in Figure 12a.

2.2.2 Gate Formation in Gate-All-Around Fabrication Process of Germanium Based Tunneling Field Effect Transistors

After mesa cleaning an Al_2O_3 gate oxide is deposited by remote plasma enhanced atomic layer deposition in an atomic layer deposition (ALD) system. A substrate temperature of T_{sub} = 250 °C was used. Tri-methyl-aluminum (TMA) and O_2 radicals were used as precursors. Argon (Ar) was used as purging gas. ALD is a cyclic process relying on self-terminating surface reactions. One ALD cycle consist of the following sequential steps (I-IV): (I) A self-terminating

reaction of TMA with the sample surface. (II) Purging of the chamber removing non-reacted reactants and the gaseous by-products. (III) A self-terminating reaction of the O_2-plasma with the sample surface. (IV) Purging and evacuation to bring chamber back to initial conditions. A detailed description of an ALD processes and the surface chemistry and physics involved is beyond the scope of this work, and the reader is referred to [121] for more information.

High-κ/Ge interfaces generally have a high D_{it}, which can degrade the carrier mobility and induce leakage currents. To improve the interface, an ultrathin GeO_x layer between the Ge and the Al_2O_3 was produced with a O_2-plasma post oxidation step with duration t = 5 min. Before the plasma post oxidation was performed, a thin Al_2O_3 cap layer with thickness $d_{ox} \sim 1.5$ nm was deposited. This cap layer protects the surface from plasma damages, but is thin enough to allow O_2-diffusion through it. It has been shown that the formation of a GeO_x layer through similar post-oxidation methods can reduce the D_{it} by one order of magnitude [122]. The electrical characterization of Ge/Al_2O_3 MOS capacitors using this post-plasma oxidation method is the topic of Chapter 7.

Except for the TFETs presented in Chapter 6, no forming gas annealing (FGA) was performed. FGA is effective in passivating bulk oxide traps, and can reduce oxide charge trapping and flatband voltage shift due to oxide charges [123]. Hydrogen passivation of Si dangling bonds is very effective in reducing the interface state density of Si surfaces [124]. However, FGA and passivation of Ge dangling bonds with hydrogen has been found to be ineffective [125]. For devices containing $Ge_{1-x}Sn_x$, the temperature sensitivity of the material was also a concern, and a reason why FGA was not performed in these experiments.

The permittivity ε_r of the ALD Al_2O_3 has been established through C-V measurements of planar MOS capacitances to lie in the range $\varepsilon_r \sim 6\text{-}7$. For good electrostatic control of the TFETs, which is especially important for achieving steep turn on characteristics, an aggressively scaled oxide with low equivalent oxide thickness (EOT) is preferable (see Appendix for definition). Thin Al_2O_3 thickness can easily be accomplished with the ALD system discussed here, due to the ML accuracy of the ALD technique. However, when examining Figure 10c, we see that the TFET structure has large overlap area between the gate and the buried Si substrate layer. This overlap region represents a parasitic leakage path. The reliability of the TFETs is greatly reduced by the downscaling of the oxide thickness, due to the increase in gate leakage currents and probability of oxide breakdown. The gate oxide leakage is also higher when one has a rough substrate surface. A tradeoff therefore exists between achieving a large number of working devices and good measurement statistics with thick gate

oxide, and improved device performance with thin oxides. In this work gate oxide thicknesses, d_{ox}, in the range 9 nm < d_{ox} < 12 nm was used.

Directly after gate oxide deposition, the Al gate metal is deposited by means of sputtering. A coarse gate electrode structure is defined through photolithography and etched with the same ICP-RIE system used for mesa etching. A transistor at this stage in the fabrication process is shown in Figure 12b. As seen in this figure, the top of the mesa is, at this stage in the fabrication process, still covered with gate oxide and Al. To complete structuring of the gate electrode, the Al covering the top surface of the mesa has to be removed. This is done by first planarizing the chip with a spin-on polymer (70F, Filmtronics Inc.). This is done by first spin coating the liquid polymer onto the chip, and following by hot plate baking at a temperature T_{bake} = 200 °C. The polymer layer is etched back with a RIE system using O_2 as process gas. When the Al covering the top of the mesa is exposed, the etching is stopped. The remaining polymer now serves as a mask covering most of the gate and the substrate. The uncovered Al is etched back using ICP-RIE. To remove Al residues, a wet etching (phosphoric acid etching solution) step is also performed. As the Ge and $Ge_{1-x}Sn_x$ regions of the mesa are under etched, the source overlap of the surrounding gate is defined by the position of the Ge/Si cap heterojunction. A transistor at this stage in the process can be seen in the microscopy image in Figure 12c. Due to the GAA geometry and the surrounding gate, the gate width w_G and the mesa area A of the devices are related through a power law relationship, $w_G \propto A^{1/2}$.

2.2.3 Isolation and Contacting in Gate-All-Around Fabrication Process of Germanium Based Tunneling Field Effect Transistors

The process proceeds with the deposition of SiO_2 as isolation oxide. This is performed using a plasma enhanced chemical vapor deposition system, with liquid tetraethoxysilane as a source of Si. The thickness of this oxide is d_{ox} ~ 300 nm, which ensures a good insulating layer. Contact windows are then structured with photolithography and opened using RIE with fluroform (CHF_3) as a process gas. The CHF_3 etching of Al_2O_3 has a low etch rate. The gate oxide covering the top and buried contacts therefore serves as a etch stop. The gate oxide is removed by a buffered hydrofluoric acid (BHF) etching step with duration t = 30 - 60 s, before mask removal (see Figure 12d). As Si oxidizes under ambient conditions, an additional short BHF-dip (t < 5 s) is performed after mask removal and cleaning, and right before Al sputtering for contact metallization. Contact structuring, and ICP-RIE etching finishes the GAA fabrication process. A finished transistor is seen in Figure 12e.

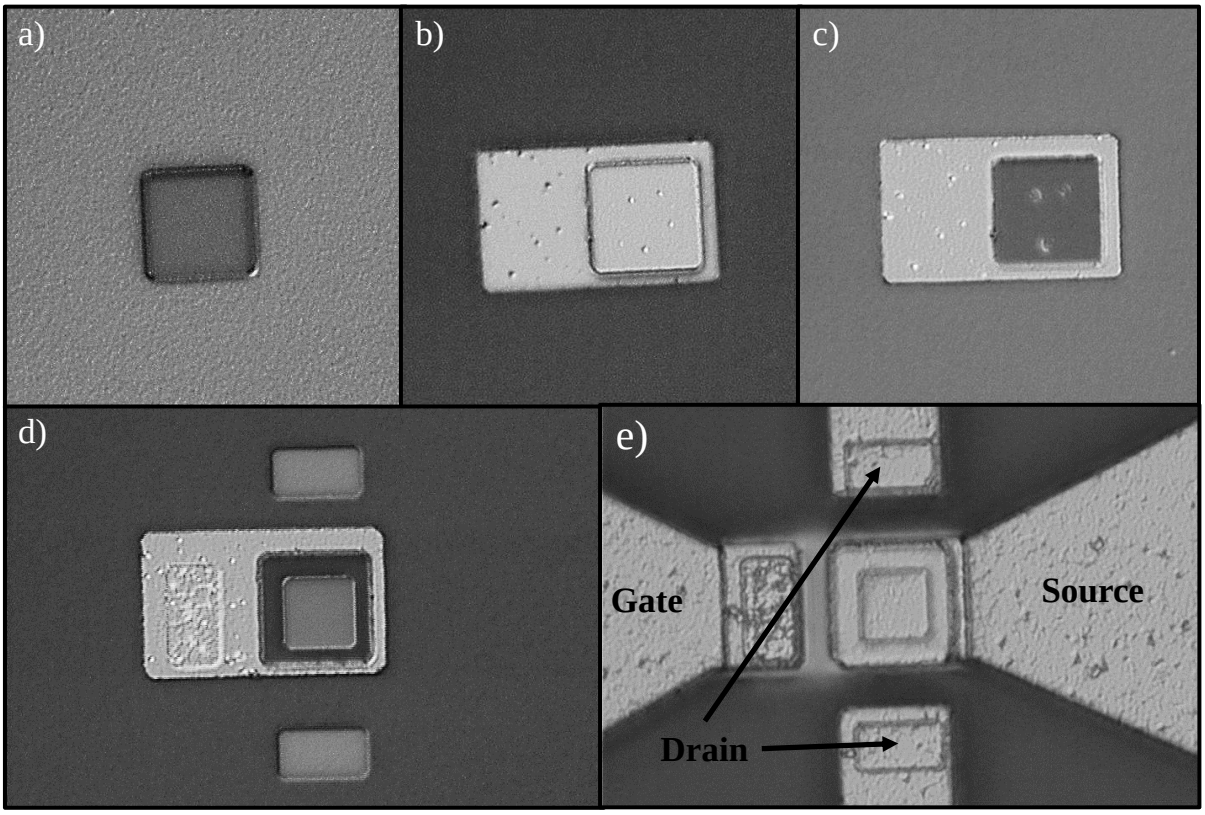

Figure 12 Top view microscopy images of a vertical Ge TFET with 10x10 μm^2 mesa area at different stages in the GAA fabrication process. **a)** After mesa etching. A somewhat rough buried layer surface can be seen as a result of HBr-etching of Ge. **b)** After photolithography structuring of gate electrode. **c)** After planarization and removal of Al from top contact. Al residues can be seen on the mesa surface. **d)** After contact window opening. The Al gate metal can be seen to be slightly etched due to the BHF-dip. **e)** A transistor after fabrication is finished. The three contact terminals are indicated.

2.3 Data Acquisition and Processing

I-V measurements presented in this work were obtained with a Keithley 4200 Semiconductor Characterization System. Two source-measuring units and a ground unit were used for the three terminals of the measured devices. The source (top) contact was kept at ground potential. Temperature measurements were performed by cooling down the measurement chuck with a compressor from Trio-Tech using a perfluoro compound (fc77) as a cooling liquid. With this system, measurement temperatures in the range from room temperature (RT) to T = 240 K could be investigated. The temperature was measured with a thermocouple attached to the sample.

Both I_{DS} versus $V_{G,}$ transfer characteristics, and I_{DS} versus $V_{DS,}$ output characteristics, were obtained. Initial measurement procedures involved measuring I_G for randomly selected devices to establish the leakage current through the gate oxide (see example in Figure 13a). The gate oxide leakage is, due to the vertical GAA TFET structure used in this work, determined by the

gate-to-substrate leakage current. It is therefore independent of mesa area and comparable for all sized transistors. The low I_G currents demand long integration time. To be able to efficiently measure a large set of transistors and reduce oxide charge trapping effects, I_G was not measured for each single transistor. From the initial I_G measurements the onset of the Fowler-Nordheim tunneling (FNT) [126] regime can be established. FNT currents are known for increasing exponentially with voltage bias. If a transistor is driven into the FNT regime, the oxide is more likely to be damaged and the reliability of the device is reduced. The gate voltage sweep range was therefore determined by the onset of FNT.

To efficiently handle large data sets, MATLAB software [127] was used for the data processing. A script was developed for parameter extraction and to perform arithmetic operations. A Savitzky-Golay filtering [128] was implemented in the script and used to smooth the characteristics. Especially for low currents (< 10 pA) signal noise could be pronounced. An example of a filtered curve is given in Figure 13b. The degree of smoothing was, however, kept at a minimum in order not to manipulate the measured characteristics.

Important for the discussion and comparison of different transistors presented in this work, is obtaining values for I_{ON}, I_{OFF} and SS. I_{ON} was extracted after choosing a fixed on-gate bias. For this gate bias the drain current should be high, and vary little with a change in gate bias.

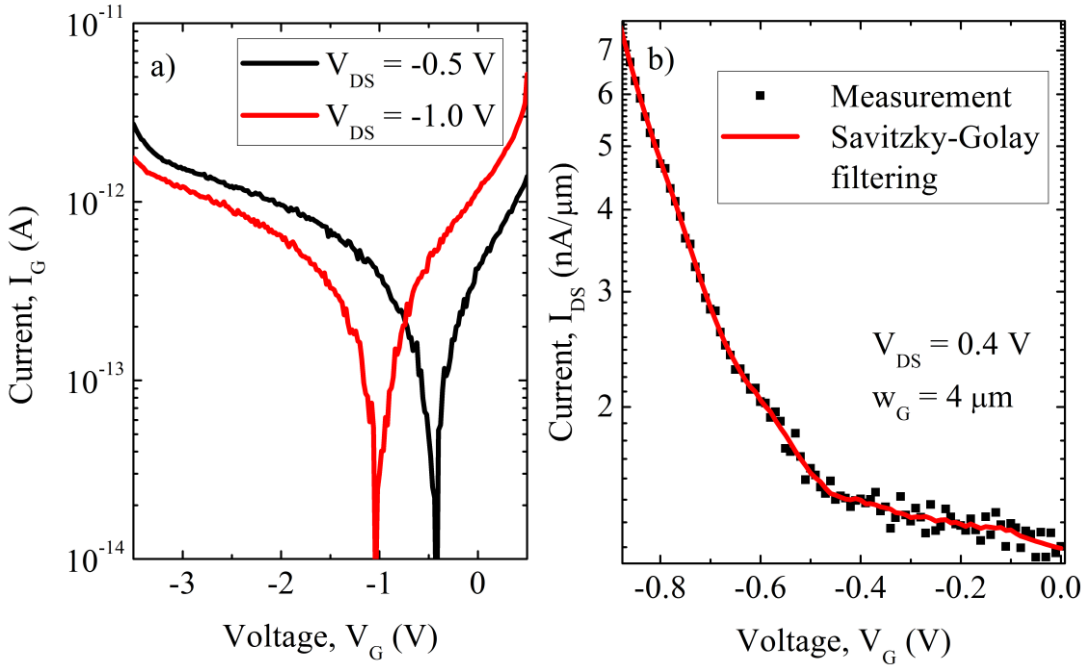

Figure 13 a) The gate oxide leakage is due gate-to-substrate leakage. As the buried substrate layer serves as drain contact the I_G curve minimum corresponds to the applied drain-source bias. Transistor shown is from sample A in Chapter 4. b) Savitzky-Goly filtering was sometimes used to smoothen the acquired data, as low current regions exhibited noisy signal.

Ideally, a transistor should have only one supply voltage in addition to the ground potential. We then should have $V_G = V_{DS}$ in the on-state. However, as a result of the inability to scale the oxide thickness of the devices, due to device reliability issues discussed earlier, larger gate biases were needed to drive the transistors into the on-state. The on-gate bias was therefore chosen based on the initial gate oxide leakage measurement and the FNT-onset voltage. Due to difference in oxide thickness, the on-gate bias can be seen to vary between the different experiments.

The leakage current, I_{OFF}, is defined as the drain current at $V_G = 0$ V. Due to ambipolarity and flatband shifts, however, this is not necessarily equal to the minimum drain current exhibited in the transfer characteristics. For devices with pronounced shifts, the minimum leakage current with floating gate bias, I_{min}, will also be referred to when discussing the leakage current.

The SS of a TFET is not linear with respect to the gate voltage like the MOSFET. Different methods have been proposed to define the SS for TFETs [50]. The most common way, and the one used in largest part of this work, is to give the tangential inverse slope of the $\log(I_{DS})$-V_G characteristics at the steepest point. This is easily obtained through simple derivation.

Final plotting of graphs was performed using ORIGIN software [129].

Chapter 3 Germanium-Tin P-Channel Tunneling Field Effect Transistors: the Effect of Tin-Content in Germanium-Tin Channel

3.1 Introduction

The ITRS requirements for I_{ON} [59] has proven to be a major challenge for group-IV TFETs. High I_{ON} is important to achieve high switching speeds in terms of RC time. After the demonstration of the first Si TFET [37] a number of material and geometry modifications have been proposed to boost I_{ON} in group-IV TFETs. The lower-bandgap material Ge has been implemented to raise I_{ON} in $Si_{1-y}Ge_y$ alloys [130] or bulk Ge[66] TFETs, and device geometry modifications have been implented to align the tunneling with the gate field in Si [9] and $Si_{1-y}Ge_y$ [84] TFETs. Those devices have been shown to achieve higher I_{ON} than all-Si TFETs, but still fail to achieve the ITRS requirement. As a measure to further boost I_{ON}, $Ge_{1-x}Sn_x$ [87, 77] has recently been introduced in parts of the channel region of Ge TFETs. In addition to being a Si-compatible alloy, $Ge_{1-x}Sn_x$ has an even smaller bandgap than Ge. Relaxed $Ge_{1-x}Sn_x$ has experimentally been shown to become a direct bandgap material for x ~ 9 %, exhibiting direct bandgap lasing [113]. Direct tunneling, without the need of phonon assistance, could further increase the tunneling probability, and hence I_{ON}. Epitaxial growth of high quality $Ge_{1-x}Sn_x$ however poses many challenges. Due to the large lattice mismatch of 14.7 % between α-Sn and Ge and the low solid solubility of 1 % of Sn in Ge, experimental effort is currently directed towards the epitaxial growth of $Ge_{1-x}Sn_x$ [108, 109, 110]. Epitaxial growth of $Ge_{1-x}Sn_x$ is however practiced by only a handful of scientific groups. The experimental work on $Ge_{1-x}Sn_x$ devices are therefore still limited, and more studies are called for. While a small bandgap material raises I_{ON}, I_{OFF} and SS are inevitably also affected. Device I_{OFF} and SS are in particular influenced by crystalline quality and interface defects due to TAT and SRH currents [131, 132].

In this chapter the fabrication and electrical characterization of $Ge_{1-x}Sn_x$ p-channel TFETs are presented. The aim of the work is to assess the potential of $Ge_{1-x}Sn_x$ as a channel material in vertical p-channel TFETs with respect to I_{ON} and I_{OFF}. Through a sample series comprising

three samples the effect of increasing Sn-content (x = 0 %, 2 % and 4 %) in a $Ge_{1-x}Sn_x$ channel of a Ge TFETs is investigated. The effect of the Sn-content on the electrical characteristics of the transistors is reported. The device area and temperature dependence on the electrical characterization of the TFETs are also studied.

3.2 Layer Growth and Device Fabrication

The semiconductor layer structure was grown by MBE. All three samples were grown on p-doped (10-20 Ω·cm) Si <100> wafers and contain a 100 nm Ge VS. The MBE layer sequence of the three samples is found in Table 3. More general information of MBE growth of $Ge_{1-x}Sn_x$ and Ge on Si was given in section 2.1 and will not be repeated here. The samples vary by having different Sn-content x in the intrinsic channel region, with x = 0 %, x = 2 % and x = 4 %, respectively. The critical thickness for the $Ge_{1-x}Sn_x$ layer with the Sn-content examined here, has been reported [112] to be less than the device channel thickness, $d_{channel}$ = 200 nm. It is therefore expect that the $Ge_{1-x}Sn_x$ channels are pseudomorphically biaxially strained on the underlying Ge. The drain region was grown with a B doping gradient dropping from initially $N_A = 1 \cdot 10^{20}$ cm^{-3} until saturating at a final doping concentration of $N_A = 1 \cdot 10^{18}$ cm^{-3} at the drain-channel interface. An asymmetric doping profile ($N_D > N_A$) is necessary to suppress ambipolar leakage of the TFET [60]. The growth of Ge and $Ge_{1-x}Sn_x$ in the channel and Sb-doped Ge in the source was performed at low temperature (T_{sub} = 160 °C) to suppress surface segregation. A heavily Sb-doped Si cap layer was grown as a final layer to ensure an ohmic top contact.

Table 3 MBE layer sequence for the $Ge_{1-x}Sn_x$ p-channel TFETs.

Layer	Material	Sample A Thickness (nm)	Sample B Thickness (nm)	Sample C Thickness (nm)	Doping (cm^{-3})	Growth Temperature (°C)
Source	Si	100			$N_D = 1 \cdot 10^{20}$	330
Source	Ge	200			$N_D = 1 \cdot 10^{20}$	160
Channel	Ge	200	-	-		160
Channel	$Ge_{0.98}Sn_{0.02}$	-	200	-		160
Channel	$Ge_{0.968}Sn_{0.04}$	-	-	200		160
Drain	Ge	200			$N_A = 1 \cdot 10^{18}$ ↑ $N_A = 1 \cdot 10^{20}$	330
Drain	Ge (VS)	100			$N_A = 1 \cdot 10^{20}$	330
Drain	Si	400			$N_A = 1 \cdot 10^{20}$	650

Figure 14a shows the secondary ion mass spectrometry (SIMS) measurement of the matrix elements Si, Ge and Sn from sample C. The measured intensity corresponds to the isotopes indicated in the legend. These were not pre-calibrated, and can therefore not be used to assess the Sn-content of the $Ge_{1-x}Sn_x$ layer. The measured layer thicknesses is in good agreement with the target values given in Table 3. Due to the high temperature annealing step performed during the Ge VS formation, Si/Ge intermixing can be seen at the Si/Ge interface at an etching depth d_{etch} ~ 800 nm. Figure 14b shows the doping concentration of the sample from the same SIMS measurement. Except for the B doping in the Si buried layer ($N_A \sim 2 \cdot 10^{20}$ cm^{-3}), the doping concentrations are in good agreement with the target values. The Si buried layer doping concentration, however, has little influence on the device characteristics, as it only serves as a contact layer. A high Sb doping concentration is measured in the $Ge_{1-x}Sn_x$ layer. As the Sb-effusion cell was closed during the growth of this region, it cannot contain intentional Sb dopants. This measurement signal must hence be due to Sn/Sb mass interference. In the figure, peaks can also be seen in the measurement signal at transition regions. These are believed to be measuring artefacts, which are due to intermixing effects with varying ion- and sputtering outputs at interfaces [133].

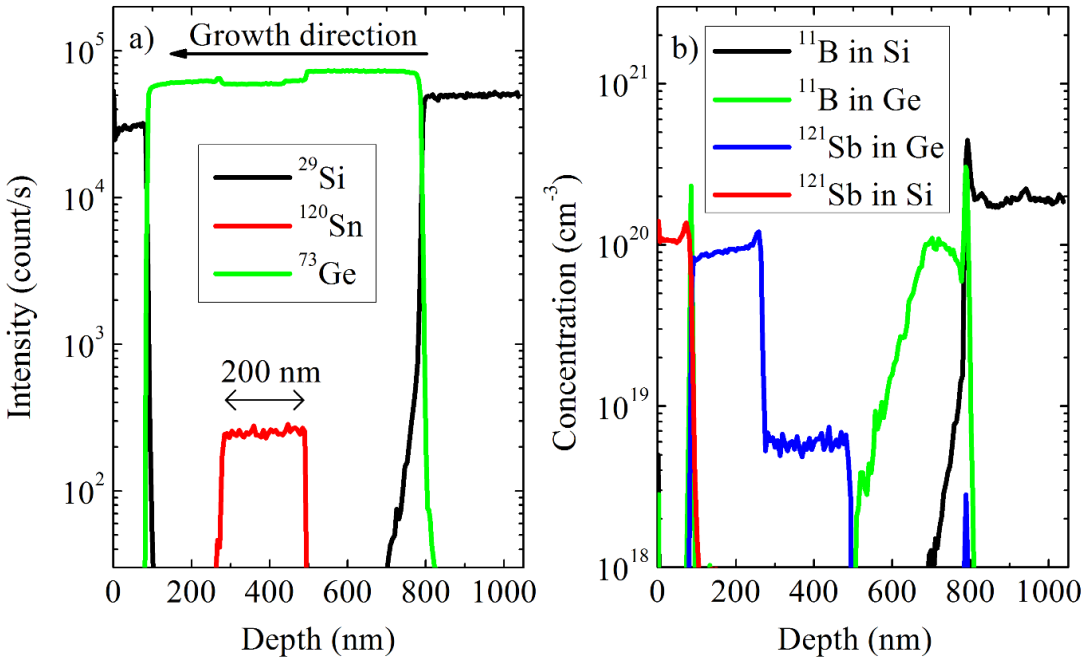

Figure 14 a) SIMS profile of the grown matrix elements Si, Ge and Sn for sample C. b) Doping profiles obtained through the SIMS measurement from sample C. Sb signal in the GeSn layer is due to mass interference between Sb and Sn. The isotopes used for the different elements are indicated in the legend. SIMS measurements were conducted by Florian Bärwolf at Innovation of High Performance Microelectronics (IHP) Frankfurt (Oder).

After MBE growth the vertical TFETs were fabricated using the GAA process described in section 2.2. A O_2-plasma post oxidation step with duration t = 5 min was performed and a total of 70 ALD cycles were conducted. A physical oxide thickness of d_{ox} ~ 11.5 nm of the particular Al_2O_3/GeO_x gate oxide was measured by ellipsometery. Based on a Si MOS capacitor reference sample, a corresponding EOT of ~ 7 nm of the gate oxide is expected. The relatively thick gate oxide was chosen to prevent leakage current between the gate and the substrate.

3.3 Results and Discussion

Transfer and output characteristics of the three samples are shown in Figure 15a and 15b, respectively. A 650 mV/dec slope is drawn in the transfer characteristics to indicate the steepness of the devices. The TFETs I-V characteristics can be considered composed of the leakage current I_{OFF}, and the gate controlled BTBT-current I_{ON}. The turn-on steepness can be quantified by the subthreshold swing, SS. The effect of Sn-content in the $Ge_{1-x}Sn_x$ channel on these three parameters will now be consider in turn.

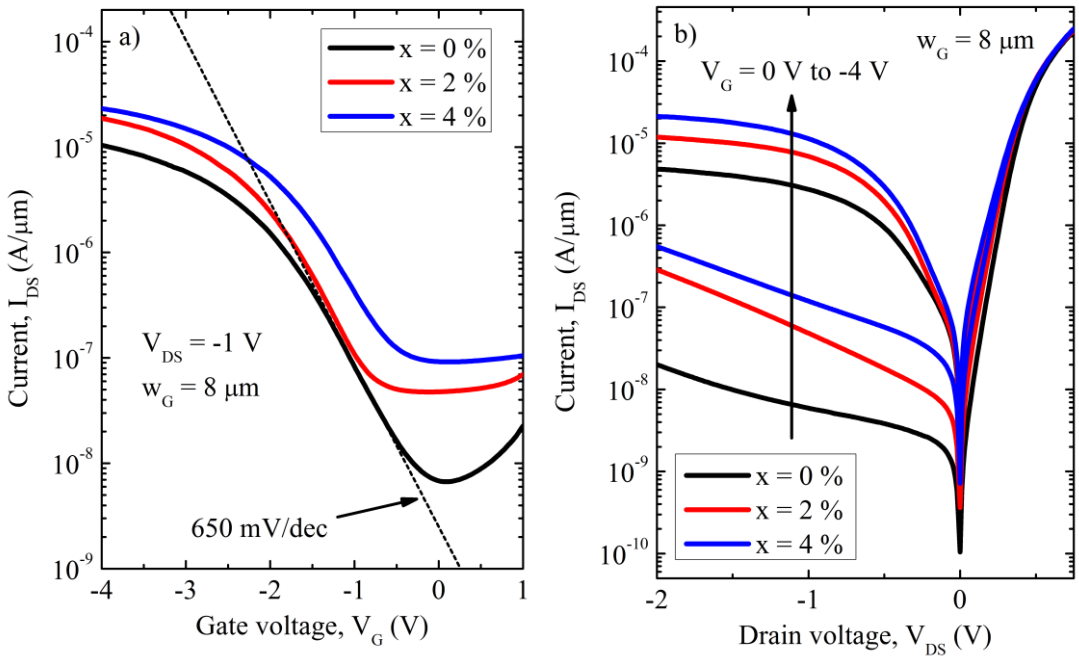

Figure 15 a) Transfer and **b)** output characteristics of $Ge_{1-x}Sn_x$ channel TFETs with x = 0 %, 2 % and 4 %. Increase in I_{ON} as well as I_{OFF} can be seen to result from increasing Sn-content in the channel.

3.3.1 Influence of Tin-Content in Channel on Leakage Current in Germanium-Tin Tunneling Field Effect Transistors

The influence of Sn-content in the $Ge_{1-x}Sn_x$ channel on the leakage current is examined by assuming that the drain current, $I_{DS,}$ for gate voltage $V_G = 0$ V can be expressed as [47]:

$$I_{DS}(V_{DS}, V_G = 0\ V) = J_A(V_{DS})\cdot A + J_P(V_{DS})\cdot P + I_G. \quad (23)$$

Here A is the device area, P is the device perimeter, J_A is the area current density and J_P is the perimeter current density. I_G is the leakage current through the gate oxide. The relative thick gate oxide of the devices, resulted in a very low I_G current ($I_G << 1$ pA for $V_G = 0$). For the following discussion I_G is therefore set equal to zero, as it is negligible compared with the other components. For the here reported vertical TFETs the perimeter equals the gate width w_G, $P = w_G$. When defining the leakage current as $I_{OFF} = I_{DS}(V_G = 0)/w_g$, we can see from (23) that I_{OFF} becomes a linear function of the area to perimeter ratio A/w_G when the V_{DS} bias is fixed. In Figure 16a, I_{OFF} for V_{DS} = - 1.0 V is plotted as a function of $A/w_{G,}$ after considering a large set of transistors with ratios varying between $A/w_G = 0.25$ and $A/w_G = 2.5$ µm. The straight line fit validates the assumption of (23), and J_A and J_P can be extracted from the slope and intercept, respectively. Following this approach, straight line fits were performed for all $I_{DS}(V_{DS})$-values obtained through the output characteristics of the samples. The resulting mapping of J_A and J_P, as a function of V_{DS} is shown in Figure 16b and Figure 16c, respectively.

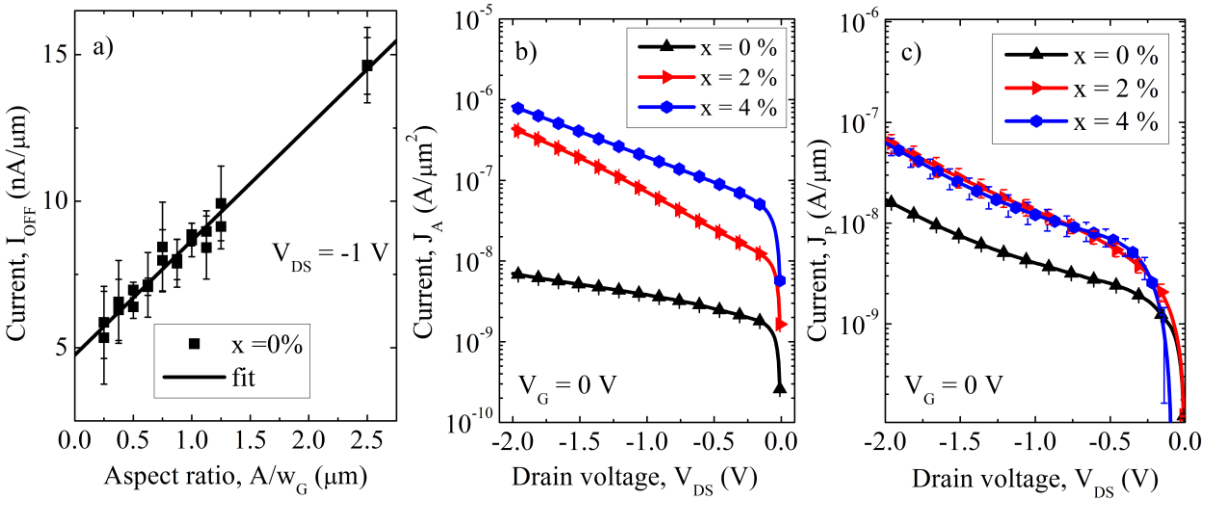

Figure 16 a) I_{OFF} for the Ge reference plotted as a function of A/w_G for V_{DS} = -1.0 V. J_A and J_P can be determined from the slope and intersect of the fitted line, respectively. **b)** The area current density component J_A of I_{OFF}. **c)** the perimeter current density component J_P of I_{OFF}. Increasing the Sn-content in the channel leads to a strong successive increase of J_A, whereas only a slight constant increase of J_P.

J_A addresses the epitaxial quality of the MBE grown diode structure. It can be seen in Figure 16b that increasing the Sn-content in the $Ge_{1-x}Sn_x$ channel leads to a strong successive increase in J_A as well as a more pronounced V_{DS} dependence. An increase in J_A is expected for $Ge_{1-x}Sn_x$ compared to Ge, due to the lowering of the bandgap. A bandgap lowering exponentially affects the intrinsic carrier concentration, and hence the diffusion current [31]. The magnitude of the increase and the strong V_{DS} dependence of these sample, however, indicates that this is not a result of bandgap lowering alone. Point defects associated with the growth of $Ge_{1-x}Sn_x$ on Ge at low temperature [108] degrade the epitaxial quality. With a high trap density both SRH generation- and TAT currents will increase. As already introduced (see (18) in section 1.4.5.2), SRH generation current can be expressed by:

$$J_{ge} \approx q \cdot U_{SRH} \cdot W_D, \tag{24}$$

where U_{SRH} is the SRH generation rate, which depends on the intrinsic carrier concentration and the generation lifetime. From (24) it is clear that J_{ge} is a linear function of the depletion width, W_D. In models including TAT contribution, U_{SRH} in (24) is replaced by U_{trap}:

$$U_{trap} = (1+\Gamma) \cdot U_{SRH}, \tag{25}$$

which includes an electric field-enhancement factor Γ (see also (21) and (22) in section 1.4.5.3). Although originally developed for Si devices, experimental results of Ge p^+n-junctions have shown to be well described by this model [134]. Now, a fair approximation of W_D for a pin diode with i-region thickness $d_{channel}$, can be found by solving the Poisson equation using the depletion approximation [31]:

$$W_D = \sqrt{d_{channel}^2 + \frac{2 \cdot \varepsilon_s}{q} \cdot \left(\frac{N_A + N_D}{N_A \cdot N_D}\right) \cdot (V_{bi} - V_{DS})}. \tag{26}$$

Here the permittivity ε_s and the built in potential V_{bi} depend on the material properties. In Figure 17, J_A is shown as a function of W_D, which was calculated using (26). Due to the modest Sn-concentration, Ge parameters were used to calculate W_D for all samples. Although this approximation will contain some error, a qualitative comparison can in either way be based on the J_A-$\sqrt{V_{DS}}$ relationship. For the Ge reference sample a linear J_A-W_D relationship is seen, consistent with (24). Based on this, SRH is assumed to be the leakage mechanism determining J_A for the Ge-reference sample. The samples with $Ge_{1-x}Sn_x$ in the channel however exhibit a

superlinear J_A-W_D relationship. This shows how TAT influences the device characteristics when crystal quality is degraded, and the field enhancement factor in (25) becomes significant.

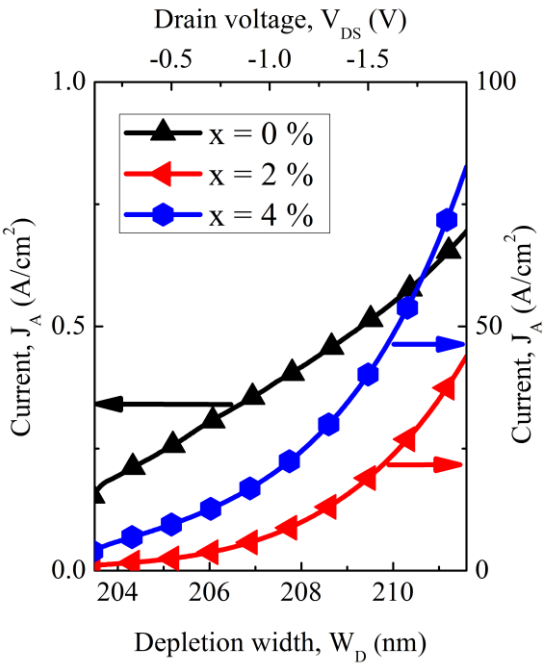

Figure 17 J_A as a function of W_D. The Ge reference shows a linear J_A-W_D relationship, while the $Ge_{1-x}Sn_x$ samples with x = 0 % and x = 4 %, show a super-linear behavior due to the modification of the SRH generation rate by the electric field-enhancement factor.

The most straight forward strategy to reduce the J_A component of I_{OFF} is through device dimension scaling of the body thickness. For a vertical structure as presented here, the body thickness is independent of the epitaxial layer thickness. Extrapolating J_A yields that a device mesa diameter D for the Ge reference sample of D ~ 17 nm for V_{DS} = -0.5 V and D ~ 10 nm for V_{DS} = -1.0 V, respectively, is necessary to reach the ITRS low power requirements for leakage current, I_{ITRS} = 10 pA/µm. These dimensions are in the same scale as the ITRS recommended multi-gate MOSFET body thickness [59], and also predicted required body thickness for achieving sub-60 mV/dec SS in TFETs using Ge [135]. For the samples containing GeSn the prospects are worse, with a required D < 2 nm for V_{DS} = -0.5 V. From these estimates it becomes clear that the the amount of GeSn in the channel has to be reduced to achieve manageable I_{OFF} for even modest Sn-contents. The desired effect of implementing a low-bandgap material, is to increase the BTBT in the on-state. This mainly takes place at the channel-source interface. If the GeSn region of the channel is confined within a thin layer, it can be positioned at this interface for more optimal use. This aspect is also considered in Chapter 4. It is also reason to believe that the crystalline quality of GeSn will improve as

progress in epitaxial growth techniques is made. Epitaxial growth of GeSn is still in an early stage and has by far not reached the same level of maturity as for example SiGe or other III-V compound semiconductors.

J_P is another concern, as it represents the minimum I_{OFF} achievable by device dimension scaling. In Figure 18 I_{OFF}, together with fits of (23), are displayed as a function of device area. As the device area is reduced, I_{OFF} will saturate towards J_P. For the TFETs with a GeSn channel, I_{OFF} is mainly dominated by J_A for device area range investigated. The fit of (23) therefore results in a linear behavior in the log-log plot for the TFETs with x = 2 % and x = 4 %. For the Ge TFET on the other hand, I_{OFF} is already close to J_P for the smallest size of the transistor. The same will be the case also for the GeSn channel devices with continued scaling. For the GeSn TFETs a reduction of almost three orders of magnitude in J_P is necessary to meet the 10 pA/µm ITRS low power requirement for I_{OFF}. It is hence necessary to reduce the D_{it} at the $Ge_{1-x}Sn_x$-oxide interface, which causes SRH and TAT surface leakage currents. In the figure we can see that J_P is increased by the incorporation of GeSn with a factor of ~ 2.3. This increase is believed to be due to increased interface state density for the GeSn surface. The increase could also result from the bandgap reduction. However, as no increase in J_P-currents between the 2 % and 4 %-Sn content samples can be seen, the addition of interface states when moving from a Ge- to a GeSn-system seems more likely. The reported D_{it} for GeSn-oxide interfaces is $2 \cdot 10^{12}$ - $6 \cdot 10^{13}$

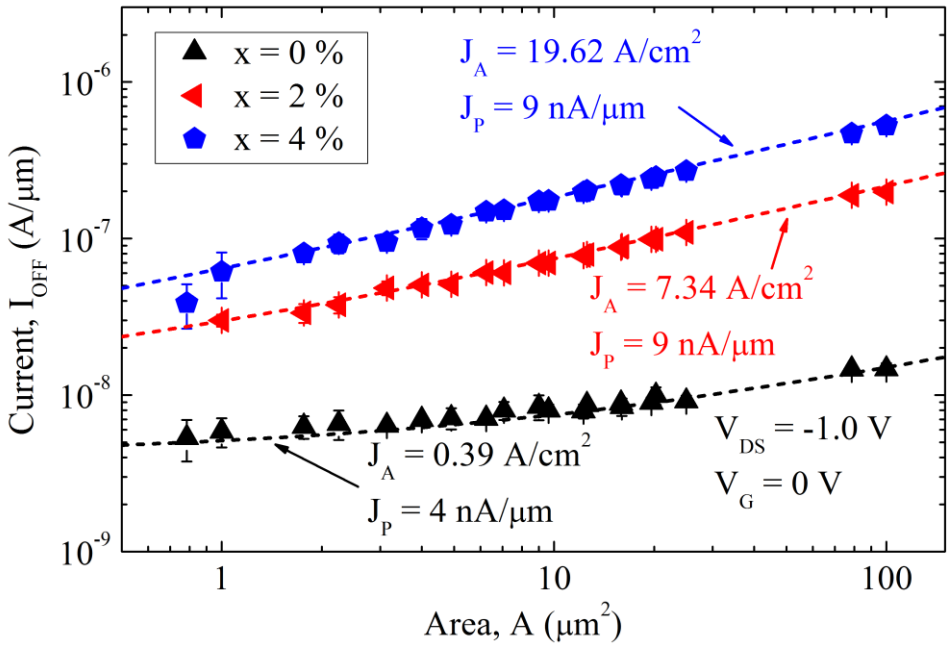

Figure 18 I_{OFF} as a function of device area. Dashed lines show the fit of (23) to the experimental data. The corresponding fit values of J_A and J_P are indicated. When scaling down the device size, the current becomes limited by J_P. Scaling is mostly effective to improve device performance when I_{OFF} is dominated by J_A.

$cm^{-2}eV^{-1}$[90, 136, 137]. To reduce SRH and TAT at the Ge-Oxide interface, a better passivation of the Ge- and GeSn-oxide interface is necessary. Current experimental work on S-passivation of the Ge and GeSn surfaces is under investigation by our group and is, like reported also elsewhere[90, 91], showing promising results. Experimental results of S-passivated $Ge/Al_2O_3/Al$ MOS capacitors are presented in Chapter 8.

It is not expect that as much as a three order of magnitude reduction in D_{it} is necessary to achieve the required J_P current. The devices presented here have a very large gate-drain overlap. GIDL [57] together with gate induced tunneling at the drain-channel interface are therefore also contributing to the high J_P currents. An increase of I_{DS} for positive V_G, *ambipolar leakage*, can clearly be seen in the transfer characteristics in Figure 15a. A reduction of gate induced leakage currents could be solved technologically by introducing a spacer [138], separating the buried layer and the gate electrode after mesa etching. This would effectively reduce the gate-drain overlap and provide a better aligned gate electrode. A spacer would also enable the use of thinner gate oxides, as the leakage path between the substrate and gate is blocked. This is important for achieving low SSes. The thickness of the spacer must however be very precise. It must align with the channel region, and deposited in a way that there is no sidewall coverage reducing the electrostatic control of the gate. How this spacer technology can be achieved has yet to be solved and is mentioned here as a suggestion for further research.

The transport mechanism determining I_{OFF} was investigated further by varying the measurement temperature T = RT to T = 240 K. In Figure 19a the temperature dependence of the transfer characteristics for a $Ge_{1-x}Sn_x$ channel TFET with x = 2 % Sn is shown. As expected, I_{DS} for high negative V_G bias shows a weak temperature dependence, consistent with a BTBT process. A stronger temperature dependence can be seen for the leakage floor and the subthreshold region. Figure 19**b** show the Arrhenius plots of I_{OFF} where the activation energies corresponding to the fitted lines are indicated. In Figure 19c extracted activation energies are plotted as a function of V_G. The activation energy for I_{OFF} of the Ge reference, E_A = 0.30 eV, and the maximum energy found at V_G = -0.5 V, E_A = 0.35, is close to half the bandgap of Ge (E_{mid} ~ 0.33-0.34 eV in the temperature range investigated [139]). This combined with the discussed J_P dependence of this sample indicates that the SRH leakage mechanism involving mid gap traps located at the surface are dominating the leakage currents of the devices. The sample with GeSn in the channel show a weaker temperature dependence for I_{OFF}, with E_A = 0.18 eV for x = 2 % and E_A = 0.19 eV for x = 4 %, respectively. As I_{OFF} was roughly equal to J_A

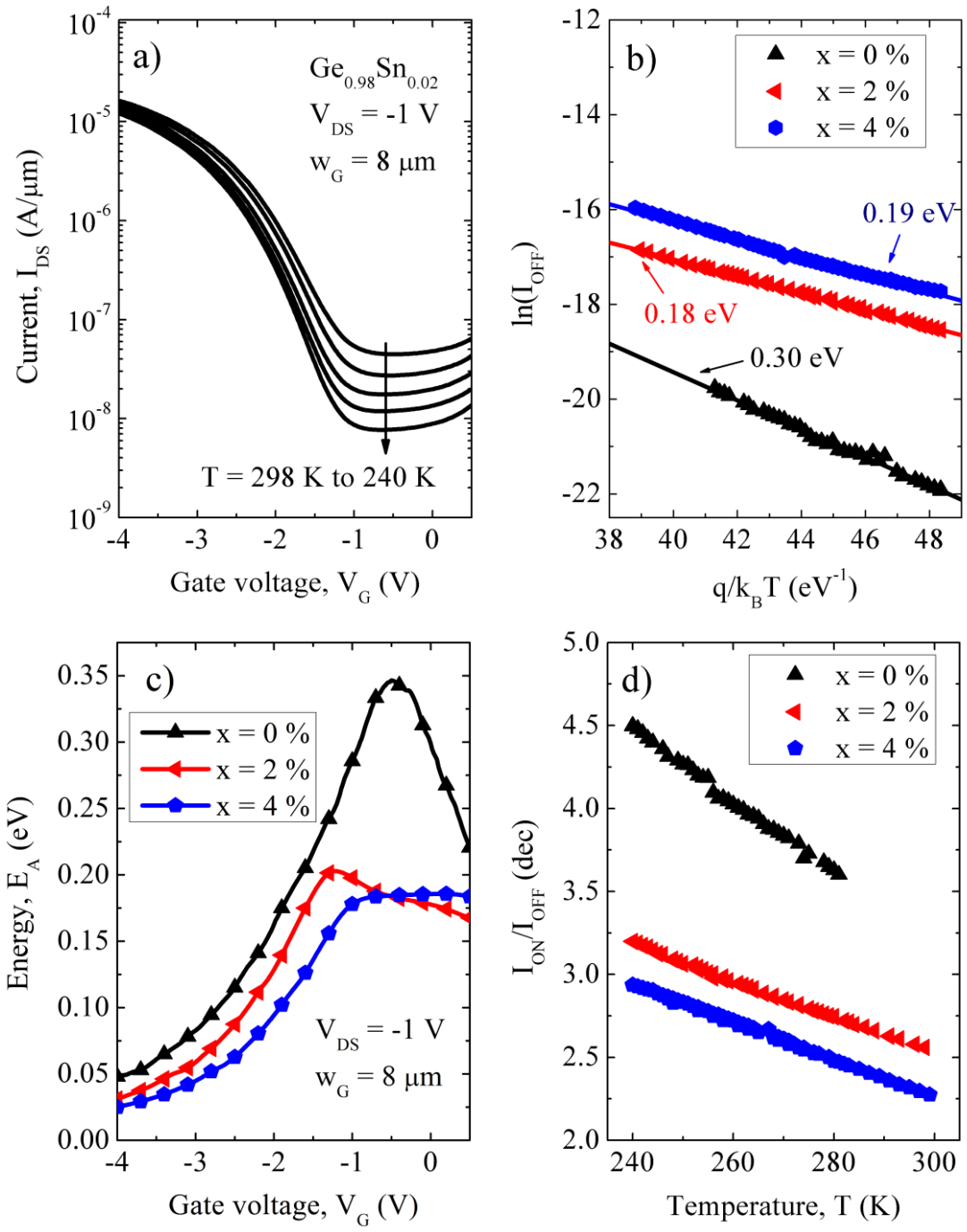

Figure 19 a) Transfer characteristics of a $Ge_{0.98}Sn_{0.02}$-channel TFET measured at different temperatures. **b)** Arrhenius plot of I_{OFF} for all three samples. Activation energies are indicated. **c)** Activation energies as a function of V_G. **d)** I_{ON}/I_{OFF} ratio as a function of temperature.

for these samples, these activation energy can be expected to relate to the bulk properties of $Ge_{1-x}Sn_x$. The activation energies are lower than half of the calculated bandgaps of $Ge_{1-x}Sn_x$ for x = 2 % and x = 4 % reported in [140]. However from the non-linear J_A-W_D relationship seen in Figure 17, a TAT contribution has already been established for these devices. The temperature dependence of the field enhancement factor Γ must therefore be accounted for. Due

to the second term of the integrand in (22) (see section 1.4.5.3), Γ, and hence the measured I_{OFF} for the two samples, have lower activation energies than the midgap values.

3.3.2 Influence of Tin-Content in Channel on Subthreshold Swing of Germanium-Tin Tunneling Field Effect Transistors

The SS, which here is defined at the steepest point in the transfer characteristics, will in the following section be analyzed. The devices all exhibit high SSes, SS ~ 550-1000 mV/dec, compared to the 60 mV/dec MOSFET limit. They are considerable higher than the lowest SS obtained in TFETs so far [23]. This can in part be explained by the thick gate oxide, EOT ~ 7 nm, necessary to eliminate I_G in (23). A thick oxide reduces the MOS capacitance and weakens the electrostatic field control of the gate. As reference, the current ITRS requirement is EOT ~ 0.7 nm [59]. A high I_{OFF} also limits the visibility of a steeper SS at low gate voltages. An example of this can be seen in Figure 20a, which shows the SS as a function of device area. For the $Ge_{1-x}Sn_x$ –TFETs with x = 2 % and x = 4 %, SS is reduced when the device mesa area is reduced. This is because I_{OFF} is dominated by J_A, for these devices. The SS of the Ge-TFET is largely unaffected by an area reduction, as I_{OFF} is dominated by J_P. Interesting is that, although exhibiting a relatively high I_{OFF}, the smallest sized $Ge_{1-x}Sn_x$ TFETs with x = 2 % and x = 4 % demonstrate roughly the same SSes as the Ge-TFET. Subtracting the J_A component of I_{OFF} from I_{DS}, the degradation of the SS due to bulk traps can be removed. Technologically, this represents further device dimension downscaling. When performing this subtraction, the GeSn TFETs are seen to hold steeper SS at RT than the Ge TFET:
SS_{sub} (x = 0 %, V_{DS} = -1 V) = 624 ± 43 mV/dec,
SS_{sub} (x = 2 %, V_{DS} = -1 V) = 505 ± 20 mV/dec and SS_{sub} (4 % Sn, V_{DS} = -1 V) = 494 ± 25 mV/dec. These result also indicate that the SS decreases with increasing Sn-content. This improvement of SS can be explained by that the tunneling probability is increased with increasing Sn-content. The SS becomes less dependent on the tunneling probability, when the tunneling probability is increased [53]. There are two reasons for why the tunneling probability is increased when the Sn-content is increased. One is the bandgap reduction, which effectively reduces both barrier height and width. The other is the contribution of direct tunneling, which is increased when the direct conduction band edge is lowered compared to the indirect conduction band edge. The decrease of SS with increasing Sn-content has also been shown in the simulation studies of Yang et al.[87].

In Figure 19c a thermal subthreshold region current could be seen, with a slow exponential decrease of activation energy for increasing negative V_G. The origin of this current is assumed

to be TAT involving phonon scattering processes. These types of processes naturally degrades the SS as they are temperature dependent. The temperature dependence reduces the energy filtering mechanism, i.e. crossing and uncrossing of the energy bands, which is a precondition for achieving steep SSes in TFETs. The combination of reducing I_{OFF} and quenching the phonon scattering processes through reducing the temperature, leads to a considerable improvement of SS. This can be seen in Figure 20b, which shows SS as a function of temperature. An almost linear relationship with a steep 3 mV/dec K^{-1} slope between SS and temperature can be seen in the temperature range investigated. This makes it evident how strongly TAT and SRH affects the steepness of the devices. Like for I_{OFF}, the SSes for the TFETs with x = 2 % and x = 4 % have a weaker temperature dependence than the SS of the Ge TFET.

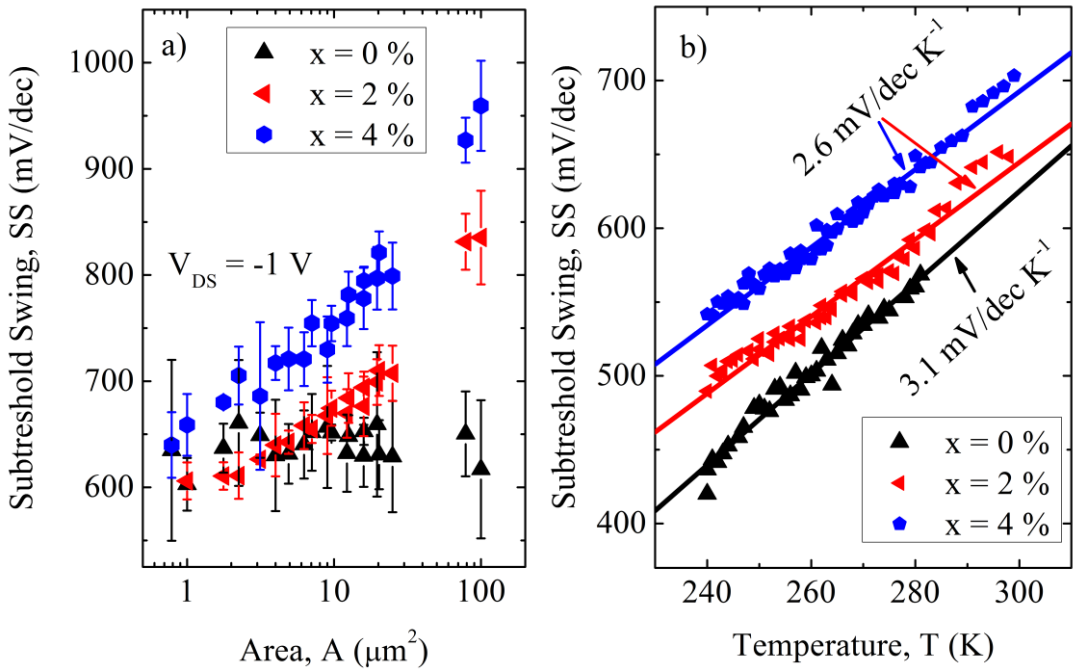

Figure 20 a) SS as a function of device area. For the GeSn-channel TFETs the SS is reduced with reducing device area. **b)** SS as a function of temperature. A linear relationship can be seen in the temperature range investigated.

Another way of reviewing the steepness of the devices is by looking at the conductance, $S = I_{DS}/V_{DS}$ in the on-state. The conductance is a measure of the tunneling probability joint density of states, and is not limited by gate oxide deficiencies [52] in the same way as the SS. The turn-on conductance of devices with gate width w_G = 40 µm is shown in Figure 21a. All devices show in general steeper conductance slopes than SSes, but still fail in coming close to 60 mV/dec steepness. As for the SS, the influence of TAT can be seen by the strong temperature dependence of the conductance slope shown in Figure 21b for sample B. Through examining

the steepness of the devices through both the SS and the conductance slope, it becomes clear that achieving sub-60 mV/dec steepness in materials with nonidealites and high defect densities is very difficult. This concern is also supported by simulations [141] and has been brought forward by others [61, 78].

3.3.3 Influence of Tin-Content in Channel on Drive Current of Germanium-Tin Tunneling Field Effect Transistors

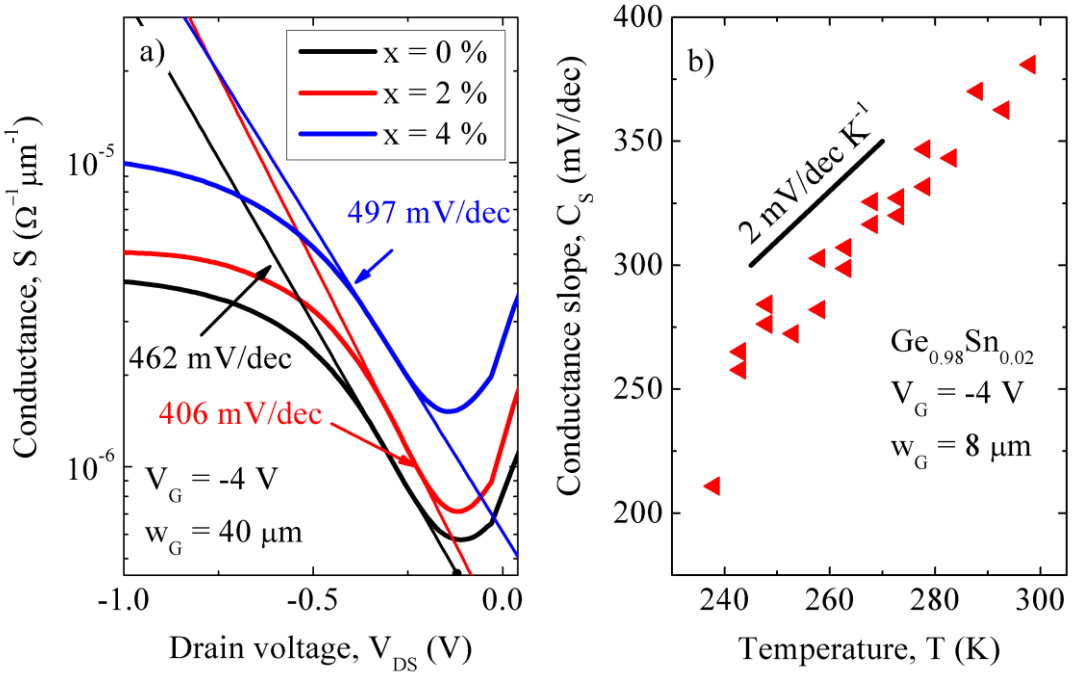

Figure 21 a) Conductance for the samples series from TFETs with the larges device areas. The devices show in general smaller conductance slopes (< 500 mV/dec) than SSes. **b)** Conductance slope plotted as a function of temperature for a transistor with x = 2 % Sn-content in the channel.

The influence of Sn-content in the $Ge_{1-x}Sn_x$ channel on the I_{ON} of the devices will now be considered. The main contribution of I_{ON} at high V_G biases is expected to be BTBT at the source-channel junction (often referred to as *point tunneling*). For devices with a source-gate overlap, BTBT in the inversion layer within the source layer (often referred to as *line tunneling*) [142], could also contribute to I_{ON}. Although the devices presented here have a large source-gate overlap, we expect a negligible line tunneling component. This is because the high source doping concentration of the devices leads to that the band structure in the material of the source region overlapped by the gate is largely unaffected when a V_G-bias is applied [77]. As already stated in section 1.4.3 the BTBT transmission probability could be estimated by using the Wentzel-Kramers-Brillouin approximation:

$$T_{WKB} \approx \exp\left(-\frac{4 \cdot \lambda \cdot \sqrt{2 \cdot m^*} \cdot E_G^{3/2}}{3 \cdot q \cdot \hbar \cdot (\Delta\Phi + E_G)}\right), \quad (27)$$

where m* is the effective mass, E_G the bandgap energy and λ the spatial extent of the tunneling region. ΔΦ is the potential difference between the valence band edge in the channel and the source conduction band edge and source Fermi level, for degenerate source doping. As mentioned in the introduction of this chapter, the promise of using GeSn in TFETs is first and foremost through raising I_{ON}. This is achieved through the lowering of E_G with respect to Ge in (27).

I_{ON}, defined here as I_{DS} (V_G = -4 V)/w_G, is plotted in Figure 22 as a function of device area A for V_{DS} = -1 V. An influence of the top contact series resistance can be seen for the 4 % Sn GeSn TFETs, with a small successive decrease in I_{ON} for devices with areas A < 10 µm^2. Considering the largest size devices, where the influence of series resistance is less, I_{ON} is seen to increase by a factor ~ 2 for x = 2 % and a factor ~ 3 for x = 4 % with respect to the Ge TFET, respectively. TAT models for TFETs have shown how traps degrade I_{OFF} and SS[135, 141]. The same models, however, show no influence of traps on the drain current at higher V_G-biases.

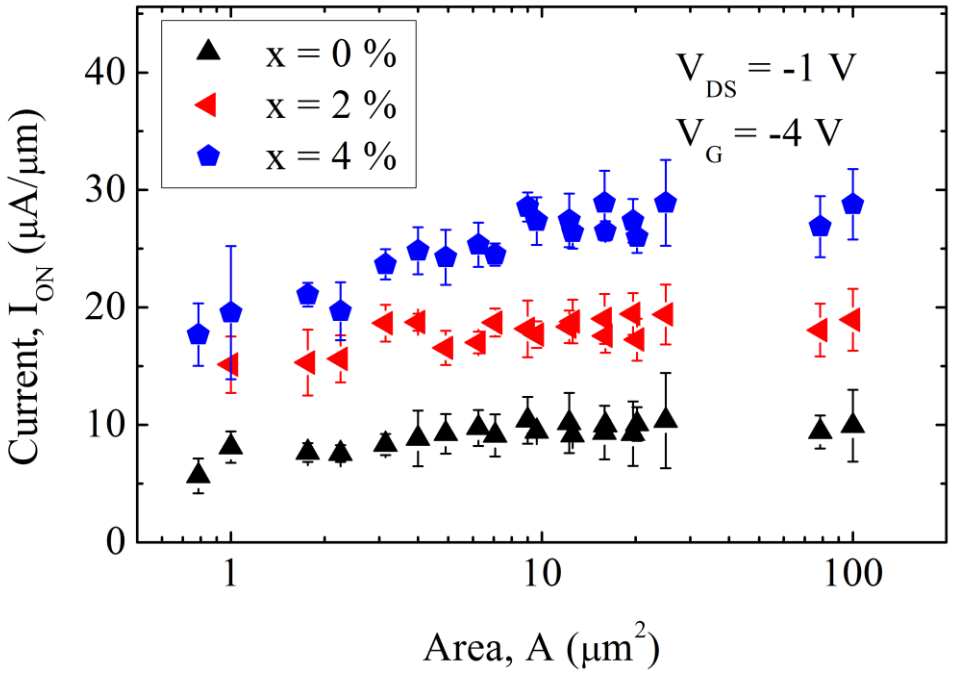

Figure 22 I_{ON} as a function of device mesa area. Due to the lowering of the bandgap I_{ON} increases when the Sn-content x in the $Ge_{1-x}Sn_x$-channel is increased. The top contact series resistance is responsible for the successive decrease in I_{ON} for smaller area devices, seen for the $Ge_{1-x}Sn_x$ TFET with x = 4 %.

The different trap densities is therefore assumed to play a minor role in determining I_{ON} for the investigated devices.

The effective mass is a material parameter, and will also affect I_{ON} when the channel material composition is altered through increasing the Sn-content. For $Ge_{1-x}Sn_x$ alloys, effective masses have been calculated [143], but show little variance within the Sn-content range investigated here. We therefore assume that the increase in I_{ON} is mainly due to the lowering of the bandgap.

In Figure 23a the averaged I_{ON} from all measured transistors is plotted as a function of Sn-content x in the $Ge_{1-x}Sn_x$ channel for different V_{DS}-biases. The ITRS low power drive current requirement is indicated (red line), $I_{ON,ITRS}$ = 456 µA/µm. It can be seen that even for a Sn-content of x = 4 %, I_{ON} is one order of magnitude below the requirement. The trend suggests that an increase of Sn-content above x > 4 % would further increase I_{ON}. However, this would seriously increase I_{OFF} which is already at an alarming level. The averaged conductance of all measured transistors as a function of V_{DS} is shown Figure 23b. For all samples the conductance can be seen to increase with increasing negative V_G before reaching saturation at at V_G ~ -1.0 V. This explains the increase in I_{ON} from V_{DS} = -0.5 V to -1 V seen in Figure 23a.

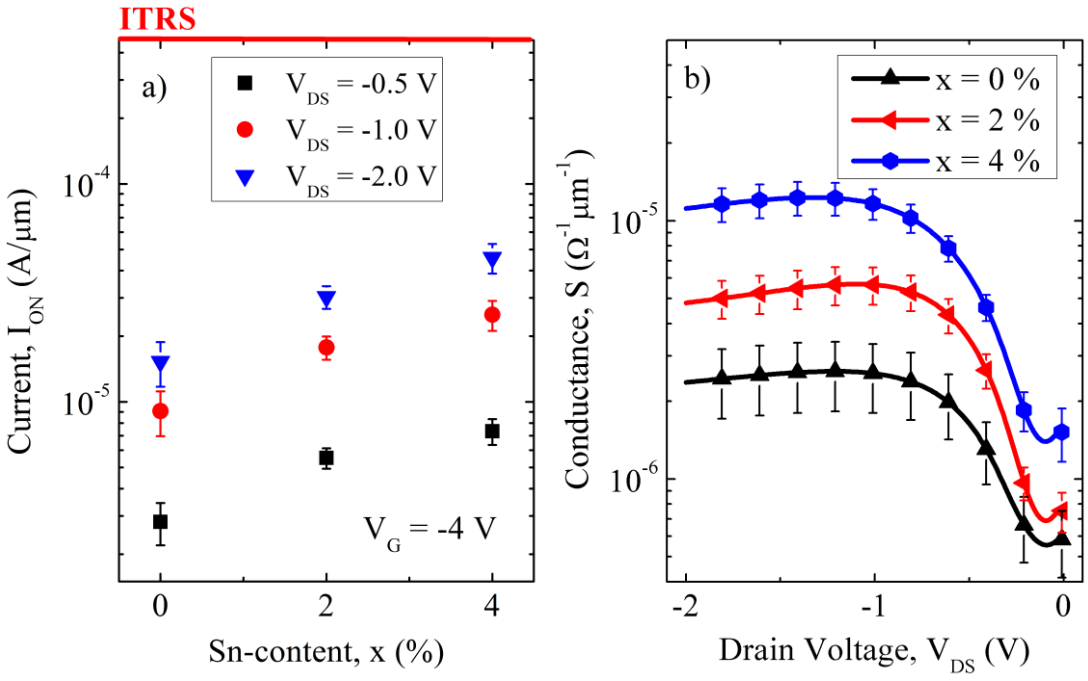

Figure 23 a) I_{ON} as a function of Sn-content in the GeSn channel for different V_{DS}-biases. **b)** The averaged conductance of all measured transistors as a function of V_{DS}.

The TFET works as an energy filter, only allowing electrons in the energy window $\Delta\Phi$ in (27) to pass. As the valence band edge in the channel cannot be raised above the valence band edge in the drain, this filtering is a function of V_{DS} as well as V_G. This sets a limit to the maximum I_{ON} for low V_{DS}. At higher V_{DS}, I_{ON} is limited by the saturating behavior of the BTBT probability. This is also seen in Figure 23a which shows only a small increase in I_{ON} from V_{DS} = -1 V to V_{DS} = -2 V. Although not as effective as it is for MOSFETs, a channel reduction could also be a means to increase I_{ON}. This is because a channel thickness reduction reduces the channel resistance [85]. If this reduction is too excessive, however, short channel effects become a concern [144].

A high interface state density also degrades I_{ON}, and a better surface passivation might improve I_{ON}. To which extent the I_{ON} of the here presented devices are degraded by interface states is, however, difficult to assess based on I-V characteristics alone.

3.4 Conclusion

GeSn could potentially be a means to realize Group-IV TFETs with high I_{ON} due to its small bandgap. However, to optimize overall device performance, it is important to understand how GeSn influences not only I_{ON} but also I_{OFF} and SS. With increasing the Sn-content in a $Ge_{1-x}Sn_x$ channel from x = 0 % to x = 4 %, I_{ON} is effectively increased. The lowering of the bandgap and the degradation of the epitaxial quality that comes with increasing Sn-content, heavily influences the I_{OFF} and SS of the devices. Due to increased TAT currents, a strong degradation of I_{OFF} was found with increasing Sn-content. It is found that achieving the required I_{OFF} and SS < 60 mV/dec with GeSn is stringent. Based on our analysis we expect that this can in part be achieved by reducing the mesa volume and reducing the GeSn layer thickness. Finding alternative and optimized MBE growth methods of GeSn, to improve crystal quality, seems also to be a must, if high performance GeSn devices are to be realized.

Chapter 4 Germanium-Tin P-Channel Tunneling Field Effect Transistors: Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface

4.1 Introduction

The GeSn channel TFETs presented in Chapter 3, together with similar studies conducted by others [87], have shown that GeSn can be implemented as channel material in TFETs as a measure to enhance the on-state currents, I_{ON}. Due to the lowering of the GeSn bandgap, tunneling probability effectively increases with increasing Sn-content. In the previous chapter it was shown that incorporating a 4 % Sn-content GeSn channel in a Ge TFET, increased I_{ON} by a factor 3 compared to a Ge TFET. However, it was also shown that the incorporation of GeSn comes at an expense. Because of crystalline defects associated with the growth of GeSn, these devices suffer from increased leakage currents, I_{OFF}. Compared to other electronic devices, the TFET needs a very high degree of perfection and accuracy with respect to material quality and fabrication[78]. Using GeSn as a performance booster, therefore puts serious requirements on the TFET design and execution. To combine the advantages of small bandgap materials (higher I_{ON}) with those of large bandgap materials (lower I_{OFF}), heterostructures with small bandgap materials positioned at the source-channel junction and large bandgap materials at the channel-drain junction are often preferable. To incorporate GeSn to boost I_{ON}, but maintain manageable I_{OFF}, a device improvement strategy is to reduce the thickness of the GeSn layer and position it at the source-channel interface.

In the experiment presented in this chapter, a 10 nm $Ge_{1-x}Sn_x$ δ-layer with x = 4 % Sn-content is implemented in 50 nm channel Ge TFETs. The position of the $Ge_{0.96}Sn_{0.04}$-δ-layer with respect to the channel-source interface is varied through an experimental series comprising three samples (A, B and C). The position of the δ-layer is shifted from completely inside the channel to completely inside the source.

It is found that I_{ON} benefit from having the $Ge_{0.96}Sn_{0.04}$-δ-layer completely or partly inside the channel. In this configuration, the spatial extent of the tunneling barrier is reduced. Furthermore, it is found that with the channel thickness of 50 nm, I_{OFF} is strongly influenced by drain induced barrier thinning (DIBT). This effect is also amplified when the $Ge_{0.96}Sn_{0.04}$-δ-layer is inside the channel, as defects in this layer induce TAT.

4.2 Layer Growth and Device Fabrication

The semiconductor layer structure was grown by MBE. All samples were grown on p-doped (< 0.05 Ω·cm) Si <100> wafers and contain a 100 nm Ge VS. The MBE layer sequence of the three samples is found in Table 4. The samples contain a 10 nm thick $Ge_{1-x}Sn_x$-δ-layer with a Sn-content of x = 4 %. This layers position with respect to the channel-source interface is varied for the three samples. In Figure 24a layer schematics of the Ge and $Ge_{0.96}Sn_{0.04}$ parts of the grown structures for the three samples is shown. More details of MBE growth of $Ge_{1-x}Sn_x$ and Ge on Si can be found in section 2.1. All samples have a total channel thickness of $d_{channel}$ = 50 nm. Compared to the samples presented in Chapter 3, the channel is reduced by 150 nm. A channel reduction in TFETs is favorable for reducing the On-resistance [85]. The thickness of the $Ge_{0.96}Sn_{0.04}$-δ-layer, d_δ = 10 nm, is well below the expected critical epitaxial thickness of $Ge_{0.96}Sn_{0.04}$ [112], and is assumed pseudomorphic biaxially strained with respect

Table 4 MBE layer sequence for the $Ge_{0.96}Sn_{0.04}$- δ-layer TFETs.

Layer	Material	Sample A Thickness (nm)	Sample B Thickness (nm)	Sample C Thickness (nm)	Doping (cm^{-3})	Growth Temperature (°C)
Source	Si	350			$N_D = 1 \cdot 10^{20}$	300
Source	Ge	100	95	90	$N_D = 1 \cdot 10^{20}$	160
Source	$Ge_{0.96}Sn_{0.04}$	-	5	10	$N_D = 1 \cdot 10^{20}$	160
Channel	$Ge_{0.96}Sn_{0.04}$	10	5	-		160
Channel	Ge	40	45	50		330
Drain	Ge	200			$N_A = 1 \cdot 10^{18}$ ↑ $N_A = 1 \cdot 10^{20}$	330
Drain	Ge (VS)	100			$N_A = 1 \cdot 10^{20}$	330
Drain	Si	50			$N_A = 1 \cdot 10^{20}$	650

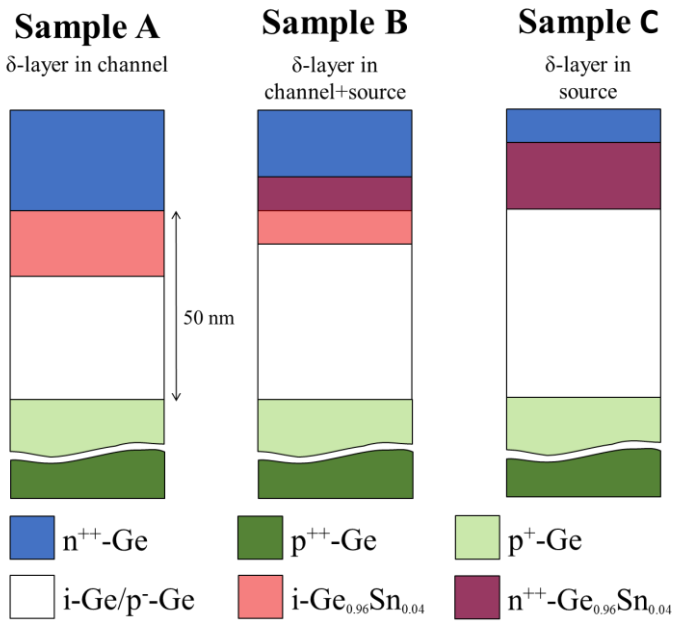

Figure 24 MBE layer schematics of the Ge and GeSn parts of the devices for samples A, B and C.

to the underlying Ge. A thickness of 10 nm is on the other hand thick enough so that quantum confinement effects (QCE) can be expected to be small. To suppress ambipolar leakage and to avoid growth interruption the drain region was grown with a doping gradient dropping from initially $N_A = 1 \cdot 10^{20}$ cm^{-3} until reaching a doping concentration of $N_A = 1 \cdot 10^{18}$ cm^{-3} at the drain-channel interface. A highly doped n-Si top contact layer was grown to ensure ohmic contacts as a final growth step.

After layer growth the devices were fabricated with the GAA fabrication process described in section 2.2. A O_2-plasma post oxidation step with duration t = 5 min was performed and a total of 60 ALD cycles were conducted. A physical oxide thickness of d_{ox} ~ 9 nm of the particular Al_2O_3/GeO_x gate oxide was measured by ellipsometery. Based on a Si MOS capacitor reference, a corresponding EOT of ~ 4.5 nm of this particular gate oxide is expected.

4.3 Results and Discussion

Figure 25a and Figure 25b show the transfer and output characteristics of samples A, B and C, respectively. The steepest SS is found for sample C with SS ~ 430 mV/dec and is indicated in the plot. When comparing the IV characteristics of transistors from the three samples, it can be seen that the position of the $Ge_{0.96}Sn_{0.04}$-δ-layer influences both the leakage current, I_{OFF}, and the drive current I_{ON}. Its influence on I_{OFF} will be considered first, while its influence on I_{ON} will be considered later on.

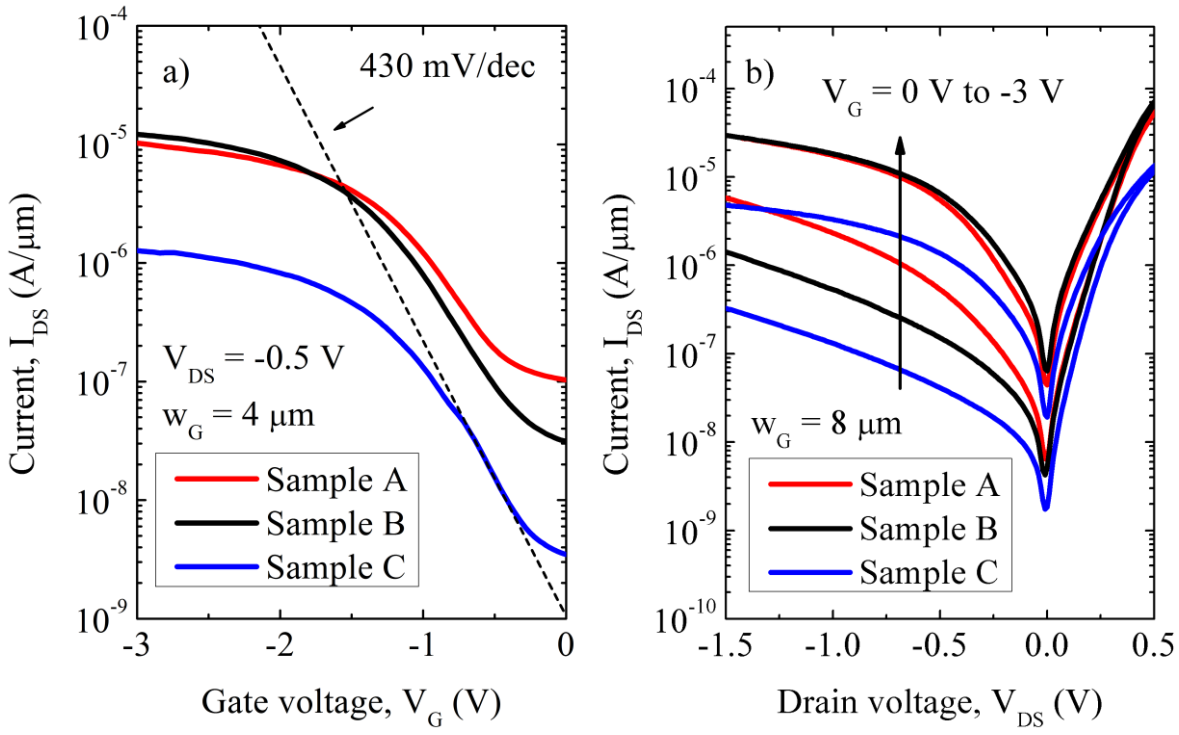

Figure 25 a) Transfer characteristics of transistors from sample A, B and C. The dashed black line indicate the minimum subthreshold slope obtained for sample C. **b)** Output characteristics of transistors from sample A, B and C.

4.3.1 Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface on Leakage Current

I_{OFF} is in the following discussion defined as the drain current at zero gate bias normalized to the gate width, $I_{OFF} = I_{DS}$ (V_{DS}, V_G = 0 V)/w_G. I_{OFF} as a function of device area is shown in Figure 26. By looking at the area dependence of I_{OFF}, we obtain information on *where* the current is flowing. All three samples can be seen to be proportional to the area (indicated by lines), indicating area leakage dominance. Perimeter and gate leakage currents can therefore be neglected in the following discussion as these play minor roles. In this respect, the off-state characteristics of the devices are similar to those of the GeSn channel TFETs presented in Chapter 3. For the smallest size TFETs (A < 1 µm^2) a deviation from the current density lines can be seen. This is believed to be due to the high series resistance (R_S) of these TFETs, which reduces the voltage drop over the diode by an amount $V = I_{OFF} \cdot R_S$. For devices with dominant area leakage, device scaling, i.e. mesa reduction, is a device improvement strategy for reducing I_{OFF} and improving the I_{ON}/I_{OFF} ratio. By establishing an area proportionality of I_{OFF}, we can now discuss the positional dependence of the $Ge_{0.96}Sn_{0.04}$-δ-layer at the source-channel interface with respect to the pin epitaxial layer structures of the samples. An increase in I_{OFF} by a decade

can be seen when shifting the $Ge_{0.96}Sn_{0.04}$-δ-layer from the source, sample C, into the channel, sample A. I_{OFF} of Sample B can be found to lie in between the other samples. The total thickness and Sn-content of the $Ge_{0.96}Sn_{0.04}$-δ-layer are the same for all devices. One can therefore expect the same total number of growth defects, i.e. traps, to be present in each samples. The positions of the traps with respect to the pin diode depletion electric field, however, are different. A strong field dependence is the signature of tunneling events. With the asymmetric doping profiles of the samples, the channel-source interface represents the position in the depletion region where the electrical field is at its maximum. With a high source doping concentration, the electrical field also rapidly decreases since the depletion width does not extend far into the source region. Different TAT leakage contributions to I_{OFF} could therefore explain the positional dependence of the $Ge_{0.96}Sn_{0.04}$-δ-layer. The traps confined within this layer are more likely to contribute to tunneling currents when positioned in the channel where the electrical field is higher. As the $Ge_{0.96}Sn_{0.04}$-δ-layer is moved further outside the depletion region the trap states are less likely to contribute to tunneling currents.

The temperature dependencies of the TFETs were investigated by lowering the measurement temperature from T = 298 K to T = 240 K. The temperature dependence of the transfer characteristics of a transistor from sample B is seen in Figure 27a. In the inset of the same figure the Arrhenius plot of $I_{OFF,}$ together with linear fits are shown. A high contribution of tunneling currents to I_{OFF} is confirmed by the low activation energies of the samples derived from

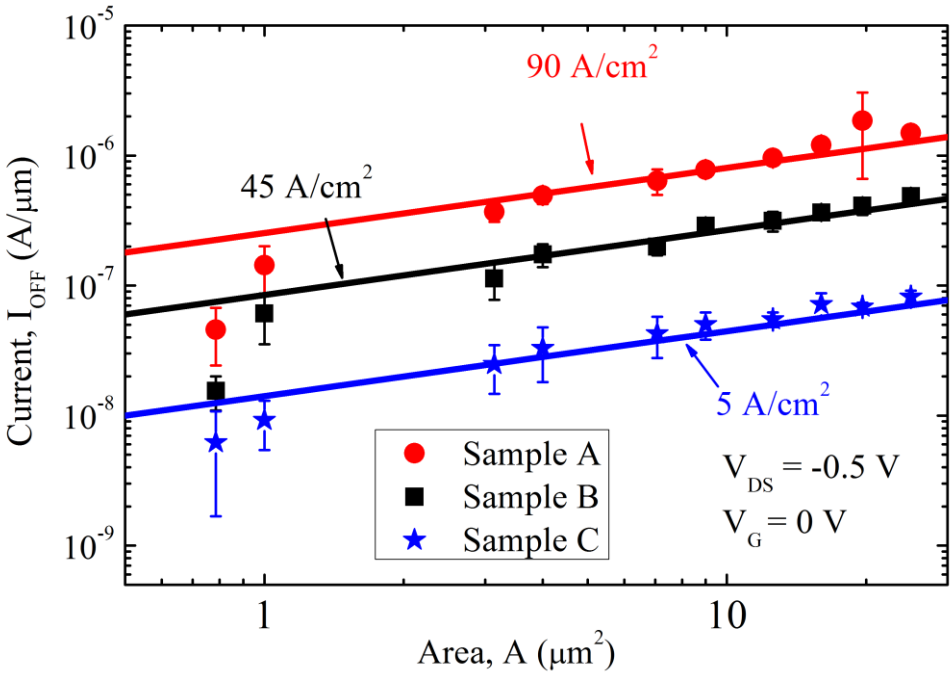

Figure 26 I_{OFF} as a function of device area for the three samples at V_{DS} = -0.5 V. I_{OFF} can be seen to be proportional to device area.

Arrhenius plots. These are shown in Figure 27b for drain-source voltages V_{DS} = -0.5 V and V_{DS} = -1.0 V. The extracted activation energies are considerably lower than half of the bandgap, which is what one would expected if SRH generation processes were dominating [31]. The low activation energies could also indicate contributions of BTBT processes without trap assistance [145]. The lowest activation energy is found for sample A. This further supports the idea of that tunneling leakage current increase when the $Ge_{0.96}Sn_{0.04}$-δ-layer is positioned inside the channel where the depletion electric field is high. The activation energies are also considerably lower than the 4 % Sn-content GeSn channel TFET presented in Chapter 3. This can be explained by the reduction in channel thickness, compared to those samples. Reducing the intrinsic channel region greatly affects the electrical field and tunneling width across the pin junction.

The activation energy of the samples can also be seen to vary with V_{DS}-bias. A strong reduction in activation energy is seen by increasing negative V_{DS}-bias. This is because the increase in V_{DS}-bias effectively reduces the extent of the tunneling barrier across the channel, inducing more tunneling currents. This effect is often referred to as drain induced barrier thinning (DIBT) [146], and is more likely to be seen for TFETs with short channels and poor electrostatic control over the body. DIBT often describes only tunneling across the entire junction, directly from valence and into the conduction band. Based on the results presented

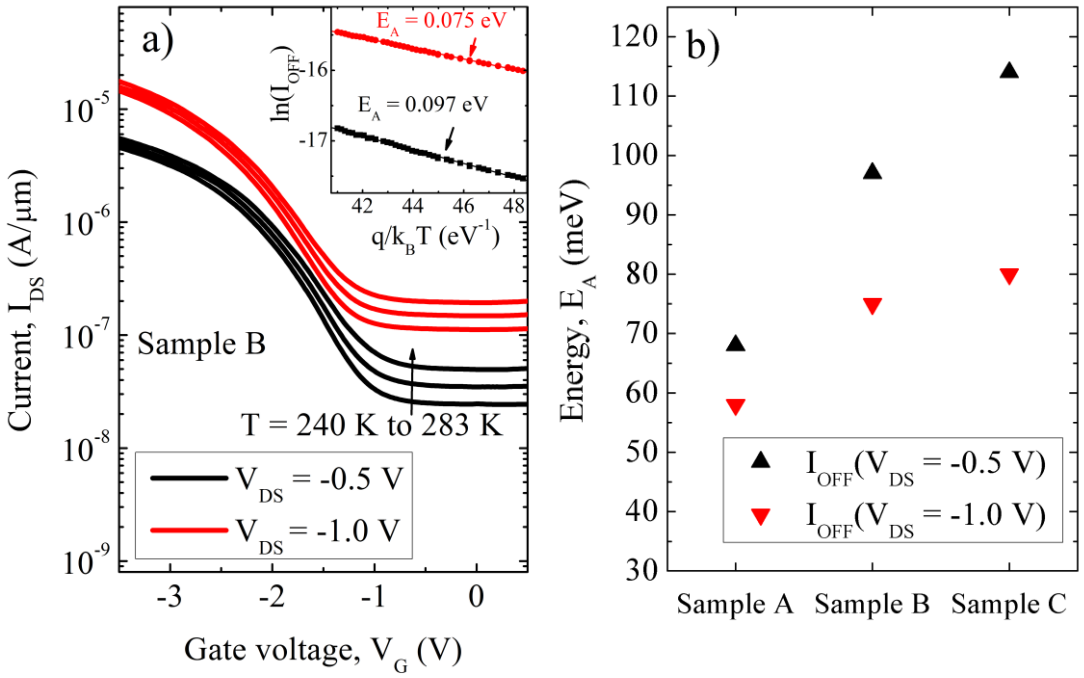

Figure 27 a) Transfer characteristics showing the temperature dependence of a transistor from sample B for V_{DS} = -0.5 V (black curves) and V_{DS} = -1 V (red curves). The inset shows Arrhenius plot of I_{OFF}. The corresponding activation energies obtained from fits are indicated. **b)** The activation energy of I_{OFF} for all samples for V_{DS} = -0.5 V and V_{DS} = -1 V. Low activation energies indicate tunneling dominance.

here we expect the traps to be influential, and the tunneling lengths are less then what expect from an ideal TFET with channel thickness $t_{channel}$ = 50 nm. The observed high I_{OFF} and DIBT, is a strong argument against further channel thickness reduction. Based on the results, a thicker channel might be favorable to reduce the leakage current.

4.3.2 Positional Dependence of Germanium-Tin-Delta-Layer at Source-Channel Interface on Drive Current

The positional dependence of the $Ge_{0.96}Sn_{0.04}$-δ-layer on I_{ON} will now be considered. In Figure 28a the transfer characteristics of the transistor with the highest I_{ON}, I_{ON} = 180 µA/µm for V_{DS} = -2 V and V_G = -4 V, is shown. Although exhibiting a very high I_{ON}, a high I_{OFF} results in a poor transistor performance with a low I_{ON}/I_{OFF}-ratio. The high I_{OFF} is resulting from the TAT leakage and DIBT at high negative V_{DS}-bias discussed above. In Figure 28b the averaged I_{ON} is shown as a function of V_{DS} for the samples. No difference between the I_{ON} of samples A and B can be seen, while both of them exhibit higher I_{ON} than that of sample C. On averaged I_{ON} is a factor ~3 higher for samples A and B than for sample C.

The effect of the position of the $Ge_{0.96}Sn_{0.04}$-δ-layer on I_{ON} can be explained by examining the band structure in each of the three cases. Band offsets including strain dependent effects were calculated using model solid theory [147], and all model parameters, except for the bandgaps, were obtained from linear interpolations of the model parameters for Ge and Sn. Quadratic interpolation according to [148] was used to calculate the bandgap energies. A similar parameter set as that of [149] was used, but updated to include the newer experimental data of [148]. Band offsets between materials were approximated according to [150]. The largest calculated band offset between Ge and $Ge_{0.96}Sn_{0.04}$ was found in the valence band between the heavy hole (hh) bands, ~ 50 meV. The conduction band offset was calculated to ~ 20 meV for the L-band, respectively. A band structure calculation of a Ge TFET was obtained using SILVACO Atlas [151] and the calculated band offsets between the hh-bands and between the L-bands of Ge and $Ge_{0.96}Sn_{0.04}$ were imposed onto these calculations for the on- and off-state of the transistor for the three different devices.

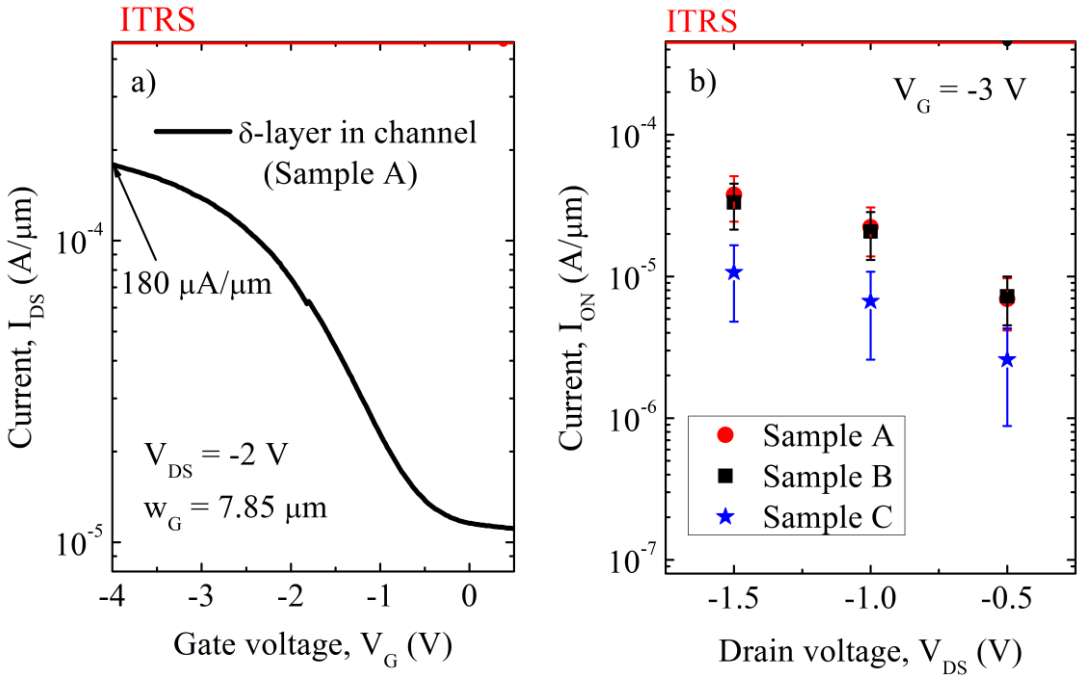

Figure 28 a) Transfer characteristics from the transistor with the highest I_{ON} (sample A). **b)** Averaged I_{ON} as a function of drain voltage. The samples with the GeSn-δ-layer completely or partly in the channel (samples A and B) exhibit higher I_{ON} than the sample with the GeSn-δ-layer in the source (sample C).

Figure 29 shows the schematic band structure diagrams for the source-channel junction of the three device types. The behavior of I_{ON} can be understood qualitatively from those band diagrams. The main contribution to point tunneling will take place at the junction where the spatial extent of the tunneling barrier, λ, has its minimum value. Tunneling is enhanced if that region is within the low bandgap material layer, both due to reduced barrier width and reduced bandgap. This is the case for both when the $Ge_{0.96}Sn_{0.04}$--δ-layer is situated in the channel (sample A) and across channel and source region (sample B), see Figure 29. Hence, I_{ON} is largely unchanged between those to samples. When the $Ge_{0.96}Sn_{0.04}$-δ-layer is shifted entirely into the source region (sample C) I_{ON} degrades as tunneling mainly occurs within the Ge.

As the $Ge_{0.96}Sn_{0.04}$-δ-layer positioned inside the source seem to have little influence on the I_{ON}, sample B has an effectively thinner $Ge_{0.96}Sn_{0.04}$-δ-layer than sample A. Sample B, however, show similar I_{ON} and much better I_{OFF} than sample A. Based on this, a strategy for device performance improvement would be to downscale the thickness of the $Ge_{0.96}Sn_{0.04}$-δ-layer. This is because reducing the thickness would reduce I_{OFF} while leave I_{ON} unchanged. With a layer reduction, quantum confinement effects (QCE) could, however, come into play. QCE increases the effective bandgap [152] and might be counterproductive with respect to increasing the tunneling probability.

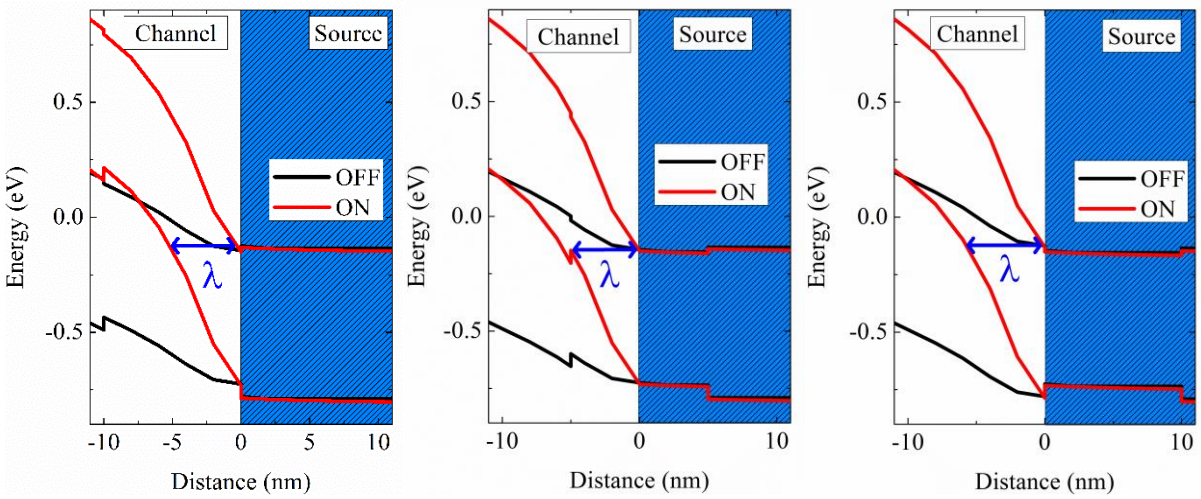

Figure 29 Schematic band structure diagrams for the source-channel junction of the three samples in off- (black) and on- (red) state of the TFETs. Left: Sample A, middle: Sample B, right: Sample C. The tunneling barrier λ is reduced when the GeSn is inside the channel. Bandgap calculations were conducted by Torsten Wendav at Institute for Physics, Humboldt-Universität zu Berlin.

4.4 Conclusion

The low bandgap of GeSn is an interesting attribute on the roads toward achieving high I_{ON} in Group-IV TFETs. However the bandgap lowering and the defect density of epitaxial GeSn on Ge causes fundamental problems for the leakage currents. In this experimental study the positional dependence of a 10 nm $Ge_{0.96}Sn_{0.04}$-δ-layer with 4 % Sn-content at the source-channel interface was investigated. When confined in a 10 nm δ-layer, $Ge_{0.96}Sn_{0.04}$ is most beneficial for I_{ON} when positioned in the channel as opposed to inside the source. As the bandgap offset between Ge and $Ge_{0.96}Sn_{0.04}$ is mainly in the valence band, the spatial extent of the tunneling barrier is reduced in this layer structure configuration. The highest I_{ON} are achieved in the sample with the $Ge_{0.96}Sn_{0.04}$-δ-layer completely in the channel with I_{ON} = 180 µA/µm for V_{DS} = -2.0 V and V_G = -4 V. The positional dependence of the $Ge_{0.96}Sn_{0.04}$-δ-layer is seen to greatly influence the I_{OFF} of the samples. Due to the strong electrical field at the channel-source interface, tunnel events involving trap states contribute to more TAT leakage when the GeSn-δ-layer is inside the channel. The devices are also seen to be a subject to DIBT, with increased tunneling current contribution to I_{OFF} with increasing negative V_{DS}-bias.

Although $Ge_{1-x}Sn_x$ show some optimistic attributes with respect to boosting I_{ON}, the associated increase in I_{OFF} raises some question about the feasibility of achieving acceptable performance $Ge_{1-x}Sn_x$ TFETs. A possible strategy to boost I_{ON} consists of increasing the Sn content x in the $Ge_{1-x}Sn_x$-δ-layer. However, the leakage current density has to be reduced to

keep I_{OFF} manageable. Based on our analysis we expect that this can in part be achieved by reducing the mesa volume and reducing the δ-layer thickness.

Chapter 5 Source Doping Concentration Variation in Germanium P-Channel Tunneling Field Effect Transistors

5.1 Introduction

The source doping concentration of TFET is an important device parameter which can influence both the BTBT drive current, I_{ON}, and the SS. When trying to determine the optimal source doping for a TFET, some important trade-off aspects have to be taken into consideration. In general, a high source doping concentration is needed to ensure a short source depletion length and achieve high junction electrical fields favorable for tunneling. However, degeneracy reduces the number of electrons available for tunneling and can limit I_{ON}. A lower source doping might in many cases also be important in achieving low SS [153]. Because of the temperature dependence of the Fermi tail and also *band edge smearing* [52], degeneracy introduces a temperature dependence which degrades the energy filtering mechanism needed to attain SS < 60 mV/dec.

In the case of TFETs with a gate-source overlap, another tunneling current contribution comes into play. The energy bands in the source region overlapped by the gate are bent due to the applied gate field. With sufficient band bending, BTBT can then take place also in this region. Unlike tunneling which takes place at the source-channel interface, often referred to as *point tunneling*, this type of tunneling is aligned with the gate field. The tunneling is hence perpendicular to the gate oxide, and is often referred to as *line tunneling* [154]. Line tunneling shares resemblance to GIDL current, but contributes to current flow for the same gate polarity as intended for the device. TFET concepts using line tunneling to enhance I_{ON} has been showed experimentally for Si [9] and SiGe[84] TFETs. Both line and point tunneling are a function of the source doping. Simulations of TFETs taking both types of tunneling into account, have proposed that there exists an optimal doping for devices with source gate overlap [88]. However, varying the source doping in gate-source overlap Ge devices has, to this author's knowledge, not been subject of experimental investigation.

In this chapter the effect of varying source doping concentration on the electrical characteristics of Ge p-channel TFETs with gate-source overlap is presented. With an experimental sample series comprising three samples, the doping concentration in source region is varied, $N_S = 1{\cdot}10^{19}$ cm^{-3}, $3{\cdot}10^{19}$ cm^{-3} and $5{\cdot}10^{19}$ cm^{-3}. The TFETs demonstrate different subthreshold characteristics dependent on N_S. Contrary to what is expected for point tunneling TFETs, the samples with the highest source doping show the steepest SSes. Based on the V_{DS} and temperature dependence of the transfer characteristics, this is believed to be due to gate induced TAT in the source region overlapped by the gate. By increasing the source doping the onset of this thermal activated subthreshold current is delayed and lower SS are achieved. Although showing steeper subthreshold characteristics, the TFETs with high source doping also demonstrate an earlier saturation. This leads to approximately equal I_{ON} between the samples.

5.2 Layer Growth and Device Fabrication

The semiconductor layer structure was grown by MBE. All three samples were grown on p-doped (10-20 Ω·cm) Si <100> wafers and contain a 100 nm Ge VS. The gate-source overlap is defined by the source Si-Ge heterojunction. For the samples this region includes the 100 nm source region with doping concentration N_S, as well as a $1{\cdot}10^{20}$ cm^{-3} top top Ge layer, which is the same for all three samples. The samples vary by having different doping concentration N_S. The doping concentration was $N_S = 1{\cdot}10^{19}$ cm^{-3}, $N_S = 3{\cdot}10^{19}$ cm^{-3} and $N_S = 5{\cdot}10^{19}$ cm^{-3} for the three samples, respectively. These doping concentrations all correspond to degenerate doping levels, being equal or higher than the effective density of states in the Ge conduction band, $N_C = 1{\cdot}10^{19}$ cm^{-3}[139]. The samples all have a 200 nm channel region, and a 200 nm Ge drain region with a gradual doping profile. An asymmetric doping profile is used to suppress ambipolar leakage. The MBE layer sequence of the samples is given in Table 5.

After MBE growth of the samples, a broken piece from the Si shutter was found in the Ge effusion cell. When reviewing the growth log, it was established that the incident had happened before the growth of the samples. A Si contamination of the grown Ge for all samples can therefore be expected. The melting point of Si (T_{Si} = 1414 °C) is above the working temperature of the Ge effusion cell (typically $T_{eff.cell}$ ~ 1300 °C). The vapor pressure of Ge is therefore expected to dominate during Ge growth. We therefore assume that the Si contamination is negligible, and in the following discussion Ge will be considered. Unfortunately, no SIMS or similar methods could be used to establish the actual Si contamination within the time scope of the experiment.

Table 5 MBE layer sequence for the Ge TFETs with varying source doping concentration.

Layer	Material	Thickness (nm)	Doping (cm^{-3})	Growth Temperature (°C)
Source	Si	100	$N_D = 1 \cdot 10^{20}$	300
Source	Ge	100	$N_D = 1 \cdot 10^{20}$ (N_D)	160
Source	Ge	100	**$N_S = 1 \cdot 10^{19}, 3 \cdot 10^{19}, 5 \cdot 10^{19}$**	160
Channel	Ge	200	-	330
Drain	Ge	200	$N_A = 1 \cdot 10^{18}$ ↑ $N_A = 1 \cdot 10^{20}$	330
Drain	Ge (VS)	100	$N_A = 1 \cdot 10^{20}$	330
Drain	Si	400	$N_A = 1 \cdot 10^{20}$	650

After layer growth the devices were fabricated with the GAA fabrication process described in section 2.2. A O_2-plasma post oxidation step with duration t = 5 min was performed and a total of 60 ALD cycles were conducted. A physical oxide thickness of $d_{ox} \sim 9$ nm of the particular Al_2O_3/GeO_x gate oxide was measured by ellipsometery.

5.3 Results and Discussion

Figure 30 shows the transfer characteristics of Ge TFETs with varying source doping concentration, N_S. A line is plotted to indicate the steepness of the devices with SS = 370 mV/dec. The three samples show similar transfer characteristics. A large set of transistors (> 25) from each sample was therefore measured for a better comparison, and to account for transistor to transistor variance within each sample.

5.3.1 Influence of Source Doping Concentration on Leakage Current in Germanium Tunneling Field Effect Transistors

The leakage current of the TFETs will now be considered first. The TFETs in Figure 30 all exhibit an ambipolar behavior, with increasing current for positive gate voltage. This ambipolar behavior is due to the gate induced tunneling which can take place at the drain-channel interface, ambipolar leakage, and/or in the drain region overlapped by the gate, GIDL. This gate induced leakage current leads to a distinct minimum in the transfer characteristics. The position

of this minimum with respect to the gate voltage can be assumed influenced by three factors: (I) the magnitude and onset of the gate induced leakage current, (II) the magnitude and onset of the drive current and (III) the flatband voltage shift. The current level at this minimum is, in addition to the ambipolar leakage and drive current, also determined by the leakage current of the reversed biased pin diode. This contribution can be assumed independent of gate voltage. The measured leakage through the gate oxide is negligible in comparison to the drain current and has no influence on the device characteristics.

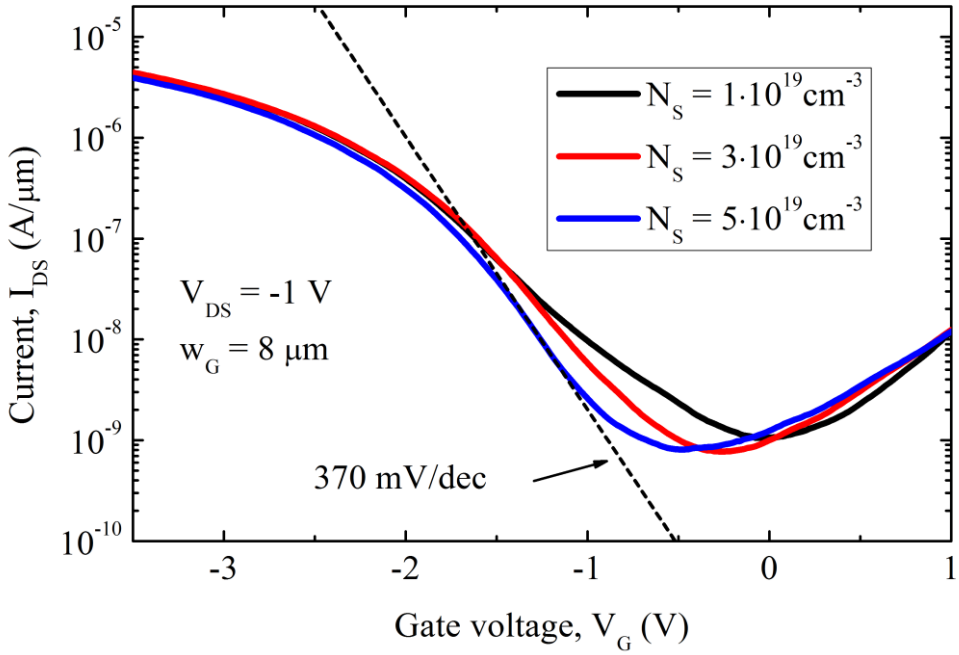

Figure 30 Transfer characteristics of TFETs with different source doping concentration. The TFETs show similar minimum leakage current and maximum drive currents, but demonstrate different subthreshold characteristics.

The averaged gate voltage corresponding to the minimum drain current, V_G,min = $V_G(I_{min})$, as a function of N_S is plotted in Figure 31a. V_G,min can be seen to vary between the samples, trending to shift towards negative gate biases as the source doping is increased. This indicates that one or more of the factors (I-III) differ for the samples. A flatband voltage shift originates from the gate metal-semiconductor work function difference as well as oxide and interface charges[123]. These parameters should, however, be comparatively equal for the samples, and result in a constant parallel shift of the transfer curve for all samples. The samples have the same gate oxide and gate metal. The gate induced leakage current is determined by the drain and drain-channel interface regions. Due to the same structure and composition of the drain regions of the samples also similar gate induced leakage currents are expected. Based on these

assumptions, the different nature of the drive current in the subthreshold region is causing the shift of the minimum. This is also supported visually by the transfer characteristics in Figure 30, which exhibit different on-set behavior and different SSes between the samples. The subthreshold characteristics will be discussed in details later on. The averaged current value at the minimum normalized to the gate width, I_{min}, is plotted as a function of device area in Figure 31b. I_{min} can be seen to be independent of device area. An area dependence of I_{min} would imply a much bigger difference (a factor of 10) between the I_{min} of the largest and smallest size transistors, respectively. I_{min} is hence mainly flowing at the surface and is proportional to the perimeter of the device. Perimeter leakage current includes the discussed gate induced leakage currents, but can also include SRH generation and TAT due to traps at the Ge/gate oxide surface, increasing the pin diode leakage current. To effectively reduce the gate induced leakage current, a gate-drain underlap is required[47]. This would necessitate the formation of a spacer [81] for the vertical devices presented here. How best to achieve this spacer technology is still unclear, as many considerations has to be taken into account. Dopant diffusion prohibits the use of high temperatures, while a nanometer thickness accuracy might be needed. Lowering the drain doping concentration and forming an asymmetry in the source-drain doping level is a common strategy to suppress the tunneling at the channel drain interface[60]. For TFETs with

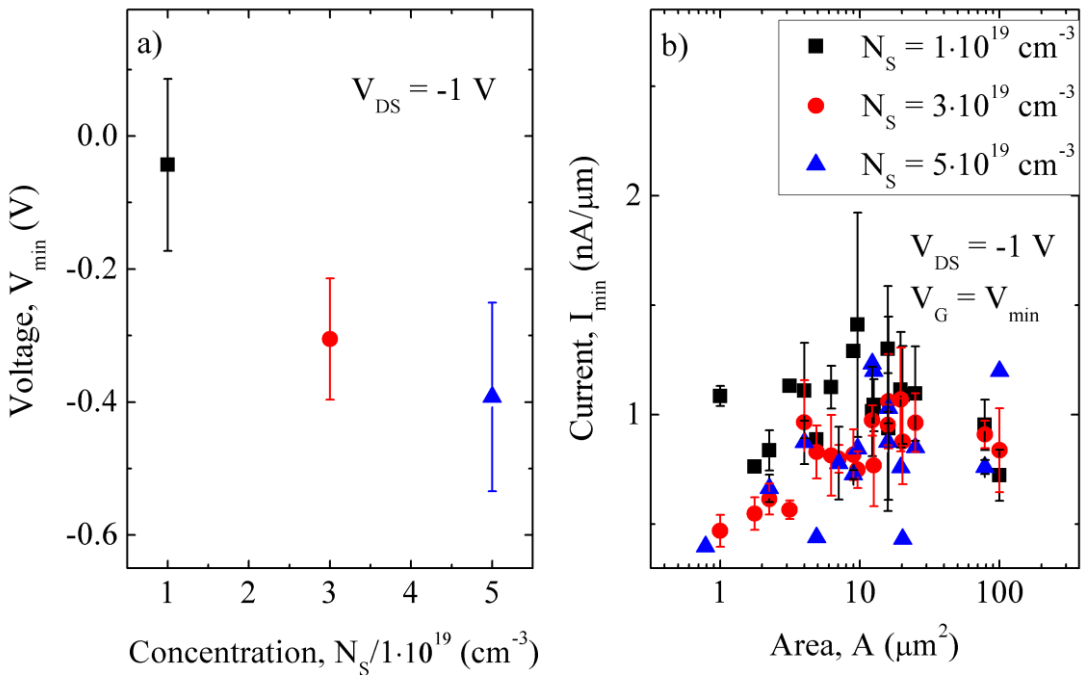

Figure 31 a) The gate voltage corresponding to the minimum drain current in the transfer characteristics, $V_{G,min}$, as function of N_S. $V_{G,min}$ shifts towards negative values with increasing doping concentration. **b)** I_{min} as a function of device area. The devices show little dependence on area. This indicates that I_{min} is determined by the perimeter of the device.

gate-drain overlap this could, however, lead to increased tunneling in the drain region overlapped by the gate, GIDL, as the onset voltage of this transport mechanism is lowered.

5.3.2 Temperature Dependence of Germanium P-Channel Tunneling Field Effect Transistors with Varying Source Doping Concentration

Temperature dependence of the transfer characteristics of the Ge TFETs was investigated by stepwise varying the measurement temperature from T = RT to T = 243 K. The transfer characteristic of a TFET with source doping $N_S = 3{\cdot}10^{19}$ cm^{-3} at different temperatures is shown in Figure 32. A strong temperature dependence can be seen for the minimum drain current, the subthreshold region and for the ambipolar branch. In the inset of the same figure, the Arrhenius plot of the current for the V_G-bias demonstrating the highest activation energy, is shown.

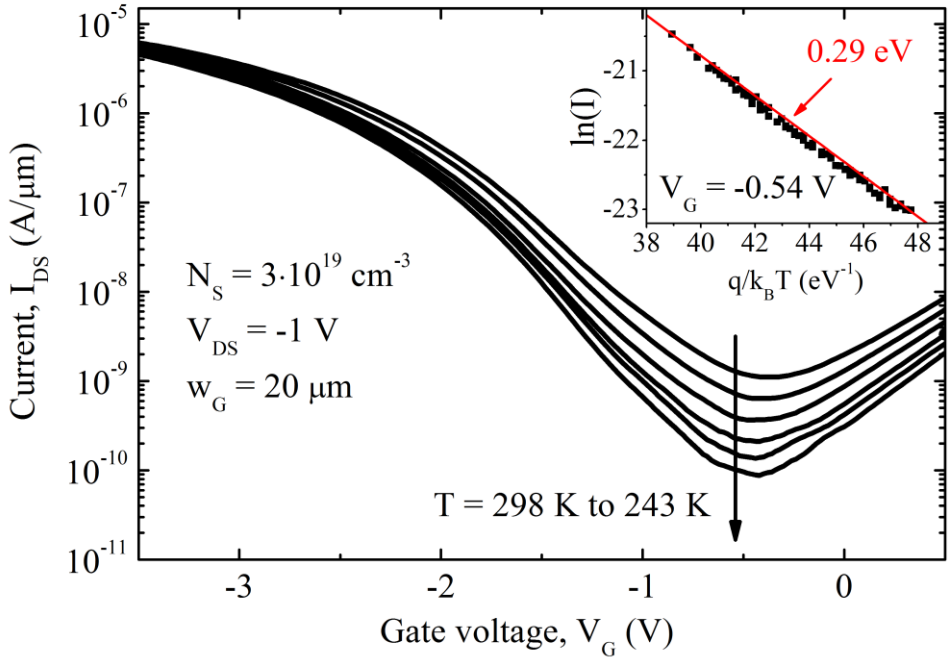

Figure 32 Transfer characteristics of a sample with $N_S = 3{\cdot}10^{19}$ cm^{-3} at different temperatures. The leakage floor and the subthreshold region exhibits a strong temperature dependence. Arrow indicates the gate bias for which the maximum activation energy was calculated. Inset shows the Arrhenius plot of the current at this bias.

Figure 33a shows the resulting plot of the activation energy as a function of gate bias. The maximum activation energy is approximately equal for all samples (E_A ~ 0.29 eV), and close to half the bandgap, $E_G/2$, of Ge. This together with the perimeter dependence, indicates that SRH generation current at the surface is the main contribution to the leakage current at this minimum. The temperature dependence of SRH generation current is equal to the temperature dependence of the intrinsic carrier concentration n_i (see section 1.4.5). The position of the maximum E_A with respect to gate voltage can be seen to shift towards negative gate voltage

with increasing source doping concentration. This correlates to the voltage shift of $V_{G,min}$ discussed above. At $V_{G,min}$ the contribution of the gate field dependent currents are weakest and therefore represent the region where SRH generation contribution will be largest. The temperature dependence of the gate induced leakage current is not consistent with BTBT mechanism. For Ge, an activation energy of $E_A \sim 0.1$ eV is expected for a BTBT process[145]. The higher activation energies therefore indicate TAT currents, involving SRH generation processes. This type of TAT process has for a long time been known to be the cause of the temperature dependence of GIDL at low gate fields for MOSFETs [155, 156].

At high negative gate bias the drain current of the TFETs is seen to have low temperature dependence, with $E_A < 0.1$ eV. This is consistent with a BTBT drive current. The combination of a strong temperature dependence of the leakage current and the weak temperature dependence of the drive current, leads to a significant improvement in the I_{ON}/I_{min}-ratio as the temperature is lowered (see Figure 33b). At a measurement temperature of T = 243 K, two of the three measured transistors demonstrate a I_{ON}/I_{min}-ratio of more than five decades for V_{DS} = -1 V. This can be considered as good for an all-Ge field effect transistor device.

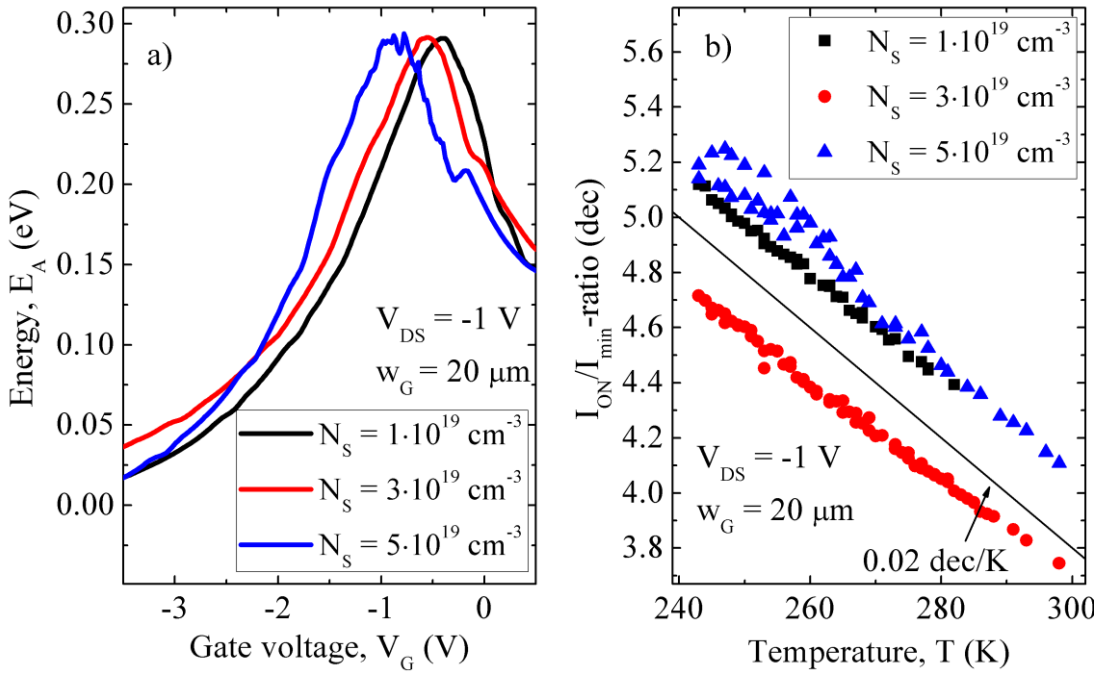

Figure 33 a) Activation energy as a function of gate voltage. The maximum activation energy of the samples is close to $E_G/2$ for Ge, indicating a leakage current dominated by SRH generation. **b)** The strong temperature dependence of I_{min}, leads to over a decade improvement of the I_{ON}/I_{min}-ratio of the TFETs.

5.3.3 Influence of Source Doping Concentration on Subthreshold Swing in Germanium P-Channel Tunneling Field Effect Transistors

From the results presented so far it becomes clear that the largest divergence between the three Ge TFET samples can be found in the subthreshold region. The SS and the subthreshold regions of the TFETs from the three samples will therefore now be examined more closely. The SS is here defined as the steepest point in the transfer characteristics. The averaged (closed symbols) and the minimum SS (open symbols) of the TFETs from the three samples are shown in Figure 34a as a function of V_{DS}-bias. The SS as a function of temperature for the three TFETs is shown in Figure 34b. The lowest SS was found for a TFET with source doping of $N_S = 5 \cdot 10^{19}$ cm^{-3} and was SS = 323 mV/dec for V_{DS} = -1 V. This is a factor ~ 5.4 away from the 60 mV/dec MOSFET-limit and considerably higher than the lowest SS measured by a TFET so far [23]. In part this can be explained by the thick gate oxide needed to prevent leakage current flowing between substrate and gate. Gate oxide thickness is, however, equal for the three samples and can therefore not explain the difference between the samples. When the doping is lowered, the width of the part of the tunneling barrier extended into the source region is increased. The contribution of the SS that is due to the gate voltage manipulation of the electrical field (see (14) in section 1.4.4), is inversional proportional to the tunneling width. Low source doping is therefore expect to improve SS for TFETs [153]. Contrary to this, the

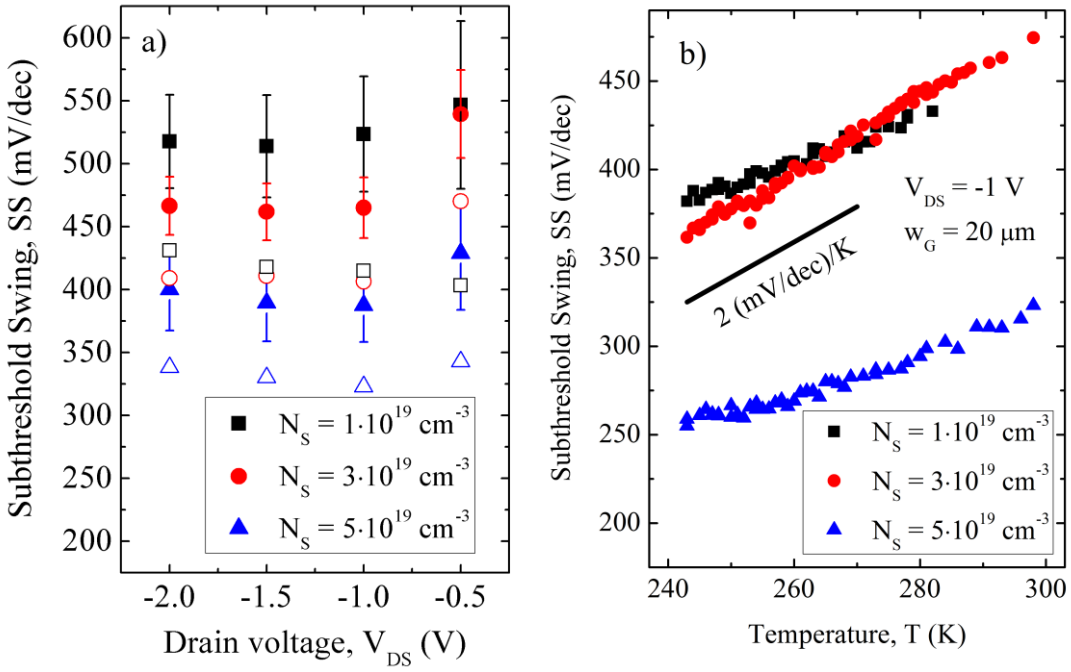

Figure 34 a) Averaged (closed symbols) and minimum (open symbols) SS as a function of drain-source voltage. SS is seen to be independent of V_{DS}-bias **b)** SS as a function of temperature. SS is improved when the temperature is reduced

results presented here show the exact opposite trend. The transistors from the sample with the highest source doping exhibit the lowest SS. This is true both with respect to the averaged SS (closed symbols) and the lowest measured (open symbols) SS, respectively. On average the SS of the TFETs with the highest source doping concentration ($N_S = 5 \cdot 10^{19}$ cm^{-3}) has over 100 mV/dec lower SS than the TFETs with the lowest source doping ($N_S = 1 \cdot 10^{19}$ cm^{-3}).

Furthermore, the SS of all samples demonstrate a weak V_{DS}-bias dependence. In Figure 35a-c transfer characteristics of TFETs from each sample are shown for different V_{DS}-biases. Similar to the subthreshold characteristics of a MOSFET, it can be seen that the drain current in the subthreshold regions (indicated with red circle) are seemingly linear in the semi-log scale and independent of V_{DS}-bias for all samples. A V_{DS}-independence of TFETs can be attained in 1D systems with aggressively scaled oxide and excellent electrostatic gate control [157]. For the bulk system with thick oxide presented here, this is, however, not expected. The line tunneling Si/SiGe heterostructure TFETs presented in[84], which are reprinted in Figure 35d, show similar subthreshold characteristics as those of shown here (see Figure 35a-c), but this is neither discussed nor mentioned by the authors. A weak V_{DS} dependence of the drain current could, however, indicate line tunneling. The magnitude of the line tunneling depends on the band bending in the source region overlapped by the gate (see Figure 36a). As the source is grounded and lies mainly outside the pin depletion region, the band bending in this region is mainly controlled by V_G alone [158]. However, a relatively high gate field is required to activate line tunneling. The energy bands must be bent to the extent that tunneling is allowed, i.e. electrons in the valence band at the surface have a higher energy than the empty states in the conduction band above the fermi level in the bulk source. The subthreshold region is therefore expected to be governed by point tunneling, which has a much earlier on-set compared to line tunneling [159]. The standard view of BTB line tunneling is therefore not consistent with the results presented here.

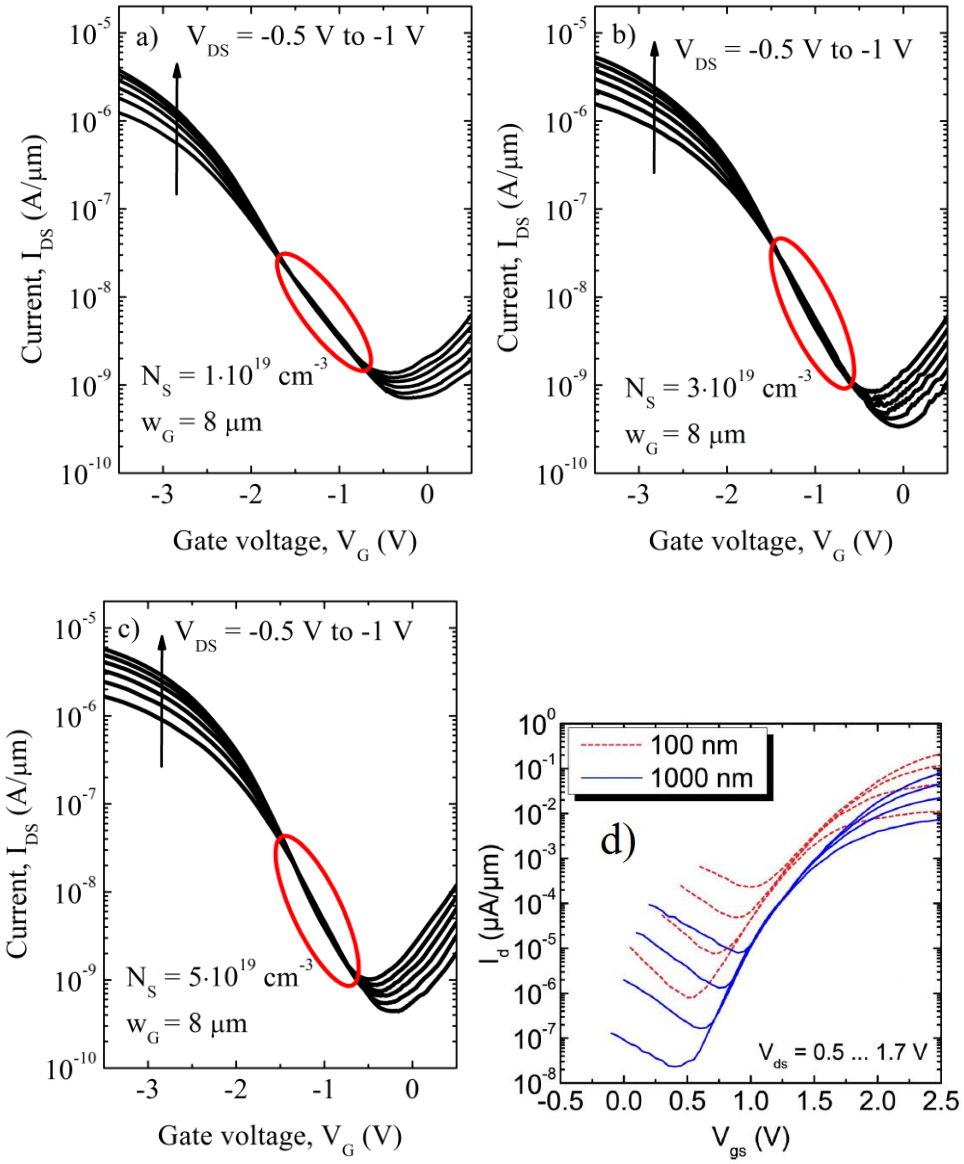

Figure 35 Transfer characteristics from sample with source doping concentration. **a)** $N_S = 3 \cdot 10^{19}$ cm^{-3}, **b)** $N_S = 3 \cdot 10^{19}$ cm^{-3} and **c)** $N_S = 3 \cdot 10^{19}$ cm^{-3} at different drain-source biases. The subthreshold region (indicated) of all TFETs can be seen to be weakly influenced by V_{DS}. **d)** Transfer characteristics taken from the n-channel Si/SiGe line-tunneling TFETs presented by Schmidt et al. [84]. These devices show a similar subthreshold characteristics as those shown here.

In Figure 34b it could be seen that the SSes exhibit a strong temperature dependence. The SSes demonstrate a close to linear relationship with respect to temperature in the temperature range investigated. A strong temperature dependence is inconsistent with BTBT, and indicates the involvement of a process driven by thermal activation. The linearity in the semi-log scale, weak V_{DS} dependence and strong temperature dependence are all not consistent with ideal TFET characteristics, and therefore raises some questions about the current transport mechanism in the subthreshold region.

A possible mechanism which could explain the behavior is the two-step TAT process shown in Figure 36b. A valence electron in the gate-source depletion region is thermally exited into a trap located at, or close to, the Ge/oxide surface, i.e. SRH generation (blue arrow). Due to band bending of the gate field, the energy level at this trap state is above the energy level of the empty states in the conduction band. The exited electron can therefore tunnel from the trap state and into the conduction band (green arrow). The expected nature of this type of process fits well with the observed IV subthreshold characteristics of the TFETs.

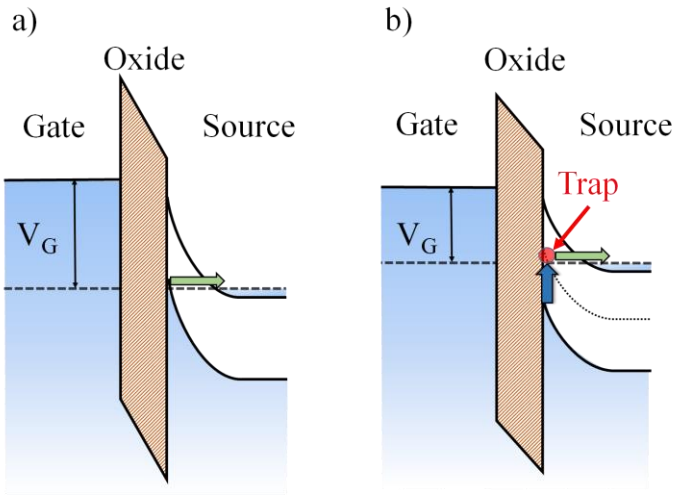

Figure 36 Schematic band diagrams of the gate-source MOS capacitor. a) At high gate bias the energy bands are bended to the extent that BTBT tunneling is activated, requiring a high gate bias. This type of tunneling is referred to as line tunneling. b) Line tunneling of an electron which has been thermally excited (SRH process) into a trap state. This type of process has a stronger temperature dependence than a), and an earlier onset as less band bending is necessary.

It would demonstrate a distinct temperature dependence, due to the thermal excitation process. It would also show line tunneling character with a weak V_{DS}-dependence, since the process takes place outside the pin depletion region. Unlike line tunneling involving a single BTBT process (Figure 36a), this process will have an earlier gate bias on-set. This is because less band bending is required to activate tunneling. It could hence contribute to current flow at relatively weak gate fields. The similarity of this type of process with the GIDL mechanism in the gate-drain overlap region discussed above should here be recognized.

Assuming that the SS is influenced by the trap-assisted line tunneling process described above, the difference between the three samples can now be explained. The gate voltage for a n-MOS capacitor is in the classical model given by [31]:

$$V_G = V_{FB} - V_S - \frac{1}{C_{OX}}\sqrt{2N_S\varepsilon_s q V_s}. \quad (28)$$

Here V_{FB} is the flatband voltage, V_S is the surface potential, C_{OX} is the oxide capacitance and ε_S the semiconductor permittivity. A TAT line tunneling process will have an onset voltage. This voltage corresponds to V_G when the surface potential has reached an energy level for which tunneling is allowed. As midgap traps are the most effective generation centers, the onset voltage can be estimated by replacing V_S in (28) with $E_G/2$. The last term in (28) represents the voltage drop across the oxide, and it can be seen that an increased source doping leads to a later onset, as the magnitude of this term increases. This is opposite to that of point tunneling in TFETs, where increased source doping leads to an earlier onset. Using rough estimates for the parameters in (28) and $V_S = E_G/2$, a larger difference between the onset voltage, $V_{G,onset}$, and the averaged $V_{G,min}$ of the samples results. This can however be explained by the fact that the position of $V_{G,min}$ is not determined by the onset of TAT line tunneling alone, but also the ambipolar branch. It can be noted that, when inserting $V_S = 120$ meV, the differences are in good agreement. The observed difference in position of $V_{G,min}$ with respect to gate voltage between the Ge TFETs can be said to agree qualitatively with this assumption.

Increased doping leads to higher fields inside the semiconductor, which increases the tunneling probabilities and hence the tunneling current. As a consequence, line tunneling currents exhibit steeper subthreshold characteristics with increased doping concentration. In the respect of onset behavior of line tunneling TFETs, the results presented here is in qualitatively agreement with the semi-classical simulations of gate-on-source only-Si n-channel TFETs presented in [160]. Simulated transfer characteristics from that study are reprinted here and shown in Figure 37b.

In Figure 37a averaged transfer characteristics of the three samples are plotted with adjusted gate voltage. The gate voltage was adjusted by subtracting the averaged gate voltage corresponding to the minimum drain current, $V_G^* = V_G - V_{G,min}$. Although this kind of manipulation of the characteristics might seem hand-waving, this could be accomplished technologically by for example adjusting the gate metal work function for each sample. By altering the gate metal-semiconductor work function difference, the flatband voltage can be adjusted corresponding to the averaged V_G (min) plotted in Figure 31a. Although, a steeper onset behavior is achieved with increasing source doping, a stronger saturation of the drain current can also be seen. This leads to similar drain currents at higher negative gate biases for the samples. Although the averaged drain source current is higher for the TFET with

$N_S = 5 \cdot 10^{19}$ cm^{-3}, the overlapping of the error bars, indicating the standard deviation, shows that this difference is not significant.

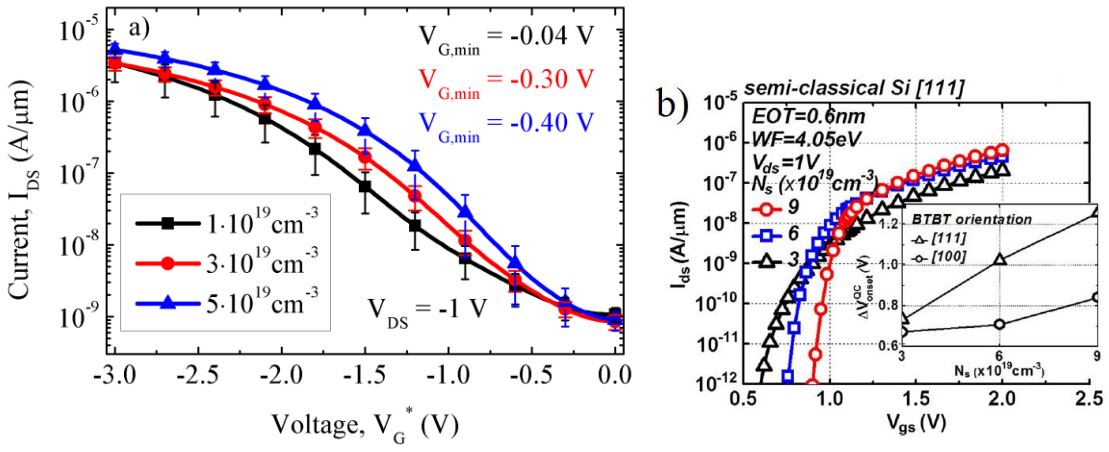

Figure 37 a) Averaged transfer characteristics as a function of adjusted gate voltage for the three different samples. The gate voltage was a adjusted by subtracting the gate voltage corresponding to the averaged minimum drain current, $V_G^* = V_G - V_{G,min}$. **b)** Simulations of transfer characteristics taken from the gate on source only Si TFETs presented by Kao et al. [160]. These simulations show a similar shift in tunneling onset voltage with increased source doping.

5.3.4 Influence of Source Doping Concentration on Drive Current in Germanium P-Channel Tunneling Field Effect Transistors

Figure 38 shows the averaged drive current, $I_{ON} = I_{DS}(V_G = -3.5\ V)/w_G$, of the samples. The difference between the samples is non-significant, and contrary to simulations [88, 160], no observable effect of source doping concentration on I_{ON} can be distinguished. Line-tunneling has been proposed to dominate over point tunneling in devices with source gate overlap at higher gate voltages [159]. All three Ge TFETs presented here have a 100 nm top Ge source layer with $N_D = 1 \cdot 10^{20}$ cm^{-3} above the 100 nm layer with doping N_S (see Table 5). Due to the high doping concentration, the starting assumption was that this region is largely unaffected when a V_G-bias is applied. If, however, line tunneling in this region stands for the dominating contribution to I_{ON}, the explanation for the comparable I_{ON} for all TFETs could lie here. A trade-off between the contributions of line and point-tunneling for different source doping concentrations could also result in similar drain currents at high negative gate bias. Another trade-off with respect to source doping is between the increased tunneling probabilities and reduced availability of electrons, which is introduced by degeneracy.

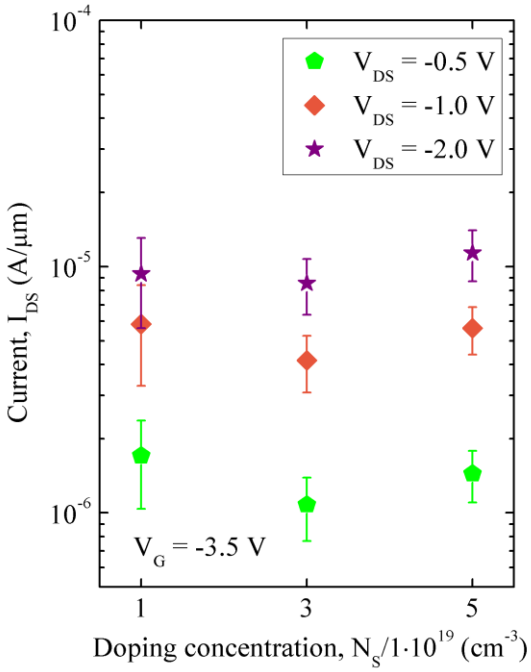

Figure 38 Averaged I_{ON} as a function of N_S for different V_{DS}-biases. No significant difference between the samples can be distinguished.

To better assess the effect of source doping concentration on the BTBT current, a broader doping concentration range than presented in this experiment is suggested for further research. An experimental series varying the thickness of the source layer for a fixed source doping would also be interesting. This could give answers with respect to the nature of line tunneling and point tunneling, and their respective contributions. When increasing the thickness of the source layer, the line tunneling component should increase, while the point tunneling component should remain unchanged. Given the vertical device geometry, increasing the source layer thickness would have no effect with respect to device area.

5.4 Conclusion

The effect of varying source doping concentration in vertical p-channel Ge TFETs with a gate-source overlap has been investigated. All devices exhibit a perimeter proportional leakage current. Based on temperature measurements, the leakage mechanism is SRH generation at the Ge/oxide surface. The TFETs also demonstrate an ambipolar behavior originating from a trap-assisted gate induced leakage current in the drain region. Steeper subthreshold characteristics was found with increasing source doping ($N_S = 5{\cdot}10^{19}$ cm^{-3}) concentration. This is opposite what is expected for source-channel point-tunneling, but in qualitative agreement with a gate-source overlap line tunneling mechanism. The early onset and temperature dependence of the

subthreshold region, on the other hand, indicate trap assisted line tunneling, involving both SRH generation and tunneling processes. Although steeper subthreshold characteristics is obtained with increased source doping, an earlier saturation leads to similar I_{ON} between the samples. Contrary to results from published simulation studies, no effect of source doping concentration on I_{ON} could be distinguished between the doping levels investigated. In this respect no advantage in reducing the source doping concentration for improving the device performance, as suggested by some, could be proven. Suggestions for further work is to investigate a broader doping concentration range and varying the source layer thickness.

Chapter 6 Source Doping Profile Tuning in Germanium P-Channel Tunneling Field Effect Transistors through Molecular Beam Epitaxy Antimony Pre-Buildup

6.1 Introduction

Compared to other electronic devices, the TFET has especially high requirements for the abruptness of the doping profiles. Due to the strong barrier thickness and field dependence of the tunneling probability, a source doping abruptness of less than 4 nm/dec is needed to maximize I_{ON} [50]. Achieving these kind of doping profiles technologically is challenging. The enabling of growth at low temperatures gives MBE an advantage in achieving sharp doping profiles as well as high doping levels. It avoids profile smearing due to dopant diffusion as might result from other technique requiring high temperature processing steps. With MBE, doping levels high above the solid solubility limit can be achieved [161].

A dominant mechanism for doping profile smearing in MBE is, however, surface segregation. Surface segregation describes the situation when impurity atoms pile up at the surface instead of being incorporated into the crystal. Surface segregation prompts the use of very low growth temperatures. This can have damaging consequences for the crystal quality.

Pre adjusting the adatom dopant concentration on the surface while growth is temporarily arrested, is a technique that has been used to compensate this effect and to realize abrupt and high doping concentration for both Si[89] and Ge[162] systems. This technique, is usually referred to as *pre-buildup*. For Si tunneling diodes, an implementation of this technique has resulted in a peak-to-valley ratio of 3.94 [163]. Recently a study of Sb doped Ge structures grown by means of MBE reported achieving 2-5 nm/dec doping gradients through implementing pre-buildup and low temperature growth[164]. This shows that this technique might be suited for realizing the level of doping abruptness needed in vertical TFETs realized with MBE.

In this chapter a Sb pre-buildup doping is used as a measure to achieve steeper source doping profiles in Ge p-channel TFETs. Through a sample series comprising three samples, the pre-buildup Sb concentration was varied with different ML of adatom concentrations. A reference with 0 ML, and samples with 1/20 ML and 1/10 ML concentrations were fabricated. The effect of Sb ML on the electrical characterization of the TFETs from the three samples is reported. The best result is achieved for the TFET with 1/20 ML buildup concentration, which shows the steepest SS as well as the highest $I_{ON.}$

6.2 Layer Growth and Device Fabrication

Table 6 show the MBE layer sequence of the three Ge p-channel TFETs. The three TFET samples differ only by different pre-buildup adatom concentration, while the rest of the growth and layer parameters were kept unchanged. Adatom pre-buildup concentration was determined by using a pre-calibrated boron flux ($F_{SB} = 1{\cdot}10^{12}$ $s^{-1}cm^{-2}$) for the $N_D = 1{\cdot}10^{20}$ cm^{-3} source doping concentration. The pre-buildup time, t_{pbu}, was then varied from t_{pbu} = 35 s to t_{pbu} = 70 s for the 1/20 ML and 1/10 ML concentrations respectively. The samples have a channel region thickness of $t_{channel}$ = 150 nm, and unlike the TFETs presented so far, no doping gradient was used in the Ge drain region. A constant doping ($N_A = 1{\cdot}10^{18}$ cm^{-3}) was instead used. More details on MBE growth of Ge p-channel TFETs was given in section 2.1. The MBE layer sequence of the samples is given in Table 6.

Table 6 MBE layer sequence for Ge TFETs with varying Sb pre-buildup concentrations.

Layer	Material	Thickness (nm)	Doping concentration (cm^{-3})	Growth temperature (°C)
Source	Si	100	$N_D = 1{\cdot}10^{20}$	330
Source	Ge	100	$N_D = 1{\cdot}10^{20}$	160
Source (Pre-buildup)	Sb	0 ML, 1/10 ML, 1/20 ML	-	160
Channel	Ge	150	-	160
Drain	Ge	200	$N_A = 1{\cdot}10^{18}$	330
Drain	Ge (VS)	100	$N_A = 1{\cdot}10^{20}$	330
Drain	Si	400	$N_A = 1{\cdot}10^{20}$	650

The TFETs structures were realized with the GAA-fabrication process described in section 2.2. The oxide consist of a total 60 ALD cycles and an oxide thickness of 9 nm was measured with ellipsometry. No post plasma oxidation was performed for these samples, unlike the previous reported TFETs. Instead a low temperature (T = 350 °C) FGA step was performed after fabrication was finished, as a measure to reduce and passivate oxide charges.

6.3 Results and Discussion

Figure 39a shows the transfer characteristics of p-channel Ge TFETs with varying pre-buildup MLs of Sb. A slope with SS = 300 mV/dec is plotted to indicate the steepness of the devices. In Figure 39b the averaged I_{ON} ($I_{DS}(V_G = -2.5\ V)/w_G$) of five transistors with gate width $w_G = 4\ \mu m$ as a function of drain source voltage are shown. These smallest sized transistors (on the chip) were shown to exhibit the best transistor performance, as leakage current was reduced by area reduction. The TFETs with 1/20 ML Sb pre-buildup show the highest I_{ON}. This shows that an increase in I_{ON} can be achieved by simply tuning the source doping profile through pre-buildup of Sb. This can be a result of a reduction of the effective depletion width within the source, which increases the tunneling probability. However, between the TFET with 1/10 ML Sb and the reference sample, the error bars overlap, indicating minimal significance. This could

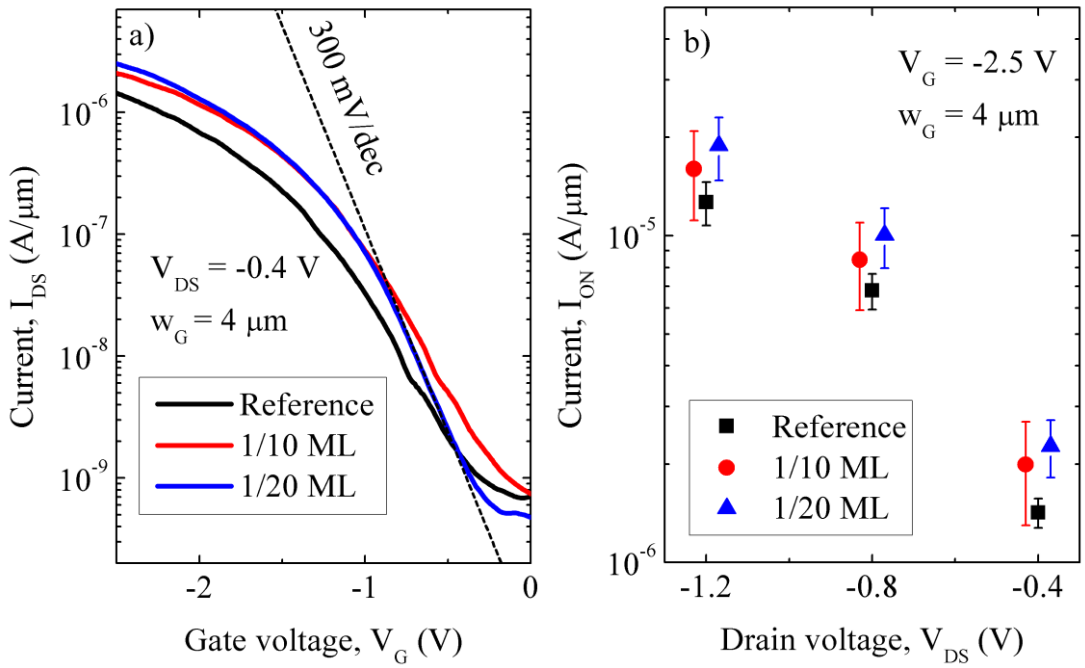

Figure 39 a) Transfer characteristics of Ge p-channel TFETs with varying pre-buildup MLs of Sb. **b)** Averaged I_{ON} as function of drain-source voltage V_{DS}. Horizontal positions of the 1/10 ML and 1/20 ML data points are shifted by ± 30 mV for readability.

indicate the existence of an optimum adatom concentration, as no successive increase of I_{ON} follows the increase of adatom-concentration. A higher Sb adatom concentration should lead to a higher chemical doping concentration at the source interface. All dopant atoms might not manage to occupy substitutional cites, hence the number of free carriers are not necessarily identical to the number of dopant atoms. The electrically active carrier concentration has been shown to strongly deviate from the chemical doping concentration for degenerately Sb doped Ge [111].

An increase in I_{ON} could also originate from increased TAT contributions. If the high doping concentration is resulting in more traps at the channel source interface, induced TAT could enhance I_{ON}. However, this seems unlikely as it would implicit that the sample with the highest pre-buildup dopant concentration would exhibit the highest I_{ON}, which is not the case.

The boost in I_{ON} achieved for the 1/20 ML Sb pre-buildup TFET is not nearly enough with respect to achieving the ITRS I_{ON} requirement ($I_{ON,ITRS}$ = 456 µA/µm)[59]. However, when considering the minor implication it imposes on the device fabrication, the results are non the less intriguing. At the writing, the status of the TFET is that a combination of more performance boosters is needed to make the TFET compatible with the MOSFET with respect to I_{ON}.

Averaged I_{OFF} of the three Ge TFETs as a function of V_{DS}-bias is shown in Figure 40. The leakage current seems to be dominated by tunneling currents, as a strong V_{DS} dependence is demonstrated. An increase of ~ 1.2 dec/V can be seen. Although showing similar behavior for low V_{DS} bias, I_{OFF} for V_{DS} = -1.2 V is higher for the Ge TFETs with Sb pre-buildup, than for the reference. This could be the result of the more abrupt tunnel transition, which for the same reason also leads to higher I_{ON}. Due to that the presented TFETs have a poor electrostatic gate control of the body, DIBT is expected to contribute to elevated leakage currents. A less steep doping profile and thicker tunneling width in the reference sample could suppress this effect.

The high leakage current level, compared to the Ge TFETs presented in Chapter 5 should also be commented. This is in part a result of reducing the channel thickness from 200 nm to 150 nm. It could, however, also be a result of a lower crystalline quality for the samples presented here. From process reliability surveillance, through fabrication and electrical characterization of reference Ge pin diodes, the condition of the MBE system has shown to vary over time.

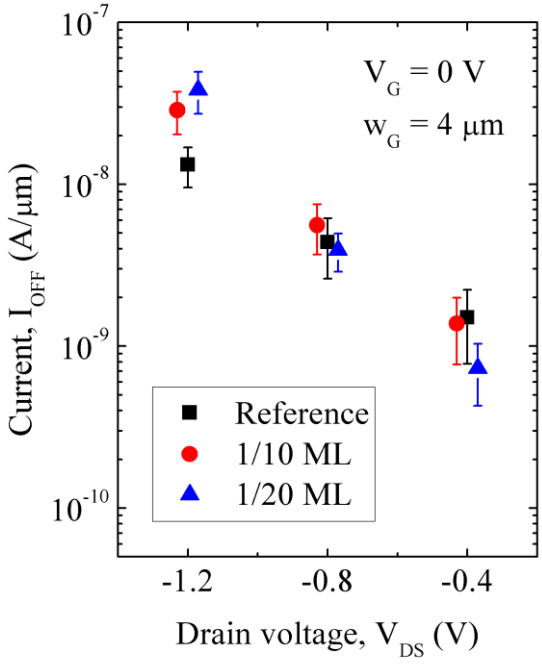

Figure 40 The I_{OFF} of the TFETs with Sb pre-buildup is higher than for the reference TFET at high reverse voltage bias. Horizontal positions of the 1/10 ML and 1/20 ML data points are shifted by ± 30 mV for readability.

The SS of the samples will now be considered. Due to measurement noise, differentiating the drain current and describing the steepness of the TFETs with a point-slope approach proved unreliable. The SS was instead calculated as the minimum V_G needed to change the drain current a minimum of one decade:

$$SS = \frac{\Delta V_G}{\Delta \log(I_{DS})}, \text{ where } \Delta \log(I_{DS}) \geq 1. \tag{29}$$

As for the I_{ON}, the best SS are found for the Ge TFETs with a Sb pre-buildup of 1/20 ML. For V_{DS} = -0.4 V and V_{DS} = -0.8 V, this TFET shows on average 100 mV/dec lower SS than the reference. This can be understood when using the same argument as in the discussion of the I_{ON}. As this sample has a more abrupt source doping profile, a shorter tunneling width and a higher tunneling probability is achieved. The closer the tunneling probability comes to unity, the more effective the band pass filtering becomes[157]. For a lower tunneling probability, the contribution of switching due to the V_G modulation of the junction-electrical field becomes more dominant[39]. For this latter switching mechanism, the SS has a quadratic dependence on V_G, and the SS is only small in a narrow gate voltage range [53]. At a drain voltage of V_{DS} = -1.2 V, the difference between the SS of the three samples is less pronounced. This is due to the higher I_{OFF} for the Sb pre-buildup samples compared to the reference sample, which affects also

the early subthreshold region. The SS of the 1/10 ML sample is similar to that of the reference sample. It could be that the high adatom concentration leads to smearing of the conduction band edge [52], which leads to less steep subthreshold characteristics. This again, suggests that an optimal pre-buildup concentration exists. To establish this, a suggestion for further studies is exploring a greater range of Sb pre-buildup concentrations between 0 ML and 1/10 ML.

Figure 41b shows the SS as a function of decades of drain current for V_{DS} = -0.4 V. As expected for a TFET, and as in contrast to the subthreshold current of a MOSFET, the SS increases as more decades of drain currents are considered. This is due that the SS of a TFET is not independent of V_G. It can be seen that the TFETs with a pre-buildup concentration of 1/20 ML, exhibits the best SS for all decades of I_{DS} considered, $\Delta\log(I_{DS}) \geq 0.5$ dec. Extrapolating the data points in Figure 41b to zero dec with a linear function, gives a rough estimate of the SS point slope, SS_{PS}. The differences between SS_{PS} of the three samples are less pronounced (error bars overlap). If the SS is closely connected to the difference in tunneling probability as argued above, since the difference between the TFET's SS is less when considering a narrow gate voltage range.

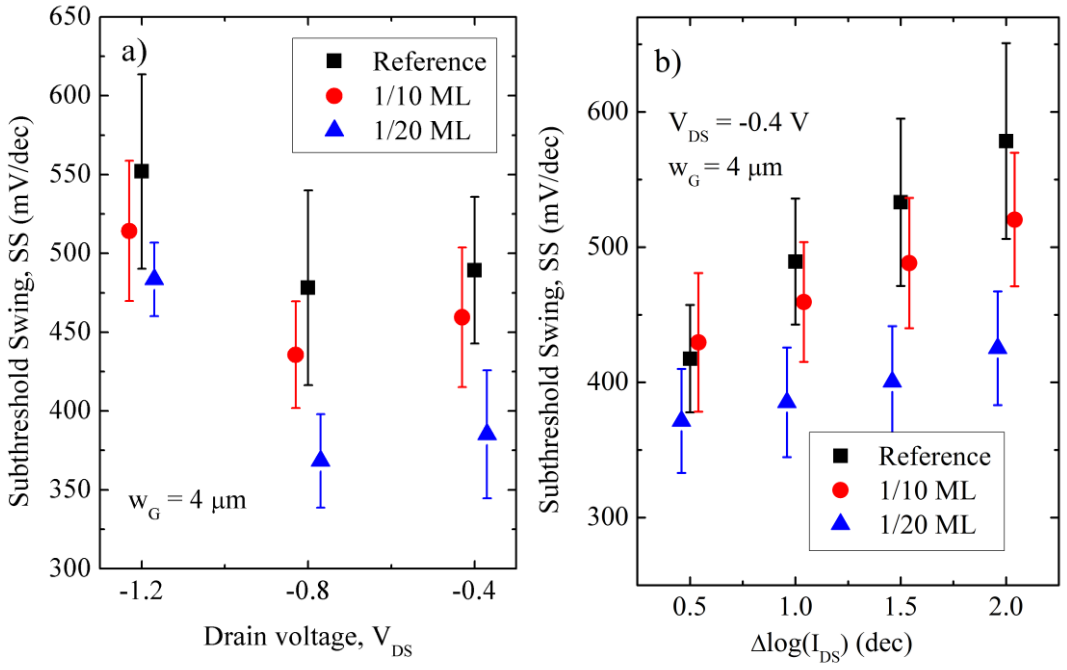

Figure 41 a) Subthreshold swing as a function of drain-source voltage. Lowest SS are found for the transistors with 1/20 ML pre-buildup of Sb. **b)** Subthreshold swing as a function of decades of drain current. The horizontal position of the 1/10 ML and 1/20 ML data points are shifted in both figures for readability.

6.4 Conclusion

A MBE pre-buildup technique of Sb has been investigated as a means to achieve steep source doping profiles in vertical p-channel Ge TFETs. It is seen that for a Sb pre-buildup concentration of 1/20 ML, the TFETs I_{ON} improves with respect to the reference sample. This is explained by the higher tunneling probability which results from the more abrupt source doping and shorter tunneling width. The boost in I_{ON} insufficient to achieve the ITRS I_{ON} requirement on its own, but could easily be implemented in combination with other strategies for boosting the drive current for TFETs. The pre-buildup technique imposes no extra load onto the TFET fabrication process itself.

The steeper source doping profiles for the 1/20 ML Sb is also seen to result on steeper subthreshold swings. This is explained by that the increased tunneling probability improves the band pass filtering.

The results also suggests that an optimal pre-buildup doping exists. The effect of using a higher pre-buildup than 1/10 ML Sb was less commendable, showing comparable device performance with the reference sample in all aspects. A suggestion for further work therefore would be to explore the range between 0 ML and 1/10 ML Sb pre-buildup concentrations in smaller intervals.

Chapter 7 Electrical Characterization of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors Passivated through Post Plasma Oxidation

7.1 Introduction

A major challenge for Ge based field effect devices is the Ge/oxide material system. The direct Ge/high-κ interfaces are known for having a very high D_{it} compared to the Si/SiO_2 system. This can lead to serious device performance degradation. For a field effect transistor, interface traps leads to elevated leakage currents and the electrostatic gate control is weakened. This affects the subthreshold and off-current characteristics of the device. A high D_{it} also reduces the channel carrier mobility and hence the drive currents. Charge trapping effects inside the oxide can also be induced by elevated D_{it} levels. This is because a high D_{it} level allows for easier communication between the charge carriers in the semiconductor and the traps in the oxide [165]. Charge trapping inside the gate oxide lead to hysteresis effects and unreliable device performance. Passivating the Ge/oxide interface is therefore an important task on the road towards Ge based field effect devices as viable alternatives to Si based ones.

The Ge/high-κ interface has however proven difficult to passivate by classical mean like the hydrogen passivation of dangling bonds[2, 124]. A more successful approach seems to be the passivation of the Ge surface through the formation of an interfacial layer (IL) between the Ge and the high-κ material[166, 167]. The criteria of the interfacial is reducing the D_{it}, while at the same time have a thickness of only a few atomic layers so as not to reduce the oxide capacitance and provide a low EOT. Different ILs and synthesis methods are currently being extensively investigated. Some examples are epi-Si-passivation[168] and nitridation[169].

GeO_x is the obvious candidate for passivating the Ge surface due to the natural availability of Ge atoms at the surface. Different methods, like using e.g. ozone [170] , H_2O or air [171],

have been investigating as methods to oxidize the Ge surface. The problems with these methods is the instability of the formed GeO_x under ambient conditions.

In this chapter results of electrical characterizations of $Ge/Al_2O_3/Al$ MOS capacitors are presented, for which a GeO_x layer is formed through a post plasma oxidation step. The plasma oxidation is conducted after first depositing a thin Al_2O_3 plasma protective cap in a remote PEALD chamber. The successive plasma oxidation and Al_2O_3-deposition is performed in the same ALD system, preventing the GeO_x from beeing subjected to ambient conditions.

7.2 Layer Growth and Device Fabrication

The epitaxial growth of Ge was achieved through MBE, the details of which were given in section 2.1.3. Here, p^{++}-Si <100> substrates were used. The MBE growth process started with the growth of 50 nm of Si buffer layer to get a smooth crystalline surface. This was followed by the growth of a 100 nm Ge VS layer. As an active layer, 300 nm Ge was grown on the Ge VS.

After growth the samples were then cleaned with HF and DI-water rinsing. After performing 15 ALD cycles (~1.5-2 nm) which were to serve as a protective cap, a post plasma oxidation was performed with a duration of seven minutes using O_2 (15 sccm) as process gass and a RF power of P_{RF} = 100 W. An Ar-flow (10 sccm) was also introduced simultaneously to support the plasma. The *post* term is referring to that oxidation is performed after the deposition of the cap layer, as opposed to directly onto the Ge surface. After post plasma oxidation, 85 additional ALD cycles of Al_2O_3 deposition where performed. An optical thickness of 11.5 nm was measured with ellipsometry. Directly after gate oxide deposition, Al gate metal was deposited by means of sputtering. After buffered HF treatment of the backside to remove SiO_2, the ohmic Al back side contact was also deposited by means of sputtering. The devices were finalized with photolithography and wet chemical etching (phosphoric acid) of Al contact pads. Details of the Al_2O_2 deposition by the same PEALD system was also given in section 2.2.2.

A reference sample was also fabricated through the same procedure as described above, except that a p^--substrate was used and no post plasma oxidation was performed.

7.3 Results and Discussion

The MOS capacitor devices were characterized via C-V and I-V measurements obtained with a Keithley 4200 Semiconductor Characterization System. For the C-V characteristics an external Keithley 590 C-V Analyzer with a measurement frequency of 1MHz was used for all measurements. The backside contact was kept at ground potential.

7.3.1 Capacitance-Voltage Characteristics of Post Plasma Oxidized Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

Figure 42 shows a dual sweep C-V measurement of the GeO_x-passivated sample using a step bias of 20mV. The characteristic high frequency C-V behavior can be recognized. As will be shown later on, the leakage current in this sweep range is very low. For the calculations it is therefore assumed that the MOS capacitance C_m is accurately described by the measured capacitance C_p. Oxide and semiconductor parameters can be found in Table 7. The parameters were calculated using the equations and theory which can be found in Appendix, after C_{ox} and C_{min} were extracted from the curve. The C-V curve in both accumulation and inversion does not completely saturate to a flat slope. The extracted C_{ox} and C_{min} therefor contain minor errors. To take into account a possible error propagation, the right column in Table 7 show minimum and maximum values when allowing a large ± 5% deviation for the extracted C_{ox} and C_{min} values. The extracted oxide capacitance corresponds to a relative permittivity of $\varepsilon_r \sim 7.7 \pm 0.4$, when using the thickness (d = 11.5 nm) measured for the Al_2O_3 deposited on the Si-reference sample. Data reported in literature for the relative permittivity of bulk Al_2O_3 shows minor discrepancies but usually lies in range $\varepsilon_r \sim$ 9-10 [172, 173]. However, the permittivity presented

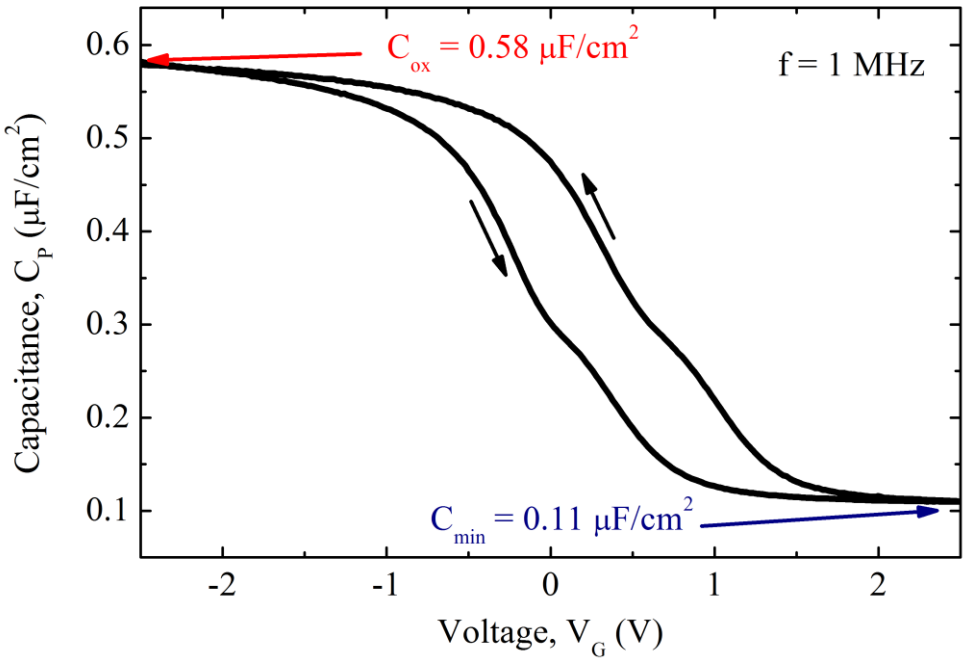

Figure 42 Dual sweep Capacitance – Voltage measurement of the sample subjected to a post plasma oxidation treatment. Arrows indicate sweep direction. The measurement exhibit a relatively large ~ 500 mV hysteresis due to charging and discharging of oxide traps.

here is comparable with results reported for thin Al_2O_3 layers where similar ALD techniques were used [174, 175]. It should be noted that the measured Al_2O_3 thickness is overestimated slightly, as the formed GeO_x layer is not accounted for in the ellipsometry measurement of Al_2O_3 on a Si-substrate.

Table 7 Calculated parameters based on the extracted values of C_{ox} and C_{min}.

Parameter	Calculated value	Min/Max (allowing ±5% deviation of C_{ox} and C_{min})
EOT	5.91 nm	5.63 nm/6.22 nm
N_A	$6.63 \cdot 10^{16}$ cm^{-3}	$5.62 \cdot 10^{16}$ cm^{-3}/$7.84 \cdot 10^{16}$ cm^{-3}
W_{DM} (max)	105.7 nm	98.2 nm/113.7 nm
L_D	18.6 nm	17.1 nm/20.2 nm
C_{FB}	$7.6 \cdot 10^{-7}$ Fcm^{-2}	$7.0 \cdot 10^{-7}$ F/cm^2/$8.3 \cdot 10^{-7}$ F/cm^2
C_{MID} (after [193])	$2.02 \cdot 10^{-7}$ Fcm^{-2}	$2.05 \cdot 10^{-7}$ F/cm^2/$2.05 \cdot 10^{-7}$ F/cm^2
W_{MS}	-0.460 V	-0.455 V/-0.464 V
V_{fb} (pos sweep)	-0.10 V	-0.03 V/-0.17 V
V_{fb} (neg sweep)	0.48 V	0.41 V/0.56 V
ψ_B	0.210 V	0.205 V/0.214 V

The calculated background p-doping concentration is similar to earlier reported Ge work from the same MBE machine [176]. The origin of the background doping has not been established, but as very high temperature is needed for B desorption, chamber memory effect from B is unlikely. It could instead be that point defects in the grown layer (interstitials, vacancies or background impurities) behave like p-type impurities. The Ge-VS is expected to contain many misfit dislocation defects, and as a consequence holds a high trap density and a higher G-R rate than in the overgrown layers. The absence of any LF-response in the C-V curve, indicates that the active layer has a good crystalline quality and that the maximum depletion width is not extending into the Ge-VS. From the calculated depletion width maximum, W_{DM}, a separation of minimum 200 nm between the depletion layer and the Ge-VS is expected. We can therefore also conclude that the main mechanism for getting electrons to and from the inversion layer is through generation-recombination rate inside the depletion layer. It has also been reported that minority carrier transport to and from the inversion layer through diffusion from the bulk starts being the dominant mechanism in Ge for temperatures higher than T > 45°C [177].

Table 8 Calculated effective oxide charges and interface state densities at mid gap.

	Positive sweep	Negative sweep
Q_{eff}	$-2.1 \cdot 10^{-7} C/cm^2$ $(1.3 \cdot 10^{12}\ cm^{-2})$	$-5.5 \cdot 10^{-7} C/cm^2$ $(3.4 \cdot 10^{12}\ cm^{-2})$
D_{itMG}	$7 \cdot 10^{11} cm^{-2} eV^{-1}$	$4 \cdot 10^{11} cm^{-2} eV^{-1}$

The measured C-V curves exhibit a hysteresis, $\Delta V_{Hyst} = 0.58$ V at flatband, seen by the parallel shift of the C-V curve dependent on sweep direction. This hysteresis can be explained by traps in the oxide. Unlike fixed oxide charges, oxide traps do not contribute to a permanent shift, but can be charged/discharged through leakage currents during a sweep cycle. This leads to the observed hysteresis. The rate of charging/discharging depends on the field strength and leakage current level. The dominant trap charging/discharging during a sweep cycle can therefore be expected to take place at the measurement bias extremes, i.e. the start and end biases. The flatband shift V_{FB} and the effective oxide charges, Q_{eff}, were calculated for both sweep directions and can be found in Table 8. With respect to the metal semiconductor work function, the V_{FB} for both sweep directions are shifted to the right, hence the sign of Q_{eff} is negative. The effective oxide charge calculated for the negative sweep is more than twice as the same quantity calculated for the case of positive sweep. This can only be explained by that the oxide traps which are charged/discharged during the sweep are mainly acceptor like (negative when filled, neutral when empty). These are charged at positive gate bias from electrons in the inversion layer in the semiconductor. When performing a negative sweep the traps are charged at the positive start gate bias resulting in a right shift of the C-V curve when the sweep is performed. At negative bias the acceptor traps are emptied, discharged, resulting in a shift in the opposite direction towards negative voltages. One cannot distinguish the fixed oxide charges from the oxide trap charges from the C-V curve alone. However, as Q_{eff} is negative for both sweep directions, it is likely that the net fixed oxide charges are also negative. If this is the case we an O-rich oxide can be expected, as it has been reported that for ALD-Al_2O_3 that O-rich regions have fixed negative charges, while Al-rich regions have fixed positive charges [178]. The possibility that these O-rich region are induced by the post plasma oxidation treatment is also viable possibility.

A density of states at mid gap in the order $D_{it} \sim 5 \cdot 10^{11}\ cm^{-2}\ eV^{-1}$ is calculated for both sweep directions following the method of Jakubowski and Ieniewski [179]. This is almost an order of magnitude higher than reported by Zhang et al. [122], where a similar post plasma oxidation method was used. The D_{it} value presented here is however still lower than the untreated

reference sample presented in the same work, and similar to methods using ozon to oxidize the Ge surface[180]. Another difference between the MOS capacitors reported here and the ones reported by Zhang et al. is the substrate used (Ge-substrate compared to epitaxially grown Ge on Si-substrate).

The bump seen in the C-V measurement curve at $C_M \sim 3 \cdot 10^{-7}$ F/cm^2 will now be discussed. Bumps, or kinks, in the C-V curves are commonly observed for Ge MOS capacitors [181], and are related to a higher D_{it} close to the corresponding energy level in the Ge bandgap. Martens et al. [182] argue that a common pitfall is misinterpreting a large D_{it} at depletion bias as relatively small D_{it} at weak inversion at room temperature, due to their similar visual appearance. The value of C_M, however in this case, does corresponds to a depletion bias. The corresponding $C_S \sim 6 \cdot 10^{-7}$ F/cm^2 is located between the calculated flatband and mid-gap capacitances. This therefore indicates a contribution of large D_{it} in depletion. Based on the energy level and assuming amphoteric traps we can also expect that these interface traps are of a donor type as they are located in the lower half of energy bandgap[183].

The repeatability of the MOS capacitor behavior can be seen in Figure 43a and Figure 43b, which show the change in C-V characteristics when doing three consecutive measurements on the same device. A weak but noticeable degradation of the interface can be seen to results from the measurement itself. The C-V curve experiences a stretch-out. The stretch-out is only seen in the accumulation region above flatband, which would indicate that interface states are generated in the lower half of the energy gap below flatband. The stretch out in accumulation can be observed for both sweep directions, but for positive sweeps also a shift towards positive gate voltages is observed. This shift comes a result of a permanent negative charging and charge storage inside the oxide.

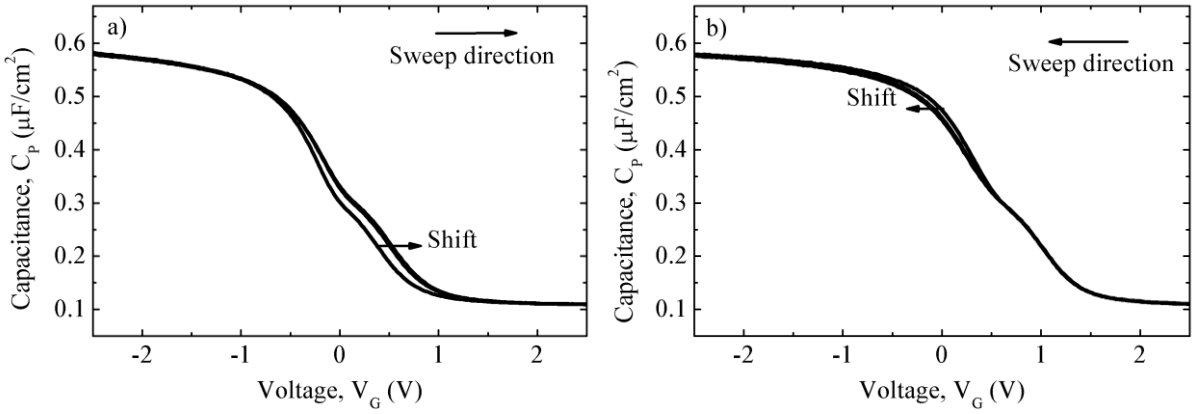

Figure 43 Plots show the C-V-characteristics of three consecutive measurements performed on the same device shows a degradation of the interface for **a)** positive sweep direction and **b)** negative sweep direction. Three measurement were performed before reproducible curves were obtained.

To further investigate the reliability of the MOS capacitor, the devices were measured after being pre-soaked at a high leakage current voltage bias. After performing an initial measurement, consecutive measurements on that same devices were executed varying the duration of the pre-soaking between the measurements. The results can be seen in Figure 44a, which shows the C-V characteristics of two MOS-capacitor devices after being pre-soaked at at a voltage bias of V_{stress} = 4.5 V and Figure 44b which shows the C-V characteristics of two MOS-capacitor devices after being pre-soaked at a voltage bias of V_{stress} = -5 V for different durations, t_{stress}.

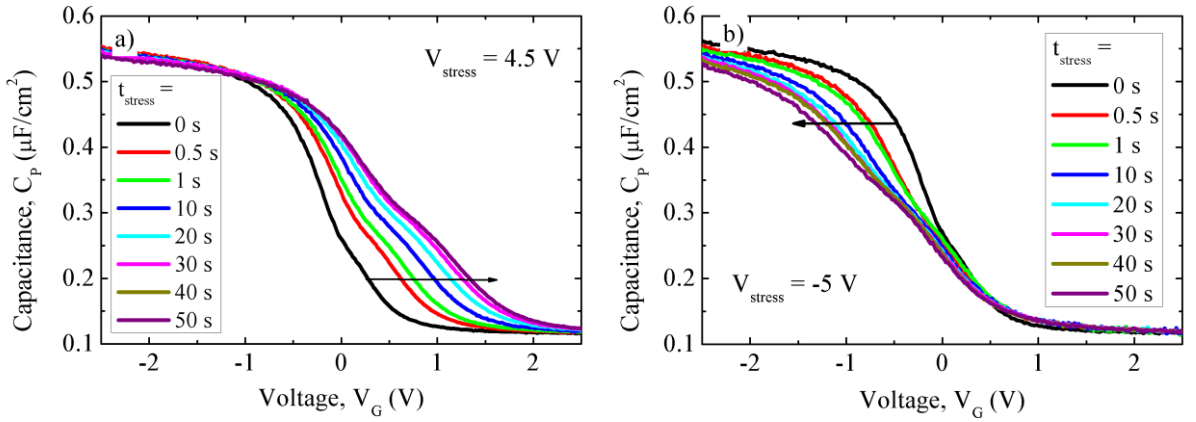

Figure 44 Repeated C-V measurement of a MOS-capacitor after pre-soaking the sample at **a)** a voltage bias of V_{stress} = 4.5 V and **b)** voltage bias of V_{stress} = -5V for different durations. Sweep direction was from negative to positive and the pre-soaking time was increased between each measurement.

The two pre-stressing voltage biases correspond to the same approximate leakage current level ($|I_G| \sim 1 \cdot 10^{-7}$ A/cm^2) which were obtained from I-V measurements. At this voltage bias, FNT is the dominant current mechanism and the current level is approximately two orders of

magnitude higher than what it is at the measurement start and end biases (I-V characteristics is shown in Figure 47 in the next section). Sweep direction is from negative to positive for both devices.

The last measurements for each sample of each measurement sequence (stressed for a total duration of t_{stress} = 151.5 s) are plotted again in Figure 45. This figure clearly shows the degradation of the devices due to the pre-soaking. The stress induced stretch-out points to the generation of surface states, which could be explained by bond breaking at the surface. The calculated $D_{it} \sim 5 \cdot 10^{12}$ cm^{-2} eV^{-1} for the negatively stressed sample, which is one order of magnitude higher than for the initial measurement. The reduction of the oxide capacitance seen in accumulation also reflects a degradation of the oxide quality and reduced oxide permittivity. For the sample stressed with a positive gate bias a clear right shift is seen in addition to the stretch out. As it has been established that we have acceptor traps in the oxide, these traps are charged from the inversion layer at the positive gate pre-soaking voltage. We can also expect that at high leakage current levels, traps are generated due to random defect formation, which in turn may allow further charging. For the negative stressed sample, no clear parallel shift can be made out, since the alteration of the curve seems mainly to be a stretch-out. This further indicates a contribution of negative fixed oxide charges.

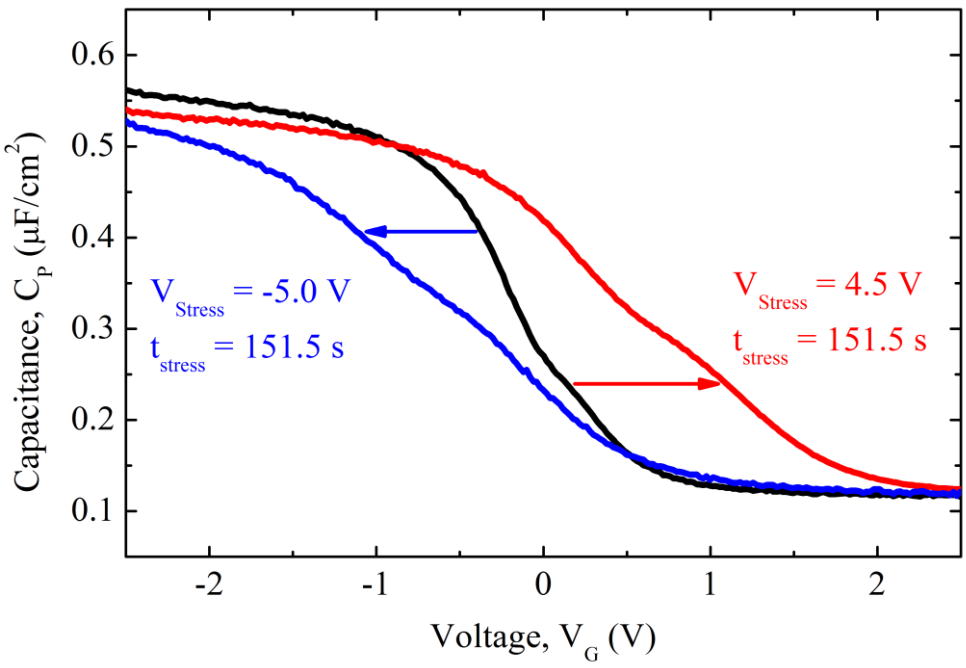

Figure 45 Comparison of an initial measurement and measurement of samples stressed at high positive (red) and negative (blue) leakage current biases.

A comparison of the C-V characteristics from the GeO_x-passivated sample and from a reference sample is plotted in Figure 46. The curves show a qualitatively different behavior, which cannot be explained by the difference in Ge/oxide interfaces alone. In accumulation the capacitance is lower for the reference sample than that of the GeO_x-passivated sample. This contradicts the assumption that a GeO_x layer has been formed for the GeO_x-passivated sample, i.e. forming an effectively thicker oxide. A reason for this could however be due to the different Si substrates used, p^--and p^{++}- substrate for the reference and GeO_x-passivated sample respectively. As the parallel model used neglects series resistance (R_S), the measured capacitance C_p contains an error (e_r) with respect to the actual capacitance C_M. The magnitude of e_r becomes larger as the product of R_S, ω and C_M becomes larger. Equaling the measured capacitance to C_M returns an underestimate of the actual value[184]. In accumulation the capacitance C_M, and hence also e_r, is largest. For a p^--substrate a higher contact resistance is expected, compared to a p^{++}-substrate. With the resistivity specifications given for the Si substrate, we could expect a contact resistance larger than 100 Ω as we have non-sintered Al/Si backside contacts [185] (no FGA was performed). When a compensation of the measured capacitance for series resistance is implemented, it is seen that if $R_S > 129$ a higher accumulation capacitance for the reference sample than for the GeO_x-passivated sample results. Due to the uncertainty of the series resistance, a confirmation of a GeO_x-IL formation cannot be based on the C-V characteristics alone. A LF response can be observed for the reference sample. The LF response is seen by the bump at $V_G \sim 1V$ and a higher value of C_{min}. The inversion layer charge responds to the alternating voltage signal when the minority carrier response time is short with respect to the measurement frequency. This means we have a higher generation-recombination (G-R) rate in the reference sample. A higher G-R rate can only be explained by a greater number of traps in the Ge, as the external factors, measurement temperature and frequency, were kept constant. We can distinguish between two types of traps in the Ge based on their spatial location. These are the interface and the bulk traps, respectively. Considering the MBE growth process for the reference and GeO_x-passivated samples were identical, one could easily conjecture a LF-response to the difference in interfaces and interface trap densities. However, interface traps are usually considered to be inefficient generation and recombination centers in strong inversion, even for high density levels[177, 186]. The GeO_x-passivated sample also seem to have a more pronounced stretch-out compared to the reference sample, which would refute a lower interface trap density. The difference can again be found in the different substrates used for the two samples. Although the MBE growth process was the same for both samples, different substrates from different manufacturers could also yield different substrate qualities.

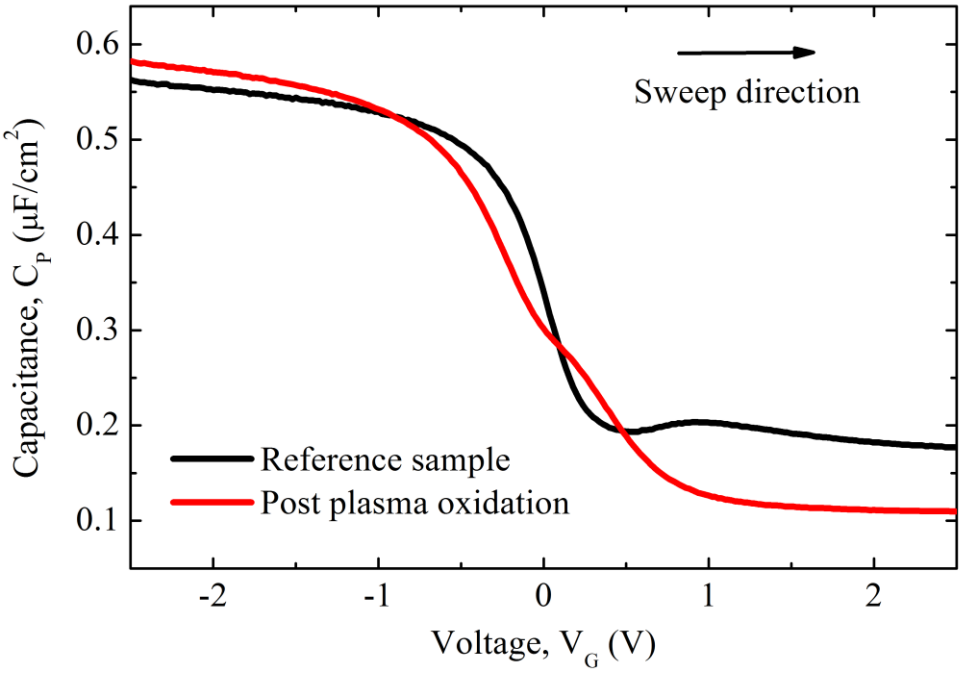

Figure 46 Comparison of a reference sample and the GeO_x-passivated sample. The two samples exhibit qualitative differences. This is expected to originate from the different substrates used.

A difference in initial substrate roughness would be projected onto the MBE grown layers. It has been shown that threading dislocation densities have a strong correlation to surface roughness [187]. A higher threading dislocation density will results in a higher G-R rate and a greater minority carrier response. The LF response can therefore be explained by a higher trap density induced by initial surface roughness. However it cannot be ruled out that interface traps in some way also plays a role and contribute to the observed LF-behavior. Mainly due to the inadequacy of the reference sample, no favorable or unfavorable effect of the GeO_x-passivation can be established based on the C-V characteristics. This information could however easily be obtained by repeating the experiment using a comparable reference sample.

7.3.2 Current-Voltage Characteristics of Post Plasma Oxidized Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

Figure 47 shows the I-V characteristics of the GeOx-passivated sample for negative and positive gate bias sweep, respectively. The devices were biased from $V_G = 0$ V and until catastrophic breakdown for each polarity. The point of catastrophic breakdown is indicated in the figure. The characteristic FNT regions are seen for voltages larger than $|V_G| > 4$ V by the strong voltage dependence, and are also indicated in the figure.

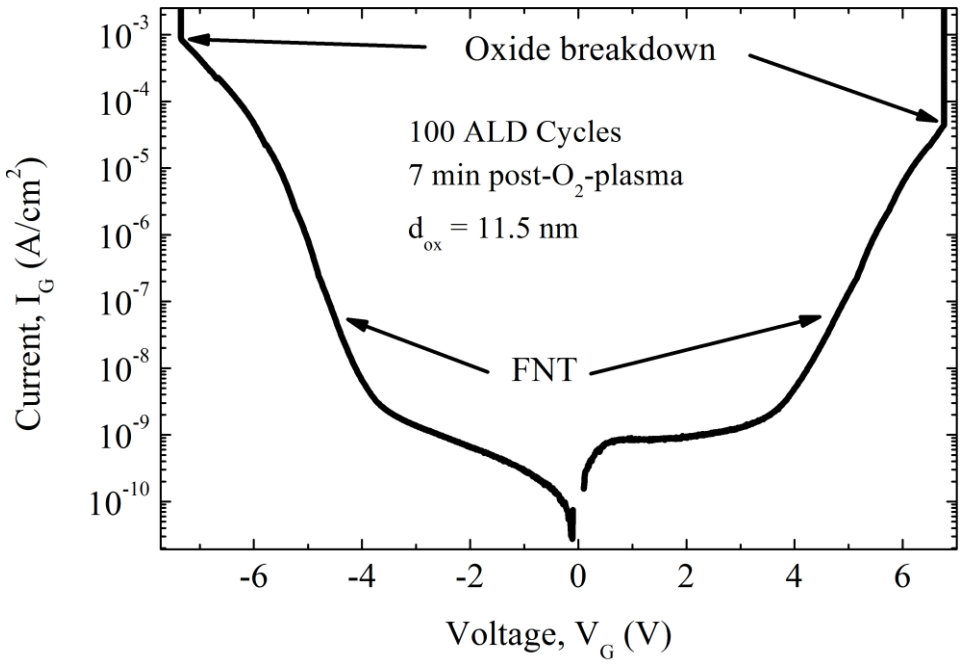

Figure 47 I-V characteristics of the post plasma treated Ge/Al_2O_3 MOS capacitor. The characteristic FNT regions are seen for $|V_G| > 4$ V by a strong field, i.e. voltage dependence.

In Figure 48 the voltage bias at catastrophic breakdown is shown as a function of device area. The average measured breakdown voltages was found to be $V_B = -7.2\ V \pm 0.9\ V$ for negative and $V_B = 6.7\ V \pm 0.6\ V$ for positive bias respectively. This corresponds to a breakdown field of ~ 6 MV/cm, which places it within the range of breakdown fields (5 - 10 MV/cm) of bulk Al_2O_3 reported elsewhere [188]. It is assumed that the mechanism for breakdown is through defect chains. Due to the probabilistic nature of the defect formation, a device with a larger area will have a higher probability of having overlapping defects for the same oxide thickness and defect density [189]. A large area device has a lower breakdown voltage than smaller area devices, since only a single breakdown path is needed to shorten the device. In Figure 48 only a modest area dependence can be seen, i.e. the highest breakdown voltage is observed for the smallest and the lowest breakdown voltage for the largest area devices, respectively. It can also be seen that the breakdown voltage varies with as much as ~1.5 V for one device area. A larger sample size would be needed to confirm with certainty a device area dependency. If the execution time of the measurements were accounted for, the area dependence would also be stronger than seen in Figure 48. When measuring a device, the integration time is automatically adjusted depending on the current level. Longer settling time is needed in the low current regimes compared to the high current regimes, respectively. Small area devices will require a longer measurement time than larger area devices, as the absolute

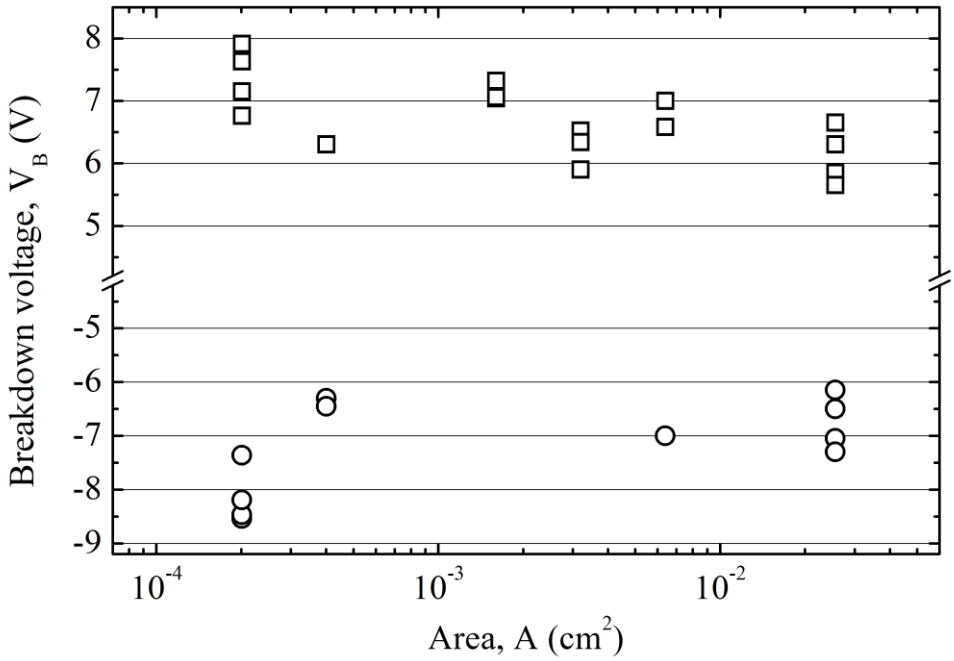

Figure 48 Voltage bias at the point of catastrophic breakdown vs. MOS capacitor device area. Circles are negative bias breakdown, while squares are positive voltage breakdown.

current is lower. It follows that the total charge passed through the device with respect to area, and the amount of stressing, is greater for small area devices.

Figure 49 shows the IV characteristics of the post plasma treated sample and a reference sample with direct deposition of Al_2O_3 on Ge. The post-plasma treated samples show a lower leakage current and a later on-set of the FNT tunneling compared to the reference. Both attributes verify that a GeO_x-IL has been formed. The later onset of almost one volt of the FNT region suggests that the GeO_x layer results in an effectively thicker gate oxide, as tunneling currents are very dependent on the electrical field and barrier width. An effectively thicker oxide would then also explain the reduction of leakage current in the low E-field region. I remind here that this was not observed in the C-V characteristics, but could be explained by the higher series resistance for p^--substrates. A difference in series resistance does however not influence the I-V characteristics for low current levels.

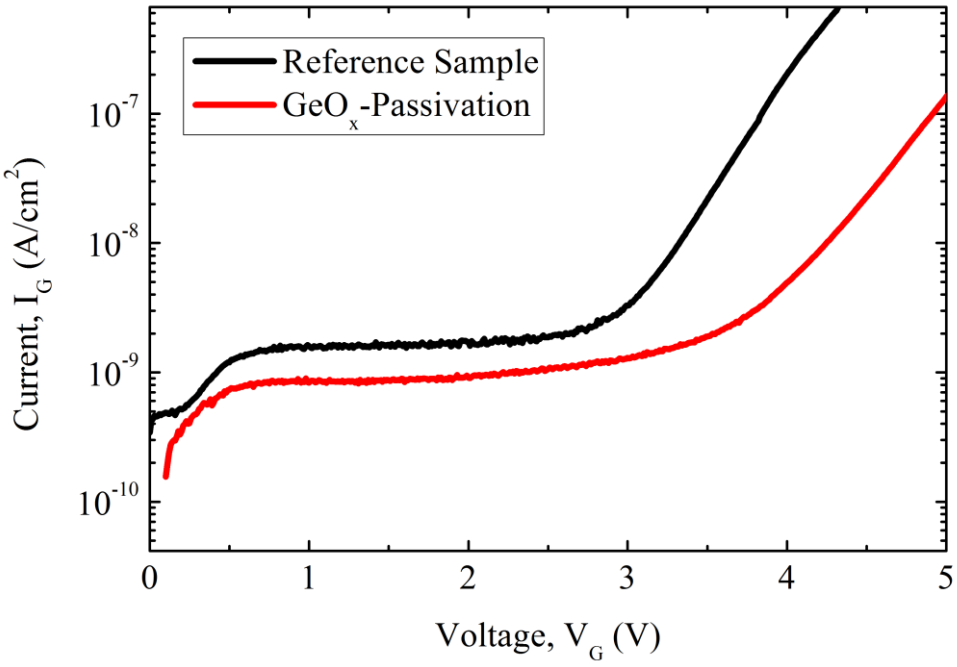

Figure 49 I-V measurement for positive V_G comparing a reference sample with the GeO_x-passivated sample. Both a lower current in the low electric field region, and a later on-set of the FNT is clearly seen for the samples that were subjected to a post plasma oxidation treatment

7.3.3 Temperature Dependency of the Current-Voltage Characteristics of Post Plasma Oxidized Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

In an attempt to determine the carrier transport mechanism through the oxide in the below FNT region, IV sweeps for positive biases were performed at different temperatures. The results are shown in Figure 50 which shows IV sweeps from V_G = 0 V to V_G = 5 V, at different temperatures. A clear temperature dependence can be seen by increasing leakage current with increasing temperature. In the inset of the figure the current for different gate biases is shown in an Arrhenius plot. The extracted activation energies are relatively constant over the low E-field regime (0.12 – 0.13 eV). This indicates a thermally activated process. Tunneling has a strong field dependence, but is essentially independent of temperature. The observed temperature dependence does therefore rule out direct tunneling and TAT as a main transport mechanism through the oxide. This is also to be expected as the oxide thickness is d > 10 nm. The weak temperature dependence of tunneling is also seen by the coinciding of the curves in the FNT region stating at V_G > - 4 V.

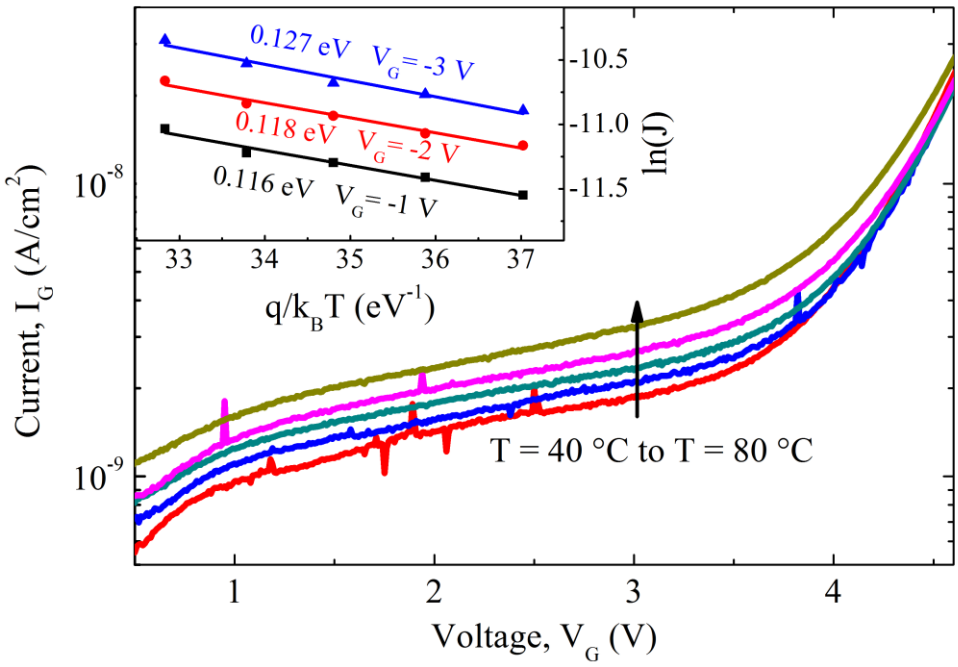

Figure 50 I-V sweeps of the post plasma oxidized sample at different temperature. A clear increase in current with increasing temperature can be seen. Inset shows Arrhenius plot of the current at different gate voltages.

Given the distinct temperature dependence, two main mechanisms are suggested to be the cause: Schottky-emission and Frenkle-poole emission.

Figure **51**a shows the same measurement in a Schottky plot and Figure 51b in a Frenkle-Poole plot. The electric field is approximated by E = V/d. The linear behavior seen in the Schottky plot points to Schottky emission as transport mechanism below the FNT regime. The Frenkle-Poole plot shows no linear behavior. The intercept A_S and the slope B_S extracted from the fits of the Schottky plot are related to the temperature, barrier height, and dielectric permittivity with [31]:

$$A_S=\ln(A^{**}\cdot T^2)-\frac{q\cdot\phi_B}{k_B\cdot T} \tag{30}$$

and

$$B_S=\frac{q^{3/2}}{k_B\cdot T\sqrt{4\cdot\pi\cdot\varepsilon_r\cdot\varepsilon_0}}. \tag{31}$$

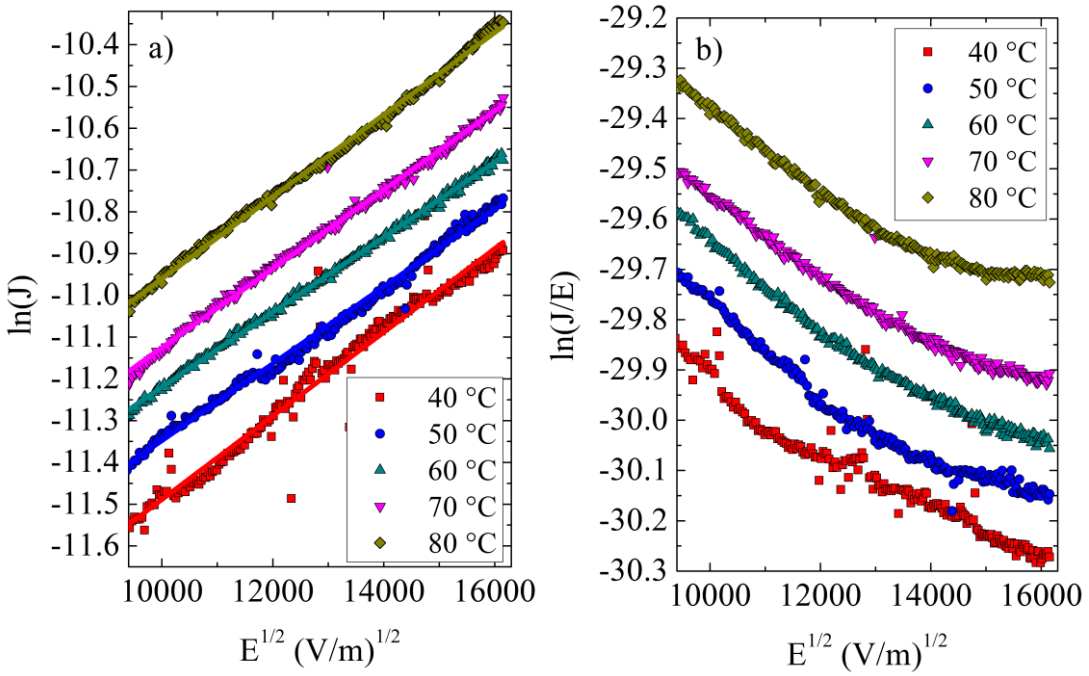

Figure 51 A comparison of **a)** Schottky and **b)** Frenkel-Poole plots of the measured I-V curves. The linearity achieved in the Schottky plot suggests that Schottky emission is the main transport mechanism for the sample for electrical fields below FNT-region.

By doing appropriate fitting one should be able to extract the Richardson constant, the barrier height and the relative permittivity, respectively. However no good fit could be achieved as can be seen in Figure 52 which shows the extracted slopes. The extracted values are hence unreasonable, with for example a relative permittivity of the oxide of $\varepsilon_r \sim 200$. An explanation for this discrepancy could be that the actual electrical field across the oxide is badly represented by E = V/d. This field expression neglects effective oxide charges and assumes that the flatband shift and band bending in the semiconductor is small compared to the applied voltage. As was shown in the C-V characteristics of the sample the effective oxide charges make a significant contribution to the flatband shift. The thickness of the oxide used in the formula is also based on the Al_2O_3/Si test sample measurement which might be deviating from the actual thickness. Another source of error is the charge trapping which takes place during a measurement and the defect formation and degradation which might be expected at high-E-field/high leakage current regimes. As was seen in Figure 44, stressing the device at an even lower bias than the end sweep bias of the I-V measurement, greatly influence the C-V characteristics through a stretch-out and a flatband shift. The stressing is even further intensified by the long integration time needed to obtain a good signal-to-noise ratio. The possibility of increased current only as a consequence of stress induced oxide degradation can also not be disregarded. Taking all this into

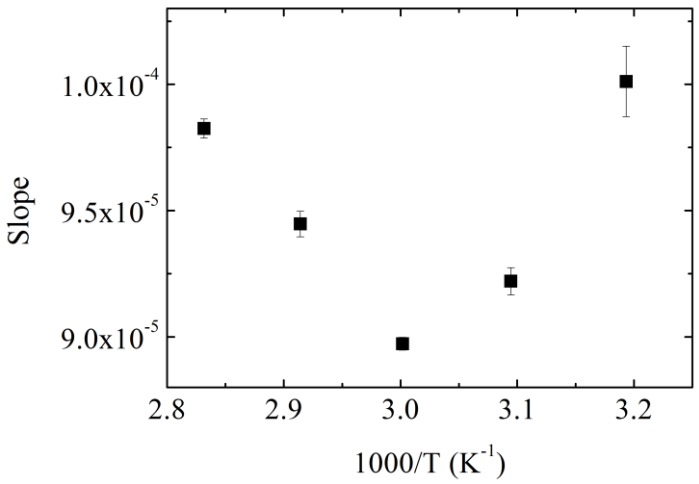

Figure 52 No reasonable linear fit can be achieved of the extracted slopes from the Schottky plots.

consideration a non-linear and complex E-V_G relationship can be expected. Although a single I-V sweep might return a reliable measurement, as seen by the linearity achieved in the Schottky plot, consecutive measurements will not be comparable since the measurement itself changes the initial conditions. The electrical field dependence would have to be adjusted before each measurement to accurately describe the MOS system. As this is difficult to achieve, a better strategy for measuring, where the effect of stressing and charging is accounted for, is needed to further investigate and extract relevant parameters for the transport mechanism in the here reported MOS system.

7.4 Conclusion

High frequency C-V characterization and I-V characterization of Ge/GeO_x/Al_2O_3 MOS-capacitors have been presented. From the C-V characteristics the interface state density at mid-gap was calculated to $D_{it} \sim 5 \cdot 10^{11}$ eV cm^{-2}. A hysteresis, and a shift in the flatband voltage, dependent on measurement sweep directions, is explained by acceptor traps in the oxide. A general parallel shift of the C-V curve towards positive gate voltages indicates fixed negative charges, and can be explained by an O-rich Al_2O_3. These O-rich regions could be due to the post plasma oxidation treatment. Comparing the C-V measurements of the GeO_x-passivated sample and the reference sample a qualitatively difference could be distinguished, with a significant minority carrier response in inversion for the reference sample. This difference is believed to be due to the difference in substrate used as well as different interface state densities. A repetition of the experiment implementing a more comparable reference sample would help to answer these questions. Stressing the device at a high leakage current bias is seen to strongly

degrade the surface by leading to a pronounced stretch-out and reduction in oxide capacitance. Temperature dependent I-V characteristics indicate a Schottky emission process as the main transport mechanism through the oxide, due to the linear behavior observed in the Schotkky plot. The degradation and flatband shift due to stressing is however thought to be the reason why no reasonable fitting parameters could be extracted from the same I-V measurements. A more sophisticated method of measurement and analysis is needed to extract system parameters.

Chapter 8 Impact of Sulfur Passivation on the Electric Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

8.1 Introduction

Sulfur (S) has emerged as an attractive candidate for passivation of the Ge surface [167, 190, 91]. Experiments have suggested that the Ge surface can be passivated by S atoms occupying bridge positions between adjacent surface Ge atoms[191]. S-passivation has also been implemented in the fabrication scheme for GeSn based field effect devices [90]. Passivating Ge and GeSn through sulfur is, however, relatively new with the first experiments performed less than a decade ago [91]. More experimental studies are therefore called for, in order to better assess its potential as a standardized passivation method for Ge based devices.

In this chapter, S-passivation of the Ge surface is studied through the fabrication and electrical characterization of Ge/Al_2O_3 MOS capacitors. The S-passivation of the Ge surface is achieved through a simple aqueous Ammonium sulfite solution treatment performed before Al_2O_3 oxide deposition by a PEALD system.

The S-passivation is seen to reduce the leakage current for low electrical fields, below the onset of FNT. The C-V characteristics reveals that this does not come at the expense of a thicker equivalent oxide thickness. Compared to a reference sample the C-V characteristics of a S-passivated sample show reduced hysteresis and a right shift of the C-V curve.

8.2 Layer Growth and Device Fabrication

The epitaxial growth of Ge was achieved through MBE, details of which was given in section 2.1.3. A p^--doped Si (100) substrate was used. The MBE growth process started with the growth

of 50 nm of Si buffer layer to get a smooth crystalline surface. Then followed the growth of a 400 nm Ge layer. No Ge VS was formed and 400 nm Ge was grown directly on the Si-buffer.

To investigate the impact of S-passivation on the Ge/Al_2O_3-system, three different surface treatments were performed. One sample was chosen as a reference sample, for which only cleaning and removal of native oxide through rinsing in diluted HF and deionized water was performed. The two other samples were subjected to the same native oxide removal treatment and were then immersed into a 35% aqueous Ammonium sulfite ($(NH_4)_2SO_3$) solution at 70 °C for a duration of 15 min for the one sample and 30 min for the other, respectively.

After the sulfur treatment the samples were loaded into a remote PEALD system (see section 2.2.2 for more details) and 100 ALD cycles were performed. A Si/Al_2O_3 sample was added to the deposition process as a reference. With ellipsometery an optical oxide thickness of this sample was measured to be d ~ 14.7 nm. With respect to Chapter 7 this oxide is thicker even though the same number of ALD cycles were performed. This is expected to be due to the time between the two experiment and variance in system chamber conditions.

Directly after gate oxide deposition, the Al gate metal was deposited by means of sputtering. After buffered HF treatment of the backside to remove SiO_2, the ohmic Al back side contact was also deposited by means of sputtering. The devices were finalized with photolithography and wet chemical etching (phosphoric acid) of Al contact pads.

8.3 Results and Discussion

The MOS capacitors devices were characterized through C-V and IV measurements obtained with a Keithley 4200 Semiconductor Characterization System. For the C-V measurement the integrated 4210 CVU-instrument was used. As all samples were grown on p^--substrates, a measurement frequency of 100 kHz was chosen to minimize the error due to series resistance at higher measurement frequencies. A step length of 50mV was used and the backside contact was kept at ground potential.

8.3.1 Influence of Sulfur-Passivation on the Capacitance-Voltage Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

Figure 53 shows a dual sweep C-V measurements of the three samples. The voltage sweep direction is indicated by arrows in the graph. The relatively low measurement frequency used leads to a considerable minority carrier response, seen by the increase of the measured capacitance in inversion. The samples were also grown directly on the substrate and have no

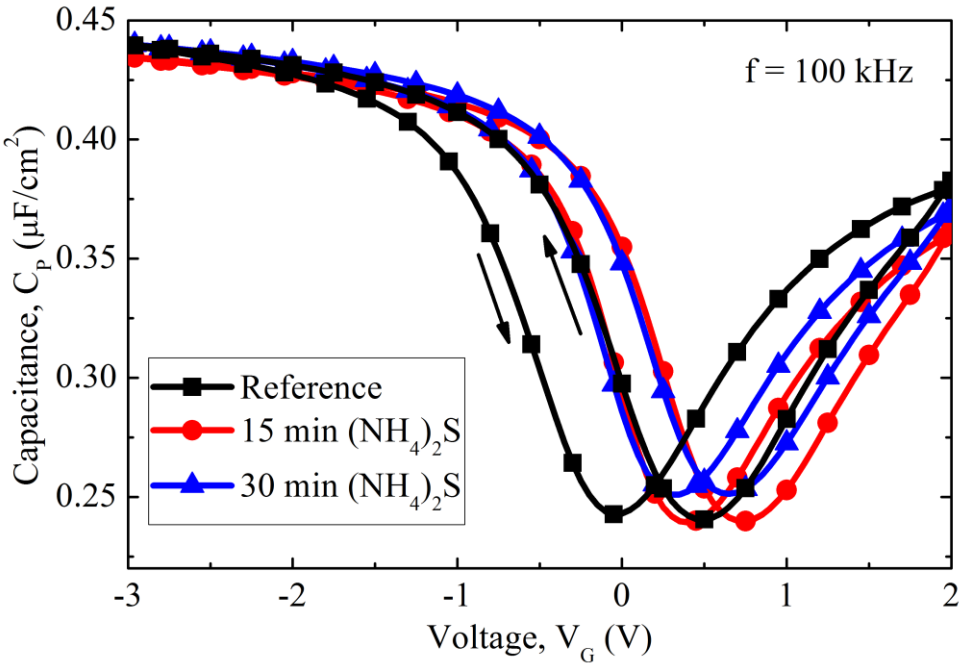

Figure 53 A comparison of the dual sweep C-V measurement of the reference sample (black line) and the 15 min treatement (red line) and 30 min treatment (blue line) S-passivated samples, respectively. The S-passivated samples exhibit a lower hysteresis and are right shifted compared to the reference sample. A measurement frequency of 100 kHz was used. Arrows indicate sweep directions for the reference sample.

Ge-VS. A high trap density in the Ge, due to misfit dislocations, is expected to lead to increased minority carrier response. The S-passivated samples exhibit a considerably smaller hysteresis, $V_{Hy} \sim 0.28$ mV compared to $V_{Hys} \sim 0.47$ V for the untreated sample. Reduced hysteresis correlates to a reduction in charging/discharging of oxide traps during a sweep cycle. The capacitance in accumulation however reveals that the reduced charging/discharging does not come at the expense of a larger EOT. The EOT of all samples are EOT ~ 7.8 nm. A reduction of charging/discharging can therefore be explained by a reduction in the number of oxide traps in the atomic layers of the Al_2O_3 close to the Ge interface. We can expect that a S-passivated surface might influence the defect formation, i.e. trap formation, in the first deposited layers, as the atomic and electronic structure at the surface is changed. As additional layers are deposited, the information of a difference in atomic surface structure is lost and process related defect generation should become equal for both the untreated and the S-passivated samples, respectively. A reduction of oxide traps resulting from the S-passivation can therefore only be a consequence of a reduction of oxide traps located close to the interface. Another possible explanation for the reduced hysteresis is not the reduction of traps in the oxide, but a reduced interface trap density. Since interface states can exchange charges with oxide traps[165], a reduction of interface traps, reduces the electrical communication between the interface and

oxide traps. Reducing the interface traps therefore quenches this charge exchange process and reduces the hysteresis. Due to the minority carrier response in inversion, the HF method for extracting the interface state density cannot be applied.

In addition to a smaller hysteresis, a right shift of the C-V curves compared to the reference sample is seen for both S-passivated samples. This is similar to the findings of Frank et al[91] in their S-passivated HfO_2/Ge MOS capacitors. They assign the right shift to a reduction of positive fixed charges. A right shift can also indicate increased negative fixed charges. In Chapter 7 it was argued that we have mainly negative fixed charges in the ALD Al_2O_3. Distinguishing between the two possibilities is, however, difficult to establish from C-V measurements only, as LF-response prevents calculating the flatband voltage through the normal flatband capacitance method[123].

The repeatability of the C-V characteristics of the devices can be seen in Figure 54. All samples show a left shift of the C-V curve when consecutive C-V sweeps are performed on the same device. A permanent charging or discharging is hence taking place. The largest shift is between the first and second measurement, while an unchanged curve is obtained after the fourth measurement. Also in this type of measurement the S-passivation seems to reduce the charging/discharging, as the magnitude of the shift between the first and fourth measurement is lower for the S-passivated samples. The smallest shift is seen for the 30 min S-passivated

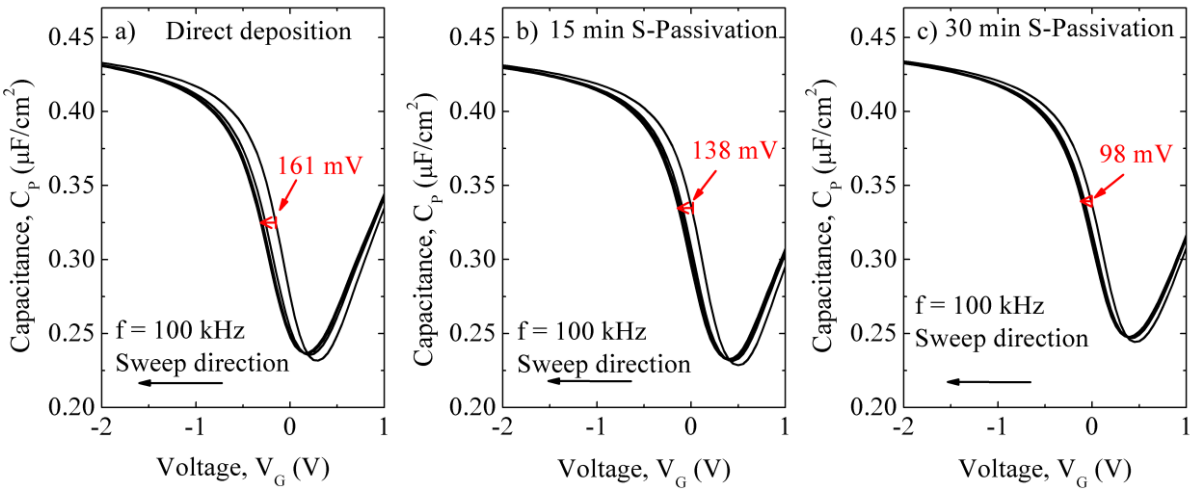

Figure 54 By repeating a negative sweep C-V-measurement on the same device, charging is seen by a left-shift of the C-V-curve for all samples. **a)** reference sample, **b)** 15 min S-passivation and **c)** 30 min S-passivation. The magnitude of the shift is less for the S-passivated samples than for the reference sample

sample. Except for the small difference in shift, the C-V measurements show no significant difference between the two S-passivated samples.

8.3.2 Influence of Sulfur-Passivation on the Current-Voltage Characteristics of Germanium/Aluminum Oxide/Aluminum Metal-Oxide-Semiconductor Capacitors

Low current measurements are very sensitive to noise interference and several precautions had to be made to ensure successful measurements. To allow spurious currents to decay, IV measurements were performed after sufficient waiting time after power-up and after changing connection. A small voltage step size of 5 mV and a long measure integration time was needed to achieve a good signal-to-noise ratio.

Figure 55a and Figure 55b shows the IV characteristics for negative and positive V_G before the onset of Fowler-Nordheim Tunneling (FNT), $|V_{FN\text{-}Onset}| \sim 4V$. A difference can be seen for low voltages ($|V_G| < 1V$) between the S-passivated samples and the reference sample for both negative and positive V_G. The current of the reference sample is higher than for the S-passivated samples, with as much as a factor 2 at $V_G = 0.5$ V. As for the reduction of hysteresis in the C-V characteristics, the reduction in leakage current does not come at the expense of an increased EOT. This again points to a successful reduction in transport of charge carriers due to surface

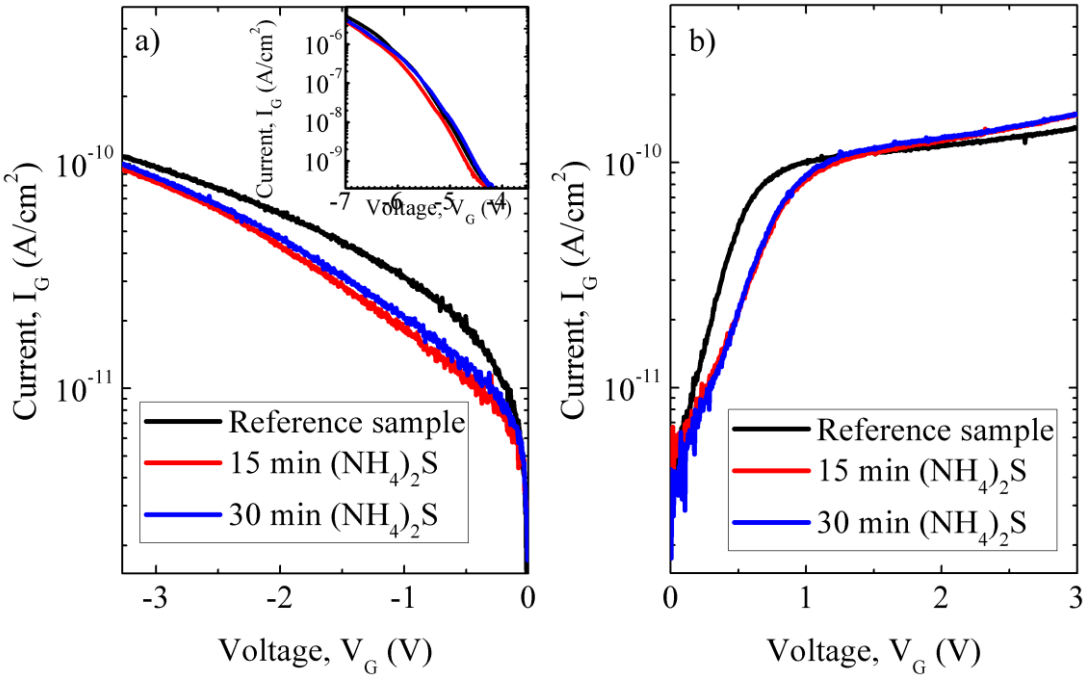

Figure 55 Leakage current density of the three samples for a) negative and b) positive V_G. A lower leakage current is observed for samples with S-passivation. The inset in a) shows the FNT leakage current for negative gate bias.

passivation. In the FNT region, (see inset Figure 55a), all three curves coincide. This can be explained by that FNT has a strong oxide thickness dependence, and interface states plays an insignificant role in the carrier transport. As with the C-V characteristics no clear difference between the 15 min and 30 min S-passivation treatment can be distinguished.

Comparing Figure 55a and Figure 55b, which are plotted in the same scale, a very distinct asymmetry and different behavior dependent on sweep direction can be distinguished. For a negative gate bias the current seems to be continuous, while for a positive gate bias two distinct regions can be recognized. For low voltages (V_G < 1 V) a steep increase is seen, before saturating towards a region with weaker V_G dependence. This behavior is qualitatively equal for the S-passivated and reference samples. To try to understand this asymmetry, the different direction of electron transport for the different gate polarities is now reviewd. For a negative gate bias the Fermi level at the metal gate is raised with respect to the Fermi level in the bulk Ge. The direction of electron transport is therefore from the gate and into the Ge. In Figure 56 one can see that transport in this direction is in qualitatively agreement with a Schottky emission process, assuming that the electric field is E ~ V_G/d.

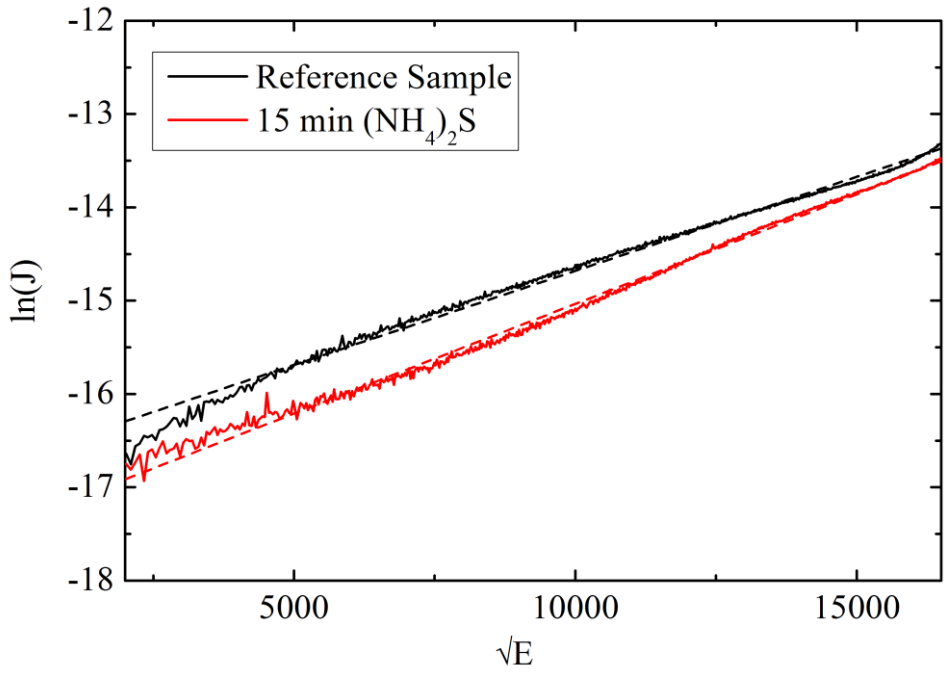

Figure 56 Schottky plot of the reference sample and S-passivated sample (15 min), for negative sweep direction. Reasonable linear fits (stapled lines) can be made, which indicates Schottky emission.

For positive gate bias, electron transport through the oxide is from the germanium surface and into the gate metal. Regardless of how electrons are transported through the oxide this travel path necessitates first the availability of free electrons in the Ge at the Ge/oxide interface. If we use the negative sweep C-V measurements (see plots in Figure 54) as a starting point, we can

see that at zero gate bias the MOS system is in depletion for the reference sample and in accumulation for the S-passivated samples. In either case as a positive gate bias is applied, the depletion layer will start to expand. We can assume that the dominant mechanism for getting minority carriers to the surface is generation within the depletion region[177]. The current will therefore increase as a result of an expanding depletion region and the increased availability of electrons at the surface. It has been reported that inversion leakage currents in Si/high-κ p-type MOS capacitors are dominated by the generation-recombination current within the depletion region [192]. At the onset of strong inversion the electrons at the interface however shield the depletion layer from expanding. As a consequence the leakage current saturates. This fits well with the bottom plots of Figure 55 where a saturation to a flat slope is observed for (V_G > 1 V) at which point all samples are driven into strong inversion. The right shift of the C-V curves resulting from the S-passivation can now also be used to explain the reduction of leakage current in this low E-field regime. For a given weak positive bias, due to the shift of threshold voltage, the depletion layer width has expanded further into the bulk for the reference sample than for the S-passivated sample. The number of available electrons is hence greater for the reference sample. A greater gate voltage bias is needed to bring the S-passivated samples into strong inversion and they will saturate at a larger gate bias than the reference sample. For higher E-fields (V_G > 2 V) all samples are in strong inversion and the availability of excess electrons at the surface only depend on the generation rate inside the depletion region. As Ge quality is comparable for all samples, i.e. equal generation rate, all samples show similar I-V characteristics.

8.4 Conclusion

The effect of sulfur passivation of Ge surface has been investigated through the electrical characterization of Ge/Al_2O_3 MOS-capacitor. Both I-V and C-V characteristics confirm the formation of an interfacial S-layer through the successful reduction of hysteresis and reduction of leakage current in the low E-field region. The measured oxide capacitance also reveal that this does not come at the expense of a thicker EOT. The reduced hysteresis is explained by a reduction of traps, either in the Al_2O_3 close to the Ge interface or at the interface itself. The S-passivation is also seen to cause a right shift of the C-V curve, which could be due to reduction of fixed oxide charges, or increased negative fixed charges. In the I-V characteristics for positive gate voltages, the leakage current seems to correlate with the availability of electrons at the Ge surface. This in turn depends on the generation rate within the depletion region. The right shift observed in the C-V curve leading to a shift of the threshold voltage can therefore be

used to explain the reduction in leakage current for low E-field regime of the S-passivated samples. Similarly it can be used to explain why no effect of the S-passivation can be seen for higher E-fields. No significant influence of the duration (15 and 30 min) of the S-passivation treatment could be observed in either C-V or I-V characteristics. It is therefore believed that the treatment duration can be further reduced and still achieve the favorable effects presented here.

In conclusion, like similar studies of S-passivation of Ge, the results presented here, shows a great promise of implementing this method in the fabrication of Ge based field effect devices as a standardized process step.

Concluding Remarks

In this thesis different device performance tuning strategies for vertical Ge p-channel have been investigated experimentally. The main goal of the work was to find a method of improving the drain drive current, which is a major problem for TFETs. Simple methods for passivating the Ge surface as a measure to improve the electrostatic control of the gate, were also investigated through the fabrication and electrical characterization of MOS capacitors.

In chapter 4 and 5 the implementation of GeSn in the channel and source region of Ge TFET was investigated. Due to the lower bandgap of GeSn, compared to Ge, a successive increase in I_{ON} is achieved when increasing the Sn-content. The increase in I_{ON} is due to the lowering of the bandgap which effectively increases the tunneling probability at the source-channel interface. An increase in Sn-content beyond the 4 % investigated here is expected to further increase I_{ON}. However, due to the lowering of the bandgap and degradation of the crystalline quality, the leakage current and SS are also seen to worsen when the Sn-content is increased. In this regard an increase in Sn-content is unfavorable, and can only be performed if compensated through other performance tuning strategies. A reduction in leakage current and improved SS can be achieved through device dimension scaling. Additional device improvement involves reducing the GeSn layer thickness. The feasibility of GeSn as channel material seems, however, also to rely on improvement in the MBE growth of GeSn.

In an effort to improve the line tunneling component originating in the source-gate overlap region, the source doping concentration was varied and its effect on the electrical characterization was investigated. It was found that varying the source doping concentration mainly influence the subthreshold characteristics of the TFETs. Steeper subthreshold characteristics was found with increasing source doping concentration. The early onset and temperature dependence, indicates that a TAT process taking place in the source-gate overlap region dominates, and is the main cause of subthreshold leakage. The SS as a function of source doping could be understood qualitatively, when this kind of process is assumed. Contrary to results from published simulation studies, no effect of varying the source doping concentration on I_{ON} could be distinguished for the doping levels investigated. More experimental research, and a greater understanding, of the contribution of line- and point-tunneling in TFETs with gate-source overlap is needed if this should be used to improve I_{ON}.

A MBE pre-buildup technique of Sb is investigated as a means to achieve steep source doping profiles. It was found that for a Sb pre-buildup concentration of 1/20 ML, both I_{ON} and SS is improved. The extent of the tunneling barrier into the source region is reduced, and the

tunneling probability is increased and the band pass filtering improved. The boost in I_{ON} is small, but the pre-buildup technique imposes no extra load onto the TFET fabrication process and can easily be combined with other strategies intended to boost the drive current in TFETs. The results also suggests that an optimal pre-buildup doping exists.

When analyzing the electrical characteristics of the vertical GAA TFETs presented in this work, some weak spots in the device geometry have become obvious. The main problem is the large overlap of the gate electrode in the drain region. This has several drawbacks. Firstly, the gate-substrate leakage causes serious device reliability issues and prevents the gate oxide being scaled down to the needed dimension. An EOT of < 1 nm is desired, however EOT less than 4.5 nm is difficult to obtain without short circuiting the devices and returning a sufficiently high chip transistor yield needed for statistical significant comparison. It therefore seems difficult to achieve < 60 mV/dec subthreshold slopes with this geometry, even for excellent quality MBE semiconductor layer structures. Secondly, the large gate-drain overlap cause gate induced leakage currents which degrade the device performance. Switching gate oxide from Al_2O_3 to other commonly used oxides like HfO_2 or ZrO_2, which have a higher permittivity would help solve the first problem, but not the latter. The only way of achieving both is if through the formation of a spacer after mesa etching. This is, however, not straight forward as many requirements have to be fulfilled. A low deposition temperature is needed not to cause doping profile smearing. A high thickness precision is required to have a well-defined gate alignment matching the layer structure and mesa height. On the same time the formation of this spacer must be performed without mesa side-wall coverage. How this can be achieved technologically is still an open question and is a suggestion for further work. I note that switching to a higher permittivity gate oxide would any case be beneficial for the overall performance of the devices.

In this work the $Ge/Al_2O_3/Al$ system was also studied. A GeO_x-passivation, achieved through a post-plasma oxidation method, and a sulfur passivation, achieved through an aqueous Ammonium sulfite solution treatment, were both investigated through the fabrication and electrical characterization of MOS-capacitors. For the sample passivated with GeO_x, a hysteresis, and a shift in the flatband voltage is explained by acceptor traps in the oxide. A general parallel shift of the C-V curve towards positive gate voltages indicates fixed negative charges and an O-rich Al_2O_3. These O-rich regions could be induced by the post plasma oxidation treatment. Temperature dependent I-V characteristics indicate a Schottky emission process as the main transport mechanism through the oxide at low electric fields. The effect of sulfur passivation of the Ge surface is seen to reduce both the C-V hysteresis and the leakage current in the low E-field region. The measured oxide capacitance also reveal that this does not

come at the expense of a thicker EOT. Both passivation methods are relatively simple with respect to implement in the vertical TFET fabrication scheme, and seem to contain room for improvement.

Appendix: The Metal-Oxide-Semiconductor System

In this section the theoretical background for the MOS capacitor is given. This appendix is mainly relevant for Chapter 7 and Chapter 8.

The Metal-Oxide-Semiconductor Capacitor

A MOS-capacitor is a parallel plate capacitor consisting of one metallic plate electrode, called the *gate*, and another electrode, a semiconductor. Separating the two electrodes is a thin insulating layer, an oxide[2]. The MOS capacitors distinctive voltage dependence motivated the pursuit of the MOS structure at first as a voltage variable-controlled varistor [31, 193]. However, its real usefulness was quickly found as an alternative low power way of controlling the current flow in a transistor[194]. It is nowadays extensively used as a simple test structure measuring the properties of MOS systems. A simple schematic of a MOS capacitor is shown in Figure 57. The MOS capacitance (C_M) is a series combination of the oxide capacitance (C_{OX}) and the semiconductor capacitance (C_S) and is therefore given by:

$$C_M = \frac{C_{OX} \cdot C_S}{C_{OX} + C_S}. \tag{32}$$

C_{OX} depends on the thickness and permittivity of the oxide as dictated by the parallel plate capacitor formula:

$$C_{OX} = \frac{\varepsilon_o \cdot \varepsilon_r}{d}. \tag{33}$$

Here ε_o is the vacuum permittivity, ε_r the relative permittivity of the oxide and d the oxide thickness. For gate oxides, SiO_2, being the preferred oxide in CMOS technology for decades, is often used as a reference for comparison. The term equivalent oxide thickness (EOT) is therefore often used when discussing oxides other than SiO_2. EOT is defined as:

$$EOT = \frac{\varepsilon_o \cdot \varepsilon_{SiO_2}}{C_{OX}}, \tag{34}$$

where ε_{SiO2} is the relative permittivity of SiO_2. One can see that from (34) that only C_{OX} is needed to obtain EOT, since $\varepsilon_{SiO2} = 3.9$ is well established[31]. This allows the quantitative

[2] As the role of the oxide is to serve as an insulating layer, the term metal-insulator-semiconductor (MIS) capacitor, is a more accurate description than MOS capacitor. The term also includes insulator materials other than only oxides. More often than not though the insulator is an oxide.

comparison of different oxides without information of the actual relative permittivity and thickness of the oxide being investigated.

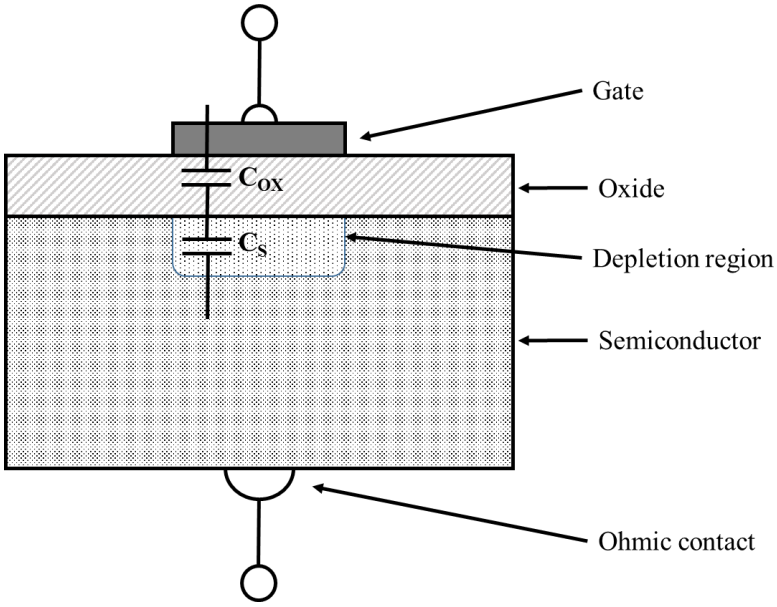

Figure 57 A simplistic schematic of MOS capacitor structure. The MOS capacitance is a series combination of the oxide capacitance C_{OX} and the semiconductor capacitance C_S.

C_{OX} makes up the passive component of the MOS capacitor. Now what makes the MOS capacitor unique is its active, i.e. voltage dependent, component C_S. To understand the functioning of a MOS capacitor one needs to understand how the potential and the energy bands in a semiconductor behave, and therefore also C_S, when a voltage is applied to the gate electrode. When a gate voltage V_G is applied, the electrical field will penetrate a certain distance into the semiconductor material. Within this region of penetration the energy bands experience a bending and the electrical conductivity is altered. This is called *the field effect*. In this regard two important potentials should be introduced, the semiconductor bulk potential Ψ_B and surface potential Ψ_S. Ψ_B depends on the doping level of the semiconductor and is given by the potential difference between the extrinsic Fermi level and the intrinsic mid gap level:

$$\psi_B = E_i - E_F = \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{N_A}{n_i}\right) \text{ (p-type)}. \tag{35}$$

The electrical field in the semiconductor is at its strongest at the surface and will decrease towards zero as one moves further into the bulk. ψ_s is therefore a measure of the maximum band bending and the total potential difference between the semiconductor surface and the bulk. Different regions, or states, of the MOS capacitor can be distinguished for different values of ψ_s, with both its magnitude and polarity with respect to ψ_B. For the following examples a p-

type semiconductor is considered. Similar results can be obtained for a n-type semiconductor when accounting for the different polarity of voltage.

Table 9 shows the different states of a MOS capacitor with respect to the surface potential. For a negative V_G the applied electrical field attracts the majority charge carriers, the positively charged mobile holes, to the surface. Here they pile up and form an accumulation layer. This state of the MOS capacitor is hence called *accumulation,* and the energy bands bend upwards. Now increasing the gate voltage from this state causes the reduction of negative charges on the gate to be compensated by holes leaving the accumulation layer. At a certain voltage called the *flatband voltage,* V_{FB}, the semiconductor is neutral everywhere. The energy bands at this bias are completely flat. When increasing V_G above V_{FB} the holes continue being repelled from the surface. When doing so they now however leave negatively charged fixed acceptor ions behind to balance the positive gate potential. This charged region of acceptor ions is called the *depletion region* since holes have been depleted from the surface. This depletion region continue to increase in width when increasing V_G and at a certain point the Fermi level at the surface equals the Fermi level of that of an intrinsic semiconductor. This state is called *midgap*. By the further increase of V_G minority charge carriers, in this example electrons, appear at the surface forming a thin *inversion layer.* This is the onset of the state called *weak inversion*. The generation of electrons comes as a consequence of thermal equilibrium. The formation of the inversion layer prevents the width of the depletion layer to increase, as the gate charged is balanced by electrons instead of acceptor ions. The inversion layer effectively shields the semiconductor from further penetration. Although we have a p-type semiconductor, in inversion the doping concentration in the semiconductor at the surface has been electrostatically inverted and will behave as a n-type semiconductor. The onset of the region called s*trong inversion* starts when the electron concentration at the semiconductor surface equals the bulk doping concentration, $n_p = N_A$.

Table 9 Different regions of the MOS capacitor defined by the surface potential.

$\psi_s < 0$	Accumulation (bands bend upward)
$\psi_s = 0$	Flatband condition (bands are flat)
$\psi_B > \psi_s > 0$	Depletion (bands bend downward)
$\psi_s = \psi_B$	Midgap
$2\psi_B > \psi_s > \psi_B$	Weak inversion $n_p > p_p$ at surface
$\psi_s > 2\psi_B$	Strong inversion

An energy band diagram schematic is shown in Figure 58 and shows a MOS capacitor in inversion and the corresponding potentials Ψ_B and Ψ_S. An expression for the potential and band bending in the semiconductor as a function of distance x from the semiconductor/oxide surface, $\Psi_P(x)$, can be obtained by solving the one-dimensional Poisson equation:

$$\frac{d^2\psi_p(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_s}, \tag{36}$$

here $\rho(x)$ is the charge distribution and ε_s the semiconductor permittivity. The reader is directed elsewhere [123] for a thorough walkthrough of the solving of the Poisson equation for the general case.

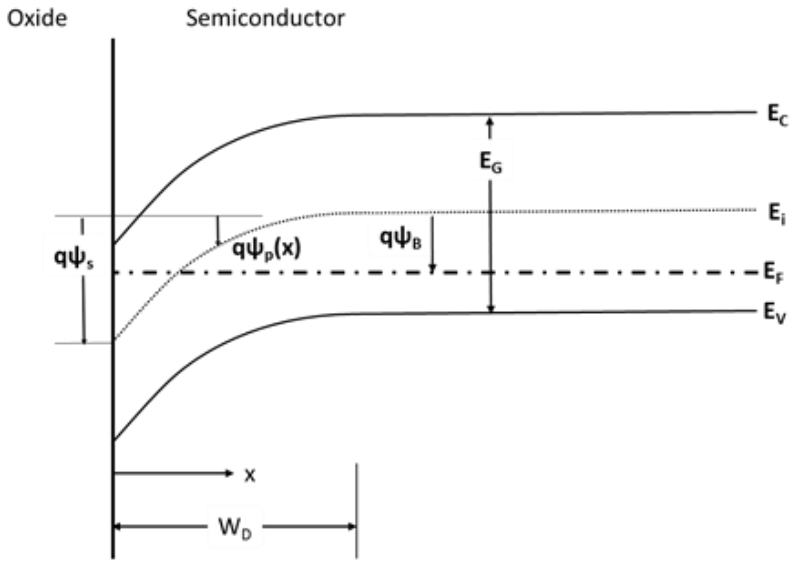

Figure 58 Energy-band diagram of the oxide/p-type semiconductor surface when a positive gate voltage is applied and the MOS capacitor is in inversion. The surface potential describes the band bending in the semiconductor at the interface, $\Psi_S = \Psi p(0)$. The bulk potential Ψ_B is the energy difference between the intrinsic mid gap level and the extrinsic Fermi level.

In the case of the high frequency MOS capacitance a similar approach as for a pn junction can be used when integrating (36). By assuming the ionized acceptors in the depletion region result in a charge distribution given by $\rho = -qN_A W_D$, the potential distribution in the depletion region yields[31]:

$$\psi_p(x) = \psi_S \cdot \left(1 - \frac{x}{W_D}\right)^2. \tag{37}$$

Where the surface potential Ψ_S is given by:

$$\psi_S = \frac{qN_A W_D^2}{2\varepsilon_S}. \tag{38}$$

Non-Idealities in the Metal-Oxide-Semiconductor System

What has been described up until now is an ideal MOS capacitor. In the real MOS capacitor, however, there exists non-idealities like traps and charges in the MOS system that will affect the ideal MOS characteristics. We can distinguish between charges and traps in the oxide based on their spatial location. Interface traps are located at the oxide/semiconductor interface and can be due to structural defects, like broken bonds, at the surface[195]. Interface traps can be donor traps, which means that they are neutral when filled and positively charged when empty, or acceptor traps, which are neural when empty and negatively charged when filled. Donor traps are usually located in the lower half of the energy bandgap, while the acceptor traps are usually located in the upper half of the energy band[196]. The interface traps causes a stretch out of the experimental curve due to a less effective modulation of the surface potential. The stretch out relates to the interface traps with that the density of interface states, D_{it}, is proportional to the change in gate voltage with respect to the change in surface potential[31].

The charges and traps inside the oxide are divided into three types[195]: mobile oxide charges, fixed oxide charges and trapped oxide charges. They all can give rise to a parallel shift of the C-V curve. Mobile charges are due to ionic impurities, mostly sodium ions, and can move through the oxide and give rise to voltage shifts depending on biasing condition. In modern MOS fabrication lines the contamination of these ionic impurities is very low and mobile charges can in many cases be neglected. Fixed oxide charges are usually located in the oxide near the oxide/semiconductor interface and are also often a consequence of structural defects. In the Si/SiO_2 the fixed oxide charges are almost exclusively positive, but for other systems this is not always the case[197]. Oxide traps are related to defects in the oxide. Unlike fixed oxide charges, oxide traps can be charged and discharged with electrons or holes. Fleetwood [165] introduced the term border traps as an effort to distinguish between traps deep in the oxide, and traps near the interfaces which can electrically communicate with the underlying semiconductor. However with the miniaturization and scaling the gate oxide thicknesses have become so narrow that all oxide traps can be considered border traps.

Like for the oxide, there are also traps in the semiconductor bulk. A high semiconductor trap density will influence the charge carrier life time and could also greatly influence the frequency

dependence of the MOS electrical characteristics. The frequency dependence of the MOS capacitor is discussed next.

Measuring the Metal-Oxide-Semiconductor Capacitor

Capacitance is by definition the ratio of change in charge to the corresponding change in voltage. To measure a capacitance at different direct current (DC) voltage biases one therefore needs an additional superimposed alternating current (AC)-voltage signal to detect a change. For a MOS capacitor the frequency of this AC-voltage (mV range) plays an important role. Unlike in a metal, where very mobile electrons respond more or less instantaneously to a voltage change, the semiconductor charge carriers are associated with a certain *response time*. The response time of majority carriers is related to the dielectric relaxation time of the semiconductor. For the frequencies of interest for this work and for most practical uses (0 - 1MHz), this response can be considered instantaneous [123]. The minority carrier response time however, is directly related to how fast on average the minority carriers can be generated and relaxed again through a generation-recombination (G-R) process [54]. In thermal equilibrium, the G and R rates are equal and inversely proportional to the minority carrier lifetime. The minority carrier lifetime is in turn dependent on material parameters such as the bandgap, intrinsic carrier concentration, doping concentration and trap density. Some of these material parameters also have a strong temperature dependence, and as a consequence so does the G-R rate. With respect to the G-R rate one distinguishes between a low-frequency (LF) and a high-frequency (HF) C-V measurement, for which the C-V characteristics especially in inversion differ qualitatively. In a LF measurement the period is long enough for minority carriers to respond to the AC-signal and the inversion layer capacitance is measured in addition to the depletion layer capacitance. As the inversion charge is confined in a thin inversion layer and shields the depletion layer from expanding, C_S becomes very large and will dominate the denominator in (32). C_M will therefore saturate towards C_{OX} for increasing inversion bias. For a HF measurement the minority carriers do not respond to the fast varying AC voltage signal. C_S therefore equal the depletion layer capacitance $C_D = \varepsilon \cdot W_D$. As the minority carriers however do respond to the slow varying DC voltage bias, the depletion layer width will reach a maximum and C_D a minimum in inversion.

A similar dependency of the C-V characteristics as that the frequency can be seen when varying the temperature. As the G-R rate is strongly temperature dependence a LF behavior results at even relatively high measurement frequencies if the temperature is increased.

In general for a Si MOS capacitor a measurement frequency of typically 100 Hz or less is needed to measure a LF C-V curve at room temperature. For a higher mobility material such as Ge on the other hand, a LF or intermediate frequency C-V curve could be obtained at much higher frequencies[123].

Modeling the Metal-Oxide-Semiconductor Capacitor

Most MOS capacitance measurements are made by measuring the impedance of a device under test (DUT) from the ratio of the AC-signal voltage to the sample current[198]. By using the 0° and 90° phase angles, the impedance is converted into a conductance G_p, and a capacitance C_p in parallel as seen in Figure 59a. In most cases the MOS capacitance is obtained simply by equaling it to the measured parallel capacitance, $C_M = C_p$. This simplistic approximation can in some cases be erroneous, for example for high tunneling currents, and more accurate models must be implemented. In Figure 59b a three element model where the capacitance C_c is the measured capacitance corrected for series resistance is shown. In Figure 59c a detailed seven element model is depicted where the MOS capacitance also includes non-idealities like single level interface state. Although being more accurate, the more elements, i.e. variables, one considers, however, the more advanced and sophisticated measurement and analysis methods are needed to single the different components out.

Parameter Extraction from High Frequency Capacitance-Voltage Measurement

Once a good model relating the measured capacitance to the MOS capacitance has been established several properties of the MOS system can be obtained from the HF C-V measurement of a MOS capacitor.

Oxide Capacitance

From the HF C-V curve the maximum capacitance is extracted in the accumulation region. Due to the fact that the accumulation layer is very thin, C_S as a consequence becomes very large and (32) reduces to $C_M \approx C_{OX}$ in strong accumulation. C_{OX}, and the corresponding EOT, can therefore be found directly from the maximum capacitance and (34), respectively. With knowledge of the relative permittivity of the deposited oxide one would also obtain the physical oxide thickness or vice versa through (33).

Semiconductor Doping Concentration

Once C_{OX} is known it can be eliminated from (32) and C_S can be directly related to C_M. At the onset of strong inversion the depletion layer reaches a maximum width W_{DM} since it is effectively shielded from further penetration by the inversion layer. C_S therefore saturate to ε_S/W_{DM} in inversion. As values of ε_S can be found in literature, the maximum depletion width W_{DM} can be extracted from the measurement. Rearranging (38) and inserting $2\psi_b$ for ψ_s (onset of strong inversion) yields:

$$W_{DM} \approx \sqrt{\frac{2 \cdot \varepsilon_S \cdot \psi_s}{q \cdot N_A}} = \sqrt{\frac{4 \cdot \varepsilon_S \cdot k_B \cdot T \cdot \ln(N_A/n_i)}{q^2 \cdot N_A}}. \tag{39}$$

Rearranging (39) yields an expression for the doping concentration:

$$N_A = \frac{4 \cdot \varepsilon_S \cdot k_B \cdot T \cdot \ln(N_A/n_i)}{q^2 \cdot W_{DM}^{\,2}}. \tag{40}$$

The doping concentration cannot be extracted directly from this nested formula, but easily by finding the zero value through a numerical approach.

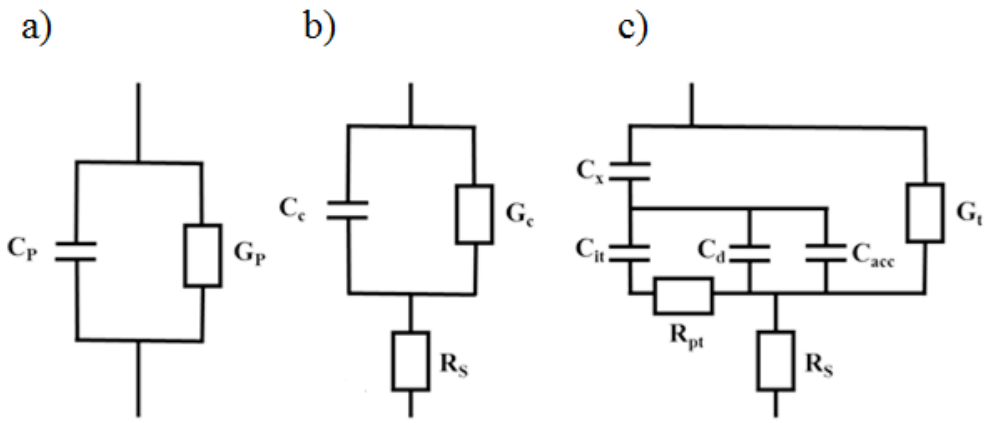

Figure 59 Equivalent circuits for a MOS Capacitor. **a)** Circuit shows the measured capacitance C_p and the measured conductance G_p. **b)** Circuit in a) transformed to show the capacitance C_c corrected for series resistance R_S. (c) A detailed general circuit model for a MOS capacitor in depletion or accumulation for a single interface state level. Model includes the interface state capacitance Cit, depletion capacitance C_d, accumulation capacitance C_{acc}, oxide capacitance C_{ox}, tunnel conductance G_t and majority carrier interface trap resistance R_{pt}. After [210].

Flatband Voltage

The most common method for determining the flatband voltage V_{FB} for uniform doping is through the flatband capacitance method [123]. In this method the ideal flatband capacitance is calculated using the relation:

$$C_{FB}=\frac{\varepsilon_S}{L_D}, \tag{41}$$

where L_D is the extrinsic Debye length for holes and is given by:

$$L_D \equiv \sqrt{\frac{k_B \cdot T \cdot \varepsilon_S}{q^2 \cdot N_A}}. \tag{42}$$

By equaling C_S in (32) to C_{FB} the corresponding value on the measured HF C-V curve can be found by interpolating between the closest V_G values. Often chosen for its simplicity, this method is in error when large interface traps contributions, charge nonuniformities as well as nonuniform semiconductor doping concentration are present.

Metal-Semiconductor Work Function and Oxide Charges

A non-zero metal-semiconductor work function leads to that the experimental C-V curve is shifted from the theoretical curve by the same amount in gate bias. This metal-semiconductor work function is given by:

$$W_{MS} = W_M - \left(\chi + \frac{E_G}{2q} + \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{N_A}{n_i}\right)\right). \tag{43}$$

Here, W_M is the work function of the gate metal, χ the electron affinity and E_G the bandgap of the semiconductor. Material parameters can be found in literature so only the doping, which can be found through the method explained above, is needed to calculate W_{MS}. An eventual deviation of flatband from the calculated W_{MS} value is a consequence of charges in the oxide. Neglecting mobile charges, both charged oxide traps and fixed oxide traps causes an effective shift of the flatband voltage given by

$$V_{FB}=W_{MS}-\frac{Q_f+Q_{ot}}{C_{OX}}=W_{MS}-\frac{Q_{eff}}{C_{OX}}. \tag{44}$$

Rearanging (44) yields:

$$Q_{eff}=C_{OX}\cdot(W_{MS}-V_{FB}). \quad (45)$$

The sign of Q_{eff} will determine if the effective charges are negative (-) or positive (+), respectively.

Interface Trap Charges

Different methods have been developed to determine the interface state density. The most frequently used are the low-frequency capacitance-, high-low-frequency capacitance- and the conductance-method [123]. All of these methods however necessitate either a very low measurement frequency, or a broad range of frequencies. Terman[199] developed the HF capacitance method in the early 60's. This method aims to compare the HF C-V experimental curve, which is stretched out due to interface traps, with the theoretical ideal curve obtained from solving (36). The method has been criticized for being unreliable compared to other methods, especially for low interface state densities[200]. Jakubowski and Iniewski also pointed to the lack of practical importance of the method and proposed a simple technique for determination of the interface trap density at the mid gap[179]. Using Linder's formula[193] the change in gate potential ΔV_M, corresponding to the change in mid gap capacitance for an incremental change of surface potential voltage is calculated. Taking the difference of this theoretical value with change in $\Delta V_M'$ from the experimental curve, which can be found by closest point interpolation, an expression for the interface state density is given by:

$$D_{it}^{MG}=\frac{C_{OX}}{2\cdot k_B\cdot T\cdot q}\cdot(\Delta V_M'-\Delta V_M). \quad (46)$$

As the interface states distribution is known to increase towards the band edges, this value of D_{it} can be considered a minimum value. The use of mid gap voltage shift to determine the interface state density is based on the assumption that the interface traps are amphoteric, also referred to as P_b-, centers [201] . With this assumption the interface traps can be considered neutral at mid gap, as all donor traps are filled and all acceptor traps are empty. Studies have however shown that this assumption is not always valid [202, 203].

Carrier Transport and Current-Voltage Characteristics of a Metal-Oxide-Semiconductor Capacitor

Ideally the energy barriers between the gate metal and the oxide, and the semiconductor and the oxide, are so large that they prevent the free flow of carriers from the metal and to the semiconductor or vice versa. In real insulators on the other hand some degree of carrier conduction will be present at sufficiently high electrical field or temperature. There exist different carrier transport mechanisms, which depend on the materials under investigation, i.e. barrier height between oxide and semiconductor and effective mass. For a given insulator different transport mechanisms may also strongly depend on the applied voltage and the temperature. To determine from a measured I-V characteristics which type of carrier transport mechanisms occur through the oxide, an estimate of the electrical field in the insulator under biasing condition is needed. A simple estimate of the electrical field across the insulator is to assume:

$$\mathrm{E} \approx \frac{V}{\mathrm{d}}. \tag{47}$$

Here E is the electrical field and d the oxide thickness. This assumption neglects oxide charges and assumes that the flatband voltage and band bending in the semiconductor are small compared to the applied voltage. Schottky emission, named after its discoverer [204], is a commonly observed transport mechanism in oxides. It describes the thermionic emission over a metal-insulator or semiconductor insulator barrier. A Schottky emission current is expressed by:

$$\mathrm{J}=\mathrm{A}^{**}\cdot\mathrm{T}^{2}\cdot\exp\left(\frac{-\mathrm{q}\cdot\left(\Phi_{\mathrm{B}}-\sqrt{\mathrm{q}\cdot\mathrm{E}/4\cdot\pi\cdot\varepsilon_{\mathrm{r}}\cdot\varepsilon_{0}}\right)}{\mathrm{k}_{\mathrm{B}}\cdot\mathrm{T}}\right). \tag{48}$$

Here Φ_B is the barrier height from the fermi level to the oxide conduction band and A^{**} is the effective Richardson constant. Schottky emission, as one can see from (48), has a distinct T^2 temperature dependency. Frenkel-Poole emission[205], is another observed transport mechanism through oxides, which describes the emission of electrons to the conduction band from trapped oxide states. Frenkel-Poole emission is expressed by:

$$\mathrm{J}\propto\mathrm{E}\cdot\exp\left(\frac{-\mathrm{q}\cdot(\Phi_{\mathrm{B}}{}^{*}-\sqrt{\mathrm{q}\cdot\mathrm{E}/\pi\cdot\varepsilon_{\mathrm{r}}\cdot\varepsilon_{0}})}{\mathrm{k}_{\mathrm{B}}\cdot\mathrm{T}}\right). \tag{49}$$

Here the barrier height, Φ_B^* is the depth of the potential well and therefore lower compared to the barrier height in the Schottky emission equation. For high electric fields, tunneling is a common transport mechanism. It can be divided into direct tunneling (DT), Fowler-Nordheim tunneling (FNT), and trap-assisted tunneling (TAT). Tunneling emission has a strong field dependency, but is essentially independent of temperature. TAT, can however also involve phonons, and might therefore have a stronger and more complex temperature dependency than DT and FNT, respectively. In DT the carriers tunnel through the complete width of the barrier and therefore only dominate for oxides with a small thickness, $d_{ox} < 5$ nm. For thicker oxides and at high enough applied gate voltage, the oxide conduction band edge at one side of the oxide is beneath the fermi level at the gate or semiconductor, depending on gate polarity, junction. As the voltage drops linearly across the oxide, the oxide barrier takes the shape of a triangle. FNT [126] describes the field induced emission through this triangular barrier, which is only a partial width of the oxide thickness. Using a free-electron gas model for the metal and the Wentzel-Kramer-Brillouin approximation [206] for the tunneling probability the following expression for the current density is obtained [207]:

$$J=(q^3\cdot E^2\cdot(m/m^*)/(8\cdot\pi\cdot h\cdot\Phi_B)\cdot\exp\left(\frac{-4\cdot\sqrt{2\cdot m^*}\cdot(q\cdot\Phi_B)^{3/2}}{3\cdot q\cdot\hbar\cdot E}\right). \quad (50)$$

Here Φ_B is the barrier height, m is the free electron mass and m^* is the effective mass. When comparing the equations for the different current mechanisms one can see that they have different temperature and field dependencies. This difference can be used to identify the exact conduction mechanism experimentally.

Dielectric Breakdown

In addition to high leakage currents, another concern for reliability of MOS based devices is the catastrophic breakdown of the dielectric film. At catastrophic breakdown the insulator loses its blocking behavior and carriers flow through it. Breakdown in insulators has successfully been described by the percolation theory[208]. As described in the section above a leakage current, usually a tunneling current for large biases, flows through the oxide. Energetic carriers cause defects in the bulk oxide. These defects are generated randomly inside the oxide. The percolation theory assumes that the traps can be consider as spheres with a certain radius[209]. When the spheres of two neighboring traps overlap, conduction between them is possible. When a critical average defect density is reached a conductive path between the gate electrode and semiconductor is formed and breakdown occurs.

References

[1] Ericsson, November 2015. [Online]. Available: http://www.ericsson.com/res/docs/2015/mobility-report/ericsson-mobility-report-nov-2015.pdf.

[2] C. Claeys and E. Simoen, Germanium-based technologies: from materials to devices, Amsterdam: Elsevier, 2007.

[3] W. H. Brattain and B. John, "Three-electrode circuit element utilizing semiconductive materials". USA Patent 2,524,035, 3 October 1950.

[4] J. S. Kilby, "Miniaturized electronic circuits". USA Patent 3,138,743, 23 June 1964.

[5] L. Esaki, "New Phenomenon in Narrow Germanium p-n Junctions," *Physical Review,* vol. 109, no. 2, pp. 603-604, 1958.

[6] M. M. Atalla, E. Tannenbaum and E. J. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides," *Bell System Technical Journal,* vol. 38, no. 3, p. 749–783, 1959.

[7] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics,* vol. 38, no. 8, 1965.

[8] R. W. Keyes, "Physical Limits in Digital Electronics," *Proceding of the IEEE,* vol. 63, no. 5, p. 740, 1975.

[9] J. Haddad, "Implications of LSI," *1974 ISSCC Digest of Technical Papers,* pp. 50-51, 1974.

[10] J. D. Cressler, "A Brief History of the Field," in *Silicon Heterostructure Handbook,* Boca Raton, CRC Press, 2006, p. 21.

[11] "SiGe-Channel n-MOSFET by Germanium Implantation," *IEEE Electron Device Letters* , vol. 12, no. 8, pp. 444-446, 1991.

[12] J. Welser, J. Hoyt and J. Gibbons, " Electron mobility enhancement in strained-Si n-type metal-oxide-semiconductor field-effect transistors," *IEEE Electron Device Letters,* vol. 15, no. 3, pp. 100-102, 1994.

[13] D. K. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang and K. P. MacWilliams, "High-Mobility p-Channel Metal-Oxide-Semiconductor Field-Effect-Transistor on Strained Si," *Applied Physics Letters,* vol. 62, no. 22, pp. 2853-2855, 1993.

[14] M. Loughran, "IBM Creates World's Fastest Semiconductor Circuits".

[15] M. T. Bohr, "The Invention of Uniaxial Strained Silicon Transistors at Intel," *Intel Corporation,* pp. 1-4, 2007.

[16] T. Jackson, C. Ransom and J. DeGelormo, "Gate-self-aligned p-channel germanium MISFETs," *Electron Device Letters, IEEE,* vol. 12, no. 11, pp. 605 - 607 , 1991.

[17] E. Crisman, J. Lee, P. Stiles and O. Gregory, "Characterisation of n-channel germanium MOSFET with gate insulator formed by high-pressure thermal oxidation," *Electronics Letters,* vol. 23, no. 1, pp. 8-10, 1987.

[18] S. Martin, L. Hitt and J. Rosenberg, "p-channel germanium MOSFETs with high channel mobility," *Electron Device Letters, IEEE* , vol. 10, no. 7, pp. 325-326, 1989.

[19] M. T. Bohr, R. Chau, T. Ghani and K. Mistry, "The high-k solution," *IEEE Spectrum,* vol. 44, no. 10, pp. 29-35, 2007.

[20] M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, C. Dewan, D. Park, H. Bu, W. Natzle, W. Yan, C. Ouyang, K. Henson, D. Boyd, S. Callegari, R. Carter, D. Casarotto, M. Gribelyuk, M. Hargrove, W. He and Y. Kim, "High-performance high-κ/metal gates for 45nm CMOS and beyond with gate-first processing," *IEEE Symposium on VLSI Technology,* pp. 194-195, 2007.

[21] R. Cavin, P. Lugli and V. Zhirnov, "Science and Engineering Beyond Moore's Law," *Proceedings of the IEEE,* vol. 100, pp. 1720 - 1749, 2012.

[22] H. Wu, N. Conrad, W. Luo and P. D. Ye, "First Experimental Demonstration of Ge CMOS Circuits," *IEEE Electron Devices Meeting (IEDM)*, pp. 9.3.1 - 9.3.4 , 2014.

[23] D. Sarkar, X. Xie, W. Liu, W. Cao, J. G. Y. Kang, S. Kraemer and P. M. B. K. Ajayan, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, pp. 91-95, 2015.

[24] O. M. Stuetzer, "Junction fieldistors," *Proceedings of the IRE*, vol. 40, no. 11, pp. 1377 - 1381, 1952.

[25] C. Zener, "A theory of the electrical breakdown of solid dielectrics," *Proceedings of the Royal Society of London*, vol. 145, no. 855, pp. 523-529., 1934.

[26] T. N. P. i. P. 1973, "Nobelprize.org," Nobel Media AB, 2014. [Online]. Available: http://www.nobelprize.org/nobel_prizes/physics/laureates/1973/. [Accessed Januar 2016].

[27] E. O. Kane, "Zener tunneling in semiconductors," *Journal of Physics and Chemistry of Solids*, vol. 12, no. 2, pp. 181-188, 1960.

[28] E. O. Kane, "Theory of tunneling," *Journal of Applied Physics*, vol. 32, pp. 83-91, 1961.

[29] R. N. Hall, "Tunnel diodes," *IRE Transactions on Electron Devices*, vol. 7, no. 1, pp. 1-9, 1960.

[30] H. S. Sommers Jr, "Tunnel diodes as high-frequency devices," *Proceedings of the IRE*, vol. 47, no. 7, pp. 1201-1206, 1959.

[31] S. M. Sze and K. N. Kwok, Physics of Semiconductor Devices, 3. ed., New Jersey: John Wiley & Sons, 2007.

[32] J. J. Quinn, G. Kawamoto and B. D. McCombe, "Subband spectroscopy by surface channel tunneling," *Surface Science*, vol. 73, pp. 190-196, 1978.

[33] T. Baba, "Proposal for surface tunnel transistors," *Japanese journal of applied physics, ,* vol. 31, no. 4B, pp. L455-L457, 1992.

[34] W. M. Reddick and G. A. Amaratunga, "Silicon surface tunnel transistor," *Applied Physics Letters*, vol. 67, no. 4, pp. 494-496, 1995.

[35] Y. Omura, "Negative conductance properties in extremely thin silicon-on-insulator (SOI) insulated-gate pn-junction devices (SOI surface tunnel transistors)," *Japanese journal of applied physics*, vol. 35, no. 11A, p. L1401, 1996.

[36] T. &. B. T. Uemura, "Large enhancement of interband tunneling current densities of over 10 5 A/cm 2 in In/sub 0.53/Ga/sub 0.47/As-based surface tunnel transistors," *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 225-227, 1997.

[37] W. M. Reddick and G. A. Amaratunga, "Silicon surface tunnel transistor," *Applied Physics Letters*, vol. 67, no. 4, pp. 494-496, 1995.

[38] W. Hansch, C. Fink, J. Schulze and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon," *Thin Solid Films*, vol. 369, no. 1-2, p. 387–389, 2000.

[39] K. K. Bhuwalka, J. Schulze and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp+ layer," *Japanese Journal of Applied Physics*, vol. 43, no. 7R, p. 4073, 2004.

[40] J. Appenzeller, Y. M. Lin, J. Knoch and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Physical Review Letters*, vol. 93, no. 19, p. 196805, 2004.

[41] T. Krishnamoan, D. Kim, S. Raghunathan and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With Record High Drive Currents and <60mV/dec Subthreshold Slope," *Proc IEDM*, p. 1:3, 2008.

[42] Y. Lu, S. Bangsaruntip, X. Wang, L. Zhang, Y. Nishi and H. Dai, "DNA functionalization of carbon nanotubes for ultrathin atomic layer deposition of high κ dielectrics for nanotube transistors with 60 mv/decade switching," *Journal of the American Chemical Society*, vol. 128, no. 11, pp. 3518-3519, 2006.

[43] D. K. Schroder, Semiconductor Material and Device Characterization (first edition), New York: John Wiley & Sons, 1990, p. 148.

[44] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low-power CMOS digital design," *IEICE Transactions on Electronics,* vol. 75, no. 4, pp. 371-382, 1992.

[45] K. K. Bhuwalka, J. Schulze and I. Eisele, "A simulation approach to optimize the electrical parameters of a vertical tunnel FET," *IEEE transactions on electron devices,* vol. 52, no. 7, pp. 1541-1547, 2005.

[46] P. F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis and W. Hansch, "Complementary tunneling transistor for low power application," *Solid-State Electronics,* vol. 48, no. 12, pp. 2281-2286, 2004.

[47] A. S. Verhulst, W. G. Vandenberghe, K. Maex and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Applied Physics Letters, ,* vol. 91, no. 5, p. 053102, 2007.

[48] R. Narang, M. Saxena, R. S. Gupta and M. Gupta, "Assessment of ambipolar behavior of a tunnel FET and influence of structural modifications," *Journal of Semiconductor Technology and Science,* vol. 12, no. 4, pp. 482-491, 2012.

[49] I. Lauer, A. Majumdar, P. M. Solomon and S. J. Koester, "Fabrication of a vertical heterojunction tunnel-FET". USA Patent 8,258,031, 4 September 2012.

[50] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE,* vol. 98, no. 12, pp. 2095 - 2110 , 2010.

[51] M. I. Nathan, "Current voltage characteristics of germanium tunnel diodes," *Journal of applied physics,* vol. 33, no. 4, pp. 1460-1469, 1962.

[52] S. Agarwal and E. Yablonovitch, "Band-Edge Steepness Obtained From Esaki/Backward Diode Current–Voltage Characteristics," *IEEE Transactions on Electron Devices,* vol. 61, no. 5, pp. 1488-1493, 2014.

[53] J. Knoch, S. Mantl and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid-State Electronics,* vol. 51, no. 4, pp. 572-578, 2007.

[54] R. N. Hall, "Recombination processes in semiconductors," *Proceedings of the IEE - Part B: Electronic and Communication Engineering,* vol. 106, no. 17, pp. 923-931, 1959.

[55] W. Shockley and W. T. Read Jr, "Statistics of the recombinations of holes and electrons," *Physical review,* vol. 87, no. 5, p. 835, 1952.

[56] G. A. M. Hurkx, D. B. M. Klaassen and M. P. G. Knuvers, "A New Recombination Model for Device Simulation Including Tunneling," *IEEE Transactions on Electron Devices,* vol. 39, no. 2, pp. 331-338, 1992.

[57] T. Y. Chan, A. T. Wu, P. K. Ko and C. Hu, "Effects of the Gate-to-Drain/Source Overlap on MOSFET Characteristics," *IEEE Electron Device Letters,* vol. 8, no. 7, pp. 326-328, 1987.

[58] S. Banerjee, D. Coleman, W. Richardson and A. Shah, "Leakage mechanisms in the trench transistor DRAM cell," *IEEE Transactions on Electron Devices,* vol. 35, no. 1, pp. 108-116, 1988.

[59] "International Technology Roadmap for Semiconductors," [Online]. Available: http://www.itrs.net/reports.html.

[60] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* 2011.

[61] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE Journal of the Electron Devices Society,* vol. 2, no. 4, pp. 44 - 49, 2014.

[62] K. Jeon, W. Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder and H. H. Tseng, "Si tunnel transistors with a novel silicided source and 46mV/dec swing," *IEEE Symposium on VLSI Technology 2010,* pp. 121-122, 2010.

[63] R. Gandhi, Z. Chen, N. Singh and K. Banerjee, "Vertical Si-Nanowire n -Type Tunneling FETs With Low Subthreshold Swing (≤ 50 mV/decade) at Room Temperature," *IEEE Electron Dev Let,* vol. 32, no. 4, pp. 437-439, 2011.

[64] Q. Huang, R. Huang, Z. Zhan, Y. Qiu, W. Jiang, C. Wu and Y. Wang, "A novel Si tunnel FET with 36mV/dec subthreshold slope based on junction depleted-modulation through striped gate configuration," *IEEE International Electron Devices Meeting* , pp. 8-5, 2012.

[65] A. Villalon, C. Le Royer, M. Cassé, D. Cooper, B. Prévitali, C. Tabone and F. Allain, "Strained tunnel FETs with record I ON: first demonstration of ETSOI TFETs with SiGe channel and RSD," *IEEE Symposium on VLSI technology 2012* , pp. 49-50, 2012.

[66] D. Hähnel, M. Oehme, M. Sarlija, A. Karmous, M. Schmid, J. Werner, O. Kirfel, I. Fischer and J. Schulze, "Germanium vertical Tunneling Field-Effect Transistor," *Solid State Electronics,* vol. 62, no. 1, pp. 132-137, 2011.

[67] P. M. Solomon, I. Lauer, A. Majumdar, J. T. Teherani, M. Luisier, J. Cai and S. J. Koester, "Effect of uniaxial strain on the drain current of a heterojunction tunneling field-effect transistor," *IEEE Electron Device Letters,* vol. 32, no. 4, pp. 464-466, 2011.

[68] R. Kotlyar, U. E. Avci, S. Cea, R. Rios, T. D. Linton, K. J. Kuhn and I. A. Young, "Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors," *Applied Physics Letters,* vol. 102, no. 11, p. 113106, 2013.

[69] M. Noguchi, S. Kim, M. Yokoyama, S. Ji, O. Ichikawa, T. Osada and S. Takagi, "High I on/I off and low subthreshold slope planar-type InGaAs tunnel FETs with Zn-diffused source junctions," *IEEE International Electron Devices Meeting 2013,* pp. 28-1, 2013.

[70] R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V. Nguyen and T. Clarke, "Demonstration of In 0.9 Ga 0.1 As/GaAs 0.18 Sb 0.82 near broken-gap tunnel FET with I ON= 740μA/μm, G M= 70μS/μm and gigahertz switching performance at V Ds= 0.5 V," *IEEE International Electron Devices Meeting 2013,* pp. 28-2, 2013.

[71] R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen and M. Wistey, "AlGaSb/InAs tunnel field-effect transistor with on-current of 78 at 0.5 V," *IEEE electron device letters,* vol. 33, no. 3, pp. 363-365, 2012.

[72] G. Dewey, R. Kotlyar, R. Pillarisetty, M. Radosavljevic, T. Rakshit, H. Then and R. Chau, "Logic performance evaluation and transport physics of Schottky-gate III–V compound semiconductor quantum well field effect transistors for power supply voltages (V CC) ranging from 0.5 V to 1.0 V," *IEEE International Electron Devices Meeting 2009,* pp. 1-4, 2009.

[73] J. Knoch and J. Appenzeller, "Modeling of high-performance p-type III–V heterojunction tunnel FETs," *IEEE Electron Device Letters,* vol. 31, no. 4 , pp. 305-307, 2010.

[74] P. R. Berger, "Silicon-based tunneling field effect transistors and transistor circuitry employing same". USA Patent 9,209,285, 8 December 2015.

[75] C. Gong, H. Zhang, W. Wang, L. Colombo, R. M. Wallace and K. Cho, "Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors," *Applied Physics Letters,* vol. 103, no. 5, p. 053513, 2013.

[76] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko and N. M. R. Peres, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science,* vol. 335, no. 6071, pp. 947-950, 2012.

[77] J. Schulze, A. Blech, A. Datta, I. A. Fischer, D. Hähnel, S. Naasz, E. Rolseth and E.-M. Tropper, "Vertical Ge and GeSn Heterojunction Gate-All-Around Tunneling Field Effect Transistors," *Solid-State Electronics,* vol. 110, pp. 59-64, 2015.

[78] S. Agarwal and E. Yablonovitch, "The low voltage TFET demands higher perfection than previously required in electronics," *73rd Annual Device Research Conference,* pp. 247 - 248 , 2015.

[79] K. Boucart and A. M. Ionescu, "Double gate tunnel FET with ultrathin silicon body and high-k gate dielectric," *IEEE European Solid-State Device Research Conference* , pp. 383-386, 2006.

[80] N. Ma and D. Jena, "Interband tunneling in two-dimensional crystal semiconductors," *Applied Physics Letters,* vol. 102, no. 13, p. 132102, 2013.

[81] M. Miranda, "IEEE spectrum," 28 June 2012. [Online]. Available: http://spectrum.ieee.org/semiconductors/design/the-threat-of-semiconductor-variability.

[82] Y. Lu, A. Seabaugh, P. Fay, S. J. Koester, S. E. Laux, W. Haensch and S. O. Koswatta, "Geometry dependent tunnel FET performance-dilemma of electrostatics vs. quantum confinement," *IEEE Device Research Conference (DRC)*, pp. 17-18, 2010.

[83] I. Fischer, A. Bakibillah, M. Golve, D. Hähnel, H. Isemann, A. Kottantharayil, M. Oehme and J. Schulze, "Silicon tunneling field-effect transistors with tunneling in line with the gate field," *IEEE Electron Dev Let*, vol. 34, no. 2, pp. 154-156, 2013.

[84] M. Schmidt, A. Schafer, R. Minamisawa, D. Buca, S. Trellenkamp, J.-M. Hartmann, Q.-T. Zhao and S. Mantl, "Line and Point Tunneling in Scaled Si/SiGe Heterostructure TFETs," *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 699-701, 2014.

[85] D. Hähnel, I. A. Fischer, A. Hornung, A. C. Köllner and J. Schulze, "Tuning the Ge(Sn) Tunneling FET: Influence of Drain Doping, Short Channel and Sn Content," *Electron Devices, IEEE Transactions*, vol. 62, no. 1, pp. 36 - 43, 2015.

[86] R. A. Soref and L. Friedman, "Direct-gap Ge/GeSn/Si and GeSn/Ge/Si heterostructures. Superlattices and microstructures," vol. 14, no. 2, pp. 189-193, 1993.

[87] Y. Yang, G. Han, P. Guo, W. Wang, X. Gong, L. Wang, K. L. Low and Y.-C. Yeo, "Germanium–Tin P-Channel Tunneling Field-Effect Transistor: Device Design and Technology Demonstration," *IEEE Transaction on Electron Devices*, vol. 60, no. 12, pp. 4048-4056, 2013.

[88] W. G. Vandenberghe, A. S. Verhulst, K. H. Kao, K. De Meyer, B. Sorée, W. Magnus and G. Groeseneken, "A model determining optimal doping concentration and material's band gap of tunnel field-effect transistors," *Applied Physics Letters*, vol. 100, no. 19, p. 193509, 2012.

[89] S. S. Iyer, R. A. Metzger and F. G. Allen, "Sharp profiles with high and low doping levels in silicon grown by molecular beam epitaxy," *Journal of Applied Physics*, vol. 52, no. 9, pp. 5608-5613, 1981.

[90] D. Lei, W. Wang, Z. Zhang, J. Pan, X. Gong, G. Liang and Y. C. Yeo, "Ge0. 83Sn0. 17 p-channel metal-oxide-semiconductor field-effect transistors: Impact of sulfur passivation on gate stack quality," *Journal of Applied Physics*, vol. 119, no. 2, p. 02450, 2016.

[91] M. M. Frank, S. J. Koester, M. Copel, J. A. Ott, V. K. Paruchuri and H. Shang, "Hafnium oxide gate dielectrics on sulfur-passivated germanium," *Applied Physics Letters*, vol. 89, 2006.

[92] E. Kasper and J. C. Bean, Silicon-Molecular Beam Epitaxy Volume I, Boca Raton, Florida: CRC Press, Inc, 1988.

[93] R. N. Hall, "Segregation of Impurities during the Growth of Germanium and Silicon," *The Journal of Physical Chemistry*, vol. 57, no. 8, pp. 836-839, 1953.

[94] D. Streit, R. A. Metzger and F. G. Allen, "Doping of silicon in molecular beam epitaxy systems by solid phase epitaxy," *Applied Physics Letters*, vol. 44, no. 2, pp. 234-236, 1984.

[95] J. Bardeen and W. Shockley, "Deformation Potentials and Mobilities in Non-Polar Crystals," *Physical Review*, vol. 80, no. 1, pp. 72-80, 1950.

[96] E. Kasper and S. Heim, "Challenges of high Ge content silicon germanium structures," *Applied Surface Science*, vol. 224, no. 1-4, pp. 3-8, 2004.

[97] E. Kasper and D. J. Paul, "Virtual Substrates and Strain Relaxation," in *Silicon Quantum Integrated Circuits*, Heidelberg, Springer-Verlag , 2005, pp. 40-47.

[98] L. M. Giovane, H. C. Luan, A. M. Agarwal and L. C. Kimerling, "Correlation between leakage current density and threading dislocation density in SiGe p-i-n diodes grown on relaxed graded buffer layers," *Appl. Phys. Lett.*, vol. 78, pp. 541-543, 2001.

[99] E. Kasper and K. Lyutovich, "Strain adjustment with thin virtual substrates," *Solid-State Electronics*, vol. 48, no. 8, pp. 1257-1263, 2004.

[100] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 97, no. 1, p. 011101, 2005.

[101] P. R. Pukite, A. Harwit and S. S. Iyer, "Molecular beam epitaxy of metastable, diamond structure SnxGe1− x alloys," *Applied Physics Letters*, vol. 54, no. 21, pp. 2142-2144, 1989.

[102] J. Piao, R. Beresford, T. Licata, W. I. Wang and H. Homma, "Molecular- beam epitaxial growth of metastable Ge1− xSnx alloys," *Journal of Vacuum Science & Technology B*, vol. 8, no. 2, pp. 221-226, 1990.

[103] H. J. Gossmann, "Determination of critical layer thicknesses in IV- IV- alloy systems using reflection high energy electron diffraction intensity oscillations: Ge (100)/GexSn1− x," *Journal of applied physics*, vol. 68, no. 6, pp. 2791-2795, 1990.

[104] E. A. Fitzgerald, P. E. Freeland, M. T. Asom, W. P. Lowe, R. A. Macharrie, B. E. Weir and S. L. Cooper, "Epitaxially stabilized GexSn1− x diamond cubic alloys," *Journal of electronic materials*, vol. 20, no. 6, pp. 489-501, 1991.

[105] W. Wegscheider, J. Olajos, U. Menczigar, W. Dondl and G. Abstreiter, "Fabrication and properties of epitaxially stabilized Ge/α-Sn heterostructures on Ge (001)," *Journal of crystal growth*, vol. 123, no. 1, pp. 75-94, 1992.

[106] K. P. Homewood and M. A. Lourenço, "Optoelectronics: The rise of the GeSn laser," *Nature Photonics*, vol. 9, no. 2, pp. 78-79, 2015.

[107] S. Wirths, A. T. Tiedemann, Z. Ikonic, P. Harrison, B. Holländer, T. Stoica and D. Buca, "Band engineering and growth of tensile strained Ge/(Si) GeSn heterostructures for tunnel field effect transistors," *Applied physics letters*, vol. 102, no. 19, p. 192103, 2013.

[108] E. Kasper, J. Werner, M. Oehme, S. Escoubas, N. Burle and J. Schulze, "Growth of silicon based germanium tin alloys," *Thin Solid Films*, vol. 520, pp. 3195-3200, 2012.

[109] K. Kostecki, M. Oehme, R. Koerner, D. Widmann, M. Gollhofer, S. Bechler, G. Mussler, D. Buca, E. Kasper and J. Schulze, "Virtual substrate technology for Ge1-XSnX heteroepitaxy on Si substrates," *ECS Trans.* , vol. 64, no. 6, pp. 811-818, 2014.

[110] B. Vincent, F. Gencarelli, H. Bender, C. Merckling, B. Douhard, D. H. Petersen, O. Hansen, H. H. Henrichsen, J. Meersschaut, W. Vandervorst, M. Heyns, L. R. and M. Caymax, "Undoped and in-situ B doped GeSn epitaxial growth on Ge by atmospheric pressure-chemical vapor deposition," *Applied Physics Letters*, vol. 99, no. 15, p. 152103, 2011.

[111] M. Oehme, J. Werner and E. Kasper, "Molecular beam epitaxy of highly antimony doped germanium on silicon," *Journal of Crystal Growth*, vol. 310, no. 21, pp. 4531-4534, 2008.

[112] W. Wang, Q. Zhou, Y. Dong, E. S. Tok and Y. C. Yeo, "Critical thickness for strain relaxation of Ge1− xSnx (x≤ 0.17) grown by molecular beam epitaxy on Ge (001)," *Applied Physics Letters*, vol. 106, p. 232106, 2015.

[113] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca and D. Grützmacher, "Lasing in direct-bandgap GeSn alloy grown on Si," *Nature Photonics*, vol. 9, p. 88–92, 2015.

[114] A. A. Tonkikh, C. Eisenschmidt, V. G. Talalaev, N. D. Zakharov, J. Schilling, G. Schmidt and P. Werner, "Pseudomorphic GeSn/Ge (001) quantum wells: Examining indirect band gap bowing," *Applied Physics Letters*, vol. 103, no. 3, p. 032106, 2013.

[115] S. M.-K. B. N. Y. S. K. C. Gupta, "Achieving direct band gap in germanium through integration of Sn alloying and external strain," *Journal of Applied Physics*, vol. 113, no. 7, p. 073707, 2013.

[116] A. Ishizaka and Y. Shiraki, "Low temperature surface cleaning of silicon and its application to silicon MBE," *J. Electrochem. Soc.* , vol. 133, no. 4, pp. 666-671 , 1986.

[117] S. Brotzmann and H. I. Bracht, "Intrinsic and extrinsic diffusion of phosphorus, arsenic, and antimony in germanium," *Journal of Applied Physics*, vol. 103, no. 3, p. 033508, 2008.

[118] M. Oehme, K. Kostecki, K. Ye, S. Bechler, K. Ulbricht, M. Schmid, M. Kaschel, M. Gollhofer, R. Körner, W. Zhang, E. Kasper and J. Schulze, "GeSn-on-Si normal incidence photodetectors with bandwidths more than 40 GHz," *Optics express*, vol. 22, no. 1, pp. 839-846, 2014.

[119] D. R. Gajula, P. Baine, M. Modreanu, P. K. Hurley, B. M. Armstrong and D. W. McNeill, "Fermi level de-pinning of aluminium contacts to n-type germanium using thin atomic layer deposited layers," *Appl. Phys. Lett.*, no. 104, p. 012102, 2014.

[120] I. M. Huygens, W. P. Gomes and K. Strubbe, "Etching of germanium in hydrogenperoxide solutions," *ECS Transactions,* vol. 6, no. 2, pp. 375-386, 2007.

[121] R. L. Puurunen, "Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process," *Journal of Applied Physics* , vol. 97, no. 12, p. 121301, 2002.

[122] R. Zhang, J. Lin, M. Takenaka and S. Takagi, "Impact of plasma post oxidation temperature on interface trap density and roughness at GeOx/Ge interfaces," *Microelectronic Engineering,* no. 109, pp. 97-100, 2013.

[123] E. H. Niccollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, New Jersey: John Wiley & Sons, 1982.

[124] A. Stesmans, "Passivation of Pb0 and Pb1 interface defects in thermal (100) Si/SiO2 with molecular hydrogen," *Applied physics letters,* vol. 68, no. 15, pp. 2076-2078, 1996.

[125] J. R. Weber, A. Janotti, P. Rinke and C. G. Van de Walle, "Dangling-bond defects and hydrogen passivation in germanium," *Applied Physics Letters,* vol. 91, no. 14, p. 142101, 2007.

[126] R. H. Fowler and L. Nordheim, "Electron Emission in Intense Electric Fields," *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character,* vol. 119, no. 781, pp. 173-181 , 1928.

[127] I. The MathWorks, *MATLAB 7.1,* Natick, Massachusetts, 2005.

[128] A. Savitzky and M. J. Golay, "Smoothing and differentiation of data by simplified least squares procedures," *Analytical chemistry,* vol. 36, no. 8, pp. 1627-1639, 1964.

[129] OriginLab, *Origin 8,* Northampton, MA, 2008.

[130] Q. T. Zhao, J. M. Hartmann and S. Mantl, "An Improved Si Tunnel Field Effect Transistor With a Buried Strained Si1-xGex Source," *IEEE Electron Dev Let,* vol. 32, no. 11, pp. 1480-1482, 2011.

[131] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan and S. Datta, "Temperature - Dependent I-V Characteristics of a Vertical In0.53Ga0.47As Tunnel FET," *Electron Device Letters, IEEE,* vol. vol. 31, pp. 564-566, 2010.

[132] C. D. Bessire, M. T. Björk, H. Schmid, A. Schenk, K. B. Reuter and H. Riel, "Trap-Assisted Tunneling in Si-InAs Nanowire Heterojunction Tunnel Diodes," *Nano Letters,* vol. vol. 11, pp. 4195-4199, 2011.

[133] C. W. Magee and R. E. Honig, "Depth profiling by SIMS—depth resolution, dynamic range and sensitivity," *Surface and Interface Analysis,* vol. 4, no. 2, pp. 35-41, 1982.

[134] E. Simoen, C. Claeys and J. Vanhellemont, "Defect Analysis in Semiconductor Materials Based on p-n Junction Diode Characteristics," *Defect and Diffusion Forum,* Vols. 261-262, pp. 1-24, 2007.

[135] U. Avci, B. Chu-kung, A. Agrawal, G. Dewey, V. Le, R. Rios, D. H. S. Morris, R. Kotlyar, J. Kavalieros and I. Young, "Study of TFET Non-ideality Effects for Determination of Geometry and Defect Density Requirements for Sub-60mV/dec Ge TFET," *2015 IEEE International Electron Devices Meeting (IEDM)* , pp. 34.5.1-34.5.4, 2015.

[136] C. Schulte-Braucks, N. von den Driesch, S. Glass, A. T. Tiedemann, U. Breuer, A. Besmehn and D. Buca, "Low temperature deposition of high-k/metal gate stacks on high-Sn content (Si) GeSn-alloys," *ACS applied materials & interfaces,* 2016.

[137] P. Guo, G. Han, X. Gong, B. Liu, Y. Yang, W. Wang and Y. C. Yeo, "Ge0. 97Sn0. 03 p-channel metal-oxide-semiconductor field-effect transistors: Impact of Si surface passivation layer thickness and post metal annealing," *Journal of Applied Physics,* vol. 114, no. 4, p. 044510, 2013.

[138] V. D. Kunz, T. Uchino, C. H. de Groot, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang and P. L. F. Hemment, "Reduction of parasitic capacitance in vertical MOSFETs by spacer local oxidation," *IEEE Transactions on Electron Devices* , vol. 50, no. 6, pp. 1487 - 1493 , 2003.

[139] "Ioffe Physico Technical Institute," [Online]. Available: http://www.ioffe.ru/SVA/NSM/Semicond/Ge/bandstr.html. [Accessed 2016].

[140] S. Gupta, R. Chen, B. Magyari-Kope, H. Lin, B. Yang, A. Nainani, Y. Nishi, J. S. Harris and K. Saraswat, "GeSn technology: Extending the Ge electronics roadmap," *IEEE International Electron Devices Meeting (IEDM)*, pp. 16.6.1-16.6.4 , 2011.

[141] M. Pala and D. Esseni, "Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs—Part I: Model Description and Single Trap Analysis in Tunnel-FETs," *IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2795 - 2801 , 2013.

[142] W. G. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Sor´ee and W. Magnus, "Analytical Model for Point and Line Tunneling in a Tunnel Field-Effect Transistor," *Proc. SISPAD* , pp. 137-140, 2008.

[143] K. L. Low, Y. Yang, G. Han, W. J. Fan and Y. C. Yeo, "Electronic Band Structure and Effective Masses of Ge1-xSnx Alloys.," *ECS Transactions*, vol. 50, no. 9, pp. 519-526, 2013.

[144] J. Wu, J. Min and Y. Taur, "Short-Channel Effects in Tunnel FETs.," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 3019-3024, 2015.

[145] G. Eneman, M. Wiot, A. Brugère, O. S. I. Casain, S. Sonde, D. P. Brunco and C. Claeys, "Impact of Donor Concentration, Electric Field, and Temperature Effects on the Leakage Current in Germanium p n Junctions," *IEEE Transansactions on Electron Devices*, vol. 55, no. 9, pp. 2287-2296, 2008.

[146] L. Liu, D. Mohata and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors.," *IEEE Transactions on Electron Devices* , vol. 59, no. 4, pp. 902-908, 2012.

[147] C. G. Van de Walle, "Band lineups and deformation potentials in the model-solid theory," *Physical Review B*, vol. 39, no. 3, pp. 1871-1883, 1989.

[148] L. Jiang, J. Gallagher, C. Senaratne, T. Aoki, J. Mathews, J. Kouvetakis and J. Menéndez, "Compositional dependence of the direct and indirect band gaps in Ge1−y Sn y alloys from room temperature photoluminescence: implications for the indirect to direct gap crossover in intrinsic and n-type materials," *Semiconductor Science and Technology*, vol. 29, 2014.

[149] G.-E. Chang, S.-W. Chang and C. S. L., "Strain-Balanced GezSn1−z–SixGeySn1−x−y Multiple-Quantum-Well Lasers," *IEEE Journal of quantum electronics*, vol. 46, no. 12, pp. 1813-1820, 2010.

[150] M. Jaros, "Simple analytic model for heterojunction band offsets," *Physical Review B*, vol. 37, p. 7112, 1988.

[151] S. Inc., Santa Clara, 2012.

[152] T. Takagahara and K. Takeda, "Theory of the quantum confinement effect on excitons in quantum dots of indirect-gap materials," *Physical Review B*, vol. 46, no. 23, p. 15578, 1992.

[153] S. O. Koswatta, S. J. Koester and W. Haensch, "1D broken-gap tunnel transistor with MOSFET-like on-currents and sub-60mV/dec subthreshold swing," *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, 2009.

[154] W. Vandenberghe, A. Verhulst, G. Groeseneken, B. Soree and W. Magnus, "Analytical model for point and line tunneling in a tunnel field-effect transistor," *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2008)* , pp. 137 - 140, 2008.

[155] M. Rosar, B. Leroy and G. Schweeger, "A new model for the description of gate voltage and temperature dependence of gate induced drain leakage (GIDL) in the low electric field region [DRAMs]," *IEEE Transactions on Electron Devices*, vol. 47, no. 1, pp. 154-159, 2000.

[156] T. E. Chang, C. Huang and T. Wang, "Mechanisms of interface trap-induced drain leakage current in off-state n-MOSFET's," *IEEE Transactions on Electron Devices* , vol. 42, no. 4, pp. 738-743, 1995.

[157] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field- effect transistors," *physica status solidi (a)*, vol. 205, no. 4, pp. 679-694, 2008.

[158] A. S. Verhulst, D. Leonelli, R. Rooyackers and G. Groeseneken, "Drain voltage dependent analytical model of tunnel field-effect transistors," *Journal of Applied Physics*, vol. 110, no. 2, p. 024510, 2011.

[159] K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken and K. De Meyer, "Direct and indirect band-to-band tunneling in germanium-based TFETs," *IEEE Transactions on Electron Devices,* vol. 59, no. 2, pp. 292-301, 2012.

[160] K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, W. Magnus, D. Leonelli and K. De Meyer, "Optimization of gate-on-source-only tunnel FETs with counter-doped pockets," *IEEE Transactions on Electron Devices,* vol. 59, no. 8, pp. 2070-2077, 2012.

[161] H. J. Gossmann, F. C. Unterwald and H. S. Luftman, "Doping of Si thin films by low-temperature molecular beam epitaxy," *Journal of applied physics,* vol. 73, no. 12, pp. 8237-8241, 1993.

[162] J. Wilhelm, W. Wegscheider and G. Abstreiter, "Sharp doping profiles and two-dimensional electron systems in Ge based heterostructures," *Surface science,* vol. 267, no. 1-3, pp. 90-93, 1992.

[163] M. Oehme, D. Hähnel, J. Werner, M. Kaschel, O. Kirfel, E. Kasper and J. Schulze, "Si Esaki diodes with high peak to valley current ratios," *Appl. Phys. Lett,* vol. 95, no. 24, p. 242109, 2009.

[164] D. V. Yurasov, A. V. Antonov, M. N. Drozdov, V. B. Schmagin, K. E. Spirin and A. V. Novikov, "Antimony segregation in Ge and formation of n-type selectively doped Ge films in molecular beam epitaxy," *Journal of Applied Physics,* vol. 118, no. 14, p. 145701, 2015.

[165] D. M. Fleetwood, " `Border traps' in MOS devices," *IEEE Transactions on Nuclear Science ,* vol. 39, no. 2, pp. 269-271.

[166] M. Muller, S. Duguay, B. Guillaumot, X. Garros, C. Leroux, B. Tavel, F. Martin, M. Rivoire, D. Delille, F. Boeuf, S. Deleonibus and T. Skotnicki, "Towards a better EOT - mobility trade-off in high-k oxide/metal gate CMOS devices," *IEEE 33rd Conference on European Solid-State Device Research,* pp. 367-370, 2003.

[167] Q. Xie, S. Deng, M. Schaekers, D. Lin, M. Caymax, A. Delabie, X.-P. Qu, Y.-L. Jiang, D. Deduytsche and C. Detavernier, "Germanium surface passivation and atomic layer deposition of high-k dielectrics - a tutorial review on Ge-based MOS capacitors," *Semicond. Sci. Technol.,* vol. 27, no. 7, pp. 1-14, 2012.

[168] M. Caymax, F. M. J. Leys, K. Martens, L. Yang, G. Pourtois, W. Vandervorst and M. L. R. Meuris, "The Influence of the Epitaxial Growth Process Parameters on Layer Characteristics and Device Performance in Si-Passivated Ge pMOSFETs," *Journal of The Electrochemical Society,* vol. 156, no. 12, pp. 979-985, 2009.

[169] C. O. Chui, F. Ito and K. Saraswat, "Scalability and electrical properties of germanium oxynitride MOS dielectrics," *IEEE Electron Device Letters ,* vol. 25, no. 9, pp. 613 - 615 , 2004.

[170] Y. Fukuda, T. Ueno and S. H. S. Hirono, "Electrical Characterization of Germanium Oxide/Germanium Interface Prepared by Electron-Cyclotron-Resonance Plasma Irradiation," *Japanese Journal of Applied Physics,* vol. 44, no. 9B, p. 6981, 2005.

[171] K. Park, Y. Lee, J. Lee and S. Lim, "Oxidation mechanism of hydrogen-terminated Ge (100) surface," *Applied Surface Science,* vol. 254, no. 15, pp. 4828-4832, 2008.

[172] G. C. Ltd., *Metals, Alloys, Compounds, Ceramics, Polymers, Composites Catalogue 1993/94,* 1994.

[173] Accuratus Corporation, "Accuratus," 2013. [Online]. Available: http://accuratus.com/alumox.html. [Accessed 9 2015].

[174] J. W. Lim and S. J. Yun, "Electrical Properties of Alumina Films by Plasma-Enhanced Atomic Layer Deposition," *Electrochemical and Solid-State Letters ,* vol. 7, no. 8, pp. 45-48, 2004.

[175] M. D. Groner, J. W. Elam, F. H. Fabreguette and S. M. George, "Electrical characterization of thin Al2O3 films grown by atomic layer deposition on silicon and various metal substrates," *Thin Solid Films,* vol. 413, no. 1-2, p. 186–197, 2002.

[176] M. Oehme, M. Gollhofer, D. Widmann, M. Schmid, M. Kaschel and E. S. J. Kasper, "Direct bandgap narrowing in Ge LED's on Si substrates," *Optics Express,* vol. 21, no. 2, pp. 2206-2211, 2013.

[177] A. Dimoulas, G. Vellianitis, G. Mavrou, E. K. Evangelou and A. Sotiropoulos, "Intrinsic carrier effects in HfO2–Ge metal–insulator–semiconductor capacitors," *Applied Physics Letters,* vol. 86, no. 22, p. 223507, 2005.

[178] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle and P. C. McIntyre, "Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate insulators on chemically treated InGaAs substrates," *Appl. Phys. Lett. ,* vol. 96, p. 152908, 2010.

[179] A. Jakubowski and K. Ieniewski, "Simple Method for detination of the interface Trap Density at the Midgap in MOS structures," *Phys. Stat. Sol.,* vol. 73, no. 2, p. 545–549, 1982.

[180] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. S. Y. Oshima and K. C. Saraswat, "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Letters,* vol. 29, no. 4, pp. 328-330, 2008.

[181] N. Taoka, K. Ikeda, Y. Yamashita and N. T. S.-I. Sugiyama, "Effects of ambient conditions in thermal treatment for Ge (001) surfaces on Ge–MIS interface properties," *Semicond. Sci. Technol.,* vol. 22, pp. 114-117, 2007.

[182] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan and K. Saraswat, "On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates," *IEEE Transactions on Electron Devices,* vol. 55, no. 2, pp. 547-555, 2008.

[183] G. A. Scoggan and T. P. Ma, "Effects of electron- beam radiation on MOS structures as influenced by the silicon dopant," *J. Appl. Phys. ,* vol. 48, pp. 294-300, 1977.

[184] B. J. Gordon, "C-V Plotting: Myths and Methods," *Solid State Technology,* vol. 36, pp. 57-61, 1993.

[185] K. Iniewski, A. Balasinski, B. Majkusiak, R. B. Beck and A. Jukubowski, "Series resistance in a MOS capacitor with a thin gate oxide," *Solid-State Electronics,* vol. 32, no. 2, pp. 137-140, 1989.

[186] A. Goetzberger and E. H. Nicollian, "Temperature Dependence of Inversion-Layer Frequency Response in Silicon," *Bell System Technical Journal,* vol. 46, no. 3, p. 513–522, 1967.

[187] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett.,* vol. 72, p. 1718, 1998.

[188] H. C. Lin, P. D. Ye and G. D. Wilk, "Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al 2 O 3 on GaAs," *Appl. Phys. Lett. ,* vol. 87, p. 182904, 2005.

[189] J. Suehle, "Ultrathin gate oxide reliability: physical models, statistics, and characterization," *IEEE Transactions on Electron Devices,* vol. 49, no. 6, pp. 958-971, 2002.

[190] R. Xie and C. Zhu, "Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectrics," *IEEE Electron Device Letters,* vol. 27, no. 11, pp. 976-979, 2007.

[191] T. Maeda, S. Takagi, T. Ohnishi and M. Lippmaa, "Sulfur passivation of Ge (0 0 1) surfaces and its effects on Schottky barrier contact," *Materials Science in Semiconductor Processing,* vol. 9 , p. 706–710, 2006.

[192] C.-H. Chen, K.-C. Chuang and J.-G. Hwu, " Characterization of Inversion Tunneling Current Saturation Behavior for MOS(p) Capacitors With Ultrathin Oxides and High- k Dielectrics," *IEEE Transactions on Electron Devices,* vol. 56 , no. 6, pp. 1262-1268, 2009.

[193] R. Lindner, "Semiconductor surface varactor," *Bell System Technical Journal,* vol. 41, no. 3, pp. 803-831, 1962.

[194] K. Dawon, "Electric field controlled semiconductor device". USA Patent 3,102,230 , 27 August 1963.

[195] B. E. Deal, "Standardized terminology for oxide charges associated with thermally oxidized silicon," *IEEE Transactions on Electron Devices,* vol. 27, no. 3, pp. 606 - 608 , 1980.

[196] L.-Å. Ragnarsson and P. Lundgren, "Electrical characterization of P b centers in (100)Si–SiO 2 structures: The influence of surface potential on passivation during post metallization anneal," *J. Appl. Phys. ,* vol. 88, no. 2, p. 938, 2000.

[197] G. Agostinelli, A. Delabie, P. Vitanov, Z. Alexieva, H. Dekkers, S. De Wolf and G. Beaucarne, "Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge," *Solar Energy Materials and Solar Cells,* vol. 90, no. 18, p. 3438–3443, 2006.

[198] D. K. Schroder, "Appendix 6.1 Capacitance Measurement Techniques," in *Semiconductor Material and Device Characterization*, Arizona, John Wiley & Sons, Inc., 1990, pp. 286-288.

[199] L. M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electronics,* vol. 5, pp. 285-299, 1962.

[200] A. Goetzberger, E. Klausmann and M. J. Schulz, "Interface states on semiconductor/insulator surfaces," *C R C Critical Reviews in Solid State Sciences,* vol. 6, no. 1, pp. 18-19, 1976.

[201] E. H. Poindexter, G. J. Gerardi, M. Rueckel, P. J. Caplan, N. M. Johnson and D. K. Biegelsen, "Electronic traps and P b centers at the Si/SiO2 interface: Band- gap energy distribution," *J. Appl. Phys. ,* vol. 56, p. 2844 , 1984.

[202] Z. Shanfield and M. Moriwaki, " Critical Evaluation of the Midgap-Voltage-Shift Method for Determining Oxide Trapped Charge in Irradiated Mos Devices," *IEEE Transactions on Nuclear Science,* vol. 34 , no. 6, p. 1987, 1159 - 1165 .

[203] E. H. Poindexter, P. J. Caplan and B. E. R. R. R. Deal, "Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers," *J. Appl. Phys. ,* no. 52, p. 879, 1981.

[204] S. W., "Über spontane Stromschwankungen in verschiedenen Elektrizitätsleitern," *Annalen der Physik,* vol. 362, no. 23, p. 541–567, 1918.

[205] J. Frenkel, "On Pre-Breakdown Phenomena in Insulators and Electronic Semi-Conductors," *Phys. Rev. ,* vol. 54, p. 647, 1938.

[206] J. L. Dunham, "The Wentzel-Brillouin-Kramers Method of Solving the Wave Equation," *Phys. Rev. ,* vol. 41, p. 713, 1932.

[207] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO2," *Journal of Applied Physics,* vol. 40, no. 1, pp. 278-283, 1968.

[208] J. H. Stathis, "Percolation models for gate oxide breakdown," *J. Appl. Phys. ,* vol. 86, pp. 5757-5766, 1999.

[209] R. Degraeve, G. Groeseneken, R. Bellens, J. Ogier, M. Depas, P. Roussel and H. Maes, "New insights in the relation between electron trap generation and the statistical properties of oxide breakdown," *IEEE Transactions on Electron Devices,* vol. 45, no. 4, pp. 904 - 911, 1998.

[210] S. Kar and W. Dahlke, "Interface states in MOS structures with 20–40 Å thick SiO2 films on nondegenerate Si," *Solid-State Electronics,* vol. 15, no. 2, pp. 221-237, 1972.

[211] F. A. Trumbore, "Solid solubilities of impurity elements in germanium and silicon," *Bell System Technical Journal,* vol. 39, no. 1, pp. 205-233, 1960.

[212] R. E. Honig, "Vapor pressure data for the solid and liquid elements," *RCA review,* vol. 23, no. 4, pp. 567-586, 1962.

[213] D. J. Eaglesham and M. Cerullo, "Dislocation-free stranski-krastanow growth of Ge on Si (100)," *Physical review letters,* vol. 64, no. 16, p. 1943, 1990.

Acknowledgements

The last four years have personally been a period of breaking new grounds. I have moved to another country, plunged into a new scientific field, and on top of that I have been trying to pursue the highest academic title achievable. For a reserved and cautious Norwegian, this has certainly been a big transition. Astonishingly, things have gone remarkably smooth. Thanks to numerous people which have supported me along the way. It is therefore long past time to hand out some thank you's and Dankeschön's.

First of all I want to thank Prof. Jörg Schulze for giving me this opportunity. Thank you for allowing me to engineer, to do research and for including me in your wonderful group at IHT. Thank you for schooling me in the field of semiconductor engineering and your guidance through my bumpy ride towards a PhD title. I have certainly learned a lot, which I am sure will come in handy later in life.

A big thank you to all my co-workers. Not only would fabricating the devices presented in this work have been an impossible task, but spending time at the university would have become very, very dull. Inga, thank you for being my go-to-person, always finding time to answer my annoying questions and reading through and commenting my work. Senthil, thanks for your great spirit, teaching me about Indian culture and for our many interesting talks and discussions. Klaus, Michael, Sabine and Thanh-Hai, thank you, not only for your help and invaluable assistance, but also for shortening down the waiting periods in the cleanroom with enjoyable conversations.

My fellow PhD collegues: Daniel, Heike, Mathias, Mark, Wogong, Konrad, Ahmed, Lion, Yasmine, thank you for making the 50 km drive from Tübingen to Pfaffenwaldring each day worthwhile. Roman, Stefan, Matze, Tobi and Martin, you guys deserve a big *Dankeschön*. Spending time with you also after work and in weekends has brought me a lot of fun and good times. The introduction to events like 'der Männertag' have given my invaluable insight into German culture. I hope to participate in this event in the years to come.

I would also like to thank Florian Bärwolf from Innovation of High Performance Microelectronics (IHP) for SIMS measurement presented in Chapter 3. The bandgap calculations presented in Chapter 4 were conducted by Torsten Wendav at institute for physics, Humboldt-Universität zu Berlin, for which he needs to be gratefully acknowledged.

My always hardworking students: Andreas, Youssef, Silvan, Aleksei and Mathias deserve acknowledgment for their assistance with device fabrication and measurements. I would also like to thank Prof. Dr. Arnab Datta and Prof. Dr. Satinder K. Sharma for insight into the MOS capacitor systems and C-V measurement techniques.

Meiner Schwiegerfamilie, „die Mücks“, danke dass ihr für mich da seid. Nach Bad Reichenhall zu fahren, ist für mich immer ein Höhepunkt. Danke, dass ihr für mich immer das Raclette angeheizt habt, und für die guaden Weißwürstl vom Gumping zum Sonntagsfrüstück.

Takk til mine utrolige gode venner som benyttet seg av anledningen til å komme og besøkte meg her i Tyskland. Særlig i de lange periodene på sommeren som gressenkemann, da ensomheten rådde. Tobias, Haakon, Glør, Mathias, Morten, Adrian, Einar, Kai og Lars, jeg håper dere fikk like stort utbytte av oppholdet som jeg fikk av besøket deres.

Takk Mamma og Pappa, for deres bunnløse støtte og deres urokkelige tro på at jeg ville klare å fulleføre doktorgraden. Dere vært svært gode å ha, og gjort meg trygg på at jeg gjorde et godt valg da jeg bestemte meg for å flytte til Tyskland med Isabel. Håper dere har fått noe igjen fra deres mange besøk til Tübingen.

Marie, takk for din positivitet og for at du fant det for godt å føre familiegenene videre i mitt fravær, og med dette satte mine gleder og nedturer litt i perspektiv. I tidvise hektiske perioder har det vært herlig å kunne koble av med oppdateringer fra Henrik og Morten. Lars, svigerbror, takk for at du har holdt meg i sjakk i denne krevende perioden.

Tante Randi og onkel Terje, takk for besøket og den supre ideen om at jeg trengte et vinkjøleskap. Et glass rødvin (T_{vin} = 16° C) venter dere som takk ved neste tysklandsvisitt.

Takk mormor for at du er så fin ei mormor. Takk for at du kom å besøkte meg i Tübingen. Selv om jeg vet at du hadde ønsket at avstanden mellom oss var mindre, håper jeg at du er stolt av meg.

Mest av alt vil jeg takke deg Isabel, for at du har vært, og forhåpentligvis vil forsette å være, min bedre halvdel. Takk for at du har pushet meg, støttet meg, fått meg til å le, og at du er den nødvendige entusiastiske motvekten til min treeeeege trønderske personlighet. Takk for at du har tatt meg med ut i verden. Takk for at jeg sammen med deg har fått sett og opplevd så mye, som jeg vet jeg aldri ville ha klart på egen hånd. Jeg elsker deg utrolig mye, og gleder meg utrolig mye til fortsettelsen på vårt felles eventyr som birøktere, globetrottere, klatrere, fjellvandrere, katteeiere, hundeeiere og foreldre.

Curriculum Vitae

Name:	Erlend Granbo Rolseth
Date of birth:	02.08.1985
Place of birth:	Trondheim, Norway
Nationality:	Norwegian

Education:

1992-1998	Nidarvoll grunnskole
1998-2001	Sunnland Ungdomskole
2001-2004	Adolf Oeien Videregående skole
2006-2011	Norwegian University of Sience and Technology
	B.Sc and M.Sc. in Physics
2012-2016	Institut für Halbleitertechnik der Universität Stuttgart