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Experimental Demonstration of an Optimised PWM Scheme for More Even Device Electro-Thermal Stress in a 3-Level ANPC GaN Inverter

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Abstract

GaN device as one potential power electronics device has been gained much attention recently. One of the power conversion systems, ANPC inverter using GaN HEMT is potentially considered to be prospective usage of low loss and high efficiency. In this work, we demonstrate one optimised PWM scheme aims at balancing the device electro-thermal stress based on Parma PWM to control 3-Level ANPC GaN inverter. The method is to decrease the loss for switches account for the large loss and increase the loss for switches with less thermal stress initially. The simulation and experimental results prove the effectiveness of the optimised PWM in controlling the loss distribution.

1 Introduction

Although the applications of GaN HEMT are still in their infancy, in recent years, the GaN HEMT has emerged as a promising device for high frequency, high efficiency, high density power conversion due to a better figure of merit than comparable Si and SiC transistors. [1] The review of recent progresses in the development of wide band gap power semiconductor devices and the introduction of their basic applications such as Sic and GaN rectifiers are summarized in [2] in 2015.

In the past century, plenty of topologies of DC/AC inverters have been created to comply with different application requirement. [3] One class of the topologies, half-bridge topologies, are popular due to natural rejection of high-frequency common mode voltage variation at the output of the inverter that causes high leakage current injection to grid. Half-bridge topologies require double voltage input in comparison to full-bridge topologies, nevertheless various topologies show that they can maintain competitive efficiency with minimum number of components. [4]

The Active Neutral Point Clamped (ANPC) inverter is a member of half-bridge neutral point clamped inverter family, introduced in [5], [6] as an alternative to neutral point clamped (NPC) inverter for improved loss balancing and better utilization of semiconductor chip areas in the inverter. [7] A new attempt of a fully GaN HEMT based ANPC inverter, which aims to explore the benefits of the use of such device technology on the system level efficiency, power density and reliability was presented by Emre in [8] using normally-off p-gate GaN HEMTs by Panasonic. One of the modulation strategy based on reverse conduction capabilityfor GaN HEMT and SiC devices in [9], employing parallel conduction of the devices during the freewheeling phases of the output current in order to pursue high power efficiency. However, the obvious limitation that the imbalanced loss distribution among each switch decreases the lifetime and the reliability of the system.

In this paper, the new optimised PWM are presented in order for more even device electro-thermal stress among six switches in 3-Level single phase ANPC inverter. Section 2 introduces the theories of new optimised PWM and their loss calculation. Section 3 shows the simulation and experimental results and discussion for the new modulation scheme and followed by a possible improvement in section 4.

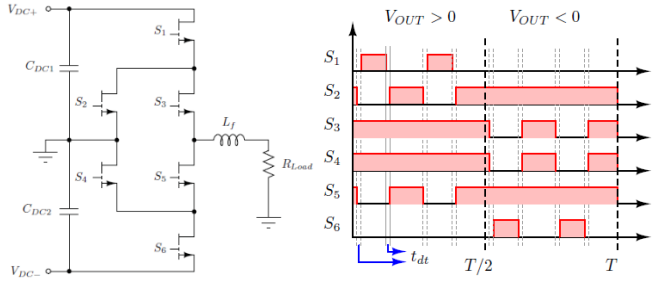
2 ANPC inverter and two PWM schemes

2.1 ANPC inverter topology and comparison of two PWMs

Figure 1(a) and (b) shows the ANPC topology and the original PWM. Table 1 summarizes the switching states for 3L ANPC inverter. The positive voltage is applied to the output of by turning-on S_1 and S_3 and the output current flows through the two devices in series. During the positive active-state, S_4 ensures an equal DC-link voltage sharing between S_5 and S_6 without conducting any current. The transition from positive active-state to zero-state is accomplished by switching S_1 off, and then simultaneously switching S_2 and S_5 on, and thus the current is divided in two parallel paths: S_2-S_3 and S_4-S_5. Same commutation scheme is used for complementary switches during the negative active state and the zero-state. This modulation method ensures low conduction losses at zero-states, and the outer switches (S_1 and S_6) are exposed to switching losses at unity power factor. Hence, the synchronous rectification capability of the transistors is utilized during zero state conduction. [7]

It is obvious that S_2 only works in zero (0P, 0N and 0PN) states which will account for the minimum power loss. S_1 and S_3 have larger power loss due to positive-active ($+V_{DC}$) switching

states. The same condition also happens in lower side. Therefore, the optimised PWM is designed to decrease the loss



(a) [9] (b) [9]

Figure 1: (a) Schematic of 3L ANPC inverter and (b) Parma PWM

Table 1 Switching states

Output State	S_1	S_2	S_3	S_4	S_5	S_6
$+V_{DC}$	1	0	1	1	0	0
0_P	0	1	1	0	0	0
0_N	0	0	0	1	1	0
0_{PN}	0	1	1	1	1	0
$-V_{DC}$	0	1	0	0	1	1

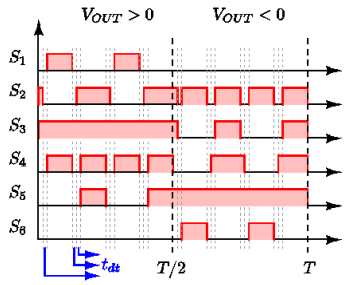


Figure 2. Optimised PWM for 3L ANPC inverter

for S_1 and S_3 but increase the loss for S_2 (same for the lower side). On one side, optimised signal introduces an extra dead time without affecting the commutation between zero and active states, but increase the number of switch in zero states for S_2 and S_4. On the other side, a time length which is the same as the dead time is substracted from the total conducting time for S_1 and S_3 every time when they are on, hence the conduction loss for S_1 and S_3 will decrease. The efficiency of two PWM schemes are expected to be the same.

2.2 Loss calculation

Conduction loss analysis for each switch for PWM shown in Figure 1(b) were presented in [10]. The similar conduction loss calculation for optimised PWM control is summarized in Table 2:

Table 2 Conduction loss for upper side devices

Switch	Conduction loss
S1	$P_{cond_{S_1}} = P_{cond\_a} + 2P_{dt_1-bp} - 2P_{dt_{red}}$
S2	$P_{cond_{S_2}} = \frac{P_{cond\_z}}{2} + 3P_{dt_2-bp} - \frac{3P_{dt\_red}}{4}$
S3	$P_{cond_{S_3}} = P_{cond_a} + \frac{P_{cond_z}}{2} + 2\left(P_{dt_1-up} + P_{dt_2-bp}\right) - \frac{3P_{dt_{red}}}{4}$

P_{cond_a} and P_{cond_z} are the conductive loss for active and zero states respectively. P_{dt_red} is the reduction in conduction loss. P_{dt1_bp} corresponds to dead-time conduction loss when the gate-source voltage is below threshold and P_{dt1_up} corresponds to dead-time conduction loss when the device is turned on. P_{dt2_bp} corresponds to reverse conduction dead-time losses at the positive half of the output when the device is turned-off, and P_{dt2_up} corresponds to increased conduction time at the negative half of the output voltage. [10]

For the switching loss, assume the switching energy is constant and the switching loss is $P_{sw} = E_{sw}f$. For unipolar PWM used in this experiment, the number of switching angle $n = f_{carrier}/f_{modulating}$. Therefore, the switching loss for upper side switched are summarized in Table 3.

Table 3 Switching loss for upper side devices

Switch	Switching loss
S1	$P_{sw_{S_1}} = 0.5n(E_{on} + E_{off})$
S2	$P_{sw_{S_2}} = 1.5n(E_{on} + E_{off})$
S3	$P_{sw_{S_3}} = 0.5n(E_{on} + E_{off})$

Due to symmetry and simplification, the lower side loss is the same as the upper side. Therefore, the total loss is $P_{loss} = P_{conduction} + P_{switching}$ where $P_{conduction} = 2(P_{cond_{S1}} + P_{cond_{S2}} + P_{cond_{S3}})$ and $P_{switching} = 2(P_{sw1} + P_{sw2} + P_{sw3})$.

3 Results and discussions

3.1 Simulation results

The plecs was used to simulate 3L ANPC inverter with two different PWM schemes. The device was chosen as normally off p-gate GaN HEMT with the output characteristics shown in figure 5, followed by table 5 shows the simulation parameters. Thermal model in plecs was constructed using figure 3.

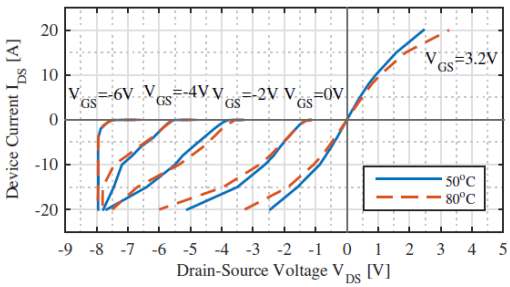


Figure 3 output characteristics of GaN device used [10]

Table 5 simulation parameters

DC link voltages (V)	400, 700
Output RMS Voltages (V)	122, 230
Output Power (W)	500, 1K
Carrier frequency (KHz)	16, 32, 64, 128, 160
Output Filter inductance (mH)	1.6 (for 16KHz and higher)
DC link input Capacitance (mF)	4
Dead-time (ns)	500
Modulation index	0.88

The typical loss distribution for two PWM are shown in Figure 4.

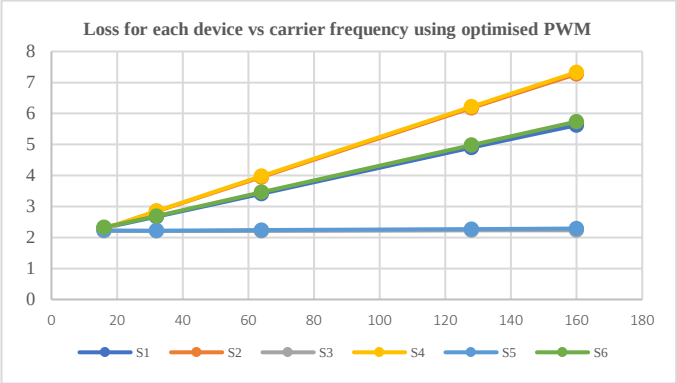


Figure 4 (a)

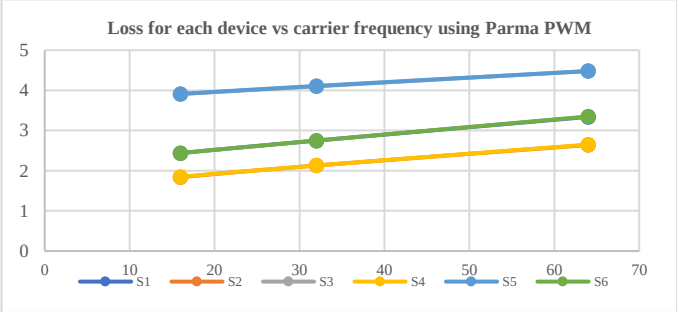


Figure 4 (b)

Figure 4: Power loss distribution for each device when input power is 400V, output power is 1KW. (a) Optimised PWM (b) Parma PWM

From Figure 4 (a), the optimised point for balanced loss distribution is when input voltage is 400V, output power is 1KW and carrier frequency is 16KHz. Therefore, optimised PWM prefers low frequency and low power.

3.2 Experimental settings

The ANPC inverter used was designed by Emre and the introduction of the device can be found in [10]. The top view of the inverter is shown in Figure 5

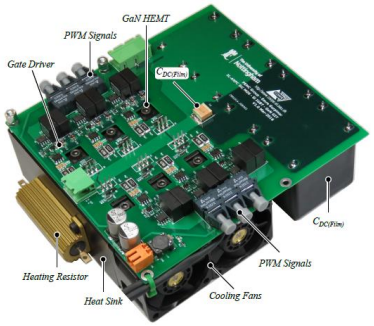


Figure 5 Top view of the ANPC inverter prototype [10]

It embeds the fiber optic receivers for transfer of PWM signals from an FPGA board, individual isolated gate drivers for each switch, film decoupling capacitors and a temperature controlled thermal management device, consisting of two cooling fans and two heating resistors mounted at the sides of a heat-sink to decouple the parametric temperature study from load conditions and switching frequency. [10]

The gate driver design still uses hard switching but the switching loss could be less compared with conventional squared pulse. The design method and pulse construction shown in Figure 6.

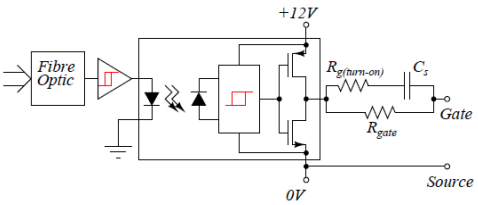


Figure 6 (a) [10]

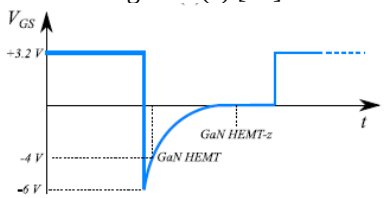


Figure 6 (b) [10]

Figure 6: (a) Schematic of GaN HEMT gate driver (b) Gate driver pulse

Figure 7(b) shows the experimental settings, the connection was based on figure 7(a).

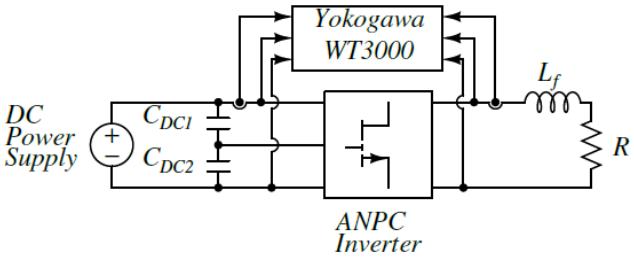


Figure 7(a) [10]

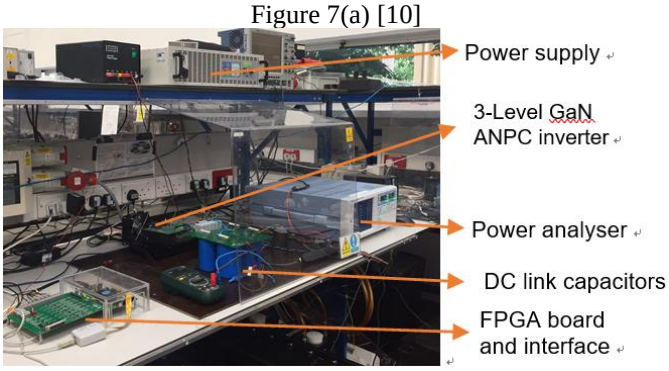


Figure 7(b)

Figure 7: (a) Schematic of test connection (b) Photo of experiment settings

3.3 Experiment results

The experiment was done when input voltage was 200V and output voltage was 250W. In order to find loss distribution of each device, we measured the case temperature of each device by thermocouple because the temparature is proportional to the loss. To avoid the bulk heatsink balancing the loss distribution automaticlly, we used individual small heatsink

with fans. The initial tempareture for each device should be almost the same. (the difference should less than 1 degree). The real-time temperature waveform could be seen on Picolog recorder. After all the devices reached the steady state, the steady state tempratures were recorded. The steps were the same for both original Parma PWM and the optimised one. The temparature data were summarised in Table 4 and Table 5.

Table 4 Temprature records for Parma PWM

Switch	Temparature measurement for Parma PWM (degrees)	
	Initial temp.	Steady state Temp.
S1	25.2	33.3
S2	25.1	32
S3	25.0	34.1
S4	25.0	31.1
S5	25.0	34.4
S6	25.1	33.1

Table 5 Temparature records for Optimised PWM

Switch	Temparature measurement for Optimised PWM (degrees)	
	Initial temp.	Steady state Temp.
S1	25.3	33.8
S2	25.2	32.7
S3	25.1	32.8
S4	25.2	32.4
S5	25.2	33.6
S6	25.3	33.3

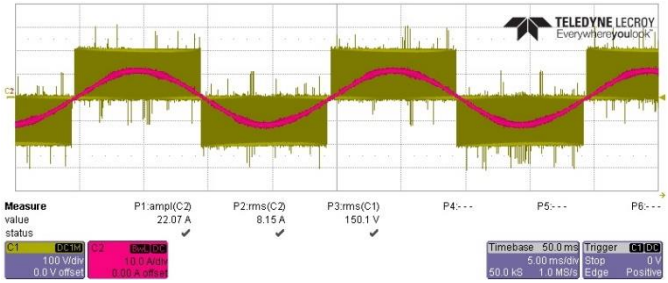


Figure 7 The output current after filtering and output current before filtering

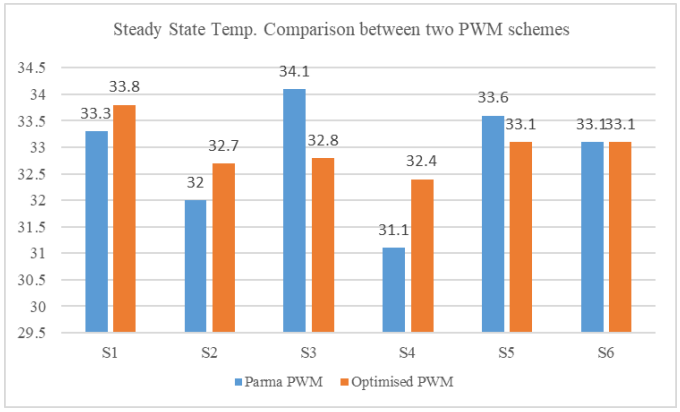


Figure 8 The comparision of steady state temprature between two PWM control schemes

Figure 7 shows the output waveforms of current and voltage, the current and voltage was measured before replacing the bulk heatsink by inidividual heatsinks. The input was 400V and output power was 1KW.
From Figure 8, the loss for S2 and S4 increase whilst the loss for S3 and S5 decrease. The loss distribution using optimised PWM is more banlanced than original PWM. Furthermore, the efficiency measured by power analyzer shown that the efficiency for parma and optimised PWM are 99.071% and 99.054% respectively.

4 Conclusion and future work

The loss control and generalization of inverter will be much easier if the balanced loss distribution could be achieved. Parma PWM was designed to achieve high efficiency and the Parma PWM based optimised PWM aims to balance the power loss as well as maintaining high efficiency are proved to be effective experimentally.

The switching loss was increased by adding more number of switching times for switches which only work in zero states, and the conduction loss was decreased by one dead time interval for every conducting time for the switches work in both active and zero states. The simulation results show that the most optimised point to achieve the same loss distribution is when input voltage is 400V, output power is 1KW and carrier frequency is 16KHz. The power loss is around 2W for each switch.

The experiment was done only in low input and low output condition because the use of small individual cooling systems which could not withstand high output power. High temperature will damage the device. Therefore, a newly designed individual cooling system is under experimenting which can solve the problem in the future.

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