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GaN HEMT Gate-Driver for Achieving High Power Converter Integration Levels

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Abstract

This work proposes a solution for implementing an isolated gate driver for GaN HEMTs based on the previous topology for SiC power MOSFETs. The isolation of the gate driver is realised by the single transformer topology with double winding in the secondary side. The Bi-level HF Amplitude Modulation scheme is retained to avoid the core saturation as well as providing simultaneously both the switching signal and the required gate power in the secondary side which ensures the full range duty ratio. The reconstruction of the original PWM signal is optimised using a simple hysteresis comparing scheme, which is the Schmitt Trigger circuit, to avoid sudden turn-on or turn-off. The experiment result shows that the Schmitt Trigger circuit could effectively avoid the sudden turn-on or turn-off but it might have some negative effect on the accuracy of duty circle. Finally, the feasibility of the gate driver is demonstrated with the PGA26E19BA GaN device with optimised final power stage.

1 Introduction

Recently, GaN-based devices are finding rapidly growing interest in power conversion applications. From the amplifier point of view, GaN-based HEMTs (High Electron Mobility Transistors) shows many advantage over other existing technology [1]. It has demonstrated one-order higher power density and high efficiency over Si-based and GaAs-based RF transistors. In addition, the high switching capability of GaN could effectively reduce the size of power system due to the miniaturization of passive components such as inductors, capacitors and transformers. Furthermore, it could also operate at high temperature and has better noise performance [2]. However, the design of compact and reliable gate driver is one of the challenges in the power converter design.

This work aims to propose an isolated gate driver for GaN HEMTs based on square waveform bi-level modulation scheme [3]. The switching PWM signal is modulated with HF (1MHz) square waveform, providing a pure AC signal. This modulated signal has two different levels indicating the turn-on and turn-off intervals respectively. Therefore, there will always be an input waveform at transformer and it provides require gate power on the secondary side even at low duty ratio. In addition, this modulated signal has ideally no DC component which could effectively avoid the core saturation. However, some inevitable noise will be introduced in the demodulation level in the secondary side which would cause the unwanted sudden switching of the PWM signal. This is optimised using the simple Schmitt Trigger circuit and has effective outcomes. In order to demonstrate the feasibility of the proposal, the gate driver has been built and tested with PGA26E19BA GaN device. Due to the limitation of the proper heat sink and fan, it was only tested with low drain-source current. It is worth to mention that the final power stage has been optimised with decreasing turn-off voltage.

2 Descriptions of proposed gate diver

2.1 System Block Diagram

Fig.1 shows the system block diagram of the proposed gate driver [3] [4]. The PWM signal is modulated with 1MHz oscillating square waveform generating the symmetric two level modulated signal $u_{Pri}(t)$ on the primary side of the transformer. The two windings on the secondary side of the transformer provide the reconstructed PWM switching signal $u_{Rect}(t)$ and constant voltage levels $u_o(t)$ and $u_{Ref}(t)$ respectively [5]. The diode rectifier is used to generate $u_o(t)$ which is the supply of the secondary side. The switching signal $u_{Rect}(t)$ enters a comparator and a power stage before reaching the final stage. It is worth to mention that a simple hysteresis comparing scheme is used to improve the This final power stage is supplied by the $u_o(t)$ and $u_{Ref}(t)$ which is required to match the V_{gs} turn-on and turn-off voltage, i.e. 3.5V and -4V.

2.2 Design specification and circuit simulation

The gate driver is designed to supply the PGA26E19BA GaN device which has 1.2V threshold voltage (VTH) and 3.5V typical gate forward voltage so the turn-on and turn-off voltage have been redesigned and the main parameters are shown in Table I [6].

Table I: Main parameters of the gate driver

Parameter	Symbol	Value
Switching frequency	f_s	120kHz
Modulation frequency	f_m	1MHz
Duty ratio range	D	0% - 100%
Gate-Source turn-on voltage	V_{gs_on}	3.5V
Gate-Source turn-off voltage	V_{gs_off}	-4V

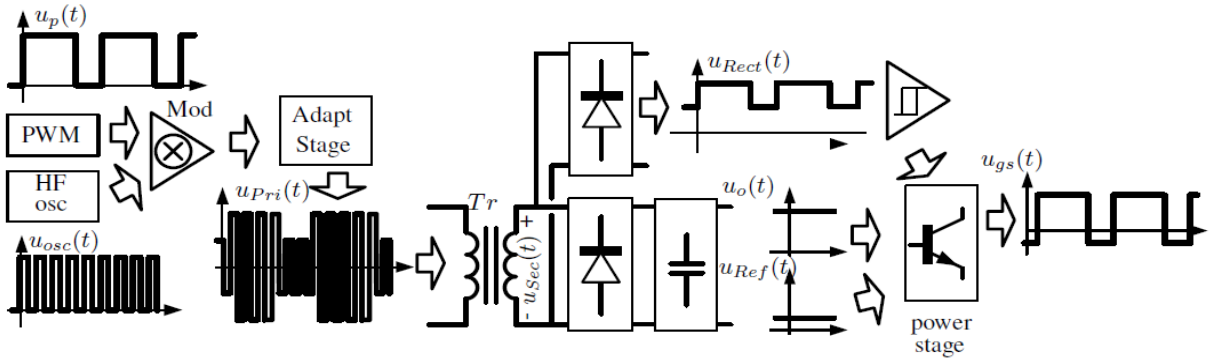

Fig.1 System block diagram

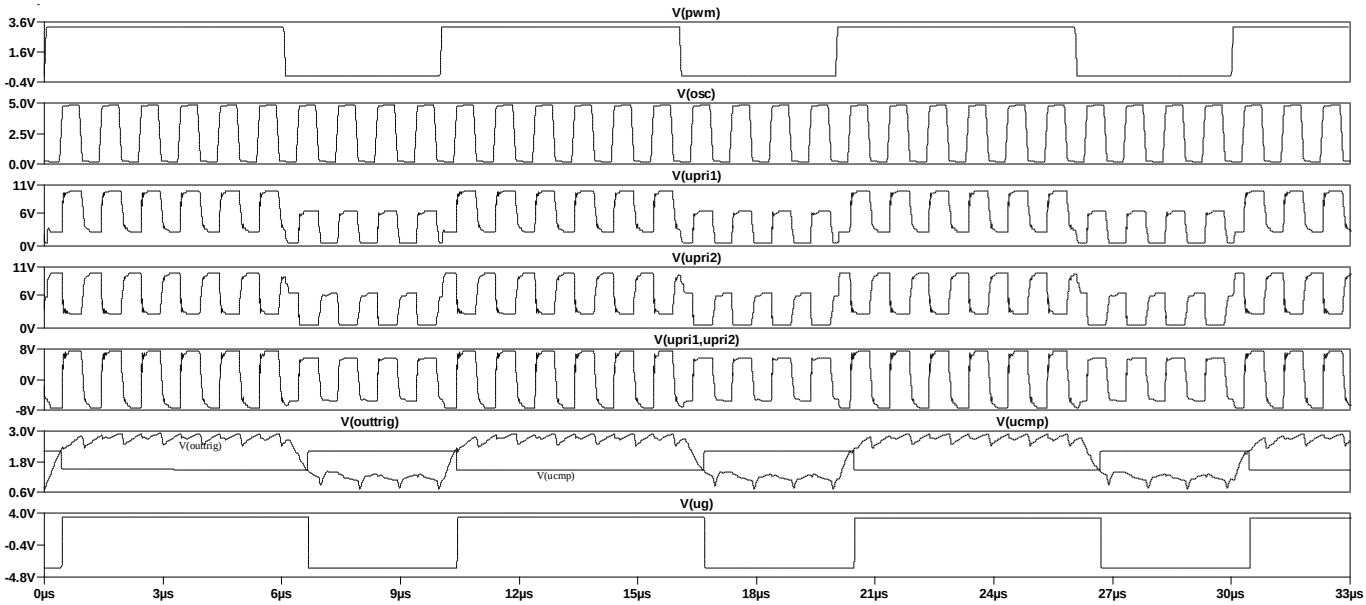

Fig. 2 Simulation waveforms of the proposed gate drive

The block at Fig.1 have been designed and simulated in *LTSpice*. The 1MHz oscillation signal is generated by implementing the MC14093BDG from *ON Semiconductor*. A ring core of 3E5 magnetic material (TX10/6/4 core size from *Ferroxcube*) has been implemented for the transformer. The comparators in the modulation stage and output stage are the LM319 from *TI*. The CPH5506-TL-E from *ON Semiconductor* has been implemented in the adapt stage on the primary side and the output power stage on the secondary side. The diode pairs in the secondary side have been implemented using MMBD4448H-7 from *MOUSER*. Fig.2 shows the simulation waveforms of the designed gate driver. As it can be seen, the driver provides desired output waveform. A 100kHz, 60% duty ratio PWM signal V(PWM) is modulated with 1MHz oscillation signal V(osc). The complementary modulated signal V(upri1) and V(upri2) are connected to the two ports of the transformer on the primary side with the overall waveform shown by V(upri1,upri2). The hysteresis comparing scheme is implemented so the V(ucmp) shows the hysteresis voltage level. This could effectively improve the noise immunity of the gate driver. The final gate voltage V(ug) shows proper turn-on and turn-off voltage. Although there is a slight delay between the PWM signal and gate signal, this effect could be solved with proper control scheme.

2.3 Circuit Testing

The proposed gate driver is built and tested in the next stage. Fig. 3 to Fig. 10 show the experimental waveforms of the built prototype with the 1 MHz oscillation signal and 120 kHz, 50% duty ratio PWM signal. The turns ratio of the transformer is 7:17 with double winding on the secondary side. The output V_{gs} leaves open at this stage and will be connect to the PGA26E19BA GaN device later. The whole power dissipation of the gate driver is approximately 2.5W.

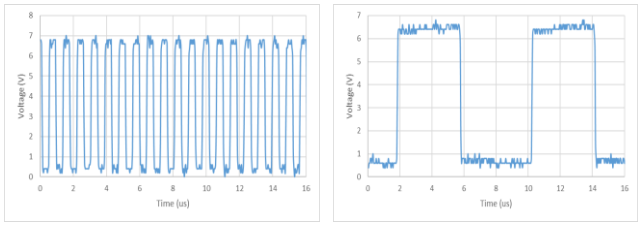

Fig. 3 and Fig. 4 1MHz oscillation signal $u_{osc}(t)$ and 120kHz, 50% duty ratio input switching signal $u_p(t)$

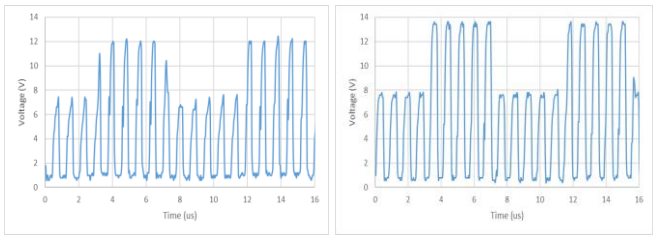

Fig. 5 and Fig. 6 Complementary modulated sinal $u_{Pri\_1}(t)$ and $u_{Pri\_2}(t)$

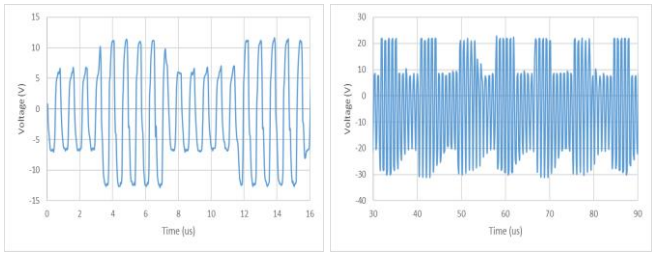

Fig. 7 and Fig. 8 Signals that transformer see on the primary side and secondary side

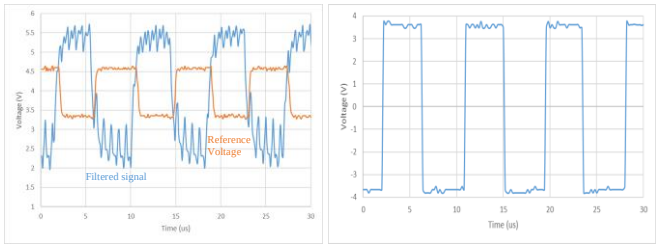

Fig. 9 and Fig. 10 Inputs of final comparater with hysteresis comparing scheme and the final gate-source voltage

It is worth to mention that initially, the hysteresis comparing scheme was not implemented as shown in Fig. 11 and Fig. 12 [7]. The constant reference voltage cuts through the 'glitching' which would lead to the unwanted switching in the gate signal. Even if the constant reference voltage is carefully chosen, this situation will be inevitably happened. Therefore, a simple Schmitt Trigger feedback circuit is implemented to improve the system noise immunity. However, the feedback loop increases the delay time between the input PWM signal and output gate signal in both turn-on and turn-off. This delay time is required to be considered in the control scheme.

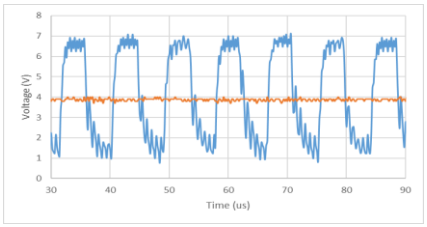

Fig. 11 Inputs of final comparator with constant reference voltage

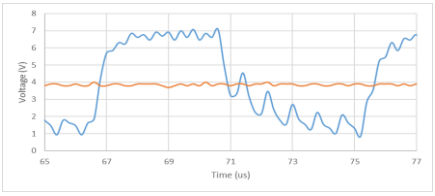

Fig. 12 Unwanted cross due to the noise in the filtered signal

3 Experimental validation and discussion

The gate driver has been tested with PGA26E19BA GaN device. The GaN device is connected in series to an eight 5.6Ω in parallel (approximately 1.2Ω in total by multimeter) and it is powered by a voltage source. As the level of voltage source increasing, the drain current steady increases but the temperature of the GaN device increases dramatically. When the supply voltage reaches 6V and the maximum drain current reaches 4A, the surface temperature is above 170°C which is above the safety level. Due to the limitation of the proper heat sink and fan, the voltage source is set as 5V and the surface temperature of PGA26E19BA GaN device is approximately 100°C. The gate-source voltage (V_{gs}), drain-source voltage (V_{ds}) and drain current (I_d) has been measured and shown in Fig. 13, Fig. 14 and Fig. 15 respectively. The prototype of the proposed driver has been shown in Fig. 16.

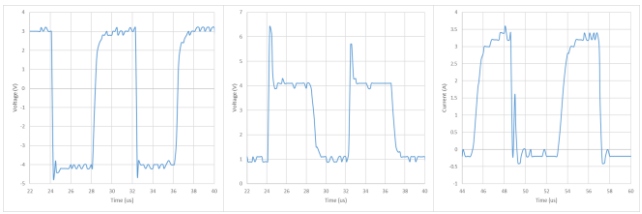

Fig. 13, Fig. 14 and Fig. 15 Input gate-source voltage (V_{gs}), Drain-source voltage (V_{ds}) and Drain current (I_d) respectively

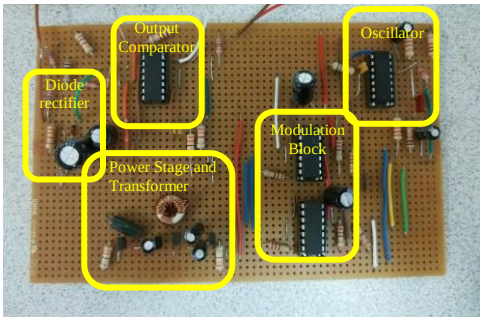

Fig. 16 Prototype of the gate driver

Notice that when the Vgs turns on, the V_{ds} decreases to approximately 0.9V and the I_d increases to approximately 3.2A. Due to the drain-source on-state resistance (RDS_{ON}) is typically 290mΩ when the temperature of the device is 150℃, the voltage across the drain and source are theoretically 0.928V which is approximately equal to 0.9V. The ringing due to the high *dV/dt* can be seen in the gate voltage but this oscillation does not reach the threshold voltage.

The rise and fall time at the gate-source voltage shown in Fig. 14 is approximately 400ns and 200ns respectively which is relatively slow. This is because the initial current peak is not high enough to charge up the gate capacitor in a short time. In addition, the rise and fall time at the drain-source voltage shown in Fig. 14 is approximately 200ns and 500ns respectively which is more than 10 times slower than the common switching time [8] [9] The similar situation happens for the drain current. One possible reason is that the lack of proper heat sink and fan causes the surface temperature exceed the safety margin which slows down the turn-on and turn-off transient time. Plus, the parasitic capacitor of the wires and tracks in the circuit have negative effect on the switching transient performance. These parasitic capacitors could be minimised by a well-designed PCB.

In order to optimise the switching performance and reduce the power dissipation, the turn-off gate bias voltage was deceased in amplitude during the off-time with the circuit in Fig. 17 [10].

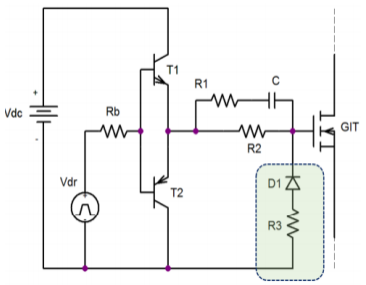

Fig. 17 The final power stage of the gate driver

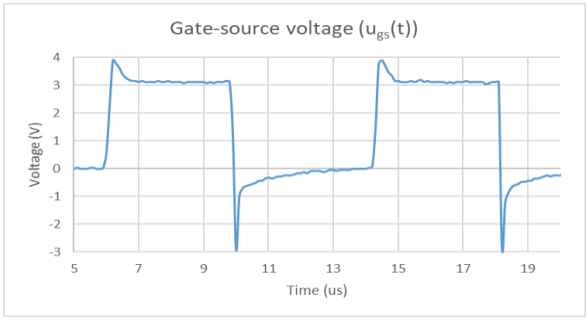

Fig. 18 The gate-to-source voltage with decreasing negative bias voltage

The gate-source voltage provided by the updated power stage has been shown in Fig. 18. The negative turn-off peak voltage is approximately -3V and it decays to 0V during the off-time. The D1 and R3 here is implemented to speed up the decreasing of the negative voltage amplitude.

4 Conclusion and future work

The isolated gate-driver for GaN HEMTs device has been designed based on the previous topology for SiC power MOSFET. The Bi-level HF amplitude modulation scheme is implemented to avoid core saturation as well as to allow providing the both switching signal and constant voltage level on the secondary side. The on and off voltage is designed to be 3.5V and -4V respectively based on the data sheet of PGA26E19BA GaN device. The hysteresis comparing scheme is implemented to optimise the noise immunity of the gate driver. The operation of the proposed gate driver has been simulated with full component model under LTSpice Environment. In the final stage, the gate driver is test with PGA26E19BA GaN device. Due to the limitation of proper heat sink and fan, the surface temperature of the GaN device reaches the safety margin when the maximum drain current reaches 4A. The turn-on and turn-off transient of the GaN device is uncommonly slow compared with the similar test. This might be caused by the high operation temperature and the parasitic capacity introduced by the track and wires. Finally, the final power stage has been optimised with the decreasing negative bias amplitude during the off-time.

Future developments include the optimisation of turn-on and turn-off switching time, high voltage and high power implementation, optimised PCB design and etc.

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