Trap assisted tunneling and its effect on subthreshold swing of tunnel field effect transistors

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We provide a detailed study of the interface Trap Assisted Tunneling (TAT) mechanism in tunnel field effect transistors to show how it contributes a major leakage current path before the Band To Band Tunneling (BTBT) is initiated. With a modified Shockley-Read-Hall formalism, we show that at room temperature, the phonon assisted TAT current always dominates and obscures the steep turn ON of the BTBT current for common densities of traps. Our results are applicable to top gate, double gate and gate all around structures where the traps are positioned between the source-channel tunneling region. Since the TAT has strong dependence on electric field, any effort to increase the BTBT current by enhancing local electric field also increases the leakage current. Unless the BTBT current can be increased separately, calculations show that the trap density $D_{\rm it}$ has to be decreased by 40-100 times compared with the state of the art in order for the steep turn ON (for III-V materials) to be clearly observable at room temperature. We find that the combination of the intrinsic sharpness of the band edges (Urbach tail) and the surface trap density determines the subthreshold swing.

I. INTRODUCTION

The Tunnel Field Effect Transistor (TFET)[1] is a candidate for low power switching in digital logic circuits for replacing or supplementing standard CMOS technologies because of its potential to reduce power dissipation via reduction of the power supply voltage. In a TFET, over-the-barrier thermionic emission is completely bypassed by triggering a BTBT current by the gate voltage, allowing steep "subthermal" change of current and reduced supply voltage. It has been shown that a small reduction in the subthreshold swing (SS) (e.g. to 45-53 mV/dec) in TFET can reduce the dynamic power dissipation by at least 50%[2,3] with little sacrifice on the switching delay. Such energy saving is calculated for the same OFF current but lower ON current (compared to the CMOS). The energy savings may enable high frequency operation that currently CMOS cannot provide. Further improvement is possible if higher ON current is achieved, which can be done with III-V semiconductors and heterojunctions[4].

However, the ideal picture of TFET operation is based upon the assumption that the Band To Band Tunneling (BTBT) current is sufficiently higher than any background current that flows before the bands overlap. In an ideal TFET operation, very little current should flow for gate voltages below a threshold voltage (defined as the gate voltage when the conduction band bottom in the channel and the valence band extrema in the source first overlap) and a large amount of current should flow above that. Such notion of steep (or ideal) switching is practically difficult to achieve since the combined leakage current, e.g. gate or substrate leakage, bulk or interface trap assisted tunneling will always be present and can easily obscure steep change of the BTBT current near the threshold voltage. In addition, the steepness of the current change partly depends on the BTBT magnitude and since it can be weak for multiple reasons, achieving the steep change of current is highly challenging. Despite numerous efforts in this field, experimental demonstrations with steep turn ON are few[5–10] and mostly at very low current levels. Most of the demonstrations involved silicon, for which the interface and bulk defect density is by far the best compared to other materials. Except for Refs.[9,11], most TFET experimental results on III-V semiconductors[12–14] do not show subthermal switching. On the contrary the subthreshold swing in these experiments shows strong temperature dependence, clearly indicating the existence of a thermal process. Two dimensional layered heterostructure based TFETs have attracted significant attention in recent times with one experiment[15] showing low subthreshold swing. But similar structures by other groups[16,17] have failed to produce such behavior.

In this work, we show that interface trap assisted tunneling (TAT) current, which is known as a leakage current mechanism in conventional *pn* junction diodes[18,19], is also a major parasitic current component in TFETs. TAT is the emission of electrons to a trap state via electron-phonon interaction, followed by tunneling into the conduction band (Fig. 1). Similarly a hole emission and tunneling from a trap is possible. This process is strongly temperature dependent compared to other non-idealities such as exponential band tails from the heavy source doping[20]. Such interband transition is also possible when phonon scattering is considered alone. Models with phonon scattering (without traps) have shown higher OFF current without sacrificing much on the subthreshold swing[21]. Although TAT has been identified in the past as a leakage mechanism in TFETs[12,22–26], a detailed quantitative study of its deleterious effects has not been performed. We show that in the presence of traps, electron capture rate prescribed by the Shockley-Read-Hall (SRH) formalism is greatly enhanced due to the high electric field near the source. This is due to the fact that the undesirable electron tunneling from trap to conduction band depends on the local electric field (Fig. 2), in much the same way as the ON state BTBT current. We

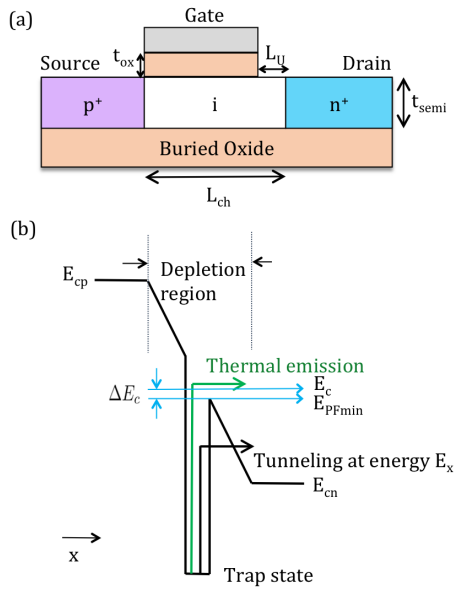

FIG. 1. (a) Schematic of the top gate device considered in this paper. (b) Schematic of the trap assisted tunneling (TAT) process: an electron can reach the conduction band from the valence band via a combination of phonon absorption and tunneling. This undesired tunneling is electric field dependent in the same way as the ON state BTBT current. The electric field enhanced generation rate is much higher than the classical Shockley-Read-Hall (SRH) formalism that does not take the electric field into account.

show that at room temperature this TAT current overshadows the steepest part of the BTBT current (Fig. 3) for realistic trap density (midgap $D_{\rm it} = 5 \times 10^{12}/{\rm cm}^2$-eV for III-V). The steep turn ON of the BTBT current is observable at low temperatures, where the BTBT dominates and the subthreshold swing becomes less temperature dependent. In our model, we consider the Poole-Frenkel effect[27] - the lowering of the electron barrier due to the Coulomb interaction of the trap with the lattice. We find that the Poole-Frenkel effect causes a substantial increase in the leakage current by enhancing the trap-channel tunneling. In the next section, we review the electric field dependent SRH formalism, the electrostatic model and the BTBT model used in this paper followed by discussions. The formalism is also applicable to most other device geometries and materials provided that the $D_{\rm it}$ is known and the electrostatic configuration is solved appropriately.

II. MODEL DESCRIPTION

In this section, we review the electric field enhanced carrier generation rate via phonon and trap states. We incorporate the Poole-Frenkel effect and the tunneling enhanced rates as done in Refs.[19,27] but apply them using the TFET electrostatics and consider only the surface trap states. The electric field profile from the electrostatic model is used in calculating both the TAT and BTBT current.

A. Trap assisted tunneling

The classical SRH formalism[28] describes the generation rate of electron and hole pairs in presence of traps. An electron in the valence band (VB) can absorb a phonon to reach a trap state before emitting to the conduction band (CB) by interaction with another phonon. However, in the presence of electric field, the trap-CB (or VB-trap) tunneling rate becomes substantial and greatly increases the electron-hole generation rate[19]. The net generation rate (per unit area) at a given position in the *pn* junction space charge region becomes,

$$G^n = \int \frac{n_i^2 - np}{\tau_p \frac{n+n_1}{1+\Gamma_p} + \tau_n \frac{p+p_1}{1+\Gamma_n}} D_{\rm it}\, dE \qquad (1)$$

where n_i is the intrinsic carrier concentration, n and p are the electron and hole densities, τ is the minority carrier lifetime and Γ is a factor that accounts for the tunneling from trap to CB. With $\Gamma = 0$, Eq. 1 reduces to the classical SRH formalism. The carrier lifetime depends upon the capture cross section and the thermal velocity, $\tau = 1/(\sigma v_{th})$. Γ is electric-field-dependent and it effectively decreases the minority carrier lifetime. When the electric field is weak, Γ is negligible and Eq. 1 reduces to the classical SRH formalism. The terms n_1 and p_1 arise from the principle of detailed balance[28] and are given by $n_1 = n_i {\rm exp}^{(E_t - E_i)/k_B T}$, $p_1 = n_i {\rm exp}^{(E_i - E_t)/k_B T}$, where E_i and E_t are the position of the Fermi level for intrinsic semiconductor and the trap state. Fig. 1b schematically shows the TAT, which is a two-step process. In the first step, the electron is emitted from the valence band to the trap state by absorbing a phonon. Afterwards, the electron can be partially lifted further and then tunnel into the conduction band. The amount of the partial lift in the second step can vary from E_{cn}, the position of the CB in the channel, to E_c the position of the CB at the position under consideration. Within the energy range $E_{\rm PF} < E < E_c$, electrons reach the conduction band without any resistance since there is no barrier to tunnel, whereas for $E_{cn} < E < E_{\rm PF}$, the transmission probability $T(E)$ through the barrier has to be accounted for. Therefore the enhancement factor Γ is the sum of two components, one for each energy regime

$$\Gamma = \Gamma_{\rm PF} + \Gamma_{\rm tunnel} \qquad (2)$$

Γ is calculated from the net flux (carrier density times the thermal velocity) and the transmission probability[27],

$$\Gamma = \frac{1}{k_B T} \int {\rm exp}(\frac{E_c - E_x}{k_B T}) T(E_x) dE_x \qquad (3)$$

E_x is the energy to which the electron (or hole) is tunneling to (Fig. 1b). $T(E_x)$ is calculated for a triangular

barrier using the Wentzel-Kramers-Brillouin (WKB) approximation.

$$T(E_x) = \exp(-\frac{4\sqrt{2m^*(E_{\rm PF}-E_x)^3}}{3q\hbar F}) \quad (4)$$

where F is the electric field at a particular position in the depletion regime for a given gate voltage. For $E_{\rm PF} < E < E_c$, $T(E_x) = 1$. From Eq. 3 it can be shown,

$$\Gamma_{\rm tunnel} = \frac{\Delta E_{n,p}}{k_B T}\int_0^1 \exp[\frac{\Delta E_{n,p}}{k_B T}u - K_{n,p}u^{3/2}]{\rm du} \quad (5)$$

$$\Gamma_{\rm PF} = \frac{1}{4}\exp(\frac{E_c - E_{\rm PF}}{k_B T})$$

$$K_{n,p} = \frac{4}{3}\frac{\sqrt{2m^*\Delta E_{n,p}^3}}{q\hbar F}$$

where $\Delta E_c = E_c - E_{\rm PF}$ is the lowering of the barrier (Fig. 1b) due to the Poole-Frenkel effect. $\Delta E_{n,p}$ is effectively the tunnel barrier height and it also defines the range of energy to which the electron (or hole) can tunnel to (from the trap). So $\Delta E_{n,p}$ is the difference between the top of the barrier and the minimum energy where the electron can tunnel to. Depending upon the position (in the depletion region) under consideration, this can vary from $\Delta E_{n,p} = E_{\rm PF} - E_t$ (if $E_t > E_{cn}$) to $E_{\rm PF} - E_{cn}$ (if $E_t < E_{cn}$)[19]. The higher the Poole-Frenkel effect, the higher the ΔE_c and the higher the Γ's in Eq. 5. For typical electric fields, the second term in Eq. 5 (which signifies the tunneling contribution), dominates over the first term and increases the exponential term for smaller $\Delta E_{n,p}$ or larger F. The lowering of the energy barrier ΔE_c is determined by the electric field[29–31] $\Delta E_c = q\sqrt{qF/(\pi\epsilon)}$, where ϵ is the electric permittivity. The Γ's are calculated for both electron and hole (so that all combinations of phonon absorption and tunneling as shown in Fig. 1b are included in the model) and used in Eq. 1.

Performance degradation in TFET can take place even without the traps due to inelastic phonon scattering[21,32]. The OFF current is increased in addition to making the transfer I-V ambipolar. But the phonon limited subthreshold swing can still be less than 60 mV/dec. Traps on the other hand increase the carrier capture rates to a large extent so that the leakage current dominates over the desired current. TAT affects both the ON-OFF current ratio and the subthreshold swing.

Fig. 2b shows the total enhancement Γ (Eq. 2) in silicon with and without the Poole-Frenkel effect. Γ can be as high as 10^8, which is effectively the enhancement of the SRH rate. Typical TFET electric fields operate around $1 - 5 \times 10^6$ V/cm, over which the Γ changes by less than two orders of magnitude.

Finally the current is calculated from,

$$I/W = q\int G^n(x)\,dx \quad (6)$$

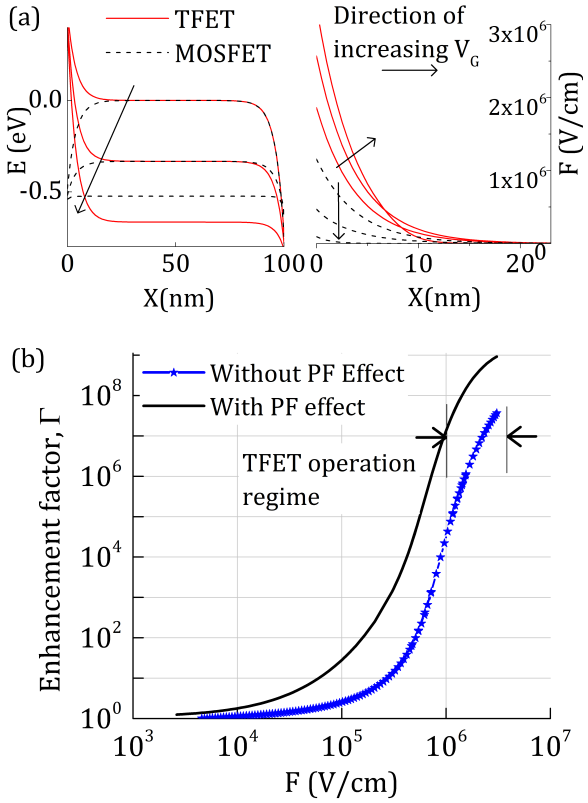

FIG. 2. Relationship of trap assisted tunneling with electric field (F) in tunnel FET. (a) Conduction band profile and the corresponding electric field for silicon TFET at various gate voltages. Solid lines are for TFET and the dotted lines are for a MOSFET configuration. The electric field is increased in TFET as much as possible with gate voltage to increase the band to band tunneling, but in the process it also increases the undesired trap to conduction band tunneling. For the MOSFET on the other hand, the electric field is reduced with gate voltage, taking the trap effects out of the picture. (b) Carrier lifetime is decreased as a result of trap assisted tunneling by a factor 1+Γ. Γ is large for the typical electric fields in TFETs and increases the generation rate in the source-channel pn junction. Here, Γ vs. F is shown at the beginning of the channel ($x = 0$).

B. Electrostatic model

As derived in[33], we use an abridged version of the 2D Poisson equation for the top gate structure shown in Fig. 1a. For an SOI structure, the electric field at the top and bottom surface of the semiconductor (given by the oxide thickness and gate potentials) can be applied to the 2D Poisson equation and can be simplified as

$$\frac{d^2\psi}{dx^2} - \frac{\psi - \phi_{gs}}{\lambda^2} = -\frac{\rho}{\epsilon} \quad (7)$$

where ψ is the surface potential and $\phi_{gs} = V_G - V_{FB}$ is the gate potential. Eq. 7 captures the 2D electrostatics quite well for a given characteristic length λ. For the top gated architecture, $\lambda = \sqrt{\frac{\epsilon_{\rm semi}}{\epsilon_{\rm ox}}t_{\rm ox}t_{\rm semi}}$. The charge density in

the channel is mainly dictated by the drain injection, since the channel is poorly coupled to the source

$$\rho \approx -q\, n_0 \exp^{(\psi - V_{DS})/k_B T} + q p_0 \exp^{-\psi/k_B T} \qquad (8)$$

where n_0 and p_0 are the equilibrium electron concentration in the channel. Eqs. 7 and 8 are solved iteratively until self-consistency is achieved. For a given ρ, the potential ψ is calculated numerically from Eq. 7 using the finite difference method subject to appropriate boundary conditions (for the doped regions). Eq. 7 is also valid for double-gate and gate-all-around nanowire structure if the characteristic length λ is changed appropriately[33].

Fig. 2a (left) shows the conduction band profile. On the right, we show the electric field for various gate voltages. For the TFET configuration, the electric field near the source end is greatly enhanced. For a MOSFET configuration on the other hand, the energy barrier (and the conduction band) is pushed down resulting in a decreased electric field near the source. This opposite trend in the electric field with gate voltage, results in a drastically different TAT current in TFET compared to MOSFET since the TAT is dependent on the local electric field. The TAT for TFETs increases with gate voltage, while for MOSFETs it diminishes quickly (not shown). Therefore the role of traps in MOSFETs is mostly limited to a decreased gate efficiency, while for TFETs, it affects both the gate efficiency and leakage. In this paper, we did not account for the impact of reduced gate efficiency due to $D_{\rm it}$. Including it would only increase the subthreshold swing relative to what we show (depending on trap density and gate dielectric thickness).

C. BTBT model

The transmission probability through the tunnel barrier is determined by the WKB approximation[1]. It can be written as,

$$J_{\rm wkb} = a V_{TW} (\frac{F}{F_0})^P \exp(-\frac{b}{F}) \qquad (9)$$

where a, F_0, P and b are material parameters taken from[34] and[35]. $V_{\rm TW}$ is the tunnel window, i.e. the energy difference between the valence band in the source and the conduction band in the channel; it is determined by an Urbach tail below the threshold voltage and it increases linearly with gate voltage above the threshold voltage[35]. $V_{TW} = E_0 \log\Big[1 + \exp\Big(\frac{E_{\rm v,source} - E_{\rm c,channel}}{E_0}\Big)\Big]$. A difference between Ref.[35] and our approach is that we find the position of the conduction band after self-consistency is achieved between carrier density and channel potential, as discussed in previous sub-section. So for any given gate voltage, the position of the conduction band is $E_{\rm c,channel}({\rm V}_G) = E_{\rm c,channel}({\rm V_G} = 0) - \psi$. E_0 is the Urbach parameter and it determines the intrinsic subthreshold swing.

The Urbach tail has been studied in the past in order to understand the sharpness of the optical absorption spectrum in semiconductors. Instead of a steep rise in the absorption co-efficient above a threshold photon energy, experimental results typically show an exponential rise following $\alpha = \alpha_0 \exp\Big[-\frac{E - E_g}{E_0}\Big]$[36,37]. Such non-abrupt absorption has been attributed to the Urbach tail which originates in heavily doped semiconductors from the smearing of the dopant energy levels. It can also happen in undoped semiconductors due to electron-phonon interaction[38] with a lower Urbach parameter E_0. The temperature variation of E_0 is weak in doped semiconductors compared to an undoped one[39]. Unfortunately the exact nature of the Urbach tail and its temperature dependence of E_0 is not well understood[40]. In the next section, we will discuss the implication of various cases of Urbach tail and how it affects the TFET performance.

For a given gate voltage V_G, we solve as discussed for the self-consistent channel potential (Eq. 7) for the top surface $\psi(x)$ and the electric field $F(x) = -\frac{d\psi}{dx}$. Using the spatial electric field $F(x)$, we calculate the enhancement factors Γ from Eq. 3, carrier densities from Eq. 8 and x-dependent generation rate $G^n(x)$ from Eq. 1.

III. RESULTS AND DISCUSSION

We apply the model for the top gate structure shown in Fig. 1a. Effective oxide thickness (EOT), $t_{\rm ox}$ and semiconductor body thickness $t_{\rm semi}$ are 1 nm and 5 nm respectively. $D_{\rm it}$ profile in Ref.[41] is used for III-V with midgap $D_{\rm it}$ of $5 \times 10^{12}/{\rm cm}^2$-eV. Although $D_{\rm it}$ is a function of energy in the bandgap, we found that in most cases the midgap trap density dominates the trap current. Channel length, $L_{\rm ch}$ is 100 nm. Source and drain contact regions are degenerately doped while the channel is undoped. The capture cross-section for electrons, holes are $\sigma_n = 5 \times 10^{-17}\,{\rm m}^2$, $\sigma_p = 5 \times 10^{-18}\,{\rm m}^2$[27,42] and the carrier lifetimes are calculated from there using the thermal velocity, $v_{th} = \sqrt{\frac{8KT}{\pi m^*}}$. An underlap (10 nm long) at the channel-drain end is used to suppress the electric field in the drain end and therefore the ambipolarity. For the transfer curves, we use a drain bias $V_{DS} = 0.3$ V. We ignore channel resistance due to carrier scattering in the channel since the resistance due to TAT and BTBT is substantially higher.

Fig. 3a shows the transfer plots for $In_{0.53}Ga_{0.47}As$ TFET at various temperatures. For room temperature, the TAT and BTBT current components of the total current are also shown. Well above the threshold voltage ($V_t \sim 0.37$ V), the total current mainly comes from BTBT. The TAT current is just enough so that it intersects with the BTBT current near the threshold voltage, therefore the total current below V_t is dominated by the TAT. The TAT thus obscures the steepest part of the BTBT ($\sim$ 40 mV/dec in this calculation) and so the minimum subthreshold swing ($\sim$ 75 mV/dec) is lim-

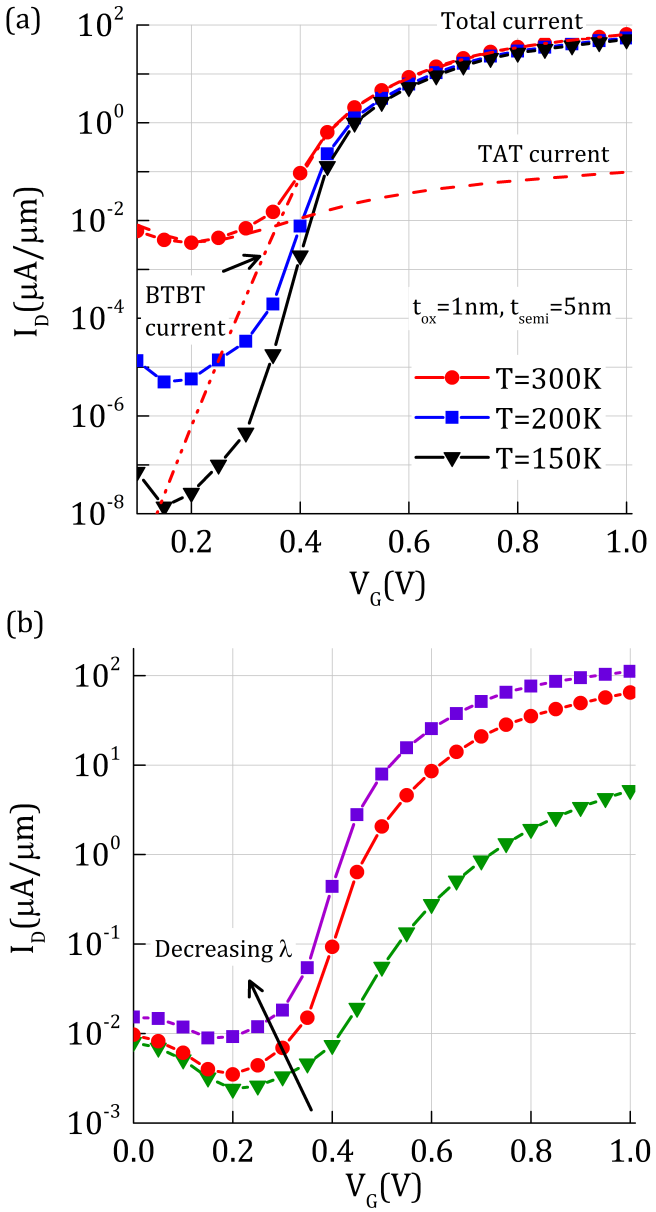

FIG. 3. (a) Total (TAT+BTBT) current in $In_{0.53}Ga_{0.47}As$ based homojunction TFET with the device structure as shown in Fig. 1 with EOT, t_{ox} and semiconductor thickness t_{semi} 1 nm and 5 nm respectively and a drain bias of V_{DS} = 0.3 V. BTBT follows WKB formalism above threshold (when the bands overlap), while below threshold the BTBT has an exponentially decaying transmission due to the band tails (Urbach tails, in this case at 40 mV/dec at 300 K, 25 mV/dec at 150 K). TAT is temperature dependent and obscures the steepest part of the BTBT current in the subthreshold regime ($\sim V_G < 0.4$ V) for temperatures above 150 K. Midgap D_{it} is assumed to be $5x10^{12}$/cm^2-eV. (b) Since both TAT and BTBT are electric field dependent, the thickness of the oxide and the semiconductor affects the current levels as well as the subthreshold slope. In this calculation, gradually decrease (from bottom to top) the thicknesses resulting in decreasing scaling lengths λ. t_{ox} is 2 nm, 1 nm and 0.75 nm and t_{semi} is 10 nm, 5 nm and 1 nm respectively. Even for very thin oxide and body thickness, TAT is large enough to overshadow the steep change of BTBT.

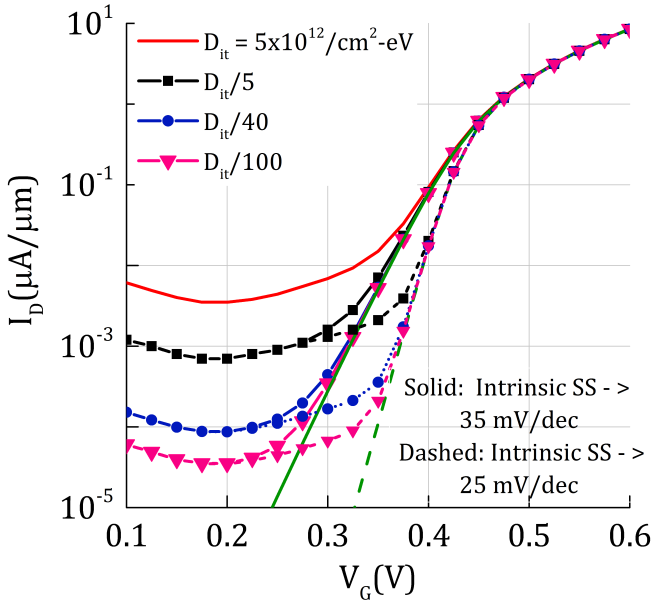

FIG. 4. Impact of D_{it} magnitude on the transfer characteristics for t_{ox} = 1 nm, t_{semi} = 5 nm for two different Urbach tail parameter E_0. Total current at different midgap D_{it} levels. At roughly 10^{11}/cm^2-eV (typical D_{it}/40), the TAT current is low enough for the steep BTBT current to be manifested (for two orders of magnitude at $\sim$ 40 mV/dec and $\sim$ 28 mV/dec).

ited by the rate of change of BTBT current just above the threshold voltage. This subthreshold swing will get much worse for thicker oxide and body thickness. Such transfer behavior with a valley near the minimum current is seen in most experiments on III-V TFETs[13,43,44]. At lower temperatures, electron hole generation rate is reduced leading to lower TAT. For temperatures lower than 200 K, intrinsic subthreshold swing is observed. The current above the threshold voltage is weakly dependent on temperature while current below the threshold varies stongly with temperature. In other words, the lowest achievable current at any given temperature is a function of temperature (decreases from $\sim$ 1 nA at 300 K to $\sim$ 10 fA at 150 K), similar to what is seen in the experiments[12–14,45,46].

To demonstrate the effect of the scaling length λ and the local electric field, Fig. 3b shows the transfer plots for different oxide and body thicknesses at T = 300 K. With t_{ox} = 0.75 nm and t_{semi} = 1 nm (violet squares), ON current increases substantially due to the increase of the local electric field near the source. Subthreshold swing also improves to $\sim$ 65 mV/dec which is still not subthermal. This is due to the fact that the TAT current has also increased, thus limiting the advantage of the higher electric field. We infer that the same effect takes place in heterojunction TFETs, making it difficult to observe subthermal switching for those structures as well.

Fig. 4 shows the transfer plots for various trap density for two different intrinsic subthreshold swings (Urbach tails at 35 and 25 mV/dec) with a motivation to find

the trap density required to achieve subthermal switching for multiple decades. We find that a trap density of 1.25×10^{11}/cm^2-eV, which is about 40 times smaller than today's typical midgap trap density, achieves about two orders of current change at $\sim$ 40 mV/dec. For the steeper intrinsic swing, we again get two orders of current change at subthermal rate ($\sim$ 28 mV/dec). In this case, the TAT and BTBT intersects at a higher V_G. Since the TAT increases with V_G, a steeper Urbach tail does not necessarily increase the ON-OFF ratio (at subthermal rate). Therefore the ON-OFF ratio at subthermal rate is determined mainly by the trap density, while the subthreshold swing is determined by the Urbach tails. We see this again when the trap density is reduced by 100 times, where we get about three orders of change in current at subthermal rate for both Urbach tails.

We applied the same model to silicon to see how the transfer characteristic changes at reduced trap density and different material properties. In Fig. 5, we see that both BTBT and TAT decrease substantially due to heavier effective mass and higher bandgap with a midgap trap density of 5×10^{10}/cm^2-eV, which is typical in today's silicon technology. Similar to III-V, the steepest part of the BTBT is not seen due to the TAT. However at 1×10^{10}/cm^2-eV, we found (dashed line) two orders of current change at 50 mV/dec (in pA range). Such $D_{\rm it}$ is much easier to achieve in silicon than the requirements mentioned earlier for III-V. This also explains, why most experiments reporting margin subthermal switching at very low currents involved silicon, where it is likely that such trap density may be achieved.

IV. CONCLUSION

We provide an analysis of the parasitic trap assisted tunneling current in TFETs. We show that in most cases, the subthreshold current in TFETs is dominated by TAT, regardless of channel material. The takeover from TAT to band to band tunneling depends on the temperature, electrostatic characteristic length, material parameters (e.g. effective mass) and the rate of change of the exponential band tails (Urbach tails). We show that engineering efforts to increase the ON current are also likely to increase the subthreshold current, since both BTBT and TAT are driven by the same mechanism (tunneling through a barrier). The TAT current is much more deleterious than just the electron-phonon scattering without traps. We find that to get a reasonable ON-OFF ratio with steeper than 60 mV/dec subthreshold swing at room temperature, trap density has to be reduced by 40-100 times compared to the state of the art for III-V semiconductors, for reasonable structural device parameters.

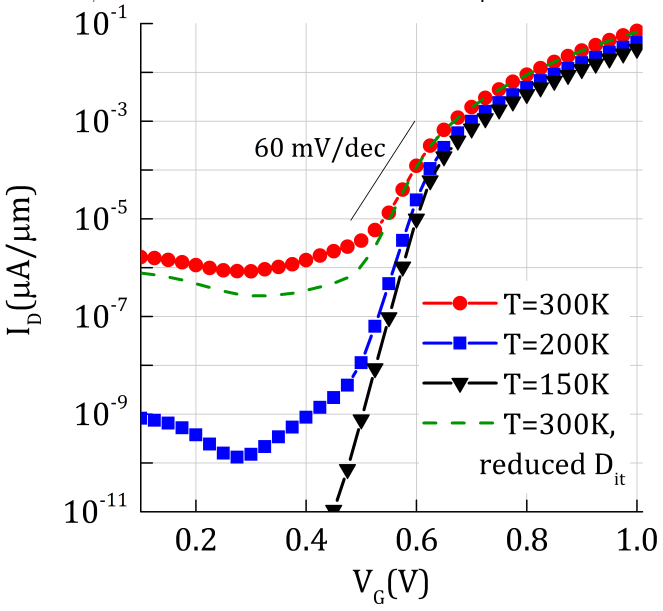

FIG. 5. TAT+BTBT current at different temperatures for homojunction silicon TFET $t_{\rm ox}$ = 1 nm, $t_{\rm semi}$ = 5 nm. Since silicon has much lower $D_{\rm it}$ (mid gap density assumed here is 5x10^{10}/cm^2-eV), TAT to BTBT transition takes place at a higher temperature ($\sim$ 200 K) compared to III-V. For a slightly lower midgap $D_{\rm it}$ of 1×10^{11}/cm^2-eV (dashed), we get two orders of current change at 50 mV/dec at room temperature.

V. ACKNOWLEDGMENT

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