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Fault blocking converters for HVDC transmission:
a transient behaviour comparison

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Abstract

A thorough comparison of the transient behaviours of two state-of-the-art converters suitable for HVDC transmission is presented. The Alternate Arm and Mixed-Cell Modular Multilevel Converter topologies both have DC fault blocking capability and are selected for the comparison. Converter performance is evaluated and compared under various transient conditions including charging sequence, unbalanced operation, and DC fault recovery. The study is conducted using high-fidelity converter simulation models, integrating detailed controllers that reflect real-scale projects. The main findings of the study assist in the selection of the most suitable converter, given specific performance specifications such as capacitor voltage ripple, cell capacitor requirements, and response during transient operation.

1 Introduction

In multi-terminal HVDC systems, converters with DC blocking capability are an attractive solution due to their ability to quickly recover from DC-side faults. The Modular Multilevel Converter (MMC) [1], [2] and the Alternate Arm Converter (AAC) [3], [4] are both the subject of considerable industry and research interest, and are therefore the focus of this study. Both MMC and AAC topologies include full-bridge cells which can reverse the cell voltage and therefore block DC current. MMCs may be based on two alternative structures with blocking capability: namely the Full-Bridge MMC (FB-MMC) and the Mixed-Cell MMC (MC-MMC)[5], where the MC-MMC exhibits better efficiency. A converter station must be protected from overvoltage stresses in order to sustain the lifespan of the semiconductors, insulation, etc., and overcurrent to avoid equipment overheating. Moreover, transient phenomena must be supressed in order to secure robust operation of the AC and DC grids. The full spectrum of transient behaviours needs to be observed in order to conclude which topology is more viable for a given application. A well-designed set of tests, employing accurate time-domain models [6], developed using the EMTP-RV power systems transient simulation and analysis software suite, is used to evaluate and compare the relative merits and performance trade-offs between different converter implementations, during the charging sequence, unbalanced AC faults, and DC faults. The study is conducted with due consideration to efficient use of simulation resources and

realistic attributes that can be reflected through real-scale projects. Converters are compared using performance indicators such as cell capacitor voltage ripple, arm current, and DC- and AC-side voltages and currents.

2 Simulation set-up

In Fig. 1(a) the MMC topology is illustrated. Each MMC arm includes a series connection of Full-Bridge or Half-Bridge cells which determine the characteristics and attributes. Specifically, in the case of HB-MMC the operational modulation index is only positive and, consequently, there is no DC fault blocking capability. In addition, the total semiconductor losses are kept low. If, however, the installed cells are a mixture of HB and FB cells, the operational modulation index can also be negative, leading to more flexible operation. Specifically if the ratio of FB to HB cells exceeds 50 % then the converter can block DC faults at the expense of increased losses. Fig. 1(b) shows one phase of an AAC. Each AAC arm consists of an array of series-connected FB cells, referred to as a 'chainlink', and a series connection of IGBTs which forms the director switch (DS). Due to the FB cells, an AAC can block DC faults whilst the semiconductor losses are kept relatively low. However, the AAC requires a DC filter in order to ensure acceptable DC power over a wide operating range [7], [8].
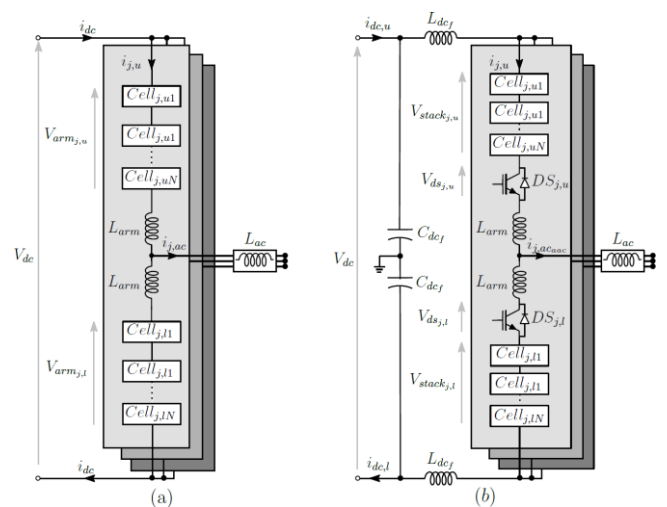

Figure 1: (a) MMC, (b) AAC

In order to validate the operation of the converters and their dedicated controllers[4],[10], a point-to-point HVDC network

is utilised as depicted in Fig. 2. The network consists of two converters in a symmetric monopole configuration which are connected via DC cables (represented using the wideband cable model). Table 1 describes the attributes for each topology that were used.

Table 1

Parameter	AAC	MC-MMC
S [MVA]	1045	1045
V_{dc} [kV]	640	640
V_{chain}/V_{DS} [kV]	388/604	640
V_{grid}/V_{conv} [kV]	400/500	400/320
Arm inductance [mH]	11.14	65.36
Phase reactor [mH]	37.8	-
Cell capacitance [μF]	397	651
Number of levels	20	20

In each test, Converters 1 and 2 in Fig. 2 are of the same type in order to avoid interactions due to mixed converter topologies.
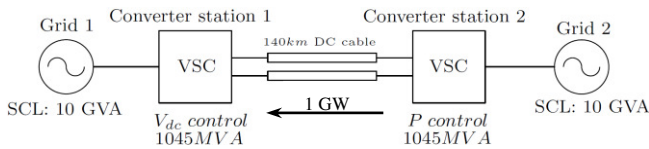

Figure 2: Point-to-point test DC network.

Fig. 3 represents an HVDC converter station. The AC-CB is the AC circuit breaker capable of clearing AC faults and disconnecting the converter from the AC network. The transformer is necessitated in order to acquire galvanic insulation between the DC network and the AC grid while it matches the AC converter and grid voltages and adjusts the converter voltage according to the DC voltage level. Moreover its leakage reactor filters harmonics and enables the AC current control. In some cases it is employed with the converter controller to adjust the voltage through tap changers to regulate the circulating currents. The AC-side pre-insertion resistors (AC-R) are employed during the charging process from the AC side in order to reduce the inrush currents that affect the converter. Usually they are inserted/bypassed with the help of a slow mechanical switch. The main converter topology can be either of those shown in Fig. 1. The DC-side resistors have the same functionality as the AC-side resistors (DC-R), being responsible for controlling inrush currents that originate from the DC grid, when the converter is energised from the DC side. DC-D is a slow mechanical DC disconnector which isolates the converter from the rest of the DC grid. Its operation is similar to that of the AC-CB but, since it can only be opened when current flowing through it is near zero, it cannot be used to clear DC faults. Unlike its AC counterpart, this device need a specific design to be capable of closing almost simultaneously to avoid voltage unbalance when the DC cable is already energized.
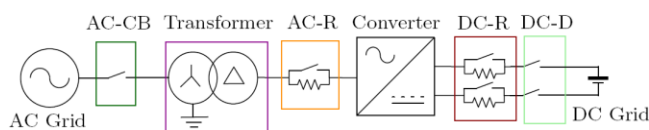

Figure 3: Converter station equipment.

3 Start-up operation

It is commonly shown in literature that the energisation process is simultaneous, meaning that many of the transient effects may be absorbed as all the converters and the DC link charge at the same time [11], [12]. This may not, however, be the case in multiterminal grids where a converter may need to be isolated and then reconnected a short time later, whilst the rest of the grid remains operational. Also DC charging is crucial for start-up operation where the converter is connecting to a weak grid. Furthermore, it is necessary that the converter that controls the DC voltage is always charging from the AC side: this converter assumes the role of "slack bus" which regulates the DC voltage. Also, in order to provide an active current path between the AC and DC sides, the FB cells must operate as HB cells, where the charging path also allows the cables to be charged [13].

3.1 MC-MMC

The energisation sequence timings are logged in Table 2. In MMC station 1, the AC-CB is closed at t=0.1s connecting the converter with the AC grid whilst the AC-R resistors are inserted, thereby minimising inrush current. Moreover at t=0.1s, the converter enters the passive charging state, imitating a blocked HB-MMC where the converter is in a blocked state that allows AC current to charge the cell capacitors while the DC cables are also charged.

Table 2

MMC station 1 (charging from the AC side)		MMC station 2 (charging from the DC side)	
AC-CB closed	t = 0.1s	AC-CB closed	t = 1.3s
AC-R bypassed	t = 0.65s	AC-R bypassed	t = 1.5s
Cells released	t = 0.25s	Cells released	t = 1.3s
Active charging	t = 0.8s	Active charging	t = 1.3s
DC-D closed	t = 0.1s	DC-D closed	t = 1s
DC-R bypassed	t = 0.1s	DC-R bypassed	t = 1.6s

At t=0.25s the cells are released from HB to FB mode and the capacitors continue to charge simultaneously as the DC voltage increase. When the cell capacitor voltages are equal to the AC RMS line-to-line voltage, the cells are unblocked and enter the normal controlled operating mode to complete the charging cell capacitor and DC voltage charging. Also at this time, MMC station 1 establishes the DC network voltage, which increases to its nominal value.

The ramp rate of the DC voltage controller reference affects the switching frequency, which leads into increased energy dissipation and temperature of the IGBTs. At t=0.8s the converter average switching frequency shows a distinct increase due to the rate of change of the cell voltages as the converter enters in the active charging state. Just after t=1s, MMC1 switching frequency reduces, as the average capacitor voltage is within the tolerance band and the capacitor voltage balancing algorithm (CBA) is no longer saturated.

At t=1s, when the DC voltage achieves its nominal value, DC-D closes allowing MMC2 to connect to the DC network. At this time, the DC-side charging procedure starts, as shown in Fig. 4, by the passive charging period of MMC2. The DC inrush current is limited by the MMC station 2 DC-R. At t=1.3s the AC-CB of MMC 2 closes enabling synchronisation

of the converter with the AC grid. Meanwhile the MMC 2 cell capacitors charge, but do not achieve their nominal voltage due to the voltage drop across the DC insertion resistors, DC-R. The effect on the arm voltages of connection to the AC grid can be observed from Fig. 4(f), where at that moment the converter controller takes its reference from the AC grid and regulates the arm voltage according to the AC voltage.
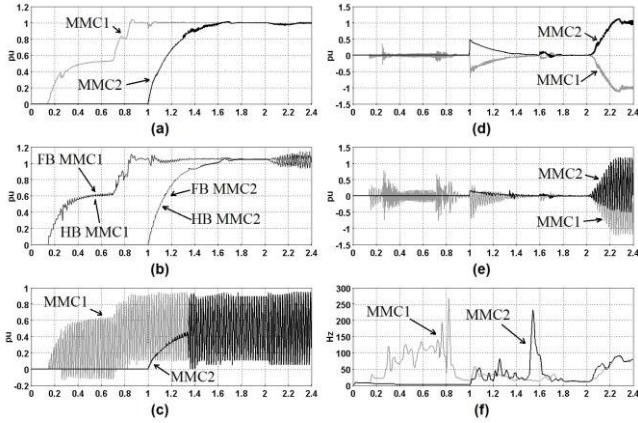

Figure 4: (a) DC voltage, (b) total cell capacitor voltage, (c) arm voltage, (d) DC current, (e) arm current, (f) cell average switching frequency.

The AC-R are disconnected at t=1.5s, affecting the switching frequency of MMC 2, due to the recovered AC voltage drop. At t=1.6s the DC-R are disconnected, leading to a mild DC current overshoot due to the sudden DC voltage increase. At t=1.8s the cell capacitor voltages in both converters are at their nominal values, DC voltage is set without any undesirable oscillation, and all residual currents are zero. As a result, at t=2s the power reference is now set to its nominal value. As a result, at t=2.4s the AC and DC voltages and currents in both converters operate at their desired values.

3.2 AAC

At the beginning of the passive charging sequence, the current phase may shift significantly due to the inrush currents resulting from the series cell capacitors. This leads to a mismatch between the calculated overlap time for the DS and the time required for the stored energy in the inductances to be exchanged between the upper and the lower converter arms. Due to the energy stored in the inductances, high overvoltage occurs during DS overlap. Therefore an appropriately sized RC snubber is employed for the DS, which absorbs the fast energy exchange from the arm inductors, and a surge arrester is employed across DS, for protection against overvoltages during IGBT commutation when the current is high [14]. As the AAC common-mode current profile is different to that in the MMC, overcurrent or overvoltage must be limited at valve level. Table 3 describes the start-up sequence of the AAC. The AC-CB is closed at t=0.05s and the AAC is connected to the AC grid with the AC-R active. Moreover the FB cells are unblocked from the beginning in order to reduce the dynamic transient resulting from FB cell insertion/bypass, while the DS operate to regulate each phase current every half-cycle of the fundamental. The converter operates in passive charging

mode until the DC voltage is equal to the AC RMS line-to-line voltage.

Table 3

AAC station 1 (charging from the AC side)		AAC station 2 (charging from the DC side)	
AC-CB closed	t = 0.05s	AC-CB closed	t = 1.5s
AC-R bypassed	t = 0.65s	AC-R bypassed	t = 1.9s
Cells released	t = 0.05s	Cells released	t = 1.3s
DS unblock	t = 0.05s	DS unblock	t = 1.3s
Active charging	t = 0.8s	Active charging	t = 1.3s
DC-D closed	t = 0s	DC-D closed	t = 1.4s
DC-R bypassed	t = 1s	DC-R bypassed	t = 1.55s

However due to the fact that in AAC, the chainlink voltage rating is chosen to support only a portion of the DC voltage, the capacitor voltages are charged to the chainlink blocking voltage. This is shown in Fig. 5(a) where the DC voltage reaches 500kV at approximately t=0.5s, while the capacitor voltages have a similar profile but the voltage magnitude is less, as shown in Fig. 5(d). At t=0.85s the DC voltage starts to ramp up to its nominal value, which is reached at t=1s. Additionally, at t=1s the DC-R are bypassed.

With regard to AAC station 2, the fast DC-D closes at t=1.4s with the DC-R employed and the AC-CB open, whilst the cells are enabled at t=1.3s. Due to the sudden connection of the DC voltage to AAC2, a high inrush DC current appears but does not exceed the nominal value, as is shown in Fig. 5(f). At t=1.5s the AC-CB of AAC station 2 closes, enabling converter synchronisation with the AC grid. Due to the inrush current, the capacitor voltages are rearranged through the capacitor balancing algorithm leading to increased switching frequency, observed in Fig. 5(h). At t=1.8s the DC-R are bypassed resulting in further inrush current due to the resulting voltage increase, as is illustrated by the arm currents in Fig. 5(g). Lastly the AC-R are bypassed at t=1.9s without any noticeable effect as the controller is settled and the voltages are at their nominal values. The converter increases power to its nominal value at t=2s, with a natural under-voltage on the DC link and small disturbance in the grid frequencies. The capacitor voltages are fully balanced around the desired value.
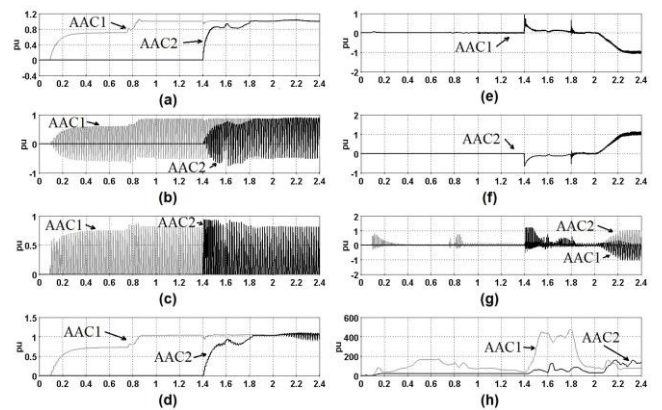

Figure 5: (a) DC voltage, (b) chainlink arm voltage, (c) Director Switch voltage, (d) total cell capacitor voltage, (e) DC current AAC1, (f) DC current AAC2, (g) arm currents, (h) cell average switching frequency.

4 Unbalance grids

HVDC converters are likely to experience unbalanced conditions due to phase-to-ground or phase-to-phase faults. It is possible to comply with the Grid Code regarding fault ride through by employing control systems which make it possible to keep the converter connected for a long period during unbalance AC faults without tripping. There are various types of AC faults, such as symmetrical AC, single line-to-ground, line-to-line and line-to-line-to-ground. However in order to illustrate the fundamental operation of the AC fault ride through (FRT) only a line-to-line fault is applied, as illustrated in Fig. 6. In the following case studies, converter 2 is affected by an AC fault where resistance of 4.5Ω is deliberately connected between phases a and b, at t=0.9s and lasting for 0.3s. The worst-case scenario is considered, where the fault occurs on the grid side of the transformer without any cable connected to the grid.

4.1 MC-MMC

The results for an unbalanced fault applied to an MC-MMC are shown in Fig. 6. Power transfer through MMC station 1 is reduced, due to the unbalanced fault at MMC station 2. With regard to the affected converter MMC station 2, the faulted lines are indicated by the significant drop in grid voltages shown in Fig. 6(a). Although the three-phase voltages at the grid side are severely unbalanced, the double-frame controller [15] provides effective support and maintenance of the AC currents by keeping the zero sequence components to zero, as reflected in converter AC current shown in Fig. 6(d). Furthermore, the proportional resonant (PR) controller [16] ensures that the magnitudes of the circulating currents are small even during the unbalanced operation, which results in minimum penetration of second-order harmonic into the DC voltage and current. Additionally from Fig. 6(f) it is clear that each converter phase contributes to each faulted phase of the AC network in order to maintain balanced AC currents. The overall strategy achieves AC current control with minimal DC current and voltage oscillation, while capacitor voltage ripple is kept low, as shown in Fig. 6(c).
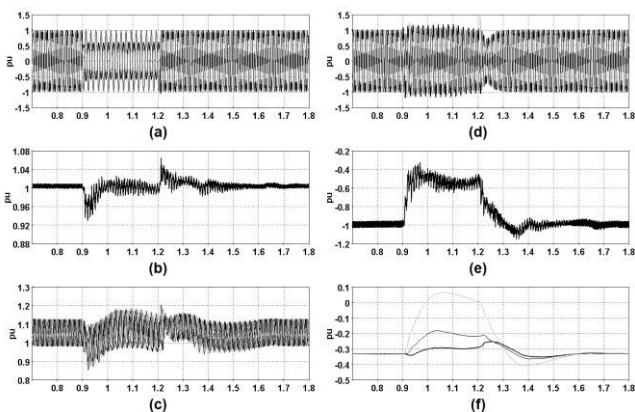
Figure 6: (a) Grid-side AC voltage, (b) DC voltage, (c) total cell capacitor voltage, (d) converter-side AC current, (e) DC current, (f) common-mode current.

4.2 AAC

During the unbalanced fault, the affected converter AAC2, regulates the AC currents effectively by keeping the zero-sequence current to zero, as can been seen from the AC currents shown in Fig. 7(d) and the current contribution from the common-mode current in Fig. 7(f). However, due to the fact that the AAC2 does not have any circulating current controller to regulate the double fundamental frequency oscillations, they are transferred to the DC voltage and current. The high-frequency currents affect the capacitor voltages, leading to temporary collapse of the voltage balancing process, as illustrated in Fig. 7(c). As a result, the AAC2 DC current and voltage are distorted by high magnitude and frequency components, which impacts the DC network (other converter terminals, cables, etc.), as can be observed from Fig. 7(b) and 7(e).
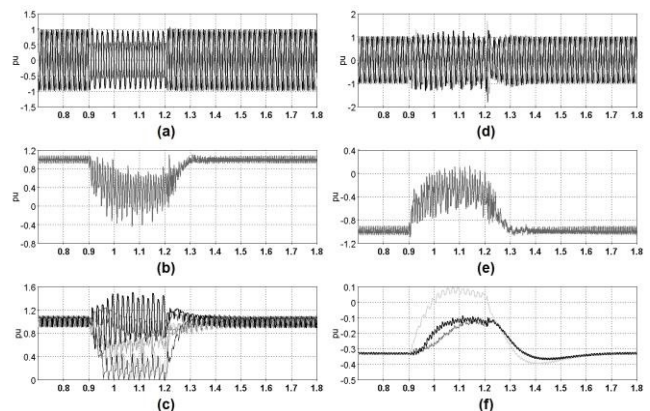
Figure 7: (a) Grid-side AC voltage, (b) DC voltage, (c) total cell capacitor voltage, (d) converter-side AC current, (e) DC current, (f) common-mode current.

5 DC pole-to-pole fault

A temporary DC pole-to-pole fault, of 5ms duration, is applied at the midpoint of the DC cables (70km from each converter) of Fig. 2. The case study will examine the DC-fault reverse blocking and controlled recharge capabilities of the MMC and AAC in order to improve the DC fault survival of the symmetrical monopole HVDC link, whilst keeping the current and voltages stresses on the converter stations within tolerable limits.

5.1 MC-MMC

The converters detect overcurrent in the DC current measurement and enable the 'block' command in order to switch off all the semiconductors in the converter cells. At the instant the DC fault occurs, the current rises to approximately 3.5p.u. whilst the DC voltage collapses to zero. The capacitor voltages are locked in the blocked state, with minimum decay through parallel-connected bleed resistors. The arm currents shown in Fig. 8(e) experience a fault current which is within the limits of what can be tolerated by the IGBTs.

After a time interval, the converter attempts to recommence operation by detecting whether or not the fault has been cleared. The method of detecting whether or not the fault is permanent is by operating the FB cell as an HB (similar to the start-up sequence). An arbitrary check at t=1.1s shows that

DC voltage has reached 80% of its nominal value, and that the fault is cleared. After a time delay, the converter cells are fully unblocked, and the DC link assumes its nominal voltage. As shown in Fig. 8(e), a high inrush current flows to charge the capacitors back to the nominal voltage. Following this, the DC and capacitor voltages are correctly set. As a result, at t=1.5s the controller begins to ramp up the power, meaning that the time between the fault and recommencement of full operation is less than 1s.
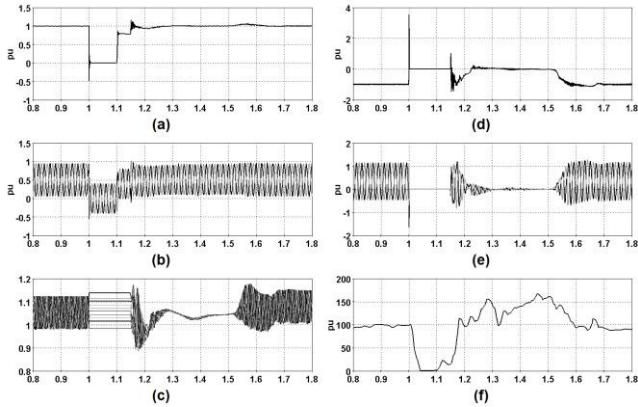

Figure 8: (a) DC voltage, (b) arm voltage, (c) total cell capacitor voltage, (d) DC current, (e) arm currents, (f) cell average switching frequency.

5.2 AAC

AAC fault current is higher than that of an MMC due to the discharge of the DC capacitor filter and the reduced combined inductance installed on the arms and the DC filter, as shown in Fig. 9(f). However, in the case where an inductive DC filter is used the DC fault current is expected to be significantly less [7]. The blocking command is issued to the chainlink, where the DS are ordered to remain open, as illustrated by the DS voltages in Fig. 9 (c). The reverse DC voltage across the chainlink is sufficient to block the DC link and therefore to block the fault. At t=0.55s the converter attempts to re-energise the DC link. At t=1s the DC voltage is settled to its nominal value, and at t=0.8s the power is ramping towards to its nominal value.
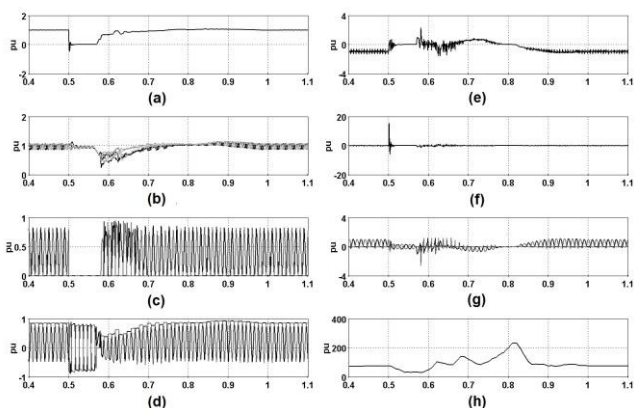

Figure 9: (a) DC voltage, (b) total cell capacitor voltage, (c) DS voltage, (d) chainlink voltage, (e) DC converter current, (f) DC filter current, (g) arm currents, (h) cell average switching frequency.

6 DC pole-to-ground fault

This section presents a simulation study for a DC positive pole-to-ground fault at the midpoint of the DC cables (70km from each converter). The fault ride through capabilities of MMC and AAC are considered. The objective is the survival of the transformer, whilst ensuring the converter stations current and voltage stresses are within tolerable limits.

6.1 MC-MMC

The moment that the pole-to-ground fault occurs, the voltage of the faulted pole collapses to zero as can been seen in Fig. 10(a). At the exact same instant the DC voltage reference is set to 0.5p.u. while a DC offset is deducted from the reference of the faulty arm. The total DC voltage then follows its reference and is set at half of the nominal value. This is illustrated by Fig. 10(b) where the healthy pole operates normally at the set modulation index, while the faulted pole is negatively over-modulated. The 50% FB cell MC-MMC is capable of supporting the specific over-modulation without the need of extra FB cells. Moreover it is evident from Figs. 10(e)-(h) that the CBA is able to distinguish between the HB and FB cell and operates accordingly. Also at that point the converter is able to extract limited active power, as illustrated by the converter AC currents in Fig. 10(d) at approximately t=1.45s and t=1.85s. Finally, the target of supporting the converter-side AC voltage is achieved and the DC offset is extinguished, as illustrated in Fig. 10(c). Although the DC current and voltage contain increased ripple and high-frequency components, the reduced magnitude should not affect either the insulation or the thermal limits of the cables.
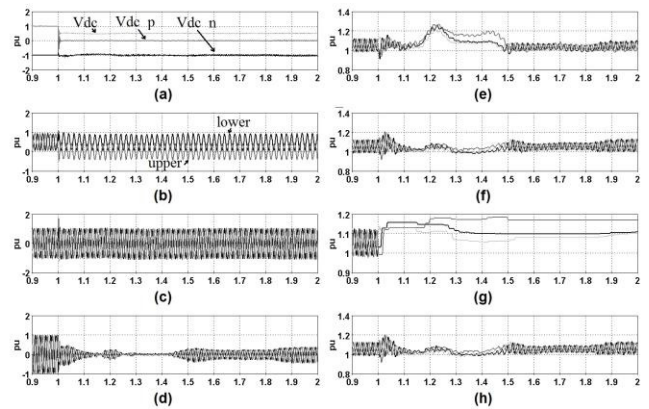

Figure 10: (a) DC voltages, (b) arm voltages, (c) converter AC voltage, (d) converter AC current, (e) upper FB total cell capacitor voltage, (f) lower FB total cell capacitor voltage, (g) upper HB total cell capacitor voltage, (h) lower HB total cell capacitor voltage.

6.2 AAC

During the pole-to-ground fault an over-modulated reference signal is applied and the AAC converter tries to support the converter AC voltage. However, the AAC is unable to achieve the 0.5p.u. voltage operation due to the stiff, non-complementary operation of the phase arms. Therefore when the voltage collapses at the faulty pole, the healthy pole has to sustain the full V_{dc}, as shown in Fig. 11(a), resulting in instantaneous collapse of the cable insulation. Additionally, in order to support the arm over-modulation, due to the internal

operation of the AAC, V_{chain} and V_{DS}, shown in Fig. 11(d) and Fig. 11(e) respectively, exceed the absolute nominal voltage. This is also illustrated by the increased capacitor voltages in Fig. 11(f). As a result the AAC is unable to achieve pole-to-ground FRT without damaging the internal voltage insulation.
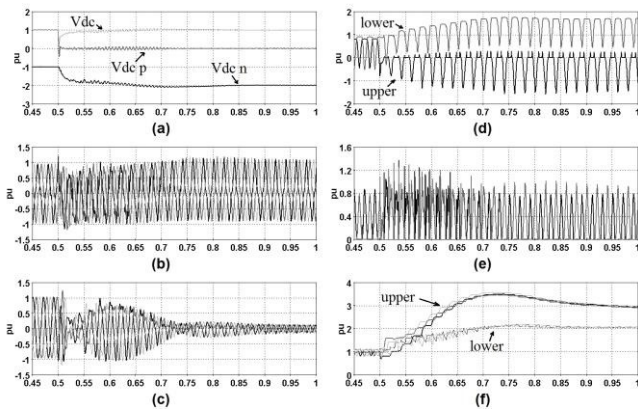

Figure 11: (a) DC voltages, (b) converter AC voltages, (c) converter AC current, (d) chainlink voltages, (e) DS voltages, (f) total cell capacitor voltage.

7 Conclusions

This paper presents a comparison between AAC and MC-MMC topologies during start-up, a phase-to-ground fault, a pole-to-pole fault, and a pole-to-ground fault. The study shows that:

- MC and AAC can achieve smooth charging sequences.
- Slowly increasing V_{dc} reference is preferred for avoiding increased switching of the converter during start-up.
- AAC and MC are capable of supporting AC currents during unbalance operation and are therefore able to stay connected as the Grid Code requires. However AAC experience internal unbalance which may have a destructive effect on cell insulation, whilst the DC voltage and current quality are unacceptable.
- MC and AAC exhibit good behaviour during DC pole-to-pole faults and during post-fault restart.
- MC achieve DC pole-to-ground fault ride through without damaging the insulation of the DC transformer, whilst maintaining some active power transfer. The AAC is unable to achieve such operation.

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