Nonvolatile memories using deep traps formed in HfO_2 by Nb ion implantation

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We report nonvolatile memories (NVMs) based on deep-energy trap levels formed in HfO_2 by metal ion implantation. A comparison of Nb- and Ta-implanted samples shows that suitable charge-trapping centers are formed in Nb-implanted samples, but not in Ta-implanted samples. This is consistent with density-functional theory calculations which predict that only Nb will form deep-energy levels in the bandgap of HfO_2. Photocurrent spectroscopy exhibits characteristics consistent with one of the trap levels predicted in these calculations. Nb-implanted samples showing memory windows in capacitance–voltage (V) curves always exhibit current (I) peaks in I–V curves, indicating that NVM effects result from deep traps in HfO_2. In contrast, Ta-implanted samples show dielectric breakdowns during the I–V sweeps between 5 and 11 V, consistent with the fact that no trap levels are present. For a sample implanted with a fluence of 10^{13} Nb cm^{-2}, the charge losses after 10^4 s are ~9.8 and ~25.5% at room temperature (RT) and 85°C, respectively, and the expected charge loss after 10 years is ~34% at RT, very promising for commercial NVMs. © *2011 American Institute of Physics*. [doi:10.1063/1.3554444]

I. INTRODUCTION

Over recent decades the demand for nonvolatile memory (NVM) devices has grown rapidly, especially for applications associated with portable electronics. Most of these devices are based on floating gate transistors whose characteristics are modified by charge stored on the floating gate. The use of discrete charge-traps prevents the catastrophic charge leakage that can occur in conventional poly-Si floating-gate memories due to local breakdown of the thin tunneling oxide and offers scaling advantages, including lower-voltage operation, faster program/erase (P/E) speeds, lower power consumption, and longer data retention. Nanocrystal (NC)-based charge-trap flash (CTF) memories are promising candidates for next-generation NVMs.[1–3] However, only a few NCs can be included in each memory cell as the devices are scaled to nanometer size, thereby limiting the number of electrons stored per bit and compromising device reliability, multibit operation, and charge retention.[4] Moreover, optimal performance requires that NCs have diameters of ~3 to 5 nm and are uniformly distributed with a density exceeding 10^{13} cm^{-2}, a technologically challenging requirement. Alternative strategies based on charge trapping at native defects have proven very successful for materials such as silicon nitrides[5] and have been studied in high-*k* dielectrics such as Y_2O_3, La_2O_3, and Tb_2O_3[6–9] as a means of scaling devices to smaller dimensions. However, the use of native defects is limited by the fact that they are uniformly distributed throughout the dielectric layer, and have a density that is process-dependent and difficult to control. We have previously proposed the ion-implantation of impurities as a means of forming deep traps in the bandgap of Al_2O_3 and have demonstrated the feasibility of this method for CTF NVMs.[10,11]

In this paper, we report charge trapping effects in Nb- and Ta-implanted HfO_2. The charge traps are characterized by photoconductivity (PC), capacitance-voltage (C–V), and current-voltage (I–V) measurements, and the results are compared with density functional theory (DFT) calculations.

II. EXPERIMENTAL

For the fabrication of metal–oxide–semiconductor (MOS) memory devices, a 5 nm SiO_2 layer was first grown on a p-type (100) Si wafer by conventional thermal oxidation. A 25 nm HfO_2 layer was then grown on top of the SiO_2 layer by atomic layer deposition. These $Si/SiO_2/HfO_2$ structures were implanted at room temperature (RT) with 60 keV Nb ions and 90 keV Ta ions to nominal fluences (n) in the range from 10^{12} cm^{-2} (from 10^{13} cm^{-2} for Ta ions) to 10^{15} cm^{-2}. The ion-range and damage distributions, calculated using the SRIM code,[12] are shown in Fig. 1(a) and 1(b), respectively. The samples were subsequently annealed in a rapid thermal annealing apparatus at a temperature of 600°C for 5 min under a nitrogen ambient.

PC spectra were measured by using a coplanar, two-probe geometry with Al electrodes of 4 mm length and 2 mm separation to characterize the energy levels of traps in the bandgap. The PC spectra were measured at 80 K in a LN_2 refrigerator using a xenon lamp as the light source and under a bias of 1 V, which is within the linear range of I–V characteristics. The power density of the incident light on the sample surface was in the range of 20 ~ 290 mW/cm^2

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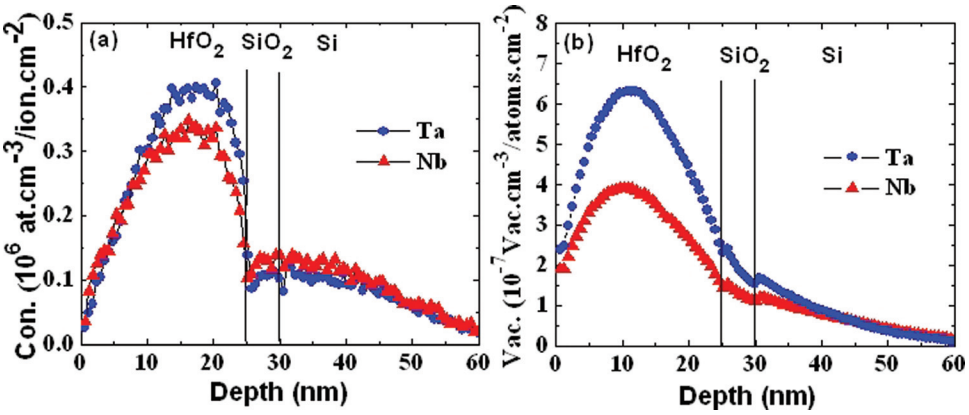

FIG. 1. (Color online) (a) Ion range distributions calculated with the SRIM2010 code for Nb- and Ta-implanted Si/SiO_2/HfO_2 structures. (b) Total vacancy concentration as a function of depth for Ta and Nb implants.

depending on the photon energy, and spectra were corrected for such variations over the measurement range of $2 \sim 5$ eV. Al electrodes with a diameter of 200 μm were deposited on the samples in a vacuum for I–V and C–V measurements of MOS capacitors. I–V and high-frequency C–V measurements were performed using an Agilent 4156C precision semiconductor parameter analyzer and Agilent 4284A precision LCR meter with a frequency of 1 MHz.

III. RESULTS AND DISCUSSION

Figure 2(a) compares PC spectra for MOS cells fabricated with unimplanted HfO_2, and with Nb- and Ta-implanted HfO_2. The spectrum from the cell with unimplanted HfO_2 shows a monotonic increase in photocurrent with increasing photon energy and no obvious emission peaks. A similar response is observed from the Ta-implanted sample. In contrast, the cell implanted with Nb ions (1×10^{13} cm^{-2}) shows a broad peak centered at around 3.2 eV. This suggests that Nb implantation produces defects with energy levels ~3.2 eV below the conduction band minimum (CBM) of HfO_2.

Periodic spin-unrestricted DFT calculations using the B3LYP functional[13] were performed to predict the energies of the defect levels introduced by Nb and Ta impurities in monoclinic HfO_2. The predicted bandgap for the bulk (unimplanted) HfO_2 lattice using B3LYP was 6.15 eV, which is in excellent agreement with experimental results.[14] Calculations for Nb predicted defect states at energies of 1.12 and 3.29 eV below CBM, both of which are unoccupied, as shown in Fig. 2(b), while similar calculations for Ta predicted no defect states in the energy gap of HfO_2. The PC peak shown in Fig. 2(a) for Nb-implanted HfO_2, located at around 3.2 eV, is consistent with the calculated defect level at 3.29 eV.

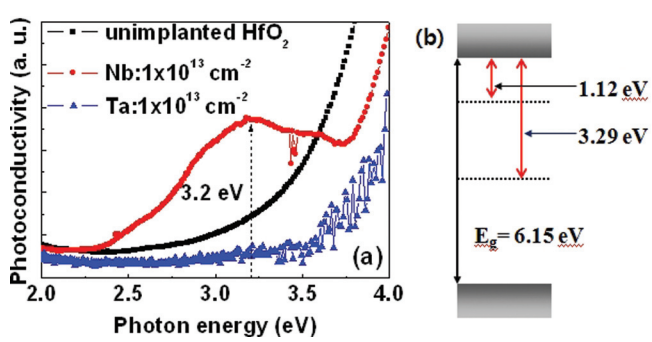

FIG. 2. (Color online) (a) Photoconductivity spectra of memory cells with unimplanted HfO_2, and with Nb- and Ta-implanted HfO_2. The implantation was done with Nb or Ta ions of 10^{13} cm^{-2} fluence. (b) Schematic diagram showing the calculated trap energy levels for Nb-implanted HfO_2.

Figure 3(a) shows C–V hysteresis loops for a cell implanted with Nb (10^{13} cm^{-2}) for various sweep voltages. All C–V curves show counter-clockwise hysteresis loops, indicating electron injection from the Si substrate to the charge-trapping layer containing Nb ions. As shown in Fig. 3(b), the memory window (ΔV) increases from ~3.6 to ~4.95 V with increasing implant fluence (over the range from 10^{12} to 10^{13} $Nb.cm^{-2}$) under a sweep voltage of ± 15 V, consistent with an increase in the density of charge-trapping states. In contrast, cells implanted to fluences $\geq 10^{14}$ cm^{-2} showed almost no hysteresis (zero memory window), even though they exhibited well-defined C–V curves. From ion-range and damage simulations in Fig. 1, it is clear that the implantation creates defects throughout the dielectric film and into the Si substrate. The resulting electrical response will reflect contributions from doping and defects, with partial annealing of the defects expected during the 600°C anneal. The defect contribution is expected to increase with increasing ion fluence, which explains why no memory window is observed for fluences $\geq 10^{14}$ cm^{-2}.

The cell with unimplanted HfO_2 showed no significant memory window for sweep voltages in the range from ± 9 to ± 15 V. This demonstrates that memory effects are attributed to the charge traps produced by the Nb ion implantation, not by natural defects in HfO_2 or the HfO_2/SiO_2 interface states. Samples implanted with Ta did not exhibit well-defined C–V curves.

The amount of charge stored in the traps can be estimated from the relation $Q = C\Delta V$, where C is the capacitance density and ΔV is the memory window.[15] In this work, C and ΔV are about 1.81×10^{-7} Fcm^{-2} (capacitance = 57 pF, contact area = $\pi \times 100 \times 100$ μm^2) and 4.95 V, respectively, for a cell with Nb ions of 10^{13} cm^{-2} fluence. Thus, the electron density stored in the traps is estimated to be 5.56×10^{12} cm^{-2}, which is comparable to the trap density of silicon-oxide-nitride-oxide-silicon.[16]

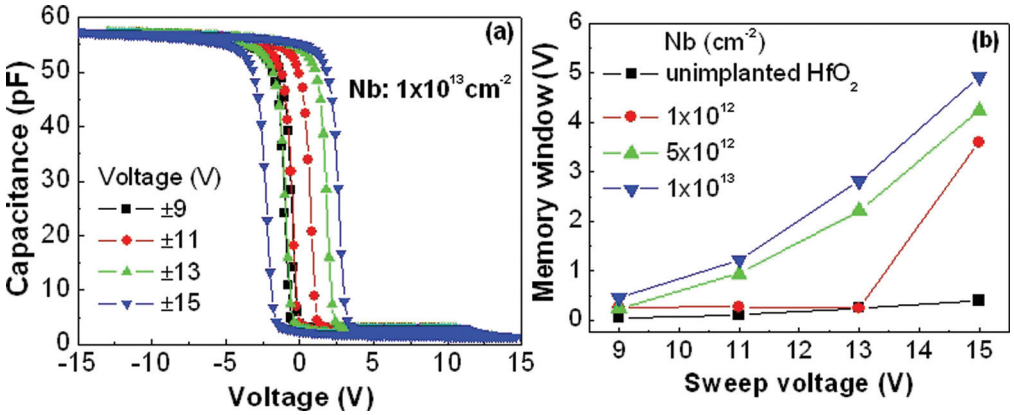

FIG. 3. (Color online) (a) C–V hysteresis loops of MOS cells fabricated with Nb implantation to a fluence of 10^{13} Nb cm^{-2}. (b) Memory window as a function of sweep voltage for various Nb fluences.

Figure 4(a) shows I–V characteristics of MOS cells with various Nb fluences under a sweep voltage of ± 13 V. The I–V curves show clockwise hysteresis loops while the bias is swept from 0 to positive and back into negative voltages. The cell with Nb ions of 10^{12} cm^{-2} fluence shows clear current peaks both in forward and backward scans. The positive and negative current peaks are known to result from the charging/discharging of electrons into/from charge traps, respectively.[17,18] In contrast, the I–V curves show much broader current peaks at $n_{Nb} = 10^{13}$ cm^{-2} and no peaks at $n_{Nb} = 10^{14}$ cm^{-2} in both scans. For $n_{Nb} = 10^{14}$ cm^{-2}, no peaks were found even for various sweep voltages of ± 7 to ± 13 V, consistent with the fact that no memory window in the C–V hysteresis is observed at $n_{Nb} \geq 10^{14}$ cm^{-2}. These results suggest that there is an optimum fluence range for achieving devices by this means. The unimplanted sample shows a very small current peak in the forward scan and a significant current peak in the backward scan. The current peaks in this case are attributed to interface defect states because no memory window is found in the C–V scans, as explained in Si-NC NVMs.[18]

Figure 4(b) shows the I–V characteristics of MOS cells with Ta-implanted HfO_2. Cells implanted with different Ta fluences show dielectric breakdowns during the I–V sweeps between 5 and 11 V. Clearly, Ta implantation produces leakage paths through the HfO_2 matrix, possibly in the form of shallow defect levels. Significantly, the Ta does not appear to play a role in forming charge traps in the bandgap of HfO_2, consistent with calculations and the measured C–V results. As shown in Fig. 1, simulation of the Ta and Nb implants shows that the ion-range and damage distributions extend beyond the dielectric layers and into the Si substrate and that the ion and damage distributions exhibit important differences. The Ta concentration is higher in the dielectric films and lower in the Si substrate than for Nb, while the damage distribution produced by Ta is higher in both the dielectric films and the Si substrate. The defect density for Ta is 30% higher at the SiO_2/Si interface and 60% higher at the HfO_2/SiO_2 interface, which likely accounts for the higher leakage current observed in Ta-implanted samples.

Figure 5 shows retention characteristics of a Nb-implanted cell ($n_{Nb} = 10^{13}$ cm^{-2}) measured at RT and 85°C. The programming and erasing states are defined as those programmed by a pulse of (+13 V, 1 s) and erased by a pulse of (−13 V, 1 s), respectively. The flat-band voltage at the programmed/erased states of the cell remains almost unchanged with time, showing very little charge loss during the retention measurements. The charge losses after 10^4 s are ~9.8% and ~25.5% at RT and 85°C, respectively, and the expected charge loss after 10 years is ~34% at RT, very promising for commercial NVMs.

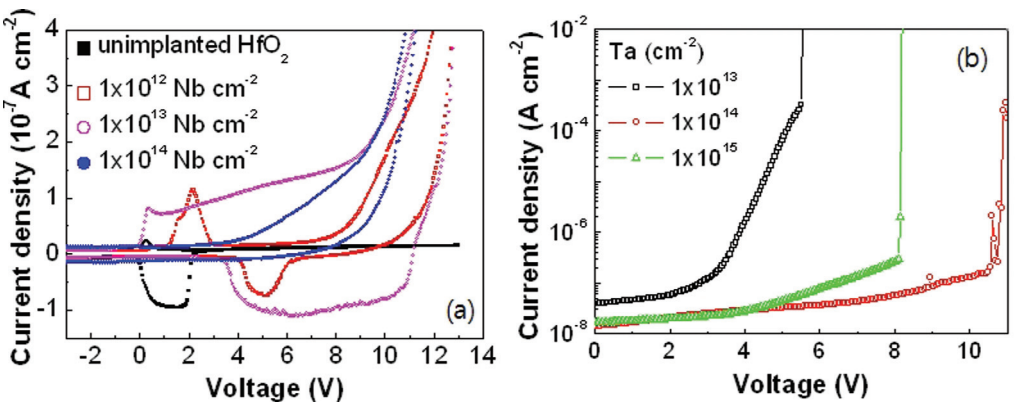

FIG. 4. (Color online) I–V characteristics of MOS cells with (a) Nb- and (b) Ta-implanted HfO_2 for various fluences.

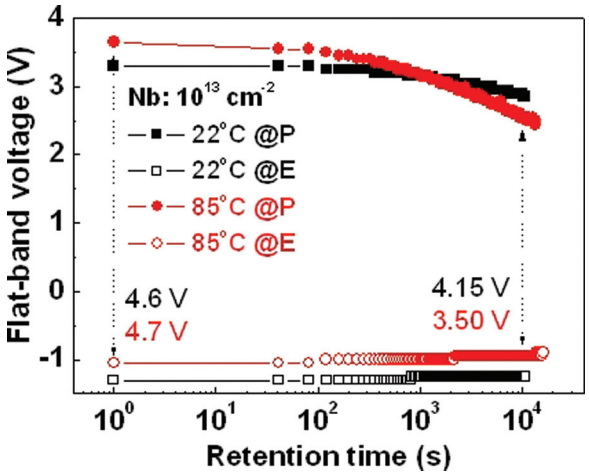

FIG. 5. (Color online) Retention characteristics of programming (P)/erasing (E) states at RT and 85°C for MOS cells fabricated with Nb implantation to a fluence of 10^{13} Nb cm^{-2}.

IV. CONCLUSION

NVM MOS cells were fabricated using deep-energy trap levels formed in HfO_2 by metal ion implantation. Photocurrent spectroscopy exhibited characteristics consistent with one of the trap levels in the bandgap of Nb-implanted HfO_2 predicted by calculations. The MOS cells with Nb-implanted HfO_2 showed NVM effects in C–V curves for n_{Nb} from 10^{12} to 10^{13} cm^{-2} but no such effects for $n_{Nb} \geq 10^{14}$ cm^{-2}, further confirmed by the existence of current peaks in I–V curves. In contrast, MOS cells with Ta-implanted HfO_2 showed no well-defined response during the C–V sweeps and only dielectric breakdowns during I–V sweeps, indicating no NVM effects, consistent with the calculations. The MOS cell fabricated with Nb implantation to a fluence of 10^{13} Nb cm^{-2} showed charge losses of ~9.8 and ~25.5% at RT and 85°C, respectively, after 10^4 s and the expected charge loss after 10 years was ~34% at RT, very promising for commercial NVMs.

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