

Unipolar and bipolar operation of InAs/InSb nanowire heterostructure field-effect transistors

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We present temperature dependent electrical measurements on n-type InAs/InSb nanowire heterostructure field-effect transistors. The barrier height of the heterostructure junction is determined to be 220 meV, indicating a broken bandgap alignment. A clear asymmetry is observed when applying a bias to either the InAs or the InSb side of the junction. Impact ionization and band-to-band tunneling is more pronounced when the large voltage drop occurs in the narrow bandgap InSb segment. For small negative gate-voltages, the InSb segment can be tuned toward p-type conduction, which induces a strong band-to-band tunneling across the heterostructure junction. © 2011 American Institute of Physics. [doi:10.1063/1.3633742]

I. INTRODUCTION

The InAs-InSb-GaSb material system has several interesting properties, such as very narrow bandgaps, small effective masses, and very high mobilities at low fields. Furthermore, exotic heterostructures can be formed, including the type III broken bandgap alignment. While the broken bandgap of InAs-GaSb has been previously studied,¹⁻³ there are very few reports on the InAs-InSb heterostructure, mainly due to growth difficulties related to the large lattice mismatch between InSb and InAs.⁴

In this paper, we discuss the electrical properties of InAs/InSb heterostructure field-effect transistors (HFETs) fabricated by nanowire technology. The nanowire technology enables the growth of non-lattice matched devices, such as InSb on InAs.^{5,6} We use a lateral transistor configuration with transistors formed to the InAs/InSb segments. We consider the InAs/InSb field-effect transistor (FET) and discuss the main transport mechanisms, and the data are compared to n-type InAs and n-type InSb FETs.⁷ We demonstrate unipolar n-type operation of the HFET and determine the height of the heterostructure junction. Furthermore, we show that the HFET may operate as a bipolar device based on hole transport in the InSb, with the possibility to observe band-to-band tunneling across the broken bandgap heterointerface.

II. DEVICE FABRICATION

The InAs/InSb heterostructure nanowires studied here are grown in a standard metalorganic vapor phase epitaxy reactor at a pressure of 10 kPa, using 40 nm-diameter aerosol gold particles, deposited onto an InAs(111)B substrate as initial seeds. The nanowires are grown using trimethylindium, arsine, and trimethylantimony as source materials. The InSb is found to be a perfect zinc blende with an increased diame-

ter with respect to the wurzite InAs stem. We observed a sharp transition at the interface, covered by limited overgrowth around the neck (10 nm-long InAs zinc blende) with about a 10 nm-long strain distribution developing on either side of the heterostructure. More information on the growth of InAs/InSb nanowires and the detailed characterization of the heterointerface are presented elsewhere.^{6,8}

In order to investigate the electrical properties of the InAs/InSb heterostructure, the nanowires are transferred from the growth substrate to degenerately-doped Si substrates with a 100 nm-thick SiO₂ capping layer. Two sets of samples are then fabricated, with and without top gates. For the back-gated sample, two pairs of 200 nm-wide Ti/Au contacts with a spacing of 160 nm are defined to each segment in the nanowire by electron beam lithography such that one pair is placed on each side of the heterostructure interface. To obtain high quality metal-nanowire interfaces, the exposed semiconductor contact areas are briefly etched in a (NH₄)₂S_x solution followed by a rinse in H₂O prior to metal evaporation. To increase the gate coupling, we further fabricate top-gated devices. Here, 140-nm-wide Ti/Au contacts with a spacing of 250 nm are placed on each side of the heterostructure interface. A 10-nm-thick Al₂O₃ dielectric is deposited using atomic layer deposition (ALD) at a temperature of 100 °C,⁹ in a 3 × 3 μm² square on each wire, also covering the metal contacts. Finally, 140 nm-wide Ti/Au finger gates are defined between the ohmic contacts, such that the gate-contact spacing is approximately 55 nm on each side of the gate finger. In order to remove the influence of the gate-voltage on the ohmic contacts, the gates are defined without overlap to the source and drain contacts.

III. ELECTRICAL CHARACTERIZATION

First, the *I-V*-characteristics of the InAs/InSb heterostructure were evaluated, at the silicon back-gate voltage, $V_{bg} = 0$ V, as a function of temperature, in the range of $T = 250$ to 170 K; see Fig. 1(b). Figure 1(a) displays a SEM image of a typical device. Here, we observe highly

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asymmetric curves, with a low-bias resistance ranging from 200 k Ω to 400 M Ω . Due to the low resistance and the symmetric I - V characteristics of the homogeneous InAs and InSb reference samples (13 and 21 k Ω , respectively), we can confirm a good quality of the metal/semiconductor contacts and thereby attribute the features in Fig. 1(b) to the intrinsic behavior of the InAs/InSb heterostructure.

At each drain-source voltage, V_{ds} , the activation energy, E_{act} , is derived in Arrhenius plots; see Fig. 1(c). Here, we find a maximum value of $E_{act} = 220$ meV, at $V_{ds} = 80$ mV applied to the InSb part of the heterostructure. The typical quality of the E_{act} fit is displayed as an inset in Fig. 1(c), for $V_{ds} = 150$ mV. The measured E_{act} is slightly larger than the bandgap of InSb ($E_g = 174$ meV at room temperature, using band-parameters from (Ref. 10)), which indicates a broken band alignment at the InAs/InSb heterostructure. At thermal equilibrium, we expect E_{act} to be equal to the sum of the bandgap of InSb and the energy of the InSb valence bandedge relative

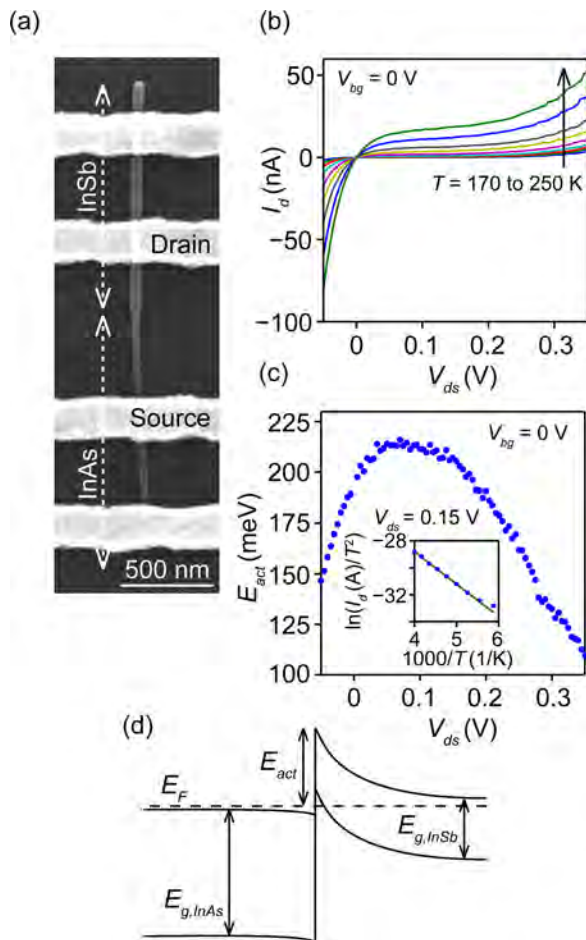


FIG. 1. (Color online) (a) A scanning electron-beam microscope (SEM) image of a typical InAs/InSb nanowire heterostructure field-effect transistor. The InAs/InSb nanowires are transferred to degenerately doped Si substrates, capped by 100 nm-thick SiO_x. Two Ti/Au contacts are fabricated to each segment, InAs and InSb, respectively, by electron beam lithography and lift-off. (b) Drain current, I_d , as a function of source-drain voltage, V_{ds} , measured across the heterostructure with the drain on the InSb segment, at different temperatures, $T = 170$ to 250 K in steps of 10 K, and a back-gate voltage, $V_{bg} = 0$ V. (c) Activation energy, E_{act} , as a function source-drain bias, V_{ds} , as deduced from (b). The inset displays the typical quality of the linear fit, shown here at $V_{ds} = 0.15$ V. (d) Schematic illustration of the band diagram of the InAs/InSb heterostructure, indicating E_{act} .

to the Fermi level, as illustrated in Fig. 1(d). This value is substantially smaller than a recently calculated value for a zinc blende InAs/InSb nanowire heterostructure, $\Delta E_C \approx 900$ meV,¹¹ whereas it agrees well with the predicted values based on band alignment arguments.¹² Although we note that these references do not take into account the wurtzite structure of the InAs segment, which might affect the InAs/InSb band-offset. We believe that this is the first experimental determination of the strained band-offset between InAs and InSb.

The output characteristics (I - V) of the top gated InAs/InSb HFET is next investigated at room temperature (RT), injecting electrons from either the InSb or InAs segment, as shown in Figs. 2(b) and 2(c), respectively. Figure 2(a) displays a SEM image of a typical top gated device. First we note that the InAs/InSb transistor shows mainly n-type behavior, in a way similar to both the InAs and InSb FETs.⁷

When the transistor is operated with the drain on InSb (Fig. 2(c)) an increase in output conductance appears at $V_{ds} > 0.4$ V. In this configuration, the large drain voltage drop occurs in the InSb segment, where the narrow bandgap of InSb combined with a high drain field can lead to electron-hole pair generation due to impact ionization and band-to-band tunneling. This behavior is not present when the device is operated with InAs as the drain due to the larger

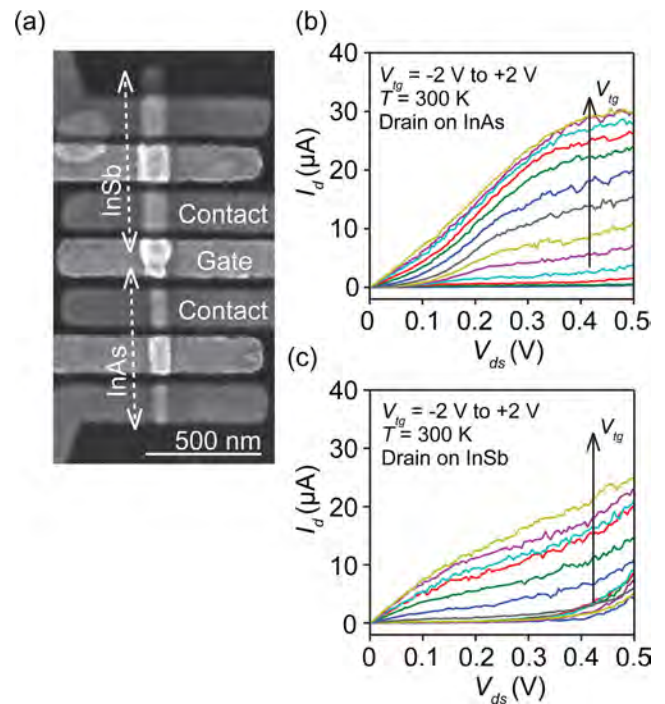


FIG. 2. (Color online) (a) A scanning electron-beam microscope (SEM) image of a typical top-gated InAs/InSb nanowire heterostructure field-effect transistor. The InAs/InSb nanowires are transferred to degenerately doped Si substrates, capped by 100 nm-thick SiO_x. First, two Ti/Au contacts are fabricated to each segment, InAs and InSb respectively, by electron beam lithography (EBL) and lift-off. Then, a 10 nm-thick layer of HfO₂ is deposited using atomic layer deposition (ALD). Finally, three Ti/Au top-gates are fabricated, by EBL and lift-off, from which one is placed directly on top of the InAs/InSb heterostructure. (b) and (c) I - V characteristics of the InAs/InSb heterostructure at room temperature. Drain current, I_d , as a function of source-drain voltage, V_{ds} , measured across the heterostructure junction with the drain on the InSb segment and InAs segment, respectively, at different top-gate voltages, $V_{tg} = -2$ to 2 V in steps of 1/3 V.

bandgap of InAs ($E_g = 350$ meV at room temperature, using band-parameters from Ref. 10; see Fig. 2(b)).

From the transfer characteristics (not shown) we deduce the threshold voltage, V_T , for the two bias configurations at $V_{ds} = 300$ mV and $V_{ds} = 50$ mV. Interestingly, while both configurations display approximately the same positive $V_T \sim 1$ V at $V_{ds} = 50$ mV, the configuration when electrons are injected from the InSb shows a strong decrease in V_T with increasing V_{ds} . Here, V_T is reduced down to ~ 0 V for $V_{ds} = 300$ mV. The origin of this asymmetric V_T with respect to drain configuration could be related to the details of the band bending at the heterojunction, with a positive barrier ($E_{c,InSb} - E_{c,InAs}$) remaining in the conduction band as the transistor is biased to inject electrons from the InAs, while this barrier is reduced due to band bending as we inject electrons from the InSb segment.

The full temperature dependence of the transfer characteristics in the temperature range of 4 to 300 K is displayed in Figs. 3(a) and 3(b), where a striking difference between the two bias configurations is revealed. As we inject electrons from InSb (Fig. 3(a)) a constant decrease in current with decreasing V_{tg} is observed, as is the usual case for FETs. In contrast, as we inject electrons from the InAs, i.e., with the drain bias applied to the InSb, we not only observe the usual current reduction as we reverse the gate bias around

room temperature, but also an increasing current around $V_{tg} \sim 0$ V appears. We attribute the latter to transport between the InAs conduction band and the InSb valence band. At positive gate biases, 0.5 V $< V_{tg} < 2$ V, both the InSb and InAs wire segments are n-type, and the current is dominated by majority (electron) injection above the conduction band barrier. As V_{tg} is made more negative, $-0.5 < V_{tg} < 0.5$ V, the InSb transport is dominated by holes,⁷ while the InAs still shows n-type behavior. This opens up a second transport channel besides the electron transport in the conduction band, and leads to an increase in the current with decreasing V_{tg} . As V_{tg} is made more negative, $V_{tg} < -0.5$ V, the InAs wire segment is depleted from electrons, which makes the transport across the band structure unfeasible. This leads to a reduction in the current. Interestingly, this observed effect is much stronger as we apply the drain bias to the InSb segment. The origin may be related to the narrower bandgap of InSb with possibilities for band-to-band tunneling at the drain side of InSb and hole injection from the ohmic contact, with both processes contributing to hole injection. The current transport across the heterojunction may have contributions from direct tunneling as along with defect assisted tunneling and recombination via defect sites. In particular, the influence of the high-k with its interface states may contribute to the current. However, our data shows a very weak temperature dependence at low temperatures. This is an indication that the transport mechanism is, in fact, dominated by direct tunneling in this low temperature range.

At each V_{tg} the activation energy, E_{act} , is derived in Arrhenius plots. The result is displayed in Figs. 3(c) and 3(d). The typical quality of the E_{act} fit is displayed for each figure; here for $V_{ds} = 300$ mV and $V_{tg} = 0$ V. For simplicity, we do not apply any T -dependent prefactor in the evaluation, since the different mechanisms observed have a slightly different temperature dependence. In the InSb drain configuration, shown in Fig. 4(d), a broad dip is present at $V_{tg} \approx -0.3$ V, in particular, at the high drain bias condition where we more effectively inject holes from the drain. The minimum value in the dip is about 60 meV, which is well below the bandgap of InSb. We attribute this value, and its voltage dependent shape, to the competition between the thermionic emission above the barriers and the transport across the broken gap heterojunction (as discussed earlier).

IV. CONCLUSION

In summary, we have investigated the temperature dependent properties of n-type InAs/InSb nanowire heterostructure FETs, and demonstrated unipolar as well as bipolar transport through the junction. The barrier height of the InAs/InSb heterojunction is determined to be 220 meV, which indicates a broken bandgap alignment. We have also examined the asymmetry of the heterojunction FET, when applying bias to either the InAs or the InSb side of the structure. Here, we find an increasing impact ionization and band-to-band tunneling when the bias is applied to the InSb, consistent with the effect of a large electric field in a narrow bandgap material. As the gate voltage is tuned toward

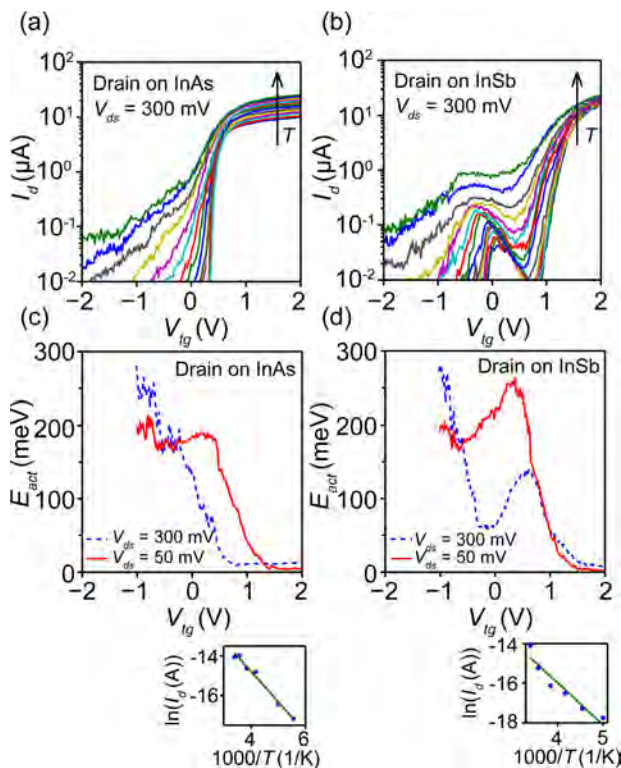


FIG. 3. (Color online) (a) and (b) Transfer characteristics as a function of temperature. Drain current, I_d , as a function of top-gate voltage, V_{tg} , measured across the heterostructure junction with the drain on the InAs segment and the InSb segment respectively, at temperatures, $T = 300$ to 4.2 K, and a source-drain voltage, $V_{ds} = 300$ mV. (c) and (d) Activation energy, E_{act} , as a function of V_{tg} , for $V_{ds} = 300$ mV (blue dashed line) and $V_{ds} = 50$ mV (red solid line), measured across the heterostructure junction with the drain on the InAs segment and the InSb segment, respectively. The typical quality of the E_{act} fit is displayed below each figure, shown here for $V_{ds} = 300$ mV and $V_{tg} = 0$ V.

slightly negative values, and the InSb segment turned toward inversion, we observe a strongly increased conductivity due to transport across the heterostructure junction.

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¹H. Sakaki, L. L. Chang, R. Ludeke, C.-A. Chang, G. A. Sai-Halasz, and L. Esaki, *Appl. Phys. Lett.* **31**, 211 (1977).

²P. Fay, J. Lu, Y. Xu, G. H. Bernstein, D. H. Chow, and J. N. Schulman, *IEEE Trans. Electron Devices* **49**, 19 (2002).

³M. B. Borg, K. A. Dick, B. Ganjipour, M.-E. Pistol, L.-E. Wernersson, and C. Thelander, *Nano Lett.* **10**, 4080 (2010).

⁴S. Yamaguchi and M. Matsumoto, *Vacuum* **84**, 1323 (2010).

⁵D. Ercolani, F. Rossi, A. Li, S. Roddaro, V. Grillo, G. Salviati, F. Beltram, and L. Sorba, *Nanotechnology* **20**, 505605 (2009).

⁶P. Caroff, J. B. Wagener, K. A. Dick, M. Jeppsson, K. Deppert, L. Samuelson, L. R. Wallenberg, and L.-E. Wernersson, *Small* **4**, 878 (2008).

⁷H. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlström, and L.-E. Wernersson, *Appl. Phys. Lett.* **96**, 153505 (2010).

⁸P. Caroff, M. E. Messing, M. B. Borg, K. A. Dick, K. Deppert, and L.-E. Wernersson, *Nanotechnology* **20**, 495606 (2009).

⁹D. Wheeler, L.-E. Wernersson, L. Froberg, C. Thelander, A. Mikkelsen, K.-J. Weststrate, A. Sonnet, E. M. Vogel, and A. Seabaugh, *Microelectron. Eng.* **86**, 1561 (2009).

¹⁰I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, *J. Appl. Phys.* **89**, 5815 (2001).

¹¹M.-E. Pistol and C. E. Pryor, *Phys. Rev. B* **80**, 035316 (2009).

¹²S. Tiwari and D. J. Frank, *Appl. Phys. Lett.* **60**, 630 (1992).