Analysis and Mitigation of Dead Time Harmonics in the Single-Phase Full-Bridge PWM Converter with Repetitive Controllers

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***Abstract*—In order to prevent the power switching devices (e.g., the Insulated-Gate-Bipolar-Transistor, IGBT) from shoot-through in voltage source converters during a switching period, the dead time is added either in the hardware driver circuits of the IGBTs or implemented in software in Pulse-Width Modulation (PWM) schemes. Both solutions will contribute to a degradation of the injected current quality. As a consequence, the harmonics induced by the dead time (referred to as "dead time harmonics" hereafter) have to be compensated in order to achieve a satisfactory current quality as required by standards. In this paper, the emission mechanism of dead time harmonics in single-phase PWM inverters is thus presented considering the modulation schemes in details. More importantly, a repetitive controller has been adopted to eliminate the dead time effect in single-phase grid-connected PWM converters. The repetitive controller has been plugged into a proportional resonant-based fundamental current controller so as to mitigate the dead time harmonics and also maintain the control of the fundamental-frequency grid current in terms of dynamics. Simulations and experiments are provided, which confirm that the repetitive controller can effectively compensate the dead time harmonics and other low-order distortions, and also it is a simple method without hardware modifications.**

***Index Terms*—Harmonics, dead time, repetitive control, resonant control, PWM converters, modulation, insulated-gate-bipolar-transistor (IGBT)**

I. Introduction

POWER electronic converters have brought an increasing power quality challenge to the grid-connected renewable energy systems like PhotoVoltaic (PV) and wind turbine systems [1], [2], due to a) the intermittent nature of renewable energies [3] that leads to a fluctuating power injection and b) the widely adopted Pulse-Width Modulation (PWM) control of power converters [3], [4]. In order to alleviate the harmonic injections from the grid-connected PWM converters, many advanced current controllers have been developed, such as the Proportional Resonant (PR) controller [5]–[11]. With those controllers, the current quality can be improved to a large extent in terms of a lower Total Harmonic Distortion (THD) level. Using higher-order passive filters (e.g., an *LCL* filter) [12] is an alternative, which contributes to a further enhancement of the power quality, yet leading to more power losses, increased control complexity (e.g., requiring an additional damping control), higher cost, and more sophisticated design [13], [14]. Increasing the switching frequency will result in one possibility to use smaller output filters and thus lower the entire cost, but the nonlinearity including dead time effects will possibly be magnified and thus the current quality may become even poorer [15].

In practice, the dead time has to be implemented in the PWM drivers to prevent the inverter from shoot-through during a switching interval [16]–[26]. The dead time should be considered in the design phase of the inverter system and possible solutions to the minimization of dead time duration were also discussed in the literature [27]. Nonetheless, the inserted dead time potentially introduces harmonic distortions in the PWM converter output voltages [17]–[19], which then propagate to the output currents. For example, it can contribute to a decrease of the fundamental-frequency component of the converter output voltages, and also it will generate low order harmonics in the output PWM voltage of the converter [20]. Both issues can lead to distortions of the injected current [4] as well as additional losses, and this situation may become even worse with an increase of the switching frequency as mentioned above [22]. In addition, harmonics in the injected current can be magnified in the case that the grid voltage is distorted (i.e., background distortions) since the current control is normally achieved in a closed-loop system without feed-forward. Thus, the dead time has to be compensated in such applications and harmonic compensators incorporated in the current controller are also preferred.

Most dead time compensation methods are based on an average value theory [16], [19], [20], [22]. In those techniques, voltage changes because of the dead time are averaged over an entire period, and the resultant value is subsequently included in the inverter voltage reference to compensate the dead time effect. However, those methods rely on the detection of the current polarity, leading to an increase of the overall complexity and also a decrease of noise immunity at zero-

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crossing points of the current. Moreover, such methods can not correctly estimate the voltage changes around zero current points as discussed in [22]. Additionally, with different modulation schemes, the dead time harmonics may vary [28]. With those concerns, other solutions were reported in the literature [20], [22], [29]–[31] by compensating the harmonics in the controllers. For instance, in [20], a compensation method using the controller integrator output has been introduced, and in [22], an adaptive dead time compensator has been developed, which calculates the feed-forward compensation duty cycle. Since the dead time mainly introduces low order harmonics [20], it is possible to mitigate these harmonics simply by using multiple parallel ReSonant Controllers (RSCs). This technique can effectively compensate the low order harmonics, but may also trigger the system resonance when higher order harmonics (e.g. 11^{th}- and/or 13^{th}-order harmonics) are compensated in order to fully mitigate the dead time effect. Especially, in the *LCL*-filtered PWM converters, the resonant frequency of the filter can be low enough to a few kilo Hz (close to the dominant low-order harmonic frequency), and it is varying with the grid stiffness. This requires more attempts to the design of RSCs in terms of phase compensation to avoid resonances. In contrast, a Repetitive Controller (RC) based on the internal model principle [9], [32] can suppress all the harmonics (including the harmonics induced by the dead time) with a negligible concern of resonance if it is designed properly, which thus may be a promising solution for the harmonic compensation.

As an extension of [26] and [28], this paper thus focuses on the analysis of the mechanism of dead time harmonics in § III after a brief introduction of the control of single-phase grid-connected inverters, where an RC-based mitigation strategy is presented. The analysis also considers the impact of modulation schemes. The RC-based solution for the dead time compensation does not require additional hardware modifications as well as complicated mathematical derivations (e.g., in terms of phase compensation). When it is implemented in a digital controller, the RC is simply plugged in parallel with a PR fundamental-frequency controller as the harmonic compensator. In order to verify the effectiveness of the RC-based dead time harmonic mitigation, simulations and experiments have been performed on a 2-kW single-phase grid-connected inverter system, and the results are provided in § IV. In addition, comparisons between the RC-based mitigation method and the RSC-based dead time compensation solution in the case of grid voltage background distortions are also carried out before the conclusion.

II. Control of Single-Phase Inverters

Fig. 1(a) shows a single-phase grid-connected PWM inverter system with an *LCL* filter, which is a typical configuration for single-phase residential PV systems of lower power ratings (e.g., 1 kWp $\sim$ 3 kWp). For such a grid-connected PWM converter, it is commonly required to operate at unity power factor or to maintain a minimum power factor of 0.85 [3], [4], [33], [34]. Consequently, in respect to the control of the grid-connected PWM converters, it consists of two cascaded

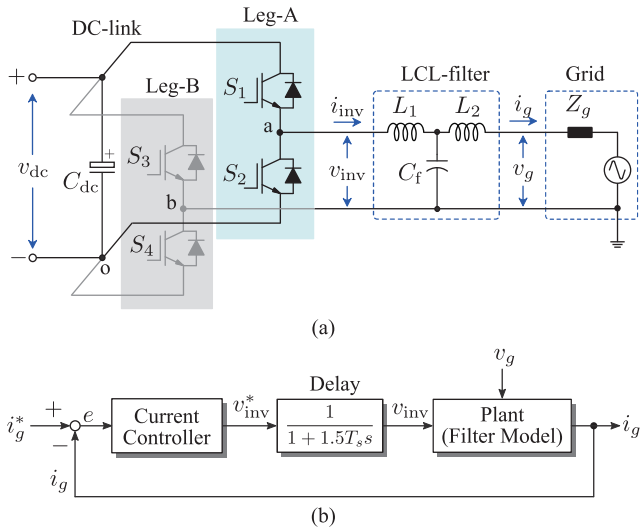

Fig. 1. A single-phase grid-connected transformerless PWM inverter system with an *LCL* filter (L_1-C_f-L_2): (a) schematics of the hardware, where v_{dc} is the DC-link voltage across the capacitor and Z_g is the grid impedance, and (b) the closed-loop current control system, where T_s is the sampling period.

loops — the outer voltage/power control loop for a reference current generation and the inner current control loop taking the responsibility to shape the injected grid current (i.e., the power quality issue). In the following, only the current controller is considered, as it is shown in Fig. 1(b).

Moreover, the grid current i_g has to be synchronized with the grid voltage v_g by means of a Phase Locked Loop (PLL) system [33]. In terms of controlling the AC grid current, the PLL system also enables the use of a Proportional Integral (PI) controller in the $dq-$synchronous rotating reference frame [5], [7], [33]. However, it requires at least two reference frame transformations (i.e., $dq \rightarrow \alpha\beta$ and/or $\alpha\beta \rightarrow dq$), which leads to an increase of complexity and controller design difficulties. An alternative is to directly implement the current control in the $\alpha\beta-$stationary reference frame, as shown in Fig. 1(b), where periodic controllers (e.g., a PR controller or an RC scheme) are able to achieve a lower tracking error [5], [8], [11], [33]. It is clear that the grid current i_g is the main control variable in order to ensure an appropriate power injection with a satisfactory power quality, whereas it is also the "victim" of the dead time harmonics, which will be detailed in the following. Notably, harmonic compensators can be implemented in parallel with the fundamental-frequency current controller to mitigate the distortions induced by the dead time and also the background distortions.

III. Repetitive Controller for Dead Time Harmonic Compensation

A. Mechanism of Dead Time Harmonics

The effect of the dead time t_d on the inverter output voltages (i.e., v_{ao}, v_{bo}, and $v_{inv} = v_{ao} - v_{bo}$) is demonstrated in Fig. 2, where the power switching device (IGBT) turn-on (t_{on}) and turn-off (t_{off}) delay time is not shown. It can be observed in Fig. 2 that the inverter output voltage v_{ao} depends on the polarity of the phase current (e.g., i_{inv}) in each switching

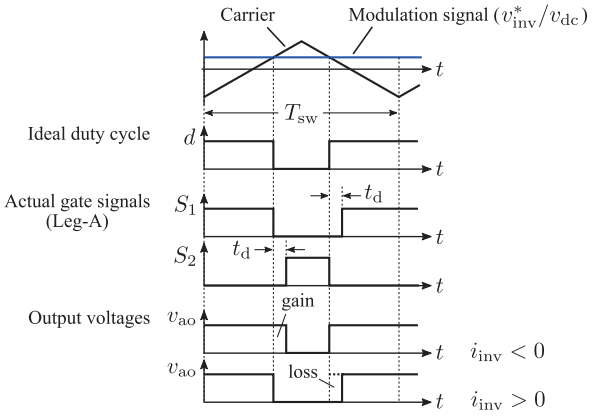

Fig. 2. Output voltages of Leg-A shown in Fig. 1 considering the dead time effect in one switching period $T_{\rm sw}$, where the turn-on and turn-off delays of the power devices are not shown.

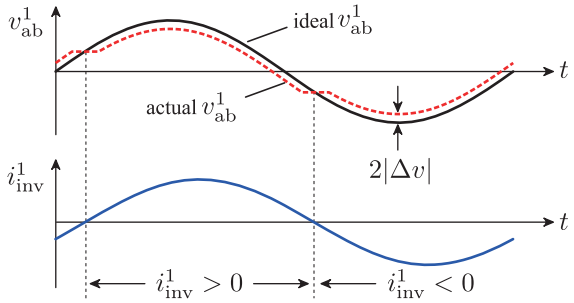

Fig. 3. Dead time effect on the fundamental-frequency inverter output voltage $v^1_{\rm ab}$ in the case of a pure sinusoidal output current $i^1_{\rm inv}$ [15].

interval ($T_{\rm sw}$). Specifically, when the phase current is positive ($i_{\rm inv} > 0$), the inverter output voltage $v_{\rm ao}$ is reduced (voltage loss), and when it is negative ($i_{\rm inv} < 0$), the inverter output voltage $v_{\rm ao}$ is increased (voltage gain), in contrast to the ideal case, where no dead time is inserted.

According to Fig. 2, in one switching period, the distorted voltage Δv (i.e., the voltage changes due to the dead time) can be averaged as

$$\Delta v = \begin{cases} \dfrac{-t_{\rm d} - t_{\rm on} + t_{\rm off}}{T_{\rm sw}} v_{\rm dc}, & i_{\rm inv} > 0 \\ \dfrac{t_{\rm d} + t_{\rm on} - t_{\rm off}}{T_{\rm sw}} v_{\rm dc}, & i_{\rm inv} < 0 \end{cases} \tag{1}$$

and assuming $t_{\rm on} = t_{\rm off}$ yields,

$$|\Delta v| \approx \frac{t_{\rm d}}{T_{\rm sw}} v_{\rm dc} \tag{2}$$

where $T_{\rm sw}$ is the switching period and $v_{\rm dc}$ is the instantaneous DC-link voltage. It can be seen in (2) that either a decrease of the dead time or an increase of the switching period (i.e., decreasing the switching frequency) will contribute to smaller voltage distortions $|\Delta v|$. However, a PWM converter with a lower switching frequency requires a large filter to mitigate the switching-frequency harmonics. Replacing the filter can be a costly task in pre-designed systems. On the other hand, with a shorter dead time period, the converter legs have risks of short-circuiting.

A similar analysis can be applied to the other leg (i.e., Leg-B) in order to obtain the dead time effect on the inverter output voltage $v_{\rm inv}$. When considering the leakage currents [2], [35]–[37], a bipolar modulation scheme is adopted, in which two pairs of power devices (S_1-S_4 and S_2-S_3) of Leg-A and Leg-B are switched synchronously in a diagonal way, leading to $v_{\rm bo} = -v_{\rm ao}$. Accordingly, the inverter output voltage $v_{\rm inv} = v_{\rm ab}$ can be obtained as

$$\begin{aligned} v_{\rm inv} &= v_{\rm ao} - v_{\rm bo} \approx \begin{cases} v^1_{\rm ab} - 2|\Delta v|, & i_{\rm inv} > 0 \\ v^1_{\rm ab} + 2|\Delta v|, & i_{\rm inv} < 0 \end{cases} \\ &\approx v^1_{\rm ab} - 2 \cdot sgn(i_{\rm inv}) \cdot |\Delta v| \end{aligned} \tag{3}$$

in which $v^1_{\rm ab}$ is the ideal inverter output voltage without the dead time $t_{\rm d}$ and the switching-frequency harmonics in the inverter output voltage are not considered. In addition, in (3), $sgn(x) = 1$, if $x > 0$; otherwise, $sgn(x) = -1$. It is worth mentioning that the adoption of a bipolar modulation is to maintain lower leakage currents. However, it will give a rise to the ripple currents, and thus additional power losses. On the contrary, the removal of the isolation transformers can compromise the power losses to a certain extent.

It can be seen in (3) that, due to the dead time voltage distortion Δv, the inverter output PWM voltage $v_{\rm inv}$ will be degraded, as demonstrated in Fig. 3. Consequently, the distortions of the inverter output PWM voltage $v_{\rm inv}$ will propagate to the inverter output current $i_{\rm inv}$, and thus the injected grid current $i_{\rm g}$ in the case of a closed-loop control [4]. This can be further illustrated with a simplified system model shown in Fig. 4, where the *LCL* filter is approximated as a single *L* filter. Referring to Fig. 4(a) and the Kirchhoff's Voltage Law (KVL), the inverter output voltage $v_{\rm inv}$ can be given as

$$v_{\rm inv} = v_{\rm g} + L\frac{di_{\rm inv}}{dt} \approx v_{\rm g} + L\frac{di_{\rm g}}{dt} \tag{4}$$

and thus the grid current $i_{\rm g}$ can be expressed as

$$\begin{aligned} i_{\rm g} &= \frac{1}{L}\int (v_{\rm inv} - v_{\rm g})dt \\ &= \underbrace{\frac{1}{L}\int (v^1_{\rm inv} - v_{\rm g})dt}_{i^1_{\rm g}\text{: fundamental}} + \underbrace{\frac{1}{L}\int v^{\rm h}_{\rm inv}dt}_{i^{\rm h}_{\rm g}\text{: harmonics}} \end{aligned} \tag{5}$$

with $L = L_1 + L_2$ being the *LCL* filter total inductance, $v^1_{\rm inv}$ and $v^{\rm h}_{\rm inv}$ representing the fundamental-frequency component and the harmonics of the inverter output voltage, respectively, where the grid voltage $v_{\rm g}$ is almost harmonic-free. Then, the fundamental-frequency phasor diagram in the case of the unity power factor operation can be obtained as shown in Fig. 4(b), where ω_0 is the grid fundamental angular frequency.

Observations from (3) and (5) and also Fig. 4 indicate that the harmonics of the inverter output voltage $v_{\rm inv}$ will affect the injected grid current $i_{\rm g}$. When assuming $v^1_{\rm ab} = v^1_{\rm inv}$, the resultant harmonics in the injected current due to the dead time can be obtained as

$$i^{\rm h}_{\rm g} = \frac{1}{L}\int \{-2 \cdot sgn(i_{\rm inv}) \cdot |\Delta v|\}dt \tag{6}$$

which implies that the grid current distortions induced by the dead time depend on the duration of this "blanking" period and

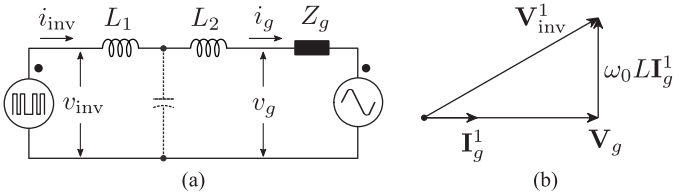

Fig. 4. Simplified single-phase inverter system: (a) *LCL* filter model and (b) fundamental-frequency phasor diagram in the unity power factor operation, where $L = L_1 + L_2$.

the polarity of the inverter output current. Additionally, in the above discussions, the bipolar modulation scheme is adopted, resulting in $v_{\text{bo}} = -v_{\text{ao}}$; while in the case of a unipolar modulation scheme (to enable the use of smaller output filters), the distribution of the dead time harmonics may be altered. Those are then explained in details as follows:

1) *Dead Time Duration Effect*

Large dead time will contribute to more voltage gains or losses according to Fig. 2, Fig. 3, and (3), thus leading to more distortions, since a couple of pulses are "covered" by the dead time (i.e., missing PWM pulses). As a result, the inverter will operate close to a square-wave modulated mode, where one pair of the power switching devices will always be in OFF- or ON-state during such a short period. It will, in turn, increase the magnitude of the fundamental-frequency inverter output voltage v^1_{inv} [15], and therefore, the magnitude of the fundamental-frequency grid current i^1_{g} will also increase according to Fig. 4(b). Thus, the injected grid current will be deteriorated, as it is shown in Fig. 5. In order to avoid this degradation, the maximum dead time duration can be approximated as

$$t^{\text{m}}_{\text{d}} \approx \frac{1}{2f_{\text{sw}}}\left(1 - \frac{V_{\text{gm}} + \omega_0 L I_{\text{gm}}}{V_{\text{dc}}}\right) \tag{7}$$

in which V_{gm}, I_{gm} are the grid voltage amplitude and the grid current amplitude, respectively, V_{dc} is the DC-link voltage, $f_{\text{sw}} = 1/T_{\text{sw}}$ is the switching frequency, and ω_0, L have been defined previously.

However, it is difficult to mitigate these distortions in a closed-loop current controller even with harmonic compensators due to its high non-linearity. In this cases, the controllability of the grid current by the power converter is lost. Instead, according to (7), an increase of the DC-link voltage V_{dc} will retain the controllability and such harmonics can be mitigated, since a larger magnitude of the fundamental-frequency inverter output voltage is possible to tolerate the dead time effect in this case. Notably, large DC-link voltages may incur more power losses and higher voltage stresses on the power devices (possibly challenging the reliability). Thus, in practice, the dead time cannot be excessive. Nonetheless, this constraint can be an add-on to the converter design, where a large dead time period is expected to ensure the safety of the converter operation. In contrast, this is limited by the controllability of the injected current (i.e., the above discussion). A contour plot of the maximum dead time is shown in Fig. 6, which can be a basic design consideration for single-phase full-bridge inverters.

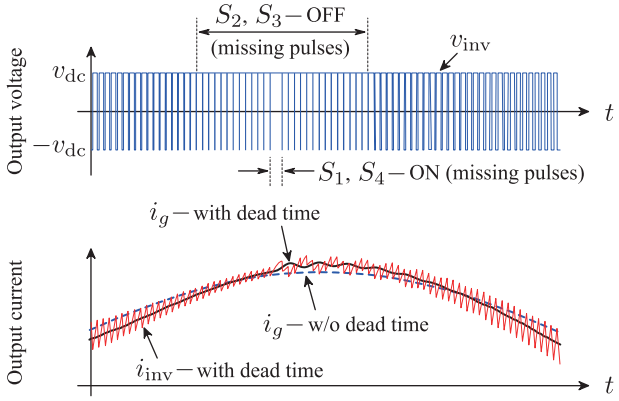

Fig. 5. Effect of large dead time on the closed-loop-controlled grid current with a fixed DC-link voltage ($V_{\text{dc}} = 400$ V).

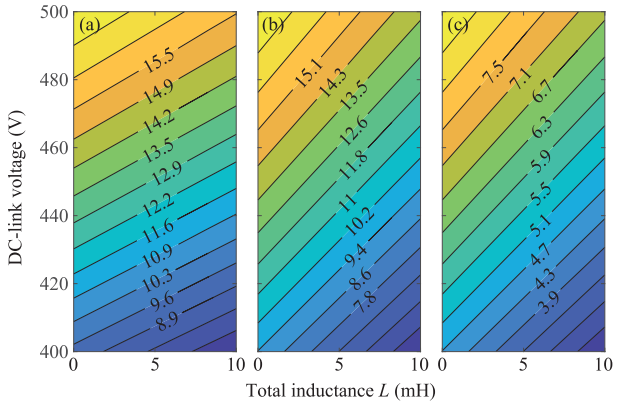

Fig. 6. Maximum dead time (i.e., t^{m}_{d} in μs) in relation to the DC-link voltage and the total inductance L of the *LCL* filter: (a) at 1-kW power level with f_{sw} = 10 kHz, (b) at 2-kW power level with f_{sw} = 10 kHz, and (c) at 2-kW power level with f_{sw} = 20 kHz, where V_{gm} = 325 V, ω_0 = 314 rad/s, and the resistance of the inductors is not considered.

2) *Polarity Effect (Zero-Crossing)*

It is demonstrated in (3), (6), and Fig. 3, that the degradation of the inverter output voltage and thus the distortions of the grid current are dependent on the inverter output current polarity. In general, when the inverter output voltage and the inverter output current have the same polarity, the inverter voltage magnitude will be reduced; otherwise, the dead time will give a magnitude increase of the inverter output voltage, as illustrated in Fig. 3. This implies that the transition from voltage gains to losses or vice versa occurs when either the polarity of the inverter output current or the polarity of the inverter output voltage changes. It happens especially in grid-connected applications in order to achieve the unity power factor operation, as shown in Fig. 4(b).

Moreover, as it is shown in Fig. 5, the output inverter current contains high switching-frequency ripples, and thus multiple polarity changes will occur around current zero-crossing points. This will also affect the inverter output current [22], [29]. In the case of a grid-connected PWM inverter operating at unity power factor as shown

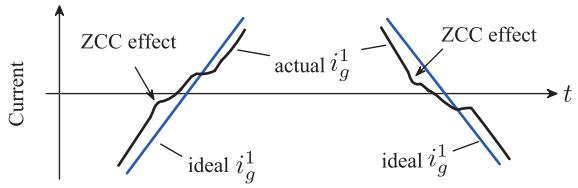

Fig. 7. Effect of zero-crossing points (ZCC: zero-current-clamping) on the fundamental-frequency injected grid current.

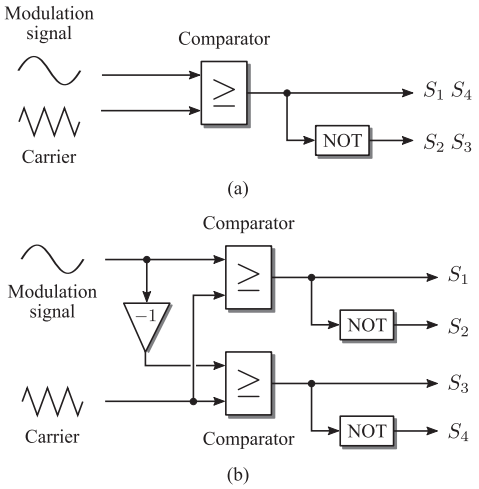

Fig. 8. Two modulation schemes for the single-phase full-bridge inverter shown in Fig. 1: (a) the bipolar modulation scheme and (b) the unipolar modulation scheme.

in Fig. 4, the inverter output current (and thus the grid current) should be lagging behind the inverter output voltage. As a consequence, before the inverter output current polarity changes from negative to positive (or vice versa), there will be a polarity inverse for the inverter output voltage, which will contribute to the Zero-Current-Clamping (ZCC) effect. Therefore, the injected grid current will approach to zero in both cases, as it is exemplified in Fig. 7. A detailed analysis of the ZCC impact on the current distortions considering dead time is directed to [22], [29], and [38].

3) *Modulation Strategy Effect*

As mentioned previously, the bipolar modulation scheme is adopted firstly, considering the transformerless applications. In practice, it is also more common to use a unipolar modulation scheme in order to reduce the requirement of bulky filtering inductors, where however, an isolation transformer is required. In the case of the unipolar modulation, each leg of the full-bridge inverter is modulated separately. Fig. 8 shows the modulation schemes for the inverter (i.e., the bipolar and unipolar modulation schemes). Clearly, the phase-leg output voltages (i.e., v_{ao} and v_{bo}) are related to the modulation, and thus the inverter output voltage v_{inv} is affected by the PWM schemes. The impact lies that the commutation in each case will be different, and the distribution of the dead time harmonics is thus changed. The effect of the modulation on the dead time harmonic distribution will be demonstrated by simulations in § IV.

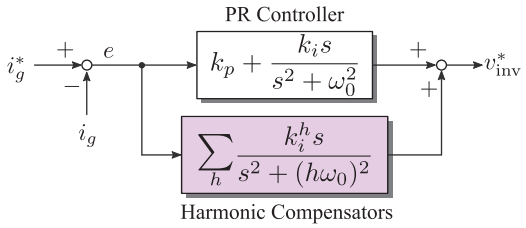

Fig. 9. Proportional resonant (PR) current controller for a single-phase inverter system with multiple resonant controllers (RSCs) to compensate dead time harmonics.

The above analysis reveals that the dead time effect is of high non-linearity, which thus results in much difficulty to compensate the distortions. However, the harmonics induced by the dead time can still be expanded into Fourier series, whose frequencies are integer-times of the fundamental grid frequency (even- and odd-order harmonics), mainly consisting of low-order harmonics [15], [20]. It thus enables the use of harmonic compensators to achieve a satisfactory THD of the injected grid current.

B. Resonant Control based Harmonic Compensation

In order to ensure a good power quality, parallel RSCs can be used as the harmonic compensators [4], [7], [11]. A PR controller has been used as the fundamental-frequency current controller. Then, the entire current control system with an RSC-based harmonic compensator is shown in Fig. 9. Accordingly, the open-loop transfer function of the entire current control loop can be obtained as

$$G_{\text{op}}(s) = \frac{v_{\text{inv}}^*(s)}{e(s)} = \underbrace{k_{\text{p}} + \frac{k_{\text{i}} s}{s^2+\omega_0^2}}_{G_{\text{PR}}(s)} + \underbrace{\sum_h \frac{k_{\text{i}}^h s}{s^2+(h\omega_0)^2}}_{G_{\text{RSC}}(s)} \quad (8)$$

where k_{p} and k_{i} are the control gains for the PR controller $G_{\text{PR}}(s)$, k_{i}^h is the control gain for an individual RSC harmonic compensator $G_{\text{RSC}}(s)$ with h being the harmonic order, and ω_0 is defined previously.

As the dead time harmonics are mainly low-order harmonics, the RSC-based harmonic compensation can effectively compensate those harmonics according to (8). It is also demonstrated by the Bode diagram shown in Fig. 10, which illustrates that the RSC gain will approach to infinity at its resonant frequency. Hence, paralleling multiple RSCs is an attractive alternative to compensate any harmonic of interest with much flexibility of parameter tuning. However, the system resonance is apt to be triggered when the relatively high-order harmonics (e.g., the 13$^{\text{th}}$ harmonic) induced by the dead time are compensated, and thereby challenging the overall system stability [39], [40]. This is possibly because the central frequencies of the resonant controllers are approaching to the filter resonance frequencies and also due to the system delays. In addition, multiple parallel connections also increase the computational burden [8] when implemented in a digital signal processor. To address the issue of resonance when high-order harmonics are compensated by RSCs, the phase compensation for each individual RSC should be included [9], and thus leading to an increase in complexity.

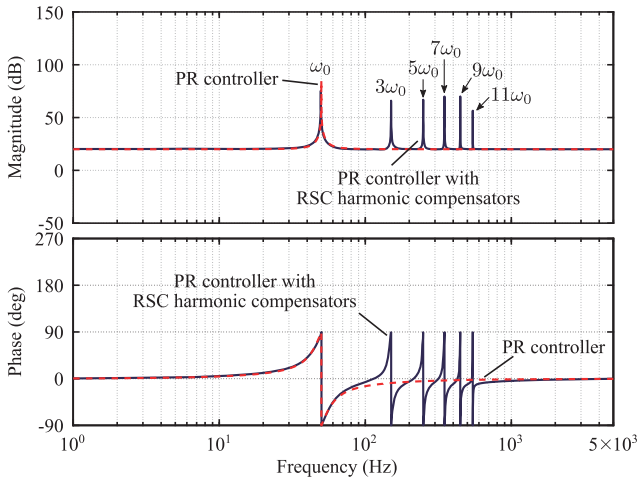

Fig. 10. Bode plot of the open-loop current controller consisting of a proportional resonant (PR) controller with resonant harmonic compensators (RSC), where the 3rd-, 5th-, 7th-, 9th-, and 11th-order harmonics are compensated, and the sampling frequency is f_s = 10 kHz.

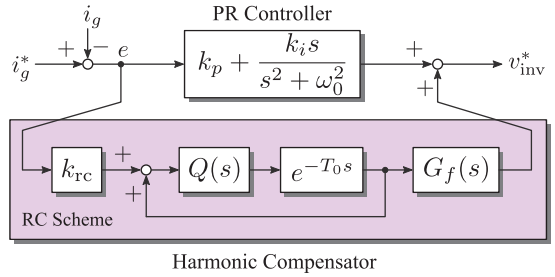

Fig. 11. Proportional resonant (PR) current controller for a single-phase inverter system with a repetitive controller (RC) to compensate the dead time harmonics.

C. Repetitive Control based Harmonic Compensation

Due to the risk of triggering resonances, the RSC harmonic compensator is normally used to compensate selected low-order odd harmonics (e.g., the 3rd-, 5th-, and 7th-order harmonics), since these are the main contributors to the current distortions in single-phase full-bridge converters [9]. However, the dead time mainly induces low-order distortions [15], [20] that may be up to a higher order (e.g., the 11th-order) and also may contain even-order harmonics. Therefore, a good THD of the injected current is far reached only by compensating these low-order odd harmonics with the RSC compensators.

Alternatively, according to the internal model principle [8], [32], any periodic signal (e.g., the expanded dead time harmonics) can be tracked with zero errors in steady-state, as long as a generator of the reference is included in a stable closed-loop control system. The RC scheme is a typical representative of such controllers. Thus, this inspires the use of the RC as a harmonic compensator to mitigate the dead time distortions [4], [29]. However, it should be noted that, although the RC can suppress all harmonics below the Nyquist frequency theoretically, its response is slow and the stability might be challenged as discussed in [22] and [29], where the RC harmonic compensator is implemented in the angle domain and the complexity is increased. In this paper, the RC is reconstructed by introducing an appropriate phase-lead compensation and a low pass filter, so that the controller can operate with an ensured stability, while with an enhanced performance in contrast to the RSC-based harmonic compensator.

Considering the dynamics, the PR controller is again adopted as the fundamental-frequency current controller to ensure a fast tracking of the fundamental grid current, and the RC is thus taken as a plug-in parallel harmonic compensator, as it is shown in Fig. 11. Accordingly, the entire current controller with an RC harmonic compensator $G_{\text{RC}}(s)$ can be expressed as

$$G_{\text{op}}(s) = \frac{v_{\text{inv}}^*(s)}{e(s)} = G_{\text{PR}}(s) + \underbrace{k_{\text{rc}} \frac{e^{-T_0 s} Q(s) G_f(s)}{1 - e^{-T_0 s} Q(s)}}_{G_{\text{RC}}(s)} \tag{9}$$

in which k_{rc} is the control parameter of the RC harmonic compensator $G_{\text{RC}}(s)$, $\omega_0 = 2\pi/T_0$ is the grid fundamental frequency with T_0 being the grid fundamental period. Notably, as aforementioned, a low pass filter $Q(s)$ is included in the RC compensator to eliminate the high frequency harmonics so that the controller stability can be attained [8], [9], [41]. However, the tracking accuracy might be degraded by the low pass filter. Typically, it is chosen in the z-domain as [8], [9]:

$$Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1} \tag{10}$$

where $2\alpha_1 + \alpha_0 = 1$, $\alpha_1 > 0$, and $\alpha_0 > 0$. In respect to the design of the lower pass filter, it can be done by examining the harmonic content of the injected current controlled only by a PR controller, where the bandwidth of the low pass filter can be determined to cover the majority of the harmonic components. In addition, a phase-lead compensator $G_f(s)$ is also incorporated in the RC compensator considering the closed-loop system stability. In the z-domain, the phase-lead compensator is given as

$$G_f(z) = z^m \tag{11}$$

with m being the phase-lead number, which is determined by experiments in practice (i.e., the trial and error method). With the above design considerations, the controller of (9) can be cost-effectively implemented in a digital signal processor without many computational efforts [8]–[10], where a more detailed parameter tuning of the RC scheme can be found.

Actually, the ideal RC (i.e., the one in (9) with the low pass filter $Q(s) = 1$ and the phase-lead compensator $G_f(s) = 1$) can be expanded as

$$G_{\text{RC}}(s) = k_{\text{rc}} \left[-\frac{1}{2} + \frac{1}{T_0 s} + \frac{2}{T_0} \left(\sum_h^{\infty} \frac{s}{s^2 + (h\omega_0)^2} \right) \right] \tag{12}$$

in which $h = 1, 2, 3, \ldots$ is the harmonic order (including the fundamental component). In practical applications, the RC scheme in the z-domain is more widely adopted as

$$G_{\text{RC}}(z) = k_{\text{rc}} \frac{z^{-N} Q(z) G_f(z)}{1 - z^{-N} Q(z)} \tag{13}$$

with $N = \lfloor f_s T_0 \rfloor$ and f_s being the sampling frequency. Clearly, the RC in (13) can be implemented in a digital microprocessor using cascaded delays.

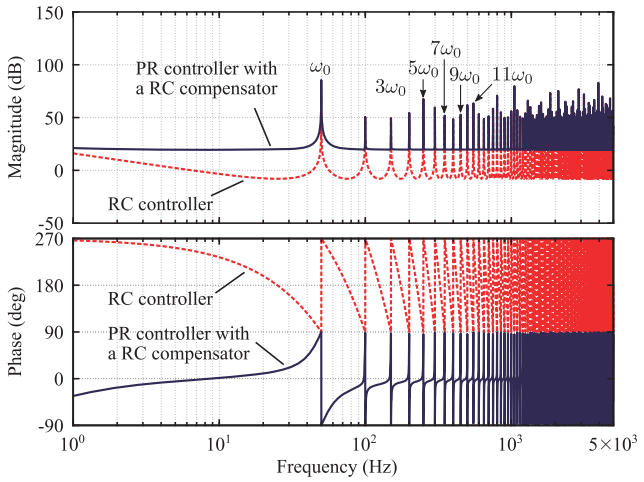

Fig. 12. Bode plot of the open-loop current controller consisting of a proportional resonant (PR) controller with a parallel repetitive controller (RC) as the harmonic compensator, where the sampling frequency f_s = 10 kHz, $Q(s) = 1$, and $G_f(s) = 1$.

Additionally, in typical cases, $h \leq N_f$, where $N_f = \lfloor f_s T_0/2 \rfloor$ is the Nyquist frequency. It is indicated by (12) that the RC scheme can compensate the harmonics up to the Nyquist frequency, since it contains N_f individual RSCs in parallel. Each RSC can approach an infinite gain at the corresponding resonant frequency $h\omega_0$, as shown in Fig. 12. Furthermore, Fig. 12 and (12) suggest that the PR current controller with the RC harmonic compensator can suppress all the harmonics, including the dead time harmonics. However, as it can be observed in (12), it is difficult to optimize its dynamic performance since it has an identical control gain $2k_{\rm rc}/T_0$ when compared to the multiple RSC harmonic compensators with separate gains (i.e., $k_{\rm i}^h$) to tune. Nevertheless, efforts have been devoted to develop optimal repetitive controllers [8], [9] for selective harmonics, which can also be utilized in mitigating the dead time harmonics. Notably, as discussed previously, the phase compensation (i.e., $G_f(z)$) has been considered in the plug-in RC harmonic compensator, which is simple but ensures the stability of the entire control system [9]. The design of the phase-lead compensation requires much less efforts compared to the RSC compensators. It is worth mentioning that due to the compact inclusion of all the resonant controllers in the RC compensator shown in (12), a proportional controller can be adopted to replace the PR fundamental frequency controller. However, the dynamics in tracking the fundamental-frequency component are degraded as discussed previously. On the other hand, when the grid fundamental frequency varies (it is practical), the number of cascaded delays N will be fractional according to (13). Due to the rounding process when implemented in a digital controller, the accuracy of the RC scheme decreases, and thus the harmonic compensation performance is degraded. From this viewpoint, the RC scheme is frequency-sensitive. Nonetheless, many attempts have been made to adapt the RC scheme to frequency variations, as the one in [10] by online changing the sampling frequency and another one in [41] by approximating the fractional number of delays with a Lagrange interpolation polynomial. It is also worth mentioning that the varying frequency makes the tracking performance of resonant controllers degraded as well. In this case, the instantaneous grid frequency has to be fed back to update the central frequencies of the resonant controllers in order to maintain the performance.

TABLE I
SYSTEM PARAMETERS OF THE SINGLE-PHASE SYSTEM.

Parameter	Symbol	Value
Rated power	$P_{\rm n}$	2 kW
DC-link voltage	$V_{\rm dc}$	400 V/450 V
Grid voltage in RMS	$V_{\rm g}$	230 V
Grid frequency	ω_0	$2\pi\times50$ rad/s
DC-link capacitor	$C_{\rm dc}$	1100 μF
	L_1	3.6 mH
LCL filter	$C_{\rm f}$	2.35 μF
	L_2	4 mH
Sampling frequency	$f_{\rm s}$	10 kHz

TABLE II
CONTROLLER PARAMETERS.

Controller	Parameter
PR controller	$k_{\rm p}$ = 10, $k_{\rm p}$ = 1200
RSC controller	$k_{\rm i}^3 = k_{\rm i}^5 = k_{\rm i}^7$ = 800, $k_{\rm i}^9$ = 500, $k_{\rm i}^{11}$ = 200
RC Controller	$k_{\rm rc}$ = 0.8
Low pass filter $Q(z)$	α_0 = 0.5, α_1 = 0.25
Phase-lead number	m = 3

IV. SIMULATIONS AND EXPERIMENTAL VERIFICATIONS

Referring to Fig. 1, simulations and experiments have been performed on a single-phase grid-connected inverter system to verify the analysis. In experiments, a Delta DC power supply is adopted as the DC-link. A commercial inverter with a fixed dead time of $t_{\rm d}$ = 3.25 μs (hardware dead time) and a constant switching frequency of $f_{\rm sw}$ = 10 kHz is connected to a programmable grid simulator (California Instrument MX-30) through an *LCL* filter and an isolation transformer. Control systems are implemented in a dSPACE DS 1103 system, which can produce programmable PWM signals with different dead time durations (software dead time). The other parameters of the grid-connected inverter system are given in Table I. The controllers are designed in accordance with the above discussions, and the parameters are listed in Table II. For comparison, the parameters in simulations are the same as those in experiments.

First, the impacts of PWM schemes are studied by simulations, and the results are shown in Figs. 13 and 14. In the simulations, the dead time was set as 5.25 μs for better visibility, and the system is controlled solely by the fundamental-frequency PR controller. Observations in Fig. 13 clearly indicate that the PWM schemes for the single-phase full-bridge inverter will change the output currents shapes (i.e., the harmonic distortions due to dead time). This is mainly due to the commutation paths of the two modulation schemes,

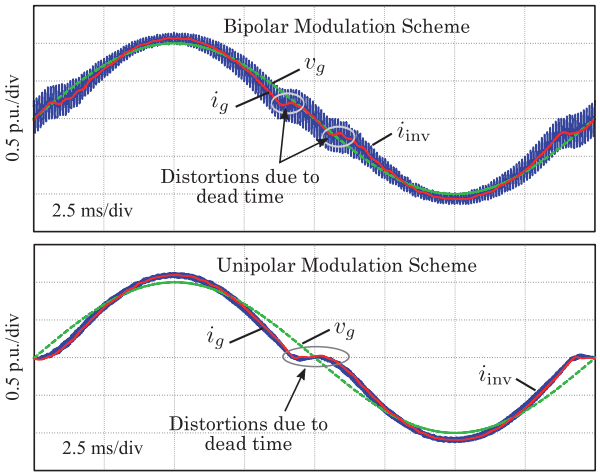

Fig. 13. Simulation results of the single-phase full-bridge inverter with the dead time being 5.25 μs, where no harmonic compensation was added to the current control loop (i.e., the inverter is only controlled by the PR fundamental-frequency controller).

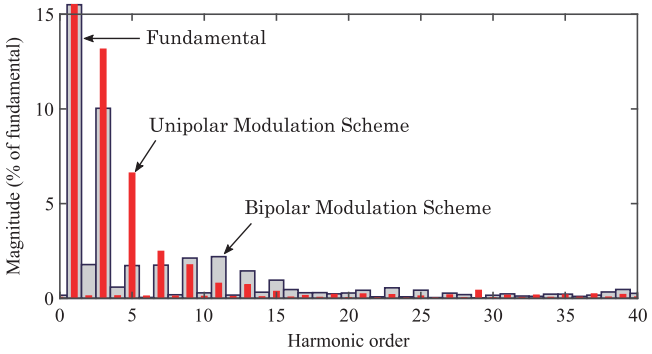

Fig. 14. Harmonic distributions of the grid currents (i.e., the simulations in Fig. 13) injected by the single-phase full-bridge inverter with two modulation schemes (i.e., the bipolar modulation and unipolar modulation schemes in Fig. 8). For demonstration of the effect of modulation schemes, the dead time was selected as 5.25 μs.

as discussed previously. Nevertheless, it has been further confirmed in Fig. 14 that with the bipolar modulation scheme, odd-order harmonics appear in the grid current. In that case, only incorporating the even-order RSC compensators may not achieve a satisfactory THD level. By contrast, the unipolar modulation scheme generates negligible odd-order harmonics, where however the magnitudes of the low-order harmonics are higher than those of the system with the bipolar modulation scheme. In all, the above simulations have demonstrated that the modulation scheme will affect the dead time harmonics, and thus the current quality. It is worth pointing out that the selection of the modulation schemes depends on applications. The unipolar modulation scheme leads to that the dead time harmonics concentrate at low- and even-orders, and it reduces the requirements of output filters. However, the common-mode voltage of the inverter will vary with the switching frequency when the unipolar scheme is adopted. Seen from this perspective, the bipolar modulation scheme results in a constant common-mode voltage (low leakage currents), which is beneficial to transformerless PV systems.

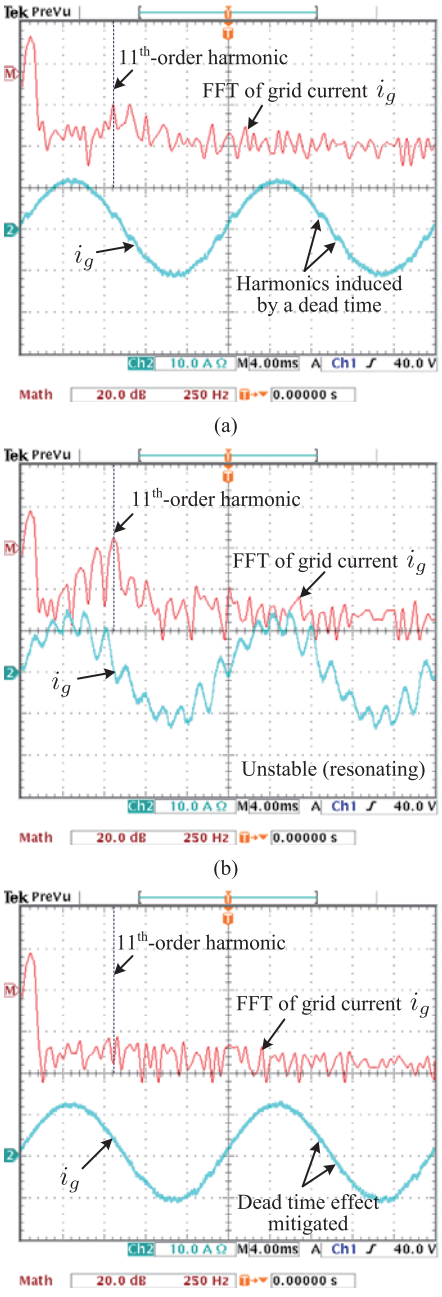

Fig. 15. Experimental results of a 2-kW single-phase grid-connected PWM inverter system at unity power factor operation with the RSC or RC harmonic compensator (f_{sw} = 10 kHz, t_d = 3.25 μs, V_{dc} = 400 V, CH 2 - grid current i_g [10 A/div, 4 ms/div] and CH M - FFT of the grid current i_g [20 dB/div, 250 Hz/div]): (a) when the 3rd-, 5th-, 7th-, and 9th-order RSCs are employed, (b) when the 11th-order RSC is adopted, and (c) when the RC compensator is used. Here, FFT represents Fast Fourier Transform.

In the following, the analysis is validated through experiments, where the bipolar modulation scheme is adopted for the application of transformerless PV systems. The single-phase PWM inverter only with the hardware dead time was firstly tested under a "clean" grid (i.e., very low background distortion). Fig. 15 shows the experimental results of the system operating at a unity power factor with an RSC or RC as the harmonic compensator to mitigate the harmonics due

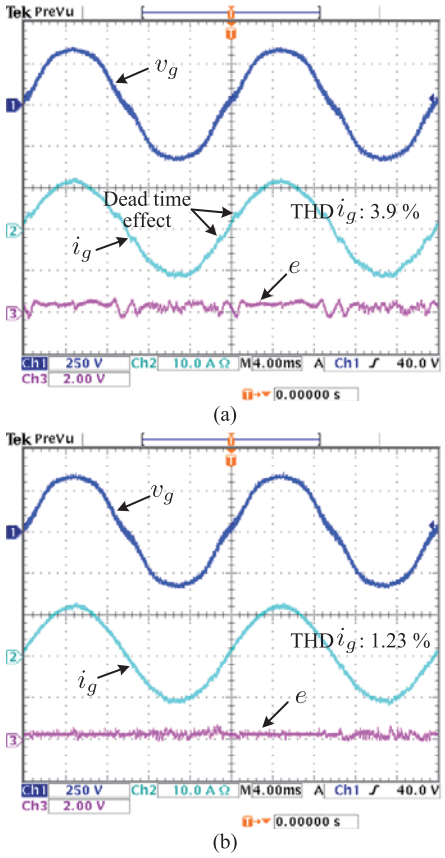

Fig. 16. Steady-state performance of the system under a distorted grid with (a) the 3rd-, 5th-, 7th-, and 9th-order RSCs and (b) the RC-based harmonic compensator (grid voltage THD 4.6%, dead time duration t_d = 3.25 μs, grid voltage v_g [250 V/div], grid current i_g [2 A/div], current tracking error $e = i_g^* - i_g$ [4 A/div], time [4 ms/div]).

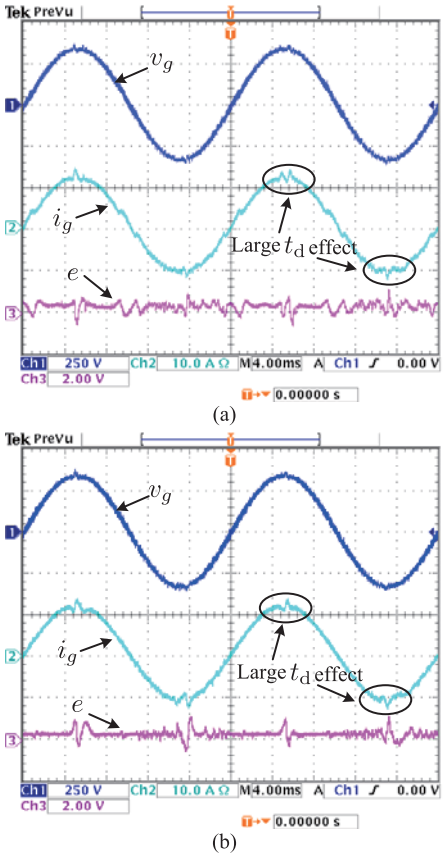

Fig. 17. Steady-state performance of the system under a large dead time with (a) the 3rd-, 5th-, 7th-, and 9th-order RSCs and (b) the RC-based harmonic compensator (grid voltage THD 0.86%, dead time duration t_d = 5.25 μs, grid voltage v_g [250 V/div], grid current i_g [2 A/div], current tracking error $e = i_g^* - i_g$ [4 A/div], time [4 ms/div]).

to the dead time. As it is shown in Fig. 15, both the RSCs and the RC can effectively mitigate the low-order harmonics. However, as it can be seen from the Fast Fourier Transform (FFT) results of the grid current i_g in Fig. 15(a), the dead time also induces higher odd-order harmonics, e.g., 11th- and 13th-order harmonics. This has also been observed in simulations shown in Fig. 14. In order to compensate those harmonics using the RSC harmonic compensators and thus to further improve the current quality, the 11th-order RSC has been added in parallel with other RSCs. However, the system resonance is triggered, and then the system goes into instability, as it is shown in Fig. 15(b). In contrast, the use of an RC as the harmonic compensator can be beneficial to the dead time harmonic mitigation without resonant issues, as illustrated in Fig. 15(c). However, the harmonics are not fully eliminated, which means that the control parameters have to be further tuned and optimized, as discussed in § III.

Additionally, the PR controller with the RC harmonic compensator is also tested under various grid voltage distortions (i.e., background distortions) with different dead time durations. The THD levels of the injected current i_g are compared to those of the same system, where the RSC harmonic compensators are adopted in parallel with the PR fundamental-frequency current controller. Figs. 16 and 17 firstly demonstrate the steady-state performance of the PR-controlled system with different harmonic compensators under a distorted grid and large dead time durations, respectively. As it can be seen in Fig. 16(a), although the RSC based compensator can suppress the harmonics to some extent, the dead time effect remains in the injected grid current, requiring a higher-order RSC to mitigate it. However, doing so may lead to resonances as it is demonstrated in Fig. 15. In contrast, the PR current controller with the RC harmonic compensator can effectively eliminate the harmonics either from the grid voltage background distortions or the dead time effect, and thus contributing to an almost harmonic-free grid current, as it is shown in Fig. 16(b).

However, when the dead time is increased to 5.25 μs, the effect from dead time on the current distortion appears again, as it is shown in Fig. 17. According to (7) and the parameters in Table I, the maximum dead time can be approximated to $t_d^m \approx 5.7$ μs. In the consideration of a weak grid (i.e., the leakage inductance of the isolation transformer in the experiments), the maximum dead time will be smaller than 5.7 μs, according to Fig. 6. As a consequence, the large dead time of 5.25 μs will exceed the limitation, resulting in more distortions in the grid current. As it is shown in Fig. 17, such harmonics are difficult to compensate even using the RC

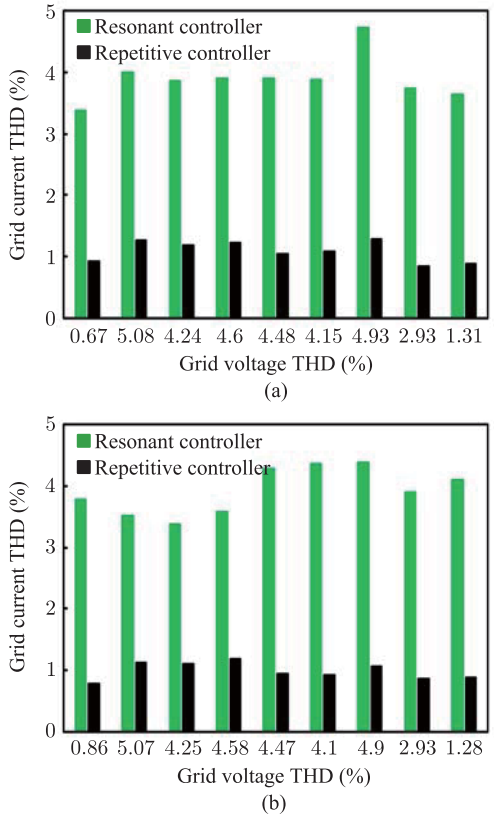

Fig. 18. Total harmonic distortion (THD) of the injected current under different grid voltage THD levels using resonant (blue) and repetitive (black) controllers as the harmonic compensator considering different dead time t_d: (a) t_d = 3.25 μs and (b) t_d = 5.25 μs.

due to the high non-linearity. In this case, the single-phase full-bridge PV inverter lost the controllability of the injected current, since the DC-link is insufficient to provide an average control voltage. Nonetheless, the above experimental results are in close agreement with the discussions in § III, where it has been mentioned that increasing the DC-link voltage is a possibility to remove these distortions. Additionally, such a case of insufficient DC-link voltage indicates the ill-design of the hardware system, which should be avoided. In other words, it means that the maximum dead time in Fig. 6 can be a criteria in the design phase and thus offers the possibility to consolidate the inverter system design.

More comparisons by experiments are presented in Fig. 18 under various voltage distortions. It can be observed that the PR current controller with the RC harmonic compensator can achieve an overall lower current THD level, and more importantly, the performance is independent on the grid voltage distortions with shorter or longer dead time (however, this is constrained by the hardware, i.e., Fig. 6). Compared to this, although the PR control with RSC harmonic compensators can also achieve an overall THD level lower than 5 %, individual harmonics may exceed the limitations that are defined in standards, e.g., the *IEEE Std. 1547* [34]. These harmonics become of interest in order to meet the requirements. Moreover, with the RSC harmonic compensators, resonances may be triggered as it has been demonstrated in Fig. 15. Notwithstanding, the simulation and experimental results have verified the discussion on the emission mechanism of dead time harmonics of the single-phase full-bridge inverter and the effectiveness of the RC-based harmonic controller to compensate the harmonics, including the distortions induced by the dead time.

V. Conclusion

In this paper, an analysis of the dead time effect on the grid current quality was in-focus for single-phase grid-connected full-bridge inverters. It has been revealed that the dead time changes the inverter output voltages, thus distorting the grid current. Its impact on the current quality is related to the "blanking" duration, the polarity of the inverter current, and also the modulation strategies. Based on the analysis, harmonic compensators using parallel resonant controllers or repetitive controllers were applied to mitigate the dead time harmonics. In contrast to the conventional solutions to dead time harmonic compensation, the repetitive-based method requires no hardware modifications and it is easy to implement in a cost-effective digital controller. Experimental verifications have been performed on a single-phase grid-connected PWM inverter with the repetitive-based dead time harmonic compensator. The performance was also compared with the parallel resonant harmonic controllers to compensate the dead time harmonics, which may introduce instability due to resonances. Test results have verified that, regardless of the background voltage distortions, the repetitive controller-based harmonic mitigation can effectively improve the current power quality (i.e., mitigate the dead time effect as well as other low-order harmonics) without stability problems if designed properly, compared to the resonant controller.

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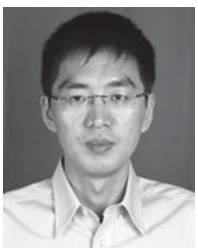

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