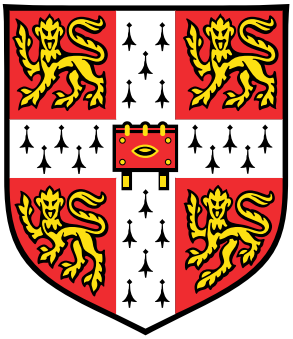
GaN-on-Silicon HEMTs and Schottky diodes for high voltage applications



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Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This dissertation is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text. This dissertation contains approximately 42,000 words including appendices, bibliography, footnotes, tables and equations and has 89 figures.

Loizos Efthymiou
April 2018

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Abstract

Gallium Nitride (GaN) is considered a very promising material for use in the field of power devices as its application in power systems would result in a significant increase in the power density, reduced power losses, and the potential to operate at high frequencies. The wide bandgap of the material allows a high critical electric field to be sustained which can lead to the design of devices with a shorter drift region, and therefore with lower on-state resistance, if compared to a silicon-based device with the same breakdown voltage. The use of an AlGaN/GaN heterostructure allows the formation of a two-dimensional electron gas (2DEG) at the heterointerface where carriers can reach very high mobility values. These properties can lead to the production of High Electron Mobility Transistors (HEMTs) and Schottky barrier diodes with superior performance, even when compared to devices based on state-of-the-art technologies such as Silicon Carbide or superjunctions. Furthermore, epitaxial growth of GaN layers on silicon wafers allows a significant reduction in the production cost and makes these devices competitive from a price perspective. This thesis will deal with a variety of topics concerning the characterization, design and optimization of AlGaN/GaN HEMTs and Schottky diodes with a 600 to 650V rating. Discussion will span several topics from device cross-section physics to circuit implementation and will be based on both experimental results and advanced modelling.

More specifically, the thesis is concerned with the characterization of AlGaN/GaN Schottky diodes and extraction of their main parameters such as ideality factor, barrier height and series resistance. A thorough investigation of their reverse recovery performance and a comparison to competing technologies is also given. Several topics which concern the operation of AlGaN/GaN HEMTs are then discussed. The underlying physics of p-gate enhancement mode transistors are analysed followed by a discussion of the challenges associated with the implementation of these devices at a circuit level. Finally, a comparison of the performance of a specific area-saving layout (Bonding pad over active area) and a conventional design is given.

The thesis aims to significantly enhance the understanding of the behaviour of these devices to enable better or new commercial designs to emerge.

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- L. Efthymiou, G. Longobardi, G. Camuso, A. P. S. Hsieh and F. Udrea, Modelling of an AlGaN/GaN Schottky diode and extraction of main parameters, 2015 International Semiconductor Conference (CAS), Sinaia, 2015, pp. 211-214.
- L. Efthymiou et al., Zero reverse recovery in SiC and GaN Schottky diodes: A comparison, 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 71-74.
- L. Efthymiou et al., On the source of oscillatory behaviour during switching of power enhancement mode GaN HEMTs, Energies Journal, vol. 10, no. 3, 2017.
- L. Efthymiou, G. Longobardi, G. Camuso, T. Chien, M. Chen and F. Udrea, On the physical operation and optimization of the p-GaN gate in normally-off GaN HEMT devices, Applied Physics Letters, vol. 110, no. 12, 2017, pp 123502.
- F. Udrea, L. Efthymiou and G. Longobardi, Fast dV/dt and dI/dt in GaN Devices, European Centre for Power Electronics (ECPE) Workshop, March 2017.
- L. Efthymiou et al., Effect of device layout on the switching of enhancement mode GaN HEMTs, International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, 2018 (accepted).
- L. Efthymiou et al, Bonding pad over active area (BPOA) layout for lateral AlGaN/GaN power HEMTs and diodes : a critical view (under review).

List of Patent applications

- Field plate structure for bonding pad over active area (BPOA) layout for lateral AlGaN/GaN power HEMTs.

Chapter 1

Introduction

1.1 Overview of the field

Power electronics is the branch of electronics that deals with processing the voltage, current, frequency and phase from a particular source into specific forms which are optimal for the desired load to be powered.

Power devices are semiconductor devices used as rectifiers or switches in power electronics systems. Applications of power semiconductor devices are quite diverse and are required in systems with a range of power ratings and operating frequencies. A good illustration of this diversity can be seen in Fig. 1.1 [1].

Power electronics is an important field of research in aspiring low-carbon economies as estimations suggest that 50% [2][3] of electrical power consumed goes through some form of power conversion before it is utilized. Power devices lay at the heart of any power electronics circuit in such a way that enhanced specifications of power devices can lead to new possibilities in the power electronics sector.

Improved power electronics technologies can enable high penetration levels of renewable energy resources, large energy savings in high voltage direct current (HVDC) transmission systems, increases in efficiency of variable speed drives for electric motors and also pave the path for widespread use of electric vehicles. Progress in the field of power electronics is therefore very important in the attempt to achieve energy savings both domestically and in industrial applications both for commercial incentives and to contribute to the reduction of carbon dioxide emissions.

The aims of research in the field of power devices is to fulfil objectives such as increasing power density, reducing the size of devices, achieving improved high temperature performance, higher frequency response, lower leakage, and lower on-resistance all of which would add up to greater operating efficiency.

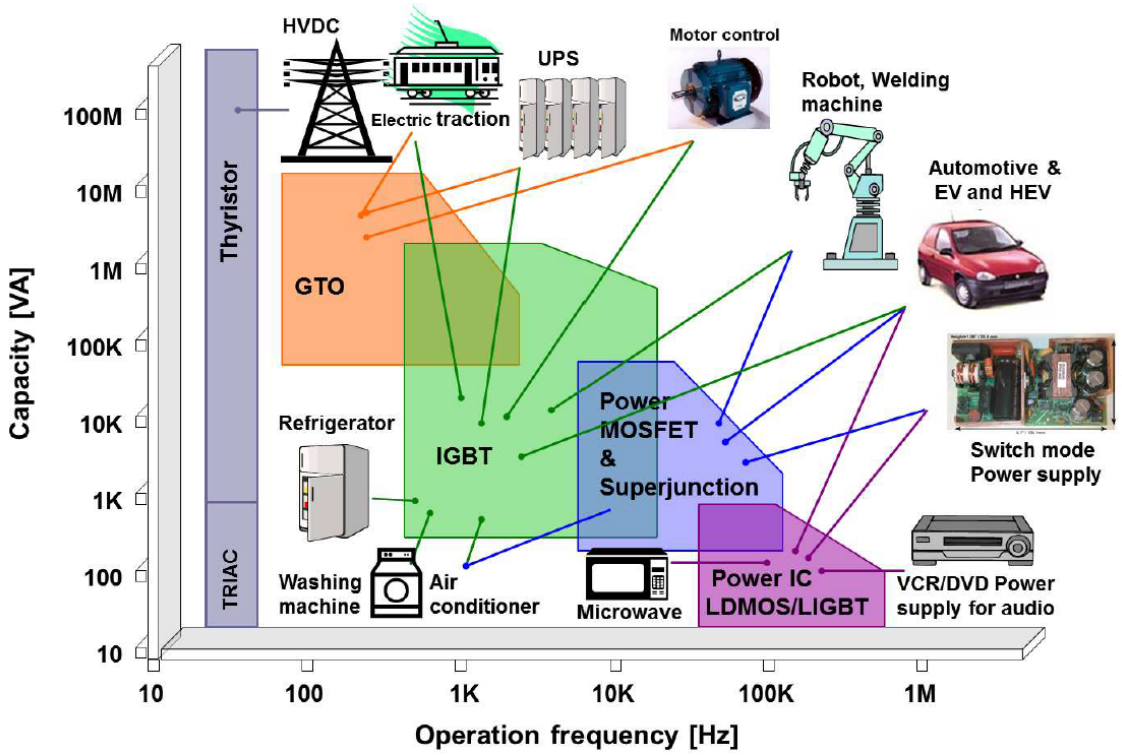


Fig. 1.1 Applications of power devices

1.2 Brief history of power devices

Research in the field of power devices originated with the invention of the bipolar transistor at Bell labs in 1948. Power rectifiers based on germanium were reported in the 1950s [4] with a switch to Silicon as the favoured material as the decade progressed. Silicon devices have dominated the field ever since with several different concepts being introduced. The thyristor structure was proposed in 1956 [5], followed by the gate turn-off thyristor in 1961[6]. A thyristor is a solid-state semiconductor device with four layers of alternating P- and N-type materials. It acts exclusively as a bistable switch, conducting when the gate receives a current trigger, and continuing to conduct while the voltage across the device is not reversed (forward-biased). Originally, thyristors relied only on current reversal to turn them off, making them difficult to apply for direct current; newer device types can be turned on and off through the control gate signal. The latter is known as a gate turn-off thyristor, or GTO thyristor.

The introduction of the power metal-oxide-semiconductor field effect transistor (MOSFET) in 1980 [7] was an important step in the growth of the power electronics market observed at this time due to its voltage controlled gate and high input impedance. A device which combines the voltage controlled gate of the MOSFET and the bipolar

on-state conduction seen in earlier devices was introduced in the mid 80s and named the insulated gate bipolar transistor (IGBT) [8][9]. Conductivity modulation in the drift region of IGBTs allows a reduction in on-state resistance and led to devices with higher current capability. Some compromise is however needed in the maximum achievable switching frequency and the transient losses due to the charge removal required when switching. This illustrates that, depending on the application requirements, different concepts appear more suitable.

At this point an important trade-off consideration in the field of power MOSFETs can be introduced. This trade off relates to the maximum breakdown voltage which can be achieved versus the on-state resistance observed in vertical power MOSFETs. This arises when the electric field distribution in an ideal planar p-n junction is considered. The reverse bias voltage needed to reach a critical electric field relates to the length and doping of the drift region. Reduced doping or increased drift region length can lead to higher breakdown but can also lead to greater on-state resistance thus the trade-off arises. This relationship is often referred to as the limit of silicon. However, a more accurate description would identify this as the limit of the specific technology of vertical power FETs. The relationship between specific on-resistance and breakdown voltage of an ideal drift region is given by:

$$R_{on} = 4BV^2/\epsilon_0\epsilon_r\mu_n{\xi_c}^3 \tag{1.1}$$

The denominator in the expression above is defined as Baliga figure of merit (BFOM) [10] and is based on minimizing conduction losses in vertical power FETs. It is worth mentioning that this assumes power losses to be solely due to on-state power dissipation and applies best to operation at lower frequencies where conduction losses dominate. It is clear that this figure of merit can be used to an extent to compare the capabilities of different materials as it contains terms which are linked to the intrinsic properties of a material. This will be discussed in more detail in the following section.

The concept for a device which can surpass the limit of Silicon was first presented in literature in 1997-1998 [11][12][13]. This concept is known as the super-junction and consists of highly n-doped and p-doped pillars in the device drift region. This offers a more optimized distribution of electric field in the drift region compared to conventional devices. While conduction occurs through only one of the pillars the increase in doping is such that a significant reduction in on-state resistance can still be observed. The superjunction concept has been implemented in different technologies (MOSFETs, IGBTs) leading to significant improvements in all round performance.

In conjunction with the vertical devices described so far another class of devices has received a lot of attention. These are lateral devices where the conduction path is parallel to the wafer surface rather than perpendicular. The advantage of these devices relates to their ability to be integrated monolithically with gate drive circuitry leading to the design of power integrated circuits. Similar concepts to the ones described for vertical devices are used in the design of these lateral devices with the lateral IGBT holding considerable market interest [14] and the superjunction concept applied in the lateral double diffused metal-oxide semiconductor (LDDMOS) [15].

While clever engineering has allowed the capabilities of silicon devices to be redefined for several decades, there is a case to be made for wide band-gap materials. The main materials which have received considerable attention as an alternative to silicon in power device applications are silicon carbide (SiC), gallium nitride (GaN) and diamond.

Research into wide bandgap materials for power electronics application can be traced back to the early 1990s [16][17]. The first wide bandgap device to be made commercially available was a SiC Schottky diode introduced by Infineon in 2001 [18]. Indeed that is where SiC devices have had most commercial success. In terms of three terminal devices, SiC JFETs, BJTs and MOSFETs have been introduced and are looking to compete in high voltage, high power applications [18]. The leading structures for the commercialization of GaN-based devices are high electron mobility transistors (HEMTs), metal-insulator-semiconductor FETs (MISFETs) and hetero-junction lateral Schottky diodes. For diamond devices most efforts are focused on the development of Schottky diodes however they still appear to be a long way from reaching the market. The suitability of wide bandgap materials for power device applications relates to their intrinsic properties which shall be discussed in more detail in the next section.

1.3 Comparison between GaN and other materials

As mentioned earlier, when referring to power devices we refer to two types of devices; switches and rectifiers. The field in both of those disciplines is currently dominated by silicon devices. In the field of switches a variety of different device structures exist (power MOSFET, IGBT, thyristor) depending on the particular requirements of the specific application for which the device is used. Silicon rectifiers are equally important in power electronics as they find use in equipment such as boost converters and are used as free wheeling diodes in bridge inverter topologies. In the field of rectifiers the latest in silicon technology comes in the form of ultrafast recovery P-I-N diodes that

utilize techniques such as carrier lifetime reduction and silicon-on insulator technologies to achieve operation at higher frequencies [19].

The dominance of silicon in the power devices industry arises from the maturity in the manufacturing process of silicon which is very reliable and low in cost. In addition to processing advantages, design of silicon devices has gone through decades of optimization allowing the best performance of the material to be extracted. However it is becoming increasingly challenging to improve the performance of silicon devices and the cost of advancements has increased dramatically.

To that effect there is very much a case of looking at alternative semiconductors with better intrinsic physical properties for use in power electronics applications. In this pursuit of new materials emphasis has been given to wide bandgap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN). These materials can theoretically offer significant improvements in the areas of specific on-resistance, blocking voltage, operation at increased temperatures and switching both in terms of losses and switching frequency. A comparison of some of the most important properties of the candidate materials which can affect performance are given in Table 1.1 which has been reproduced from [18].

Table 1.1 Material properties of wide bandgap semiconductors compared to Silicon

Parameter	Silicon	4H - SiC	GaN	Diamond
W_g, eV	1.12	3.26	3.39	5.47
E_{crit}, MV/cm	0.23	2.2	3.3	5.6
ϵ_r	11.8	9.7	9.0	5.7
μ_n, cm^2/Vs	1400	950	800/1700[b]	1800
BFoM[a] relative to Si	1	500	1300/2700[b]	9000
n_i, cm^{-3}	$1 * 10^{10}$	$8 * 10^{-9}$	$2 * 10^{-10}$	$1 * 10^{-20}$
λ	1.5	3.8	1.3/3[c]	20

[a]Baliga's figure of merit for the power devices: $\epsilon_r * \mu_n * E_{crit}^3$
[b]Significant difference between the bulk and the 2DEG
[c]Difference between the epitaxial layers and the bulk material

A wider bandgap is desirable as it theoretically allows for a higher breakdown voltage per unit length of device (breakdown field, E_{crit}). As can be seen in Table 1.1 the performance of GaN and 4H-SiC[1] exceed the performance of silicon by an

[1]The prefix 4H- refers to a specific polymorph of SiC used for comparison purposes. Other polymorphs exist which are suitable for the development of power devices e.g. 6H-SiC, 3C-SiC. These may have different bandgap, mobility, saturation velocity etc. due to their different crystal structure.

order of magnitude in that respect. A wide bandgap also allows lower intrinsic carrier concentration which can affect off-state leakage. The possibility of shorter devices for the same blocking voltage as well as increased carrier mobility (μ_n) can allow a lower on-resistance to be achieved. Furthermore, high mobility and high saturation velocity allow higher switching frequencies to be achieved and therefore a reduction in the size and weight of magnetic components used in power electronic modules. The theoretically superior nature of wide bandgap materials such as SiC and GaN to silicon is seen when calculating figures of merit used to compare the suitability of materials for power device applications.

It can be seen in Table 1.1 that using the Baliga figure of merit (BFOM) introduced earlier, GaN has a distinctive advantage over other materials, other than diamond. One area in which GaN is not as competitive is that of thermal conductivity (λ).

Other than intrinsic advantages of the material there are numerous other factors which need to be considered before a commercial power device can be produced. Issues such as ease of doping, mass production capability, wafer quality, ease of processing techniques, number of masks required and production costs in general need to be taken into account. These factors provide significant challenges in utilizing new materials. That is why diamond, despite its exceptional properties, is still at very early stages of development due to difficulties in mass production, doping (in particular n-doping) and cost. SiC devices also deal with certain technology issues. For example, SiC MOSFETs have traditionally suffered from poor oxide semiconductor interface quality, which has led to large threshold voltage instability. Furthermore, use of normally-on SiC JFETs and SiC BJTs requires the design of more challenging gate driving [20].

GaN is considered a very promising material as it has several advantages over other wide bandgap semiconductors in the aspects just mentioned. One major advantage is that high quality GaN layers can be grown epitaxially on several substrates, the most significant of which being silicon. This can be done using standard silicon production lines and hetero-epitaxy on upto 8-inch wafers has been demonstrated already. On the other hand, SiC devices can only be produced on SiC substrates which are costly to produce and are only made up to 6-inch wafers, leaving SiC only able to satisfy sections of the market which require top performance at a price. Table 1.2 reproduced from [18] clearly illustrates the point discussed with GaN-on-Si costing 1/100th of the price of GaN on SiC. This thesis will thus consider the development of lateral rather than vertical GaN devices. The main drawback of a vertical device would be cost, as even though vertical GaN rectifiers with very good properties have been reported in

literature [21][22], the cost of such devices makes them unrealistic in a commercial environment due to the need of a bulk GaN wafer [18].

Table 1.2 Implications of the usual substrate materials for the GaN epitaxy

Substrate	Bulk GaN	SiC	Sapphire	Silicon
Lattice mismatch	none	+3.5%	-16%	-17%
Thermal mismatch	none	+33%	-25%	+116%
Electrical resistance	low	low[a]	∞	very low[a]
Thermal resistance	same	0.3x[a]	3x	0.9x
Available wafer size	2"(3")	4"(6")	up to 8"	any
Cost, Euro/cm^2	100	10	1	0.1

[a]Only non-conductive interfaces yet

A second major advantage of GaN is that it allows the formation of hetero-structures through the use of aluminium. The formation of a heterostructure comprising of a layer of GaN and a layer of AlGaN allows a two dimensional electron gas layer to be formed close to the interface of the heterojunction; this is referred to as a 2DEG. This is a region of high carrier concentration as well as high mobility due to no additional doping being necessary for the formation of the 2DEG. The use of the 2DEG as a channel can result in low on-state resistance and fast switching. The physics behind this are explained in more detail in Chapter 2.

Given the intrinsic and practical advantages of GaN for use in power devices the motivation for research in the development of GaN-based power switches and rectifiers becomes apparent. Nonetheless, while GaN devices appear to be promising due to the advantages discussed above it is worth considering for which breakdown voltage capabilities, current capabilities and frequencies of operation these advantages will best be exploited. In this respect it is again worth considering the trade-off between on-state resistance and breakdown voltage capability. The discussion earlier considered vertical MOSFET devices however the relationship given by equation 1.2 does not apply to lateral devices or superjunction devices. Therefore, the relationship does not apply to the lateral AlGaN/GaN heterojunction devices that are discussed in this thesis. It has indeed been derived that the relationship between R_{on} and BV for high voltage lateral FETs is:

$$R_{on} = BV^2/q\mu_n n_s {\xi_c}^2 \tag{1.2}$$

where n_s is the electron sheet charge density at the channel of the device. Note that this equation assumes a uniform electric field distribution at the surface of the drift region and thus presents an ideal case. A plot showing the relationship between specific R_{on} and BV for the different technologies is shown in Fig. 1.2 [23]. It is important to note the slope of the line for the different materials/technologies. The plot illustrates the intrinsic advantage that wide bandgap semiconductors have over Silicon devices in an ideal device. Nonetheless, it is observed that as breakdown voltage rating rises, the improvement in performance which can be achieved by using WBG materials over the Silicon SJ is reduced, with possible improvements which can be achieved being more stark at lower voltages. It is worth stating that, while this is a useful indicator, it relies on theory and thus does not take into consideration a variety of challenges which can be presented for the different technologies when attempting to increase the breakdown capability. The figure illustrates some state of the art devices for each technology to give a better comparison of where the performance of each technology currently lies. Finally, it is important to note that performance is not the only measure when considering a device for a given application with cost often being a prohibiting factor an example of which being why SiC FET devices have had a hard time displacing their Silicon counterparts.

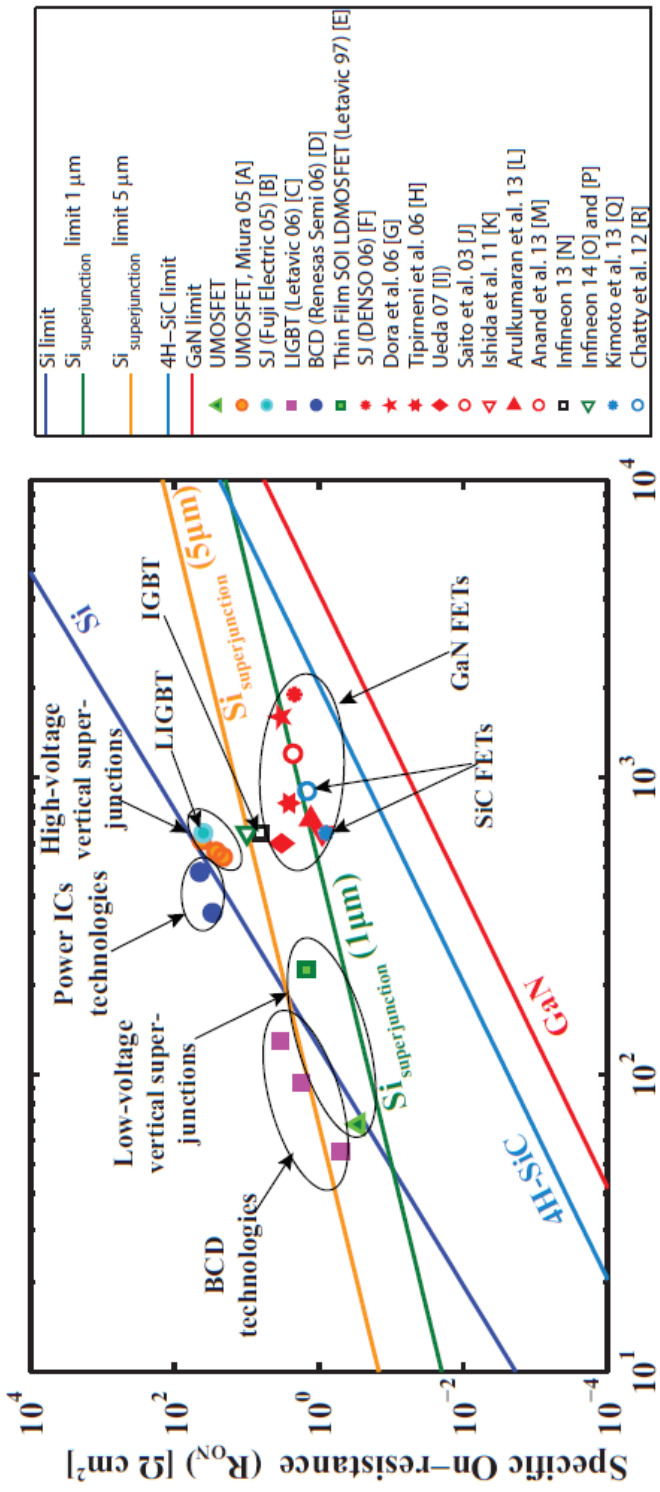


Fig. 1.2 R_{on} vs breakdown: Comparison of intrinsic and demonstrated performance of different technologies. [23]

1.4 Applications of GaN power devices

Taking into consideration the comparison between GaN and its competitors, a clearer picture appears of applications in which new GaN devices can displace the technologies which currently dominate the market. A number of devices have made an appearance in the market in recent years. A summary of the available devices is illustrated in Fig. 1.3 [24].

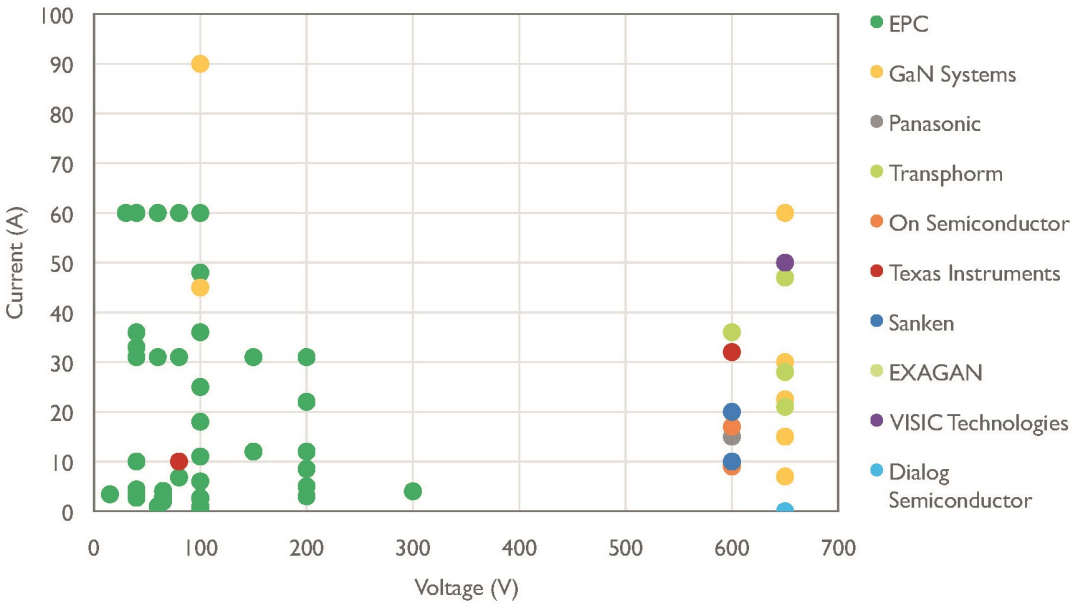


Fig. 1.3 Commercially available GaN devices

The majority of devices target the 100-200V voltage range and the 600-650V range. In terms of current capabilities the majority of devices are available for currents below 60A. The lower voltage capability devices would be suitable for point-of-load applications i.e. low voltage DC-DC converters for IT or consumer electronics applications. Large market potential however exists at the 600V range for applications such as power factor correction (PFC), uninterrupted power supplies (UPS), motor drives, and photovoltaic (PV) system inverters. 600V GaN devices can also find use as chargers in hybrid electric vehicles (HEV) and electric vehicles (EV), a market which is growing at an enormous pace. Future development of devices with breakdown capabilities up to 1.2kV and power ratings which can reach 7.2kW can lead to GaN devices being used in EV and HEV converters where the high frequency of operation will allow a reduction in system size, a parameter which is significant when considering mobile systems. Ultimately, if the power rating is extended enough GaN devices could find application in wind turbines (1.7kV) and rail traction systems (1.7kV-6.5kV). Nonetheless, this

would be a hard market to penetrate with 60kW + systems being more suited to the use of the latest generation of Si IGBTs and even SiC MOSFETs.

Regarding applications for GaN-based Schottky diodes the starting point for market penetration would be 600-650V devices targeted for use in server and telecommunications switch mode power supplies (SMPS), PC power and lighting applications, as well as solar inverters and UPS systems. GaN Shottky diodes face a challenging market to compete in, considering the performance of the latest generation of SiC Schottky diodes which achieve very low on-state and switching losses. The advantage of GaN-based devices could be price and the ability to be included in power integrated circuits monolithically with GaN HEMTs. A more thorough comparison of AlGaN/GaN Schottky diodes against SiC Schottky diodes will be given in Chapter 4.

A report by *Yole developpment* [25] makes a prediction about the time to market of the GaN technologies and the compound annual growth rate (CAGR) that might be observed. These predictions are illustrated in Fig. 1.4. The CAGR is the mean annual growth rate of an investment over a specified period of time longer than one year. The time-line extends to 2024 and suggests a very encouraging picture with growth in large segments of the power electronics industry, especially in the mid-voltage range.

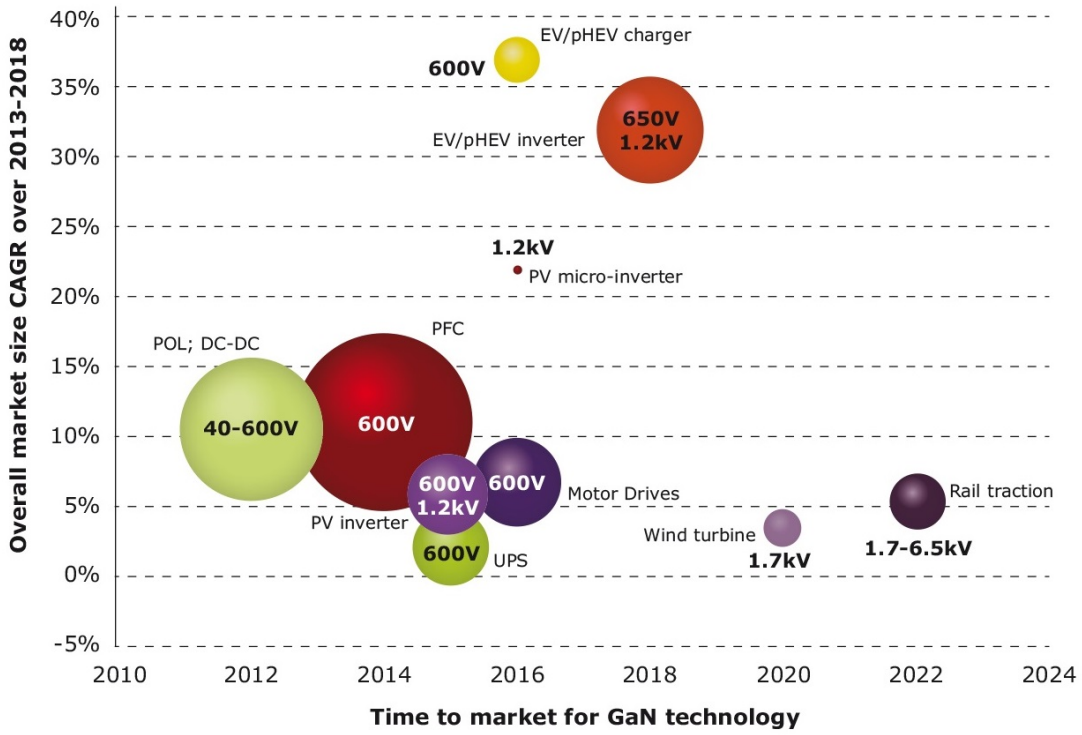


Fig. 1.4 Estimated accessible markets, growth rate and time-to-market for main GaN applications

1.5 Overview of the thesis

This thesis will deal with a variety of topics concerning the design and optimization of AlGaN/GaN HEMTs and Schottky diodes with a 650V rating. Discussion will span several topics from device cross-section physics to circuit implementation and will be based on both experimental results and advanced modelling.

- In Chapter 2, the physics of the AlGaN/GaN heterojunction will be presented in more detail. Furthermore, the state of the art in AlGaN/GaN HEMTs and diodes will be presented and a discussion of the challenges that these devices face will also be discussed.

- In Chapter 3, an overview of the simulation tools used in this thesis will be given with the discussion focusing mostly on important considerations when setting up TCAD simulations of GaN-based devices.

- Chapter 4 will describe a method to extract the ideality factor, barrier height and series resistance of a lateral AlGaN/GaN heterostructure power Schottky diode using a simple I-V measurement in on-state and sub-threshold domains. An analytical model previously developed for Gallium Arsenide (GaAs) and Silicon vertical diodes [26] is applied to lateral AlGaN/GaN Schottky diodes and calibrated using extensive experimental results both at room and increased temperature.

- Chapter 5 will discuss the development of a TCAD model for a lateral AlGaN/GaN Schottky diode and offer an in depth investigation of the operation of such a device during switching. A comparison of the switching capability of the GaN-based diode with its main competitors (SiC Schottky diode, Si fast recovery diode) will then be given both experimentally and supported by simulations.

- Chapter 6 will discuss the development of the TCAD model of a p-gate enhancement mode HEMT. Through the variation of some of the gate parameters an improved understanding of the operation of the p-gate will be achieved offering the ability to optimize the design of these devices.

- Chapter 7 will discuss the switching of GaN HEMTs and the concerns that arise due to their fast switching capability. These are revealed to be both circuit and device layout related.

- Chapter 8 will offer a critical view of bonding pad over active area layouts for use in GaN HEMT devices compared with conventional layouts for both on-state and off-state performance, switching capability and reliability concerns.
- Chapter 9 will summarize and provide some conclusions for the work done as well as provide a discussion on the possible continuation of this work.

Several fabricated devices will be discussed in this thesis. It is important to note that these devices were provided by the commercial partner involved in this project, Vishay Intertechnology Inc., an American manufacturer of discrete semiconductors and passive electronic components. The devices described have not necessarily been fabricated or processed by Vishay and at times have been produced on its behalf at commercial foundry partners. Some activities in this project are subject to a non-disclosure agreement and as such certain information (e.g. precise device cross-section dimensions) will not be disclosed in this thesis. A range of reasonable values will be given where possible to aid understanding.

Chapter 2

GaN device physics and state of the art

This chapter deals with the device physics of GaN devices starting with a short discussion of the wafer processing challenges faced in the development of GaN-on-Si devices. This will be followed by a discussion of the AlGaN/GaN heterojunction to achieve a better understanding of the mechanisms which lead to the formation of the two dimensional electron gas that gives these devices their unique properties. Furthermore, a review of the state of the art AlGaN/GaN HEMTs and Schottky diodes will be given to provide some insight into the challenges and trade-offs faced when attempting to improve their performance.

2.1 Wafer processing

Epitaxial layers of GaN are most commonly grown on a silicon substrate using metal-organic chemical vapour deposition (MOCVD). MOCVD is a method used to produce single or polycrystalline thin films. It is a highly complex process for growing crystalline layers to create semiconductor multilayer structures. In contrast to molecular beam epitaxy (MBE) the growth of crystals is by chemical reaction and not physical deposition. This takes place not in a vacuum, but from the gas phase at moderate pressures. A discussion of the technical and commercial considerations associated with the two methods can be found in [27].

A typical GaN-on-Si wafer can be seen in Fig. 2.1. GaN-on-Si is far from a straightforward process and the production of high quality, crack-free GaN layers on silicon substrates is faced with many challenges [28]. These arise from the large lattice mismatch between Si and GaN which causes a large number of dislocations to appear

in the GaN channel layer. To mitigate this problem a transition layer is used before the deposition of the GaN channel layer as seen in Fig 2.1.

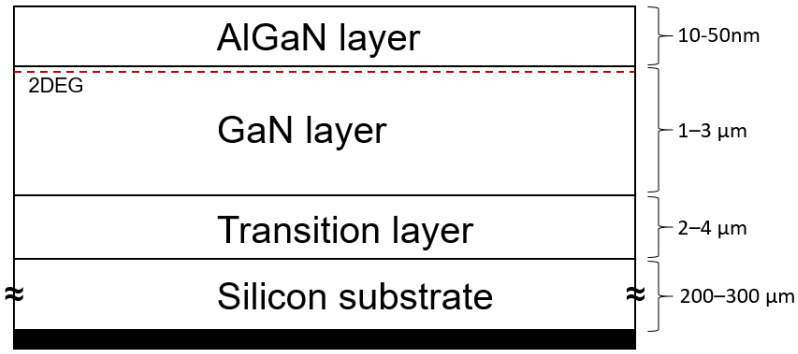


Fig. 2.1 Typical structure with several GaN-based layers grown on a Silicon substrate

The transition layer often consists of either a single layer of AlN/AlGaN [29] or a superlattice structure composed of several GaN/AlGaN/AlN layers [30] [31] . The quality of the epitaxial layers is of great importance as it affects bulk leakage in the off-state and the severity of current degradation mechanisms. Another major obstacle in obtaining high quality wafers is the difference in the thermal expansion coefficients of Si and GaN which causes stresses to develop during processing and film cracking to occur. It has been suggested that to effectively compensate for the tensile stress induced into the sample during cooling down, it is better to build up sufficient compressive stresses in the nitride heterostructures at the growth temperatures [32]. Other than material quality the doping of the GaN layer is of great importance. Carbon doping in the range of $10^{16} - 10^{17}$ is often included during growth. This has been demonstrated to enhance reverse blocking capability and to suppress the vertical leakage current [33]. Nonetheless, Carbon which has a complex set of acceptor trap levels in the lower half of the bandgap [34], has also been linked with current-collapse [35][36].

2.2 Physical properties of the AlGaN/GaN heterojunction

A heterojunction is defined as the interface that occurs between two layers of dissimilar crystalline semiconductors. These semiconducting materials have unequal band gaps. To be able to obtain a heterostructure without compromising the quality of the crystalline structure of the two layers, the lattice constants of the two materials must be close to each other. The lattice constant of GaN and AlN is very similar as can be

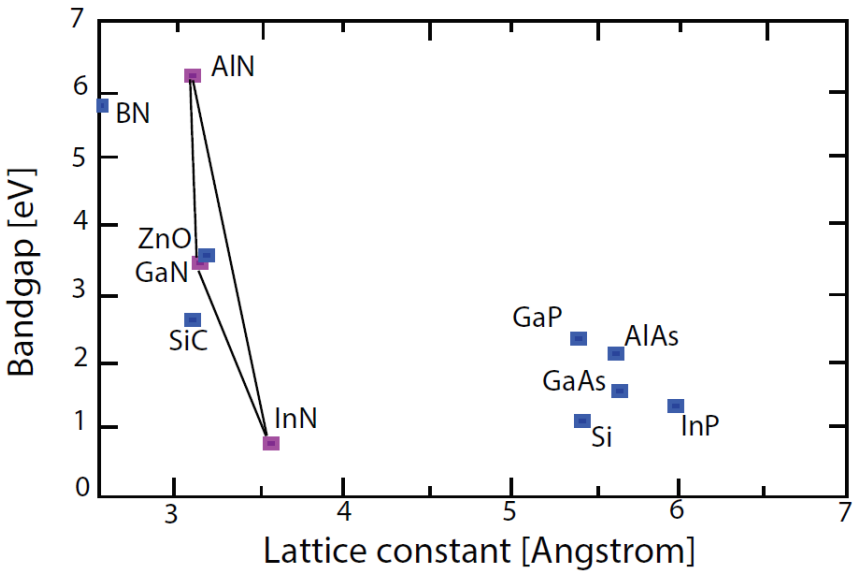


Fig. 2.2 Bandgap vs Lattice constant for different semiconductors [37]

seen in Fig. 2.2. Incorporating an aluminium mole fraction, x (between x=0 and x=1) in the GaN layer leads to the formation of Al_xGaN_{x-1} with electrical and mechanical properties between those of GaN and AlN.

The difference in the band gaps of the two materials leads to band discontinuity when the two layers are brought together and this band discontinuity leads to the formation of a quantum well. The 2DEG layer is formed at the interface between the GaN channel layer and AlGaN barrier. A thorough study on the formation of the 2DEG layer was given in a highly cited paper by Ambacher et al. [38] which focuses on the electrical and structural characterization of AlGaN/GaN/AlGaN heterostructures grown by MOCVD. The study describes, in detail, other contributing factors which lead to the formation of the 2DEG other than the band discontinuity at the interface. The confinement of a high concentration of electrons at the interface to create the 2DEG can be explained further by the compensation of a positive polarization induced sheet charge. This sheet charge is caused by different spontaneous and piezoelectric polarizations of the GaN layer and the AlGaN layer. Gallium Nitride can exist in three different crystal structures: Wurtzite, Zinc blende, and Rock salt. At room temperature the most stable structure for GaN and AlN is Wurzite and is the one most commonly used. Wurzite crystalline structure exhibits spontaneous polarization. Based on its aluminium content, the AlGaN layer has a greater spontaneous polarisation P_{sp} than GaN. Additionally, both GaN and AlN are piezoelectric materials. The piezoelectric effect is the ability of certain materials to generate an electric charge in response to

applied mechanical stress. AlN and therefore AlGaN has a smaller lattice constant than GaN therefore if AlGaN is grown on a relaxed GaN layer a piezoelectric polarisation charge (P_{pe}) is also formed due to the strain in the AlGaN layer. These charges form a net positive charge at the AlGaN/GaN interface which is compensated by a large concentration of electrons which forms the 2DEG. A schematic illustration of these polarization charges along with the resulting hetero-junction band diagram is shown in Fig. 2.3. Note that the polarisation induced sheet charge densities and directions of the spontaneous and piezoelectric polarisations are dependent on the crystal structure so Fig. 2.3 applies to the Wurzite structure.

The density of the positive polarization charge at the AlGaN/GaN interface is in excess of $10^{13} cm^{-2}$ in a strained $Al_{0.3}GaN_{0.7}$/relaxed GaN system [38]. Thus, a large concentration of carriers can be present in the 2DEG channel without any additional doping. This leads to very limited scattering in the channel and allows very high mobility values to be reached. As described, the aluminium mole fraction is an important parameter in the device as it affects the size of the polarization charge at the interface and thus the number of carriers in the 2DEG channel.

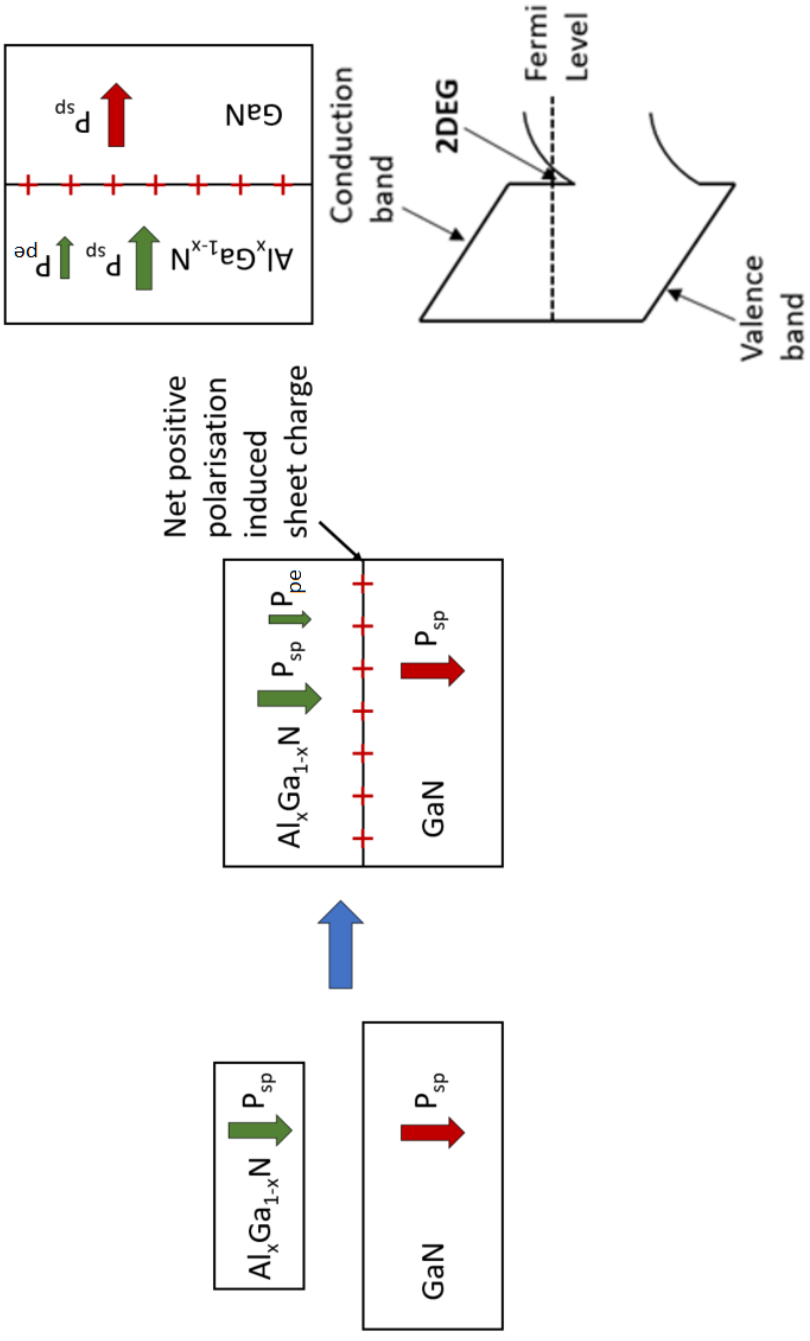


Fig. 2.3 Polarization charges in GaN channel/AlGaN barrier and formation of the 2DEG

2.3 Typical AlGaN/GaN Schottky diode structure

The typical structure of a lateral AlGaN/GaN Schottky diode will be presented as well as a brief overview of the operation of such a device. Figure 2.4 shows a typical lateral AlGaN/GaN Schottky diode. The device consists of a Silicon substrate and GaN-based epitaxial layers mentioned in section 2.1 as well as three terminals; the anode, cathode and substrate. The cathode and substrate terminals are Ohmic contacts and the anode is a Schottky contact.

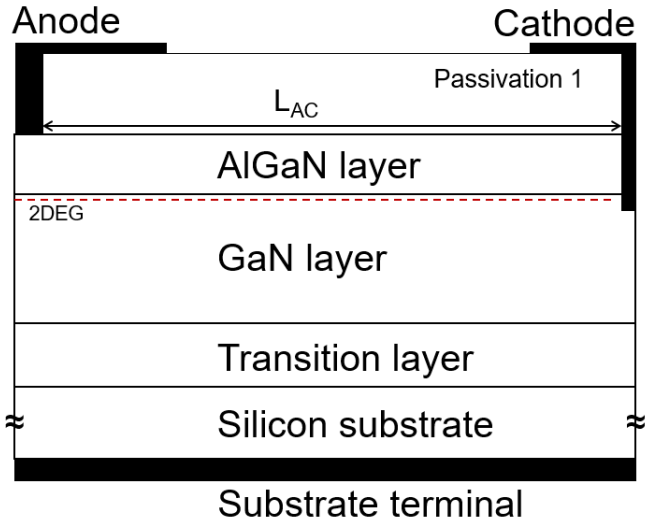


Fig. 2.4 Typical lateral AlGaN/GaN Schottky diode structure

The rectifying characteristics of the device come from the anode Schottky contact. Depending on the metal used for the contact, a potential barrier forms which blocks current flow from cathode to anode when the device is reverse biased. When a forward bias voltage is applied current flows from the anode though the 2DEG to the cathode. It is important that the threshold voltage is low to limit on-state losses. A popular design characteristic with lateral topology GaN SBDs is the use of a recessed anode [39][40][41] as seen in Fig. 2.5.

In this structure, the anode Schottky contact is made directly to the 2DEG by etching through the AlGaN barrier before depositing the contact. This causes a decrease in the turn-on voltage of the device thus limiting on-state losses but can lead to higher leakage in the off-state. Tunnelling at the Schottky contact which is dependent on the magnitude and spatial distribution of the electric field peak at the edge of the anode contact [42] is one of the major concerns. An example of such a recessed anode device is reported in [39] with an onset voltage as low as 0.43V and a

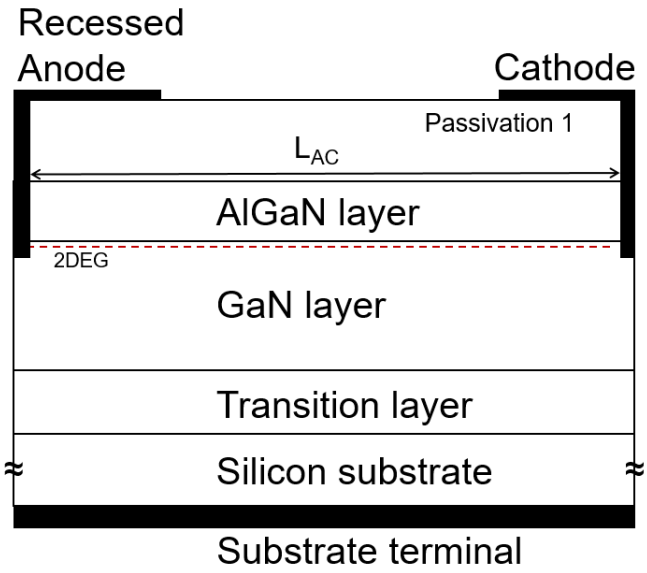


Fig. 2.5 Typical lateral AlGaN/GaN recessed Schottky diode structure

reverse blocking capability greater than 1000V. Nonetheless, the leakage observed is considerable despite the use of carbon doping in the GaN layer to suppress it. One of the most important arguments for the development of GaN heterostructure diodes is their unipolar nature which can allow negligible reverse recovery to be achieved during switching compared to the bipolar Silicon PIN diodes. Chapter 5 will focus on specific issues concerning the operation of AlGaN/GaN Schottky diodes including their switching capability through the development of a TCAD model of a test device and experimental comparison to other state of the art technologies. A brief overview of several other aspects which concern the design of lateral AlGaN/GaN diodes (field plate design, passivation, bulk leakage, current collapse) which are also encountered in HEMTs will be discussed in the next section.

2.4 AlGaN/GaN High Electron mobility transistor

The cross-section of a basic GaN HEMT device can be seen in Fig. 2.6. The structure is similar to the diode with the additional gate terminal to modulate the 2DEG thus moving from a three terminal device to a four terminal device. On-state conduction between the source and the drain occurs through the 2DEG formed at the AlGaN/GaN interface. The source and drain terminals are Ohmic and electrically connected to the 2DEG. In this first example of a AlGaN/GaN HEMT device the gate terminal is a Schottky contact placed directly onto the AlGaN layer. As the 2DEG inherently

exists at the AlGaN/GaN interface the device shown is normally-on. By negatively biasing the gate of the device below a certain voltage the 2DEG beneath the gate is depleted and the device is in the off-state. If the gate is positively biased above the bias required to turn on the Schottky diode then current will flow between the gate terminal and the source terminal. The transfer and output characteristic of a basic HEMT device can be seen in Fig. 2.7 [23]. When the high voltage terminal (drain) is biased with the device in the off-state the potential is supported in the drift region of the device between the gate and the drain.

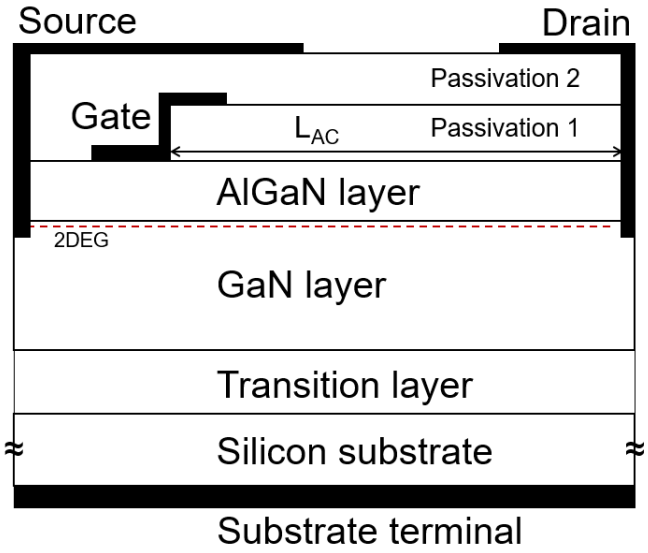
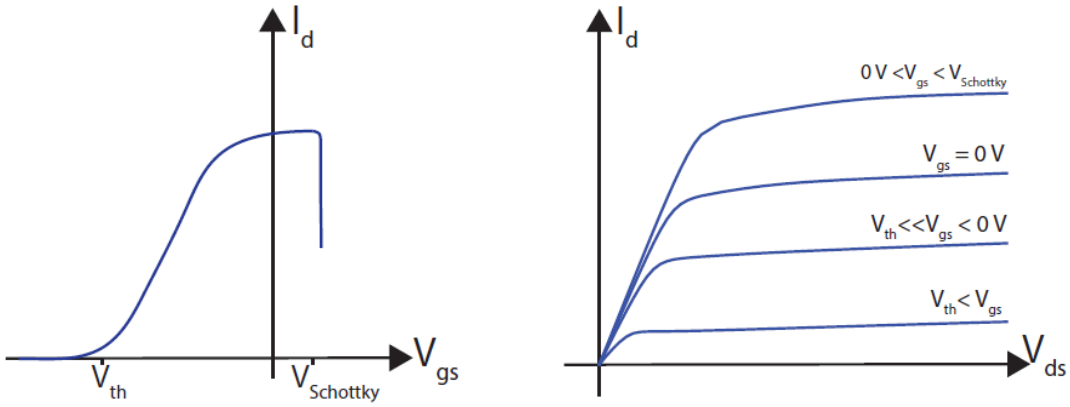


Fig. 2.6 Typical lateral AlGaN/GaN HEMT transistor structure

2.4.1 Enhancement mode HEMT

Since the two dimensional electron gas (2DEG) inherently exists at the AlGaN/GaN hetero-interface this creates a challenge when attempting the design of normally-off rather than normally-on devices. Nonetheless, as normally-off transistors are preferable in most power electronic applications, several methods have been proposed which can lead to enhancement mode devices. Some of the most important techniques used are as follows:

- The use of a metal insulator semiconductor structure [43] through the placement of a passivation layer under the gate which extends down to the AlGaN/GaN heterostructure as can be seen in Fig. 2.8. The channel is cut off below the gate at zero bias however when a sufficient positive bias is applied to the gate



(a) Transfer Characteristic (b) Output Characteristics

Fig. 2.7 Typical lateral AlGaN/GaN depletion mode HEMT characteristics

an electron channel is formed under the passivation layer. As the GaN layer is typically p-doped the electron channel formed can be considered similar to the inversion channel obtained in classical MOS structures. The main issues with this approach are the considerable levels of undesirable fixed charges and traps present at the semiconductor/passivation interface.

- The use of a recessed gate structure [44] as can be seen in Fig. 2.9. As described earlier the density of carriers in the 2DEG is dependent on the thickness of the AlGaN layer. Furthermore, if the thickness of the AlGaN layer beneath the gate is sufficiently reduced by etching the depletion region extending from the Schottky gate can reach the 2DEG channel. A combination of these two factors can lead to a normally-off device. The threshold of the device is dependent on the extent to which the AlGaN is etched. One major disadvantage is that etching leaves a rough surface where trap related phenomena can occur. Furthermore, the etching process needs to be controlled very carefully as a variation of a few nm can affect the threshold voltage significantly and lead to instability across the wafer.

- The use of fluorine treatment first described in [45] as can be seen in Fig. 2.10. By introducing negatively charged fluorine ions beneath the gate the positive charge at the AlGaN/GaN hetero-interface is compensated which leads to a lower concentration of electrons in the 2DEG. The main concern with this technique is that a threshold voltage instability is observed [46].

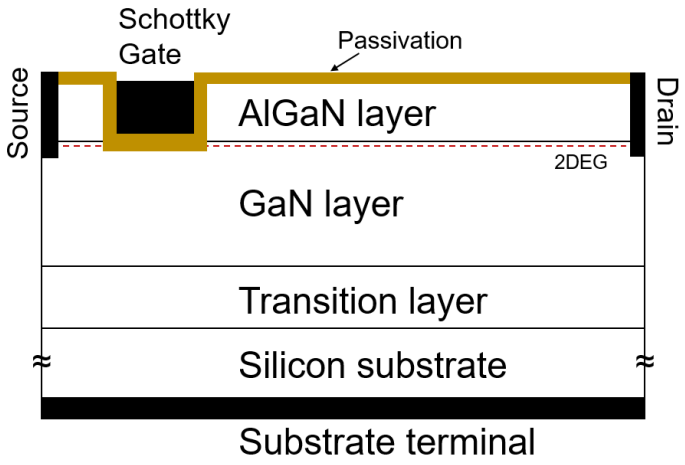


Fig. 2.8 Typical lateral AlGaN/GaN enhancement mode MISHEMT

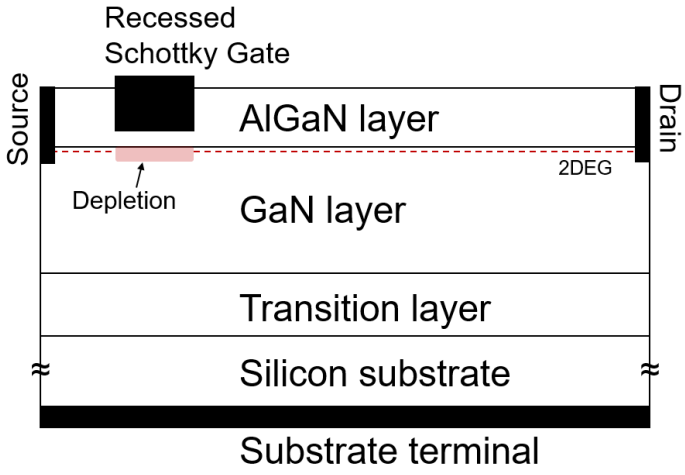


Fig. 2.9 Typical lateral AlGaN/GaN enhancement mode HEMT using recessed Schottky gate

- The introduction of a p-type cap layer beneath the gate terminal[47][48][49] as can be seen in Fig. 2.11. The high concentration of p-doping causes the 2DEG to deplete beneath the gate by shifting the Fermi level towards the valence band at the AlGaN/GaN interface. A thorough analysis of the operation of the p-gate shall be given in Chapter 6.

Due to the relative maturity and controllability in the epitaxial growth of p-GaN layers compared to the other techniques, p-GaN/AlGaN/GaN HEMTs are considered the leading structure for commercialization. While several publications exist on different aspects of the performance of GaN devices (breakdown, buffer leakage, current collapse) [50][51] there is less focus on the role that gate design parameters have in determining

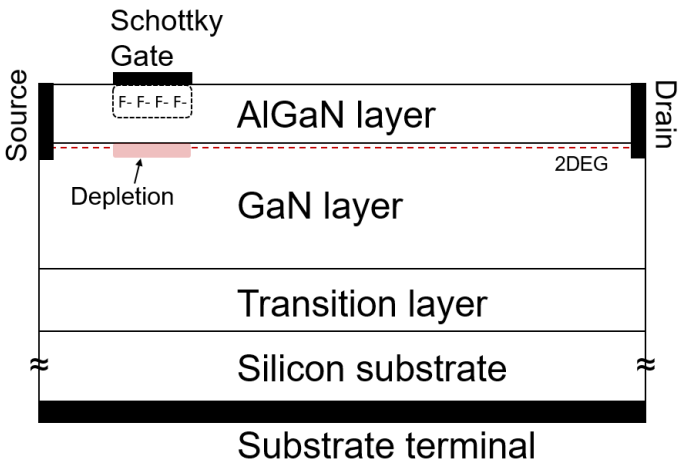


Fig. 2.10 Typical lateral AlGaN/GaN enhancement mode HEMT using fluorine treatment

the on-state characteristics (threshold voltage, trans-conductance and gate turn-on current) of p-GaN devices. These parameters are of great interest as problems such as unwanted device turn-on when the device is supposed to be off may occur in operation if the threshold voltage is low. Secondly, gate turn-on may be a problem due to the non-insulated gate structure. Furthermore, several studies have reported that the gate structure can play an important role in the reliability of p-GaN HEMTs due to the high electric field that is developed in the region under forward bias stress. The high electric field can lead to the generation of defects in the p-GaN [52] which can subsequently increase the leakage current via a defect percolation process and ultimately lead to device failure [53][54][55]. An understanding of what affects parameters such as threshold voltage, trans-conductance, gate leakage and gate turn-on current is therefore paramount to achieving a good design. This will be discussed extensively in Chapter 6.

2.5 Brief discussion of issues related to GaN-based devices

This section will give a brief overview of some of the main issues faced by GaN SBDs and GaN HEMTs. Note that the Schottky gate contact in HEMTs can be considered as the equivalent of the anode in SBDs and the drain contact can be considered as the cathode when drawing analogies between the two.

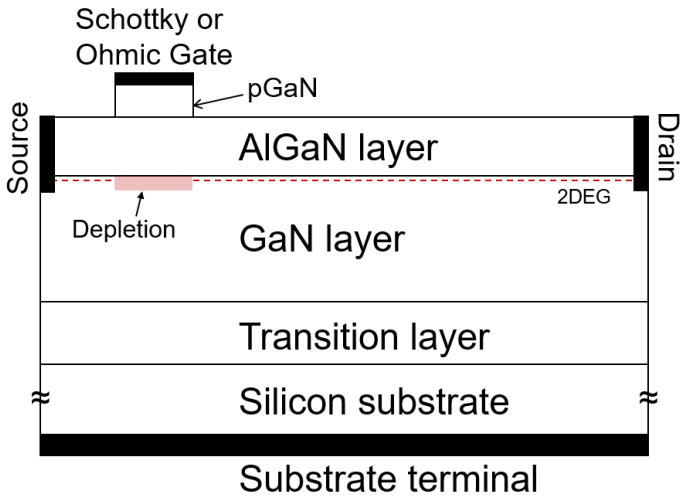


Fig. 2.11 Typical lateral AlGaN/GaN enhancement mode HEMT using p-GaN gate

2.5.1 Off-state leakage and breakdown

Several leakage/breakdown mechanisms during high off-state bias have been reported in GaN-based devices. In the case of the Schottky diode tunnelling at the Schottky contact is a major concern. Another mechanism identified is a leakage path from cathode to Si/buffer layer interface and then the anode (or the source contact in HEMTs [56]). Furthermore, bulk current from the Ohmic contact to the substrate contact is a major concern and can occur through various mechanisms which are dominant at different bias conditions such as a resistive mechanism (at low bias) and Poole-Frenkel trap assisted tunnelling (at high bias) [56]. Impact ionization coefficients for GaN have been evaluated in the pre-breakdown regime of HEMTs with small gate to drain separation [57]. However, avalanche breakdown due to impact ionization is often dismissed as a possible breakdown mechanism with the argument that the maximum electric field present in GaN devices is present in either the passivation or AlGaN barrier. Therefore dielectric breakdown of the overlying insulating layers is suggested as a possible mechanism [58]. Furthermore, the lifetime of these devices may be limited due to time dependent dielectric breakdown [58][59].

Several groups have reported an increase in the breakdown voltage of HEMTs with an increase in gate to drain separation that could be attributed to the breakdown mechanisms just mentioned. However, this only occurred until a bias voltage was reached where buffer layer breakdown became critical [60][61]. Buffer layer breakdown might be associated with epi-related defects across the wafer [62]. An illustration of the most important mechanisms described in this section can be seen in Fig. 2.12.

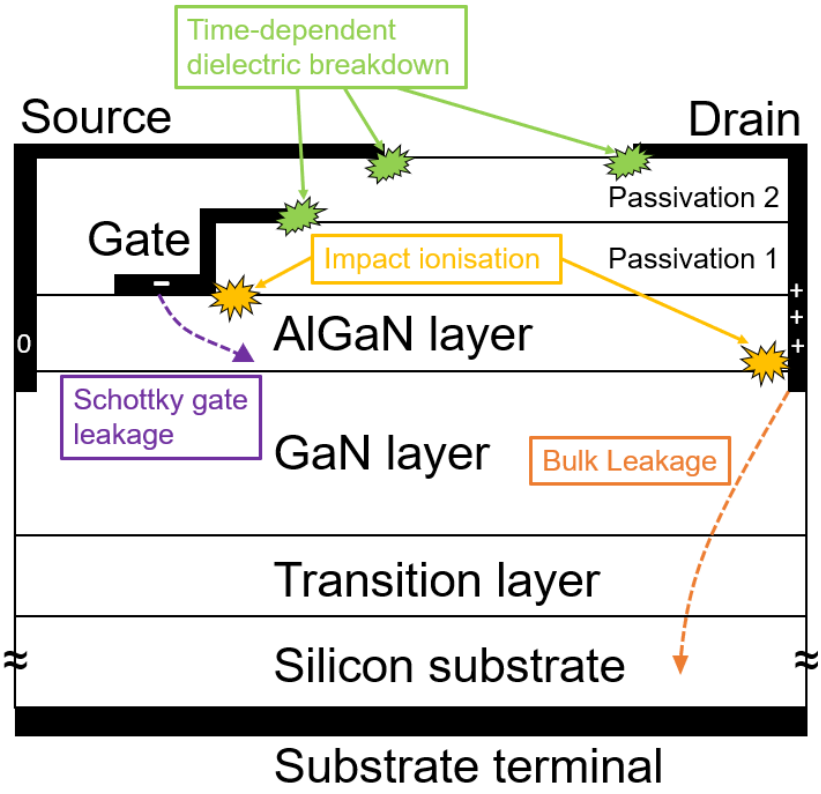


Fig. 2.12 Common off-state leakage and breakdown mechanisms associated with AlGaN/GaN HEMTs and Schottky diodes

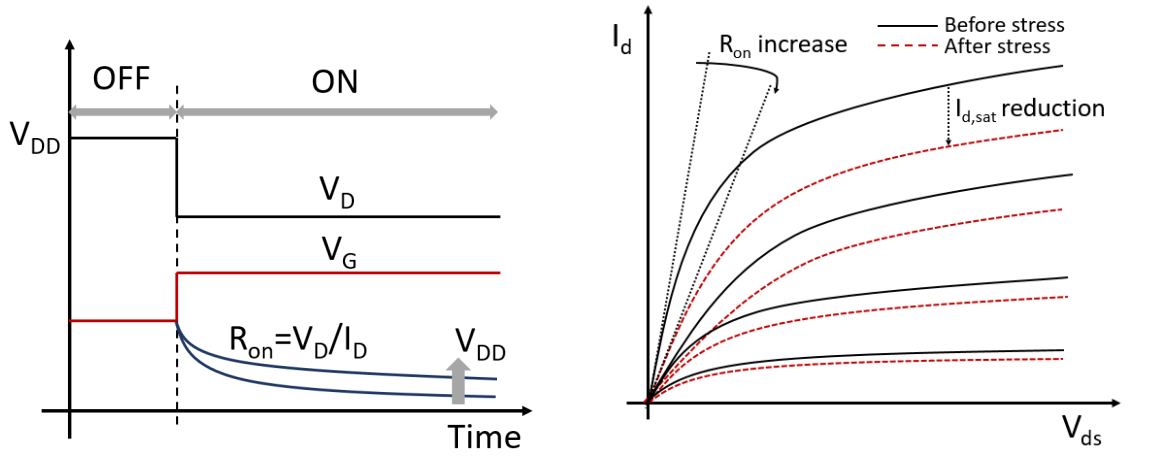
2.5.2 Current Degradation

Another major concern associated with GaN devices is that of current collapse[1] (or dynamic R_{on}) which is an increase in the on-resistance of the device when the device is switching at high frequencies. A test to quantify the change in on-state resistance that may be observed in GaN devices is illustrated in Fig. 2.13. A high voltage off-state bias is applied to the device (V_{DD}) followed by an immediate on-state characterization where the R_{on} is recorded. The technique is described in more detail in [63]. It is often found that a higher off-state bias can lead to a greater increase in on-state resistance. An illustration of the changes in the output characteristic of a device after it has been subjected to off-state stress can be seen in Fig. 2.13. The current collapse mechanism is represented as an increase in the on-state resistance R_{on} and a reduction in the drain saturation current $I_{d,sat}$.

Current collapse can be associated with traps located either at the surface [64] or in the bulk [65]. In both cases electrons trapped in trap states during off-state

[1]The name "current collapse" is no longer appropriate but it is still commonly used.

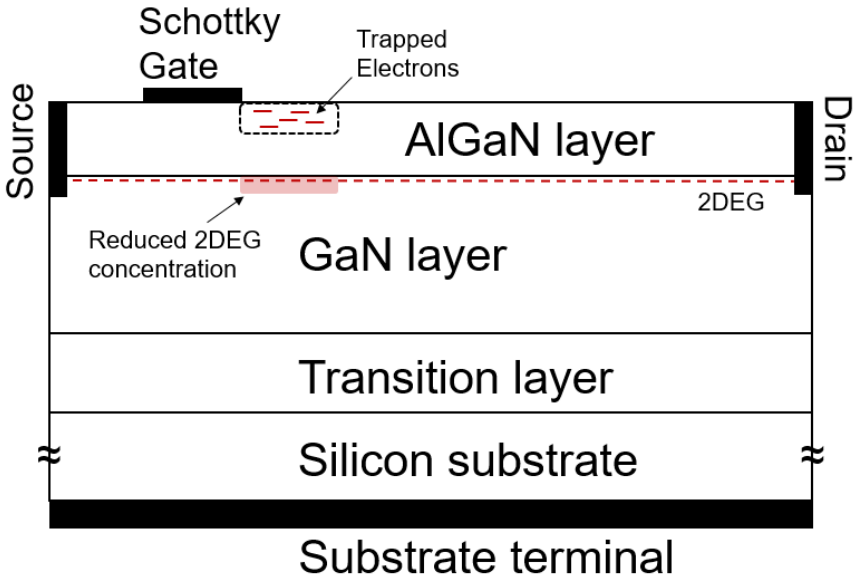
cause a depletion in the 2DEG when the device is turned-on as seen in Fig. 2.14. Normal on-resistance is resumed if the device is left in the on-state long enough for these electrons to de-trap. Current collapse is a problem that may be permanently amplified when the device is under stress conditions for a long period of time. Reliability concerns such as these have been widely reported in literature. Alamo et al. [66] relates increased current collapse as well as observed increases in leakage of GaN HEMTs to the formation of crystallographic defects at areas where a high electric field is present in the device. The formation of these defects is attributed to the presence of large stresses due to the inverse piezoelectric effect. This theory was verified by images of these defects obtained using scanning electron microscopy by Li et al. [67]. Other mechanisms for the creation of traps under reverse bias stress conditions have also been suggested such as hot electron degradation [68] and impurity diffusion [69] processes driven by high electric field and leakage currents.



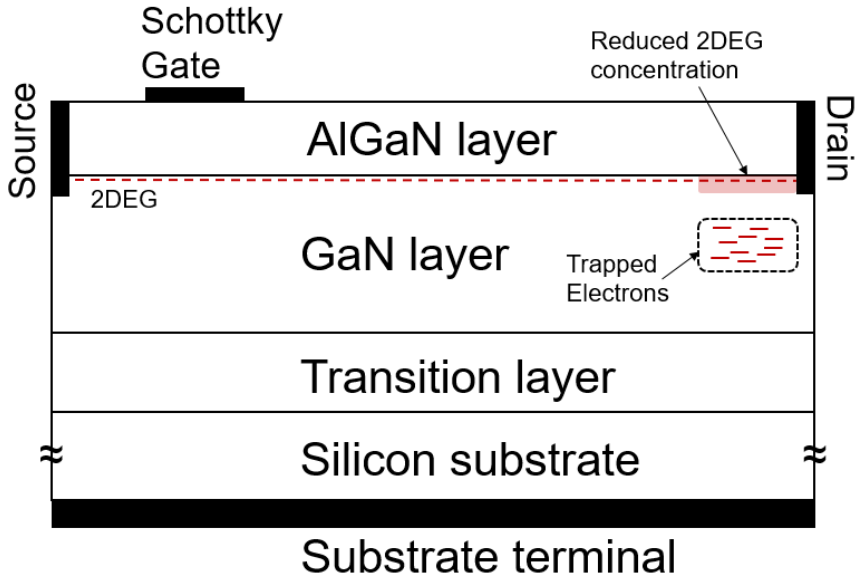
(a) Current collapse test

(b) Output characteristic before and immediately after high-voltage stress

Fig. 2.13 Current collapse or Dynamic R_{on} phenomenon



(a) Virtual Gate phenomenon



(b) Trapping in the bulk region

Fig. 2.14 Trapping mechanisms responsible for current collapse

2.5.3 Passivation

The most common passivation material used in GaN-based devices is Silicon Nitride (Si_3N_4). Other passivation materials such as Silicon dioxide (SiO_2) [70] or Hafnium dioxide (HfO_2)[71] have also been investigated in literature. A combination of stacked passivation layers may also be used with several layers of passivation often needed to allow the design of field plate structures. A good passivation layer is important as current collapse arising due to surface trapping centers has been reported in literature [64].

2.5.4 Field plate design

The use of field plates in lateral GaN/AlGaN devices is of great importance. Their optimal design is very important to mitigate leakage and early breakdown. Electric field peaks in the semiconductor section of the device are commonly reported at the gate/anode edge and drain edge [72] of the structure. A field plate design should take into consideration the gate-drain separation and the channel electron concentration as this determines the depletion of the 2DEG and thus the location of the most critical points where a high electric field is encountered [73][74]. An analysis of the depletion of the 2DEG in AlGaN/GaN Schottky diodes will be given more extensively in Chapter 5. Several studies on field plate optimization can be found in literature [73] with some interesting techniques such as floating metal rings [75] and slanted field plates (see example in Fig. 2.15) [72]. Furthermore, it has been demonstrated that field plate design may affect the severity of current degradation in a device [76] [77] given that capture of carriers in trapping centres would be more prominent in regions with high electric field.

2.5.5 Cap layer

Another design feature that is reported in the literature is an additional GaN cap layer on the AlGaN barrier as can be seen in Fig. 2.15. This can have the effects of decreasing the reverse leakage through the Schottky contact, reducing the peak electric field, protecting the AlGaN barrier against processing and improving the reliability of the device [78][79]. Nonetheless, this may have a significant adverse effect on on-state conduction by reducing the 2DEG carrier concentration [79].

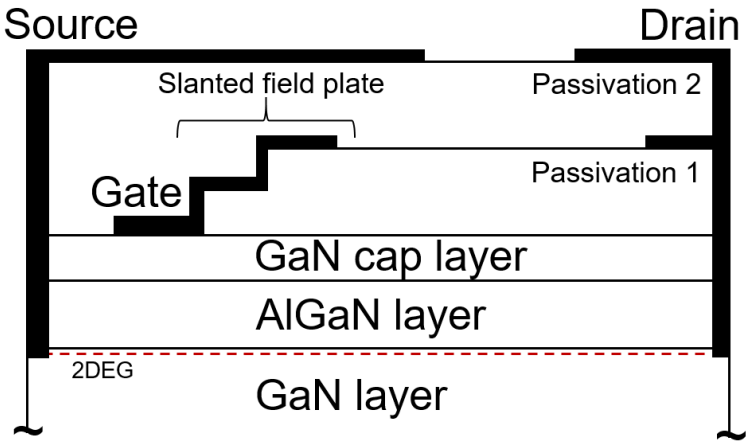


Fig. 2.15 Slanted field plate and GaN cap layer device example

2.6 Switching of GaN HEMTs and Schottky diodes

As mentioned, the higher breakdown field of a wide bandgap semiconductor allows for devices to be optimized with thinner drift regions, resulting in power devices with lower specific ON-resistance. The high mobility of GaN further reduces the ON-resistance. This allows a smaller die size to achieve a given current capability, and therefore lower input and output capacitances. Higher saturation velocity and lower capacitances enable faster switching transients. Operation at higher frequencies is desirable as it allows a reduction in the size of passive components and thus a reduction in overall system size. Fast switching however does not come without its challenges. In the case of GaN HEMTs this thesis will examine the source of some of the problems arising from fast switching (Chapter 7). Furthermore, in the case of GaN Schottky diodes, a comparison will be made between the turn-off performance of GaN Schottky diodes, SiC schottky diodes and Si fast recovery PIN diodes (Chapter 5). Both investigations were carried out in a clamped inductive switching configuration and involved both experimental characterisation and the use of simulation tools.

2.7 Device layout

As GaN-based devices moved closer to commercialisation at the start of this decade some of the research focus started shifting towards other considerations such as device layout and packaging. An example of an inter-digitated device layout can be seen in Fig. 2.16. With GaN devices looking to compete in the medium voltage range (600V - 1.2kV) a challenge develops as the breakdown voltage is extended. This

relates to the lateral configuration of GaN devices which is much less suited to higher voltage applications compared to vertical devices as more wafer area is used when the drift region is extended. Bonding Pad over active (BPOA) layouts have been suggested as a design feature that can improve current density in lateral AlGaN/GaN heterostructure devices and studies which show competitive on-state and off-state characteristics for such structures can be found in literature. Lee et al. [80] reports the use of a BPOA layout for an AlGaN/GaN power diode with excellent on-state and off-state characteristics while [81] reports the improvement of on-state current density by utilizing a BPOA structure for a normally-on HEMT device. [82] describes the use of a photosensitive poyimide (PSPI) dielectric layer instead of SiO_2 between the active semiconductor area and the bonding pad of a normally-off HEMT device; the study reports a reduction in the chip size by 50 per cent without an increase in leakage current compared to the conventional design and no issues with the packaging. In this thesis the on-state, off-state and switching performance of a fabricated BPOA layout normally-off HEMT device is presented to illustrate the relative advantages and disadvantages of this design when compared to a device with a conventional layout (see Chapter 8). Furthermore the fabrication of several other designs illustrated that device level parasitics arising from different layouts can have a significant influence on the switching capability of GaN HEMT devices. This shall be discussed in detail in Chapters 7 and 8.

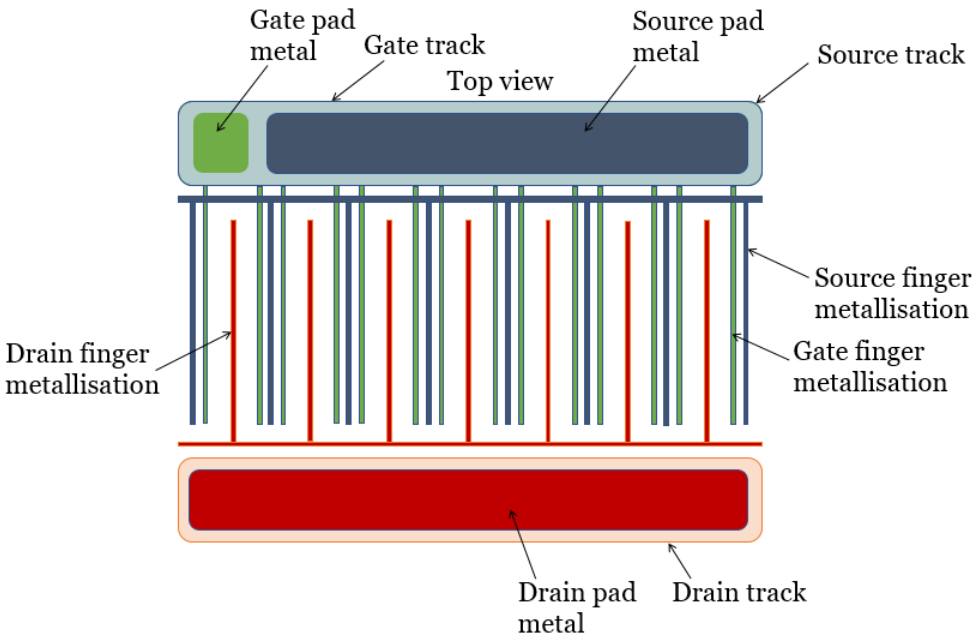


Fig. 2.16 Typical lateral AlGaN/GaN HEMT inter-digitated layout

Chapter 3

Simulation tools

This thesis employs simulation tools in several sections in order to support some of the experimental findings and offer a better understanding of the physical mechanisms underlying the operation of AlGaN/GaN HEMTs and Schottky diodes at both device and circuit level. Simulation tools are widely used in the semiconductor and power electronics industries as they provide valuable insight into the operation of devices and circuits and allow observing the effects that changing some critical parameters will have on performance in a much shorter time scale than that which is required when fabricating and testing real devices. The main software packages used in this thesis have been Sentaurus TCAD, a finite element software by Synopsis for device level simulations (Chapters 5, 6, 8) and LTSpice for circuit level simulations (Chapter 7). Furthermore, Sentaurus allows circuit level simulations i.e. mixed mode simulations, using a device TCAD model. Mixed mode deals with one or more devices, plus extra components such as resistors, voltage sources etc., modelled by Spice. These simulations provide a more accurate picture of the device behaviour during switching however a trade-off exists as they are much slower and take longer to set up than Spice simulations. Mixed mode simulations were employed for an analysis of the AlGaN/GaN Schottky diode switching as will be described in Chapter 5.

3.1 Sentaurus TCAD

Finite elements models have been used in the design of silicon power devices for decades. Sentaurus TCAD is a physically based simulator that predicts the electrical characteristics that are associated with specified physical structure and bias conditions. This is done by solving systems of coupled, non-linear partial differential equations that describe the semiconductor physics. Simulation set-up requires the input of the physical

structure and material parameters to be simulated, the physical models to be used and the bias conditions for which electrical characteristics are to be simulated. With the increasing interest in GaN based devices simulation packages such as Synopsis Sentaurus have updated their platform to allow the use of these tools for GaN device design. GaN-based heterojunction devices add complexity to achieving accurate simulations compared to Silicon. This is due to [83]:

- Piezo-polarization effects that are main contributors to the device performance.
- Wide bandgaps and therefore much lower intrinsic carrier concentrations.
- Abrupt interfaces between semiconductor materials (hetero-interfaces) and partially floating regions.
- Increased importance of traps and their properties.

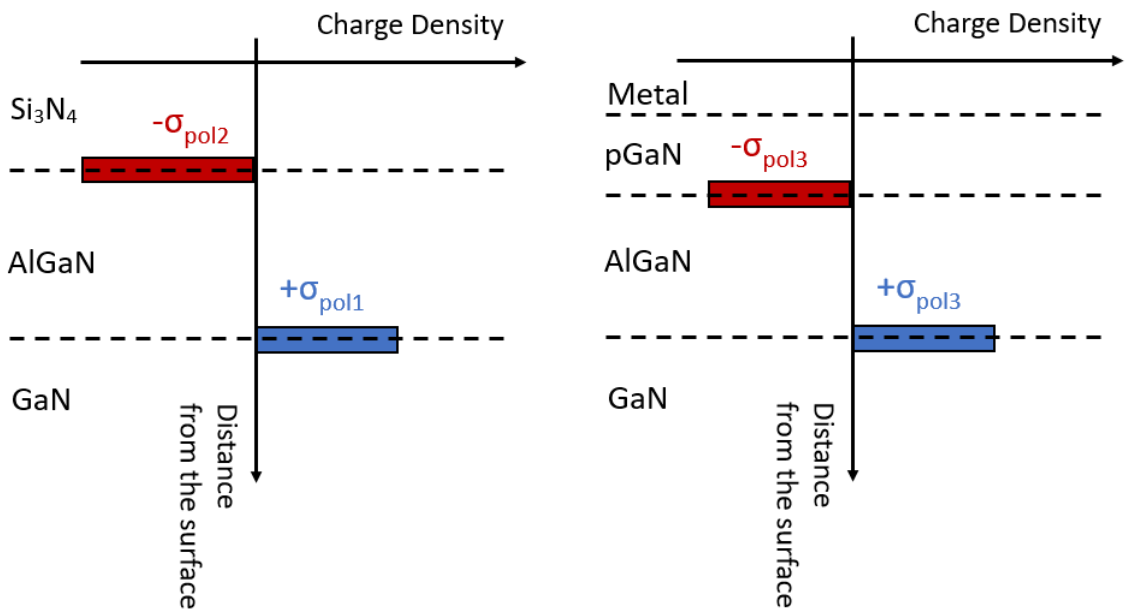
Nonetheless, TCAD simulations are a very important tool in the understanding and design of GaN-based devices. In this section, focus will be given to some of the most critical material parameters and physical models used in the TCAD simulations.

3.1.1 Spontaneous and Polarization Effects

As discussed in Chapter 2, the spontaneous and piezo-polarization charges in AlGaN/GaN heterojunction devices have a great effect on the characteristics of these devices. It is therefore important to include the necessary charges at the interface of the model developed. The interface charges can be calculated as outlined in [38] and are included as fixed charges at the relevant interfaces. In this thesis two different TCAD models have been produced to simulate the operation of a GaN-based Schottky diode and a GaN-based HEMT (see Chapters 5 and 6 respectively). Different combinations of semiconductor/passivation/metal stacks are present in these two devices and a schematic illustrating the location and polarity of the theoretically predicted charges in these different configurations can be seen in Fig. 3.1.

3.1.2 Traps

The inclusion of surface and bulk traps is often required in order to accurately model transient effects in the behaviour of AlGaN/GaN devices. The simulator allows the specified traps to be spatially placed at interfaces (in this case their concentration is expressed as sheet charge density in cm^{-2}) or distributed in a specific region or



(a) Si_3N_4/AlGaN/GaN present in the Schottky diode and HEMT drift region

(b) Metal/GaN/AlGaN/GaN present at the E-mode HEMT gate region

Fig. 3.1 Location and polarity of the theoretically predicted interface charges for different structures

material of the device structure (in this case their concentration is expressed as volume charge density in cm^{-3}). There are two possible types of traps:

- Donors: uncharged when de-ionised (filled with electrons) and positively charged when ionised.
- Acceptors: uncharged when de-ionised (filled with holes) and negatively charged when ionised.

Sentaurus TCAD allows for several possibilities of specifying the energetic distribution of traps within the bandgap. In this thesis, single-level traps have been used where needed. More details on the use of traps in the different TCAD models produced will be given in Chapters 5, 6.

3.1.3 Fermi - Dirac statistics

In all semiconductor devices, mobile charges (electrons and holes) and immobile charges (interface charges, ionized dopants or traps) play a central role. The charges determine the electrostatic potential and, in turn, are themselves affected by the electrostatic potential. Therefore, each electrical device simulation must, at the very least, compute

the electrostatic potential. When all contacts of a device are biased to the same voltage, the device is in equilibrium, and the electron and hole densities are described by a constant quasi-Fermi potential. Therefore, together with the electrostatic potential, the relation between the quasi-Fermi potentials and the electron and hole densities forms the basis of any unbiased solution. Electron and hole densities can be computed from the electron and hole quasi-Fermi potentials, and vice versa. Boltzmann statistics are often used to calculate the electron and hole concentration however this is an approximation which applies best if the energy of the states is much higher than the Fermi level. Nonetheless, physically more correct, Fermi (also called Fermi - Dirac) statistics model was used in the TCAD simulations described in this study. Fermi statistics becomes important for high values of carrier densities, for example, $n > 1 * 10^{19} cm^3$ and is suggested for simulation of heterostructure devices [84].

3.1.4 Contacts

Sentaurus TCAD allows the specification of contacts as Ohmic or Schottky. The metal work function when an electrode is defined as Schottky can be further specified. The simulator calculates the electrode charge differently depending on whether the contact is made on an insulator or semiconductor. For an electrode that contacts an insulator region only, the charge is computed from Gauss's law and represents the charge that would sit on the surface of a real contact to the device. For an electrode that contacts a semiconductor region, the charge is also computed from Gauss's law; however, the Gaussian surface used for the integration includes the doping well associated with the electrode. In this case, the electrode charge represents the charge that sits on the electrode plus the space charge in the doping well [84]. Lump or distributed contact resistance can also be added to the contacts as required.

3.1.5 Transport models

Several models exist to describe the transport of carriers in the device. This section will discuss the three most relevant to the simulations undertaken in this thesis. These are as follows:

- **Drift-Diffusion model**

  The drift-diffusion model is the default carrier transport model in Sentaurus. For the drift-diffusion model, the current densities for electrons and holes are given by [84]:

$$\vec{J_n} = \mu_n(n\nabla E_c - 1.5nkT\nabla ln(m_n)) - D_n(\nabla n - n\nabla ln\gamma_n) \tag{3.1}$$

$$\vec{J_p} = \mu_p(p\nabla E_v - 1.5pkT\nabla ln(m_p)) - D_p(\nabla p - p\nabla ln\gamma_p) \tag{3.2}$$

  where μ = carrier mobility (cm^2/Vs), n, p = electron, hole carrier density (cm^{-3}), k = Boltzmann constant (J/K), E_c, E_v = conduction, valence band energy level (J), T = temperature (K).

  Note that for Boltzmann statistics $\gamma_n = \gamma_p = 1$. Furthermore the diffusivities (D_n, D_p) are given through the mobilities by the Einstein relation, $D = kT\mu$.

  The first term takes into account the contribution due to the spatial variations of the electrostatic potential, the electron affinity, and the bandgap. The remaining terms take into account the contribution due to the gradient of concentration, and the spatial variation of the effective masses m_n and m_p.

- **Tunnelling model**

  Tunnelling refers to the quantum mechanical phenomenon where carriers can tunnel through a potential barrier that could not be surmounted according to classical theory. Sentaurus offers three tunneling models. The most versatile tunneling model is the non-local tunneling model and is the one used in this thesis because of its suitability when describing tunneling at Schottky contacts and tunneling in heterostructures [84] which are scenarios of interest as will be discussed in more detail in the chapters that follow. Tunnelling conduction mechanism at a simple Schottky junction is illustrated in Fig. 3.2. The tunnelling current density is expressed as the product of the carriers available to cross the barrier (n), the Richardson velocity (v^R) and the probability of tunnelling (Θ) according to the following equations [85].

$$J_n = ev^R n\Theta \tag{3.3}$$

$$\Theta = exp(\frac{-4\sqrt{2em_n^*}{\phi_b}^{3/2}}{3\hbar\xi}) \tag{3.4}$$

where ϕ_b is the barrier height, m_n^* is the effective electron mass and ξ is the electric field within the potential barrier.

- **Thermionic Emission model**

  Thermionic emission is the thermally induced flow of charge carriers from a surface or over a potential-energy barrier. This occurs because the thermal energy given to the carrier overcomes the work function of the material. An example of thermionic emission at a simple Schottky junction is shown in Fig. 3.2. The thermionic current density can be expressed as [85]:

$$J_n = ev^R N_c exp(e\Phi_b/kT)[exp(-eV_a/kT) - 1] \tag{3.5}$$

  where Φ_b is the barrier height and V_a is the external voltage applied to the barrier. The average velocity with which the electrons reach the barrier is named Richardson velocity (v^R) and is equal to $\sqrt{kT/2\pi m_n}$, with m_n is the electron mass.

3.1.6 Mobility models

The carrier mobility characterizes how quickly an electron (or hole) can move through a metal or semiconductor, when pulled by an electric field. In the presence of high electric fields there is a maximum velocity that carriers can attain and this is termed the saturation velocity. Mobility field dependence can be modelled in several ways in Sentaurus. The default option is the Extended Canali high field saturation model [86] which is described by the Eqn. 3.6 and is the model that is more commonly used in Silicon device simulations.

$$\mu = \frac{\mu_0}{[1 + (\frac{\mu_0 F}{v_{sat}})^{\beta}]^{1/\beta}} \tag{3.6}$$

where μ_0 = mobility at low fields, F = driving field, v_{sat} = electron saturation velocity

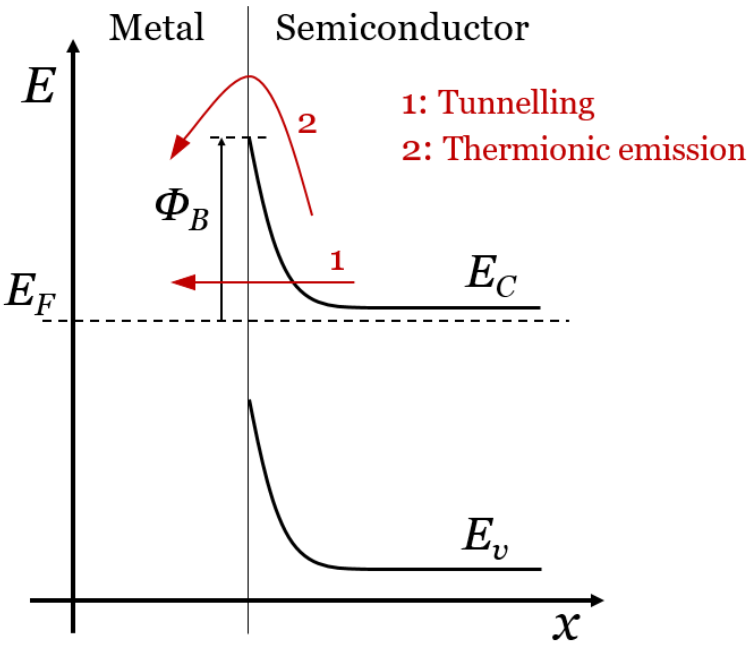


Fig. 3.2 Conduction mechanisms at a Schottky junction

Nonetheless, according to Monte Carlo calculations [87], GaN should exhibit velocity overshoot and therefore a negative differential mobility. Sentaurus TCAD provides a model specifically for III-nitride materials which can describe this effect [84]. This model is referred to as Transferred Electron Model 2 and was used in the HEMT TCAD model described in Chapter 6.

In the Schottky diode model described in Chapter 5, a simple mobility model with no field dependence, which only accounts for phonon scattering effects was used. This model is referred to as the constant mobility model [84]. In this model, mobility is only dependent on the lattice temperature which is a valid assumption given that the 2DEG channel is in a region of low doping and the electric fields present under on-state conditions are not too high in the operation of a Schottky diode. The equation which describes the constant mobility model is as follows:

$$\mu = \mu_L * (\frac{T}{300K})^{-\zeta} \tag{3.7}$$

where T is temperature in K, μ_L = mobility at room temperature and ζ = mobility exponent.

An illustrative plot of the carrier velocity relationship with electric field for the three models described above can be seen in Fig. 3.3.

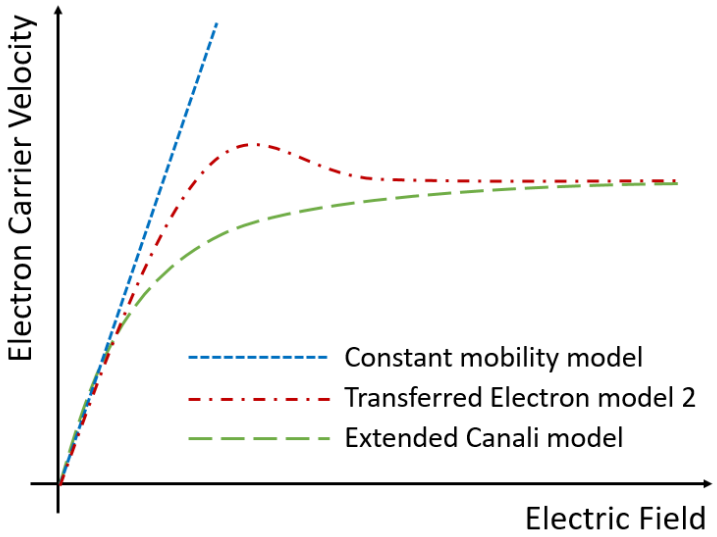


Fig. 3.3 Illustration of different velocity saturation models available in Sentaurus TCAD software

3.1.7 Mesh

A proper mesh definition is an important aspect in achieving reliable results in TCAD simulations. If the mesh is not sufficiently refined then the results may not be very reliable or convergence issues might arise. On the other hand, if the mesh is excessively refined the simulations may take a long time to complete. A balance is achieved by defining a very refined mesh at important points for example the hetero-junction, Schottky contacts and regions of high electric field while defining a coarser mesh at bulk regions. An example of the mesh definition in a TCAD model and the increased refinement at significant regions of the structure is shown in Fig. 3.4. The location shown is a magnification of the edge of the gate field plate.

3.2 LTspice

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator. It is a powerful program that is used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior. LTspice is a high performance SPICE simulator, schematic capture and waveform viewer.

The software was used to achieve a better understanding of the effect that circuit parasitics have on the switching of the GaN HEMTs. This was done by reproducing

the experimental switching board in LTspice. The set-up used is a clamped inductive switching circuit for double pulse measurement tests. A simple example of such a circuit can be seen in Fig. 3.5. More details will be given in Chapter 6.

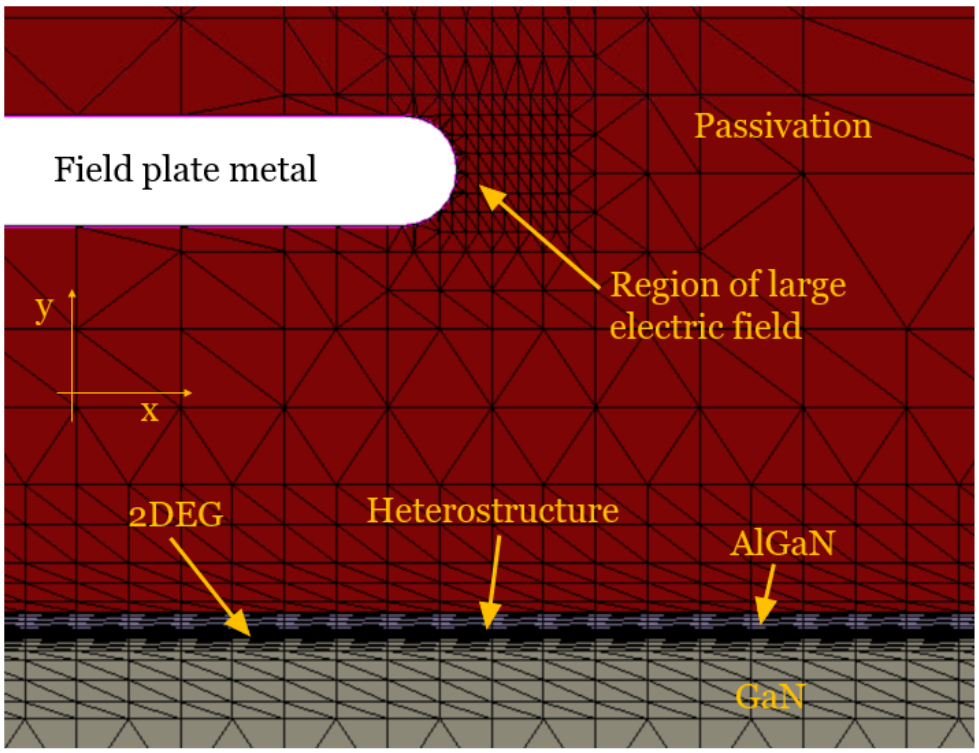


Fig. 3.4 Example of mesh definition in a TCAD model

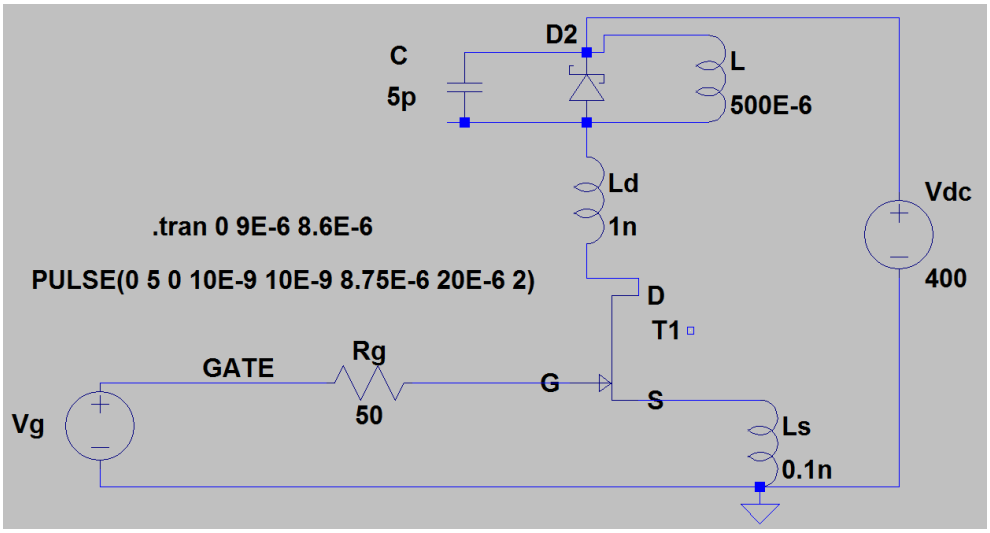


Fig. 3.5 Example of a simple clamped inductive switching circuit in LTspice

3.3 Mixed mode simulations

As mentioned earlier, Sentaurus allows circuit level simulations i.e. mixed mode simulations, using a device TCAD model. Mixed mode deals with one or more devices, plus extra components such as resistors, voltage sources etc., modelled by Spice. Rather than defining the circuit schematically as done in LTspice (see Fig. 3.5), the circuits are described using a simple circuit description language which is composed of components with terminals attached to particular nodes. These groups of components attached to nodes are called netlists, an example of which can be seen in Fig. 3.6. This example is equivalent to the circuit schematic seen in Fig. 3.5, however the IGBT and diode used in the circuit are defined as TCAD models. More details will be given in Chapter 5.

```
System {
        Inductor_pset l1 (1 2 ) {inductance=@l1@}
        Diode DUT  (anode=2 cathode=1 substrate=2)  {}
        Capacitor_pset  c1 (2 1) {capacitance=@cap@}
        Inductor_pset lc (2 3 ) {inductance=@lc@}
        Inductor_pset le (5 0 ) {inductance=@le@}

        IGBT switch (collector=3 gate1=4 gate2=4 emitter=5 ) {}


        Resistor_pset r_g (driver 4) {resistance=@Rg@ }

        Vsource_pset vg    (driver 0)   { pwl = (       0                                                                    0
                                                10E-9                                                                    15
                                              !(puts [expr {10E-9+gate_pulse_w}])!                                       15
                                              !(puts [expr {20E-9+gate_pulse_w}])!                                       0
                                              !(puts [expr {20E-9+gate_pulse_w+dead_time}])!                             0
                                              !(puts [expr {20E-9+gate_pulse_w+dead_time+10E-9}])!                       15
                                              !(puts [expr {20E-9+gate_pulse_w+dead_time+10E-9+gate_pulse_w}])!          15

                                              )
                                       }

   Set (0=0 , 1=0 )

     Plot "n@node@_circuit" (time()  v(driver 0) v(4 0) v(3 0) v(5 0) v(1 0) i(l1 2) i(DUT 1) v(1 2) v(3 5)  i(switch 5) i(c1 1))
}
```

Fig. 3.6 Example of a netlist defining a simple clamped inductive switching circuit for mixed mode simulations

Chapter 4

Modelling of an AlGaN/GaN Schottky diode and extraction of main parameters

This chapter describes a method to extract the ideality factor, barrier height and series resistance of a lateral AlGaN/GaN heterostructure power Schottky diode using a simple I-V measurement in on-state and sub-threshold domains. An analytical model previously developed for Gallium Arsenide (GaAs) and Silicon vertical diodes [26] is applied to lateral AlGaN/GaN Schottky diodes and calibrated using extensive experimental results. The validity of the model at increased temperatures (up to 428K) is also investigated and the dependence of the ideality factor and barrier height with temperature are obtained and assessed against those previously reported in the literature [88].

4.1 Introduction

As discussed in Chapter 2, GaN-based devices are faced with several issues where improved understanding can allow enhancements in performance. For example, significant attention has been focused on identifying and reducing the leakage current mechanisms in GaN-based Schottky diodes. This is crucial for the proper operation of the devices in the off-state and several works can be found in the literature that attempt to investigate the reverse bias leakage current mechanisms associated with metal/GaN Schottky contacts, with effects such as field emission tunneling [89][90] and dislocation related current paths being reported [91]. On the other hand, there seems to be limited

research into the on-state characterization of lateral AlGaN/GaN heterostructure Schottky diodes where interesting deviations from the thermionic equation have been observed [92]. In this work a method is outlined for the experimental extraction of the Schottky parameters (ideality factor, barrier height) of a lateral AlGaN/GaN Schottky diode as well as the series resistance present in the device. This technique is a variation of a method described in a paper by Cheung et al. [26] for GaAs and silicon vertical diodes which allows the extraction of ideality factor, barrier height and series resistance using a single on-state current-voltage measurement.

4.2 Device Structure and Methods

4.2.1 Device Structure

The device cross-section is shown in Fig. 4.1(a). Note the formation of the 2DEG at the AlGaN/GaN interface and the use of a GaN cap layer. The use of a GaN cap layer has an effect on the band diagram of the structure as can be seen in Fig. 4.1(b). The device fabricated had an inter-digitated layout as seen in Fig. 4.2. On-state I-V measurements were taken at a range of temperatures (298K - 428K) on three identical devices to verify the accuracy of the results presented. All the experimental measurements were taken at wafer level using a Keithley 2600 series source-measure unit.

4.2.2 Literature Background and methods for parameter extraction

The analytical equation [93] that describes the conduction at a conventional metal - semiconductor Schottky contact is as follows:

$$I = I_s[exp(\frac{qV_J}{\eta kT}) - 1] \tag{4.1}$$

where

$$I_s = A_{eff}A^*T^2exp(\frac{-q\Phi_{bn}}{kT}) \tag{4.2}$$

- Ideality factor, η
- Barrier height, Φ_{bn}

- Effective area of the junction, A_{eff}
- Richardson constant, A^*
- Voltage across junction, V_J

The objective of this study is to extract the ideality factor, η and barrier height, Φ_{bn} of the device shown in Fig. 4.1 using on - state characteristic I-V measurements and Eq. 4.1. The ideality factor is interesting as it reveals how close the on-state characteristic observed is to the ideal thermionic emission equation and how significant alternative conduction mechanisms such as tunnelling are. Knowledge of the barrier height is important as it determines the turn-on voltage of the device.

Several textbook methods exist that allow some or all of the parameters of interest to be extracted using on-state experimental results. The most significant methods are listed below:

- Method I: Current - Temperature plot [93], also known as Richardson plot. This requires measurements at several temperatures and allows extraction of the barrier height and Richardson constant. One limitation of this method is that, since the barrier height might be temperature dependent, the value extracted could not be the accurate one for the barrier height at a specific temperature.

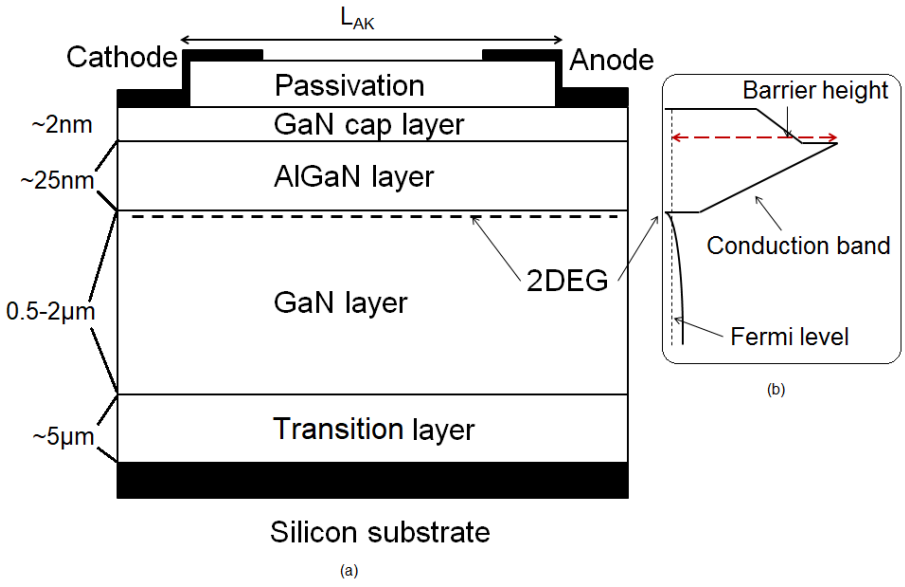


Fig. 4.1 Device structure (a) Cross section, (b) Band diagram schematic at the Schottky/GaN/AlGaN/GaN interface

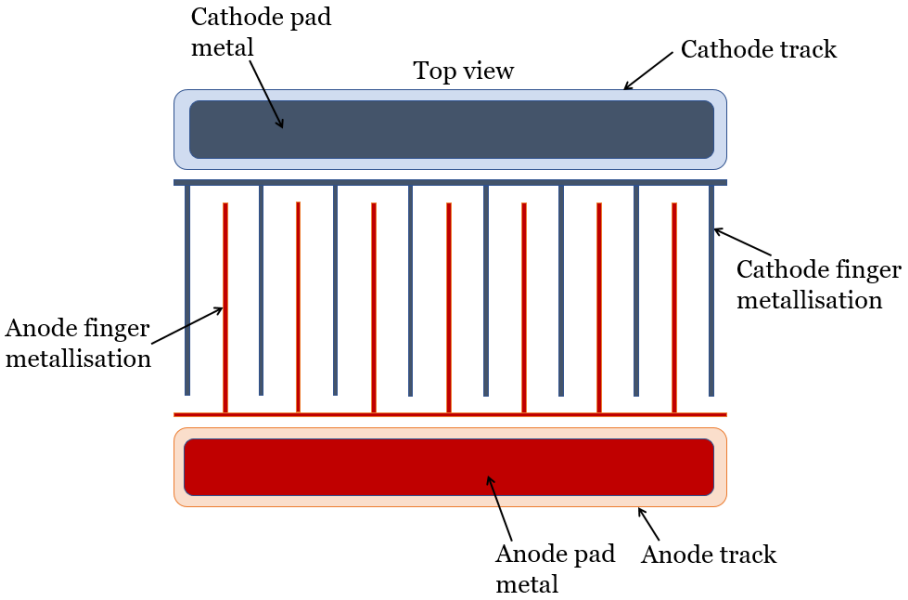


Fig. 4.2 AlGaN/GaN Schottky diode layout

- Method II: This is a technique described in a paper by Cheung et al. [26] which allows extraction of ideality factor, barrier height and series resistance from a single I-V measurement. While this technique allows the extraction of all the parameters of interest the exact method outlined in the paper cannot directly be applied to the device tested here or in fact any lateral device due to the fact that manipulated equations used to extract the relevant parameters work with the current density, J through the device. The difference in the lateral Schottky AlGaN/GaN device measured in this study is that the current flows through different areas when flowing through the Schottky contact and the 2DEG channel.

In this work the method is thus adjusted to work with current, I rather than current density, J as described in the next section.

4.2.3 Outline of extraction method used in this study

In power devices where a significant breakdown voltage rating is required (650V) an extended drift region is a necessity. The long drift region contributes heavily to the on-state resistance of the device. In a lateral AlGaN/GaN diode on–state conduction occurs through the 2DEG therefore the drift region resistance can be labeled as R_{2DEG}. Total diode series resistance is composed by the drift region resistance (R_{2DEG}) and the contact resistance (R_{con}) although the drift region resistance is expected to be far more significant. The voltage drop across the diode is that of the junction and the

series resistance. Therefore extracting this series resistance is also of interest. The analytical model given in Eq. 4.1 is adjusted to include this resistance (Eq. 4.4).

$$V_J = V - I(R_{con} + R_{2DEG}) \tag{4.3}$$

where V = Voltage drop across diode, V_J = Voltage drop across junction, R_{con} = Contact resistance and R_{2DEG} = 2DEG channel resistance.

For $V_J > \frac{3kT}{q}$,

$$I = I_s[exp(\frac{qV - I(R_{con} + R_{2DEG})}{\eta kT})] \tag{4.4}$$

The parameters in this new analytical model can be extracted as follows:
Rearranging and substituting $\beta = \frac{q}{kT}$,

$$V = (R_{con} + R_{2DEG})I + \eta\Phi_{bn} + \frac{\eta}{\beta}ln(\frac{I}{A_{eff}A^*T^2}) \tag{4.5}$$

Differentiate Eq. 4.5 with respect to (ln I):

$$\frac{dV}{d(lnI)} = (R_{con} + R_{2DEG})I + \frac{\eta}{\beta} \tag{4.6}$$

By plotting $dV/d(lnI)$ vs I the ideality factor is extracted by extrapolating the plot and finding the y-intercept. The total series resistance can be found by looking at the gradient of the plot.

Define the function, H(I):

$$H(I) = V - \frac{\eta}{\beta}ln(\frac{I}{A_{eff}A^*T^2}) \tag{4.7}$$

Rearranging Eq. 4.5 and substituting for the defined function gives:

$$H(I) = (R_{con} + R_{2DEG})I + \eta\Phi_{bn} \tag{4.8}$$

By plotting $H(I)$ vs I the barrier height can be extracted by extrapolating the plot and finding the y-intercept. A second value for the total series resistance can again be found by looking at the gradient of the plot.

Some interesting points to consider are:

- Effective area used is the Schottky contact area which in a finger structure diode as the one shown in Fig. 4.2, A_{eff} = Number of Schottky fingers x Length of finger x Width of finger.

Table 4.1 Extracted Schottky Parameters

Ideality factor, η	1.56
Resistance[Ω]	0.083
Schottky Barrier, $\Phi[eV]$	0.87

- Value of Richardson constant used in plotting equation 4.8 is the theoretical value of $2.6x10^5 Am^{-2}K^{-1}$ [94] calculated using the effective mass of electrons in GaN. Experimentally determined values have been found to deviate from this theoretical value [88].

- It is expected that plots of $dV/d(lnI)$ vs I and $H(I)$ vs I are linear allowing for an easy extraction of the Schottky parameters. This suggests that ideality factor, barrier height and resistance are independent of the bias voltage applied.

4.3 Results and Discussion

The method described in section II.C was followed using data from the on-state measurements taken from several fabricated devices with the structure shown in Fig. 4.1. The extracted parameters at room temperature can be found in Table I.

Figures 4.3 and 4.4 show a comparison between experimental results and the analytical model calibrated using the extracted parameters reported in Table I. It can be seen that a good match was achieved in both the high current end of the characteristic (Fig. 4.3) and in the sub-threshold region (Fig. 4.4). This illustrates that the method is very accurate in extracting the relevant parameters as well as the fact that the analytical model given by Eq. 4.4 describes the on-state behaviour of the tested device very well.

In order to validate the model the same measurements were performed at increased temperatures up to 428K. The parameters of interest were again extracted and used to plot the analytical model against the experimental results as seen in Figs. 4.5 and 4.6 (sub-threshold). It is observed once more that the analytical model calibrated using the parameters extracted can match the experimental measurements very accurately.

A variation in values of ideality factor and barrier height extracted is seen with temperature. This is plotted in Fig. 4.7. It is observed that the ideality factor comes closer to unity and barrier height increases at increased temperatures. Similar behaviour has been reported in literature and values from Adari et al. [88] are included in Fig. 4.7 for comparison purposes. The device tested in [88] was a lateral Co-nGaN

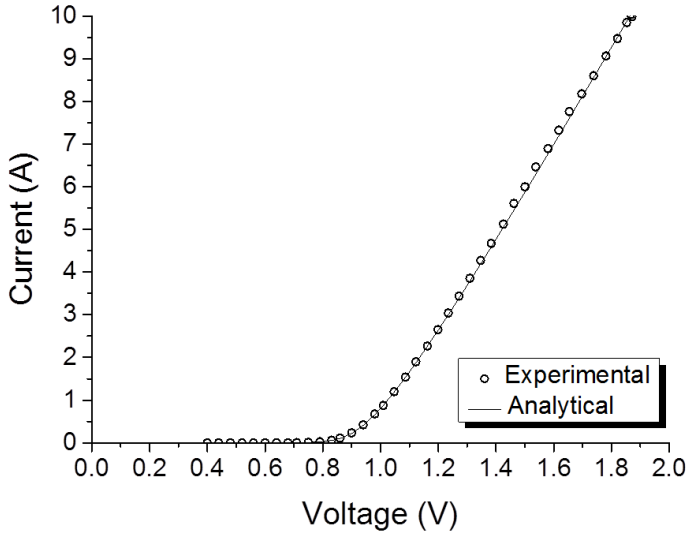


Fig. 4.3 Experimental and analytical on - state I-V characteristic for device shown in Fig. 4.1

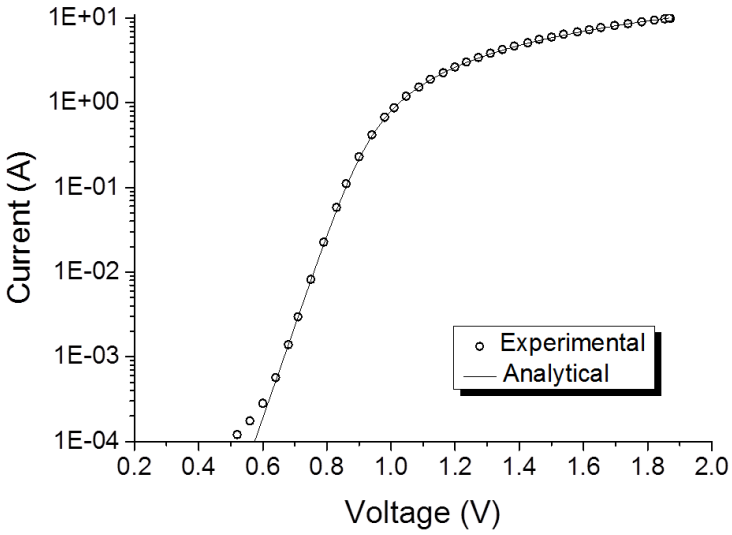


Fig. 4.4 Sub - threshold experimental and analytical on - state I-V characteristic for device shown in Fig. 4.1

Schottky diode device but not one that uses a heterojunction. While the barrier height values found are comparable, the ideality factor of the devices investigated in this study is closer to one. This could be attributed to the wider barrier (as seen in Fig. 4.1) between the Schottky contact and the 2DEG limiting any tunnelling effects.

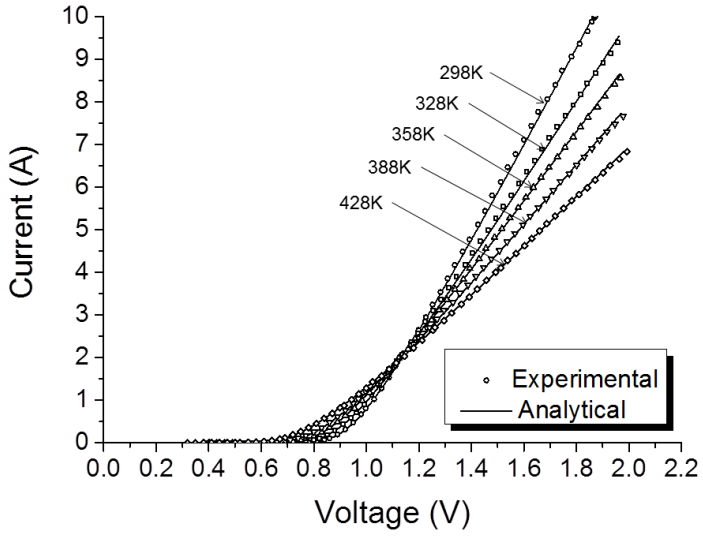


Fig. 4.5 Experimental and analytical on-state I-V characteristic for device shown in Fig. 4.1 at increased temperatures

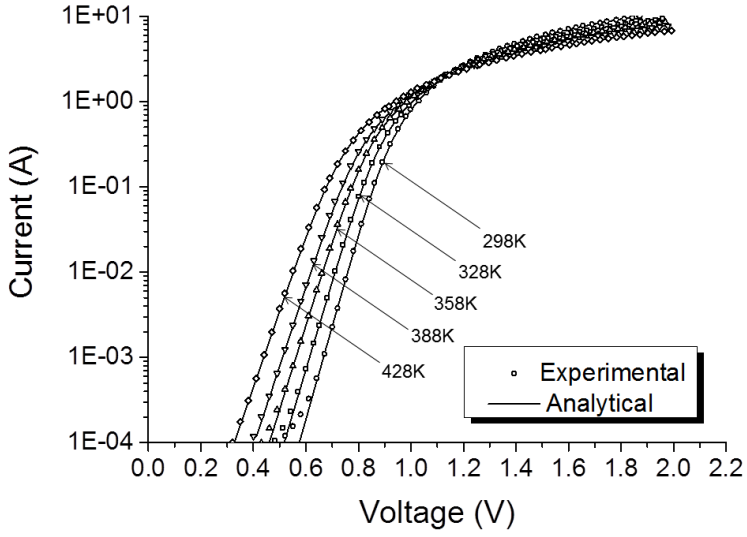


Fig. 4.6 Sub-threshold experimental and analytical on-state I-V characteristic for device shown in Fig. 4.1 at increased temperatures

The variation of device series resistance with temperature was also investigated. As mentioned, the series resistance in a GaN/AlGaN heterostructure power diode is composed of the contact resistance (R_{con}) and the drift region resistance (R_{2DEG}). Series resistance in such a device is affected by temperature mainly due to the effect of temperature on the mobility of carriers in the 2DEG channel. A simple mobility model

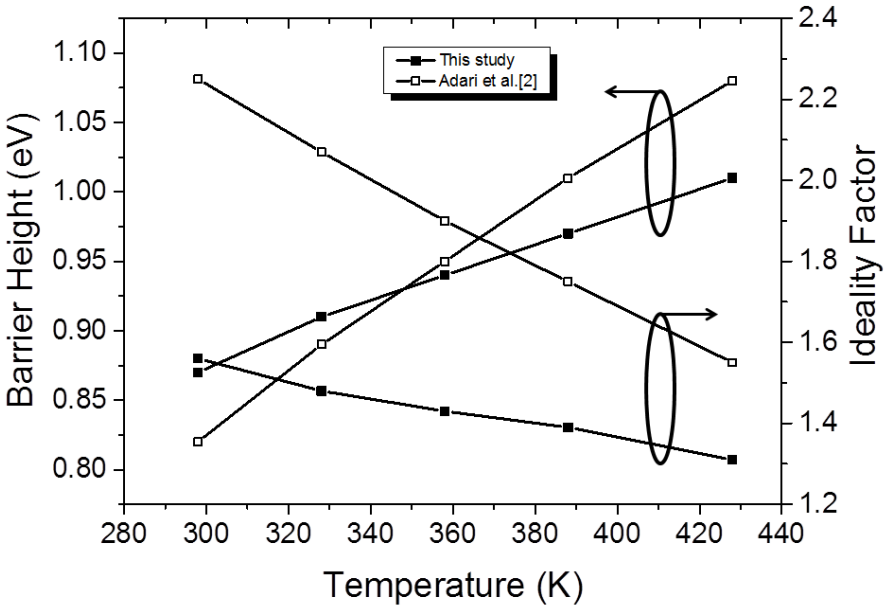


Fig. 4.7 Extracted ideality factor and barrier height as a function of temperature for device shown in Fig.4.1

which accounts for phonon scattering effects is described by Eq. 4.9 [95]. In this model mobility is only dependent on the lattice temperature which is a valid assumption given that the 2DEG channel is in a region of low doping and the electric fields present under on-state conditions are not very high.

$$\mu = \mu_L * (\frac{T}{300K})^{-\zeta} \tag{4.9}$$

where T is temperature in K, μ_L = mobility at room temperature and ζ = mobility exponent.

The mobility exponent can be found using the data extracted in the following way:

$$R = l/n\mu qA \tag{4.10}$$

where l is length of drift region, A is conduction path area and n is number of carriers available which is assumed to be constant with temperature.

Combining Eq. 4.9 and Eq. 4.10 and rearranging:

$$log(R) = \zeta log(\frac{T}{300K}) + log(\frac{l}{Aqn\mu_L}) \tag{4.11}$$

The value of the mobility exponent is the gradient of the plot log(R) vs (T/300K). The value for the mobility exponent extracted was $\zeta = 1.84$ which agrees well with values found in literature for GaN devices [96].

4.4 Conclusions

The following parameters, ideality factor ($\eta = 1.56$), barrier height ($\Phi = 0.87eV$) and series resistance ($R = 0.083\Omega$) of a Schottky AlGaN/GaN diode were extracted using a single I-V measurement at room temperature. I-V measurements performed at different temperatures up to 428K allowed the extraction of the above parameters at different temperatures. The series resistance, of which a large component is given by the 2DEG resistance, increases with temperature, as expected, due to the mobility decrease in the channel (mobility exponent, $\zeta = 1.84$) . The ideality factor was found to move closer to one at increased temperatures while the extracted Schottky barrier height was found to increase. This is in line with the experimental findings reported in the literature, although the dependence of both ideality factor and barrier height with temperature seem to be softer in our case which makes the device more stable in temperature.

The results discussed in this chapter are published in [97].

Chapter 5

Overview of the operation of AlGaN/GaN Schottky diode and comparison with competing technologies

5.1 Motivation

As discussed in Chapter 1, wide bandgap semiconductors such as SiC and GaN are considered very promising materials for use in the field of power devices with the potential to achieve increases in power density, reduced on-resistance, and high frequency response. The wide bandgap of these materials allows a high critical electric field to be sustained which can lead to the design of devices with shorter drift regions than silicon devices for the same breakdown voltage [98]. SiC Schottky diodes have in recent years found use in several applications allowing a reduction in power losses and increase in switching frequencies [99]. GaN-on-Si lateral diodes have been suggested as possible alternatives to these SiC schottky diodes in the 600 V - 1.2 kV voltage range. Both SiC and GaN-based diodes are unipolar devices proposed to have a negligible reverse recovery current during turn-off and can therefore be switched at very high frequencies with low power losses [100][101]. While this may certainly hold true for SiC Schottky diodes, this claim regarding GaN Schottky diodes will be examined by comparing the reverse recovery characteristic of an AlGaN/GaN diode with that of a SiC diode and fast recovery Si PIN diode for the same current (4A) and voltage rating (700V) both experimentally and in TCAD simulations. This will be preceded by a

thorough investigation of the reverse recovery of an AlGaN/GaN Schottky diode and in particular an examination into the differences which arise due to the presence of the heterostructure and the three terminal configuration of the AlGaN/GaN Schottky diode compared to a conventional vertical Schottky structure.

A TCAD model of a test AlGaN/GaN device was built and thoroughly matched with on-state, off-state and reverse recovery experimental measurements. The model was employed to analyse the different options available for connection of the substrate contact, a consideration specific to the AlGaN/GaN lateral configuration. The reverse recovery current components and the transient depletion of the 2DEG during turn-off are also examined. The turn-off behaviour of a lateral AlGaN/GaN Schottky diode has not been analysed to this extent elsewhere in the literature. Finally, the comparison of the different technologies (GaN, SiC, Si) will be made based on the trade-off between on-state and reverse recovery parameters at both room and high temperatures. Experimental and TCAD results show that while the AlGaN/GaN heterostructure Schottky diode is expected to provide a significant improvement in switching performance when compared to the conventional bipolar Si P-N diodes, the SiC diode offers a more favourable trade-off between on-state and reverse recovery.

5.2 Device Structure

The schematic cross-sections of the AlGaN/GaN and SiC Schottky diodes analysed in this work are presented in Fig. 5.1. In this figure, the electron concentration forming the channel of the GaN diode and the N-doping included in the SiC diode are also shown. An SiC Schottky diode structure is included as a reference of a conventional vertical structure. The SiC diode is based on a vertical two-terminal structure with the anode Schottky contact on the top and the cathode contact at the bottom of the device (Fig. 5.1b). The design includes a P-N junction grid under the conventional metal-semiconductor junction of the Schottky contact (MPS concept) to improve off-state performance [99]. A uniform distribution of N-doping concentration of $5x10^{15}\,cm^{-3}$ has been included in the drift region of the TCAD model in order to match the experimental data. A higher concentration of $1x10^{18}\,cm^{-3}$ has been added in the substrate region.

The GaN Schottky diode is a lateral three-terminal device with an AlGaN/GaN heterostructure grown epitaxially on a standard silicon wafer (Fig. 5.1a). A buffer layer is used to allow a high quality GaN layer to be grown despite the significant lattice mismatch between GaN and Si. The structure features a recessed anode where the

Schottky contact is made directly to the 2DEG. The anode metal used to provide the Schottky barrier is Platinum (Pt). Two major differences between the two structures can be pointed out. Firstly, a third terminal is present in the GaN Schottky diode. Secondly, while charge is uniformly distributed in the volume of the drift region of a SiC diode, in the GaN diode it is confined at the interface of the AlGaN/GaN heterojunction. Schematic representations of the electron concentration forming the channel of the GaN diode and the N-doping included in the SiC diode drift region can be seen in Fig. 5.1.

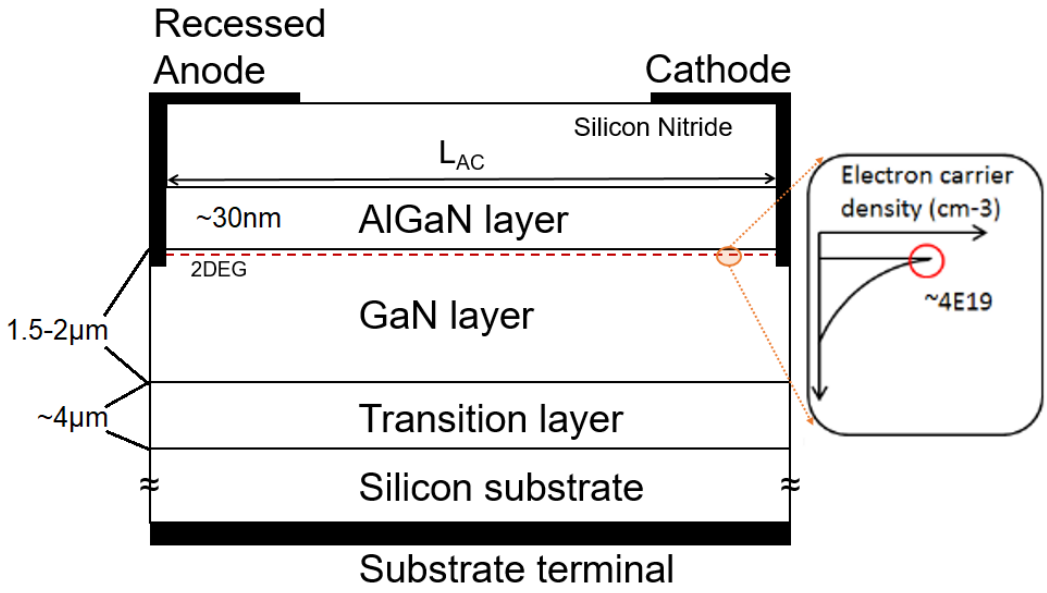
5.3 Experimental methods

Pulsed on-state and off-state measurements were taken using a Keithley 2600 series measurement unit. These measurements were used to calibrate the model of the device constructed in the Sentaurus TCAD simulation platform. Reverse recovery measurements were carried out using a standard inductive switching circuit (see Fig. 5.2) which comprises a gate resistance (R1) for controlling the dI_F/dt to define the switching condition ($300\,A/\mu s$). The main inductor L1 ($400\,\mu H$) behaves as a constant current source. The test diodes characterised correspond to the device under test (DUT) shown in the circuit. Parasitic inductances and capacitances (LC, LE, C1) were also included. In the case of the lateral GaN diode, an additional consideration exists regarding the connection of the substrate terminal as described in section 5.2. The substrate was connected to the anode terminal in the test device. An analysis of the optimum substrate connection (grounded, floating, anode terminal connection) was undertaken by reproducing the same circuit in mix-mode simulations using the Sentaurus TCAD simulation software platform. This will be discussed in section 5.4.2.

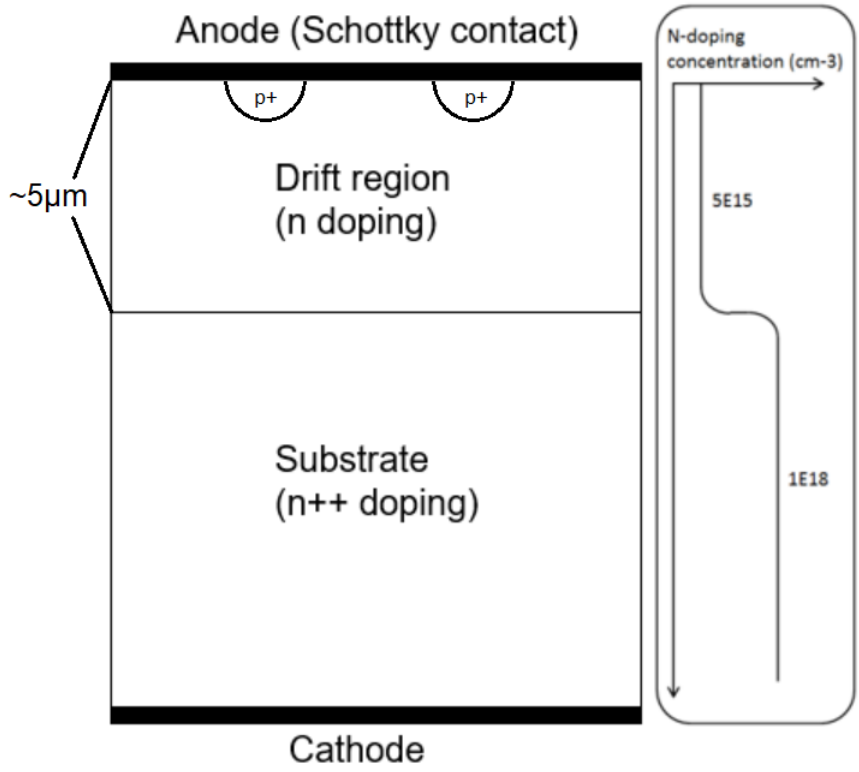
5.4 TCAD model

5.4.1 Model matching

The TCAD model was matched thoroughly with the corresponding experimental data. Fixed charges were included in the TCAD simulation deck according to [38] to take into account the piezo-polarisation effect observed in GaN devices. The resulting interface charge is a function of both the thickness (t=30nm) and Aluminium content (x=0.25) of the AlGaN layer. An anode metal work function was specified to provide a Schottky barrier height of 0.90eV in agreement with the literature for a platinum



(a)



(b)

Fig. 5.1 Cross section of (a) AlGaN/GaN device and (b) SiC device used for experimental measurements and TCAD model.

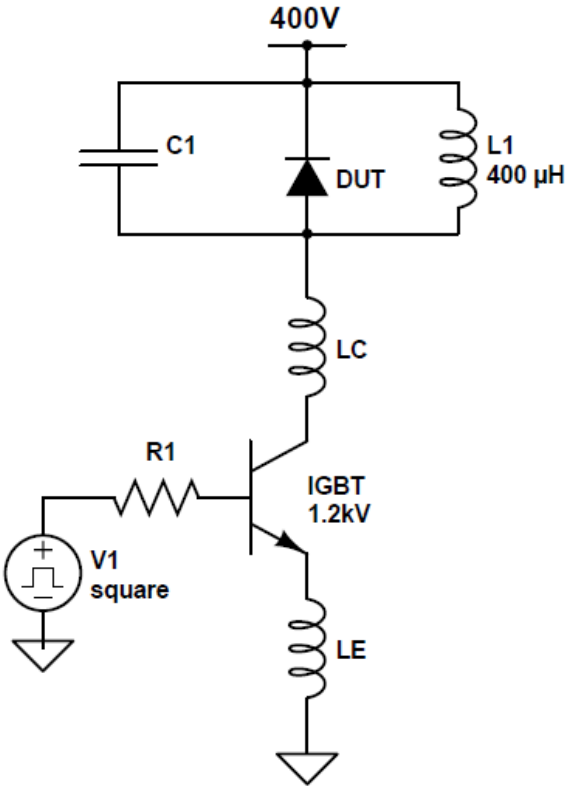


Fig. 5.2 Experimental and simulation reverse recovery test circuit

on n-GaN (2DEG layer) contact [102][103]. A surface donor trap concentration at the AlGaN/passivation interface was included in the TCAD model according to the analysis discussed in [104]. This was used as a fitting parameter to achieve a better match between the experimental and simulation results. A p-type doping of $1x10^{16}cm^{-3}$ was added in the GaN layer to take into account the carbon doping effects as reported in the literature [105]. The model was also calibrated to be reliable at increased temperatures. R_{on} in such a device is affected by temperature mainly due to the effect on the mobility of carriers in the 2DEG channel. A simple mobility model which accounts for phonon scattering effects was used [95] as described in section 3.1.6. In this model, mobility is only dependent on the lattice temperature which is a valid assumption given that the 2DEG channel is in a region of low doping and the electric fields present under on-state conditions are not very high. The value for the mobility exponent used was extracted as described in [97]. The value of $\zeta = 1.8$ used is consistent with values found in the literature for GaN devices [96]. A good on-state match was achieved both at room temperature and increased temperature as seen in Fig. 5.3. A good off-state match was also achieved as seen in Table 5.1. The TCAD model reveals that a relatively high

leakage current is observed in these devices due to tunnelling at the Schottky contact which is made directly to the 2DEG where a very high density of carriers exist. The effect of tunnelling was verified by running simulations where the tunnelling physical model was not activated and the off-state leakage observed was found to be greatly reduced.

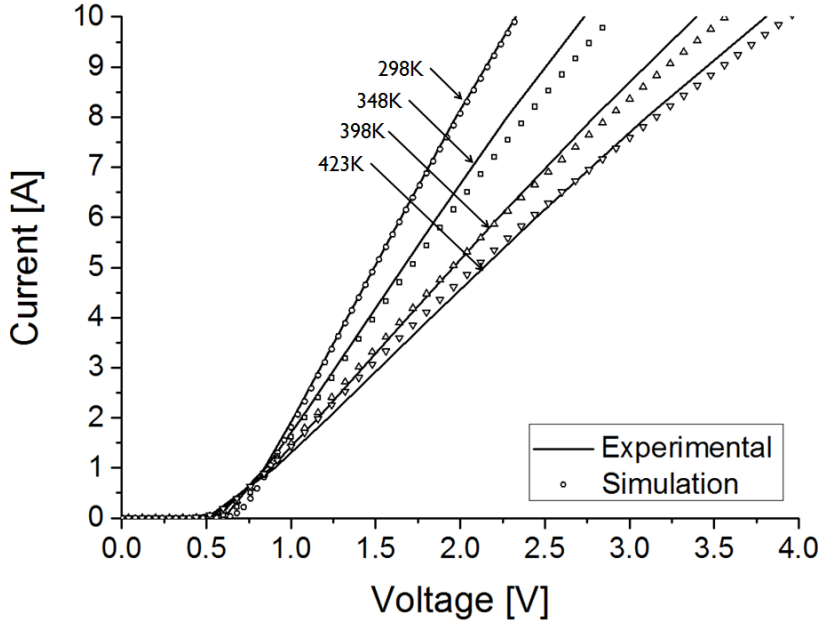


Fig. 5.3 Experimental measurement and TCAD model simulation on-state matching at a range of temperatures

	TCAD model	Test device
$I_r(\mu A)$ at 600V	1.7	6.1
V_r(V) at 10μA	737	710
V_r(V) at 100μA	>800	803

Table 5.1 Comparison of off-state leakage observed in experimental measurements and TCAD model simulations

The carrier concentration in the 2DEG channel of the TCAD model was varied by adjusting the Aluminium mole fraction in the AlGaN layer of the heterostructure. The simulated effect of the 2DEG carrier concentration on the reverse recovery performance of the device is shown in Fig. 5.4. A trade-off was observed between the on-state and reverse recovery characteristic of the GaN diode where increased channel charge leads to reduced on-state losses but increased reverse recovery losses as will be discussed in this analysis.

Taking into consideration this trade off, a fairly accurate match was obtained between the simulated reverse recovery characteristic of the AlGaN/GaN Schottky diode model and the experimental result, as shown in Fig. 5.5. Note that a contribution of the circuit parasitic capacitance in parallel with the device under test as seen in Fig. 5.2 is included in the reverse recovery curves which match the experimental results. Despite the good match between the experimental measurements and the TCAD model simulations, there are still some limitations to the accuracy of the TCAD model and this shall be outlined at the end of the chapter.

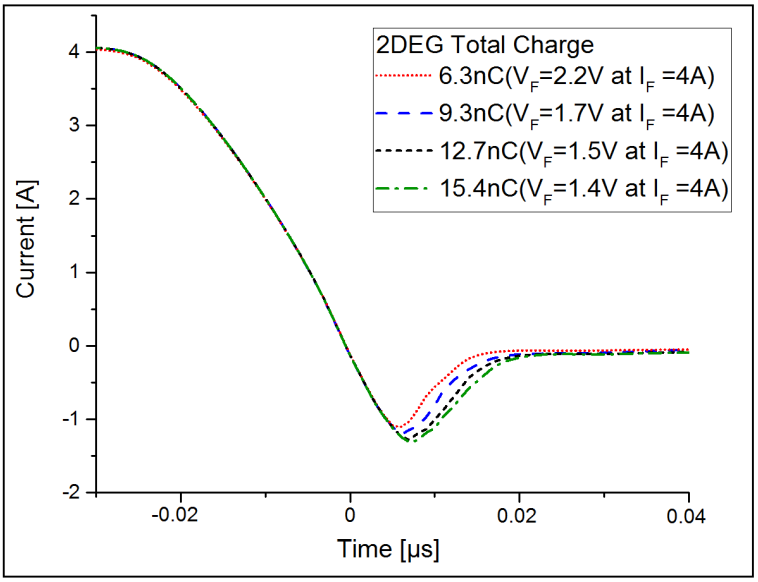


Fig. 5.4 Effects of 2DEG charge level on TCAD model reverse recovery characteristic for AlGaN/GaN Schottky diode device shown in Fig. 5.1a.

5.4.2 Effect of substrate connection on GaN device performance

As mentioned in section 4.3 there is an added consideration in the connection of the substrate contact of the three-terminal GaN device compared to the two-terminal SiC devices. Three possible substrate terminal connections exist: grounded, floating, and anode terminal connected. The chosen substrate connection is found to have a very significant effect on the on-state and reverse recovery performance of the device when operating in the inductive switching circuit outlined in section 4.3. To understand this it is necessary to look at the bias of the three terminals (anode, cathode, substrate) at different stages of the switching waveform applied to the gate of the switch (IGBT). A

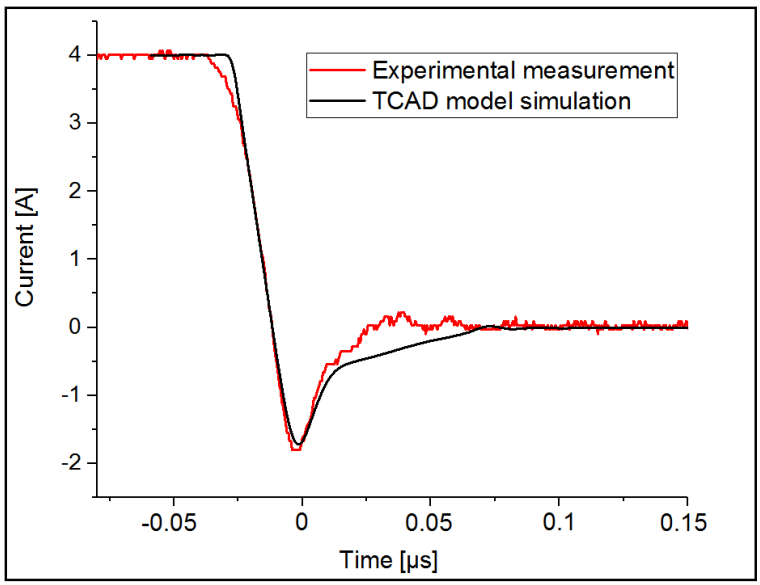


Fig. 5.5 AlGaN/GaN Schottky diode reverse recovery characteristic match between TCAD model simulation and experimental result at room temperature.

series of two pulse signals (V1) to the gate of the IGBT are used to obtain the reverse recovery of the diode as shown in Fig. 5.6. First on-pulse turns the IGBT on and charges the inductance L1 until the desired current level (4A) is reached. When pulse signal (V1) goes low the IGBT turns off causing the potential at V3 to start rising, eventually turning the diode on. The inductance current is then directed through the diode with the current level remaining fixed at 4A. A second on-pulse turns the IGBT back on. Voltage at V3 starts dropping turning off the diode and the reverse recovery of the diode is observed. Note that in Fig. 5.6 the waveforms shown are ideal for illustrative purposes. The state of the diode during the pulse applied is pointed out in Fig. 5.6.

When the pulse is applied in TCAD simulations with the substrate grounded, the current observed in the Schottky diode in the on-state is negligible. Thus, as the IGBT turns off, voltage V3 keeps rising beyond the IGBT breakdown capability. Furthermore, it is observed that during the time period when the diode is ON a higher voltage drop, V_{on} is observed across the diode for a given current (4A) in the case where the substrate is floating rather when it is connected to the anode terminal. These results are summarised in Table 5.2.

The substrate connection affects the 2DEG carrier density due to the potential difference developed between the surface terminals (anode/cathode) and the substrate. This is better understood when looking at Table 5.3 where the voltage bias of the

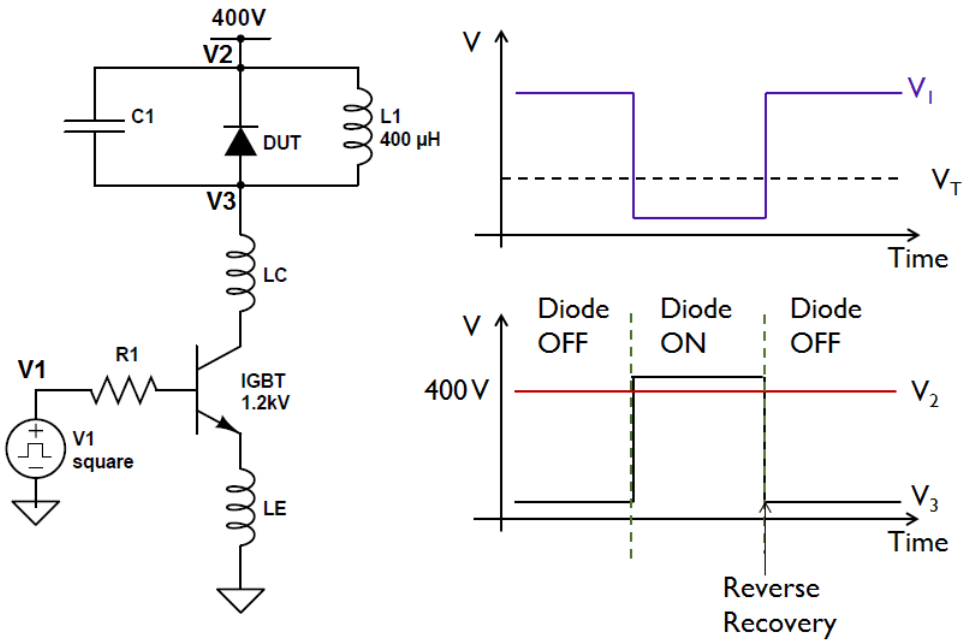


Fig. 5.6 (a) Experimental and simulation reverse recovery test circuit (b) Electrostatic potential at points V1, V2, V3 during reverse recovery test

different terminals of the device when the diode is in the ON state is shown according to the TCAD simulations.

If the substrate is grounded then a large vertical field develops in the device between the surface terminals and the substrate. This vertical field reduces the carrier density in the 2DEG and therefore affects the on-state performance of the device. If the substrate is floating, a weaker vertical field is present and thus a stronger 2DEG carrier density is produced (see Table 5.2). It is therefore expected that the lowest forward voltage drop will be observed when the substrate is connected to the anode as the potential difference between the surface terminals and the substrate is eliminated when the device is ON. Nonetheless, a higher 2DEG carrier density leads to more charge present during turn-off which affects the reverse recovery performance. Reverse recovery performance parameters for different substrate connections in the TCAD model mix-mode simulations are again summarized in Table 5.2. A comparison of the corresponding simulated reverse recovery curves for the floating and anode connected configurations (as no switching was achieved with the grounded substrate) can be seen in Fig. 5.7. It is clearly demonstrated that a trade-off exists between the on-state and reverse recovery performance of the device when considering the substrate connection. As on-state losses would account for the majority of losses in such a device,

Substrate	2DEG carrier density (cm-2)	Charge (nC)	V_{on} (V)	Reverse recovery parameters		
				$I_r(A)$	$T_{rr}(ns)$	$Q_{RA}(nC)$
Grounded	N/A	N/A	N/A	N/A	N/A	N/A
Floating	$0.97x10^{12}$	2.59	4.7	0.52	14	2.63
Anode connected	$5.5x10^{12}$	14.6	1.5	1.28	21	13.7

Table 5.2 Effect of substrate connection on on-state and switching performance

Substrate	Terminal potential (V)		
	Anode	Cathode	Substrate
Grounded	N/A	400	0
Floating	404.7	400	270
Anode connected	401.5	400	401.5

Table 5.3 Effect of substrate connection on terminal potential in TCAD simulations

the substrate/anode terminal connection would prove to be the most efficient option and this was therefore used in the test device produced.

5.4.3 AlGaN/GaN Schottky diode turn-off

As described in section 5.2, the lateral AlGaN/GaN diode has a very different structure to a conventional vertical device such as the SiC device described. The charge distribution in SiC and GaN is completely different. In SiC the charge is uniformly distributed in the drift region which leads to a smooth recovery as the depletion region gradually advances in the drift layer during the reverse recovery. In GaN, the 2DEG layer is confined at the interface, has a very high carrier density and depletes initially laterally from the anode field plate, and then vertically from below due to the acceptor charge in the GaN buffer.

The TCAD model offers the opportunity to observe the depletion of the 2DEG in time as shown in Fig. 5.9b. The density of carriers in the 2DEG is plotted along the length of the 2DEG between the anode and the cathode. Electron carrier density curves (numbered: 1-10) correspond to different points in time as shown on the reverse recovery curve. A large proportion of the charge is removed through the anode/cathode current path as the depletion extends from the recessed anode contact. The tail in

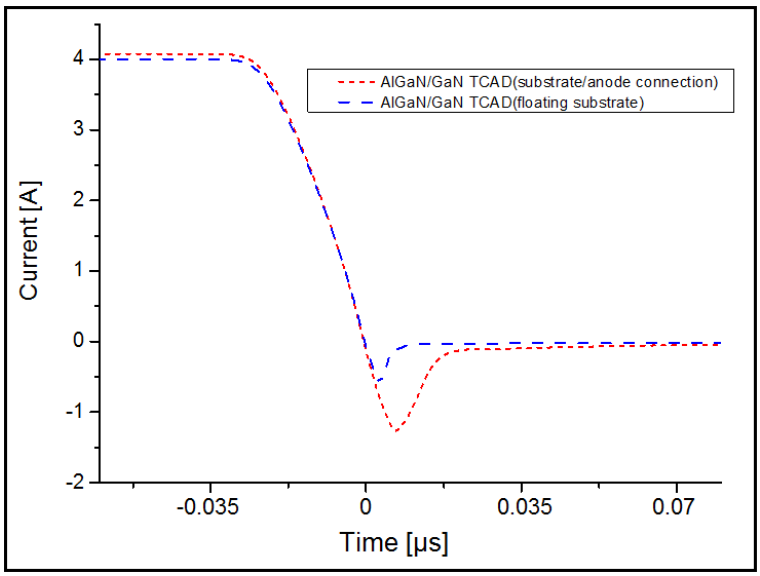


Fig. 5.7 Effects of substrate connection on TCAD model reverse recovery characteristic for AlGaN/GaN Schottky diode device shown in Fig. 5.1a.

the reverse recovery characteristic is seen due to charging of the capacitance along the vertical p-n junction formed between the large concentration of electrons in the non-depleted 2DEG layer (close to the cathode contact) and the p-doped GaN layer. When the substrate is connected to the anode terminal this current component makes a significant contribution to the reverse recovery current observed. Since this is a capacitive current its magnitude is proportional to the rate with which the potential difference grows between the cathode terminal (which remains biased to 400V) and the substrate terminal (which falls from 400V to 0V) as plotted in Fig. 5.9a. This dV/dt in turn relates to certain circuit parameters such as the parasitic emitter inductance in the circuit and the IGBT gate resistance. In conclusion, two displacement current components can therefore be distinguished: anode to cathode and cathode to substrate. These two components add to give the total reverse recovery characteristic. The contribution of each of these two components can be seen in Fig. 5.8.

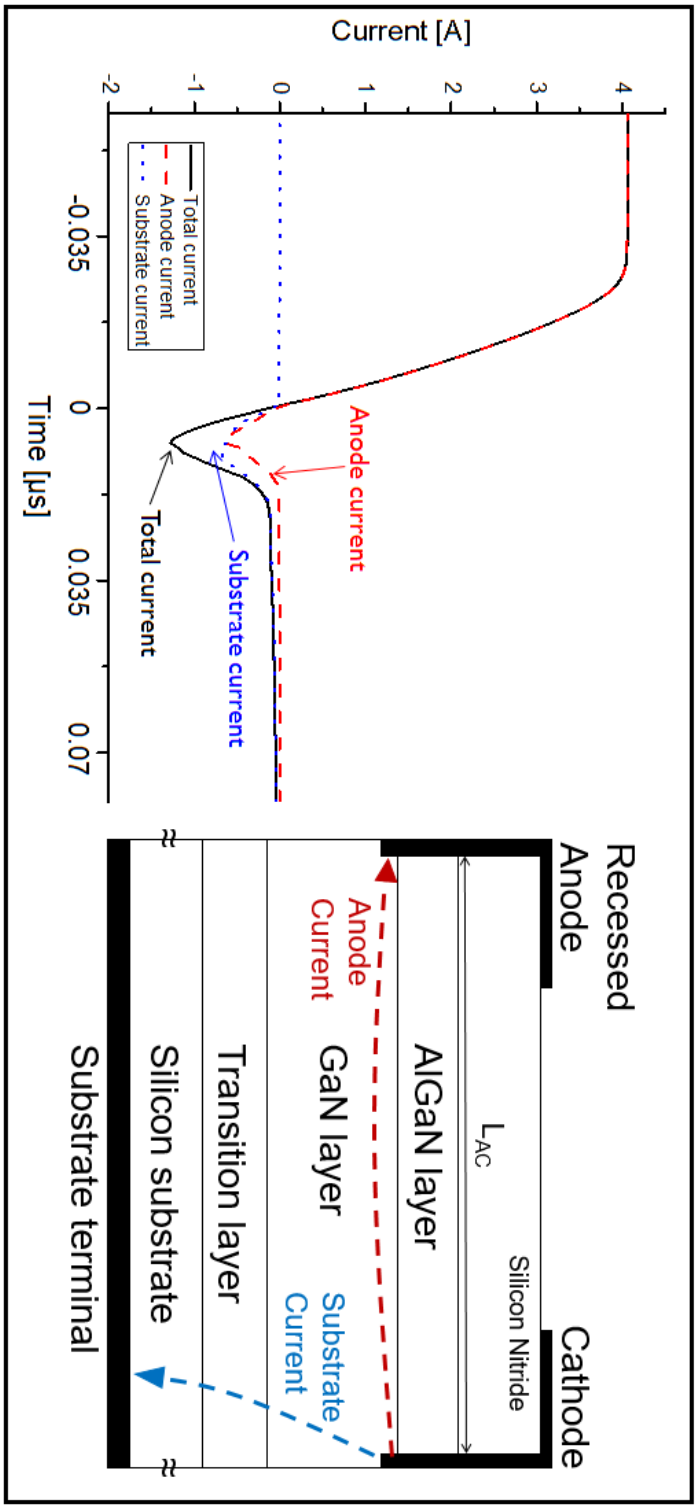
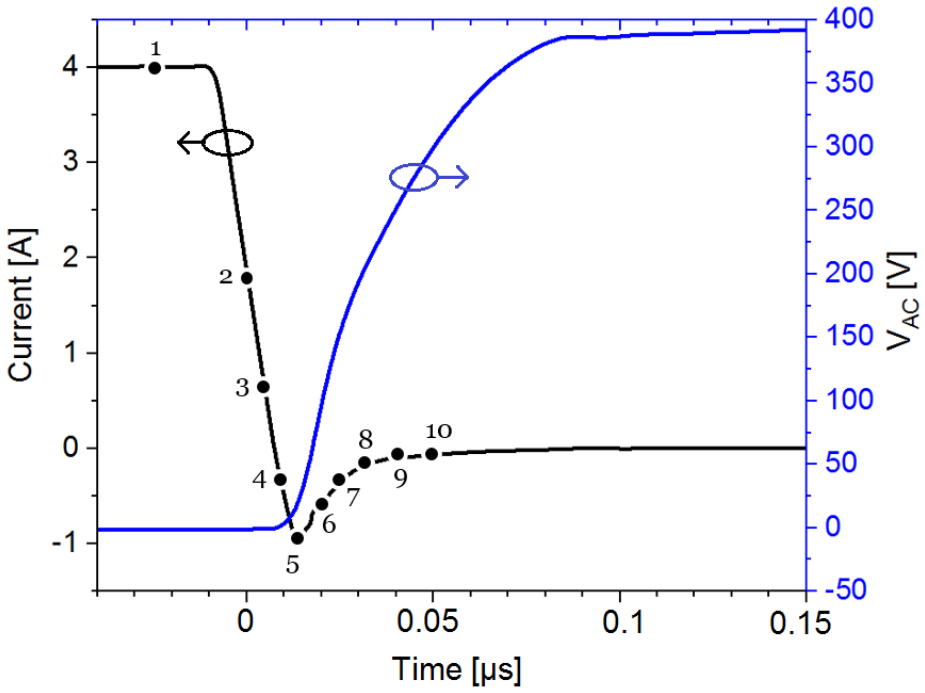
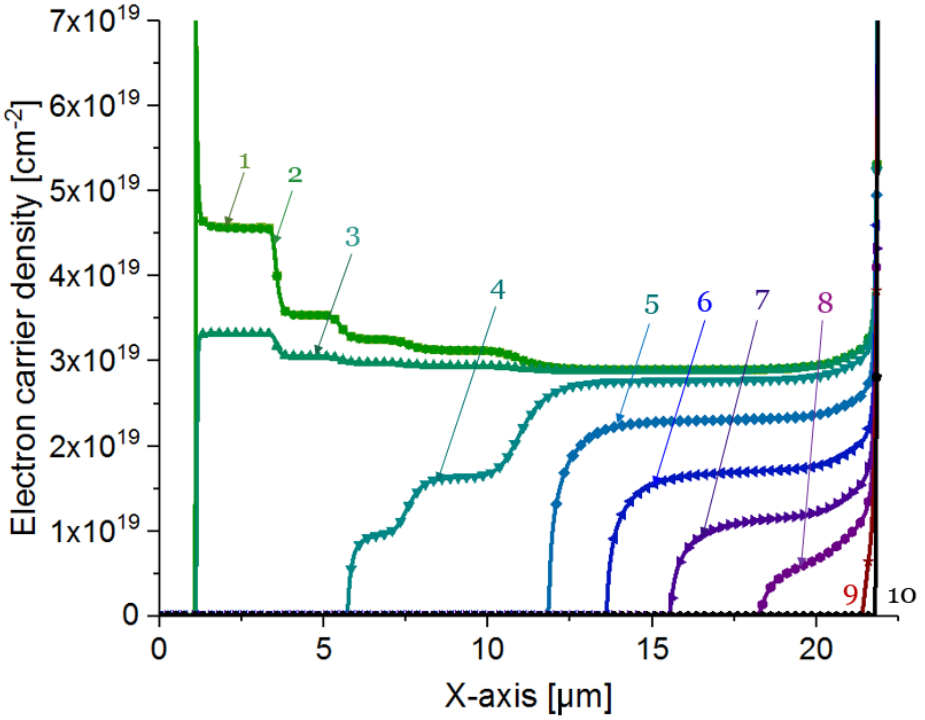


Fig. 5.8 Reverse recovery current components with anode/substrate connection



(a) AlGaN/GaN Schottky diode current and voltage across diode (V_{AC}) during turn-off : saved solutions



(b) TCAD model electron carrier density across the 2DEG at different times during turn-off waveform

Fig. 5.9 Illustration of depletion of 2DEG carrier denisty with time during turn-off

5.5 Comparison with competing technologies

To follow the discussion on the reverse recovery of AlGaN/GaN Schottky diodes, a comparison with their main industry competitors will be given. This was done using real devices and supplemented with TCAD model simulations.

5.5.1 Experimental Measurements

Several 600-650 V Si[1], SiC[2] and GaN diodes of the same current rating were tested using the experimental circuit shown in Fig. 5.2. On-state performance of these diodes is shown in Table 5.4.

	Forward Voltage, V_F at $I_F = 4A$	
Type of the diode	$T = 25^oC$	$T = 150^oC$
GaN	1.4V	1.9V
SiC(1)	1.4V	1.9V
SiC(2)	1.5V	1.8V
Fast recovery Si(1)	2.6V	1.5V
Fast recovery Si(2)	2.2V	1.3V

Table 5.4 Forward voltage drop of tested devices at room temperature and increased temperatures

Figures 5.10 and 5.11 show the measured reverse recovery curves of the same devices at 25^oC and 150^oC. One can note that the vertical SiC diode offers the best trade-off between on-state and reverse recovery losses. Both the SiC and the GaN diodes outperform the fast recovery Si diodes, and have an insignificant increase in the reverse recovery losses when operating at high temperatures, unlike silicon. The opposite trend is however observed in on-state losses where the performance of the unipolar GaN and SiC diodes is diminished at increased temperatures due to reduced carrier mobility. On the other hand the on-state performance of fast recovery Si diodes is improved at increased temperatures due to increased conductivity modulation.

[1]In this section, Fast recovery Si(1) device refers to a STMicro-STTH8R060 diode and Fast recovery Si(2) device refers to a Vishay-ETX0806 diode.

[2]In this section, SiC(1) device refers to a CREE-C3D04060 diode and SiC(2) device refers to a STMicro-STPSC406D diode.

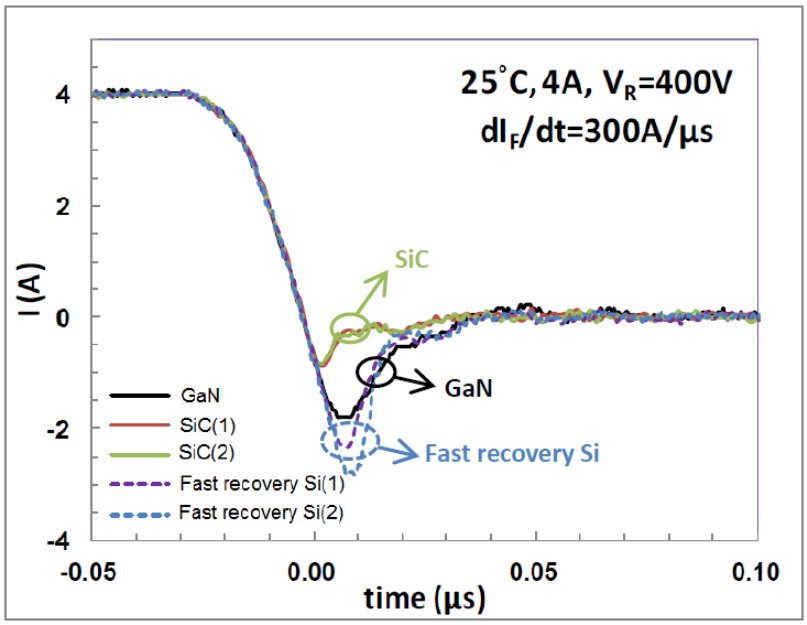


Fig. 5.10 Experimental reverse recovery characteristic of AlGaN/GaN diode compared with SiC Schottky diodes and fast recovery Si diodes of similar rating at room temperature.

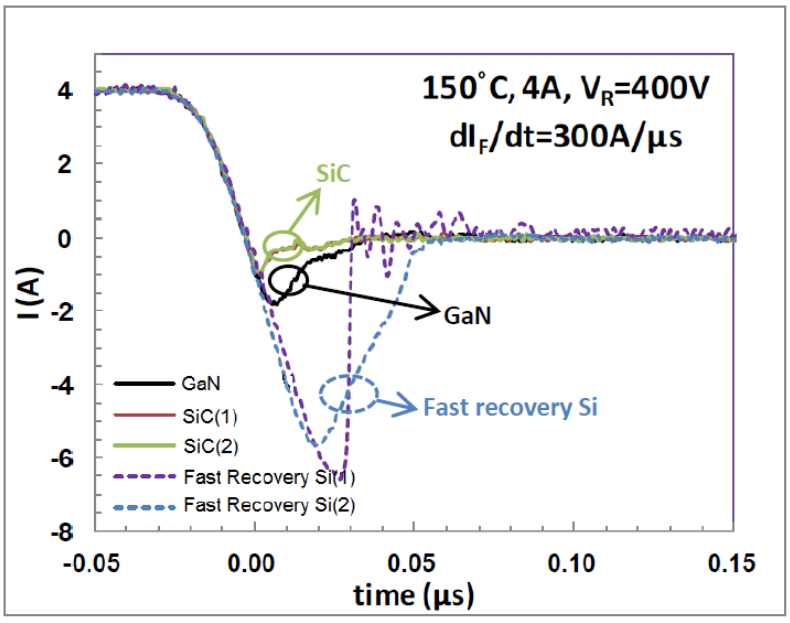


Fig. 5.11 Experimental reverse recovery characteristic of AlGaN/GaN diode compared with SiC Schottky diodes and fast recovery Si diodes of similar rating at room temperature.

	AlGaN/GaN		SiC(1)		SiC(2)		Fast recovery Si(1)		Fast recovery Si(2)	
	$I_F = 4A$, $dI/dt = 300A/us$, $V_R = 400V$									
Temp	25^oC	150^oC	25^oC	150^oC	25^oC	150^oC	25^oC	150^oC	25^oC	150^oC
$I_R(A)$	1.80	1.70	0.70	0.73	0.64	0.67	2.28	7.04	2.55	5.58
$t_{rr}(ns)$	30.9	32.0	26.6	29.7	28.9	29.1	30.8	32.3	22.9	51.7
$t_{rrA}(ns)$	33.2	34.3	28.9	32.3	31.5	31.6	33.1	32.7	24.2	54.6
$Q_{RA}(nC)$	29.8	29.2	10.2	11.9	10.1	10.6	37.7	115.1	30.9	152.2

Table 5.5 Reverse recovery parameters of AlGaN/GaN Schottky diode at room temperature and increased temperature compared with SiC Schottky diodes and fast recovery Si diodes of similar rating

As shown by the reverse recovery measurements summarised in Table 5.5, the SiC vertical Schottky diodes are by far the closest to the claim of *zero reverse recovery losses*. This very significant result can be explained when considering the differences in the structure of the GaN and SiC diode. While charge is uniformly distributed in the volume of the drift region of a SiC diode, it is confined at the interface of the heterojunction for the AlGaN/GaN Schottky diode (see Fig. 5.1). When the SiC diode is turning off, the depletion region extends vertically into the drift region along the entire length of the Schottky contact. On the other hand, when the GaN Schottky diode is turning off the 2DEG layer is depleted laterally from the recessed Schottky contact and vertically from the GaN layer. A high concentration of carriers is removed through the narrow path of the 2DEG layer which extends only up to a few nm away from the heterointerface. To provide a more robust analysis of the effects that the distribution and magnitude of the drift region charge has on the reverse recovery characteristic of the GaN and SiC Schottky diodes, TCAD simulations were performed. The results of this analysis are discussed in the next section.

5.5.2 TCAD model comparison

TCAD simulations of on-state, leakage and reverse recovery characteristics were matched thoroughly with the corresponding experimental data as described in section 4.4. A very accurate match was obtained between the simulated reverse recovery characteristic of the AlGaN/GaN Schottky diode model and the experimental measurement, as previously shown in Fig. 5.5.

The TCAD model of the SiC diode was built with equivalent on-state and breakdown capabilities as the AlGaN/GaN diode. This was done in order to enable a direct comparison of the reverse recovery of the two devices in these conditions, as was the case with the real devices used. This revealed the difference in the charge present in the two devices when these matching conditions were achieved. Furthermore, a hypothetical SiC diode with a drift region charge equal to the charge in the 2DEG of the GaN diode was simulated. This was done to enable a comparison between the two devices when the drift region charge was matched, rather than the on-state characteristic. Fig. 5.12 shows the simulated on-state characteristics of the AlGaN/GaN and SiC devices for on-state matching and drift region charge matching.

It is observed that the SiC diode offers a better on-state performance for a given level of drift region charge. Fig. 5.13 highlights this observation, showing that the amount of charge necessary for a SiC diode to conduct a fixed current (8A) is significantly lower than the one required from a GaN diode to conduct the same current at a fixed forward

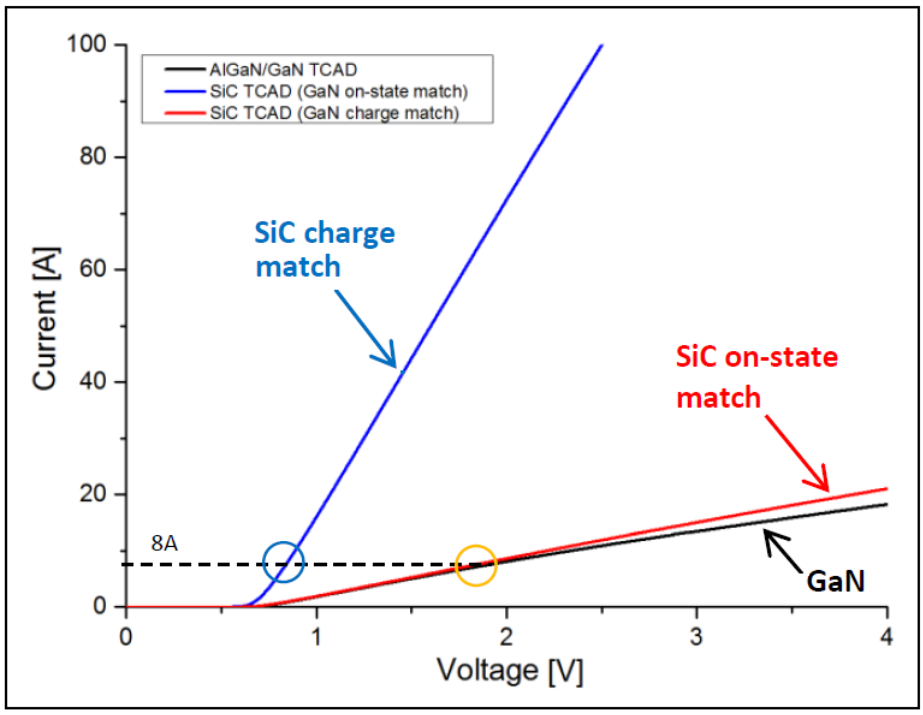


Fig. 5.12 Simulated on-state I-V characteristic of AlGaN/GaN diode model matched with SiC diode model. The on-state I-V characteristic comparison between the two devices is also shown with equal drift region charge.

voltage drop. This is due to the vertical configuration of the SiC diode compared to the lateral geometry of the AlGaN/GaN diode. Despite the higher critical electric field of GaN compared to SiC, a longer drift region is required in the GaN diode to achieve an equivalent breakdown voltage thus leading to increased drift region charge. This is a direct consequence of the less optimized electric field distribution observed in a lateral device. Simulations of the reverse recovery of the AlGaN/GaN and SiC devices were compared for both the models with matching on-state characteristic and the models with matching drift region charge. This comparison can be seen in Fig. 5.14 and is found to agree with the experimental results presented in the previous section revealing the superior performance of the SiC diode. The following observations are made:

- The 2DEG charge in GaN is significantly higher than the drift region charge in a SiC diode for equal rating and on-state performance (see Fig. 5.13). This results in the GaN device having a slower turn-off characteristic as well as larger reverse recovery current peak and losses.

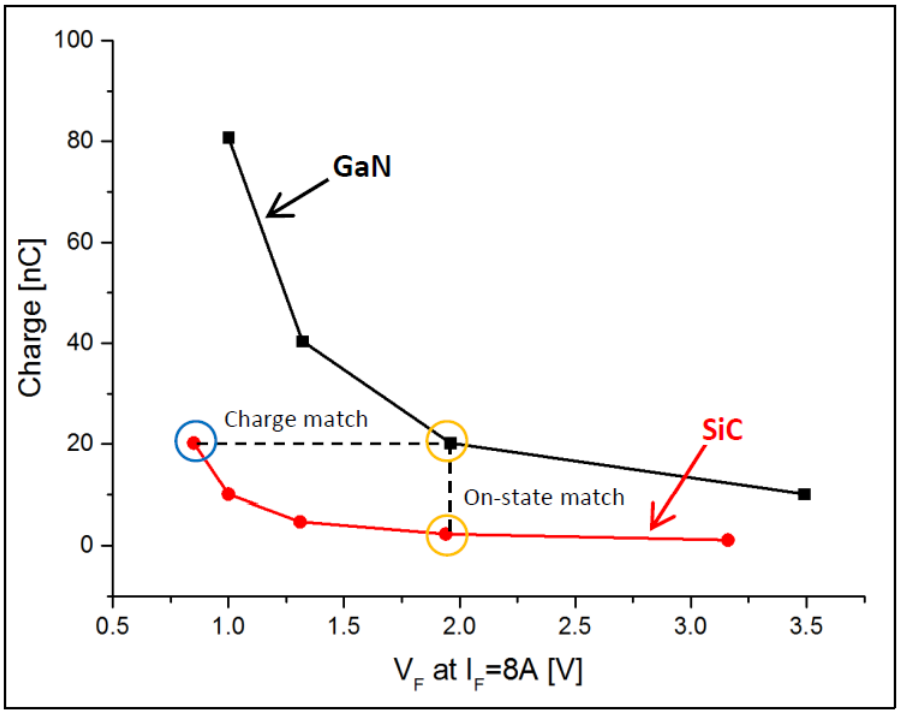


Fig. 5.13 Comparison of drift region charge for SiC and 2DEG charge for GaN vs forward voltage drop for a current rating of 8A for GaN and SiC Schottky diode TCAD models.

- In the hypothetical case where the drift region charge in SiC matches the 2DEG charge, the SiC diode still outperforms the GaN diode (with much lower on-state voltage drop and slightly better reverse recovery characteristics).
- The charge distribution in SiC and GaN is completely different. In SiC the charge is uniformly distributed in the drift region which leads to a smooth recovery as the depletion region gradually advances in the drift layer during the reverse recovery. In GaN, the 2DEG layer is confined at the interface, has a very high carrier density and depletes initially laterally from the anode field plate, and then vertically from below due to the acceptor charge in the GaN buffer.

5.6 TCAD model limitations and future work

The AlGaN/GaN diode TCAD modelling described in this chapter entails some simplifications which shall be described here. These simplifications can be removed in future research so that their effect on the results described in this thesis can be investigated. The first simplification relates to the definition of the acceptor doping in

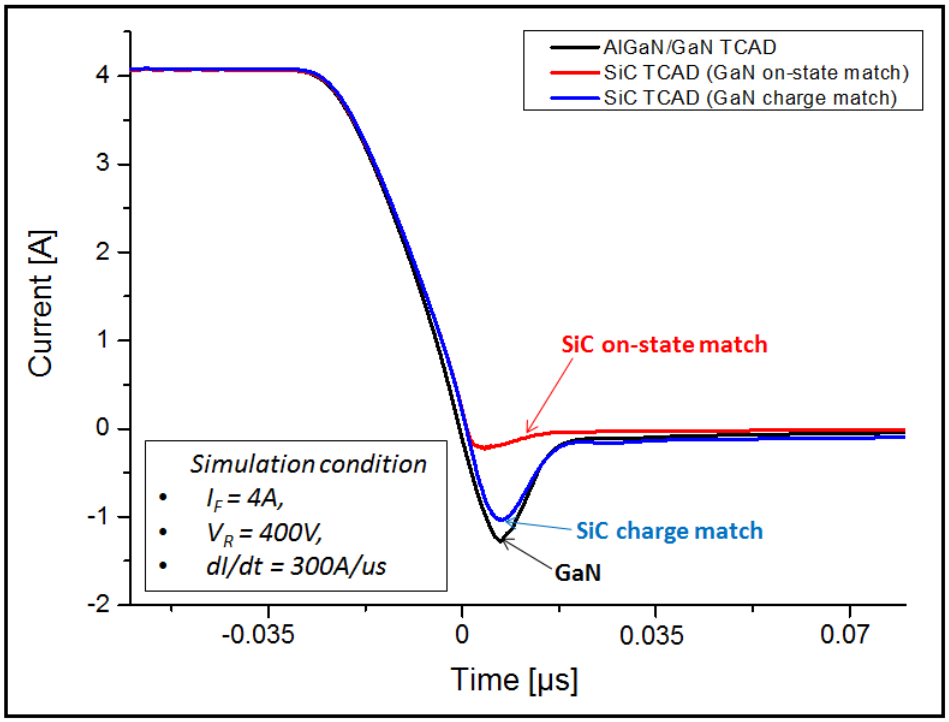


Fig. 5.14 Simulated reverse recovery characteristic of AlGaN/GaN diode model compared with SiC Schottky diodes of equal on-state current characteristic and equal drift region charge.

the GaN layer. In the current model, doping was specified as fully ionized under zero bias with the acceptor energy level specified very close to the valence band. In reality, as numerous studies in the literature have shown, this is not the case with Carbon doping reported to form energy levels at around 0.9eV [105][106] above the valence band. The ionization of these acceptor traps which are uncharged when de-onised (i.e. not captured electrons) and negatively charged when ionised is dependent on the electric field present in the specific region of the GaN layer as well as any current paths that exist in the device when it operates. High fields are formed during turn-off in the regions where the depletion region extends vertically from the 2DEG into the GaN layer which will lead to the ionisation of the majority of these acceptor traps. Due to the transient nature of these experiments, the capture rates of the traps are of interest as they can determine the activation percentage of the traps during turn-off. Nonetheless, capture rates are often fast [106][107] and therefore the effect on the reverse recovery curves observed are not likely to be very significant. On the contrary, during the diode turn-on, these traps will release electrons as the high electric field retreats. The much slower emission rates of electrons during turn-on and thus the negative space charge

which remains in the GaN layer can lead to current degradation in the on-state and the simplification in this model will likely be significant.

Another simplification relates to the accuracy with which the transition layer was reproduced in the TCAD model. Several challenges are related to this. Firstly, the information provided by the foundry on the transition layer is not very extensive. As described in Chapter 2 producing crack free GaN-on-Si wafers is a challenging task and the know-how is very well protected by the foundries. Secondly, the characterization of the transient layer is a very difficult topic in itself with numerous studies being conducted on the conduction mechanisms between the different layers, as well as the interface charges and traps present in these layers [108]. The transition layer is of interest in the reverse recovery of the diode as it can affect the extension of the depletion region during turn-off. Given that a significant component of the reverse recovery relates to this vertical displacement current the extent of this depletion region is significant. According to [38] a large negative interface charge is predicted at the GaN/transition layer interface. This may lead to the formation of a two dimensional hole gas (2DHG) which can stop the vertical depletion. However, the presence of this 2DHG is still being investigated [109]. Due to this very uncertainty about the 2DHG, many theoretical and simulation works have adopted the approach of treating the multi-layered epi with a simplified composition of layers or, more often, lumping them into a single layer, avoiding the issue of 2DHG at the interfaces altogether [106][109][110] as was done in this study. Future work can focus on improving the TCAD model by carrying out an investigation which takes into consideration the aspects described above and their effect on turn-off behaviour.

5.7 Conclusions

A TCAD model of a test AlGaN/GaN device is built and thoroughly matched with on-state, off-state and reverse recovery experimental measurements. The model is employed to analyse the different options available for connection of the substrate contact, a consideration specific to the AlGaN/GaN lateral configuration. TCAD simulations results show that the substrate connection affects the 2DEG carrier concentration due to the potential difference developed between the surface terminals (anode/cathode) and the substrate. It is demonstrated that a trade-off exists between the on-state and reverse recovery performance of the device when considering the substrate connection. As on-state losses would account for the majority of losses in such a device, the substrate/anode terminal connection would prove to be the

most efficient option. Furthermore, experimental and TCAD results show that while the AlGaN/GaN Schottky diode is expected to provide a significant improvement in switching performance when compared to the conventional bipolar Si P-N diodes, the suggestion of *zero reverse recovery* is not truly valid. This is due to the high level of 2DEG charge density, necessary in the on-state to compensate for the lateral geometry of the heterostructure diode. In conclusion, the SiC diode offers a more favourable trade-off between on-state and reverse recovery and its performance can be controlled more accurately as it is not subject to surface or bulk traps. The analysis carried out here uses complex TCAD models matched to extensive experimental results and it contains aspects which contradict findings in literature that suggest comparable turn-off performance between GaN and SiC Schottky diodes of equal rating.

The results discussed in this chapter are published in [111].

Chapter 6

On the physical operation and optimization of the p-GaN gate in normally-off GaN HEMT devices

In this chapter an investigation is undertaken to determine the effect of gate design parameters on the on-state characteristics (threshold voltage, gate turn-on voltage) of p-GaN/AlGaN/GaN HEMTs. Design parameters considered are p-GaN doping and gate metal work function. The analysis considers the effects of variations in these parameters using a TCAD model matched with experimental results. A better understanding of the underlying physics governing the operation of these devices is achieved with a view to enabling improved optimization of such gate designs.

6.1 Introduction

A two dimensional electron gas (2DEG) inherently exists at the AlGaN/GaN hetero-interface which creates a challenge when attempting the design of normally-off rather than normally-on devices. Nonetheless, as normally-off transistors are preferable in most power electronic applications, several methods have been proposed which can lead to enhancement mode devices, among them, the use of metal insulator semiconductor structures [43], use of fluorine treatment [45], recessed gate structures [44] and use of a p-type cap layer [47][48][49]. Due to the relative maturity and controllability in the epitaxial growth of p-GaN layers compared to the other techniques, p-GaN/AlGaN/GaN HEMTs are considered the leading solution for commercialization. While several publications exist on different aspects of the performance of GaN devices (breakdown,

buffer leakage, current collapse) [50][51] there is less focus on the role that gate design parameters have in determining the on-state characteristics (threshold voltage, trans-conductance and gate turn-on current) of p-GaN devices. These parameters are of great interest as problems such as unwanted device turn-on when the device is supposed to be off may occur in operation if threshold voltage is low. Secondly, gate turn-on may be a problem due to the non-insulated gate structure. Furthermore, several studies have reported that the gate structure can play an important role in the reliability of p-GaN HEMTs due to the high electric field that is developed in the region under forward bias stress. The high electric field can lead to the generation of defects in the p-GaN[52] which can subsequently increase the leakage current via a defect percolation process and ultimately lead to device failure [53][54][55]. An understanding of what affects parameters such as threshold voltage, trans-conductance, gate leakage and gate turn-on current is therefore paramount to achieving a good design. Some literature exists on controlling these parameters, specifically on the impact that the gate metal used has on the on-state performance [112][113]. While Hwang et al. [113] reports a large shift in threshold voltage when gate metal is varied, Lee et al. [112] does not. The disagreement between the two results can be explained when the different Schottky metal/p-GaN barrier present in the two devices is taken into consideration and specifically relates to the scale of hole tunnelling current observed at this interface. The Schottky barrier observed is affected both by the gate metal work function and the acceptor doping used in the p-GaN cap.

This study offers a comprehensive analysis of the underlying physics which governs the operation of the p-GaN/AlGaN/GaN gate structure. A TCAD simulation model is matched thoroughly with device experimental measurements and is used to enable better understanding and optimization of such gate designs.

6.2 Device Structure and TCAD models

The device investigated is a lateral three-terminal device with an AlGaN/GaN heterostructure grown epitaxially on a standard silicon wafer (Fig. 6.1). A buffer layer is used to allow a high quality GaN layer to be grown despite the significant lattice mismatch between GaN and Si. While, as described in Chapter 2, the characteristics of the buffer layer may have an important effect on device off-state bulk leakage and breakdown as well as transient performance the analysis described in this chapter is not concerned with these topics. Therefore, very little effort has been put into achieving an accurate representation of this buffer layer. Nonetheless, accurate dimensions of

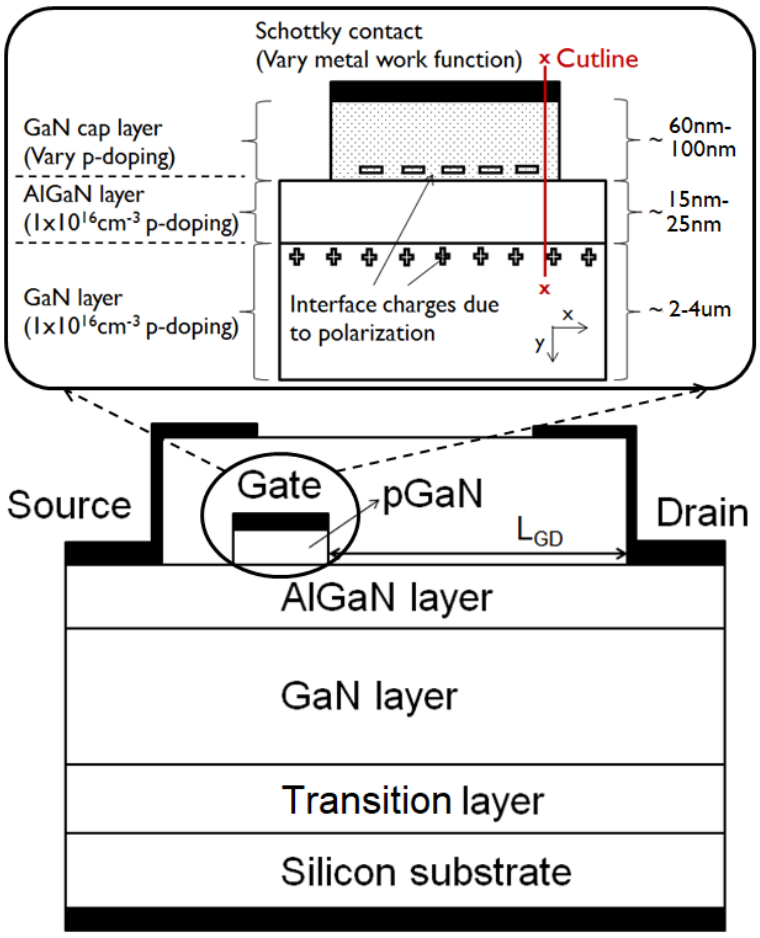


Fig. 6.1 Cross-section of p-GaN/AlGaN/GaN HEMT device modelled

the surface design of the device were provided by the device manufacturer allowing the TCAD model to be a very close physical representation of the actual device cross-section (not shown here due to confidentiality constraints). A more detailed look at the p-GaN/AlGaN/GaN gate structure can be seen in the inset of Fig. 6.1. A range of dimensions often used in devices is given so as not to reveal the specific device design. Some of the important parameters for matching are interface charges, p-GaN doping, GaN doping, Al mole fraction, AlGaN thickness, AlGaN dielectric constant, GaN electron mobility and gate dimensions (i.e. w/l).

Fixed charges were included in the TCAD simulation deck according to Ambacher et al. [38] to take into account the piezo-polarisation effect observed in GaN devices. A p-type doping of $3.5\text{x}10^{16}\text{cm}^{-3}$ was added in the GaN layer to take into account the carbon doping. Finally, a thin cap GaN layer was added to form the gate with a Magnesium(Mg) p-type doping density of $2\text{x}10^{19}\text{cm}^{-3}$. This doping value, also reported elsewhere in literature [48], matched the experimental results best. The very good

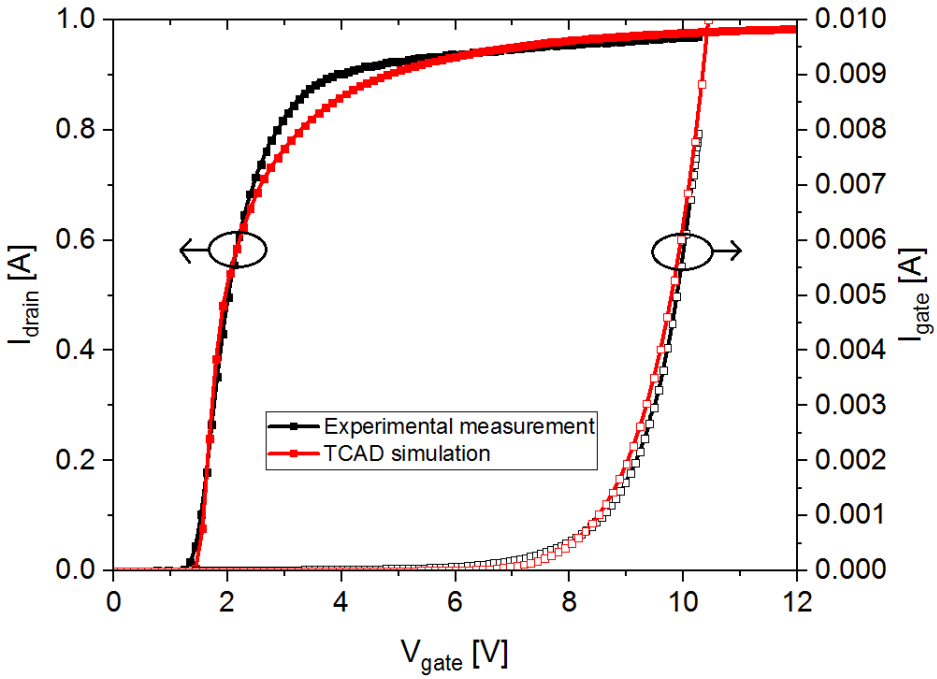


Fig. 6.2 Experimental measurements and TCAD simulations of I_dV_g and I_gV_g characteristic

match achieved between the measured I_dV_g and I_gV_g curves of the real device and the TCAD simulation model results can be seen in Fig. 6.2. To obtain the most accurate matching the effect of Mg out-diffusion from the p-GaN layer into the AlGaN/GaN layers beneath as described in [114] was taken into consideration.

Furthermore, it is worth discussing that at room temperature Mg doping is not fully ionized under zero bias conditions given its energy level at 170meV-250meV above the valence band [113] [115]. Nonetheless, incomplete ionization does not affect the Schottky barrier and the depletion region observed at the gate Schottky metal/p-GaN cap interface, both at zero bias and when the gate is biased, as activation of dopants occurs due to the presence of a large electric field. Therefore, in order to simplify the analysis the p-GaN doping included in the TCAD model is fully ionized. However, this does not fully consider that part of the Mg atoms may be passivated by Hydrogen(H) atoms [116] or that self-compensation may occur due to deep donor states attributed to Nitrogen(N) vacancies [117]. Nevertheless, it has been reported in literature that for [Mg]<$3x10^{19}cm^{-3}$ a doping efficiency in excess of 70% with a maximum net acceptor concentration of $1.8x10^{19}cm^{-3}$ can be achieved [118]. Thus, considering the constant efforts to enhance P-type activation in Mg-doped GaN [115][117][118] the simplification made here can be considered valid for the doping levels considered in this study. The

p-GaN cap acceptor doping and metal work function were varied in the analysis and the effect on threshold voltage and gate turn-on voltage were examined.

6.3 TCAD results and discussion

6.3.1 Variation of p-GaN doping and Schottky gate work function

The gate p-GaN cap acceptor doping in the TCAD model was varied first. Looking at the conduction band along x-cutline (as shown in the inset of Fig. 6.1) at zero bias it can be observed that as the doping is increased a stronger depletion of the 2DEG beneath the gate is created as the conduction band moves further away from the Fermi level (see Fig. 6.3). The variation in doping has a very significant effect on the threshold voltage of the device as seen in Fig. 6.4. As the doping initially increases, the threshold voltage of the device is also increasing (for doping values of $1x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$) however as the doping is increased further the threshold voltage starts decreasing (for doping values $>6x10^{18}cm^{-3}$).

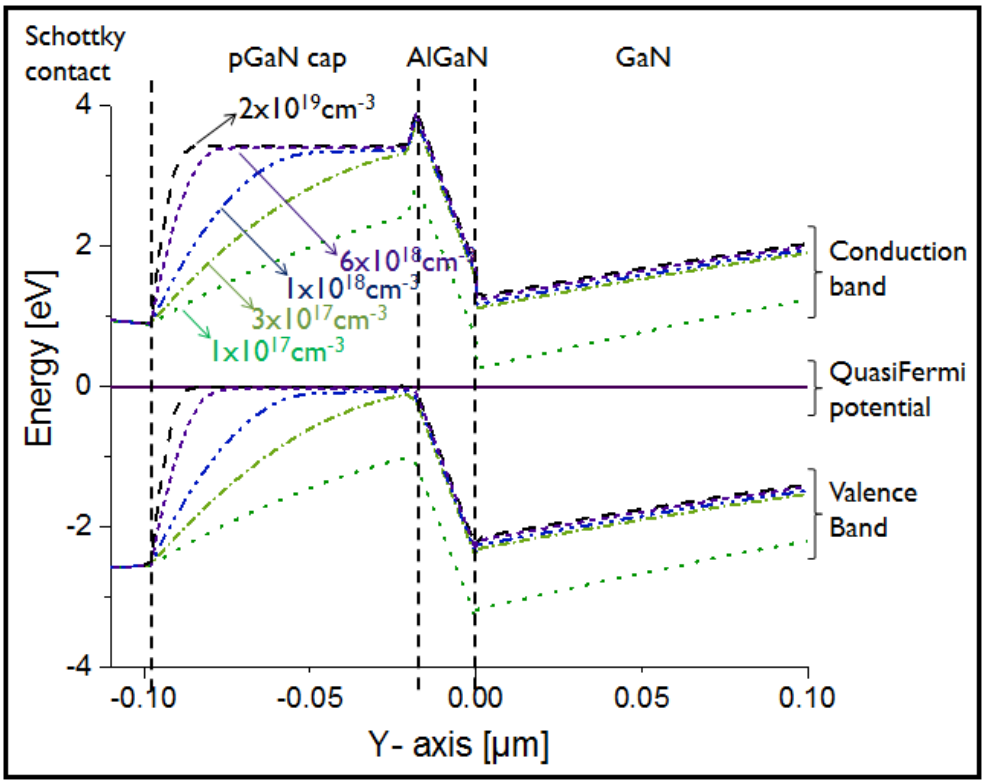


Fig. 6.3 Effect of p-GaN gate doping variation on band diagram at zero bias

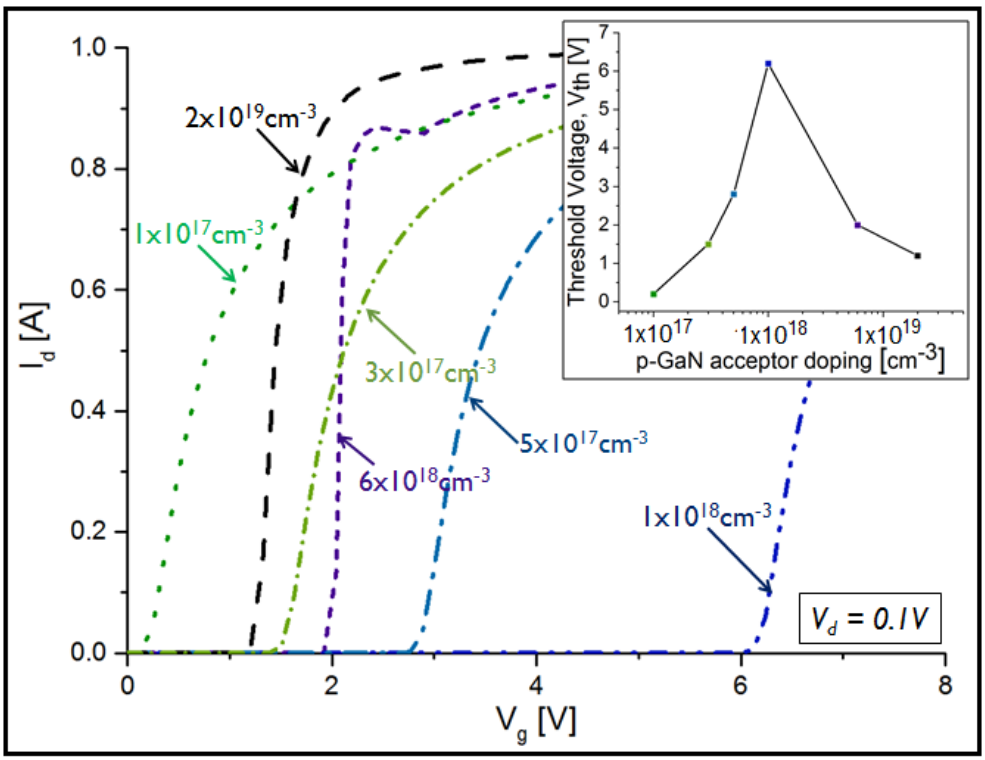


Fig. 6.4 $I_D - V_G$ transfer characteristic with variation in p-GaN gate doping (Inset: Device threshold voltage, V_{th} vs p-GaN acceptor doping)

To understand the variation of the threshold voltage with p-GaN acceptor doping the band diagram when the gate is biased needs to be examined. When a positive gate bias voltage is applied this can lead to two effects:

- One effect is to modulate the 2DEG. When potential is applied at the p-GaN/AlGaN/GaN junction, as seen in region (i) of Fig. 6.5, the energy of electrons at the AlGaN/GaN interface increases so the conduction band moves closer to the eFermi level forming the 2DEG.

- The other effect occurs at the Schottky/p-GaN interface which can be seen in region (ii) of Fig. 6.5. As the gate bias voltage is increased the junction is reverse biased and the depletion from the Schottky contact extends into the p-GaN.

The potential drop across this depletion region, when the gate is positively biased, is higher at increased values of the p-GaN cap acceptor doping. This translates into the need for a higher gate bias voltage in order to modulate the 2DEG and is what causes the threshold voltage of the device to initially increase when p-GaN doping is increased.

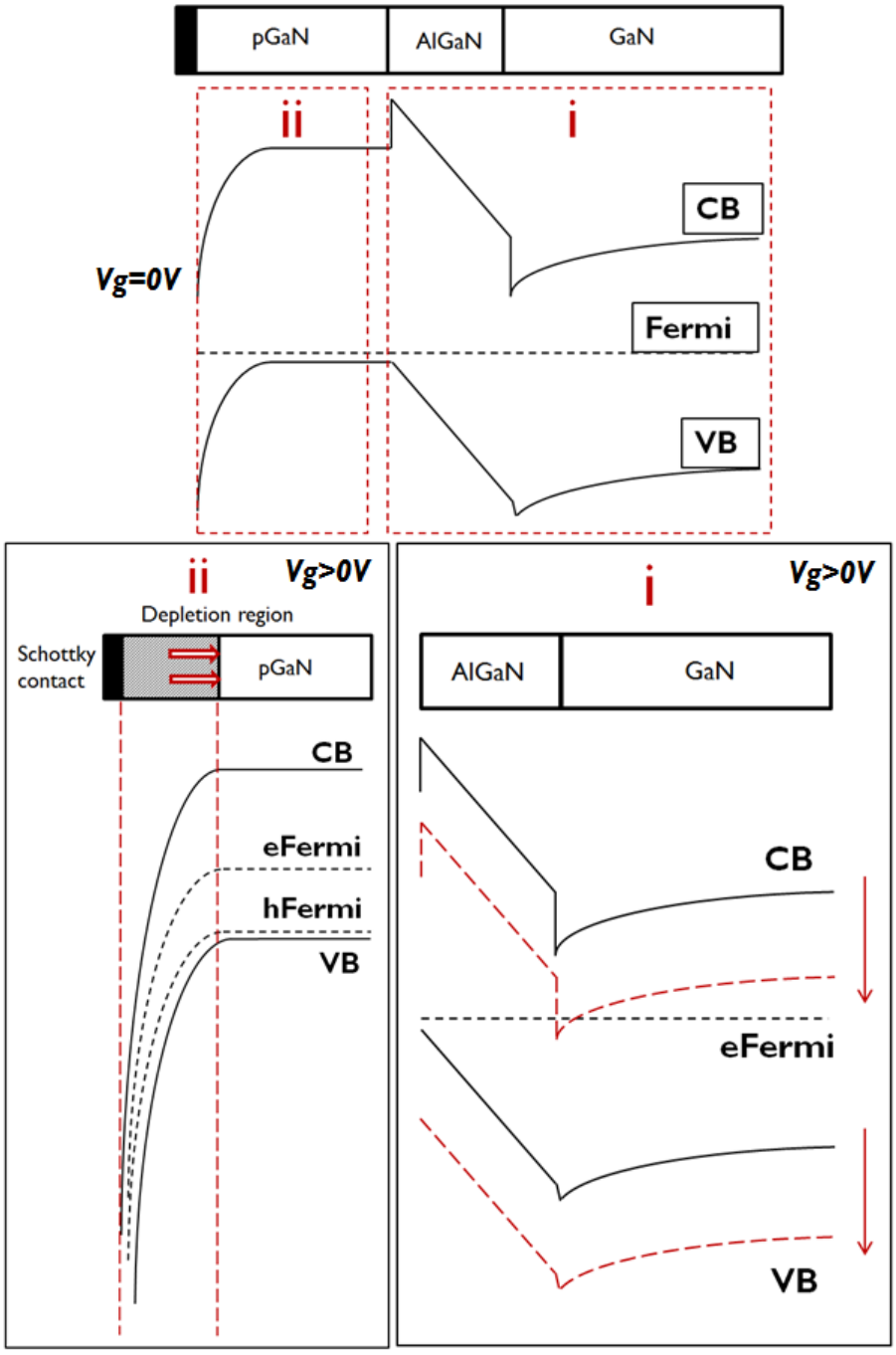


Fig. 6.5 Effect of gate bias on different sections of the gate structure band diagram (i) Schottky junction, (ii) AlGaN/GaN Heterojunction

However, at a sufficiently high acceptor doping in the p-GaN cap the potential barrier for holes at the Schottky contact/p-GaN interface becomes very narrow and this can lead to tunnelling of holes through the barrier. At this point, no further

depletion of the p-GaN layer occurs when the gate voltage bias is increased. Gate potential applied is no longer dropped across the depletion region in the p-GaN but contributes to the shifting of the AlGaN/GaN interface conduction band towards the Fermi level and thus the formation of the 2DEG at a lower gate bias voltage. Note that the p-GaN layer is electrically connected to the gate in this regime. Therefore, the threshold voltage is lowered ($V_{th} < 2V$) at high p-GaN doping values (>6x10^{18}cm^{-3}) instead of increasing further as was the trend observed initially. This analysis is illustrated best when looking at Fig. 6.6 which compares the band diagrams for a doping of 1x10^{18}cm^{-3} (negligible hole tunnelling current) and 2x10^{19}cm^{-3} (considerable hole tunnelling current) at a gate bias voltage of 3V. This analysis is further verified by not including the hole tunnelling model in the TCAD simulations. In this scenario, the threshold voltage keeps increasing as the doping is increased instead of decreasing when a p-GaN doping value above a certain level is used. The critical p-GaN acceptor doping level needed for substantial tunnelling to occur is dependent on the gate metal work function and the effective hole mass. The latter has been fixed to $0.3m_e$ according to Santic et al. [119][120]. A reduced gate metal work function would lead to a higher and narrower Schottky potential barrier for holes where increased tunnelling can be observed.

Very importantly, what this analysis also reveals, is that above a certain p-GaN doping level, variations in Schottky contact work function have a limited effect on the threshold voltage of the device (see Fig. 6.7 - TCAD model p-GaN doping: 2x10^{19}cm^{-3}) which can explain the observations in the study by Lee et al. [112] where a high p-GaN doping of 5x10^{19}cm^{-3} is used. A model with an Ohmic gate contact was also simulated and shows an identical threshold voltage to that given by the Schottky metal/high p-GaN doping models (see Fig. 6.7). This again reinforces the argument that a high level of tunnelling occurs at the Schottky/p-GaN interface.

6.3.2 Gate turn-on

The effect of p-GaN doping and gate metal work function on the gate turn-on voltage is also of interest in order to achieve as wide a gate bias operating range as possible. The band diagram at the AlGaN/GaN interface was analyzed as the gate terminal was biased to higher voltages (i.e. at Vg>3V>Vth). The analysis was undertaken for the TCAD model with high p-GaN acceptor doping (2x10^{19}cm^{-3}) as this matched the experimental device data.

Below the threshold voltage, the conduction band shifts towards the Fermi level with no electric field change across the AlGaN layer (see Fig. 6.5(i)). This occurs up to

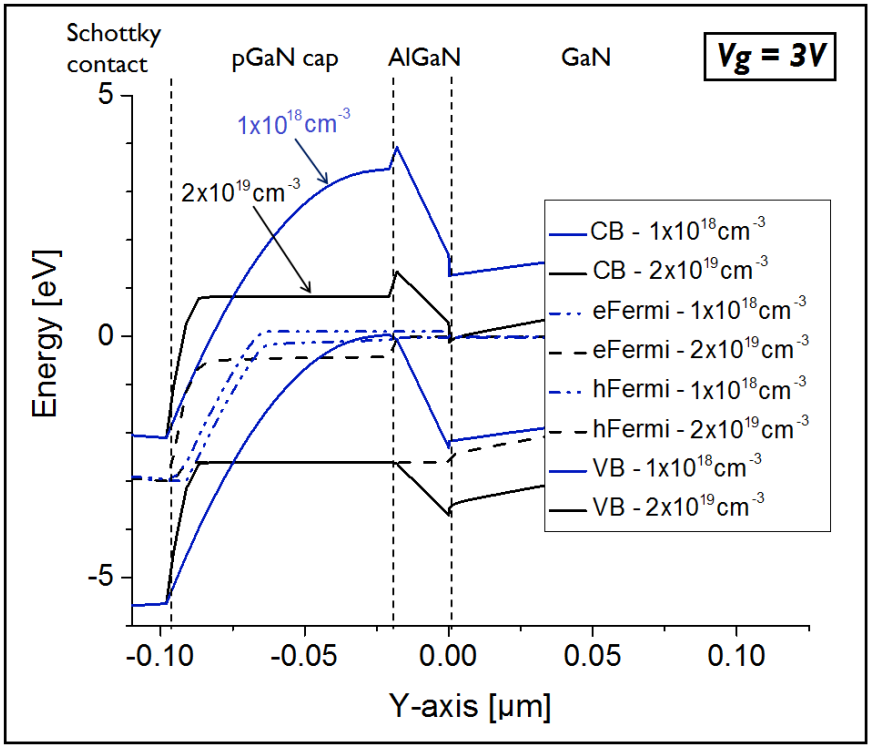


Fig. 6.6 Gate structure band diagram at gate bias of 3V for p-GaN doping of $1x10^{18}cm^{-3}$ (negligible hole tunnelling) and $2x10^{19}cm^{-3}$ (considerable hole tunnelling)

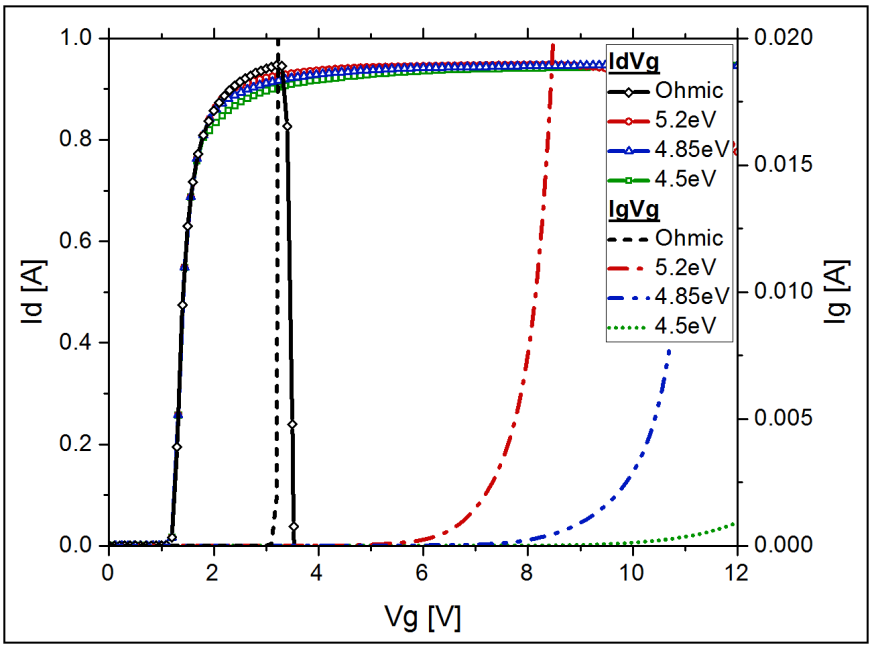


Fig. 6.7 $I_D - V_G$ transfer characteristic (solid lines) and gate turn-on (dotted lines) as gate metal work function is varied

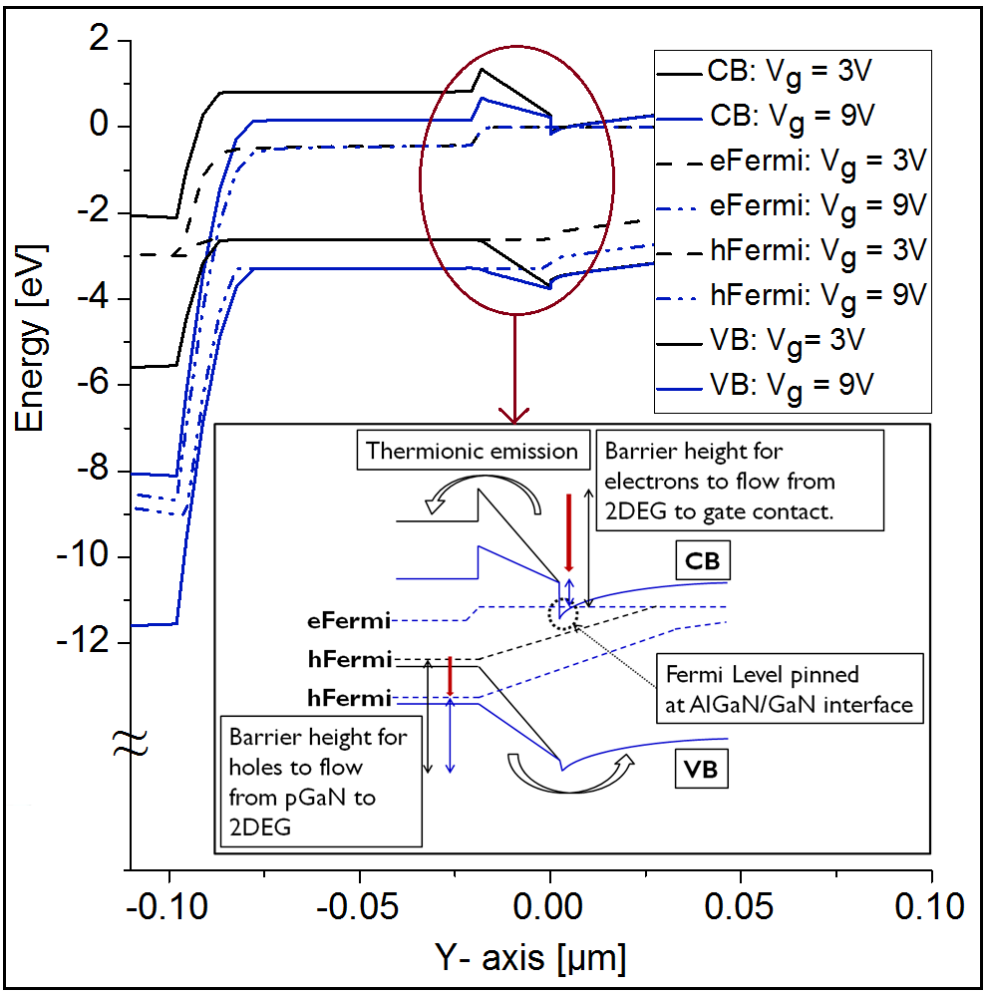


Fig. 6.8 Gate structure band diagram at gate bias of Vg= 3V, 9V > Vth for TCAD model with p-GaN doping of $2x10^{19}cm^{-3}$ (Inset: Conduction mechanism at the heterojunction barrier)

the point where the Fermi level is pinned at the AlGaN/GaN interface (see Fig. 6.8). As gate bias voltage is increased further, the barrier at the AlGaN/p-GaN interface starts to be lowered both for electrons flowing from the 2DEG to the gate contact and holes flowing away from the p-GaN. This is illustrated by observing the band diagram at two different gate bias conditions (Vg = 3V, 9V) as seen in Fig. 6.8. The majority of gate turn-on current is comprised of electrons flowing from the source contact to the gate contact. The following interesting observations can be made:

- The use of a Schottky contact compared to an Ohmic contact leads to a gate turn-on at a higher gate bias (see Fig. 6.7). With a Schottky gate contact a higher bias voltage is needed to reduce the potential barrier at the p-GaN/AlGaN

interface as a potential drop is also observed across the p-GaN cap layer depletion region. The use of a Schottky barrier in order to achieve a wide operating gate bias range is therefore essential and contradicts the suggestion regarding the use of an Ohmic contact in the study by Chang et al. [121].

- Gate turn-on in this device is at a gate bias $> 8V$ which allows a reasonably wide range of operation.

- A higher gate metal work function will lead to a lower gate turn-on voltage (see Fig. 6.7). This agrees with the observation made by Hwang et al. [113].

- For high p-GaN doping values ($>1x10^{19}cm^{-3}$), an increase in the acceptor doping will not affect the threshold voltage of the device but will affect the gate turn-on voltage.

6.4 Conclusions

In conclusion, TCAD simulations have been used to enable a thorough understanding of the operation of the gate structure of the p-GaN cap E-HEMT. Some very important design considerations are summarized below.

- As p-GaN doping initially increases the threshold voltage of the device is also increasing (for doping values of $1x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$) however, as the doping is increased further the threshold voltage starts decreasing (for doping values $>6x10^{18}cm^{-3}$). This is due to hole tunnelling at the metal/p-GaN interface establishing a tight electrical connection between the gate metal and the p-GaN layer.

- At high doping levels, the threshold voltage cannot be significantly altered by the use of a different gate metal. This finding provides clarity to the observations in the study by Lee et al. [112].

- A variation in gate metal used affects the gate turn-on voltage of the device. This agrees with the observation in the study by Hwang et al. [113].

- The use of a Schottky gate contact rather than an Ohmic gate contact is essential in order to achieve a wide operating gate bias range. This finding contradicts the suggestion given in the study by Chang et al. [121].

This study reveals the trends that need to be taken into consideration when designing the gate characteristics such that the gate operation range is maximized and the device operates in an optimal way.

The results discussed in this chapter are published in [122].

Chapter 7

Oscillatory Behaviour during Switching of normally-off GaN HEMTs

With Gallium Nitride (GaN) device technology for power electronics applications being ramped up for volume production, an increasing amount of research is now focused on the performance of GaN power devices in circuits. In this chapter, an enhancement mode GaN high electron mobility transistor (HEMT) is switched in a clamped inductive switching configuration with the aim of investigating the source of oscillatory effects observed. These arise as a result of the increased switching speed capability of GaN devices compared to their silicon counterparts. The study identifies the two major mechanisms (Miller capacitance charge and parasitic common source inductance) that can lead to ringing behaviour during turn-off and considers the effect of temperature on the latter. Moreover, the experimental results are backed by SPICE modelling to evaluate the contribution of different circuit components to oscillations. Furthermore, the analysis considers the parasitic components at the device level due to different layouts. It is indeed shown that these have a very significant effect on the switching capability. Some good design techniques that can suppress the effects discussed are also mentioned at both circuit and device level.

7.1 Introduction

In the last decade, an extensive amount of research has focused on the development of power devices using AlGaN/GaN heterostructures grown on silicon substrates. In

particular, efforts have focused on the development of enhancement mode switches in the 100-650V range. Devices with very competitive specific R_{on} compared to the latest silicon MOSFET Superjunction technologies [123] have been reported both in academia and industry, as can be seen in Table 7.1 [51][124].

	Si MOSFET Superjunction	AlGaN/GaN E-mode HEMT
Specific R_{on}	$10m\Omega cm^2$	$2m\Omega cm^2$

Table 7.1 State of the art Specific R_{on} of different technologies for a 650V device

Additionally, the use of GaN devices can lead to lower switching losses, thus allowing an increase in switching frequency and therefore an overall increase in power density and efficiency of power conversion equipment [100][125][126]. Therefore, with GaN device technology being ramped up for volume production an increasing amount of research is now focused on the performance of GaN devices in various power electronic converters such as, boost, buck-boost, half-bridge and indirect matrix inverter topologies [100][127][128]. This study focuses on the challenges circuit design engineers are presented with when using GaN devices and in particular focuses on how parasitic components can create oscillatory behaviour and therefore lead to additional circuit losses. Ways to optimise the gate drive circuit in order to achieve a robust design are also discussed. Two major sources of ringing are identified in literature [129], one of which relates to the device Miller capacitance and controlling the dV/dt rate and the other relates to the presence of parasitic common source inductance in the circuit. The effects of these mechanisms were examined for a 650V enhancement mode GaN HEMT by switching it in an inductive clamped switching configuration both at room and increased temperatures. Extensive SPICE simulations were used to support the analysis.

7.2 Device structure and characteristics

A normally-off HEMT device based on p-gate technology (see cross-section in Fig. 7.1) was used in this study. The device has a lateral configuration with an AlGaN/GaN heterostructure grown epitaxially on a silicon wafer. A buffer layer is used to allow a high quality GaN layer to be grown despite the significant lattice mismatch between GaN and Si as described in [111]. Finally, a thin cap GaN layer was added at the gate with a high p+ doping concentration to achieve normally-off operation. The device has an inter-digitated layout as shown in the schematic design in Fig. 7.2 and was

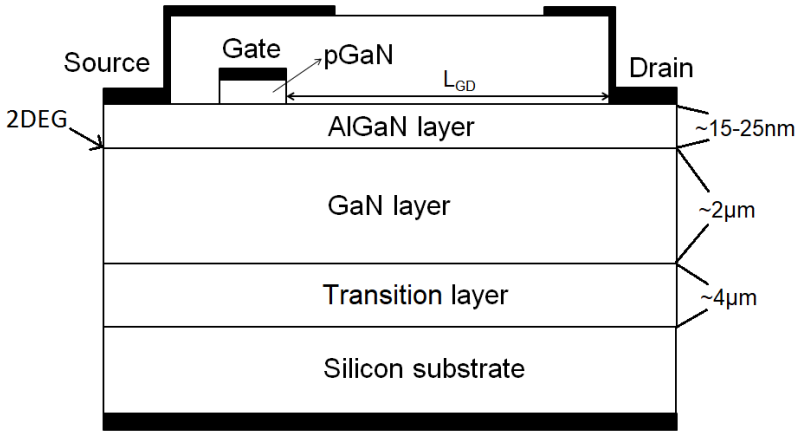


Fig. 7.1 AlGaN/GaN heterostructure p-gate enhancement mode HEMT cross-section

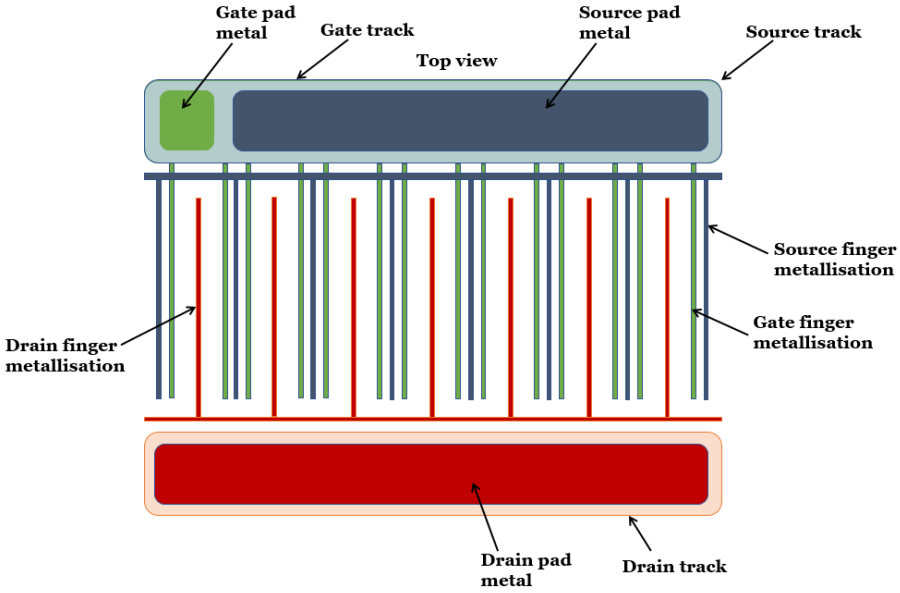


Fig. 7.2 AlGaN/GaN HEMT Inter - digitated layout

packaged in TO-220 before characterisation. The device has a voltage and current rating of 650V and 15A respectively and an R_{on} of $130m\Omega$.

The HEMT device under test differs from a silicon power MOSFET in several aspects. Conduction occurs through a two dimensional electron gas (2DEG) which is formed at the AlGaN/GaN interface [38]. High mobility of carriers ($\mu \approx 1700cm^2/(Vs)$) and a shorter drift region for a given breakdown due to higher critical electric field ($E_{br} = 3.3MV/cm$) [98] can lead to very low drift region charge, Q_{gd}. Furthermore, the device gate charge Q_g is measured to be $3.1nC$ compared to $35nC$ in corresponding state of the art silicon devices [130]. As a consequence the GaN HEMTs can switch

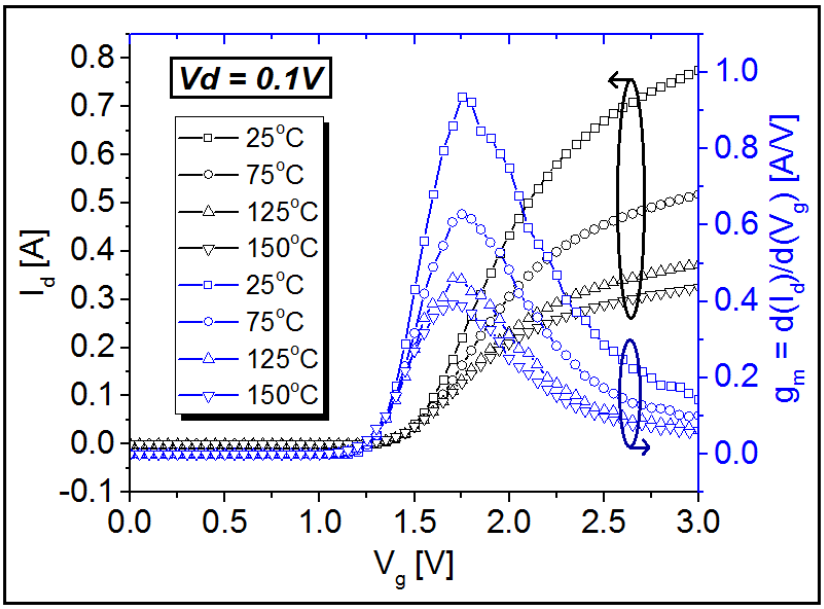


Fig. 7.3 GaN HEMT transfer characteristic and transconductance at room and increased temperatures.

at much higher speeds than silicon MOSFETs. A low threshold voltage close to 2V is typically observed in p-gate GaN HEMTs [48][112]. This is also the case in the device under test that shows a threshold voltage of 1.5V. Furthermore, substantial current leakage is observed through the gate contact at high V_g bias (>8V) due to the non-insulated gate structure [112] as opposed to a MOS-like gate. This results in a narrower operational gate bias window. The internal gate resistance, R_{gi} was measured to be 1.8Ω. An on-state gate bias voltage of 4V is applied to achieve minimum R_{on} and gate leakage. The transfer characteristic and transconductance of the device at a range of temperatures can be seen in Fig. 7.3.

7.3 Experimental method

Experimental measurements were carried out using a clamped inductive switching circuit that is shown schematically in Fig. 7.4[1]. The current and voltage waveforms were recorded with a Tektronix DPO5104 oscilloscope using a sample interval of 0.2ns. The circuit consists of an external gate resistance (this will be referred to as simply Rg as the same value was used for both Rgh and Rgl for all measurements) which in association with the internal resistance of the gate driver used (Rsink) has a large influence on

[1]The circuit was designed and built by Dr. Nishad Udugambola.

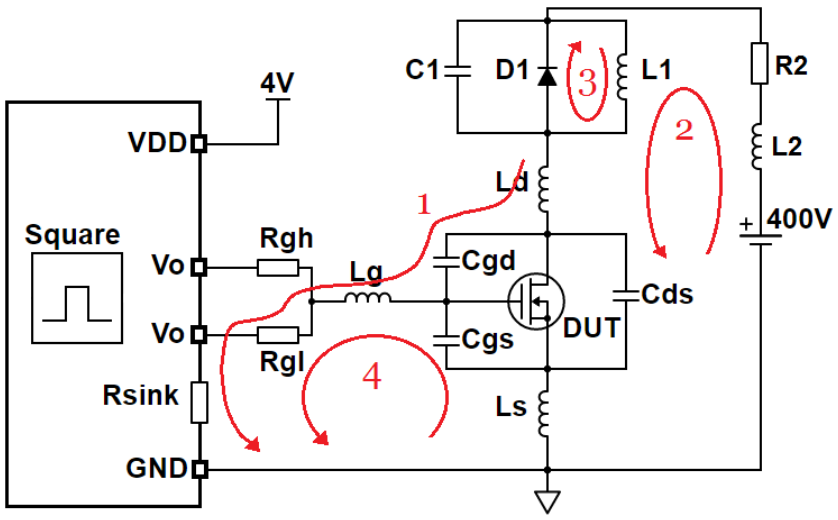


Fig. 7.4 Clamped inductive swithing circuit

the switching performance of the circuit by controlling the switching conditions (dI/dt rate, dV/dt rate). A high-speed MOSFET driver was used (Microchip TC4452V). The square pulse input to the gate driver was provided by an Agilent 33220A. The main inductor L1 ($500\,\mu H$) behaves as a constant current source. The HEMT characterised corresponds to the device under test (DUT) shown in the circuit. A silicon carbide diode (CREE C3D10060) was used as the clamping diode (D1). Gate voltage was measured with a Tektronix TPP1000 probe. Drain-source voltage was measured with a Tektronix TPP0850 probe. The drain current was measured with a TCP0030A current probe by inserting a wire-bridge in series with the DUT. Power source, circuit and sensing probe related parasitic inductances and capacitances are included in the schematic (C1, Ld, Lg, Ls, Cgd, Cgs, Cds, L2, R2). To obtain the measurements at increased temperatures the devices were heated in a custom made plastic oven placed on the board. The switching performance of the device was investigated during turn-on and turn-off using a double pulse test. A 400V off-state bias (V_{off}) was used and a range of on-state current values were obtained by adjusting the gate drive pulse width.

A Spice model for the device under test was developed based on a core provided by GaN systems for a 650V, 15A E-HEMT (GS66504B) and used in LTspice. The model consists of a sub-circuit rather than a physical model (which would provide more accuracy) and has been chosen to allow ease of convergence and simplicity in the simulations. A schematic of the Spice model sub-circuit is given in Fig 7.5. A detailed analysis of the operation of the Spice model provided by GaN Systems will not be given here.

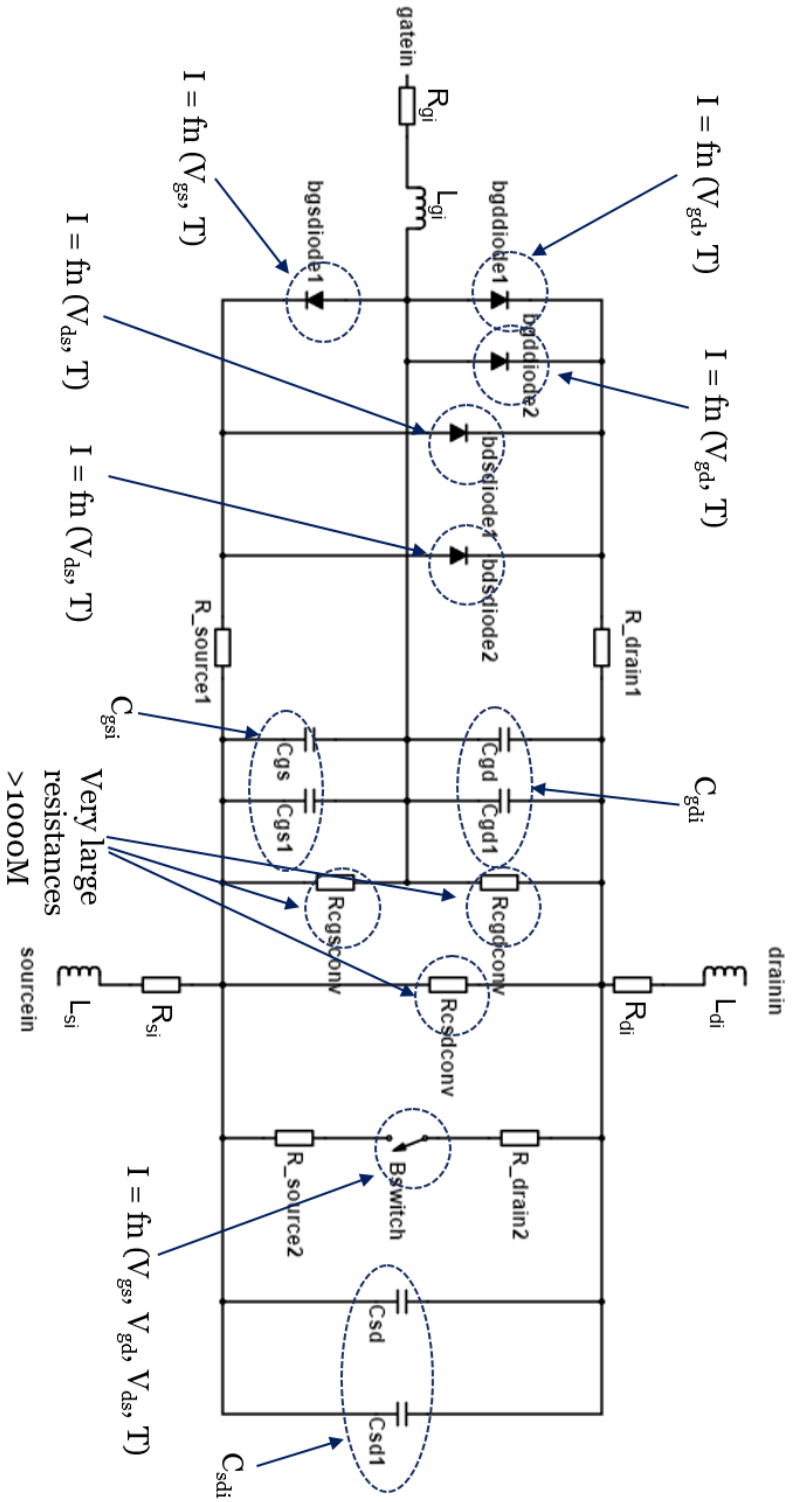
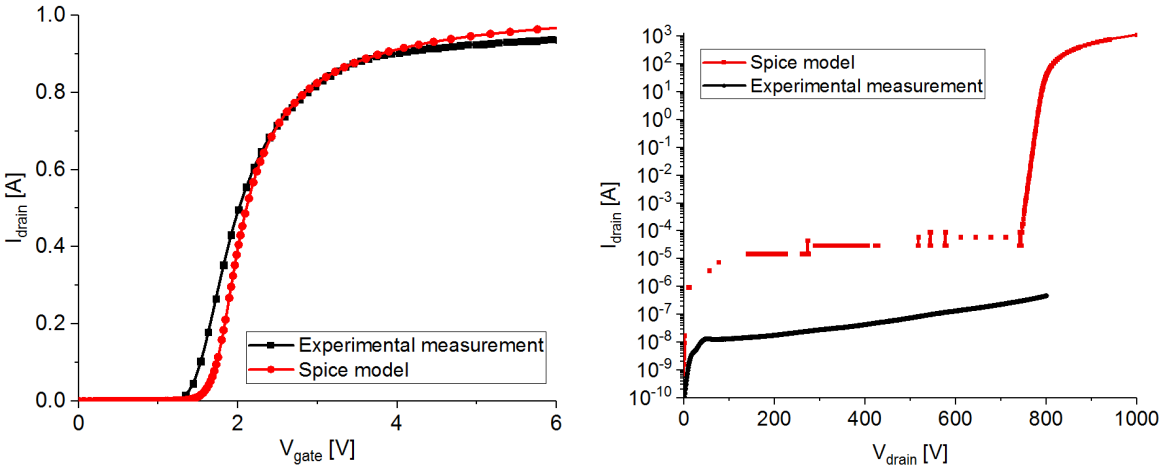


Fig. 7.5 Spice model sub-circuit schematic



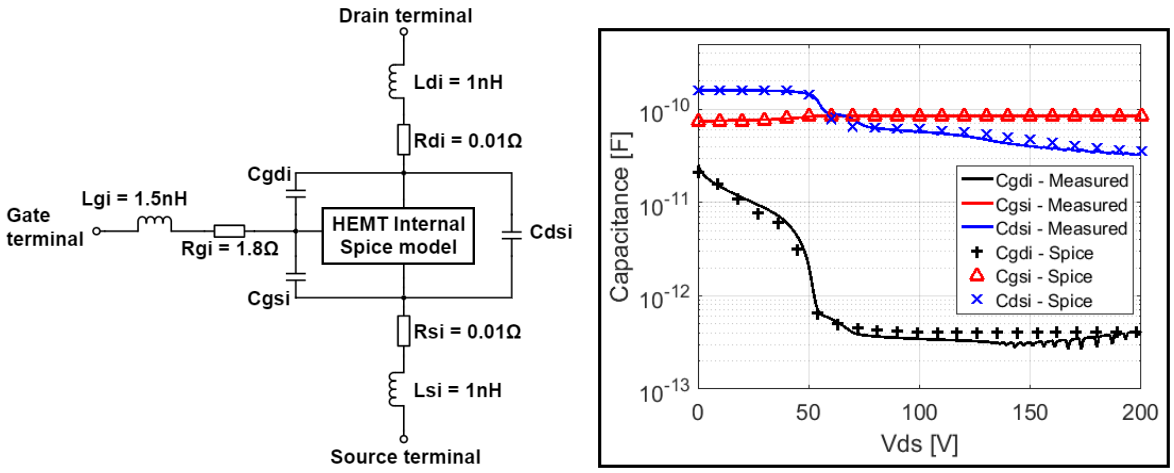
(a) Transfer characteristic (b) Off-state leakage

Fig. 7.6 GaN HEMT measured and Spice model characteristics

A fairly good match was achieved between the measured transfer characteristic of the device and the Spice model transfer characteristic as shown in Fig. 7.6. The off-state leakage was overestimated in the Spice model (see Fig. 7.6) however this has no effect on the investigation of the switching performance. Nonetheless, adjustments were made to the internal parasitic inductances (Lgi, Lsi, Ldi) and resistances (Rgi, Rsi, Rdi) of the three terminals and the voltage-dependent device capacitances (Cgdi, Cgsi, Cdsi) as illustrated in the schematic in Fig. 7.7(a). These components are the result of device design and, as such, are specific of a given technology. Parasitic inductances and resistances were estimated through measurements and simulations (Ansys Q3D extractor). Device capacitances were measured using a Keithley 4200 parameter analyser and are plotted in Fig. 7.7(b). Theoretical equations which describe the device capacitance-voltage curves were fitted to the measurements (see Fig. 7.7(b)) and implemented in the Spice model.

7.4 Results and Discussion

The increased switching speed of GaN devices leads to higher dV/dt and dI/dt values and can make the circuit more susceptible to oscillatory behaviour. This section focuses on discussing the origins of the oscillations observed, first analysing the relevant effects during device turn-off and then extending the analysis to cover the turn-on. Understanding these effects is a very important step in producing a circuit and device design unaffected/or less affected by oscillations.



(a) HEMT DUT spice model (b) Measured and Spice model capacitance

Fig. 7.7 SPICE model parameters adjusted

7.4.1 dV/dt related effect

During device turn-off the drain voltage is rising steeply. A high dV/dt causes a current to flow through the Miller capacitance (C_{gd}) and then Rg as illustrated by path 1 in Fig. 7.4. A sufficiently high voltage drop across Rg can turn the device on during switching and cause oscillations [129]. Furthermore, as the voltage rises above 400V the diode turns on abruptly changing the current path in the circuit (from loop 2 to loop 3 as seen in Fig. 7.4) thus creating oscillations as energy is transferred between the passive components in the two current loops. Any ringing in the power loop is also coupled to the gate terminal via the Miller capacitance. These effects were observed very clearly in both experimental results and Spice simulations.

The waveforms in Fig. 7.8a refer to the simulation of the circuit in Fig. 7.4 and will be used as a reference for the following analysis. The reference values for components in the circuit are as follows: Rg = 68Ω, Lg = 2nH, Ls = 3nH, Ld = 40nH (note that this includes the parasitic inductance contribution from the current sensing probe used to measure Id), Cds = 10pF, Cgd = 8pF, Cgs = 5pF, C1 = 20pF, L2 = 40nH, R2 = 0.5Ω. In the reference curves it is important to note the negligible ringing on all waveforms. Nonetheless, the switching current level in the reference curves is fairly low (2A) and, as will be described in section 7.4.2, the current level plays a significant role in the ringing behaviour observed. Furthermore, it is worth pointing out that the starting value of external gate resistance (Rg) used in the model is quite significant. Rg was therefore subsequently modified and its impact on the switching waveforms was studied. Rg was initially decreased from 68Ω to 50Ω. This had a significant effect

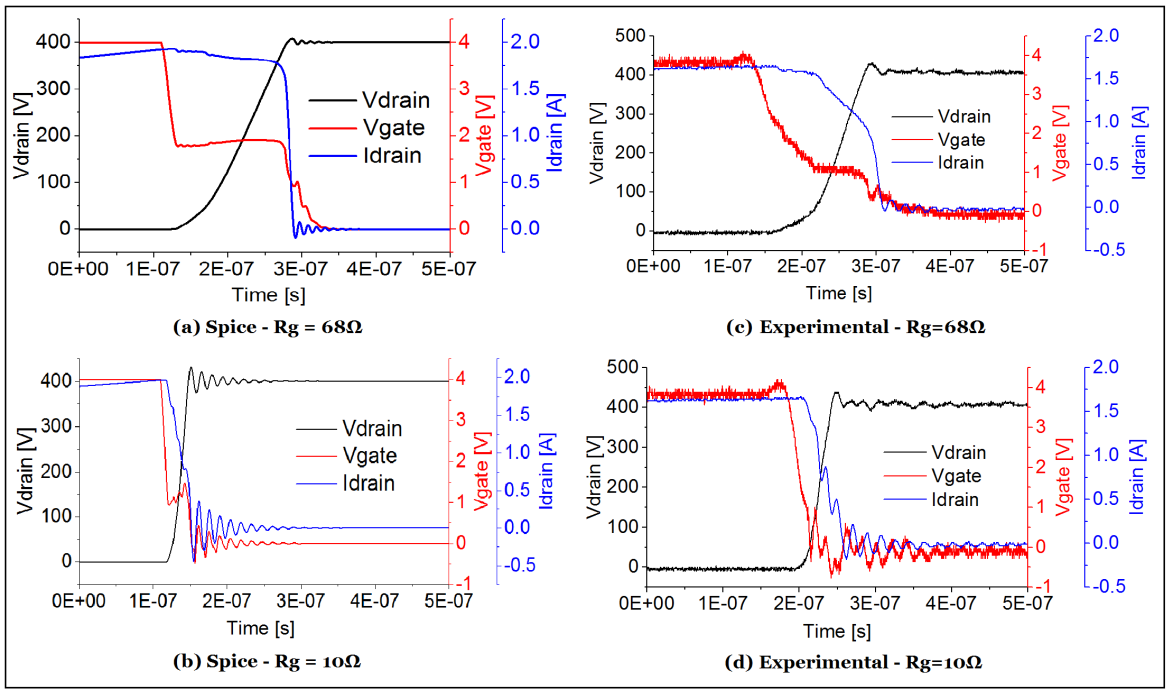


Fig. 7.8 Spice simulated and experimental HEMT turn-off waveforms: (a) Spice - Rg = 68Ω, (b) Spice - Rg = 10Ω, (c) Experimental - Rg = 68Ω, (d) Experimental - Rg = 10Ω

on the drain voltage dV/dt which increased from 4.7V/ns to 6V/ns. Furthermore, the gate waveform shows a shorter plateau and a slight drain voltage overshoot. However, no significant ringing is observable (not shown here). As the gate resistance is further decreased to 10Ω a very high dV/dt (26V/ns) results in an overshoot of the drain voltage during turn-off and ringing on the drain current. The ringing is coupled on the gate signal through C_{gd} and oscillatory behaviour is also observed on the gate terminal as seen in Fig. 7.8b.

The same trend was observed when the gate resistance was varied in the experimental circuit. An additional gate resistance (Rg) of 68Ω produced a dV/dt of 6V/ns which is close to the simulated value and a clean waveform was recorded as seen in Fig. 7.8c. When the resistance was reduced to 10Ω the dV/dt rate increased to 17V/ns and ringing was observed as seen in Fig. 7.8d. A good match was achieved between experimental measurements and Spice simulations. Note that the resistance of the driving circuit R_{sink} needs to also be considered in this analysis. A second driver (Microchip TC4432V) was used in this study with different current capability/sink resistance. The second driver with higher sink resistance allowed turn-off without ringing with a lower additional gate resistance.

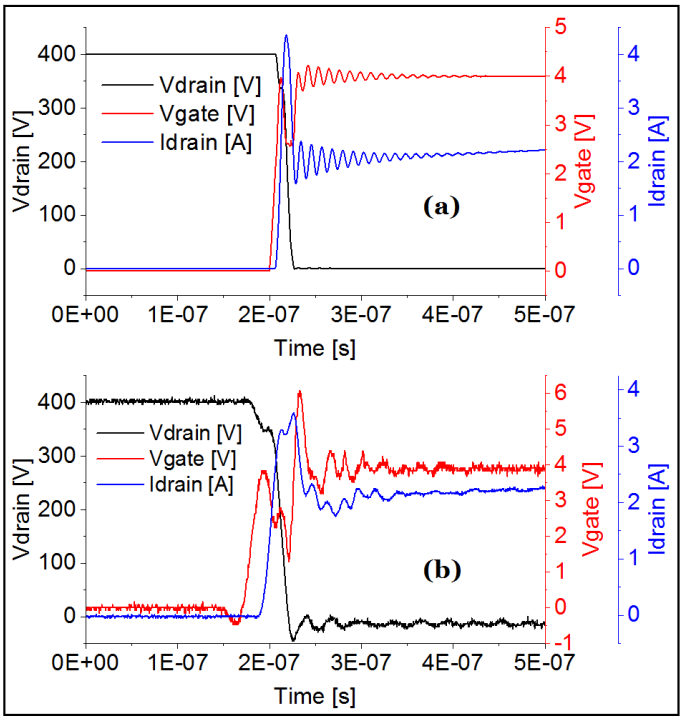


Fig. 7.9 HEMT turn-on waveforms with Rg = 10Ω (a) Spice simulation, (b) Experimental

The same source of oscillations was observed during device turn-on. A higher dV/dt rate is observed during turn-on both experimentally (22V/ns) and in Spice simulations (36V/ns). A good match was again achieved between Spice simulations and experimental measurements as seen in Fig. 7.9. A spike is observed in both gate current and drain current. Since a gate voltage spike can damage the device if operated close to the maximum gate bias rating, its possible maximum value should be taken into consideration when choosing a suitable gate drive bias. It is worth mentioning that a slight discrepancy between the measured and simulated oscillation frequency is observed in Figs. 7.8 and 7.9. This relates to the values of the parasitic components in the power loop (L2, C1, Ld) which may not be fully accounted for in the Spice model.

7.4.2 dI/dt related effect

A second area of concern arises from the formation of a LCR resonant tank comprising the common source inductance (L_s), gate capacitance, and gate drive pull down loop as seen in path 4 of Fig. 7.4. This resosnant circuit needs to be damped in order to avoid an equivalent positive voltage ringing across the gate [129]. L_s is therefore identified as a critical parameter for good performance. During turn-off, dI/dt coupled with L_s

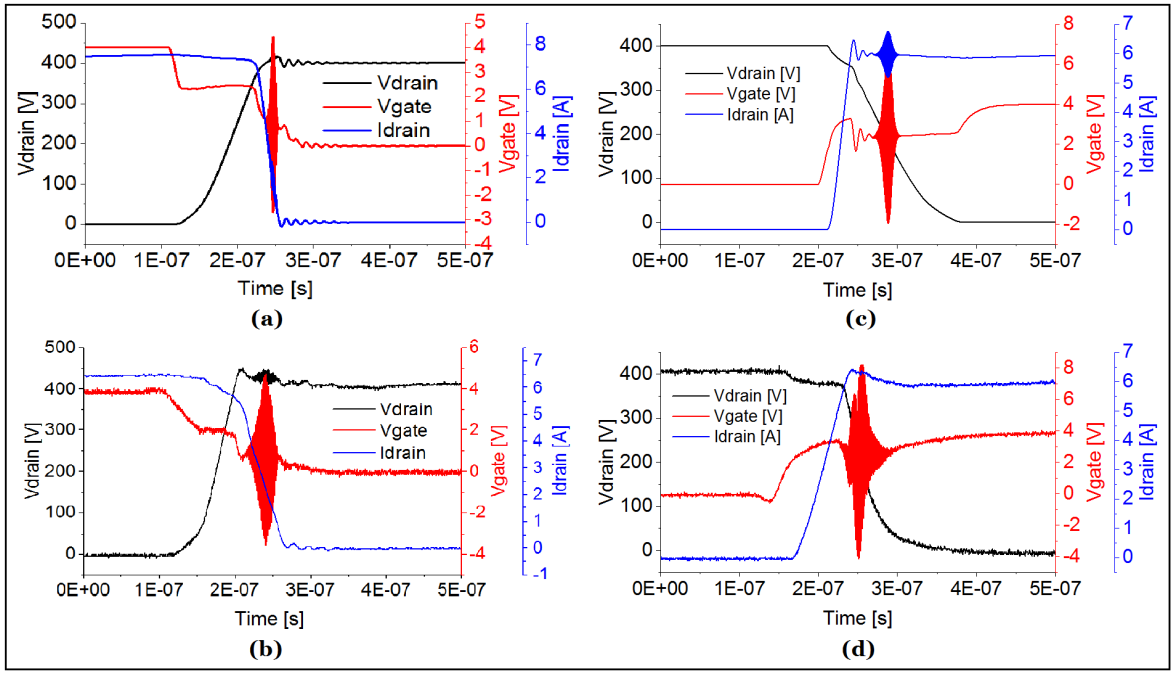


Fig. 7.10 *dI/dt* related oscillations in Spice simulated and experimental HEMT turn-off and turn-on waveforms: (a) Spice turn-off, (b) Experimental turn-off, (c) Spice turn-on, (d) Experimental turn-on

causes a considerable voltage drop to develop across the inductance with the source voltage V_s swinging negative when referenced to ground. This voltage drop can be seen on the gate voltage waveform (note this is Vg-ground) at the end of the plateau where *dI/dt* is at its peak ($300A/\mu s$) as seen in Fig. 7.8. This gate swing would not be observed without the presence of L_s as an ideal RC gate discharge would be expected (not shown here). This swing is also observed in the experimental turn-off of the device (see Fig. 7.8c) and suggests the presence of a considerable L_s.

Starting again from the reference circuit described in section 7.4.1 oscillations arising from the gate loop LCR resonant tank were observed when the switching current level in the Spice simulation model was increased (from 2A to 7A) as seen in Fig. 7.10a. Similar oscillatory behaviour was observed in experimental measurements as can be seen in Fig. 7.10b. Oscillations commenced only as the switching current level was increased due to higher current leading to faster *dI/dt* (I_d = 6.5A, *dI/dt* = 90A/μs). Ringing is observed primarily on the gate voltage (V_g) as shown in Figure 7.10(a), with a frequency of approximately 600MHz. These oscillations could turn the device back on during switching creating additional losses that can raise the temperature via self-heating and eventually cause reliability problems. In addition, slight oscillations are observed in the simulated drain voltage and current which increase in amplitude

as the switching current level is increased further. It is important to highlight that oscillations on the current waveform observed in the simulations may not be observable in experimental measurements due to the bandwidth of the current probe used. In fact, the current probe used in this experiment had a maximum bandwidth up to 120MHz while the frequency of the oscillations as measured from the drain voltage ringing is approximately 700MHz, which is very close to the simulated value. To verify the cause of the oscillations in the experimental circuit, a parasitic inductance in the form of a wire was added between source and ground. This led to ringing becoming much more severe and appearing at lower current levels as expected. The same trend was observed when Ls was more easily varied in the Spice model (not shown here).

The turn-on of the device was also investigated under these conditions and oscillations were again observed both experimentally and in Spice simulations as seen in Figs. 7.10c and 7.10d. In a similar manner to the turn-off, the turn-on associated oscillations were found to be dependent on the *dI/dt* rate. During the turn-on, however, the *dI/dt* rate was found to be higher than during turn-off (I_d = 6A, dI/dt = 105A/μs) leading to oscillations generated at a lower current level than during turn-off. The difference in the dI/dt rate observed during turn-on and turn-off can be understood by solving for the transient duration analytically using an equivalent device gate circuit as described in [131].

Increased Temperature

The effect of temperature on oscillations caused by the parasitic common source inductance was also investigated. It is observed that the maximum current level that can be switched without the presence of ringing increases with increasing temperature. Fig. 7.11 shows switching at a current level of 5A where ringing is observed at room temperature but no such ringing is observed at a temperature of 150^oC. It is interesting to note the appearance of oscillations at a lower current level compared to Fig. 7.10b. These turn-off measurements were taken using a second HEMT device with a higher internal parasitic inductance further confirming the analysis in section 4.2. The *dI/dt* rate is lower at increased temperature and falls to 66A/μs compared to 81A/μs at room temperature. This could be a result of the increase in gate metallisation resistance observed at increased temperature and can thus be the reason behind the improved stability observed at higher temperature. Furthermore, as observed in Fig. 7.3 the transconductance in the device is reduced at increased temperatures and this can also account for a reduction in oscillations observed as demonstrated in [132]. It is therefore important to understand that in this instance, a self-heating effect created by

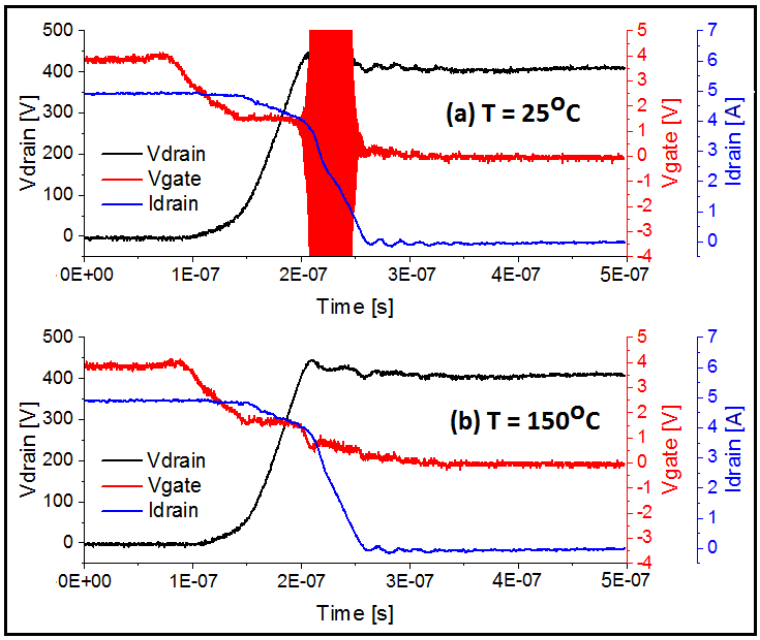


Fig. 7.11 Effect of temperature on experimental turn-off waveforms of HEMT device

the presence of oscillations which can lead to additional losses, can act as to reduce the oscillations present when switching. Nonetheless, self-heating can lead to other adverse effects such as increase in device R_{on}, increased probability for time dependent dielectric breakdown and higher overall losses.

7.4.3 Good design suggestions

Optimising gate drive circuit to address dV/dt related ringing

An optimised circuit is more immune to ringing caused by dV/dt effect as discussed in section 4.1 if:

- $R1$ is high enough to control dV/dt, but not too high to generate a significant voltage drop when the discharge current of C_{gd} is flowing through. A trade-off is thus revealed. To allow stable switching the rate of switching of the device needs to be reduced however this can lead to increased losses.

- Smart driving is used such as an active Miller clamp function as seen in commercially available drivers (e.g. Fairchild FOD8318). This function avoids a large C_{gd} discharge current flowing through $R1$ by grounding the gate through the turn-on of a transistor when a certain voltage is developed across $R1$.

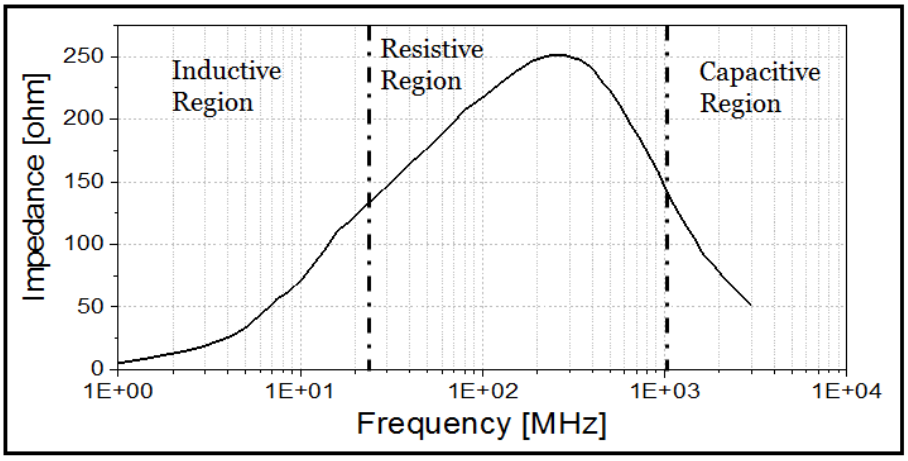


Fig. 7.12 Ferrite bead impedance against signal frequency

- Gate inductance L_g is minimised as Spice simulations reveal that gate inductance acts as to increase the amplitude of the oscillations observed. This is a result of the storage of energy when current is flowing through L_g.
- The gate is driven to a negative voltage at turn-off to ensure unwanted device turn-on is avoided. This can however add cost and complexity to the design [133].

Use of ferrite bead to address dI/dt related ringing

As discussed in section 7.4.2 it becomes apparent that to achieve a good design it is essential to reduce L_s as much as possible. Nonetheless, other solutions that can lead to a more robust design should also be considered. Increasing the gate drive sink resistance can help damp the LCR resonance. That could, however, create other issues as described in section 7.4.1. The addition of a ferrite bead that is resistive at the resonant frequency can achieve the same result with less increase in Miller turn-on sensitivity [129]. A ferrite bead exhibits three response regions: inductive, resistive and capacitive depending on the signal frequency as can be seen in Fig. 7.12 [134]. The appropriate ferrite bead has to be chosen in order to be resistive in the range of frequency at which the oscillations occur. A ferrite bead by Tai Tech Advanced Electronics was used in the experimental set-up [135]. A Spice model for the particular component was not available so the model of a ferrite bead with similar characteristics by Wurth Electronics was used in the Spice simulation circuit [136].

The effect of the bead in successfully damping the oscillations observed was verified using both the Spice circuit and experimental measurements. In the Spice model, the

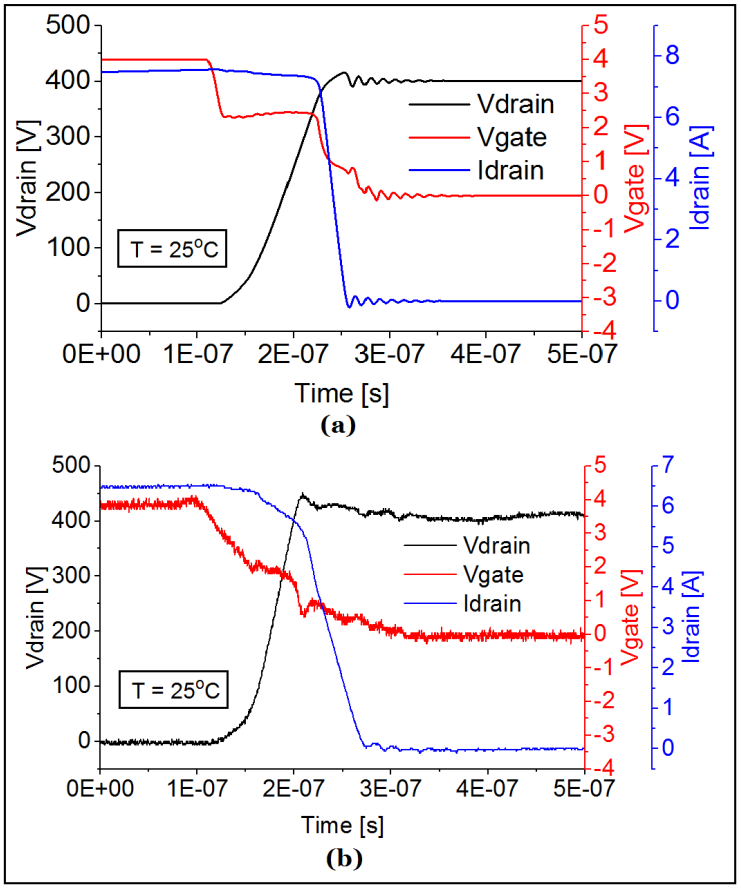


Fig. 7.13 Effect of ferrite bead on ringing observed in (a) Spice simulated and (b) experimental circuit turn-off waveforms seen in Figs. 7.10a and 7.10b

ferrite bead was added to the gate track and optimized for the frequency at which oscillations were observed (600MHz). The resulting waveform can be seen in Fig. 7.13a.

In the experimental circuit the bead was placed around the gate leg of the TO-220 package of the device. The resulting switching turn-off waveform can be seen in Fig. 7.13b. Oscillatory behaviour was successfully eliminated in both the experimental results and the spice simulations illustrating the effectiveness of the ferrite bead.

7.5 Effect of internal parasitics

So far it has clearly been demonstrated that with the very fast switching that can be achieved with GaN HEMTs, significant oscillatory behaviour can be an issue due to circuit level parasitics. The analysis can be extended further to take into account the effect of device level parasitics. This effect was revealed when additional devices

with different layouts were tested. The different layouts used can be seen in Fig. 7.14 and 7.15. The active area cross-section of these devices is identical to the one shown in Fig. 7.1 and were also packaged in TO-220. The basis of the layout is again an interdigitated finger structure however the connections of the different terminals to the fingers and the contact pads connecting the device to the package vary in these designs.

Fig. 7.14 shows the first of the additional test devices. This design will be referred to as Source-Drain-Source (SDS) layout. The source connection runs around the outside of the active area with the gate finger connection also running on the outside beneath the source connection as multiple metal layers are utilized. The source contact pad for package connection is only placed on the top side as seen in Fig. 7.14. The gate contact pad on the other hand is placed both at the top and bottom as seen in Fig. 7.14. Drain contact to the fingers is made through the middle with the active area divided into two sections. This configuration is a conventional lateral high voltage device design with the high voltage terminal (drain) surrounded by low voltage terminal (source). Fig. 7.15 shows the second of the test devices which will be referred to as Drain-Source-Drain (DSD) layout. In this design the drain connection runs around the outside of the active area and is connected to the package through a contact on the top section. Source and gate finger connection is now made through the middle. It is important to point out that while the finger length is divided in half in SDS and DSD layouts compared to the SD layout the total device gate width remains constant. Nonetheless, the device area is increased compared to the SD design due to the additional connections present in the SDS and DSD designs. Furthermore, the series resistance is increased in SDS and DSD design due to the additional connection path. A comparison of the transfer characteristic per unit gate width and per unit area is seen in Figs. 7.16 and 7.17 respectively. SD layout as expected has a lower R_{on} per unit gate width and even more significantly a lower R_{on} per unit area.

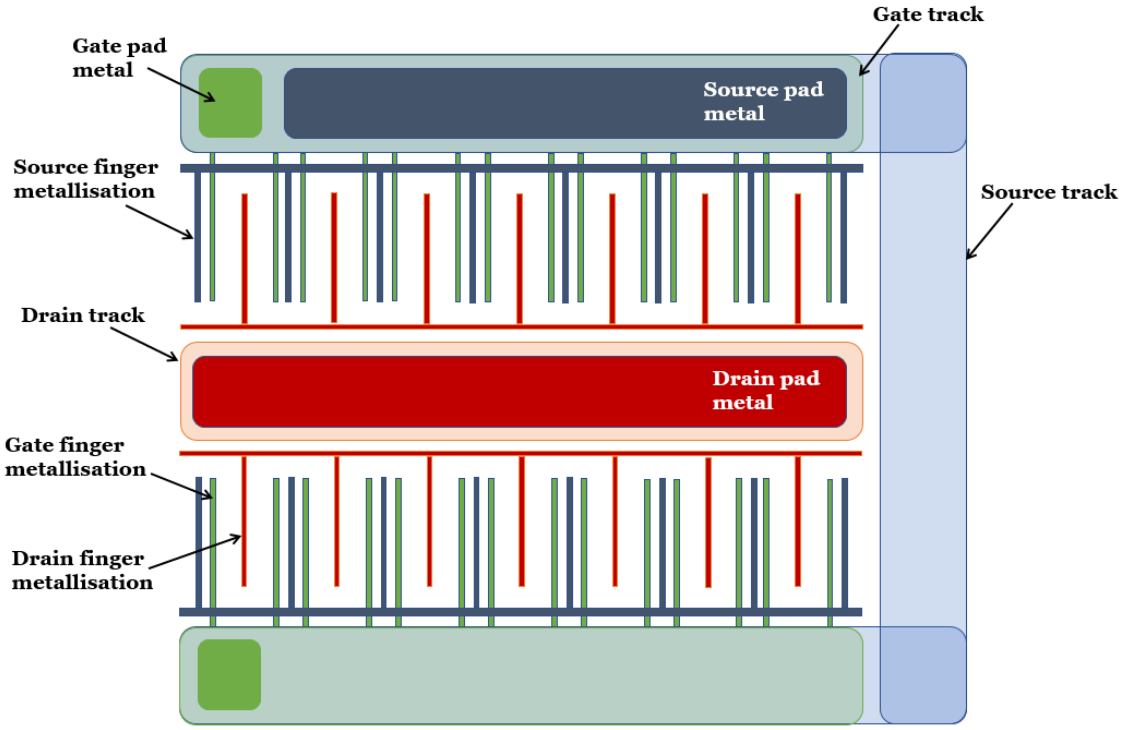


Fig. 7.14 Source-Drain-Source layout of a high voltage HEMT

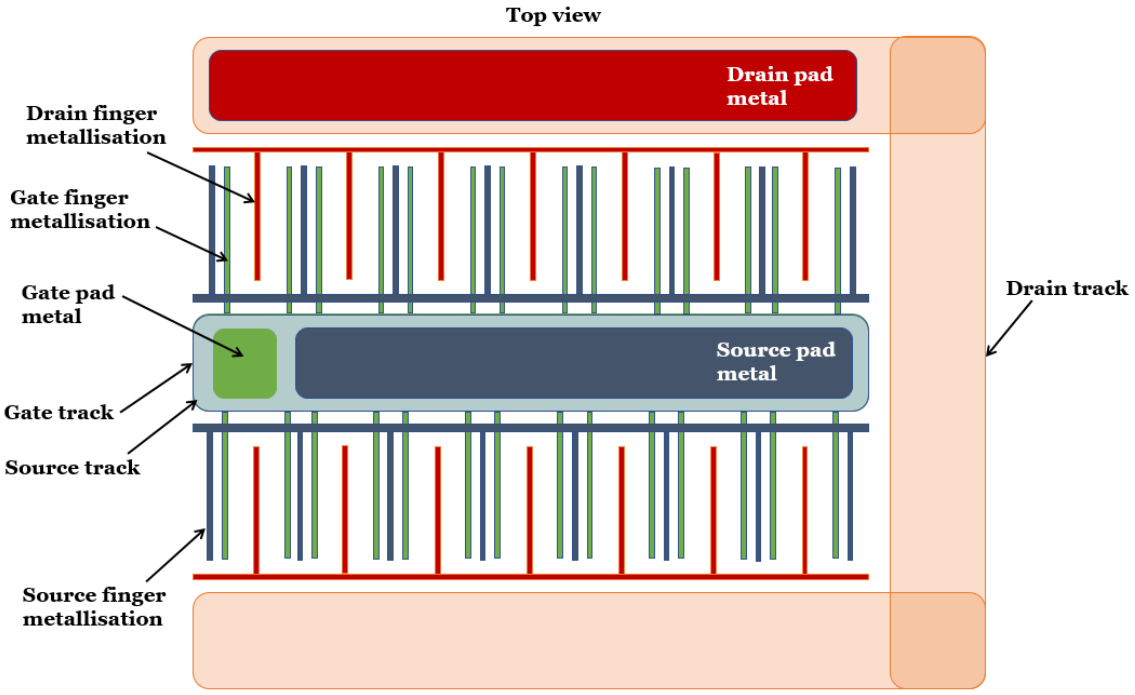


Fig. 7.15 Drain-Source-Drain layout of a high voltage HEMT

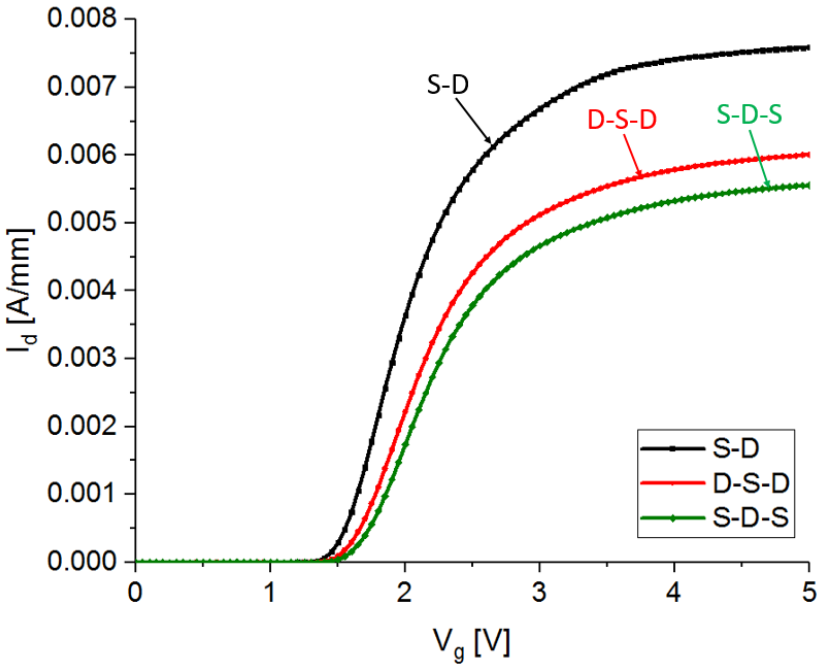


Fig. 7.16 Transfer characteristic comparison of different layouts with y-axis as current per unit gate width

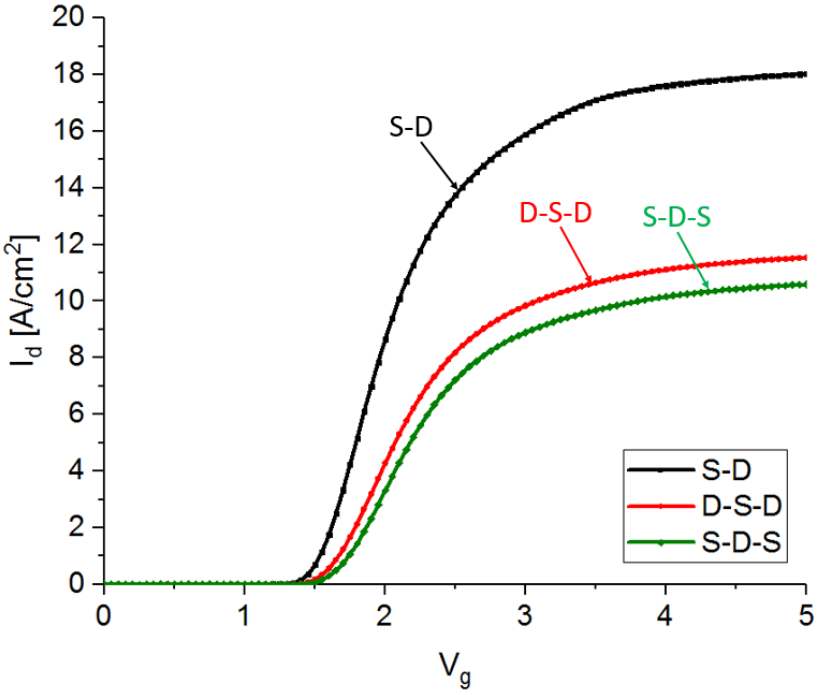


Fig. 7.17 Transfer Characteristic comparison of different layouts with y-axis as current per unit area

7.5.1 Switching capability

While SD appears to be the best solution when considering just the device on-state current capability, it was observed that changes in the device layout had an effect on the device switching capability. The same setup that was described in section 7.4.1 was used to switch the devices. The switching current was gradually increased until dI/dt related oscillations were observed during device turn-off. The current at which oscillations were first observed for the three layouts (SD, SDS, DSD) are summarized in Table 7.2.

Table 7.2 HEMT switching

	Driver	R_g	S-D		S-D-S		D-S-D	
1	TC4452V	68Ω	$5A$	$98.7A/cm^2$	$7A$	$110.9A/cm^2$	$13A$	$207.4A/cm^2$
2	TC4432V	10Ω	$2A$	$39.5A/cm^2$	$3A$	$47.5A/cm^2$	$8A$	$127.6A/cm^2$

DSD and SDS layout were found to switch without oscillations at higher currents compared to the SD design. Table 7.2 illustrates two scenarios where different gate drivers and external gate resistances were used as specified. While the current that was switched without oscillations differs in the two scenarios as expected taking into account the earlier analysis, the trend in the switching performance for the three different designs remains the same. With switching scenario (1) the DSD device was switched close to the device maximum current rating without any problem.

The difference in the switching capability of the three devices with different layouts can be explained when looking at the parasitic source inductance that arises from each design. As pointed out earlier, the source pad is only placed at the top in the SDS design. The group of fingers at the bottom end thus see an additional inductance when conducting current due to the source connection track. The poor performance of the SD design can be accounted for when considering that the length of the fingers in this design is twice the size of the fingers in the other two designs which leads to additional inductance to be present per finger. The DSD design which performed the best has both shorter fingers and a shorter package/contact pad/finger source connection which minimises the source inductance observed. In the DSD design the drain pad is only placed on one side and thus the device will have an increased drain inductance due to the additional connection track. This however does not lead to the same problems that increased source inductance causes.

7.6 Conclusions

Two major issues, dV/dt and dI/dt induced oscillations that arise as a result of the increased switching speed capability of GaN devices compared to their silicon counterparts are identified experimentally and successfully modelled in Spice. These issues were revealed by investigating the turn-off and turn-on of a GaN E-HEMT device during a double pulse test in a clamped inductive switching configuration. Limiting the current through the device Miller capacitance and therefore a control of the drain voltage rise (dV/dt) during turn-off are essential in achieving a good circuit design. Furthermore, the need to minimise the common source inductance in order to avoid severe ringing on the gate waveform is also demonstrated. The use of a ferrite bead in order to damp the oscillation observed has also been illustrated. Additionally, it is shown that more robust switching is possible when the device operates at an increased temperature. The self heating effect is, in this respect, beneficial as it can reduce the oscillations. Finally, through the switching of various devices with different layouts in the same circuit it is illustrated that device level parasitics associated with the different layouts can affect the device switching performance. The main issue is again the presence of a common source inductance.

The results discussed in this chapter are published in [137].

Chapter 8

Bonding pad over active area (BPOA) layout for lateral AlGaN/GaN HEMTs : a critical view

This chapter investigates the advantages and disadvantages of bonding pad over active area (BPOA) layout over a conventional layout (e.g SD layout in Chapter 7) for lateral AlGaN/GaN HEMTs designed for use in power applications. Extensive analysis of the performance of a BPOA device, both experimentally and supported by 3-D TCAD model simulations, reveals that while it can offer a higher current capability per unit area it can lead to other disadvantages compared to a conventional design when considering reliability aspects and the switching behaviour.

8.1 Introduction

An extensive amount of research has focused on the development of power devices using AlGaN/GaN heterostructures. Bonding Pad over active (BPOA) layouts have been suggested as a design feature that can improve current density in lateral AlGaN/GaN heterostructure devices and studies which show competitive on-state and off-state characteristics for such structures can be found in literature. [80] reports the use of a BPOA layout for an AlGaN/GaN power diode with excellent on-state and off-state characteristics while [81] reports the improvement of on-state current density by utilizing a BPOA structure for a normally-on HEMT device. [82] describes the use of

a photosensitive poyimide (PSPI) dielectric layer instead of the more commonly used SiO_2 between the active semiconductor area and the bonding pad of a normally-off HEMT device; the study reports a reduction in the chip size by 50% without an increase in leakage current compared to the conventional design and no issues with the packaging. In this chapter the on-state, off-state and switching performance of a fabricated BPOA layout normally-off HEMT device is presented to illustrate the relative advantages and disadvantages of this design when compared to a device with a conventional layout. Furthermore, an analysis of the factors that may lead to poorer reliability in BPOA layouts is undertaken using TCAD model simulations; such an investigation has not been reported, to the author's knowledge, elsewhere in literature. In particular, attention is focused on the electric field peaks observed in the inter-metal dielectric (SiO_2) when the device is biased in the off-state. Such field peaks are relevant when designing devices which are intended to be resilient to time dependent dielectric breakdown (TDDB) [138][139].

8.2 Device Structure

Devices investigated in this study are described in this section. The devices used have the same cross-section as the normally-off HEMT device described in Chapter 6 with regards to the dimensions of the semiconductor layers and the surface contacts. The device metallisation and dielectric layers however differ for the two layouts (BPOA and conventional) that were produced for comparison. Fig. 8.1 shows a schematic design of these layouts. Both layouts employ an identical finger structure with the difference observed in the placement of the contact pads. The device referred to as the conventional layout here is the SD device described in more detail in Chapter 7. SiO_2 layers were used as the inter-metallisation dielectric and both BPOA and conventional devices were packaged in TO-220 before characterisation. The devices have a voltage, current rating of 650V, 15A. A TCAD model of the HEMT structure was built and matched with experimental results such that it can be used in the reliability analysis as will be discussed in more detail in section 8.4.1.

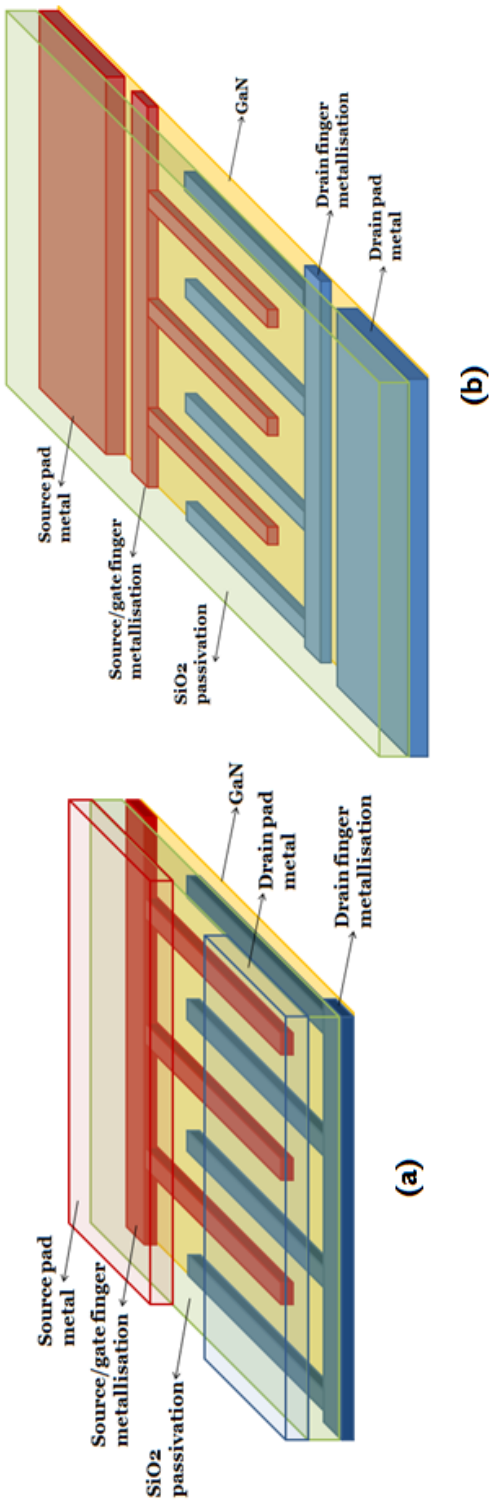


Fig. 8.1 Device layout (a) BPOA, (b) Conventional

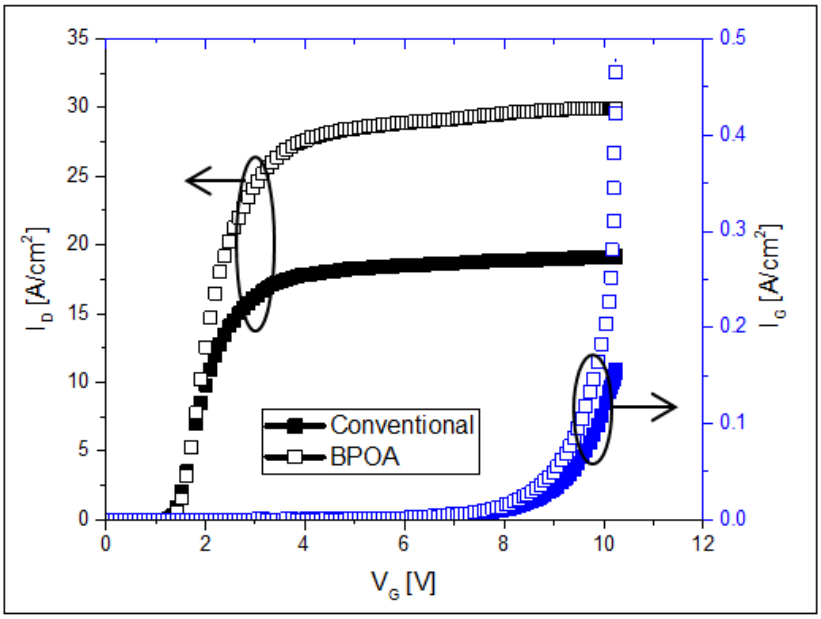


Fig. 8.2 On-state comparison between AlGaN/GaN heterostructure p-gate enhancement mode HEMT with BPOA vs conventional design

8.3 Experimental Results

The on-state, off-state and switching performance of the BPOA HEMT were compared to those of the conventional design. The transfer characteristics and gate turn-on of the two devices are shown in Fig. 8.2. BPOA structure shows higher current capability per unit area as expected while the current capability between two devices per unit gate width was the same. Off-state leakage of the two different devices can be seen in Fig. 8.3. BPOA structure shows higher leakage per unit area as expected. But again the leakage per unit gate width between the two devices is very similar suggesting a high quality inter-metallisation dielectric in the BPOA structure which does not lead to additional leakage paths.

The switching performance of the device with a BPOA layout versus a device with a conventional design was investigated. Turn-off curves were recorded with a single pulse measurement in a clamped inductive switching configuration. The switching circuit used was the one described in detail in Chapter 7. The driver and gate resistance used were the ones in scenario of Table 7.2. Switching was performed at a voltage of 400V and a current level of 2.5A. Switching current was limited well below the device current rating as already large oscillations are observed when switching the BPOA design which could permanently damage the device or the switching circuit used. (see Fig. 8.4). No such issues are observed with the conventional pad design (see

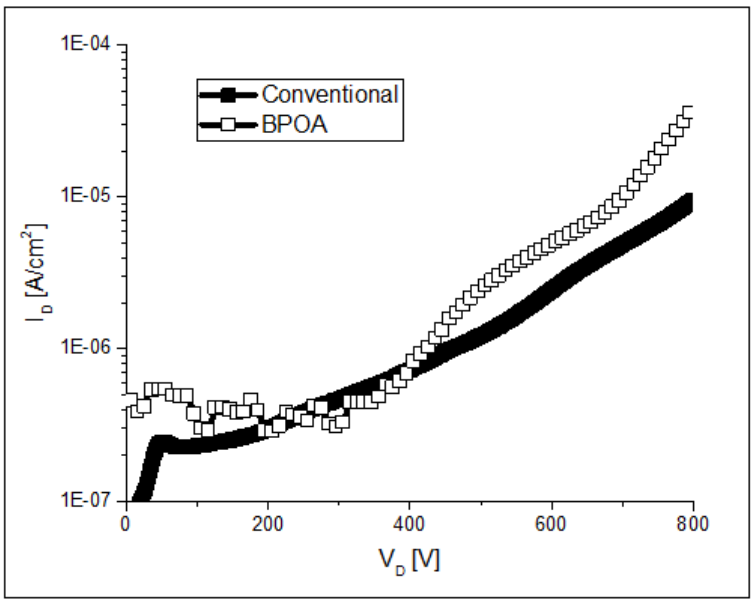


Fig. 8.3 Leakage comparison between AlGaN/GaN heterostructure p-gate enhancement mode HEMT with BPOA vs conventional design

Fig. 8.5) until a significantly higher switching current was reached (5A). The origin of the very poor switching performance of the BPOA device is not very clear and further research in this area needs to be undertaken. A couple of ideas which could explain this observation are listed below:

- The BPOA TO-220 package was produced with the pins in a GSD configuration rather than the standard GDS configuration which is used more commonly. The circuit described in Chapter 7, which was used to switch the BPOA design (and the conventional design), was produced with a test socket connected to accommodate the GDS configuration. Thus, in order to allow switching of the BPOA design, a small additional wire was added to the drain pin such that it was placed between the gate and source pin. The wire was intentionally added to the drain terminal as such a wire would add additional inductance which, as analysed, can lead to severe oscillations if present on the source terminal. Nonetheless, this arrangement through the introduction of additional parasitics could lead to the large oscillations observed rather than the layout itself. A near identical circuit which accommodates the GSD design could be produced for a fairer comparison. Additionally, a package with the BPOA design packaged in GDS could be produced such that it can be used in the current testing circuit.

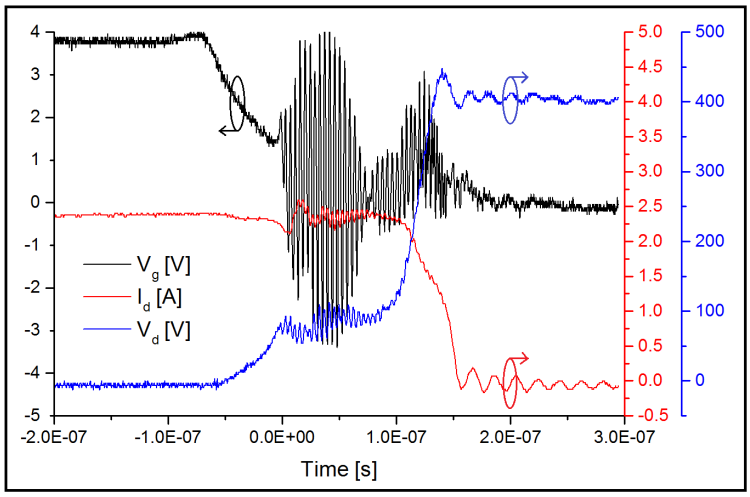


Fig. 8.4 BPOA layout HEMT clamped inductive switching. (400V, 3A)

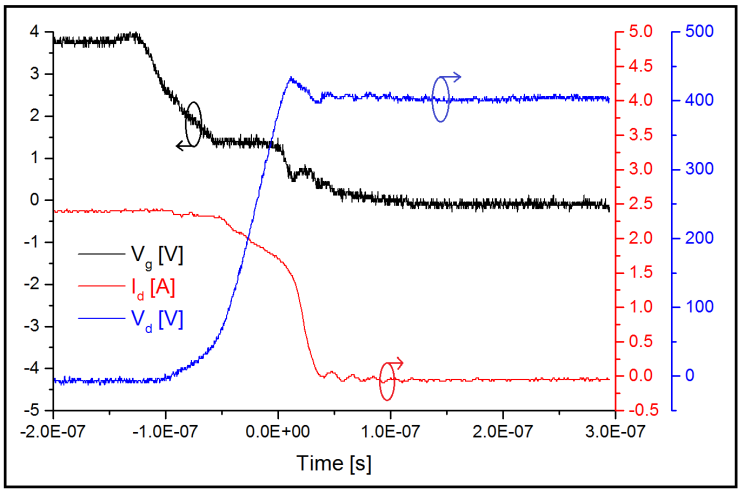


Fig. 8.5 Conventional layout HEMT clamped inductive switching. (400V, 3A)

- The BPOA design could lead to increased electromagnetic interference between the high voltage (drain) and low voltage (source/gate) terminals due to the presence of the bonding pads over the active area. This could be quantified through the use of an electromagnetic simulator such as ANSYS Maxwell. This could be a very interesting extension to this work[1].

[1]This is recommended as future work at the end of this thesis (see Chapter 9)

8.4 Reliability analysis

8.4.1 TCAD Model

Thus far, the comparison in performance of the two devices reveals the current density advantage of the BPOA-HEMT device but also points to some problems in switching when compared to the conventional design. To complete the analysis, the possibility that the BPOA layout might lead to reliability concerns was also examined.

This concern arises as bonding pads over the active area change the way in which the potential is distributed in the structure when biased compared to a conventional structure. This is of greater interest when the device is biased in the off-state as high electric field peaks in the semiconductor can lead to breakdown. Nonetheless, high electric fields cannot only harm the semiconductor but also the inter-metallisation dielectric layers used (SiO_2) and can lead to reliability issues such as time dependent dielectric breakdown (TDDB). To reduce the risk for TDDB, the electric field peaks in the dielectric layer must be minimized.

To investigate this, a model of an AlGaN/GaN HEMT, as described in Chapter 6, was built in Sentaurus TCAD platform and matched with the fabricated device. For this particular examination the model was extended in the third dimension which was done to capture more accurately the electric field distribution in the device. The capability of developing a 3D model was important as will become apparent later in this analysis. The section of the device modelled can be seen in Fig. 8.6. Some significant features of the model are illustrated such as the second metallization layer which is acting as a field plate and is also needed to reduce finger resistance. The dimensions of the SiO_2 passivation are reproduced according to the dimension provided by the foundry. It is important to note that the AlGaN layer and surface contacts cannot be seen in Fig. 8.6 due to their very small dimensions compared to the rest of the device. In the analysis that follows cross-sections which are not to scale will be produced for better understanding.

The section in Fig. 8.6 was chosen as it captures the critical locations of the device and all the areas where the field distribution may differ compared to a conventional device. TCAD model off-state simulations were performed to identify locations of electric field peaks in the structure both in the semiconductor layers and the SiO_2 passivation.

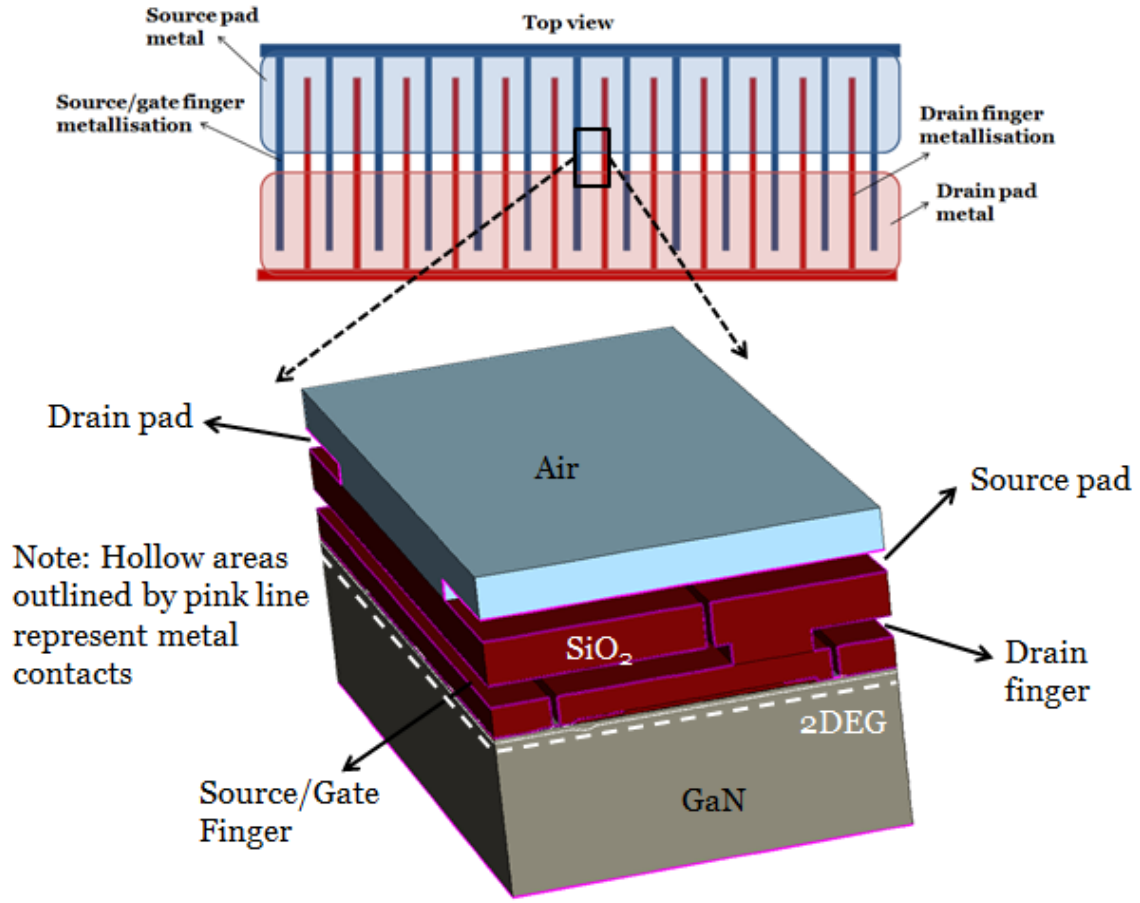


Fig. 8.6 3D TCAD model of bonding pad over active (BPOA) structure

8.4.2 Off-state simulations

A closer look at the BPOA structure reveals that a distinction can be made between three different sections of the device as seen in Fig. 8.7. These are as follows:

- No pad over active area (NPOA)
- Drain pad over active area (DPOA)
- Source pad over active area (SPOA)

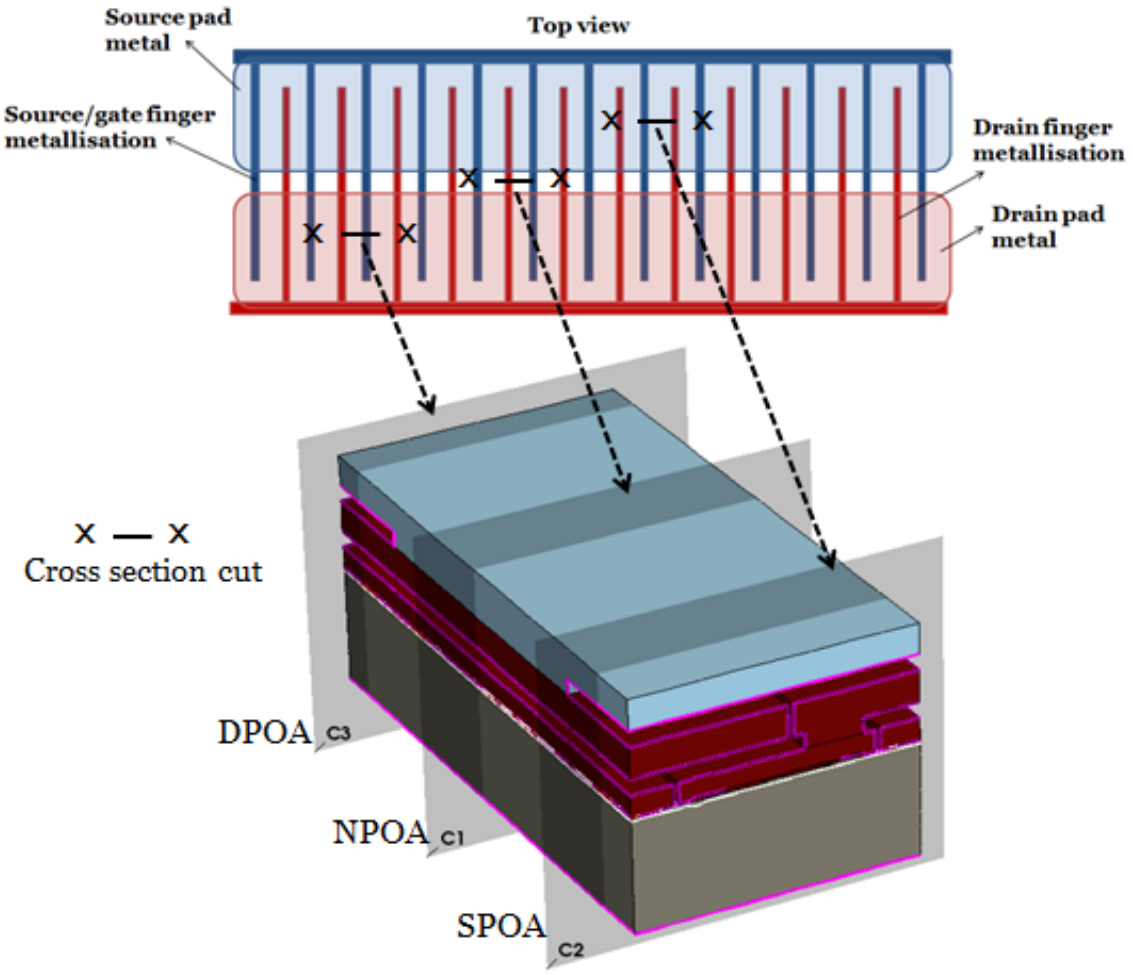


Fig. 8.7 Three locations (no pad - NPOA, source pad over active - SPOA, drain pad over active - DPOA) in the active area of the layout that give different cross-sections

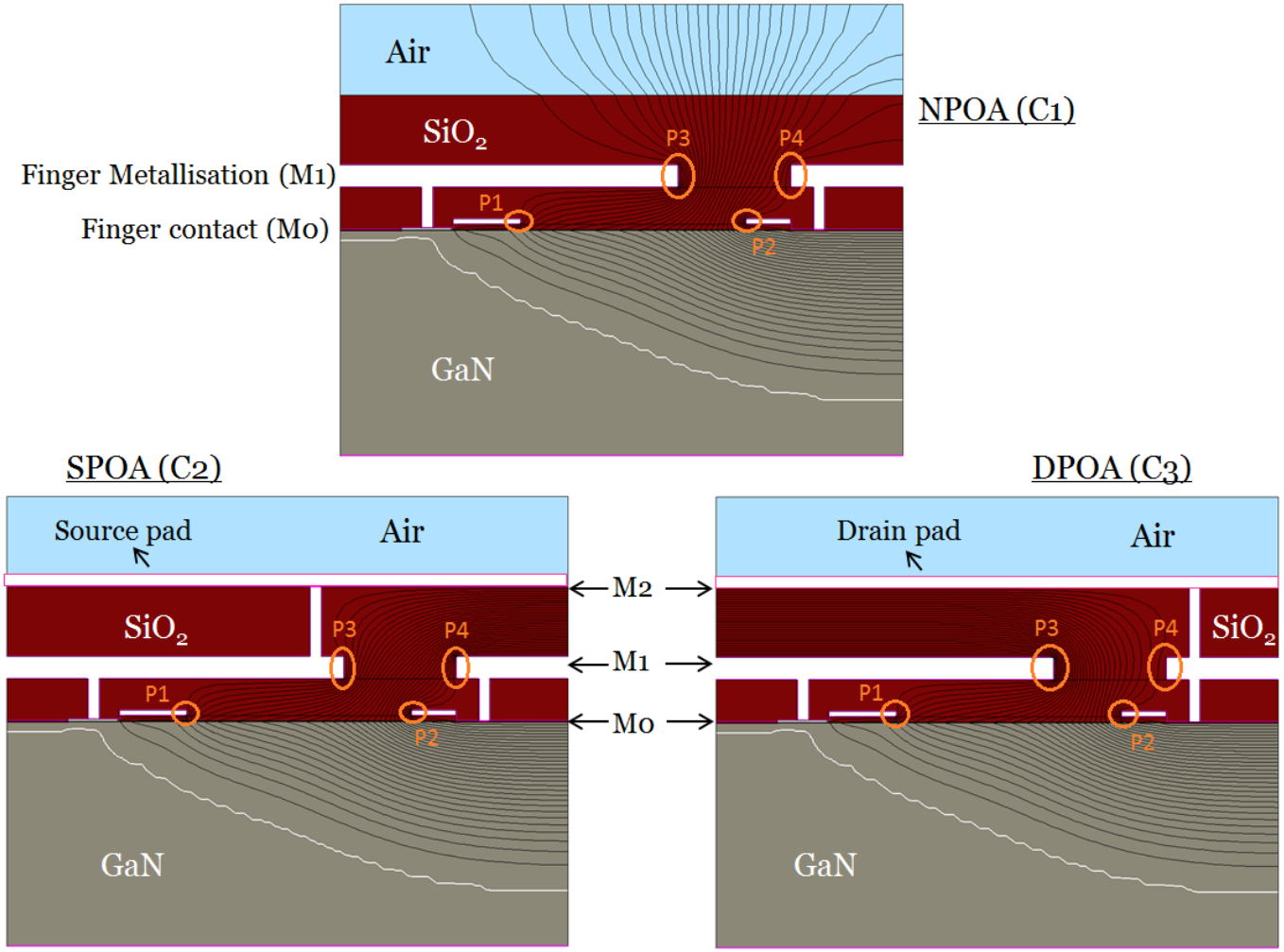


Fig. 8.8 Electrostatic potential lines at three different locations when the device is biased in the off-state (650V)

A cross-section of the device at these different locations was simulated with off-state bias applied to the drain terminal of the device. Fig. 8.8 shows the electrostatic potential lines at a bias voltage of 650V. It becomes apparent that the distribution of the potential is significantly altered in the regions where the active area is covered by the bonding pads. This has an effect on where the electric field peaks appear in the structure. However, a close look at the simulation results reveals that the distribution of potential in the semiconductor layers and the surface of the semiconductor is relatively uniform for the three different sections.

While surface electric field peaks are very important and the surface contact field plate design can be further optimized in this device to mitigate those, the concern related to these would be the same in both the BPOA and conventional layout. The analysis here focuses on the advantages and disadvantages between the two designs and will thus consider in more detail the dielectric layers as the change in the distribution of the electrostatic potential observed there was very significant.

A very interesting observation can be made at this point. The optimum metallization structure which can minimize the electric field peaks observed in the dielectric can vary depending on the section of the device investigated. The absolute electric field contour lines were plotted in MATLAB for the cross-sections in the three different locations (NPOA, SPOA and DPOA) of interest in the structure. Main areas of concern are easily identified in these plots which can be seen in Fig. 8.9 - NPOA, Fig. 8.10 - DPOA and Fig. 8.11 - SPOA. Note that the cross-section dimensions in these plots are based on those in the real device as provided by the foundry and the metallization structure is not necessarily optimized to reduce the electric field peaks observed. In the current design, it is observed that the electric field peaks are significantly higher in the SPOA and DPOA section of the device compared to the NPOA section. Note that the NPOA section electric field peaks present are equivalent to those in a conventional design. The maximum field values observed in the three sections are summarized in Table 8.1. As mentioned an optimum metallisation structure may differ between the three sections and this may lead to a novel layout design. By adjusting the TCAD model changes were made in the design to investigate whether a reduction in the peaks observed could be achieved.

This was done by varying the width of the field plate metallization for source/gate and drain. The optimized absolute electric field contour lines were plotted for the cross-sections in the three different locations (NPOA, SPOA and DPOA) of interest in the structure. Main areas of concern are again easily identified in these plots and can be seen in Fig. 8.12 - NPOA, Fig. 8.13 - DPOA and Fig. 8.14 - SPOA. The peaks that

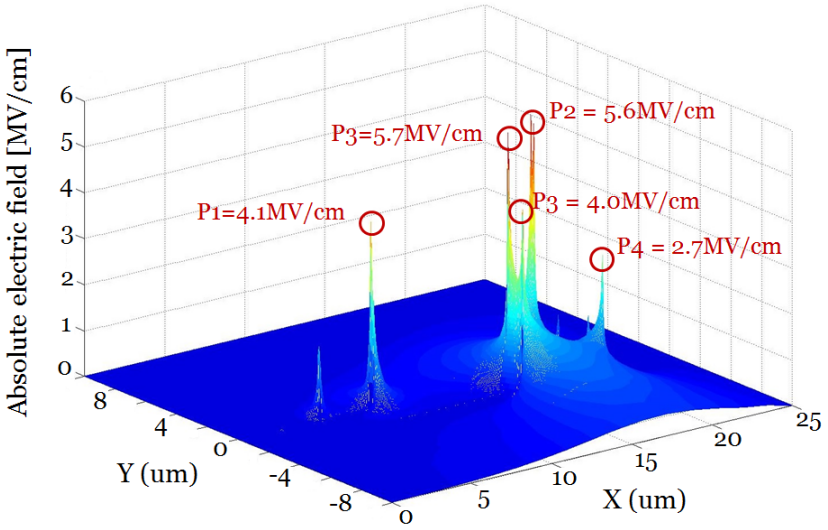


Fig. 8.9 Electric field peaks in SiO_2 at NP section of the structure

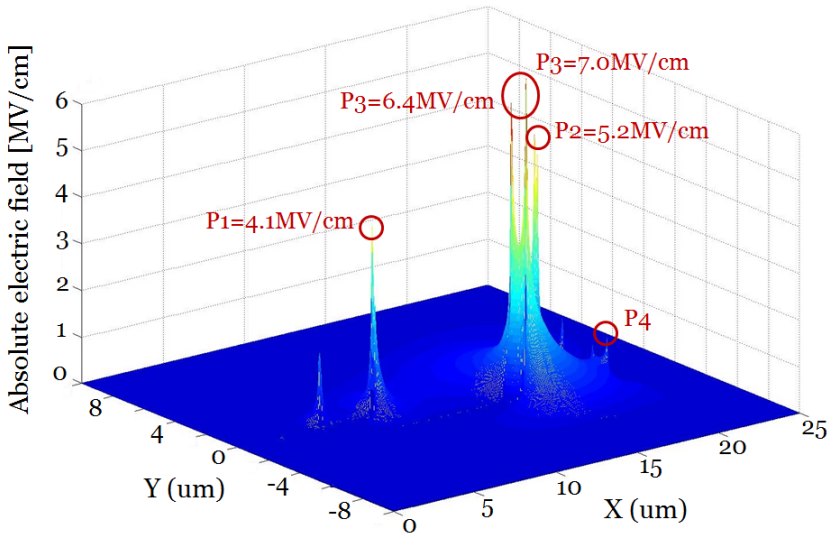


Fig. 8.10 Electric field peaks in SiO_2 at DPOA section of the structure

arise in the source pad and drain pad cover region are still much higher than those observed with no pad cover. A maximum value of 6.9 MV/cm was observed in the DPOA section and a maximum value of 6.2 MV/cm was observed in the SPOA section compared to the maximum value of 4.4 MV/cm observed in the NPOA section.

In the DPOA and SPOA regions the maximum electric field peak remained almost exactly the same despite the optimization attempts. The peak observed is in a similar location (P4 in SPOA, P3 in DPOA) where the electrostatic potential lines curve sharply due to the high voltage terminal metallisation/low voltage contact pad and vice versa. This is directly related to the presence of the pad over the active area and

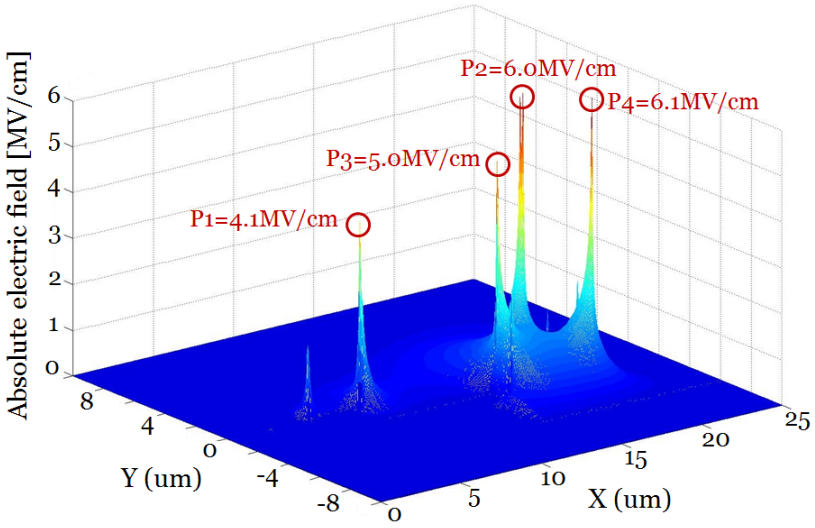


Fig. 8.11 Electric field peaks in SiO_2 at SPOA section of the structure

Table 8.1 Summary of electric field peaks observed in different regions of the BPOA device

Region	NPOA	DPOA	SPOA
Maximum EF peak before optimization, MV/cm	5.7	7.0	6.1
% difference compared to conventional	-	+23	+7
Maximum EF peak after optimization, MV/cm	4.4	6.9	6.2
% difference compared to conventional	-	+57	+41
% change after optimization	-23	-1	+2

explains the difference to the field peak observed in the conventional design. The peak observed in the BPOA structure is to a large extent dependent on the thickness of the SiO_2 layer which has not been varied here either before or after the optimization process. While a more complex design may indeed succeed in reducing the peak observed this analysis illustrates that additional care must be taken when designing a BPOA device. A possible solution to reduce the peak observed in DPOA and SPOA would be to increase the thickness of the second dielectric layer. Nonetheless, there are limitations to the thickness of a high quality SiO_2 that can be achieved, as well as added costs which can discourage the use of such a design.

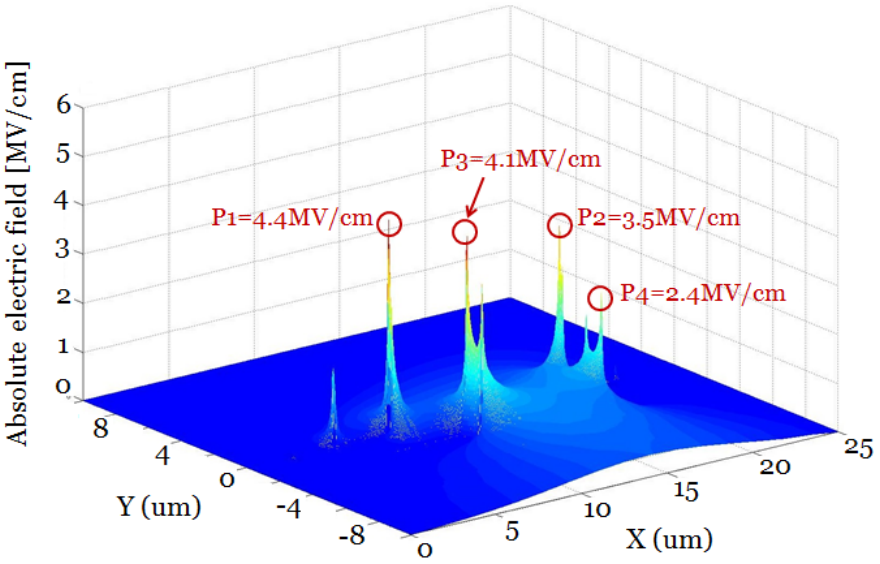


Fig. 8.12 Electric field peaks in SiO_2 at NP section of the structure after optimization

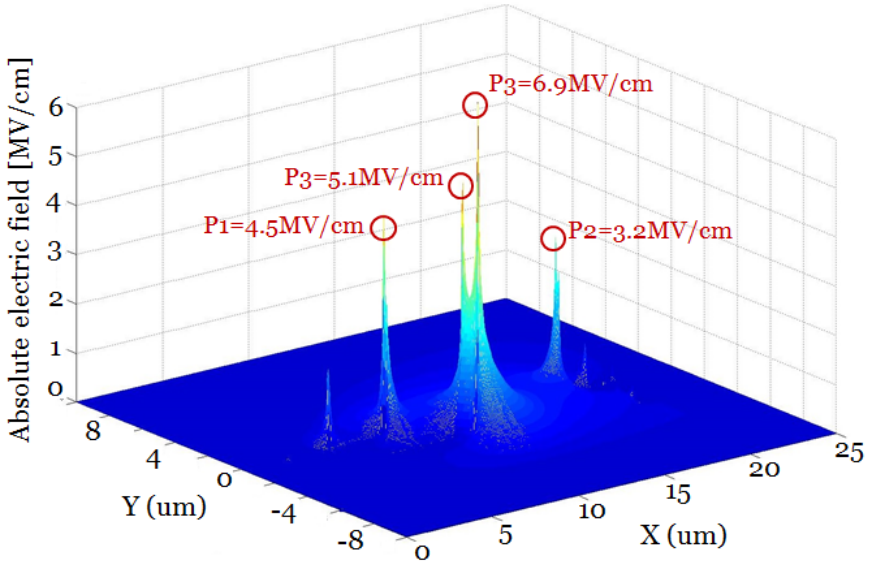


Fig. 8.13 Electric field peaks in SiO_2 at DPOA section of the structure after optimization

This analysis suggests that the maximum field observed in the BPOA design compared to a conventional design is found to increase by more than 55 per cent in the worst case scenario. These results are summarized in Table 8.1. The critical electric field which can be sustained by SiO_2 is 8-9 MV/cm [93][140]. While this value is not reached, the increase in field can lead to increased probability of TDDB breakdown, a relationship widely reported in literature [138][139].

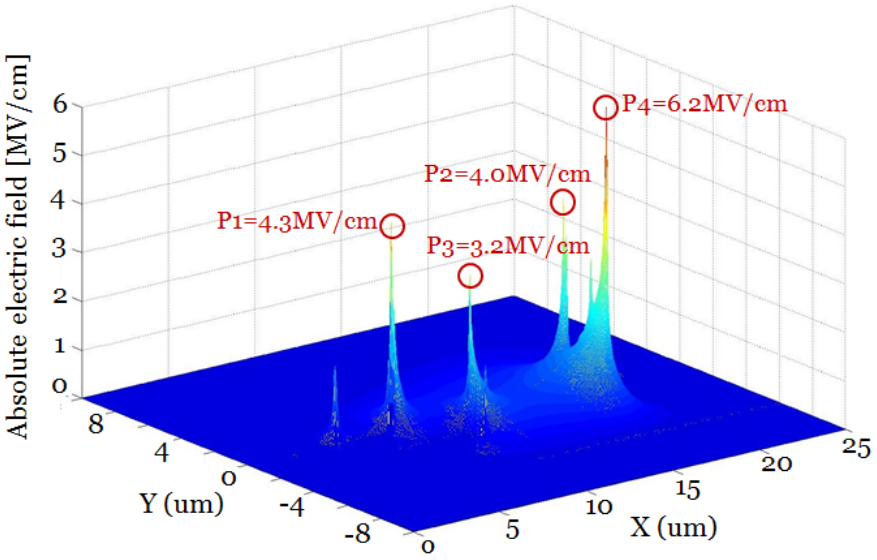


Fig. 8.14 Electric field peaks in SiO_2 at SPOA section of the structure after optimization

8.4.3 Electric field peak at pad edge

3-D simulations are useful in identifying any locations where a high electric field may be present in the z-dimension due to the placement of the pads on the active area of the device. These locations cannot be modelled with the use of the standard 2D cross-section simulation model. A point identified as a possible concern with a BPOA structure is at the edge of the metal contact pad (see point P6 in Fig. 8.15).

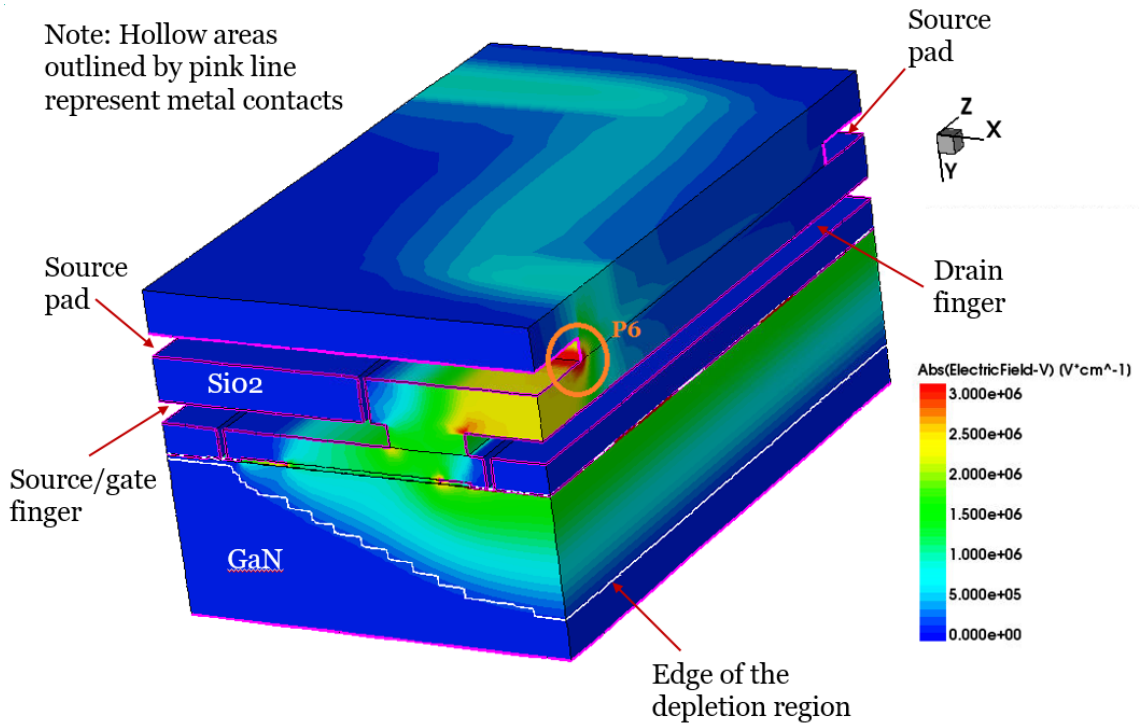


Fig. 8.15 Electric field peak in SiO_2 at pad edge

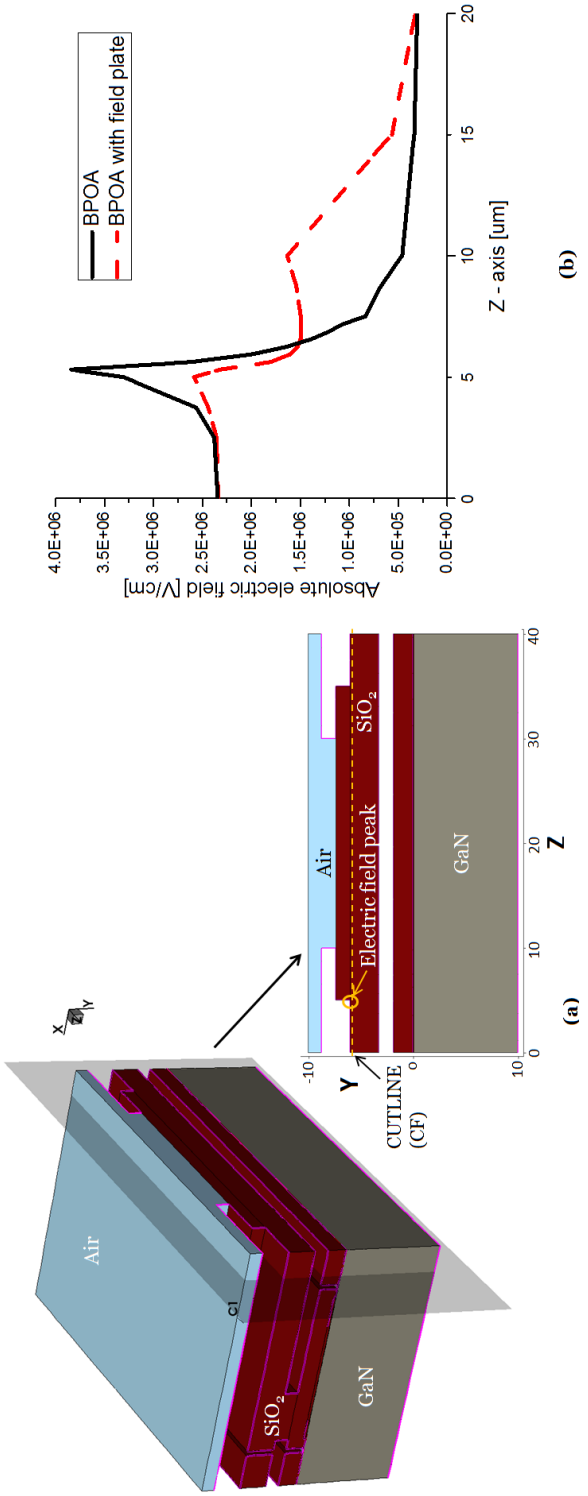


Fig. 8.16 (a) Field plate at pad edge (b) Electric field peak reduction in SiO_2 at pad edge

A maximum absolute electric field level of 4 MV/cm is observed as seen in Fig. 8.16(b). Several adjustments to the TCAD model were investigated to provide a reduction in the peak field observed. The most effective of these attempts was adding a step field plate to the edge of the pad as can be seen in Fig. 8.16(a). With the field plate optimized a reduction by 35 per cent of the electric field peak was achieved.

8.5 Conclusions

A detailed analysis of the performance of a bonding pad over active area (BPOA) design compared to a conventional layout for use in AlGaN/GaN heterostructure power HEMTs was undertaken. A superior on-state performance in terms of current density per unit area was observed from the BPOA layout as expected due to the area saving design. Higher off-state leakage current per unit area was observed in the BPOA design. However, this current was found to be equivalent between the two designs when a comparison per unit gate width was made for the two devices revealing that the BPOA design does not lead to any additional leakage paths. Significant problems were encountered when switching the BPOA-HEMT design in a clamped inductive switching configuration compared to the conventional-HEMT device. Finally, the reliability of the two layouts was examined using 3D TCAD modelling. The analysis focused on the high electric field peaks observed in the inter-metallic dielectric layers. A peak electric field increase of 55 per cent is observed in the BPOA-HEMT which severely increases the probability of TDDB breakdown in the SiO_2 dielectric layer. This increase can be significantly reduced by optimizing the field plates in the third dimension. In conclusion, while BPOA design can improve current density per unit area, this study suggests that there are significant drawbacks in switching and reliability performance which can hamper the use of such a layout to achieve a competitive and reliable commercial device.

The analysis in this chapter forms the basis of a recent patent application and has been submitted for publication to IEEE Transactions on Electron devices journal where it is under review.

Chapter 9

Conclusions and Future work

This chapter will submit conclusions of the work carried out in this thesis and will offer suggestions for possible extensions of the work in the future.

9.1 Conclusions

Power semiconductor devices lie at the core of all power electronics systems. With efficient power conversion being an area of significant interest in economies of the future, the importance of research in the field of power semiconductors has increased tremendously. The aims of research into to the field of power devices is to fulfil objectives such as increasing power density, reducing the size of devices and the packages they are housed in, achieving improved high temperature performance, higher frequency response, lower leakage and lower on-resistance, and increasing the operating frequency, which would allow the shrinking of passive components in the systems such as inductors and capacitors. Improvements in the performance of Silicon devices, which have been dominating the field, are requiring increasingly more investment, resulting in research in the field of wide bandgap semiconductors receiving significantly more attention in recent years. Gallium Nitride (GaN) is a material set to challenge Silicon technologies for low to medium voltage applications.

- Wide bandgap materials such as GaN can theoretically overcome the performance of silicon devices as the wider bandgap (3.4eV for GaN compared to 1.1eV for Si) translates into a higher breakdown field and a lower intrinsic carrier concentration. The former would result in smaller drift region with increased charge, while the latter would in theory reduce the leakage considerably.

- GaN is considered a very promising material compared to other WBG materials due to parameters other than just performance. High quality GaN layers can be grown epitaxially on several substrates, the most significant of which being silicon. This can be done using adjusted silicon production lines and with hetero-epitaxy on up to 8-inch wafers demonstrated already, production costs are becoming increasingly more competitive.

- Another advantage of GaN is that it allows the formation of heterostructures through the use of Aluminium to create an AlGaN layer. This leads to the formation of a two dimensional electron gas (2DEG) close to the interface of the AlGaN/GaN heterojunction which results in a quantum well region of high carrier density (of the order of $10^{13} cm_{-2}$) and high carrier mobility (up to $2000 cm^2/Vs$).

- The high carrier concentration at the heterojunction interface is enhanced due to the spontaneous and piezoelectric nature of GaN. The combination of spontaneous and piezoelectric charges at the AlGaN/GaN interface leads to a net positive charge which is compensated by a large concentration of electrons which forms the 2DEG.

- Since the two dimensional electron gas (2DEG) inherently exists at the AlGaN/GaN hetero-interface, this creates a challenge when attempting the design of normally-off rather than normally-on HEMTs. Nonetheless, as normally-off transistors are preferable in most power electronic applications, several methods have been proposed which can lead to enhancement mode devices, one of which is the use of a p-GaN gate. This thesis focuses on some of the challenges concerned with the p-GaN gate devices.

- In the short term, the majority of commercial GaN HEMTs will target the 100-200V and 600-650V voltage range with several commercial devices appearing in the market. Large market potential exists at the 600V range for applications such as power factor correction (PFC), AC to DC converters, uninterrupted power supplies (UPS), motor drives and photovoltaic system inverters. GaN-based Schottky diodes are targeted towards use in server and telecommunications switch mode power supplies (SMPS), PC power and lighting applications, as well as solar inverters and UPS systems.

This thesis has focused on several aspects of the operation of GaN-based HEMTs and Schottky diodes from device to circuit level with the view to gaining improved

understanding of the behaviour of these devices to enable better commercial designs to emerge. Some of the main findings are summarized below.

- In Chapter 4 a method to extract the ideality factor, barrier height and series resistance of a lateral AlGaN/GaN heterostructure power Schottky diode using a simple I-V measurement in on-state and sub-threshold domains is described. The analytical model for the on-state conduction of such devices is calibrated using extensive experimental results both at room and increased temperature.

- The following values, ideality factor ($\eta = 1.56$), barrier height ($\Phi = 0.87eV$) and series resistance ($R = 0.083\Omega$) were extracted at room temperature. I-V measurements performed at different temperatures up to 428K allowed the extraction of the above parameters at different temperatures. The ideality factor was found to move closer to one at increased temperatures while the extracted Schottky barrier height was found to increase. This is in line with the experimental findings reposted in the literature, although the dependence of both ideality factor and barrier height with temperature seem to be softer in our case which makes the device more stable in temperature. Finally, the series resistance, of which a large component is given by the 2DEG resistance, was found to increase with temperature as expected due to the mobility decrease in the channel (mobility exponent, $\zeta = 1.84$).

- In Chapter 5 a TCAD model of a test AlGaN/GaN device is built and thoroughly matched with on-state, off-state and reverse recovery experimental measurements. The model is employed to analyse the different options available for connection of the substrate contact, a consideration specific to the AlGaN/GaN lateral configuration. The reverse recovery current components and the transient depletion of the 2DEG during turn-off are also examined. The turn-off behaviour of a lateral AlGaN/GaN Schottky diode has not been analysed to this extent elsewhere in literature. Finally, the comparison of the different technologies (GaN, SiC, Si) for Schottky diodes is made based on the trade-off between on-state and reverse recovery parameters at both room and high temperatures.

- Experimental and TCAD results show that while the AlGaN/GaN Schottky diode is expected to provide a significant improvement in switching performance when compared to the conventional bipolar Si P-N diodes, the suggestion of *zero reverse recovery* is not truly valid. This is due to the high level of 2DEG charge density, necessary in the on-state to compensate for the lateral geometry of the

heterostructure diode. In conclusion, the SiC diode offers a more favourable trade-off between on-state and reverse recovery and its performance can be controlled more accurately as it is not subject to surface or bulk traps. The analysis carried out here uses complex TCAD models matched to extensive experimental results and it contains aspects which contradict findings in literature that suggest comparable turn-off performance between GaN and SiC Schottky diodes of equal rating.

- In Chapter 6 an investigation is undertaken to determine the effect of gate design parameters on the on-state characteristics (threshold voltage, gate turn-on voltage) of p-GaN/AlGaN/GaN HEMTs. Design parameters considered were p-GaN doping and gate metal work function. The analysis considers the effects of variations in these parameters using a TCAD model matched with experimental results.

- In conclusion, an improved understanding of the operation of the gate structure of the p-GaN cap E-HEMT was achieved. Some very important design considerations are summarized below.

  - As p-GaN doping initially increases the threshold voltage of the device is also increasing (for doping values of $1x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$) however, as the doping is further increased the threshold voltage starts decreasing (for doping values $>6x10^{18}cm^{-3}$). This is due to hole tunnelling at the metal/p-GaN interface establishing a tight electrical connection between the gate metal and the p-GaN layer.
  - At high doping levels, the threshold voltage cannot be significantly altered by the use of a different gate metal. This finding provides clarity to the observations in the study by Lee et al [112].
  - A variation in gate metal used affects the gate turn-on voltage of the device. This agrees with the observation in the study by Hwang et al [113].
  - The use of a Schottky gate contact rather than an Ohmic gate contact is essential in order to achieve a wide operating gate bias range. This finding contradicts the suggestion given in the study by Chang et al [121].

  These points reveal the trends that need to be taken into consideration when designing the gate characteristics such that the gate operation range is maximized and the device operates in an optimal way.

- In Chapter 7, an enhancement mode GaN high electron mobility transistor (HEMT) is switched in a clamped inductive switching configuration with the aim of investigating the source of oscillatory effects observed. These issues were revealed by investigating the turn-off and turn-on of a GaN E-HEMT device during a double pulse test. These arise as a result of the increased switching speed capability of GaN devices compared to their silicon counterparts. The experimental results are backed by SPICE modelling to evaluate the contribution of different circuit components to oscillations. Furthermore, the analysis considers the parasitic components at the device level due to different layouts. It is indeed shown that these have a very significant effect on the switching capability. Some good design techniques that can suppress the effects discussed are also mentioned at both circuit and device level.

- Two major issues, dV/dt and dI/dt induced oscillations are identified. Limiting the current through the device Miller capacitance and therefore a control of the drain voltage rise (dV/dt) during turn-off are essential in achieving a good circuit design.

  An optimised circuit is more immune to ringing caused by dV/dt effect as discussed in section 4.1 if:

  - Gate external resistance is high enough to control dV/dt, but not too high to generate a significant voltage drop when the discharge current of C_{gd} is flowing through. A trade-off is thus revealed. To allow stable switching the rate of switching of the device needs to be reduced however this can lead to increased losses.
  - Smart driving is used such as an active Miller clamp function as seen in commercially available drivers (e.g. Fairchild FOD8318). This function avoids a large C_{gd} discharge current flowing through the gate external resistance by grounding the gate through the turn-on of a transistor when a certain voltage is developed across $R1$.
  - Gate inductance L_g is minimised as Spice simulations reveal that gate inductance acts as to increase the amplitude of the oscillations observed. This is a result of the storage of energy when current is flowing through L_g.
  - The gate is driven to a negative voltage at turn-off to ensure unwanted device turn-on is avoided. This can however add cost and complexity to the design.

Regarding the *dI/dt* induced oscillations, the need to minimise the common source inductance in order to avoid severe ringing on the gate waveform is also demonstrated. The use of a ferrite bead in order to damp the oscillations observed has also been illustrated. Additionally, it is shown that more robust switching is possible when the device operates at an increased temperature. The self heating effect is, in this respect, beneficial as it can reduce the oscillations.

Finally, through the switching of various device layouts in the same circuit it is illustrated that device level parasitics associated with the different layouts can affect the device switching performance. The main issue is again the presence of common source inductance and novel designs which can minimise this parameter should be studied.

- In Chapter 8 the on-state, off-state and switching performance of a fabricated BPOA layout normally-off HEMT device is presented to illustrate the relative advantages and disadvantages of this design when compared to a device with a conventional layout. Furthermore, an analysis of the factors that may lead to poorer reliability in BPOA layouts is undertaken using TCAD model simulations. To the author's knowledge, such an investigation has not been reported elsewhere in literature. In particular, attention is focused on the electric field peaks observed in the inter-metal dielectric ($Si0_2$) when the device is biased in the off-state. Such field peaks are relevant when designing devices which are resilient to time dependent dielectric breakdown (TDDB).

- As expected, a superior on-state performance in terms of current density per unit area was observed from the BPOA layout due to the area saving design. Higher off-state leakage current per unit area was observed in the BPOA design however this current was found to be equivalent between the two designs when a comparison per unit gate width was made for the two devices revealing that the BPOA design does not lead to any additional leakage paths. Significant problems were encountered when switching the BPOA-HEMT design in a clamped inductive switching configuration compared to the conventional-HEMT device. Finally, the reliability of the two layouts was examined using 3D TCAD modelling. The analysis was focused on the high electric field peaks observed in the inter-metallic dielectric layers. A peak electric field increase of 55 per cent is observed in the BPOA-HEMT which significantly increases the probability of TDDB breakdown in the SiO_2 dielectric layer. This increase can be reduced by optimizing the field plates in the third dimension. In conclusion, while BPOA design can improve

current density per unit area, this study suggests that there are significant drawbacks in switching and reliability performance, which can discourage the use of such a layout to achieve a competitive and reliable commercial device.

9.2 Future work

This work can be continued in several directions:

- One possible extension of the work would be related to the AlGaN/GaN Schottky diode TCAD model described in Chapter 5. As previously described in detail some simplifications were made in the model.
  - The first simplification relates to the definition of the acceptor doping in the GaN layer. In the current model, doping was specified as fully ionized under zero bias with the acceptor energy level specified very close to the valence band. In reality, as numerous studies in literature have shown, this is not the case with Carbon doping reported to form energy levels at around 0.9eV above the valence band. This simplification could be removed in an improved model and any possible effects on the reverse recovery performance of the device could be investigated. Additionally, the effect on the reverse recovery of surface donor traps at the AlGaN/passivation interface could be investigated.
  - Another simplification relates to the accuracy with which the transition layer was reproduced in the TCAD model. The characterization of the transient layer is a very difficult topic in itself with numerous studies being conducted on the conduction mechanisms between the different layers, as well as the interface charges and traps present in these layers. The transition layer is of interest in the reverse recovery of the diode as it can affect the extension of the depletion region during turn-off. Furthermore, interface charges predicted at the GaN/transition layer interface may lead to the formation of a two-dimensional hole gas (2DHG) which can stop the vertical depletion. However, the presence of this 2DHG is still being investigated. Due to this very uncertainty about the 2DHG, many theoretical and simulation works have adopted the approach of treating the multi-layered epi with a simplified composition of layers or more often lumping them into a single layer, avoiding the issue of 2DHG at the interfaces altogether as was done in this study. Future work can therefore focus on using the TCAD model

to investigate the effect that different epi configurations can have on the turn-off behaviour of the AlGaN/GaN Schottky diode.

- Another possible extension could be related to the AlGaN/GaN HEMT TCAD model described in Chapter 6. As mentioned, a simplification of including fully ionized Magnesium doping in the p-GaN layer is made in this work. This simplification could be removed and the effect that trapping phenomena may have on the device transient performance could be investigated. It has been observed in measurements of these devices that when high gate bias is applied to the gate, a threshold shift is observed in the device. This threshold instability could be better quantified and possibly related to the trapping phenomena in the p-GaN layer.

- Additionally, given the improved understanding of the effect of gate parameters on the device on-state characteristics, new improved designs which can increase the device threshold voltage, the gate turn-on voltage and the gate bias window of operation can be developed.

- Several ideas of continuing the work described in Chapter 7 are being considered, with some of the work already underway. As has been discussed in this thesis, common source inductance is an important parameter in observing oscillations during switching. From the perspective of a device designer the objective should be to reduce the source inductance arising from the device as much as possible. Thus, novel layout designs which can achieve that are being considered. Electromagnetic simulation software such as Ansys Maxwell can be used to evaluate and optimize the parasitic components present in these designs before fabrication. Furthermore, it is reported in literature that when parallelizing GaN HEMTs, unbalanced common source inductance may lead to circuits which are even more susceptible to oscillatory behaviour. Spice model simulations which illustrate this effect have been performed using the setup and models described in Chapter 6. A suggestion that the unbalanced source inductance between different sections of the layout at device level can have the same effects is also currently being investigated. Electromagnetic simulation software such as Ansys Maxwell would again be very useful in this study with some preliminary models developed thus far.

- Continuations of the work described in Chapter 8 would focus on an improved understanding of the differences observed between the switching performance of the BPOA device and the conventional device. As mentioned in section 8.3, a

near identical circuit which accommodates the GSD package of the BPOA device could be produced for a fairer comparison. Alternatively, a package with the BPOA design in GDS configuration could be produced so that it can be used in the existing test circuit. Moreover, the suggestion that the BPOA design could lead to increased electromagnetic interference between the high voltage (drain) and low voltage (source/gate) terminals due to the presence of the bonding pads over the active area could be investigated through the use of an electromagnetic simulator such as ANSYS Maxwell.

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