Testing High Resolution SD ADC's by using the Noise Transfer Function

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Abstract

A new solution to improve the testability of high resolution SD Analogue to Digital Converters (SD ADC's) using the quantizer input as test node is described. The theoretical basis for the technique is discussed and results from high level simulations for a 16 bit, 4th order, audio ADC are presented. The analysis demonstrates the potential to reduce the computational effort associated with test response analysis versus conventional techniques.

1. Introduction

Testing high-resolution mixed signal interfaces in production requires high accuracy testers, large data storage resources and processor intensive response analysis. Test time, infrastructure and cost per device are therefore currently too high for this class of function. Much effort has been put into addressing this problem for ADC's and DAC's [1-8].
Commonly accepted Automatic Test Equipment (ATE) based testing of ADCs is based on the verification of a subset of converter performance parameters that include offset, gain, signal-to-noise ratio, total harmonic distortion, INL, DNL and power consumption. Dynamic performance parameters are extracted from the output bit stream by using FFT analysis of the converter's response to a sinusoidal test stimulus. Static performance parameters can be determined from measured code transition edges (feedback loop test) or from the number of code occurrences in response to a periodic signal (histogram testing). The accuracy of such parameter measurements requires a large number of samples (approx. 16536 for 90dB THD and SNR measurements) and up to 10s of test time for a single channel 16-bit audio ADC.
Various Built-In Self-Test (BIST) techniques for analog and mixed signal circuitry have been published in [1-9] that target test time reduction. All these techniques address the measurement of just one or of only a limited number of specification parameters using conventional techniques. Moreover, the circuitry introduced by most of these methods tends to require significant die area and dedicated additional test patterns for verification before use.
In this work the focus is on how to simplify and accelerate the testing of high order sigma-delta converters for audio applications without degrading test quality. The method presented in this paper utilises the noise transfer function (NTF) of the converter as figure of quality. In practice extracting this function requires the injection of a sine-wave into the quantizer input and performing a spectral analysis at the ADC output.
The NTF contains crucial information related to the dynamic behaviour of the converter. The comparison of a measured response with a reference can in itself be a powerful test and diagnostic tool. The information in this curve can also be used to extract three important specifications: gain, noise, and distortion. Furthermore, by using the NTF together with the techniques described in section 3, these parameters can be extracted through a lower number of samples than required for traditional FFT evaluation. The technique preserves the accuracy of the measurement without the need for complex design modification or Design-for-Testability (DfT) structures.
The paper is organised as follows. In section 2, a brief overview of the theory of the sigma-delta converters will demonstrate the importance of NTF characteristic on the quality of the converter. Section 3 will discuss the noise

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transfer function test method and present results from high level simulations to demonstrate its applicability. Section 4 will finally draw conclusions.

2. Sigma-Delta Modulator

Sigma-delta modulators use negative feedback and over-sampling techniques to reduce the in-band quantization noise. Figure 1 illustrates the basic first-order architecture. Due to the negative feedback, the digital output y will, on average, be forced to track the analogue input signal x. By over-sampling the input signal and averaging the output, the input signal can be accurately converted without the need for a high-resolution quantizer [10].

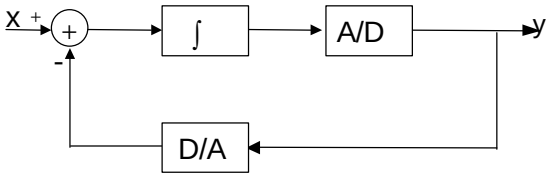

Figure 1 Basic architecture of a first-order ADC.

The linearized model shown in figure 2 can also be used to illustrate the behaviour of a first-order sigma-delta modulator. The quantization noise contribution is modeled as an input E(z). It can be seen from this model that the transfer function from the quantization error source to the output is given by $(1\text{-}z^{-1})$, which is effectively a high-pass characteristic and the noise transfer function (NTF) of the first order modulator. The quantisation noise in the signal band is hence attenuated relatively to frequencies higher than the filter characteristic break point. The noise attenuation property is described by evaluating the total noise power in the signal band:

$$P_{Q,\Sigma\Delta} = \int_{-f_{BW}}^{f_{BW}} \frac{P_{Q,Nyquist}}{M} \cdot \left(1 - z^{-1}\right) df = \frac{P_{Q,Nyquist}}{M^3} \cdot \frac{p^2}{3} \quad (1)$$

where $P_{QNyquist}$ is the total power of noise, f_{BW} is the cutoff frequency, M is the over-sampling ratio (>>1).
In case of higher order modulators, the in-band attenuation is higher and the characteristic steeper.
Simple feedback theory shows that the transfer function from the quantization noise source to the output for higher order modulators is modified to $(1\text{-}z)^L$, where L is the order of the sigma-delta modulator. In this case the noise rejection is given by:

$$P_{Q,\Sigma\Delta} = \int_{-f_{BW}}^{f_{BW}} \frac{P_{Q,Nyquist}}{M} \cdot \left(1 - z^{-1}\right)^L df = \frac{P_{Q,Nyquist}}{M^{2L+1}} \cdot \frac{p^{2L}}{2L+1} \quad (2)$$

for M>>1.

This is a generalized equation for the in-band quantization noise in a L-order sigma-delta modulator. The dynamic range (with quantization noise being the only noise source) can be easily derived and is shown in Equation (3):

$$DR_{\Sigma\Delta} = 10 \cdot \log\left[\frac{3}{2} \cdot \left(2^B - 1\right)^2 \cdot \frac{2L+1}{p^{2L}} \cdot M^{2L+1}\right] \quad (3)$$

where B is the resolution of the quantizer.

It can be observed that by increasing the order of the modulator, the over-sampling ratio or the quantizer resolution, the dynamic range can be increased.

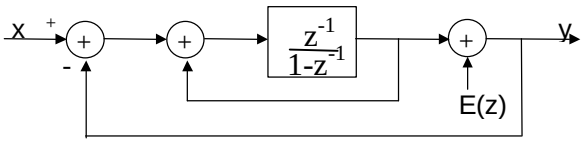

Figure 2 Delta-sigma

The output of the modulator is given by:

$$Y(z)=H_S(z)X(z) + H_N(z)\,E(z) \quad (4)$$

where H_S and H_N are the signal and noise transfer function functions, respectively and X(z) is the input signal. Thus, the digital output contains a delayed replica of the analogue input signal plus a noise component whose spectrum is that of the quantization noise E(z) shaped by the noise filtering function due to H_N. The eq. (4) gives then a relationship between the input signal, x in figure 2, and the quantizer input.

3. Testing the DS ADC by using the Noise Transfer Function

As described in the previous paragraph in a delta-sigma circuit, feedback via an integrator shapes the spectrum of the modulation noise, placing most of its energy outside the signal band. The characteristics of the filter included in the feedback loop determine the shape of the noise spectrum and the quality of all the modulator is determined by the noise prediction and rejection capability. Since the Noise Transfer Function is in fact describing how much the quantization noise is attenuated in the modulator band, it can represent a figure of merit of the ADC. Consequently, to measure the NTF can be a fast test to determine the quality of the converter. To perform this measure, following the linearized model of the

converter showed in fig. 2, the quantizer input has to be used as test input.
On the other side the high sensitivity of the NTF offers also the possibility to measure in fast way three important specifications of the ADC which normally have a strong impact on the test time: gain, SNR and THD. Even in this case, the technique uses the quantizer input as test input and then performs a FFT analysis on the output bit stream.
The device under test used as a demonstrator is a fourth order sigma-delta 16 bit audio converter designed for a CODEC application. Figure 3 depicts its topology. This ΣΔ converter has a 24kHz bandwidth and clock frequency of 3.07 MHz. and uses single loop architecture.
Each integrator has a separate gain stage with an output that feeds into a summing node. The output of this summation forms the input to the quantizer.
To further improve the noise rejection in the signal band, the system zeros are spread over the signal bandwidth instead of placing them all at DC. The zero's spread is achieved by introducing a local resonator feedback loop.

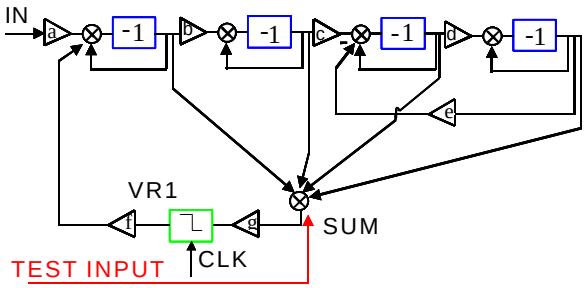

Figure 3 New test access for a 4th order ΣΔ ADC

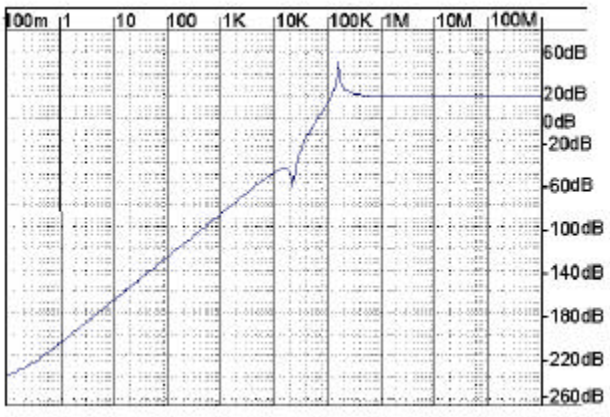

Figure 4 Noise Transfer Function for a 4th order modulator

The Noise Transfer Function of the converter is shown in figure 4. The high-pass behavior of the converter can be observed. The figure also shows the effect of the system zeros causing in particular a slope change at 20kHz.
To obtain this curve, the quantizer input (SUM node in figure 3) is stimulated with a sine-wave of variable frequency and the output bit-stream of the converter is sampled and processed. It should be noted that access to this input node is not difficult since it is already accessible for leakage compensation purposes.
The NTF contains a significant amount of information in particular related to the dynamic characteristics of the converter hence a first fast diagnosis of the correct behavior can be achieved by comparing the curve shapes to a reference.
The following sections will describe how it is possible to reduce the number of samples measuring important specifications parameters during the FFT analysis by using the same test input. It will also be shown that by observing the response to a test stimulus applied at this new test input, a higher sensitivity can be achieved with respect to distortion and noise. This is due to the fact that the spectral line of the test signal is attenuated by the filter characteristic hence increasing the relative magnitude of the parameters of interest. The test procedure will be demonstrated through high level simulations using the SMASH simulator [13], provided by the project partner Dolphin Integration. Results from simulations are presented for each of the specifications investigated.

3.1. Gain Evaluation by measuring the Noise Transfer Function Attenuation

As described in the theory, the path from the quantizer node to the output of the modulator is effectively a high pass filter as described by eq. (2) above. This function attenuates the signal injected into the quantizer node in the signal band. By using this concept, each signal injected into this node will be attenuated of the same amount of the quantization noise in the signal band. The test procedure is then the same as the one used to test the attenuation of a high pass filter. The technique involves the injection of a sine wave of a known frequency (in the signal band) and amplitude into the SUM node in fig. 3. In this example the sine wave is set to 4kHz. The analysis of the response essentially requires a comparison of the amplitude of the fundamental spectral line at the output with the input amplitude. This measurement effectively provides the gain or the noise attenuation of the loop at the stimulus frequency. The direct relation between this attenuation and the modulator gain allows the evaluation of the gain. The measurement can be repeated several times to achieve better accuracy.

The amplitude of the sine wave used as test signal is not crucial in this technique as it is for traditional test procedure, where it is easy to incur in saturation problem. The simulation results showed that for a 16-bit accuracy a

test time of 0.05s is required which is half of what is generally required to measure the gain of the converter.

3.2. SNR Measurement

Another measurement possible, using the same test access node, is the SNR evaluation. Considering the case where no signal is applied at the input of the ADC but a test signal is injected into the test input, the spectral analysis (FFT) of the output will contain only the in-band noise still present after filtering, plus the attenuated spectrum of the injected test signal. If a low pass filter (see LPF curve in fig. 5) is used to amplify and extract the in-band spectral components, it is possible to extract both the magnitude of quantization and the pattern noise. The effect of applying the test signal to the SUM node is that on the output the amplitude of the test stimulus is now attenuated as well as the noise in the signal band. By choosing the correct frequency for the test signal it is possible to increase the amplitude of the noise relative to the test signal. This simplifies noise evaluation computations. The spectral line of the test signal can also be eliminated by a (digital) notch filter around the test signal frequency. However, this will have a slight impact on the in-band noise power.
To not neglect the noise generated outside the loop, the input of the converter can be also stimulated by a sine-wave of a known amplitude and frequency.

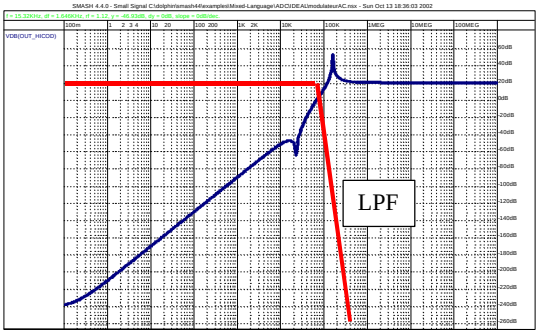

Figure 5 Low Pass Filtering (red line) used to measure the quantization noise.

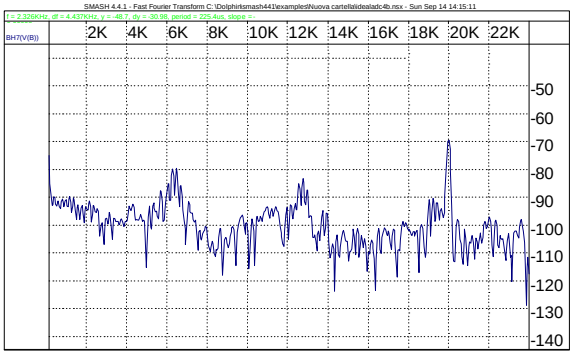

Figure 6 FFT over 65536 samples: S/(N+THD)=0.6dB,

Since of course this component will not be attenuated, a digital notch filter can be used to suppress it and not perturb the noise evaluation.
Figure 6 shows the FFT over 65.536 samples at the output of the fourth-order single loop converter, when a sine-wave of 20 kHz is applied as test stimulus. The test signal (20kHz in fig.6), is attenuated increasing the visibility of the noise component. In table 1 the evaluation of S/(N+ residual THD) is shown. Those measurements are extracted using an FFT analysis. The calculations are made 3 times, each based on a different number of samples. In case of an in-band amplification of 10, it can be seen that only 0.8 dB of accuracy is lost when using 16.384 samples rather than 65.536. A resolution of 90dB, without in-band noise amplification can be achieved with 16.384 samples.
By improving the low pass filtering gain and shape, an additional reduction on the number of points can be achieved. The FFT evaluations have been carried out at the output of the modulator without post processing (low pass filtering) through the decimator.
Comparing the method with the conventional technique, the computation time is significantly reduced since no curve fitting is required and the test waveform generation does not require sophisticated equipment.

Table 1 Impact of sample size on measurement results

n. samples	S/(N+THD)	THD
65536	16.6 dB	135.1 dB
16384	15.8 dB	135.3 dB
8192	13.7 dB	135.3 dB

From this measurement it is possible to directly obtain the in-band noise power, eq. (6), plus the total harmonic distortion. This is however not the dominant component whwn no signal is applied at the input of the converter, since the most significant source of THD is the first integrator.

3.3. Measuring the THD

The evaluation of the THD cannot be achieved directly and still requires additional work to correlate this parameters measurement with the individual electrical performance.
For the THD measurement, both the input of the converter and the test input have to be stimulated, such that the

distortion contribution of each block can be measured. An FFT has to be performed at the output of the converter.

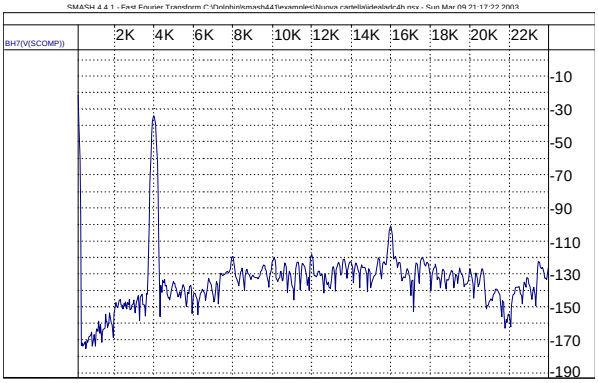

Figure 7 FFT at the converter output when the *SUM* node is stimulated

From preliminary investigations came out that just observing the impact that the distortion has on the amplitude of the spectral line due to the test signal it is possible to have information on the amount of the THD. In fact the quantizer input is very sensitive to the dynamic parameters of the circuit (poles and zeros) especially if a high order modulator is considered. In fig. 7 the FFT at the output of the converter is shown where a 16 kHz sine-wave is injected at the *SUM* node (fig. 3) while a 4 kHz sine-wave is applied to the input. The same electrical configuration as in fig.7 is shown in fig.8, in presence of additional distortion.

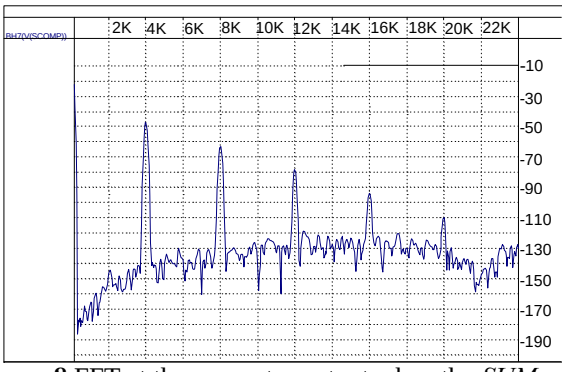

Figure 8 FFT at the converter output when the *SUM* node is stimulated and the distortion is assumed

In order to introduce non-linearity in the converter behavior, in the high level description of the converter obtained by using SMASH simulator, a diode at the first integrator input is inserted to clamp the signal and to model this effect.
The FFT analysis at the output of the modulator shows additional spectral lines, which are due to the introduced perturbation (fig. 8). Observing the 16 kHz spectral lines due to the test signal and comparing it with the same spectral component in the previous diagram where the distortion was not modeled (fig. 7), an attenuation of 10 dB can be detected when the distortion model is applied (fig. 8). The test signal spectral component can be extracted by post-processing the output to make the attenuation evaluation easier.
This is not a direct measure of the THD, but it is possible to define a direct correlation between the amount of the attenuation that the test signal spectral line exhibit and the total distortion.
The procedures seen up to know don't cover the full set of specifications normally needed to satisfy the quality verification of the converter. However they allow to reduce the test time by reducing the number of samples requested to perform some of the more critical specifications.
Table 2 summarizes the time test reduction that can be achieved by using the NTF based test procedure respect the traditionally used based on the Automatic Test Equipment with a microprocessor on board to analyze the response of the converter to the test signal applied to converter input. For the parameters not measurable from the quantizer input, the standard ATE based procedure and the relative number of samples are considered.

Table2 Comparison between the ATE based techniques and the analysis of the NTF

Specifications	Samples ATE	Test time [s] ATE	Samples NTF	Test time [s] NTF
THD (90dB)	16384	0.6	8192	0.3
SNR (90dB)	8192	0.3	8192	0.3
Gain (16 pt)	32	0.1	16	0.05
Crosstalk	8192	0.3	8192	0.3
CMRR	4096	0.2	4096	0.2
PSRR	4096	0.2	4096	0.2
Power cons.		0.2		0.2
		1.9		**1.55**

4. Conclusion

In this paper a potential solution to improve the testability of ΣΔ ADCs has been described using the quantizer input as test node. Both a theoretical description of the method and results from investigations using a high level simulator to study a 16-bit audio ADC have been discussed.
From the analysis, the method appears promising and fast, as it does not require sophisticated computations as in case of conventional techniques. It has been shown that for SNR and THD a 50% test time reduction at a moderate decreases in accuracy can be achieved.
The use of the test input at the SUM node makes this technique compatible with system level test access structures such as IEEE1149.4 where a separate test input

as to be provided. Higher frequency applicability is currently under further investigation.

5. Acknowledgements

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