The Application of I_{DDX} Test Strategies in Analogue and Mixed Signal IC's

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Abstract

Supply Current Testing (I_{DDQ}) has become an important defect oriented test strategy for digital IC products. The technique takes advantage of the low quiescent supply current drawn by static CMOS circuits relative to the current consumption during state changes. However, in analogue and mixed signal IC's this condition can rarely be observed, as in most circuits, steady state currents depend on the biasing conditions and the circuit design.

This paper reviews analogue current monitoring proposals, investigates some of the problems related to the use of these techniques and attempts to categorise a number of analogue design styles against the probable suitability for current testing methodologies.

1 Introduction

In the digital world, supply current monitoring is almost entirely based on I_{DDQ} testing that involves measurements of supply current in the quiescent state. For analogue circuits, several schemes exist and are generically referred to as I_{DDX} where, (amongst others) the "x" may be a "d" to represent dynamic current measurement, a "q" to represent static current measurement or a "t" to represent transient current measurement. This paper aims to summarise proposals for current monitoring and discusses the effect of process variations on fault free quiescent current levels. An initial study into analogue circuit design styles and the predicted effectiveness of current testing for a number of examples extracted from a categorisation process will be reported.

2. Current Monitoring Techniques

A number of supply current monitoring techniques for testing analogue and mixed signal IC's have been proposed [1-6] that have generated results that in many cases are contradictory. In [1] I_{DDQ} levels for both opens and shorts in a Sallen and Key high pass filter were investigated. Results showed that DC voltage measurements were far more effective. On the other hand simulation results obtained on a op-amp structure [2] identified 80% of simulated defects causing supply current changes of >25%. In this study, DC sweeps of the input voltages was found to be the most revealing test vectors. A continuation of this

work led to the use of non-periodic pseudo random signals being used as input vectors [3].

Steady state response magnitudes such as RMS. values are extracted from the supply current in [4] for various analogue circuits exercised by sinusoidal or square wave inputs. Optimisation of input conditions have been shown to generate high fault coverages. The approach of transient response I_{DDT} has been used on continuous time filters in [5]. This is however more complex requiring built-in-self-test (BIST) circuitry. Initial results have again suggested high coverage. Pulse response testing has been suggested in [6]. In this case the V_{DD} and V_{SS} rails are pulsed whilst applying a fixed voltage on the inputs. Temporal and spectral analysis is then applied to the transient rail current.

3. Effect of Process Variations

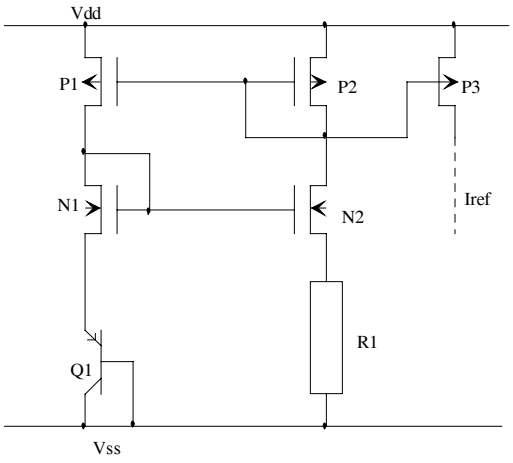

Figure 1: Schematic of current reference cell (iref)

In the majority of previous studies, the effect of process variations on fault free current levels has been identified as being critical for both setting pass/fail thresholds and deriving realistic coverage figures. The following section summarises an evaluation carried out on the current reference cell shown in fig 1 and subsequent measurements on silicon. [7]. In this circuit the reference current is given by:

$$Iref = \frac{V_{EB}(Q1)}{R1} \qquad (1)$$

Both absolute and relative component variation has been evaluated across a single wafer and from wafer to wafer for both biasing and biased cells.

3.1 Absolute Component Variation

The reference current generated in the circuit shown in fig. 1 is dependent on the emitter-base voltage drop of transistor Q1(V_{BE}) and the value of resistor R1. The value of (V_{BE})Q1 does not vary significantly in relation to the process dependent value of the resistor R1 which does show considerable variation. The minimum, typical and maximum process values (i.e. $\pm 3\sigma$) for resistor R1 have been considered to evaluate the range of current variations. A hand calculation of current range and a 1000 point monte-carlo simulation, using the same parameters, gives the results shown in fig. 2.

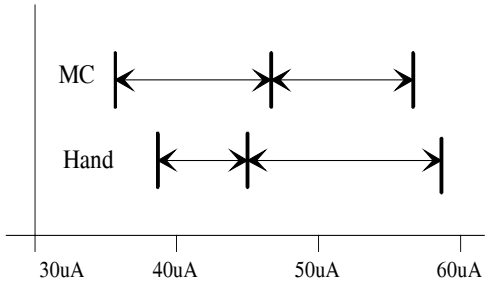

Figure 2: Hand & Monte-carlo 3σ simulation results

The balanced nature of this current source ensures that absolute component variation of the MOS transistors has only a relatively small effect on the reference current value. A 1000 point monte-carlo simulation of the MOS HSPICE parameters, within 3σ limits, yields a current variability 3σ value of only 0.24μA.

Temperature variation affects the reference current value in that both the value of resistor R1 and V_{BE}(Q1) are temperature dependent. Respective temperature coefficients are typically +3600ppm/^{O}C and -2mV/^{O}C which gives a net temperature coefficient of -0.3μA/^{O}C for the whole circuit. Assuming the testing temperature can be controlled to within

a range of ± 5^{O}C then the total current change due to this effect is ± 1.5μA.

The absolute value of resistor R1 dominates other absolute value sources of current variability. A superposition of the effects of variation of resistor value, FET process values and temperature variation is illustrated in Fig. 3.

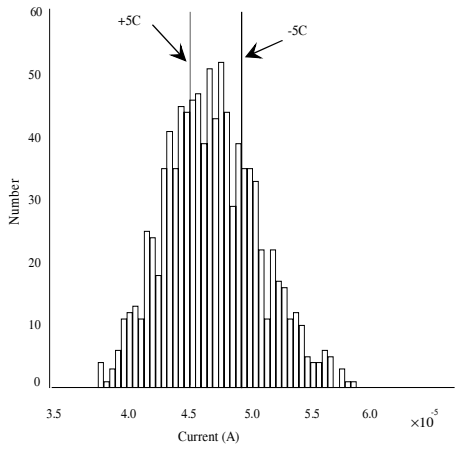

Figure 3: Resistor, FET parameter and temperature effects on reference current

3.2 Relative component variation

Relative component variation (mismatch) manifests itself as two problems. First, mismatches within the components of the two arms of the current reference cell shown in fig. 1 cause small changes in the value of the reference current. Second, two or more current reference cells will not carry exactly the same current since their resistor values will also generally not be equal.

3.2.1 Relative component variation within one cell

Ideally, the transistor pairs P1,P2 and N1,N2 are perfectly matched to ensure that the currents in either arm of the reference cell are equal. Using process mismatch data an accurate estimate of the maximum likely current mismatch may be obtained by hand calculation. If the input referred threshold voltage (V_T) mismatch (the net effect of both V_T and all other process parameter mismatches) is defined to be ΔV_T for both NMOS and

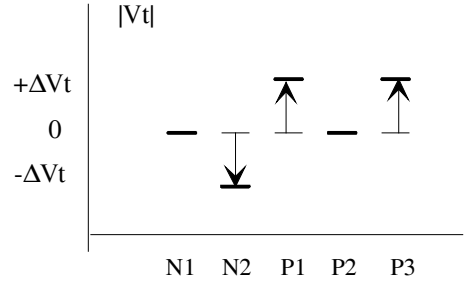

Figure 4: Parameter changes necessary for maximal current offset

PMOS devices the necessary changes to the MOS transistors of fig. 1 to generate maximum current offset within the core are those shown in Fig.4. The sense of V_T changes does not matter since the results are combined in quadrature.

The drain-source current of a MOS transistor operating in the saturation region may be written to a good approximation as,

$$I_{DO} = K' \frac{W}{2L}(V_{GS} - V_T)^2 \qquad (2)$$

where K' is the MOS transconductance parameter, W and L are the width and length of the MOS transistor respectively, VGS is the gate-source voltage and V_T is the threshold voltage. If the change in the value of V_T (ΔV_T) is small with respect to its nominal value the equation representing the current with offset values present is written,

$$I_D = K' \frac{W}{2L}(V_{GS} - V_T + \Delta V_T)^2. \qquad (3)$$

and the change in current may be approximated to:

$$\Delta I_D = K' \frac{W_P}{L_P}(V_{GSP} - V_{TP})\Delta V_{TP} \qquad (4)$$

where ΔI_D is the change in drain current and all other symbols have the same meaning as in eq. 2. In the reference cell shown in fig. 1 the net mismatch in currents between transistors P1 and P2 is thus,

$$\Delta I_{P12} = K^1 \frac{W}{L} (V_{GS} - V_T) \Delta V_T. \quad (5)$$

The threshold voltage mismatch of N1 and N2 causes the voltage drop on the resistor Rq to change by ΔV_T .(It has been assumed that the small current mismatch between transistors N1 and N2 has negligible effect on mismatching their gate-source voltages.) Mismatch between transistors P2 and P3 must also be accounted for using

$$\Delta I_{P23} = K^1 \frac{W_{P3}}{L_{P3}} (V_{GS} - V_T) \Delta V_{T3} \quad (6)$$

where A3 is the aspect ratio of transistor P3 and ΔV_{T3} is its threshold voltage shift from the nominal value of V_T.

Inserting the 3σ values for ΔV_T into equations 4,5 and 6 are combining them in quadrature (i.e. assuming no correlation between offset values and taking into account that P2 and P3 act so as to reduce the RMS core current error by a factor of $\frac{8/12}{18/10}$) gives a predicted 3σ current mismatch of 0.22µA.

A monte-carlo simulation of the same circuit with the same offset values gives a 3σ current tolerance of 0.32µA. Hand calculation and monte-carlo results are shown in fig. 5.

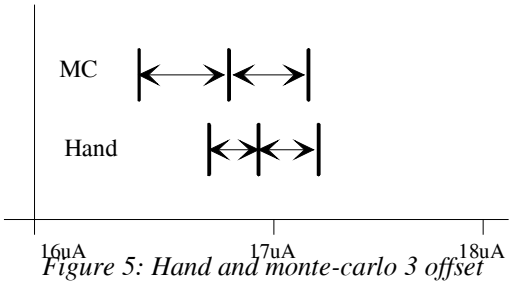

Figure 5: Hand and monte-carlo 3 offset simulation results

3.2.2 Relative component variation between cells

In addition to the current tolerance predicted in the above section there will also be an intra cellular current tolerance caused by resistor mismatch. This may be calculated in the same way as for the wafer current distribution but using the resistor matching value rather than the absolute resistor value range. A value of ± 0.46µ A is predicted for this component of the 3σ current variation assuming a 1% resistor match from cell to cell.

Combining in quadrature this current variation value with that shown in fig. 5 the net current variation is ± 0.6µA about the nominal current at the ± 3σ level.

4 Measured results

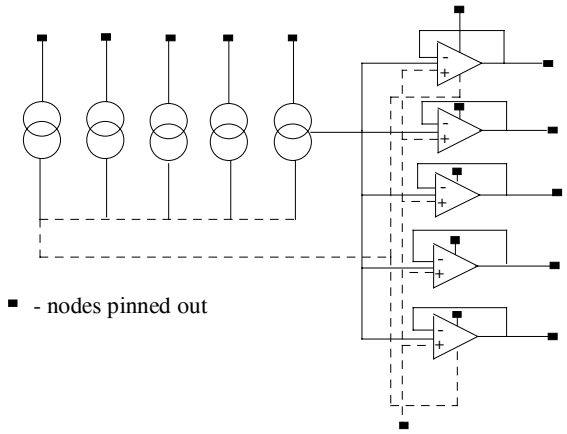

Figure 6: Schematic diagram of current reference chip cells

4.1 Test chip

Figure 6 shows a schematic diagram of a test chip which was fabricated to test the accuracy of the predicted current variation values. The chip consists of five current reference cells each identical to that shown in fig. 1. One of these reference cells was used to generate a bias current for five operational amplifiers. Ten chips were fabricated in total.

4.2 Fully on chip reference circuit

The average current drawn by all the current reference cells will give an indication of the accuracy of the prediction of absolute current value determined primarily by the value of the bias resistor, R1. The average measured value of reference current was 18.77µA measured over all current reference cells on all chips. Figure 7 compares this with the hand calculated and monte-carlo calculated results. Ideally several wafers from different batches should be

used to verify this prediction, but cost and time scale constraints made this impractical. Within these limitations the measured results are consistent with those predicted.

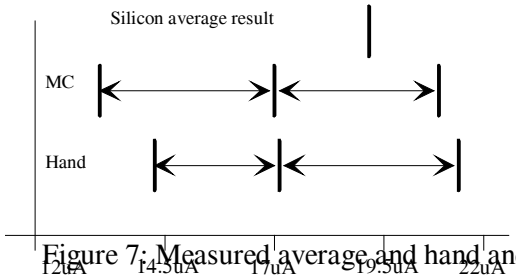

Figure 7: Measured average and hand and monte-carlo 3σ current values

4.3 Relative component variation effects

Measurement of the scatter on the current drawn by the five reference cells on one chip allows the total mismatch induced current scatter component to be determined. The average scatter of current values measured in this way over all chips at the ± 3σ level is 0.81μA in 18.77μA. Comparing this value with predicted scatter values of ± 0.6μA for hand calculation and ± 0.86μA for monte-carlo simulation. We can conclude that agreement between monte-carlo simulation and silicon is thus good although hand calculations are less accurate.

4.4 Fully off chip current source

All five operational amplifiers on one chip are biased from one current source, thus scatter of Iddq current values among these five operational amplifiers gives a measure of the accuracy of Iddq current which could be obtained from the use of a fully off chip reference circuit. The average measured scatter (at 3σ level) over all ten chips was 7.2μ A in 134.8μ A which amounts to approximately 5%.

5 Normal I_{DD} distributions

We can now conclude that absolute component variation has been shown to be the major cause of variation of current reference value on a standard CMOS process if a fully on-chip reference cell is used. If one (or more) components are taken off chip to improve accuracy then mismatch between components on chip has been shown to determine the accuracy by which an I_{DDQ} current can be determined.

For the fabrication process used by the authors, an approximate I_{DDQ} current definition accuracy of 5μ A exists. However, in many cases the transistors N1,N2 and P1,P2 in fig 1 will not be physically close and the net threshold voltage offset between them will be larger than those used in this paper. Temperature gradients across a chip will also become an important issue in this situation. Poorer definition of the I_{DDQ} current will result and an I_{DDQ} current definition error in excess of 5μ A will be observed.

6. Potential applications of I_{DDX}

It is likely that future applications of supply current monitoring will need to address the above problems as well as the relatively high quiescent current levels in many analogue circuits. In analogue design there is often a trade off between high speed operation and low power dissipation causing supply currents to vary between zero to several mA from design to design. Another point worth considering is the influence of the input signals. In most digital circuits, the inputs do not have a significant effect on supply current levels. This is not the case in many analogue designs. In an attempt to formalise the applicability of I_{DDX} techniques, three dominant design styles have been identified.

6.1 1. High I_{DD}

This tends to be a consequence of class A behavior of many circuits in which the output current can never exceed the bias current. Since the bias current is constant, either I_{DDQ} or I_{SSQ} are independent of the input signals. Some circuits which belong to this group are conventional two stage voltage mode comparators and amplifiers, one stage (folded-cascode) amplifiers or current mode blocks such as class A switched current memory cells.

6.2 I_{DD} a function of inputs

These circuits are designed to consume a low quiescent current whilst maintaining a high driving capability. They can source or sink current from a load which is greater than the bias current. This extra current is provided by the power supplies, either directly as is the case in class AB circuits (buffers, current conveyors, class AB memory cells etc) or via a dynamic or input dependent current source (dynamic and adaptive biasing amplifiers).

6.3 Low I_{DD}

These tend to be circuits that are driven by their inputs so that in the absence of input signals their quiescent current is practically zero. These circuits result from the combination of current mirrors without biasing currents, such as current mode maximum operators, current mode full wave rectifiers and some current mode A-D and D-A converters.

An intuitive analysis suggests that supply current testing will be more applicable to the latter two categories of circuits. A collaborative project between Lancaster University and CNM is in progress which involves an analysis of the effectiveness of I_{DDX} techniques for specific examples of circuits from each of the above categories. This will involve the application of results presented in section 3 to determine realistic pass/fail thresholds and the use of sensitivity analysis and IFA techniques to determine the effect of layout dependent defects on various supply current related parameters.

7. Conclusions

This paper has summarised a number of I_{DDX} techniques for analogue and mixed signal circuits and reported on results obtained from the evaluation of the effect of process variations on fault free quiescent current levels. It has been shown that the distribution of fault free quiescent current levels will be greater than +/-5% and that in most applications, especially where on chip reference current generation is used a pass/fail threshold of at least +/-20% should be used.

An initial attempt has also been made to categorise analogue circuits against supply current behavior with the aim of determining which circuit classes will be suitable for I_{DDX} techniques to be used.

8. References

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