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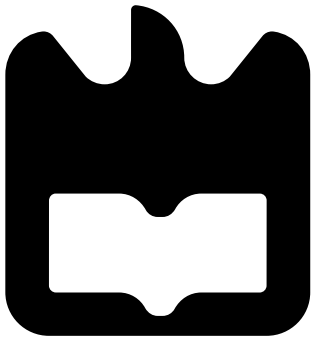
Amplificadores de Envolvente para Transmissores de Rádio Frequência



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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requesitos necessários à obtenção do grau de Mestre em Engenharia Electrónica e Telecomunicações, realizada sob a orientação científica do Doutor Pedro Miguel Da Silva Cabral, Professor Auxiliar Convidado do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro, e sob a co-orientação científica do Doutor José Carlos Esteves Duarte Pedro, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro

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agradecimentos / acknowledgements

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Resumo

Neste trabalho é feita a análise matemática de um amplificador comutado auto-oscilante, considerando a existência de um atraso de propagação e/ou histerese no comparador, por forma a garantir as condições de oscilação. Para validar este resultado teórico, diversas simulações são realizadas, e é descrito o projecto de um amplificador auto-oscilante. É montado um protótipo experimental e os seus resultados observados na prática são comparados com os obtidos quer pela simulação do circuito, quer pelo modelo matemático apresentado.

Abstract

In this work, the mathematical analysis of a switched self-oscillating amplifier is performed, considering a propagation delay and/or hysteresis in the relay in order to ensure the oscillation conditions. To validate this theory, several simulations are performed, and the design process of a self-oscillating amplifier is described. Then, a practical prototype is built, and its experimental data is compared against circuit simulation data and the results obtained using the proposed mathematical model.

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List of acronyms

ADC Analog-to-Digital Converter

ACPR Adjacent Channel Power Ratio

BJT Bipolar-Junction Transistor

BTS Base Transceiver Station

CMOS Complementary metal-oxide-semiconductor

DAC Digital-to-Analog Converter

DSP Digital Signal Processing

EER Envelope Elimination and Restoration

EMI Electromagnetic Interference

ESR Equivalent Series Resistance

ET Envelope-Tracking

EVM Error Vector Magnitude

FET Field-Effect Transistor

FM Frequency Modulation

FoM Figures of Merit

HSxPA High-Speed Upload/Download Packet Access

IMD Intermodulation Distortion

IP Intercept Point

LC Limit-Cycle

LDO Low Drop Out

LTE 3GPP Long-Term Evolution

LVDS Low-Voltage Differential Signalling

MOSFET Metal-Oxide-Silicon Field-Effect Transistor

NMSE Normalized Mean of the Squared Error

PA Power Amplifier

PAE Power Added Efficiency

PAPR Peak-to-Average Power Ratio

PWM Pulse-Width Modulation

RF Radio-Frequency

RF-PA Radio-Frequency Power Amplifier

SISO Single-Input Single-Output System

SMPA Switched-Mode Power Amplifier

SNR Signal-to-Noise Ratio

SOPA Self-Oscillating Power Amplifier

WCDMA Wideband Code Division Multiple-Access

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Chapter 1

Introduction

1.1 Project Context

Energy efficiency is a hot-topic nowadays. Particularly speaking about electronic systems, our world is now facing an unprecedented growth of devices which increase our global energy needs, despite the fact that the energy has never been as expensive as now.

Moreover, the ever-growing demands for performance also increase the energy requirements for such devices, establishing one of the main performance-limiting factors on the mobile-devices industry.

In the wireless communications industry, the power is also a very important factor. Not only on the mobile radios, but also in the fixed ones (e.g. base-stations) which need to cope with high Radio-Frequency (RF) power. The main problem comes from the fact that the average efficiency of Radio-Frequency Power Amplifiers (RF-PAs) is very low (about 30%), increasing the energy budget not only from the dissipated power, but also from the power needed to cool down the RF apparatus. Another downside, is the fact that the power needed to run such a base-station is too high to be completely fed from local energy-harvesting methods, e.g. photovoltaic cells, one of the main aims of the so called "Green Radio" [1],[2].

The efficiency problem on signal amplification has long been studied, and several classes of amplification have been developed [3] [4] [5], suggesting that switched stages in RF can be very efficient, reaching 80% of Power Added Efficiency.

Since the efficiency of traditional amplifiers is strongly dependant on the ratio between power-supply voltage over signal voltage, and, for example in a RF Class-A amplifier, a theoretical efficiency peak of 50% is achieved when the sine-amplitude equals the rail-voltages, it is important to select the optimum power-supply voltage for a particular input signal, in order to increase the overall Power Added Efficiency (PAE). However, this must be done without increasing too much the unwanted non-linear distortion of the amplified signal since amplifiers, when fed with input amplitudes near supply voltages, work in the gain-compression zone, producing distortion components at the output.

When designing RF output stages, the collector or drain bias of the amplifier is selected to maximize efficiency, yet, keeping non-linear distortion low. This is only feasible when the amplitude of the RF carrier has a low Peak-to-Average Power Ratio (PAPR). The drawbacks that arise from this are considerable: keeping signal's envelope constant, all the information has to be modulated within carrier's phase, reducing the bit-rate, hence, the spectral efficiency.

Reducing spectral efficiency is unwanted, since the wireless communications are demanding for more performance, mainly in the mobile market, and only spectrally efficient modulations are able to cope with these demands.

Moreover, it has been proven that the sum of constant-envelope uncorrelated signals result in high PAPR signals [6], which means that when the RF-PA has to amplify several constant-envelope channels, if it has been designed for a particular PAPR, the efficiency and linearity will degrade.

Two major techniques have been developed in order to cope with large PAPR signals, using envelope amplifiers to dynamically adjust the power supply voltage: Envelope Tracking [7] and the Envelope Elimination and Restoration [8]. For this, several approaches have been reported in the literature, for example [7], [9], [10], [11], among others.

One of the most interesting architectures, explored in [9] and [12], is the self-oscillation-based switched amplifiers. These amplifiers are very simple from the system's point of view, yet, they are capable of efficient and linear amplification of signals, namely, the base-band envelope.

Unfortunately, although several analysis can already be found in the literature for this kind of systems, none of them considered the signal propagation delay, which constitutes a significant limitation for their use in envelope amplifiers intended to operate at higher switching frequencies, and thus to process nowadays broadband signals.

1.2 Objective of this work

Indeed, the objective of this work is to derive the necessary conditions for the oscillatory behaviour, accounting for the propagation delay and hysteresis in order to predict the self-oscillating frequency, and the input-to-output quasi-static transfer characteristics. These are the two fundamental parameters needed to predict the Self-Oscillating Power Amplifier (SOPA)'s switching losses (and thus efficiency), bandwidth and non-linear distortion behaviour.

Moreover, an experimental envelope amplifier prototype will be designed and built, in order to test the theoretical results.

1.3 Synopsis

This Master Thesis is divided in four main chapters.

In Chapter 2, a general insight on RF power amplifiers is given. It will cover the main figures of merit, relevant output stages, switched modulation schemes, envelope amplification techniques, and two previous implementations of amplifiers.

In Chapter 3, the necessary conditions for the SOPA oscillation are derived. A single expression which accounts for systems with and without hysteresis is developed. Since some of the results suggest the feasibility of oscillation at higher frequencies when negative hysteresis exist, a relay with negative hysteresis is proposed and the main properties of a negative hysteresis SOPA investigated. Theoretical results predicted for a system with positive hysteresis, negative hysteresis and without hysteresis are successfully checked against simulated (in *Simulink*) data.

A similar technique is found in [13] which shares some of the oscillation conditions derived here. However, since the always present propagation delay is not considered in the closed-loop transfer function, the conditions in [13] lead to ambiguous solutions when the propagation delay is considered. Here it is proven that these predicted surplus solutions are not physically feasible.

In Chapter 4, a low-pass self-oscillating power amplifier will be object of design. Before design, important aspects will be pointed out, as well as possible output configurations. The design of the prototype will be described in detail.

In Chapter 5, the experimental results are presented against theoretical and simulated (SPICE) data, which validates the proposed mathematical model.

Final chapter draws the conclusions, and points out possible future work.

Chapter 2

State of the art

In this chapter, the major output stages used in power amplifiers will be briefly described.

Moreover, the two major architectures used to efficiently amplify RF signals with high PAPR, using envelope amplifiers, will be presented (Envelope-Tracking (ET) and Envelope Elimination and Restoration (EER)). Two practical examples using two different techniques are described (hybrid switched-linear amplifier, and stepped supplies amplifier).

Finally, the major modulation techniques used in low-pass switched-mode amplifiers are described.

2.1 Figures of merit of amplifiers

The design of a power amplifier emphasizes the power efficiency. This is due to the fact that power amplifiers deal with a large amount of power, so any percentage of dissipated power constitutes a large absolute quantity of wasted power, increasing the power budget of the system.

This gives a strong ecological and economical motivation for efficient DC-to-RF power conversion.

However, efficiency should not be the only concern, linearity is also a major concern as will be seen.

In order to compare different amplifiers, to aid the choice among different architectures for a specific application, several quantitative Figures of Merit (FoM) can be defined. Before continuing, some FoM of amplifiers shall be introduced.

2.1.1 Gain and efficiency

The gain of an amplifier can be formally defined in several ways (solely “formally“ different, because all gain figures depict the same system).

One of the simplest definition is only based on current or voltage gain. This approach is widely accepted when the input impedance of the amplifier is considered ideal (infinite for voltage amplifiers or zero for current amplifiers), hence, the input power is zero, making no sense defining the amplifier gain as ”power-gain“, being usualy defined in current or voltage gain.

However, when the input impedance of the amplifier is not ideal, the input power is non-zero. If the input power is non-zero, it is possible to define power gain, however efficiency calculation needs a slightly change. When the input power is zero, the efficiency is simply the ratio between the output power over the DC power. However, if some power is given to the amplifier through the input port, that power should also be considered as power supplied to the amplifier. This definition of efficiency is called Power Added Efficiency (PAE), and is simply the general case of the former definition. In RF amplifiers, since the loads need to be matched to avoid wave reflections, the input supplies some power to the amplifier, which requires the use of the PAE definition.

Other FoM include input impedance, maximum power, output impedance, and noise factor. Noise factor is a very important quantity when dealing with low power signals, since the Signal-to-Noise Ratio (SNR) could be severely degraded if low-noise design techniques are not employed.

2.1.2 Non-linear figures of merit

There are several other figures of merit [14], [15]. The most used are 1dB compression point, 3^{rd} order Intercept Point (IP), Dynamic Range, Sensitivity and, qualitatively, if it is memoryless or not. The analytical analysis of systems with memory (e.g. non-linear capacitances or inductances) is usually made through the use of Volterra series (when is possible to "extract" the kernel of the system).

2.1.3 The importance of linearity in power stages

Recalling the previous non-linear FoM, namely the 3^{rd} order Intercept Point, and from [14], the resulting IP of a cascade of non-linear elements numbered from 1 to M, where M-th element is the last one, can be calculated from

$$I_T = \left(\sum_{i=1}^{M} \frac{1}{\left(\prod_{k=i+1}^{M} G_k \right) I_i} \right)^{-1} \tag{2.1}$$

Which means that if the gain of the last stage is large (the case of power amplifiers), the overall system's IP is very dependant on the output-stage's IP. With this, one can conclude that the transmitter Power Amplifier (PA) should not only be very efficient, but also very linear, because it can compromise the linearity of the whole system. Assuring linearity is important to comply with spectral masks in order to avoid interference in adjacent channels, but also to avoid co-channel interference which degrades the transmitted signal, decreasing the SNR.

Several transmitter output-stage configurations exist. For the sake of objectivity, an exhaustive list will not be described here, neither a deep explanation on each configuration. Only the key aspects of the most general output stages used in wireless communications will be exposed. Note that although Bipolar-Junction Transistors (BJTs) will be used on

figures, that is a mere representation of the active elements, since they can be Vacuum tubes, Field-Effect Transistors (FETs) or any other similar devices.

Here, the output stages will be divided in two major groups: Envelope amplifiers, and RF amplifiers.

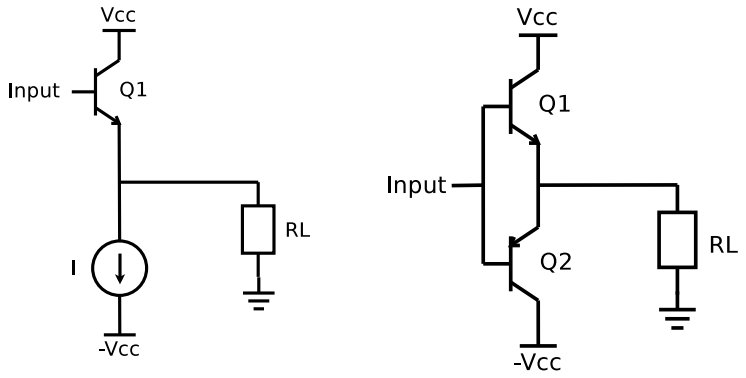
The first group of amplifiers work in Class-A, Class-B and Class-D and are characterized by the high linearity, and bandwidth which goes from DC to a few tens of MHz.

Additionally, the modern output stages of RF amplifiers work in Class-C or are solely based on conduction and cutoff of the active element, providing a theoretical efficiency of 100%. These efficient classes include Class-E, Class-F and Class-F^{-1}, and are characterized by a narrow bandwidth.

Since this work is based on a Class-D output stage, a deeper insight will be given on this type of output stage in Section 2.4.

2.2 Envelope amplification classes

2.2.1 Class-A



(a) Class-A output stage (b) Class-B and C output stage

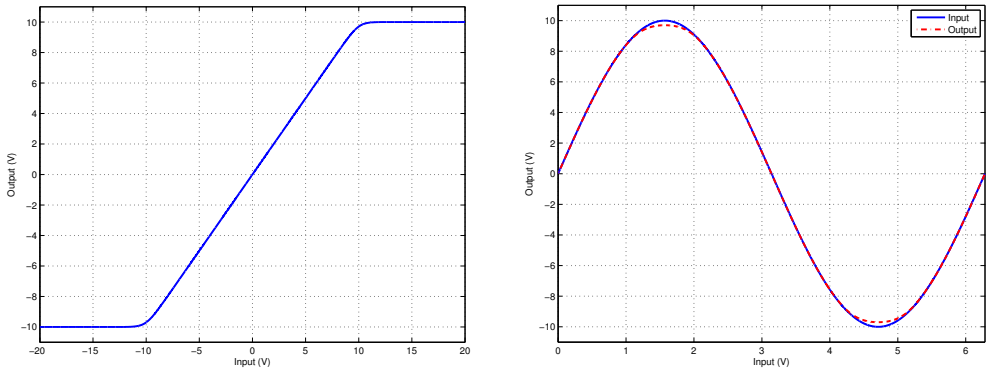
Figure 2.1: Circuit configurations for Class-A, Class-B and Class-C output stages. The only difference between classes B and C is the conduction threshold of the active devices.

In a envelope Class-A amplifier, the active element is always conducting. The basic circuit is depicted in Figure 2.1a. As it may be seen in Figure 2.3b, when the sine-wave amplitude equals the DC bias voltage (which is the saturation threshold) the efficiency is 25%.

The input/output characteristic can be seen in Figure 2.2, as well the output for a sine-wave with amplitude V_{cc}, where the saturation can be noticed.

Saturation occurs from two conditions: for high input voltages, transistor Q_1 saturates, for low input voltages, the current in the load equals the current sank by the current source, so the output cannot decrease more. In practical implementations, since the current source (in it's simpler configuration) is composed by a transistor, if $I \cdot RL$ is larger than V_{cc}, the current source saturates.

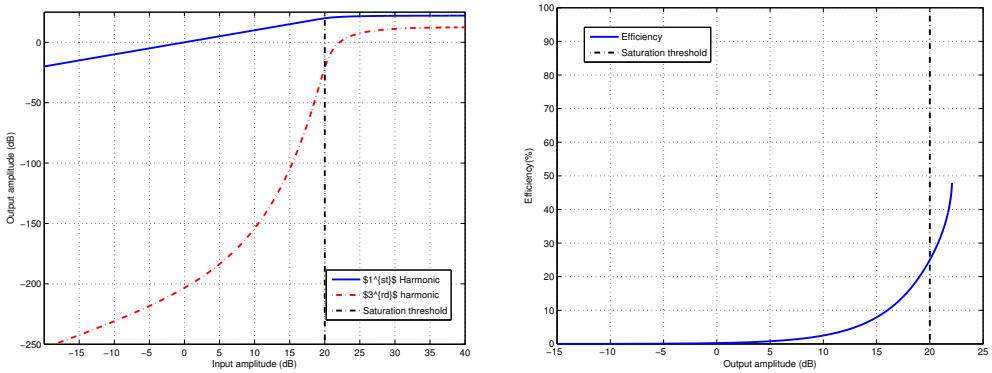
The distortion introduced by saturation can be measured (for example, by looking at the output's harmonics) and the result can be seen in Figure 2.3a, where the amplitude of the



(a) Input/Output characteristic (b) Output for a sine input

Figure 2.2: Class-A Input/Output characteristic. $V_{cc} = 10$V

third harmonic[1] is plotted.



(a) Gain and IMD curves (b) Efficiency

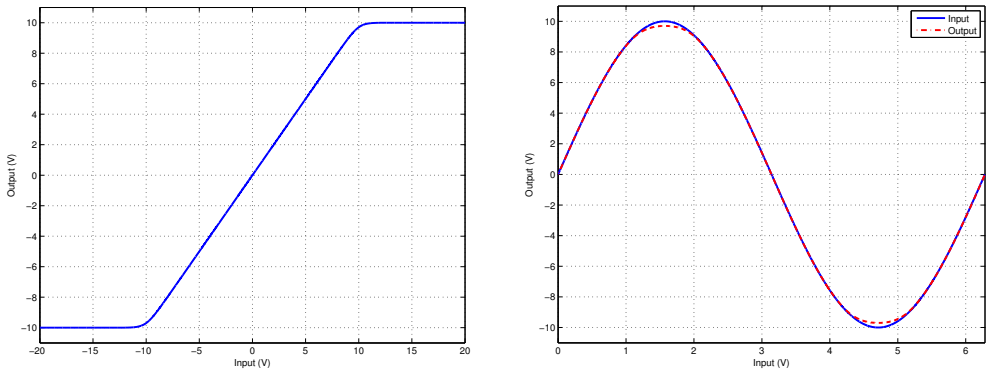
Figure 2.3: 1^{st} and 3^{rd} harmonics amplitude, and efficiency curves for a Class-A output stage. $V_{cc} = 10$V

[1]Looking at the third harmonic amplitude of the output of a memoryless non-linear system, is an indirect mean of measuring the coefficients of the intermodulation products

2.2.2 Class-B

A Class-B amplifier, on the other hand, is composed by two active elements, and each one of them only conducts when the input is positive or negative, respectively – refer to Figure 2.1b. The conduction angle of the Class-B amplifier is defined as $2\theta = \pi$, because for a unbiased sine-wave each active element conducts π radians. The input/output characteristic of an ideal Class-B output stage is the same as a Class-A, being efficiency the only difference. The instantaneous dissipated power is $[(V_{cc} - |V_o|) \cdot |I_{out}|]$, instead of $[(V_{cc} + V_o) \cdot I]$ for every V_o, plus $[(V_{cc} - V_o) * I_{out}]$ for $V_o > 0$, as is the case of Class-A operation. For ideal Class-B output stage, I consider that the conduction threshold of the active component is zero, if it is not, as shall be presented later, it would ensemble a Class-C output stage.

The efficiency and gain over input power, can be seen in Figure 2.4, and the peak efficiency is $\frac{\pi}{4} \approx 78.5\%$ when the input amplitude equals V_{cc} (which is $20log_{10}(10) = 20\text{dB}$), signalled as the saturation threshold. Note that the graph is plotted against the amplitude of the output sine-wave component at the same frequency as the input, that means that for a large input sine-wave (i.e. square wave at the output) the output amplitude would be $\frac{4}{\pi}V_{cc} = 22.1\text{dB}$, which is the largest possible.



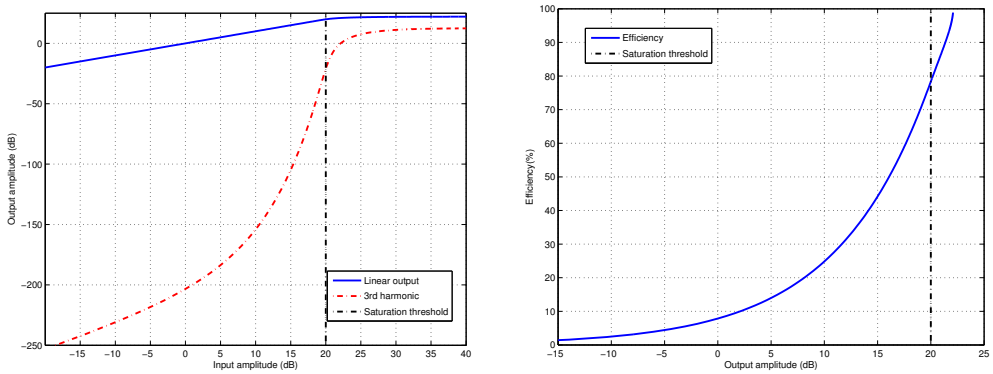
(a) Input/Output characteristic

(b) Output for a sine input

Figure 2.4: Class-B Input/Output characteristic. Note that it resembles the Class-A characteristic. $V_{cc} = 10\text{V}$

Usually this class is approximated by what is called "Class-AB", which is a particular case where – since the conduction threshold of real active components is larger than zero – active devices are biased in order to cancel the conduction threshold. This makes the conduction angle of the stage be $2\theta > \pi$.

To keep the overall Error Vector Magnitude (EVM) low, envelope amplifiers have to be driven in low distortion regions. However, their power dissipation may become unbearable for high-power operation (e.g. Base Transceiver Station (BTS)) or efficiency-critical applications (e.g. mobile devices). This requires the envelope to be amplified with efficient and linear amplifiers.



(a) Gain and IMD curves

(b) Efficiency

Figure 2.5: 1^{st} and 3^{rd} harmonics amplitude, and efficiency curves for a Class-B output stage. $V_{cc} = 10\text{V}$

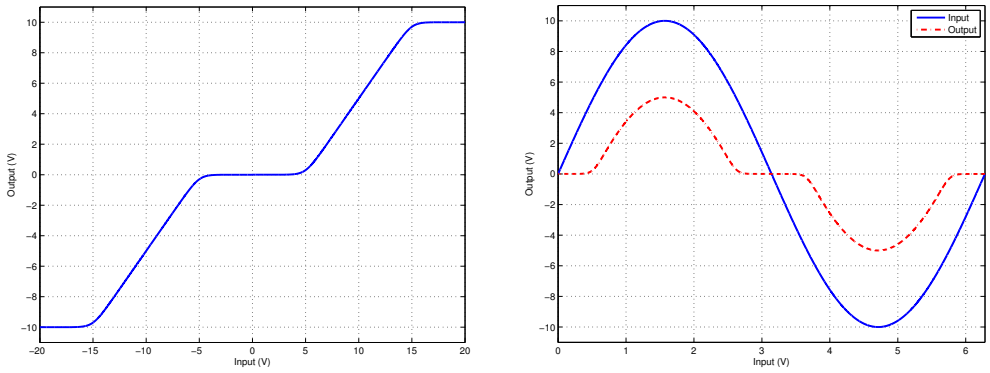
2.3 Efficient RF amplification classes

2.3.1 Class-C

One possible Class-C circuit configuration can be seen in Figure 2.1b, where the only difference from Class-B is the conduction threshold of the active elements which is larger than zero (which is the case for regular BJTs).

Class-C RF amplifiers are more non-linear than RF-Class-A or RF-Class-B amplifiers, since the active elements only have a conduction angle $2\theta < \pi$. This makes the unfiltered output of a Class-C amplifier fed with a sinusoid ensemble the wave depicted in Figure 2.6b. Since these are used in RF, the introduced distortion is easily filtered by band-pass filters. As can be seen in Figure 2.7b, the efficiency plots of Class-B and Class-C stages are not much different (being Class-C slightly more efficient), however, Class-C exhibits a phenomena that makes it usable at high-efficiency output amplitudes: for a specific range of amplitudes, the distortion shows a notch (refer to Figure 2.7a). This makes the Class-C more efficient than the other two classes (RF-Class-A, and RF-Class-B) in a practical point of view.

The notch only appears in the Class-C stage, because the input/output characteristic has an expansive behaviour for low amplitudes, and compressive behaviour for high amplitudes. This makes the coefficient of the 3^{rd} order product to be positive, while the coefficient of the 5^{th} order product is negative (instead of both being negative, as would be in a function which is compressive over all input range). This allows, for a specific amplitude, that both components cancel each other, leaving only all other odd-numbered Intermodulation Distortion (IMD) products[2], which are much lower.

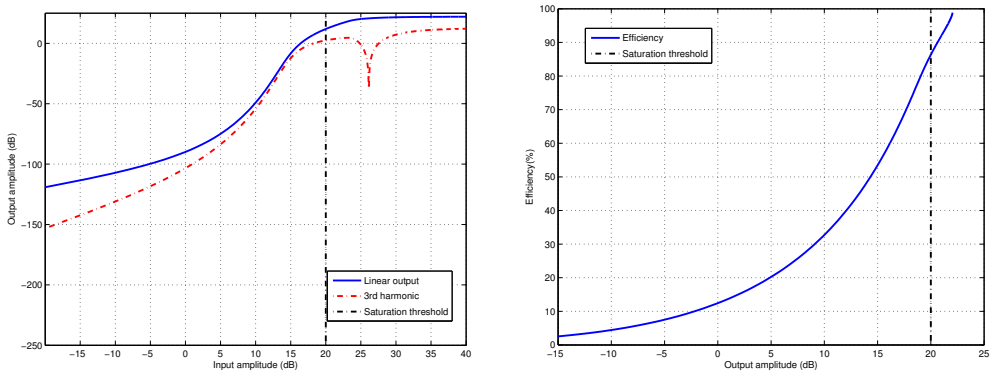


(a) Input/Output characteristic

(b) Output for a sine input

Figure 2.6: Class-C Input/Output characteristic

[2]Only odd-numbered, since the input/output characteristic is an odd-function, the coefficients of the even powers are zero.



(a) Gain and IMD curves

(b) Efficiency

Figure 2.7: 1^{st} and 3^{rd} harmonics amplitude, and efficiency curves for a Class-C output stage. $V_{cc} = 10\text{V}$

2.3.2 Class-E, Class-F and Class-F^{-1}

These are high-frequency switched stages (at the frequency of the RF carrier), on which only phase-modulation is employed. The switched transistor output is terminated to cancel specific harmonics, so that the current and voltage waves do not overlap in time. This way, high efficiency can be obtained. In practice, these classes are able to reach more than 80% of PAE, [3], [5], [16].

In Figure 2.8 a Class-E amplifier is depicted, as it was first presented in [3].

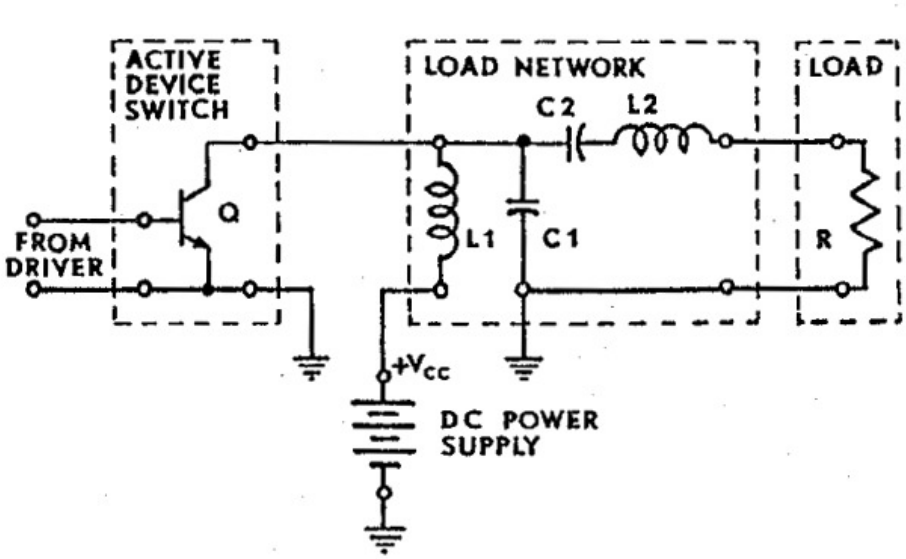


Figure 2.8: Circuit configuration for a Class-E output stage. Source: [3]

2.4 Class-D

Class-D is based on high-frequency switching – higher frequency than the highest frequency of the signal, which is a low-pass signal – such that the low-pass energy is varied (using Pulse-Width Modulation (PWM)) in order to track the input signal. Although the output stage works in strong non-linear states (cut-off and conduction), the overall system behaviour at the frequencies of interest has very low (i. e. controlable) distortion.

Since this kind of output stage aims the output of continuous amplitude signals, proper modulation should be made. Refer to section 2.5 for an insight on major modulation schemes used.

2.4.1 Output filtering

Output filtering is one of the key aspects on switching stages, since it is responsible to increase the efficiency of the switching modulation techniques. Please note that the efficiency being mentioned is the modulation efficiency. To understand what this is, please note that the output stage is efficient as long as the switching losses are near zero. However, if the

output contains power out-of-band beyond the amplified signal, that also must be accounted to calculate overall efficiency, since it is not useful power.

As can be seen in Section 2.5, one consequence of the non-linear behaviour of these modulation schemes is that the output has much more spectral components than the actual input. As a consequence, the unfiltered output has unwanted power beyond the amplified signal. The filtering is critical to ensure that the power is reflected back to the power-supply, i.e. since the input impedance of the low-pass filter is very high at high frequencies, the delivered power at those frequencies is low.

This way, if the modulation scheme has significant components above the cut-off frequency – as usual, since the amplifier switches at a very high frequency – the filter should make the modulation scheme to be approximately 100% efficient.

2.4.2 Feedback

Feedback is crucial to reduce the non-idealities[3] of the forward-path, namely the output stage and the non-linearities of the output filter. When feedbacking the output, stability ought to be checked not only at the low-pass frequencies, but also at the switching frequencies.

However, in this work, feedback will be used to destabilize the system – to provide dithering at the input of the system, allowing a quasi-linear operation without the use of a precision local oscillator/triangle-wave generator – as well as to reduce the forward-path non-idealities.

[3]Non-idealities like power-rail asymmetry for example.

2.5 Modulation Techniques

The main requirement of a modulation scheme used in low-pass switching amplifiers (as the Class-D), is that the switching output includes the input spectra, such that the amplified input can be obtained using passive (and efficient[4]) filters – the so called reconstruction filters.

By switched-mode output, it is understood that the output has a stepped characteristic, either in current or voltage, such that the switching element dissipates minimum power in steady state (conducting current when the voltage across its terminals is zero, or not conducting any current when the voltage across its terminals is non-zero).

To modulate continuous amplitude signals using discrete amplitude ones, amplitude-to-time modulations are performed. This implies that the output amplitude resolution is dependant on the time resolution.

For practical purposes, two-voltage-levels are used. Firstly, voltage levels are used instead of current levels because it is easier to deal with voltage sources. Secondly, two levels are usually used because it simplifies the system (it is a simple push-pull half-bridge) or, more rarely, three levels can be used (as is the case in a full-bridge configuration).

In this chapter, some modulation schemes used in switched-mode output stages will be presented, alongside with system-level descriptions of the modulating systems. Recall that no demodulation systems are required, since that task must be carried out solely by passive filters.

2.5.1 Pulse-Width Modulation

Pulse-Width Modulation (PWM) is constituted by a stream of width-modulated pulses, spaced in time by a constant period.

In Figure 2.9 the system-level schematic of a PWM modulator can be seen. One of the main advantages of it, which widespread its use, is the fact that it works well in open-loop (dismissing any feedback for reasonable modulation), and it is quite predictable.

The amplitude-to-time conversion is made simply by comparing the input signal with a locally generated triangular wave.

In [17] the spectral components of a clocked pulse-width modulated signal were calculated, using the Bessel series expansion, and the results are very close to cited simulation data, which makes it a good method to predict the effect of PWM modulation over frequency domain.

2.5.2 $\Sigma\Delta$ Modulation

$\Sigma\Delta$ (Sigma-Delta, or Delta-Sigma) modulation was developed to digitally encode analogue signals. However, since the output of a $\Sigma\Delta$ modulator includes the spectra of the input, regular reconstruction filters can be used to filter it out efficiently in the analogue domain.

A significant amount of theoretical work has been developed on $\Sigma\Delta$ modulators, either in Analog-to-Digital Converter (ADC)s or Digital-to-Analog Converter (DAC)s, mainly because there is a characteristic that attracted a lot of attention - it shapes the quantization noise. To better understand this, lets look at a simple first-order $\Sigma\Delta$ modulator in Figure 2.10.

[4]By efficient, it is meant that the filter does not include dissipative elements besides the load.

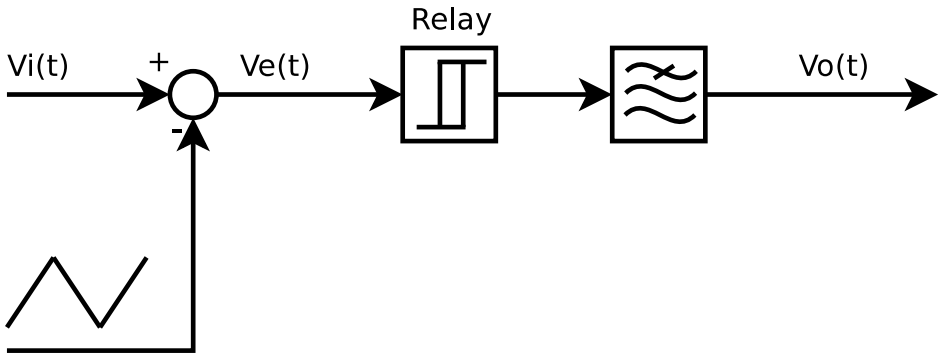


Figure 2.9: Simple open-loop Pulse-Width Modulator

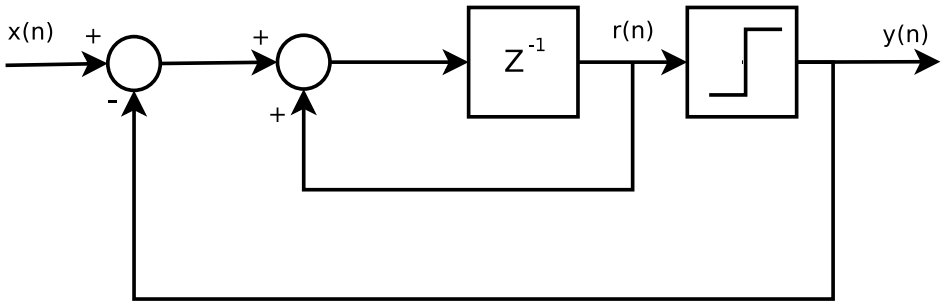


Figure 2.10: $\Sigma\Delta$ Modulator

One method widely used to analyse this system, which can be seen in [18], is modelling the 1-bit quantizer as a sum between it's input and some uncorrelated noise $e(n)$. It has been experimentally observed that despite the fact that the behaviour of the comparator by itself yields the input plus distortion (i.e. correlated "noise"), the system's overall behaviour matches the predictions made with this model.

From this assumption, the output will be split in two parts, $y(n) = y_x(n) + y_e(n)$, relative to the signal and error, respectively. From this, closed-loop gain for each of the input signals ($x(n)$ and $e(n)$) can be calculated in the Z domain, yielding

$$Y_x(z) = \frac{\frac{z^{-1}}{1-z^{-1}}}{1+\frac{z^{-1}}{1-z^{-1}}} Y(z) = z^{-1}Y(z)$$

$$Y_e(z) = \frac{1}{1+\frac{z^{-1}}{1-z^{-1}}} = (1-z^{-1})E(z)$$

Using the transform $Z \Rightarrow e^{2\pi j \frac{f}{f_s}}$, $\quad Y_e(z)$ yields

$$Y_e(f) = 2je^{-\pi j \frac{f}{f_s}} sin\left(\pi \frac{f}{f_s}\right) E(f)$$

which means that the quantization noise is shaped like a sine in the frequency domain, having the zero at DC and the maximum at $\frac{f_s}{2}$.

But how is the output of a $\Sigma\Delta$ modulator? Is it periodic? And more: how does the output for a DC input look like, since it is supposed to have no error, considering the noise shaping formula? These are important questions to figure out the differences between $\Sigma\Delta$ and the modulation scheme of the SOPA.

Considering that the $\Sigma\Delta$ modulator only has two levels (0,1), that it is fed with a constant input $x(n) = x_i$, and that in $t = 0$ the accumulator state is zero, then at each clock edge k, the accumulated value in the integrator is equal to $Nx_i - n_1$ where n_1 is the number of '1' bits since the last time that the state of the accumulator has been zero, and N the number of total bits since then. One bit, is, of course, each rectangle pulse, of duration $\frac{1}{T_{clock}}$, since the $\Sigma\Delta$ modulators are, clocked.

From this, the period of the output can be calculated, since the periodic condition would be

$$Nx_i - n_1 = 0$$

which is the case when the initial condition is reached again. Simplifying yields

$$N = \frac{n_1}{x_i}$$

It is possible to conclude from this equation that the output is only periodic if x_i is a rational number, and that the period would be the denominator of the reduced fraction.

Moreover, when modulating DC signals, this type of modulator has the best period (i.e. the period which yields zero error at the end of each period).

In order to test this hypothesis, two simulations were made with two different DC inputs x_i: a rational number (Figure 2.11), and an irrational number, to see if the output is aperiodic in the last one (Figure 2.12).

One can conclude that the $\Sigma\Delta$ modulator yields a periodic output when the input is rational (2/5), being the period the reduced denominator (5bits), as is clearly seen in the frequency domain.

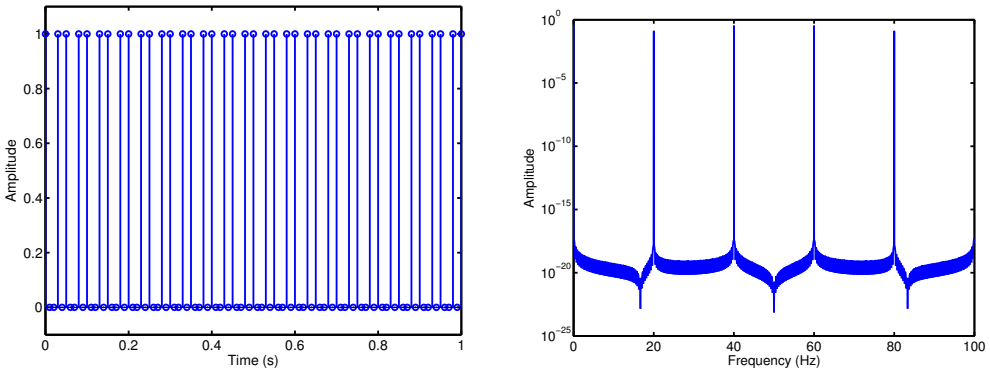
On the other hand, with the irrational number as input, the output is aperiodic, as is seen in the frequency domain plot of Figure 2.12.

One problem of using this type of system in analogue domain is the fact that the reconstruction filter requires a pure integrator, which is inefficient. However, other architectures exist, namely with low-pass or band-pass characteristic [18]. These architectures have different noise-shapping formats, namely with the zero-noise centred at a non-zero frequency, for the case of a band-pass sigma delta.

These data converters are used with sampling frequencies much higher than the Nyquist frequency of the input signal in order to reduce quantization noise in the signal band. Moreover, higher order modulators increase the noise-shaping, being the noise shaping function of a n-th order modulator $(1 - z^{-1})^n$. Just for the sake of completeness, one of the major challenges in the design of delta-sigma converters of order greater than three, is the stability.

The SNR obtained in a converter like this, for the signal bandwidth, is

$$SNR = 6.02 * N_{eq} + 1.76$$



(a) Output signal in time domain (b) Output signal in frequency domain

Figure 2.11: Output of a first-order $\Sigma\Delta$ modulator, for a rational DC input $x_i = \frac{2}{5}$. The period is exactly 5 bits, and it is clearly not a PWM signal since two pulses exist for each period, instead of one. The simulation time was chosen tacking into account the signal period, to reduce spectral regrowth artefacts. $T_{clock} = 0.01$ (s) Simulation time : 99.89 (s)

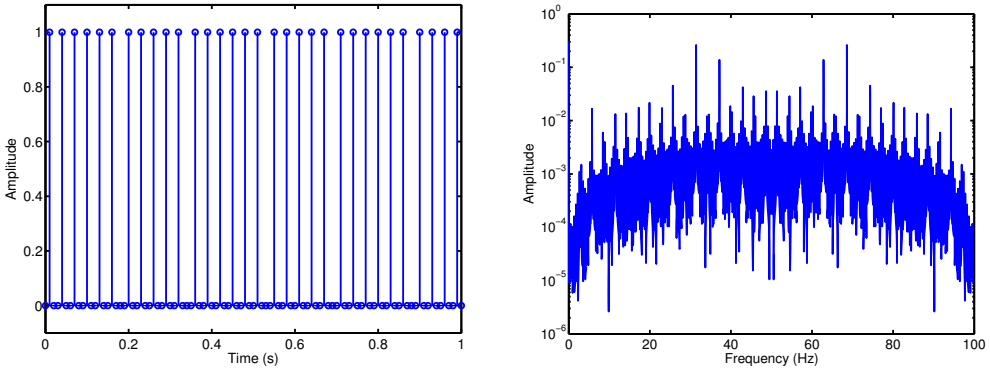
where N_{eq} is the equivalent number of bits. For a 1-bit 1^{st} order converter, the number of equivalent bits is 1 when no oversampling exists, and increase by one at each quadruplication of oversampling ratio [18].

2.5.3 Alternative Modulation

Another possible way to represent signals is by changing not only the duty-cycle, but also the frequency.

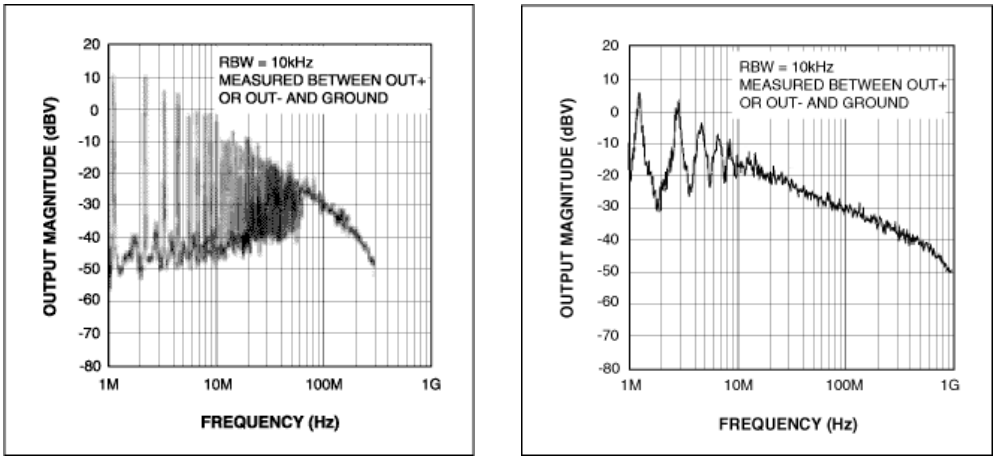
Frequency modulation does not change the output mean value. However, one of the advantages of a system which modulates a signal this way its the simplicity, as is illustrated in Section 3.1.

Moreover, according to [19], the use of a spread-spectrum modulation instead of a fixed-frequency modulation improves the Electromagnetic Interference (EMI) performance of this kind of amplifiers. Refer to Figure 2.13 for a quantitative comparison, where it is clear that the power peaks are much lower, result of the spread of EMI power along the spectre due to Frequency Modulation (FM) of the dithering signal.



(a) Output signal in time domain (b) Output signal in frequency domain

Figure 2.12: Output of a first-order $\Sigma\Delta$ modulator, for a irational DC input $x_i = \frac{\pi}{10}$. Although the time domain excerpt shown is too small, the frequency domain of the full simulation data shows the aperiodicity. $T_{clock} = 0.01$ (s), Simulation time : 100s



(a) Spectrum in fixed-frequency mode (b) Spectrum in spread-spectrum mode

Figure 2.13: Output spectra comparison between a fixed frequency and a spread spectrum PWM modulator (MAX9700) Source: [19]

2.6 Efficient RF system topologies

In order to amplify signals while keeping the distortion levels low, the classes A and AB[5] are the best suited, however, has have been shown before, they are very inefficient, even more when working near the quiescent point (i. e., for small-signal amplitudes). One simple way to increase efficiency at the expense of sacrificing linearity is to use those classes slightly saturated (which is called "back-off"), where they are more efficient and where, for the case of Class-C amplifiers, the superposition of IMD products yields a distortion valley at the high-efficiency amplitudes, as can be seen in Figure 2.7a.

Unfortunately, since the IMD valley is narrow, and real signals are composed of a carrier modulated with a stochastic range of amplitudes, this absolutely null IMD can never be obtained and distortion inevitably increases.

However, some techniques have been developed to reduce distortion, as long as the input/output characteristic of the amplifier is still injective, using pre-distortion. Pre-distortion translates the input of the system to the input the amplifier would need, to give the desired output. There are several architectures (some of them quite sophisticated, employing adaptive systems) but the basic concept is simply to mimic the inverse of the PA input/output characteristic. When designing a system with pre-distortion, the additional power consumed by the Digital Signal Processing (DSP) reduces overall system efficiency and thus should be taken into account.

2.6.1 Envelope Elimination and Restoration and Envelope-Tracking

As was seen before, for classes E and F, constant envelope signals can be effectively amplified. However, constant envelope modulations generally have low spectral efficiency, and are not used in modern high-performance wireless communications, such as Wideband Code Division Multiple-Access (WCDMA), High-Speed Upload/Download Packet Access (HSxPA) and 3GPP Long-Term Evolution (LTE), where hybrid modulations (employing amplitude and phase modulation schemes) are used, to form constellations up to 64-QAM [20].

To cope with envelope-varying signals in an efficient way, one can use an RF power amplifier with a regular output stage (such as Classes A, AB, B, C, E, F, and F^{-1}), and bias its V_{cc} dynamically, using an envelope Switched-Mode Power Amplifier (SMPA), as in Figure 2.14. This way, as the input signal envelope varies with time, the ratio $\frac{Vin}{Vcc}$ is kept near 1[6], to reach the maximum of efficiency. The overall efficiency is calculated by making the product of both efficiencies, which, for two amplifiers having 80% efficiency, yields 64%, which is much lower, and constitutes a stronger motivation to increase the efficiency of the envelope amplifier even further.

If the envelope SMPA is able to amplify with low distortion, the RF amplifier stage can be driven into saturation and cut-off (increasing efficiency), like a Class-E, where the input is only the phase up-converted to RF. The envelope is then restored from the bias, thus, this is called EER.

A less strict approach, is by making the bias roughly track the envelope, requiring the final RF stage to be fed with the full baseband modulated RF signal. This approach is less

[5]Class AB is just a practical implementation of a pure Class-B output stage

[6]Or higher than one for a Class-C amplifier, to bias the amplifier in the "sweet spot".

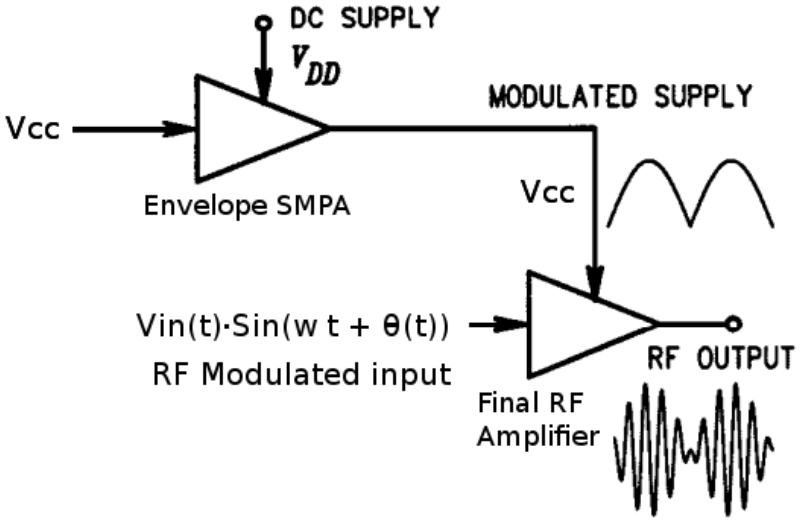
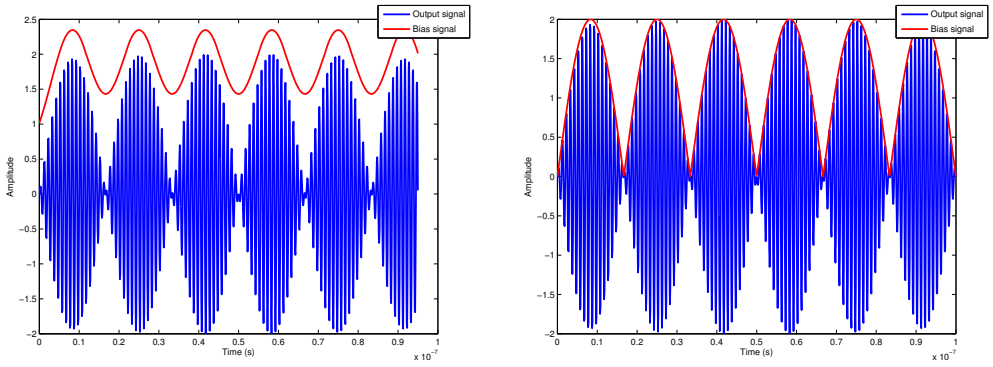


Figure 2.14: Dynamic bias system overall. Here w refers to the carrier frequency, and θ is the phase-modulating signal.

efficient, however it does not require so much performance (i.e. bandwidth) from the envelope SMPA, as can be seen in Figure 2.16, neither time-delay matching.

EER was introduced by Leonard R. Kahn [8]. Instead of feeding the amplitude information to the input of the RF amplifier, the amplitude information is removed[7] and it is restored back by dynamic biasing the final amplifier with the amplitude of the envelope.

Both techniques are depicted in Figure 2.15.



(a) Envelope Tracking (b) Envelope Elimination and Restoration

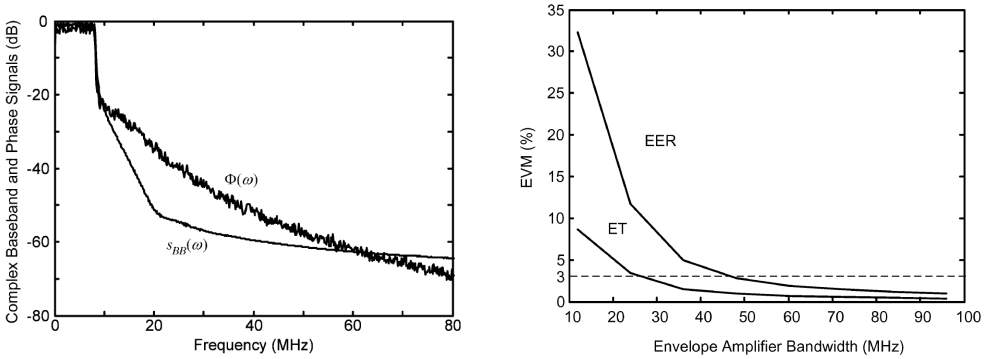
Figure 2.15: Both bias schemes, for the same output, for the ET and EER architectures

Although these approaches employ the same dynamic-bias principle, ET architecture does not need to ensure perfect delay-matching between the signal and the envelope branches

[7]Nowadays, since the signal is generated by DSP, it is not needed to remove the amplitude information of the signal. The DSP can digitally split the phase and amplitude information from the signal, hence the name *Polar-transmitters*

since it does not remove the amplitude information from the signal fed to the final amplifier, and keeps the final RF amplifier in active mode. On the other side, in EER, since phase and amplitude information is split and joint again, the timing of both signals should be as matched as possible. The effect of propagation-delay mismatch between phase and amplitude signals was modelled and experimentally verified [21], and suggests that to obtain a carrier to IMD ratio of $40dBc$ requires a maximum propagation mismatch of $\frac{0.05}{B_w}$ where B_w stands for base-band bandwidth. The cited graph can be seen in Figure 2.17.

In [22] some simulations were performed, in order to check the bandwidth of phase and amplitude of the baseband signal, and to compare the bandwidth requirements for both architectures. Results can be seen in Figure 2.16.



(a) Spectra of the complex baseband signal (phase and envelope)

(b) EER and ET bandwidth

Figure 2.16: Simulated envelope amplifier bandwidth requirement for an 802.11g signal in ET and EER systems. The required EVM is 5% for WLAN 802.11g PA. Source: [22]

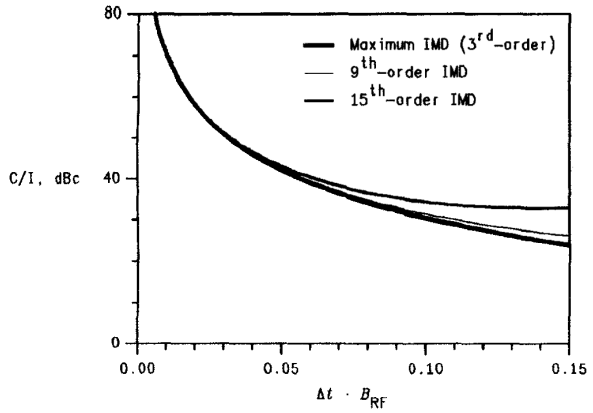


Figure 2.17: Effect of propagation-time mismatch between phase and envelope. Source: [21]

2.7 Envelope Amplifiers

There are several architectures for the envelope amplifier. Despite the fact that it can be a linear amplifier, only quasi-linear and switched-mode amplifiers will be discussed in this section, since those are the most efficient amplifiers known.

2.7.1 Quasi-linear Envelope Amplifiers

The main principle of quasi-linear amplifiers is by making an hybrid out of a SMPA joint together with a linear stage. While the switched stage delivers the bulk of energy, the linear has a much wider bandwidth, correcting the non-linearities and removing ripple (i.e. removing the error between the input and the output signals). The nomenclature is taken from [23], where a the principle is applied to constant-output DC-DC converters.

One of the most important parts of this scheme (besides the design of the linear and switched-mode amplifiers) is the power-combining method, which should be efficient.

Since in [23] the power combining is made using Low Drop Out (LDO) linear regulators, which, despite the fact that the ones employed are LDO, will inevitable dissipate more power because the linear stage is constantly delivering DC power, and not only surpassing the ripple. I will not refer to that work any more, but use the nomenclature presented.

The main quasi-linear architecture that will be exposed here is the one presented by [22], which composed the Ph.D thesis [9].

First of all, the power combining is made through a reactive component, thus making the power combining very efficient. Moreover, the switched-mode section of the envelope amplifier delivers the low-pass power, while the linear stage only conducts the band-pass power above.

The circuit-level schematic can be seen in Figure 2.18

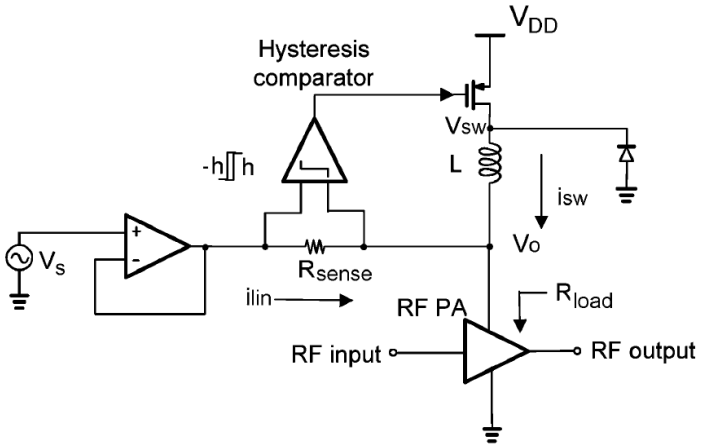


Figure 2.18: Circuit of the quasi-linear EER system. Source: [22]

This system is an interesting implementation of a linear amplifier which is aided by a switching stage in order to improve its efficiency.

As can be seen, for a DC output V_o, when the current sourced by the switching stage increases above $\frac{h}{R_{sense}}$, the switching stage turns on, and the inductor starts to integrate $\frac{1}{L}(V_{sw} - V_o)$ as current, making the current of the linear stage to decrease (since the current sank by the load is constant $\frac{V_o}{R_{load}}$), making it start to sink current, until the threshold $\frac{-h}{R_{sense}}$ is crossed, turning off the switching stage and decreasing the inductor current with the slope $\frac{-V_o}{L}$. This is a complete oscillation period of this aiding SOPA.

Refer to Appendix A for further analysis concerning this system.

Another implementation, employing a stepped source configuration of switching stages have been presented in [7], where several switching elements contribute with different current slopes, and the linear stage, as in before, corrects the error, delivering a small amount of energy.

2.7.2 Switched Envelope Amplifiers

Switched-only architectures have the advantage of efficiency, so, the hybrid linear-switched configurations are foreseen as a medium or short-term solution, at least for the $20MHz - 40MHz$ bandwidth of the baseband signals used nowadays in commercial mobile communications.

There is at least one very interesting switched-only implementation in [12], where a 8GHz SOPA is implemented. The design of a SOPA oscillating at this frequency is not straightforward, since the wavelength of the signals involved became very small, requiring (as is the case) an integrated solution, where the passive devices available are very limited.

To understand why does the size of the circuit is a determinant factor when it comes to the oscillation frequency, please refer to the Chapter 3.8, where it is proven that a stable oscillation occurs, at most, with an oscillation frequency $F_{osc} = \frac{1}{2\tau}$, where τ is the propagation delay across the feedback path. So, to keep a stable oscillation at 8Ghz, considering the wave speed to be $0.8c$, the largest loop size would be 30mm, which is very small, considering that the loop is composed at least by a comparator, an output-stage, an output-filter and the feedback path (which may also include a filter).

Chapter 3

System Analysis

In this chapter, the mathematical background for analysis and design of a SOPA will be developed in order to predict the behaviour of a Limit-Cycle (LC) system like the one depicted in 3.2, taking into account the inherent propagation-delay (which can only be neglected when the idle-state oscillation period is much larger that it) and hysteresis, which, as will be seen, can be used as an artificial means of controlling the oscillation frequency.

This allows a more realistic analysis because, even if one could develop a system with negligible hysteresis, allowing a near-pure phase-shift system behaviour, the propagation-delay must be taken into account when designing one with hysteresis operating at high frequencies.

In order to predict the behaviour of the system, time-domain analysis (using classic theory and state-space representation) will be done.

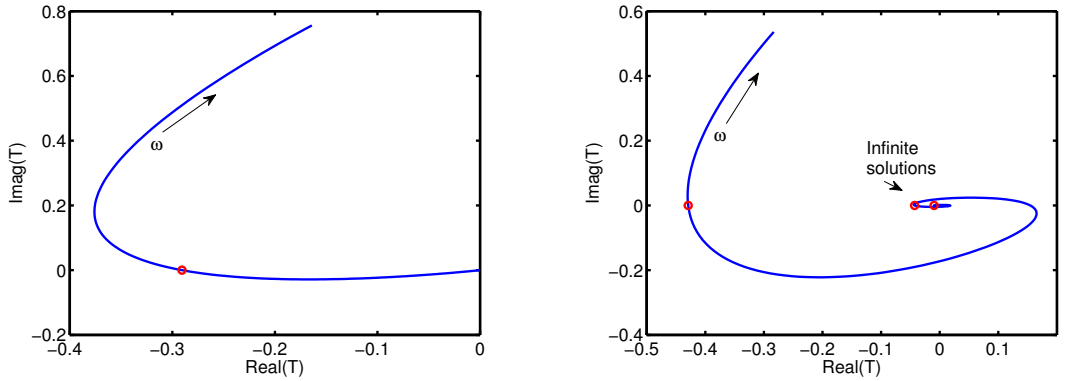
The same principle used to determine the main oscillation condition is used in [13] and the Tsypkin's method [24]. However, one crucial condition is not specified in those works, which fails when a propagation delay is considered. When applying those methods in systems with a propagation delay, several solutions exist, and no condition is given that eliminates the feasibility of the excess solutions (which are impossible, according to (3.33), derived in this work).

To demonstrate that the previous cited works fail, I will pick the Tsypkin's method, and show the behaviour with and without propagation delay. According to Tsypkin, a valid solution requires that the imaginary part of $T(j\omega)$, the Tsypkin's locus, is zero, and that the real part of $T(j\omega)$ is negative. Moreover, the imaginary part must increase with frequency.

3.1 System Architecture

The system analysed is depicted in Figure 3.2. It is easily observed that for a stationary input, the system is unstable (Figure 3.3).

Since the system converges to a periodic state when stimulated by a stationary input, all the system equations must be true at least for one periodic output signal. Starting from that principle, the necessary conditions will be obtained, which will lead to the determination of the oscillatory solutions.



(a) Tsypkin's locus without propagation delay

(b) Tsypkin's locus with propagation delay

Figure 3.1: For the case of a system without propagation delay, the Tsypkin's conditions only address one possible frequency. However, when a propagation delay is inserted, infinite solutions exist.

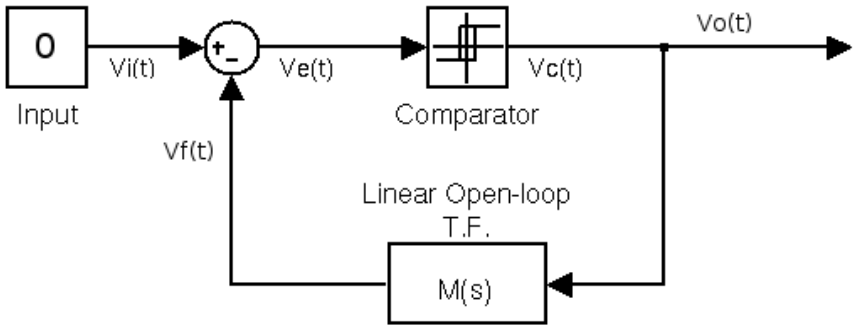


Figure 3.2: System architecture. The linear filter may include a propagation delay, or positive feedback.

3.2 Classic-theory Method

Defining the comparator block equation:

$$V_c(t) = \begin{cases} 1 & \text{if } V_e(t) >= 0 \\ -1 & \text{if } V_e(t) < 0 \end{cases} \tag{3.1}$$

In order to calculate the output of the system, the solutions of the equation $V_e(t) > 0$ must be calculated to evaluate the output of the comparator $V_c(t)$, which will allow us to the determine the output of the filter $V_f(t)$. A time-step transient simulation can give us reasonable results, however it is computationally costly. Some improved simulation techniques have been developed [12], [25], [26] however, all concern to higher-order output filters, and little attention is given to propagation delays.

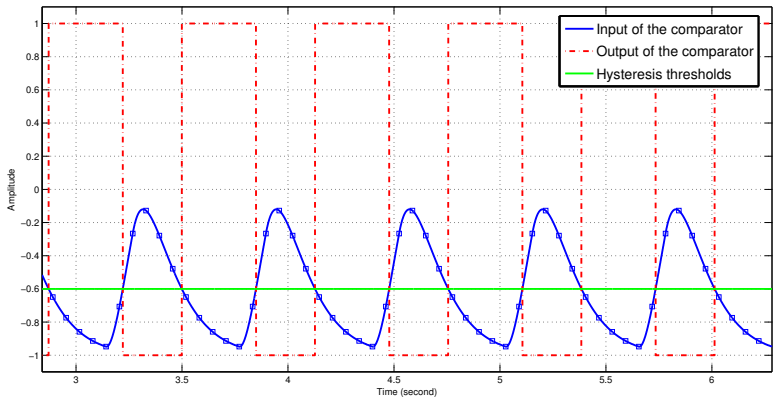


Figure 3.3: Output and input waveforms of a periodic solution of the system. The hysteretic thresholds are also depicted.

The method about to be used allows one to quickly obtain the oscillatory solutions, easing the use of sweeps along a determined system variable using numerical computation tools.

The output of this kind of system when excited with a constant input is known to be a periodic rectangular wave. From this, a generic output can be described as a rectangular-wave with period T and duty-cycle D, defined in (3.2) and which can be seen in Figure 3.4. This describes every periodic rectangular wave possible, however, only a smaller set of waves (completely defined by a duty-cycle D and a period T, the phase is not relevant) satisfy the system's equations. The first step shall be the determination of such set of points (D, T) that represent valid solutions for the system.

The stability of each solution should be tested against the system equations. Since the system is unstable, and its output is periodic, it allows one to predict the system's actual output when running in closed-loop.

First of all, a periodic rectangular wave like the one that can be seen in Figure 3.4, can be mathematically defined as:

$$V_c(t) = \begin{cases} 1 & \text{for } t \in [0 + kT, DT + kT], k \in \mathbb{Z} \\ -1 & \text{for } t \in (DT + k, T + kT), k \in \mathbb{Z} \end{cases} \tag{3.2}$$

$$V_f(t) = V_c(t) * m(t) \tag{3.3}$$

$$V_e(t) = V_i(t) - V_f(t) \tag{3.4}$$

where $0 \leq D \leq 1$ is the duty-cycle of the rectangular wave $V_c(t)$, and $m(t)$ is the impulse response of the loop filter. $*$ is the convolution operator.

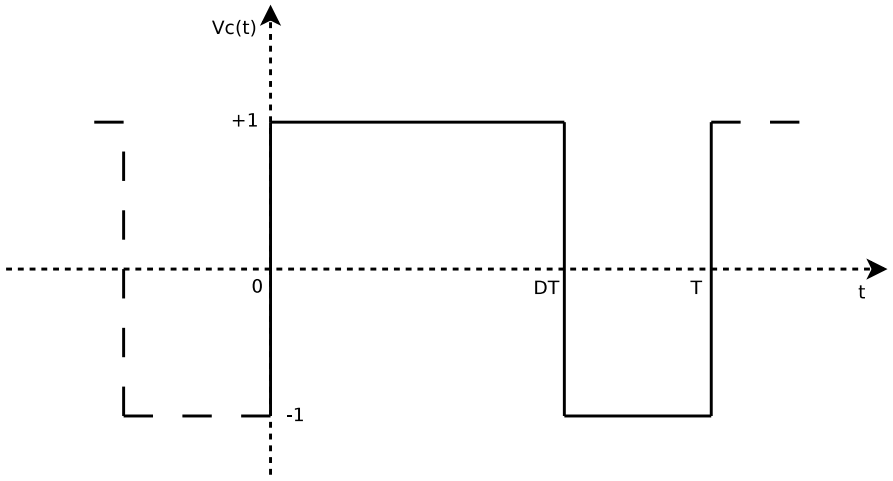


Figure 3.4: Rectangular wave which will be tested as solution of the output of the relay.

Calculating the Fourier transform of the rectangular wave $V_c(t)$, then calculating $V_f(t)$ in the frequency domain, and replacing in (3.4) we get, after transforming back to time-domain (please refer to Appendix C.1, for the detailed calculations):

$$V_c(t) = 2 \cdot D - 1 + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{2sin(\pi nD)}{\pi n} \cdot e^{-j\pi nD} \cdot e^{j2\pi \frac{n}{T}t} \tag{3.5}$$

$$V_f(t) = 2 \cdot D - 1 + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{2sin(\pi nD)}{\pi n} \cdot e^{-j\pi nD} \cdot M(j2\pi\frac{n}{T}) \cdot e^{j2\pi \frac{n}{T}t} \tag{3.6}$$

$$V_e(t) = V_i(t) - (2 \cdot D - 1) - \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{2sin(\pi nD)}{\pi n} \cdot e^{-j\pi nD} \cdot M(j2\pi\frac{n}{T}) \cdot e^{j2\pi \frac{n}{T}t} \tag{3.7}$$

3.3 Oscillation conditions

In order to check the proposed output for validity, the following must be true:

$$\begin{cases} V_e(t) >= 0 & , t \in [0 + kT, DT + kT] \, \forall \, k \in \mathbb{Z} \\ V_e(t) < 0 & , t \in (DT + k, T + kT) \, \forall \, k \in \mathbb{Z} \end{cases} \tag{3.8}$$

This condition can be simplified to these three conditions:

$$\begin{cases} V_e(t) = 0 & , \text{iif } t \in \{kT, DT + kT\}, k \in \mathbb{Z} \\ \frac{dV_e(t)}{dt} > 0 & , \forall \, t = kT, k \in \mathbb{Z} \\ \frac{dV_e(t)}{dt} < 0 & , \forall \, t = DT + kT, k \in \mathbb{Z} \end{cases} \tag{3.9}$$

From now on, *solution point* refers to a (D, ω) pair of values, where $\omega = \frac{2\pi}{T}$.

These equations are not trivial to be solved since there is no relationship known yet between output duty-cycle and the input $V_i(t)$.

However, it is possible to continue the analysis disregarding the value of $V_i(t)$, considering that $V_i(t)$ is a DC signal or a quasi-static signal compared to T. This restriction makes $V_i(0) = V_i(DT)$, which is an acceptable approximation if $V_i(t)$ does not change too much within an oscillation period.

As one can see, the first condition of (3.9) is also not trivial to solve, because it states that the **only** zeroes of $V_e(t)$ are the ones in $t \in \{kT, DT + kT\}, k \in \mathbb{Z}$. However, since any other zero-crossing within $(T, DT + kT])$ and/or $(kT + DT, kT)$ can only happen when the linear filter has such underdamped conjugated poles which allow overshots, it is reasonable to assume that, for open-loop systems without underdamped poles, $V_e(t)$ is zero only at $t \in \{kT, DT + kT\}$. This allows to replace the first condition of (3.9) by less general two conditions:

$$V_e(kT) = 0 \tag{3.10}$$

$$V_e(DT + kT) = 0 \tag{3.11}$$

Note that these conditions only refer to the points $t \in \{kT, DT + kT\}, k \in \mathbb{Z}$, while the first condition of (3.9) refers to all t!

Expanding $V_e(t)$ in (3.11) using (3.4),

$$V_i(DT + kT) - V_f(DT + kT) = 0 \tag{3.12}$$

$$V_i(kT) - V_f(kT) = 0 \tag{3.13}$$

So, it is valid to subtract both equations, namely subtract the first from the second, which yields

$$V_i(kT) - V_f(kT) - V_i(DT + kT) + V_f(DT + kT) = 0$$

Finally, recalling that $V_i(t)$ was considered to be quasi-static relatively to T, the $V_i(t)$ terms cancel each other, giving

$$V_f(DT + kT) - V_f(kT) = 0$$

And since $V_f(t)$ has the period T, this expression can be further simplified to

$$V_f(DT) - V_f(0) = 0 \tag{3.14}$$

From this, it is possible to reformulate the system conditions:

$$\begin{cases} V_f(kT) - V_f(DT + kT) = 0 & , \forall\, k \in \mathbb{Z} \\ V_e(t) \neq 0 & , t \in (kT, DT + kT) \bigcup (DT + kT, kT), \forall\, k \in \mathbb{Z} \\ \frac{dV_e(t)}{dt} > 0 & , \forall\, t = kT, k \in \mathbb{Z} \\ \frac{dV_e(t)}{dt} < 0 & , \forall\, t = DT + kT, k \in \mathbb{Z} \end{cases} \tag{3.15}$$

Which are equivalent, but are rewritten this way to focus the use of the first condition of (3.15) to retrieve a set of solutions which are then checked against overshooting phenomena (which constituted the second condition of (3.15)).

Expanding (3.14) using (3.3), we get:

$$\sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{2sin(\pi nD)}{\pi n} \cdot e^{-j\pi nD} \cdot M\left(j2\pi\frac{n}{T}\right) \cdot \left(e^{j2\pi nD} - 1\right) = 0 \tag{3.16}$$

Which does not depend on the value of $V_i(t)$. Further algebraic manipulation (just by transforming the two-sided summation into a single sided one), and defining $\omega = \frac{2\pi}{T}$ gives what will be defined as $\varphi(D, \omega)$:

$$\varphi(D, \omega) \equiv \sum_{n=1}^{+\infty} \frac{-8sin^2(\pi nD)}{\pi n} \cdot Imag\left[M\left(j\omega n\right)\right] = 0 \tag{3.17}$$

This constitutes the main condition for oscillation to take place for an output wave at angular frequency ω and duty-cycle D.

Note that if only one sine is considered, by neglecting all terms but $n = 1$, and making $D = \frac{1}{2}$ this equation turns to the Barkhausen phase-criterion [27]. For rough estimates, the idle frequency can be calculated this way, which is approximately at the $-\pi$ phase for the $M(j\omega)$.

3.4 Hysteresis

3.4.1 Hysteresis - First approach

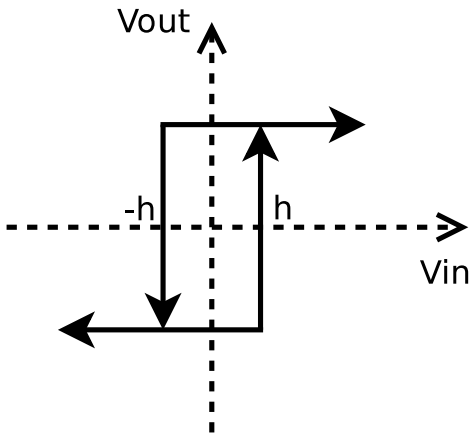


Figure 3.5: Input/Output characteristic for a hysteretic relay

From the definition of hysteresis (Figure 3.5), considering that the relay toggles when the input is $+h$ or $-h$, with positive or negative derivative, respectively, and that

$$V_e(0) = V_i(0) - V_f(0) = +h \tag{3.18}$$
$$V_e(DT) = V_i(DT) - V_f(DT) = -h \tag{3.19}$$

Recalling the quasi-static property of $V_i(t)$ and the fact that the waves are periodic on T, then (3.14) turns into

$$V_f(DT) - V_f(0) = 2h \quad \forall\, k \in \mathbb{Z} \tag{3.20}$$

This gives us a wider oscillation condition:

$$\varphi(D,\omega) \equiv \sum_{n=1}^{+\infty} \frac{-8sin^2(\pi nD)}{\pi n} \cdot Imag\left[M\left(j\omega n\right)\right] = 2h \tag{3.21}$$

Picking for example, as the linear filter, a first-order integrator s^{-1}, and substituting in (3.21) $M(j\omega n)$ for $-j(\omega n)^{-1}$, since every term of the summation is positive one can see that $\varphi\left(\frac{1}{2},\omega\right)$ goes asymptotically to zero from the upper positive plane, as can be seen in Figure 3.6.

This means that it does not oscillate without hysteresis, but let hysteresis exist and oscillation will occur, since it will cross the $\varphi\left(\frac{1}{2},\omega\right) = 2h$ line.

3.4.2 Self-oscillation in systems with sub-third-order feedback path

Picking a second-order low-pass filter, $M(j\omega) \equiv \frac{1}{(j\omega+1)^2}$, one can see that $\varphi\left(\frac{1}{2},\omega\right)$ goes asymptotically to zero from the positive plane (refer to Figure 3.7a). This means that the

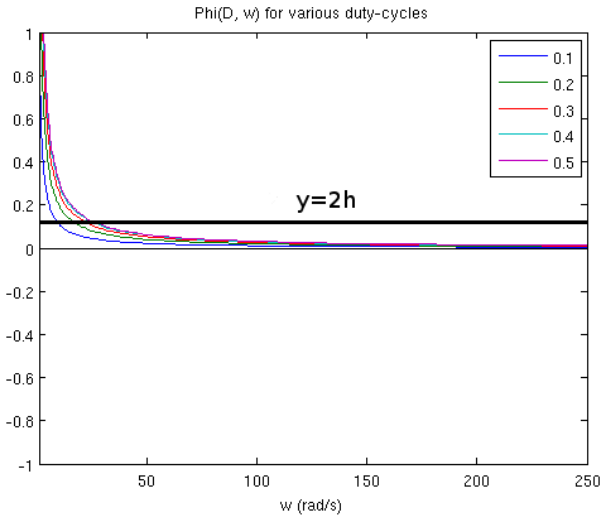
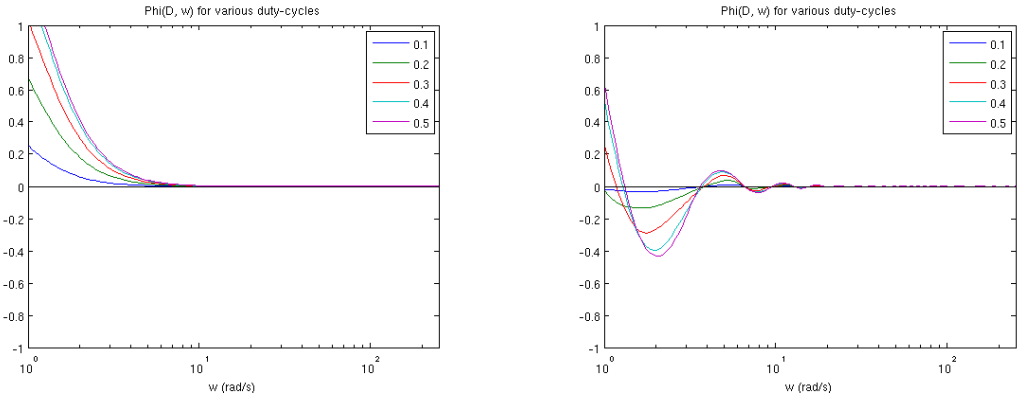


Figure 3.6: $\varphi(D, \omega)$ for various duty-cycles, for a first-order integrator.

system is unable to oscillate, unless $h > 0$. This is one possible way to make the system enter a stable oscillation[1].

On the other hand, if a propagation delay is inserted in the feedback path, $\varphi\left(\frac{1}{2}, \omega\right)$ exhibits a sinusoidal component around zero, a direct consequence of the fact that the imaginary part of $M(j\omega)$ was modulated by a sine. Refer to Figure 3.7b. This aspect will be further developed in sub-section 3.4.3.



(a) Without propagation delay

(b) With propagation delay

Figure 3.7: $\varphi(D, \omega)$ for various duty-cycles, for a second-order low-pass filter with and without a propagation delay

3.4.3 "Negative" hysteresis

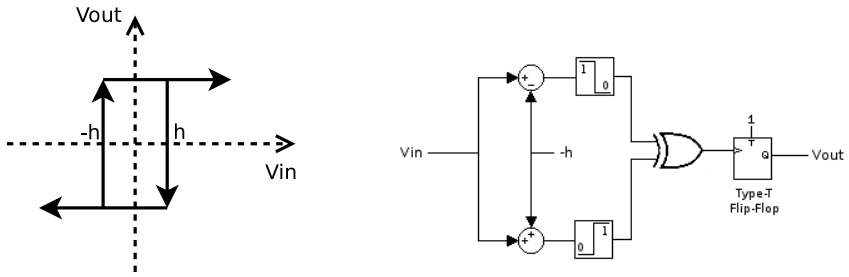
As can be seen in Figure 3.7b, the function with a propagation delay crosses the zero even without hysteresis (the same happens e.g. for a third-order low-pass filter). Besides the fact

[1] A stable oscillation is considered to be an oscillation with stable frequency and duty-cycle.

that positive hysteresis can be added to the comparator in order to reduce the oscillation frequency, it is also possible to use negative hysteresis (i.e. a negative h) in order to make $\varphi(\frac{1}{2}, \omega)$ cross the zero at higher frequencies.

However negative hysteresis is not simply obtained changing the sign of the positive feedback because that is transforming a positive feedback in negative feedback.

First of all, negative hysteresis is defined the same way as positive hysteresis, except for the derivatives, which are the symmetric. The positive edge of the output occurs when the derivative of the input signal is positive, and the negative edge of the output occurs when the derivative of the input signal is negative. The characteristic and a possible implementation can be seen in Figures 3.8a and 3.8b.



(a) Vin/Vout characteristic (b) Possible Implementation

Figure 3.8: Negative hysteresis relay implementation.

For $t = 0$, if the input resides between h and $-h$ the output is undefined, which also happens in positive hysteresis. It is mandatory that for $t = 0$ the output is not within these bounds.

In Figure 3.9 a solution to a system with negative hysteresis can be seen.

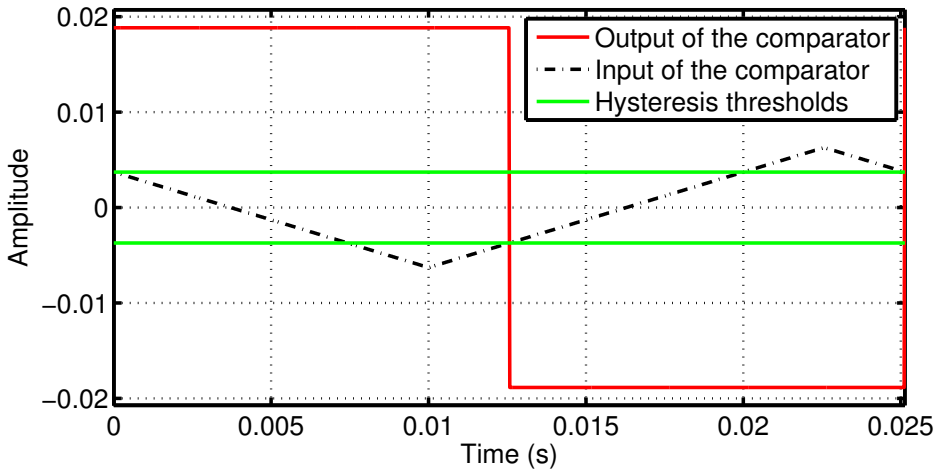


Figure 3.9: Solution of a closed-loop system with negative hysteresis.

Likewise positive hysteresis, if the input signal of the system $V_i(t)$ makes the error signal $V_e(t)$ unable to cross the $-h$ or h thresholds, the system will stop to oscillate indefinitely.

But, if the system is already oscillating, that means that $V_i(t)$ is not quasi-static relatively to the oscillation period T.

A big difference is that the initial output of the output filter should be outside that interval, otherwise, the system is stable and does not enter into oscillation because the switching thresholds are not reached.

Calculating the Sinusoidal-Input Describing Function gives:

$$n_p(A) = \frac{4}{\pi A}\sqrt{1-\left(\frac{h}{A}\right)^2} \tag{3.22}$$

$$n_q(A) = \frac{4h}{\pi A^2} \tag{3.23}$$

Which means, from the positive sign of $n_q(A)$, that this kind of hysteresis provokes a "phase-lead" on the sine wave, further supporting the fact that the idle frequency increases.

To check the prediction that negative hysteresis increases the oscillating frequency, simulations were carried out for the same system, but changing the amount hysteresis of the relay: 0.1, -0.1 and 0.

The linear filter $M(s)$ employed, was a second-order low-pass filter, with cut-off frequency $w_c = 1(rad/s)$ in series with a propagation delay $\tau = 1(s)$.

The simulation results can be seen in Figure 3.10. Theoretical data is overlapped, and shows to be an accurate prediction.

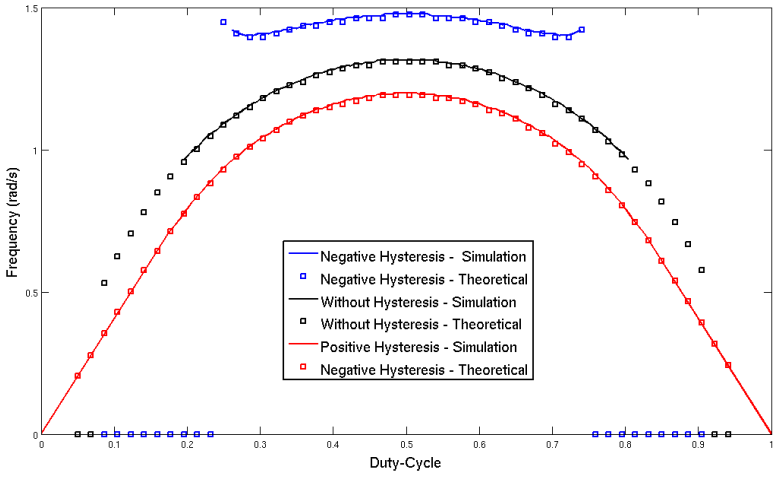


Figure 3.10: Comparison between the same system, with both types of hysteresis and without any hysteresis. Theoretical data is overlapped, and shows to be an accurate prediction.

3.4.4 Hysteresis extended point of view

In order to extend the positive hysteresis concept, the hysteretic SOPA of Figure 3.2 will be evolved into a more general form as in Figure 3.11.

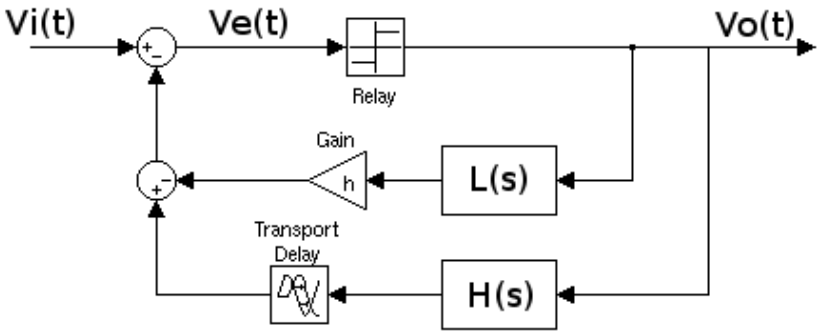


Figure 3.11: System architecture of a hysteretic system. The propagation-delay is explicit, but can be zero and/or included in the linear filter $H(s)$.

This gives a clearer view that positive hysteresis may be included in the filter itself.

Moreover, this point of view explicits that this model is able to predict the system behaviour even when the hysteresis has some dynamic, represented as $L(s)$.

However this approach reveals a pitfall of the system, as shall be described in the following section.

3.5 Convergence issues

In the previous sub-section, the system was generalized so that hysteresis could be made part of the filter, and not of the comparator itself.

That rises the question: If the positive hysteresis may be included in the filter, why is it explicit in (3.21) ?

Picking the simplest example where this can be employed, for a second-order filter without propagation delay and with hysteresis h, the following must be true, from (3.17) and (3.15):

$$\sum_{n=1}^{+\infty} \frac{-8sin^2(\pi nD)}{\pi n} \cdot Imag\left[M\left(j\omega n\right) - h\right] = \sum_{n=1}^{+\infty} \frac{-8sin^2(\pi nD)}{\pi n} \cdot Imag\left[M\left(j\omega n\right)\right] - 2h$$

Which is clearly false, because the $Imag(\bullet)$ operator crops the hysteresis out.

This is a consequence of the problem formulation. The first step was based on the representation in the Fourier domain of a rectangular wave, which does not fulfil the Dirichlet boundary conditions [28].

The particular problem comes from the fact that the inverse of a Fourier-transform, at points with no defined derivative, will give the mean-value between the left-side and right-side neighbours of the discontinuity. This means that this problem does not come from the fact that the series is being truncated to be computationally feasible. The $2h$ in (3.21) is the difference between the comparator input at $t = 0$ and $t = DT$, which are precisely the points where the discontinuity exist, which will lead to erroneous results.

Modelling hysteresis in the linear filer is only valid if $L(s)$ (as defined in Figure 3.11) is low-pass such that the output of such filter has no discontinuities (at least at $t = 0$ and $t = DT$).

3.6 Extending theory to State-Space

In order to predict the trajectories of the system, the same idea will be employed in a state-space representation. If relevant state variables are used (for example filter currents and/or voltages), this representation easily predicts those variables over time. This could be used to avoid stressing components.

Considering a linear filter (without propagation delay), one can define the following state equations:

$$\vec{x}(t) = \vec{A}\vec{x}(t) + \vec{B}\vec{r}(t) \tag{3.24}$$

$$\vec{y}(t) = \vec{C}\vec{x}(t) + \vec{E}\vec{r}(t) \tag{3.25}$$

Where $\vec{x}(t)$ stands for the state variable, $\vec{r}(t)$ for the system input and $\vec{y}(t)$ for the system output.

In the complete system, since the comparator's input and output signals are the linear filter's output and input, respectively, the system is defined as a Single-Input Single-Output System (SISO), which implies that $\vec{r}(t)$ and $\vec{y}(t)$ are scalars. Moreover, since the only forward path is through the comparator, it is also true that $\vec{E} = 0$. It is also important to note that using a state-space definition, the propagation delay must be explicit. That way the true output of the system, $V_f(t)$ is a delayed version of $y(t)$, thus, the input fed in the comparator is not $V_e(t) = V_i(t) - y(t)$ but $V_e(t) = V_i(t) - y(t-\tau)$ where τ is the total propagation delay along the feedback path from the comparator's input to it's input.

Solving the state equations using the Laplace-transform, we get:

$$\vec{X}(s) = (s\vec{I} - \vec{A})^{-1}\vec{B}R(s) \tag{3.26}$$

$$\tag{3.27}$$

As it is clear, $(s\vec{I} - \vec{A})$ must be a non-singular matrix.

The state trajectory over time can then be calculated from the integral, recalling that $r(t) \equiv V_c(t)$ and using the transformation $s \equiv 2\pi fj$:

$$\vec{x}(t) = \int_{-\infty}^{+\infty} (2\pi fj\vec{I} - \vec{A})^{-1}\vec{B}R(2\pi fj)e^{j2\pi\ ft}, \delta f \tag{3.28}$$

Replacing $R(2\pi fj)$ by the Fourier-transform of $V_c(t)$, the final solution is obtained:

$$\vec{x}(t) = (-\vec{A}^{-1}\vec{B})(2D-1) + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{2sin(\pi nD)}{\pi n} \cdot e^{-j\pi nD}e^{j2\pi\ t\frac{n}{T}} \cdot (2\pi fj\vec{I} - \vec{A})^{-1}\vec{B} \tag{3.29}$$

$$V_f(t) = \vec{C}\vec{x}(t-\tau) \tag{3.30}$$

To test the trajectories obtained from this expression, a simulation was performed, and the theoretical trajectory was plotted over the simulation data. The match is perfect, as can be seen in Figure 3.12. For an arbitrary initial condition, the system converges towards the solution, as in Figure 3.13.

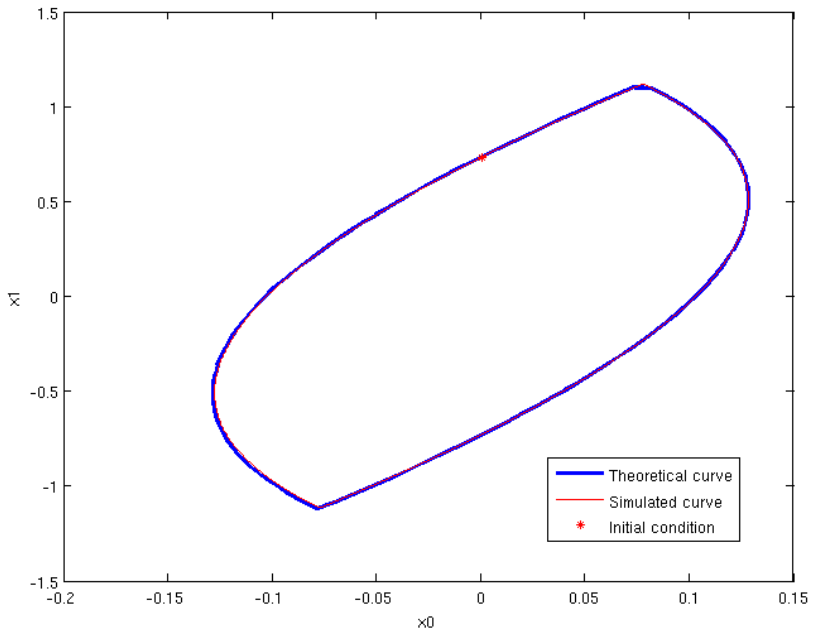


Figure 3.12: State-Space trajectory of a system with a second-order low-pass filter, showing simulated trajectory, theoretical trajectory, and the initial condition of the simulation, taken from the theoretical curve.

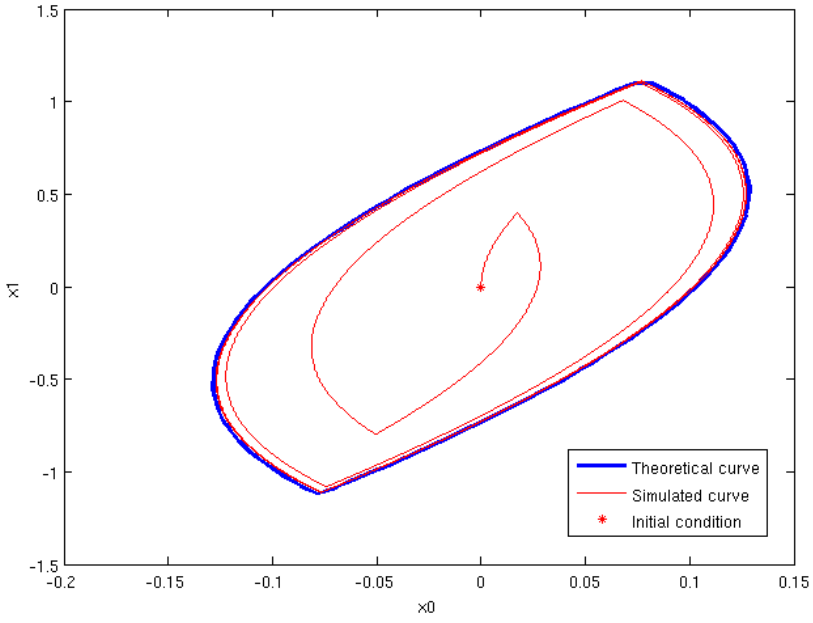


Figure 3.13: Trajectory of a system with a second-order low-pass filter, showing simulated trajectory, theoretical trajectory, and an arbitrary initial condition.

3.7 Validity of the oscillatory solutions

When the linear filter includes a propagation-delay, the equation $\varphi(D, \omega) = 0$ exhibits infinite solutions. It happens because the imaginary part of the frequency response of the linear filter is modulated by a sinusoidal component. That is clearly seen in the Figure 3.7b.

This leads to uncertainty about the natural oscillation frequency, so it is mandatory to identify if those solutions are possible.

First of all, a physical constraint about the minimum pulse-width will be presented, which will allow to proof that those solutions are physically impossible.

Considering a relay and a linear (and causal) filter with a propagation delay, if the loop is closed at $t = 0$ so that the feedback is negative, and considering that for $t < 0$ the relay was in steady state (either 1 or -1), then, if no external input exists, the input of the relay is just the output of the filter. So, any change in the output of the relay, can only affect the input of it, at least, after the propagation delay.

This means that the minimum pulse width is, at most, the propagation delay (at most, because the dynamics of the filter may require the pulse to last longer, in order allow a sufficient change in the output, to toggle the output of the relay). That can be formally expressed making the positive pulse width $T \cdot D$ and the negative pulse width $T \cdot (1 - D)$ higher than τ:

$$\frac{2\pi}{\omega} D > \tau \tag{3.31}$$

$$\frac{2\pi}{\omega} (1 - D) > \tau \tag{3.32}$$

And for the best case, where no modulation is present so that both pulses have the maximum possible width for a given frequency, which occurs for $D = \frac{1}{2}$, the expression can be further simplified into

$$\frac{\pi}{\omega} > \tau \tag{3.33}$$

This gives us a way to check if a solution is impossible. Now, an estimation of the set of solutions will be made, in order to check if they are invalid.

Recall the system in Figure 3.2, which is replicated in page 47 for convenience.

Consider that the filter $M(s) \Rightarrow M(j\omega)$ is composed by a propagation delay τ and a regular filter in series, so that $M(j\omega) = \left[e^{-j\omega\tau} \cdot H(j\omega)\right]$ where $H(j\omega)$ has no propagation delay. In order to obtain a good approximation in the following analysis, $H(j\omega)$ should be quasi-static in terms of frequency relatively to $e^{(-\tau\omega)}$. For example, by exhibiting an almost constant phase over frequency near the frequencies where $\varphi(D, \omega)$ crosses zero. That happens for a n-th order low-pass filter, where the phase is roughly $-\frac{n\pi}{2}$ for frequencies higher that the cut-off frequency.

For the sake of simplicity, a first-order low-pass filter will be chosen, $H(j\omega) = (1 + j\omega T_p)^{-1}$, where T_p is the time constant. This makes $M(j\omega) = \frac{1}{(1+j\omega T_p)} e^{-j\omega\tau}$.

Recalling (3.21), one can see that one way of cancelling the sum, is by making the imaginary part of $M(j\omega n)$ zero. Expanding $e^{-j\omega n\tau}$ into $cos(\omega n\tau) - jsin(\omega n\tau)$, and splitting the real and imaginary parts of $H(j\omega n) = \frac{1}{1+\omega^2 T_p^2 n^2} - j\frac{\omega T_p n}{1+\omega^2 T_p^2 n^2}$, $M(j\omega n)$ can be expanded into

$$M(j\omega n) = \frac{cos(\tau\omega n) - sin(\tau\omega n)\omega T_p n}{1+\omega^2 T_p^2 n^2} - j\left(\frac{cos(\tau\omega n)\omega T_p n + sin(\tau\omega n)}{1+\omega^2 T_p^2 n^2}\right) \tag{3.34}$$

In order to cancel the imaginary part, $sin(\tau\omega n) + cos(\tau\omega n)\omega T_p n = 0$, which, considering that $\omega T_p >> 1$, can be simplified, because near the zero of the cosine, although the sine has unitary amplitude, the derivative of the cosine is much higher. This makes the zero of the imaginary part be next to the zero of the cosine part. And is much closer as ωT_p increases.

Moreover, since the sine is positive when the derivative of cosine is negative (this can be seen just by calculating the derivative of cos(x)), the frequency at which the zero occurs is slightly higher than the zero of the cosine. So, if the frequencies at which the cosine is zero are too high to be physically possible according to the condition (3.33), then the exact zero frequency would be too.

As is clear, the zeroes of the cosine can be given by:

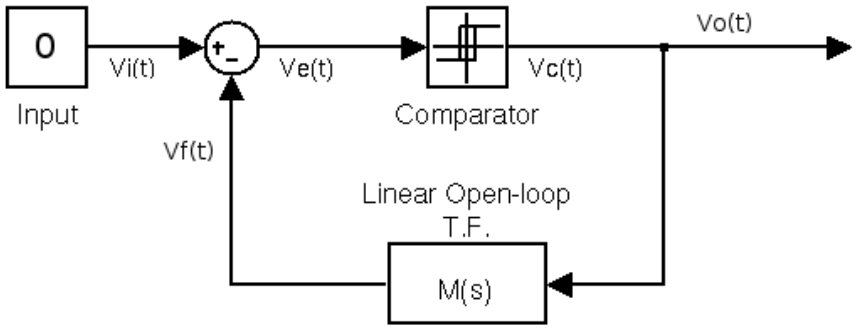
$$\tau\omega n = \frac{\pi}{2} + k\pi \quad , k = 0, 1, ... \tag{3.35}$$

Remember that n is the index of the summation at (3.21). This means that higher harmonics of $cos(\tau\omega n)$ have its zeroes at lower frequencies[2]. Some algebraic manipulation over (3.35) yields:

$$\omega = \frac{(2k+1)\pi}{2\tau n} \tag{3.36}$$

However, the zeroes of $n > 1$ harmonics are not zeroes of the summation, because the fundamental component is much larger than the harmonics (refer to (3.34), and notice that

[2]Please, be aware that the independent variable is ω, and that this is being done in frequency domain.



System architecture.

the harmonics have a $\frac{1}{n}$ factor). This way, the zeros of the imaginary part of $M(j\omega)$ are close to the zeroes of $cos(\tau\omega)$, given by (3.36) when n = 1, as can be seen in Figure 3.14.

$$\omega = \frac{(2k+1)\pi}{2\tau} \tag{3.37}$$

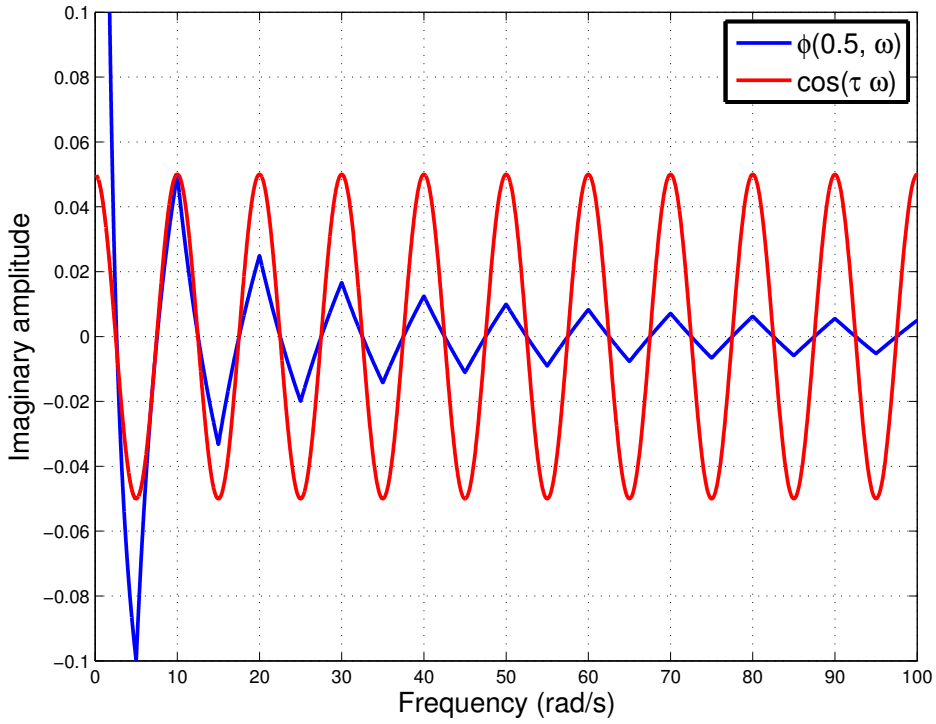


Figure 3.14: The zeros of both functions $\varphi(D,\omega)$ and $cos(\tau\omega)$ are very close. The scale has been changed to enhance visibility

From (3.33), and replacing ω by the solutions (3.37), gives:

$$\frac{\tau}{\frac{1}{2}+k} > \tau \quad , k = 0, 1, ... \tag{3.38}$$

Which is only valid for $k = 0$.

This is valid for filters where the frequency response above the higher-frequency singularity is imaginary, as is the case of odd-numbered low-pass filters. For a second order filter for which the frequency response at $\omega = +\infty$ is real, the imaginary part of $M(j\omega)$ is modulated not by a cosine, but by a sine. Remaking all the calculations, this yields:

$$\frac{\tau}{k} > \tau \quad , k = 0, 1, ... \tag{3.39}$$

Which, for $k = 0$, is an indetermination, however the limit $\lim_{\sigma \to k} \frac{\tau}{\sigma} \quad , k = 0$ is true. And this is the only solution which satisfies (3.33).

3.8 Complete set of conditions for oscillation

In order to summarize all the oscillation conditions, refer to the following list:

- The following must be true for a given D and ω

$$\sum_{n=1}^{+\infty} \frac{-8sin^2(\pi nD)}{\pi n} \cdot Imag\left[M\left(j\omega n\right)\right] = 2h$$

- The derivative of $V_e(t)$ at $t = 0$ must be positive and negative at $t = DT$ (this can easily be calculated from the derivative of (3.7)

- Including hysteresis in the feedback path, instead of expliciting it in the previous equation is only valid when hysteresis has low-pass dynamic, which ensures continuity at $t = 0$ and $t = DT$.

- $$\frac{2\pi}{\omega} D > \tau \tag{3.40}$$
$$\frac{2\pi}{\omega} (1 - D) > \tau \tag{3.41}$$

- The filter should not have underdamped conjugate poles

3.9 Modulating Signals

3.9.1 Quasi-static signals

Since this system is supposed to be an amplifier, which is supposed to be linear, the modulation effect of the input signal on the output is a very important aspect.

Since the starting point of the analysis was based on a quasi-static input signal, the output should also be seen as a quasi-static signal, although it has high-frequency components (considered as dithering signal from the input point-of-view).

This means that the output V_o will be considered to be the mean-value of the output, $(2D-1)$ for a relay with $-1, 1$ as possible output levels, as has been considered from the beginning.

Considering that (D_0, ω_0) is a valid solution according to section 3.8, then, from (3.19), and since $V_e(0) = 0$ because the relay toggles at that instant,

$$V_i(0) = V_f(0) - h$$

So $Vi(0)$ can be calculated from $V_f(0)$. Defining $Vo \equiv (2D-1)$, and defining $t = 0$ for (3.6), we get

$$V_i(V_o) = V_o - h + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \frac{2sin(\pi n \frac{V_o+1}{2})}{\pi n} \cdot e^{-j\pi n \frac{V_o+1}{2}} \cdot M(j\omega n) \tag{3.42}$$

In this case, what is obtained is the input as a function of the output, which is an unusual way to represent the relationship between the input and the output. It's not easy to algebraically invert this expression, however, it can be directly used by pre-distorters.

The derivative is also easy to calculate:

$$\frac{dV_i}{dV_o}(V_o) = 1 + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \left(cos(\pi n \frac{V_o+1}{2}) - j \cdot sin(\pi n \frac{V_o+1}{2}) \right) e^{-j\pi n \frac{V_o+1}{2}} M(j\omega n) \tag{3.43}$$

Although linearity is obtained if the summation is zero, that condition is too strict, since it also forces the gain to be unitary. A more objective condition can be obtained by getting the linear gain at $V_o = 0$

$$\frac{dV_i}{dV_o}(0) = 1 + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \left(cos(\pi n \frac{1}{2}) - j \cdot sin(\pi n \frac{1}{2}) \right) e^{-j\pi n \frac{1}{2}} M(j\omega n) \tag{3.44}$$

And making the $Vi(Vo)$ keep the same gain. The following expression can be used to analytically calculate the deviation from linearity of the system.

$$V_i(V_o) - \frac{dV_i(0)}{dV_o} V_o \tag{3.45}$$

For most of the filters tested[3], when the oscillation frequency is near the cut-off frequency, the $V_i(V_o)$ characteristic assembles a sine from $-\frac{\pi}{2}$ to $\frac{\pi}{2}$, so an interpolation can easily be made, simply by matching the derivative at $V_o = 0$:

$$V_i(V_o) \approx sin(\frac{dV_i}{dV_o}(0) \cdot V_o) \tag{3.46}$$

Please, note that this is just a suggestion for interpolating the output. The interpolation should always be checked against $V_i(V_o)$ calculated from 3.42.

The result of the interpolation for a Second-order low-pass filter with propagation delay, can be seen in Figure 3.15.

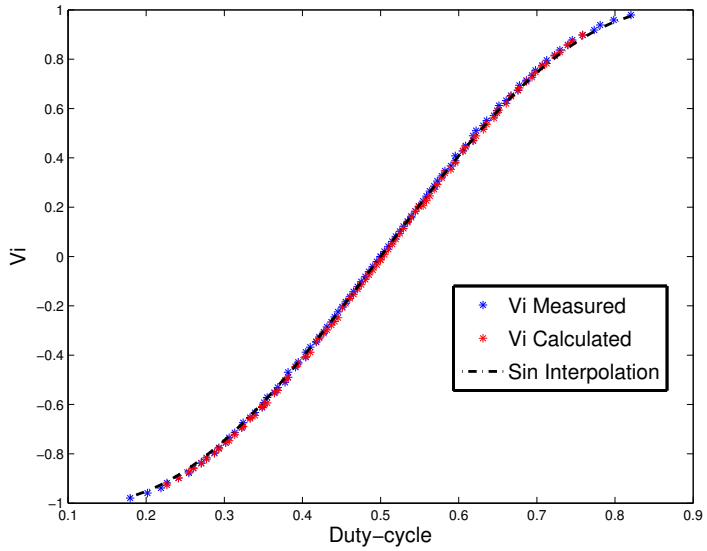
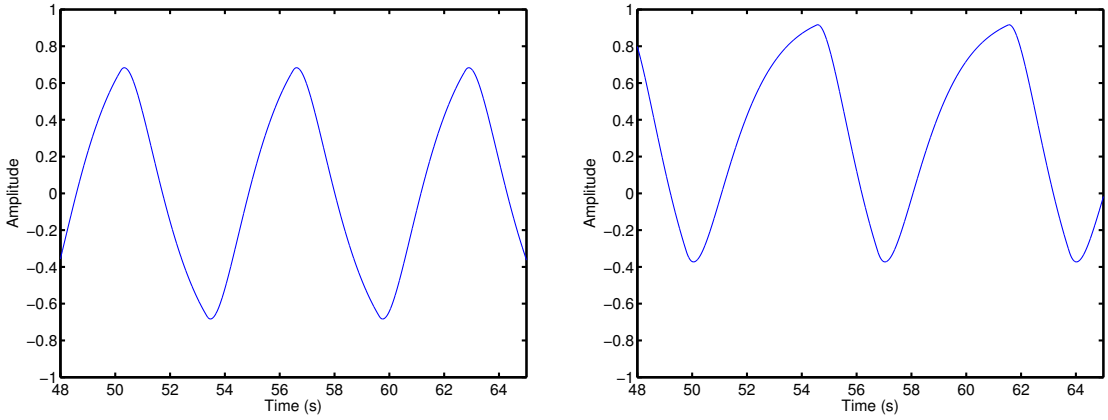


Figure 3.15: $V_i(V_o)$ characteristic of a phase-shift second-order low-pass system, and the proposed sinusoidal interpolation.

Note that the characteristic assembles that of a sinusoidal-dithering system not because the harmonics are so much attenuated making the dithering signal appear sinusoidal, but because the resulting modulation assembles it. To show that the dithering for each input signal is not sinusoidal, the dithering waveform of the second-order filter is depicted in Figure 3.16 for two duty-cycles.

[3]The tested filters are first, second and third-order filters, with such a propagation delay, that the system oscillates at the cut-off frequency. When they oscillate at higher frequencies, the sinusoidal interpolation is no longer acceptable, since the characteristic assembles one straight line



(a) For $V_i = 0$ (b) For $V_i = 0.8$

Figure 3.16: Dithering waves for two distinct duty-cycles, to depict the fact that although the characteristic of the shown second-order system assembles that of a sinusoidal-dithering system, the dithering changes with duty-cycle, and is never a sine wave.

Chapter 4

Low-pass SOPA Design

4.1 Design Considerations

As can be seen from (3.43), (3.44) and (3.45), the linearity can be obtained by lowering the $M(j\omega n)$ terms, which, for a low-pass output filter, means making ω large compared with the cut-off frequency. This has two advantages: the linearity increases, while the output ripple decreases.

As a guideline, Table 4.1 shows the stationary figures-of-merit. Keeping the same propagation-delay $\tau = 0.017$s over all configurations, simulations were performed for three low-pass filters, having a cut-off frequency $w_c = 1$ (rad/s). The self-oscillation frequency for 50% and 10% duty-cycles, the filter attenuation at those frequencies (which give a clue about the amplitude of the ripple) and the quasi-static linearity, represented by the Normalized Mean of the Squared Error (NMSE) of the $V_i(V_o)$ error from the first-order Taylor series at $V_o(V_i) =$ 0V are all shown in the table.

Low-pass filter	$\omega_{50\%}$	$\omega_{10\%}$	Filter atten. at $\omega_{50\%}$	Filter atten. at $\omega_{10\%}$	NMSE of $V_i(V_o)$ curve
First-order	94.55	33.42	39.0dB	30.5dB	1×10^{-3}
Second-order	10.00	6.10	40.0dB	31.6dB	1.5×10^{-3}
Third-order	1.67	1.25	17.4dB	12.3dB	6×10^{-2}

Table 4.1: Oscillation frequency for 50% and 10% Duty-cycle, ripple attenuation at those frequencies, and NMSE of the $V_i(V_o)$ characteristic

In the referred table, it is clear that a larger phase margin in each filter's phase plot increases the frequency. First and second order filters, although having distinct oscillating frequency, have slightly the same attenuation at the fundamental frequency of the carrier. The third-order filter is clearly a worse option, because is much less linear, and the output ripple will be much larger.

Considering now only the first and second-order filters, the first is slightly more linear, which would suggest to be the best option, however, there is a big drawback that makes the second-order filter the best option: since the frequency in the first-order is approximately ten times higher than the second-order, so will be the power-losses from the charge/discharge cycles (from $\frac{1}{2}CfV^2$). From this, a second-order filter is more efficient.

4.2 Closed-loop gain

In order to predict the frequency response of the system, the closed loop linear gain can be calculated, using (3.44), to derive the $V_o(V_i)$ characteristic (namely the first-order derivative at the origin). Both bode-plots for a first and second order system loops are shown in Figure 4.1.

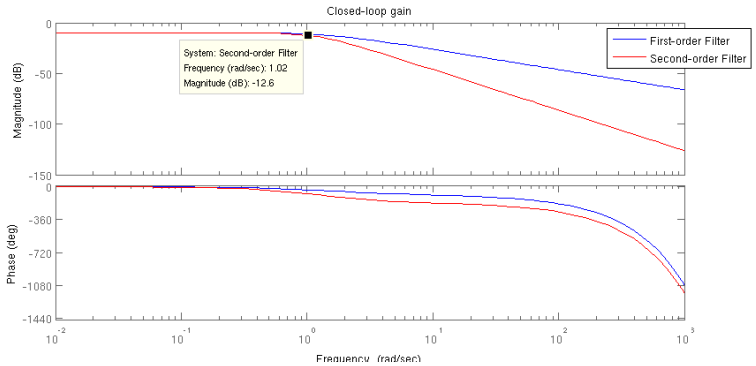


Figure 4.1: Linear closed-loop bode-plots for first and second-order filters.

4.3 Choosing the oscillation frequency

Since the best option is to keep the dithering far from the cut-off frequency of the filter, it is good to have the smallest propagation delay possible. That leads us to either technological limits (comparator plus power-stage) or to size limits (due to wave propagation delays). So, it is assumed that the propagation delay is already known. It will be assumed to be $\tau = 1{\times}10^{-2}$s.

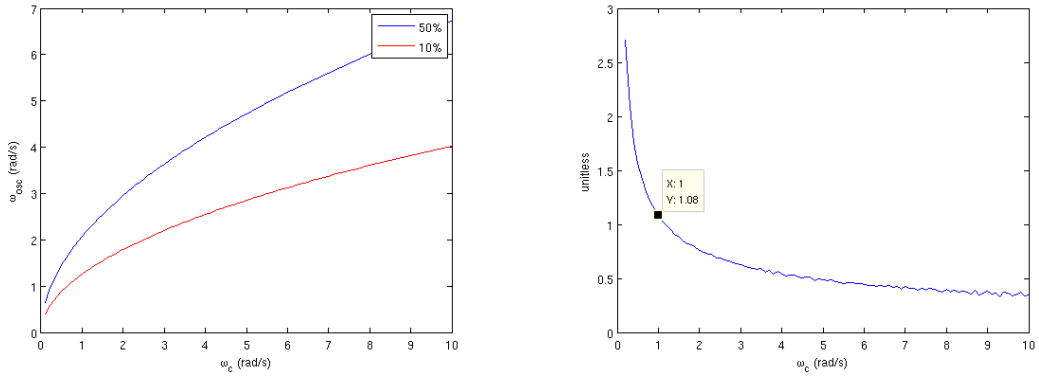
A second order filter will be chosen from Table 4.1. In order to select the cut-off frequency ω_c, two approaches can be taken. The most natural is to select the cut-off frequency equal to the desired bandwidth of the amplifier. However, when the signal bandwidth is unknown, it may be preferable to maximize the bandwidth of the amplifier.

In order to do that, the first step is to plot the $\omega_{50\%}(\omega_c)$ and $\omega_{10\%}(\omega_c)$ functions. It is preferable to choose a high-derivative point (greater than or equal to 1), because it means that for a given increase in cut-off frequency, the oscillation frequency will at least increase proportionally, attenuating more the carrier. This makes the highest frequency where the derivative is unitary the highest advantageous frequency. This is shown in Figure 4.2, although, for this filter, it is exactly the same. It may not be for more sophisticated filters.

Choosing $\omega_{50\%} = 1$ (rad/s), the system is complete.

In order to design an hysteretic system, another step can be taken. Considering as a starting point a second order filter, and a propagation delay of $\tau = 1 \times 10^{-}4$s, we obtain the $\varphi(D, \omega)$ in Figure 4.3, for which the natural frequency is 129(rad/s). With hysteresis, the frequency may be lowered to a more conservative one.

A great advantage of the $\varphi(D, \omega)$ function, is that it may then be used as a graphical aid on hysteretic systems design, since with this plot it is clearer how much hysteresis is needed to change the system idle frequency to a particular one.



(a) $\omega_{50\%}(\omega_c)$ and $\omega_{10\%}(\omega_c)$ (b) $\frac{d\omega_{50\%}(\omega_c)}{d\omega_c}$

Figure 4.2: The use of $\omega_{50\%}(\omega_c)$ in filter selection. This graphics plot the oscillating frequency dependency over the cut-off frequency of the filter, for a particular propagation-delay.

To fine tune the frequency, to 10 (rad/s) for example, it is just needed to get the $\varphi(D, \omega)$ at that point, which is equal to $2h$. The example of Figure 4.3 shows that for an idle frequency of $10(rad/s)$, $2h = 0.0049$ and for a 10% duty-cycle, the frequency will be 5 (rad/s).

This method can be fairly used to choose the oscillation frequency of the amplifier.

4.4 Closed loop gain

From [29], the DC gain of a comparator (with output limits +1 and -1) fed with the DC signal plus a triangular wave of amplitude $A_{triangle}$ is

$$K = \frac{1}{A_{Triangle}}$$

In order to obtain a more accurate result, the expression derived in Section 3.9 should be used.

4.5 Implementation aspects of switching architectures

There are three mainstream switching architectures. The circuit schematic of one of each can be seen in Figures 4.4, 4.5 and 4.6.

These architectures have different advantages and drawbacks. So, the selection of one over another should be careful, taking into account the desired characteristics of the amplifier. Here the main aspects of these configurations will be described. Usually only N-Channel Metal-Oxide-Silicon Field-Effect Transistor (MOSFET)s are employed because the higher mobility of the carriers allows a faster switching and lower R_{DSon}.

Using N-Channel MOSFETs in the high-side of the switching output, unlike the Complementary metal-oxide-semiconductor (CMOS) output stage, requires a floating circuit to control the gate in order to keep V_{GS} high even when the source of the transistor is at the potential of the highest power rail.

That will be shown in detail in Section 4.6, where a floating circuit will be employed.

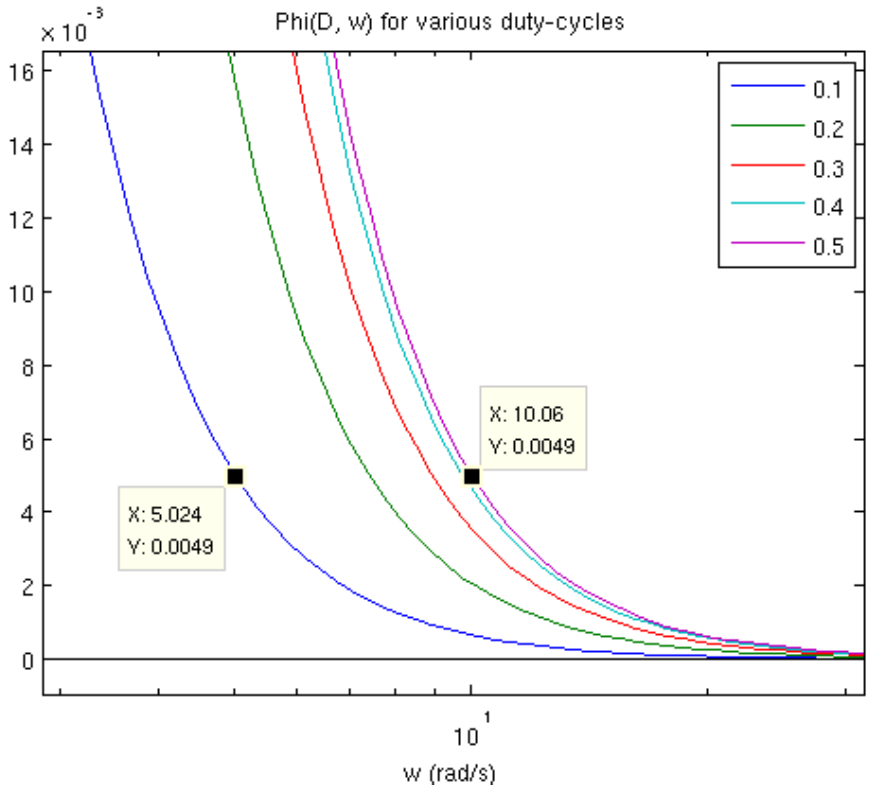


Figure 4.3: Linear closed-loop bode-plots for first and second-order filters.

4.5.1 Quarter-bridge

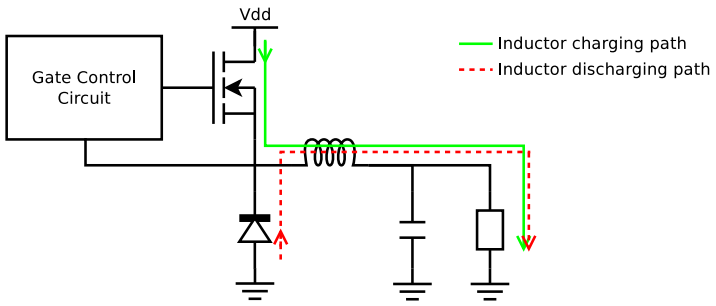


Figure 4.4: Switching stage I: Switching element plus flywheel diode.

This architecture is the simplest of all the three. The switching element simply switches on or off, charging the output inductor. To sustain the discharge current flow when the switch is turned off, the fly-wheel diode closes the discharging path. More sophisticated circuits exist (snubber networks, [30]) that surpass ringing, and minimize the power losses.

The main advantages of this architecture is its simplicity, since the control circuit only needs to control one switching element. This way, no timing constraints to ensure break-before-make are needed.

On the other hand, this output stage has no sinking capability, hence, the rising-time is the same as the falling time when the output has half the voltage rail, instead of ground.

4.5.2 Half-bridge

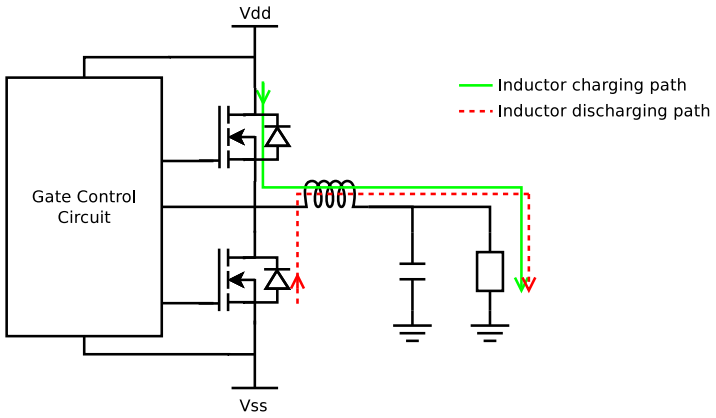


Figure 4.5: Switching stage II: Half-bridge configuration.

The half-bridge configuration is much more symmetrical than the quarter-bridge configuration. Unlike the quarter-bridge configuration, this output stage is able to sink current. However, care should be taken so that both transistors are not turned on at the same time. In order to toggle the output, the conducting transistor should be turned off first, so that the other can be turned on. This is usually called *break-before-make* and is crucial to keep the system efficient.

This requirement adds some complexity to the gate driver, and increases the overall delay from input to output.

The discharge path of the inductor can be closed by the body-diode of the MOSFETs. But, in order to achieve a small minimum pulse duration[1] and lower losses, a Schottky[2] diode can be placed in parallel with each of the transistors.

4.5.3 Full-Bridge (or bridge-tied-load)

The full-bridge configuration is the most complex configuration, and the one which requires more components. Moreover, the gate control is much more complex, as it controls 4 transistors.

This configuration has mainly two advantages. First, it is capable of delivering twice the output voltage than the half-bridge configuration, for the same power rail. This is done by inverting the load. The second advantage is about source pumping, and will be discussed in subsection 4.5.5.

[1]The body diode compromises the minimum pulse duration, because, although the low-side MOSFET can be turned off fast (extinguishing the conduction channel), the body-diode would continue to conduct while recovering from voltage inversion, shorting the supplies when the high-side MOSFET starts to conduct.

[2]Metal-semiconductor junctions do not exhibit reverse-recovery.

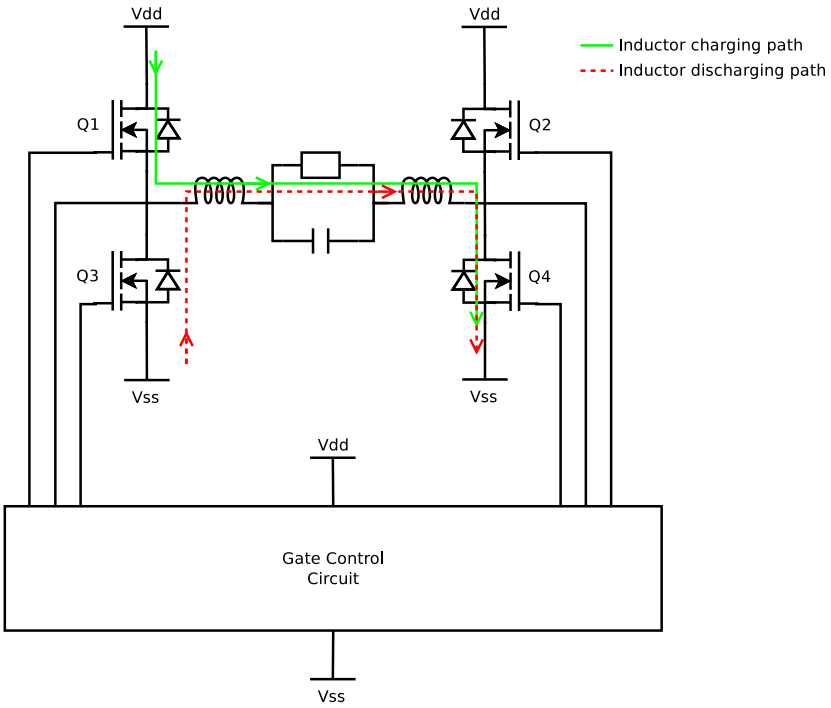


Figure 4.6: Switching stage III: Full-bridge configuration.

Another advantage is that its anti-symmetric nature reduces the symmetric non-linearities of the transistors [19] relatively to the half bridge (responsible for the even-numbered inter-modulation products)

4.5.4 Break-before-make

Although some switching stages are made from complementary transistors [31] (mainly in integrated circuits where it is difficult to design floating n-channel transistors), efficiency is greatly improved using a floating high-side N-channel MOSFET.

However, some timing constraints must apply. Namely, in a half-bridge configuration, the conducting transistor must be turned off – break – before turning the other on – make. This is crucial not only to keep efficiency high, but also to keep the devices intact.

4.5.5 Source pumping

Here one important phenomena which occurs for half-bridge and full-bridge configurations will be presented. This phenomena constitutes a severe efficiency issue.

First of all, in Figure 4.5, notice that the discharge path of the inductor forces the current to flow in the opposite direction of one of the power sources (in Figure 4.5 current flows in the opposite direction of Vss) forcing the power supply to absorb energy. This compromises efficiency, because if the power supplies are not able to store energy (for example by not having enough output capacitance) so that they can return it later, that energy must be dissipated. Nevertheless, a large output capacitance is not enough if the output stage is outputting

DC, since one[3] of the sources will absorb DC current which implies that the other source is delivering more power than what is needed by the load, thus reducing overall efficiency.

In Figure 4.7 the absorbed power for each of the power supplies is plotted for a half-bridge configuration, and 75% duty-cycle. Since with 75% duty-cycle the inductor discharges 25% of the time, the negative power supply will absorb energy 25% of the time.

However, bridge-tied-load configuration allows to cancel this effect. When the inductor is discharging, the current must flow through the branch in Figure 4.6, turning off Q1 and Q2 and turning on Q3 and Q4 (turning on Q1 and Q2 and turning off Q3 and Q4 is equivalent).

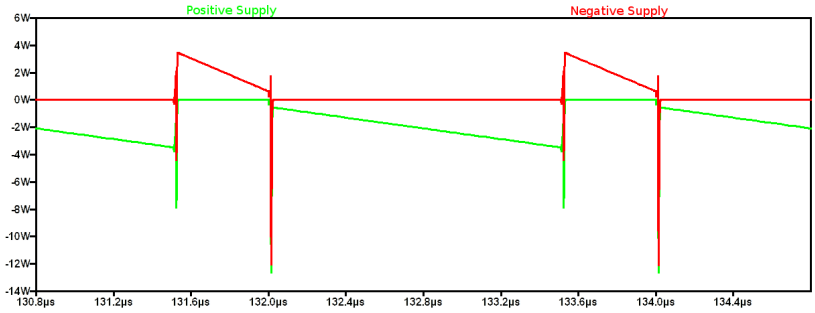


Figure 4.7: Power absorbed by both power supplies, in a half-bridge configuration with 75% duty-cycle. A regular supply would have a negative mean value.

4.5.6 Summary

After explaining all these aspects, Table 4.2 summarises the main characteristics of these three architectures.

	Component Count	Gate circuit	Efficiency	Source Pumping
Quarter-Bridge	Low	Simple	High	No
Half-Bridge	Medium	Medium[a]	Medium	Yes
Bridge-tied-load	High	Complex	Low	Yes[b]

[a] Degraded by break-before-make constraints.
[b] However, can be used the workaround explained in subsection 4.5.5.

Table 4.2: Qualitative table about different switched output stages

4.6 Prototype Design

In this chapter, a self-oscillating prototype will be designed. Main decisions will be explained, along with technical details.

[3]If the DC output is positive, Vss will have to absorb DC power, otherwise, if the DC output is negative, is Vdd the source which will absorb energy.

4.6.1 Load specifications

First of all, the main specifications should be selected. Since the amplifier is supposed to be a voltage amplifier, the feedback will be in the form of voltage. Moreover, the output of an envelope amplifier is unipolar, hence, the designed amplifier will only output positive voltages. The gain and bandwidth will be chosen according to self-oscillating frequency (which will depend on the overall propagation delay from the input of the comparator, to the output of the switching stage).

Since the output is always positive, the quarter-bridge configuration will be chosen in order to minimize propagation delay. Indeed, the gate driver does not need any artificial delay to ensure the necessary break-brefore-make when controlling two series transistors.

Considering the 10W Class-E amplifier of [16] as the load, the $I(V)$ characteristic is important to define the current/voltage requirements of the amplifier.

In Figure 4.8 the $V(I)$ characteristic is plotted, including the linear regression using minimum-squared-error method.

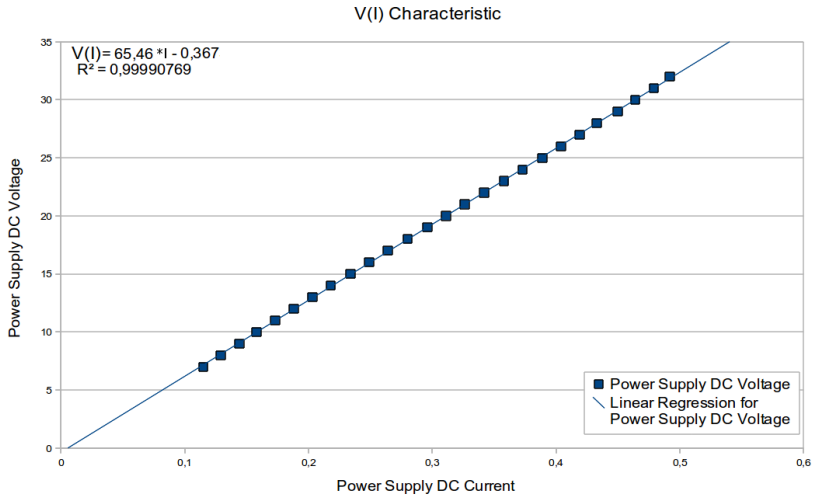


Figure 4.8: $V_{RFamplitude}(I_{DC})$ characteristic of the Class-E amplifier. Courtesy of Luis Carlos Cotimos Nunes.

Aiming for 30V maximum output, and according to Section 4.8 the amplifier must be able to source 500mA. This way, the power transistor does not need to be a high-power transistor, which means that a faster one can be selected, since the speed of the MOSFET is largely dependant on its total input charge, which depends on the maxim power capability of the transistor.

4.6.2 Gate controlling method

Since the power transistor is a high-side N-channel MOSFET, the gate must be controlled by a floating circuit. This happens because when the transistor is turned on, the MOSFET source is (roughly) at the power-rail voltage. In order to keep V_{GS} high, the gate driver circuit must either be fed by a voltage higher than the power-rail, or by a floating power supply. The

floating power supply option is much better, because the former option would drive the gate of the MOSFET at very high voltages.

To understand why, suppose that the power rail is 30V, and the secondary power supply is 35V in order to drive the gate at $5V$. When the transistor is in its off-state and the gate-driver charges its gate, V_{GS} would be momentarily 35V which is above the V_{GS} stress limit for most transistors, and then stabilize at 5V. On the other hand, when the transistor would be turned off, V_{GS} would be momentarily at -30V, which is also too large, and then stabilize at 0V.

Moreover, the floating power supply is the option in most applications [32].

In order to maximize the switching speed, an integrated gate driver will be selected.

4.6.3 Main system blocks

Considering that the complete system would consist in a low-pass filter, a comparator, the floating gate-driver, the MOSFET, the output filter (second-order) and the feedback, the circuit will assemble the one depicted in Figure 4.9. The floating power supply is composed by the diode D1 and the capacitor C2. This imposes a bootstrap condition so that the MOSFET is turned-off at the initial condition, and C2 can be charged. V_{CC} is the voltage amplitude which will control the gate.

The cut-off frequency of the low-pass filter at the input is selected to be 190kHz ,since the self-oscillating frequency is aimed at 1MHz to 2MHz.

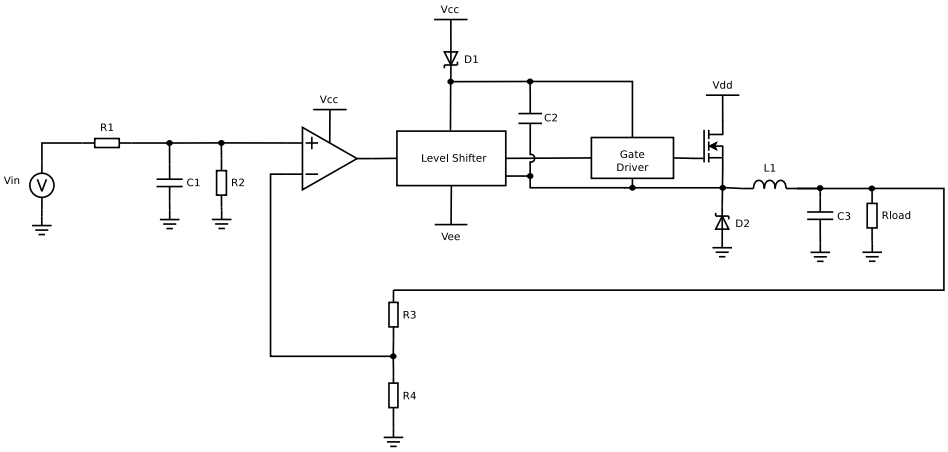


Figure 4.9: The overall circuit.

4.6.4 Transistor Selection

The switching speed of a transistor is mainly determined by the total input charge[4], and the efficiency is not only determined by its R_{DSon}, but also by the output capacitance, since the power dissipated when switching between V_{DD} and 0 is roughly $C_{OSS}V_{DD}^2 f$, where C_{OSS} is the output capacitance, V_{DD} the switching voltage swing, and f the switching frequency (independent on duty-cycle).

[4]The input capacitance is of little value, since it is a non-linear capacitance which is dependant on voltage. The total input charge is the total charge needed to rise the varying input capacitance to a specific voltage level

Looking at these figures of merit, searching for a suitable MOSFET in the market yielded the transistor ZXMN10A11G from Diodes, Inc.. The maximum voltage is 100V, and the maximum current is 1.7A. The PCB layout must include a large copper pad to serve as heat sinker.

Another important decision is on the voltage used to charge the gate. The voltage selected should be minimal, since it must be provided by a gate driver whose dissipated power should also be kept as small as possible. The power dissipated in the gate driver is roughly $V_G^2 * C_{ISS} * f$ where V_G is the gate voltage which is used to turn the MOSFET on, C_{ISS} is the input capacitance[5], and f is the switching frequency.

However, if the gate voltage is too low, the R_{DSon} may increase too much. Inspecting the transistor transfer characteristic, shown in Figure 4.10, 5V is the best choice since 10V does not reduce the R_{DSon} resistance very much, yet, quadruplicates the dissipated power in the gate driver. Moreover, a voltage lower than 5V is not enough for the gate-driver to function.

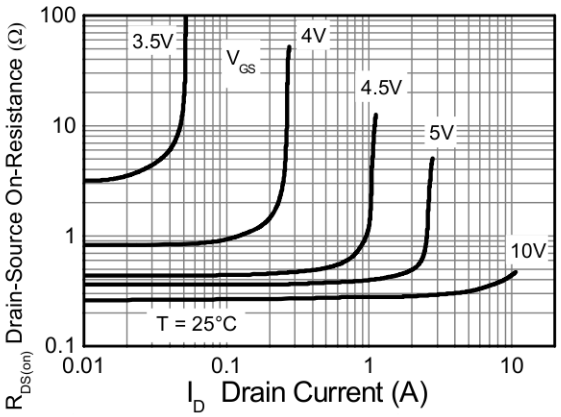


Figure 4.10: R_{DSon} resistance vs drain current, for various gate voltages. Note that the maximum drain current will be 0.5A.

Moreover, some SPICE simulations were made, switching the output stage at 1MHz, using $V_{PP} = 25$V, and $Rload = 65\Omega$, for various V_G. The plot of the total dissipated power is depicted in Figure 4.11. This reinforces the use of 5V as the controlling gate voltage.

4.6.5 Gate driver

The gate driver chosen is the EL7155. Although it includes an internal level shifter, the maximum voltages supported do not allow to directly control the gate without a floating circuit. Hence, the gate driver will be employed with a floating circuit in order to charge/discharge the gate quickly. The documented propagation time is less than 12ns for a 2000pF load which is likely to be less, since the selected MOSFET has 274pF of input capacitance.

[5]Since the input capacitance is non-linear, the use of a constant capacitance is an approximation solely for the purpose of dissipated power estimation.

4.6.6 Comparator

The comparator is one of the most important components, since it has to be fast, yet low-power. The first option was the Maxim's MAX9600 because the documented propagation time is 250ps, however, since it draws approximately 300mW, the final choice was the National's LMH7220 which consumes 120mW and has a maximum propagation time of 3.5ns.

The output of the LMH7220 is Low-Voltage Differential Signalling (LVDS)n which requires a differential interface.

4.6.7 Level-shifter

Since the output of the comparator is differential, the level shifter employed a differential pair of BJTs. The differential pair is fed by a $2.8mA$ current source.

Figure 4.12 shows the level shifter employed, with the external signals indicated.

In order to minimize the output voltage swing of the level shifter (to increase speed), the resistors R5 and R6 were chosen so that the input of the gate driver swings between 0.5V and 3.3V instead 0V and 5V (the gate driver V_{IL} is 0.8V and the V_{IH} is 3V). Please note that the resistor R6 is supposed to have a constant voltage across its terminals since its current is the same as the current source.

D3 is used to avoid that the input of the gate driver inverts polarity, damaging the gate driver.

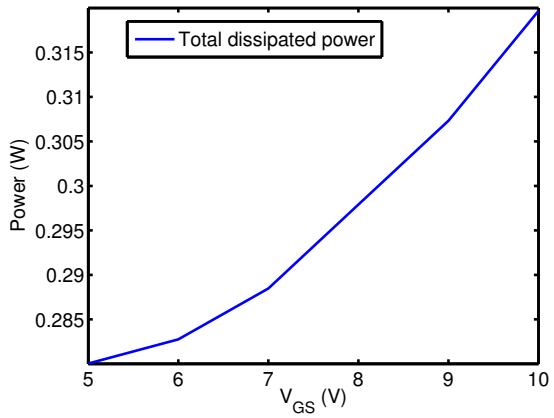


Figure 4.11: Dissipated power in the MOSFET, as a function of V_G voltage. The dissipated power increases due to switching losses at the gate. 5V is the best option. The minimum V_G is 5V, because it is the minimum voltage of the selected gate-driver.

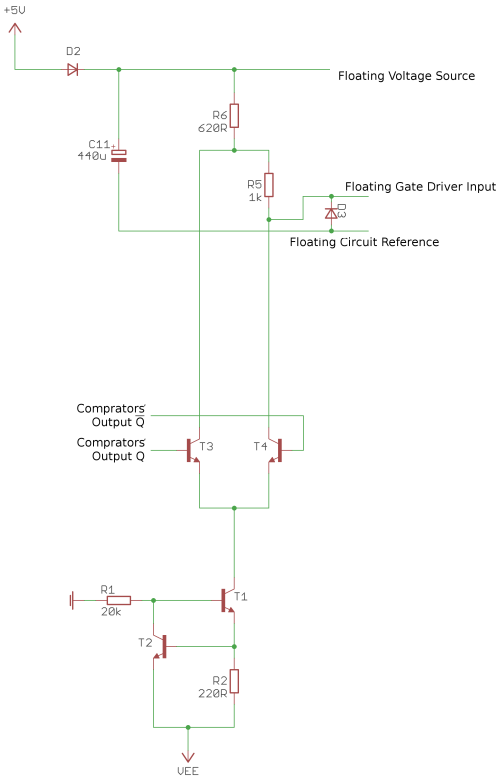


Figure 4.12: Level shifter designed, with all the relevant signals labelled.

4.6.8 Output filter

In order to design the output filter, and yet obtain the most accurate predicted values, the output filter was designed after measuring the overall propagation time of the system as is shown in Chapter 5, Experimental Results.

The filter designed is a second-order filter. Using the mean between the High-to-Low and Low-to-High propagation times, 48.8ns, and using 10uH as inductor inductance, the expected oscillation frequency was plotted against the cut-off frequency (changing the capacitor value). The result is plotted in Figure 4.13. Since the derivative of the curve is roughly constant at its maximum until 1.5MHz, that is the selected cut-off frequency, which is obtained for a capacitance of 1.12nF. A final value of 1.2nF was used.

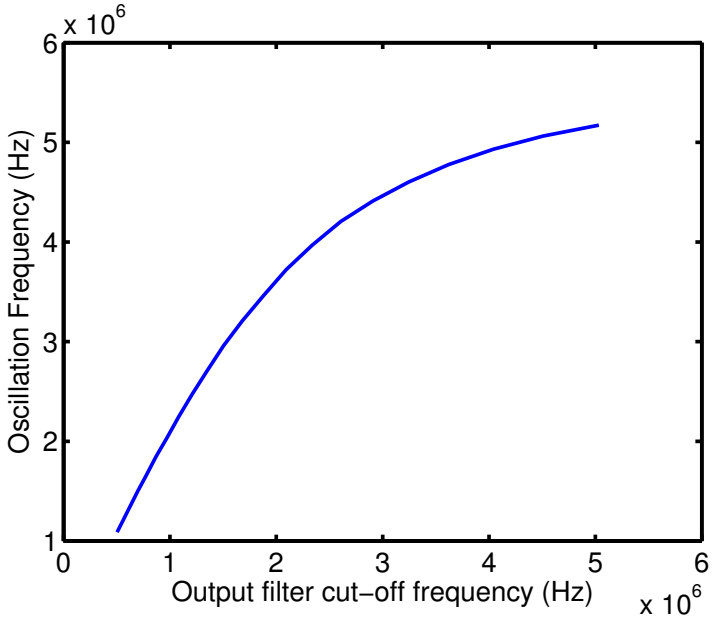


Figure 4.13: Expected oscillation frequency vs cut-off frequency of the designed filter.

4.6.9 Final Circuit and voltage selection

The final circuit is presented in Figure 4.14, which identifies all blocks.

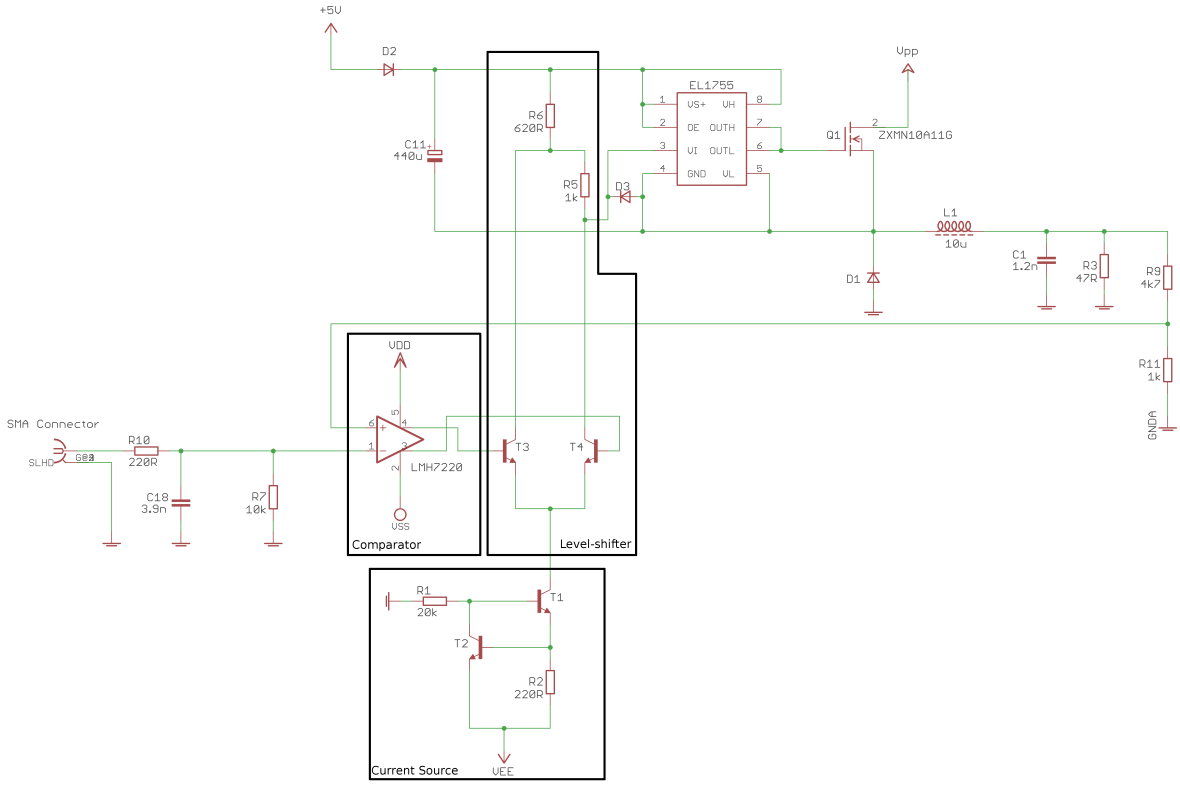


Figure 4.14: Main circuit schematic.

The next step was to select the voltage sources in order to keep the current source always in active mode, and avoid the differential pair to be saturated[6].

The selected voltages are shown in the following table.

Supply name	Voltage
$Vgate$	5V
V_{DD}	7V
V_{SS}	-3V
V_{EE}	-5V
V_{PP}	[10V, 30V]

Table 4.3: Voltages for the several voltage supplies across the circuit.

[6]Although each of the transistors of the differential pair could saturate when conducting, a BJT is much slower when leaving saturation region than leaving active mode.

4.6.10 Power supply

In order to provide all the necessary voltages, different power supplies could be used, but that is impractical. To power the circuit from only two voltages (the higher one, V_{PP}, and the lower one, V_{EE}), a power supply was designed to provide all the other voltages. However,since the system efficiency is also determined from the efficiency of the power supply, the lower positive voltages should not be obtained through the use of linear regulators.

In order to keep the power supply efficient, a DC-DC converter is employed to obtain V_{DD} from V_{PP}, and the 5V V_G is obtained from V_{DD} using a low drop-out regulator. V_{SS} is obtained using a negative low drop-out regulator, fed by V_{EE}.

The final power-supply circuit is depicted in Figure 4.15. No major attention will be given to this circuit, since it has been designed just following the application notes of the respective datasheets.

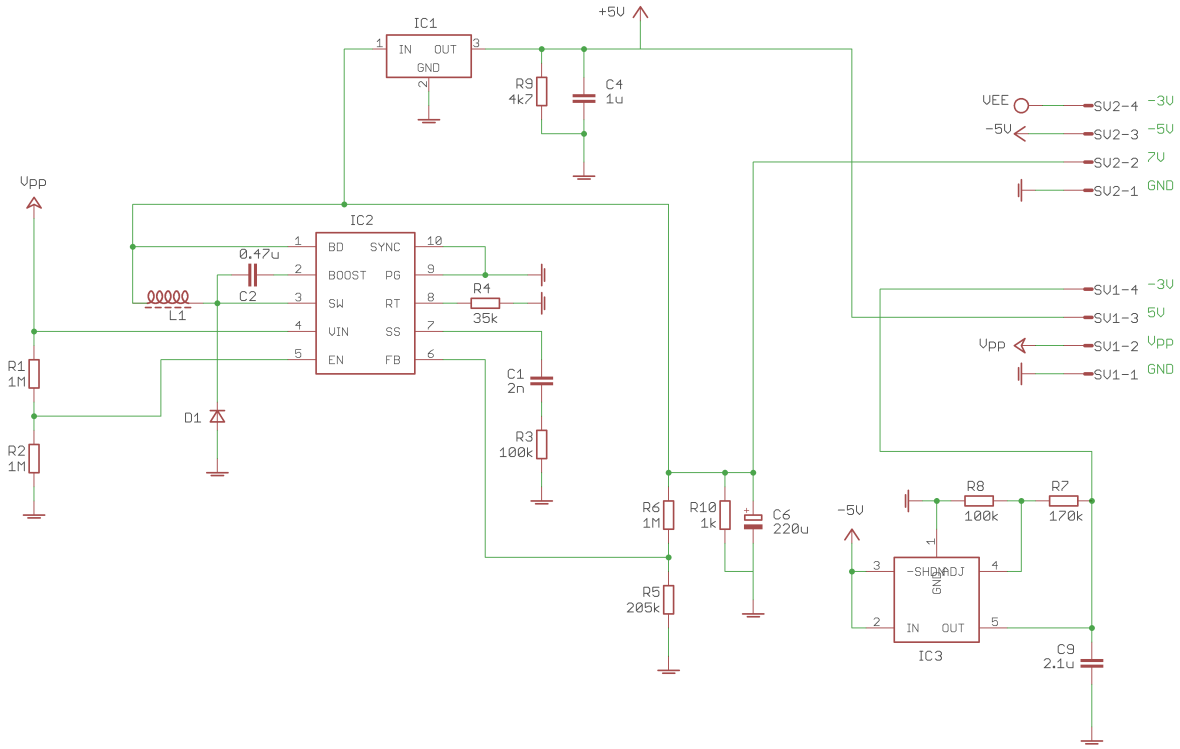


Figure 4.15: Power-supply circuit.

4.6.11 Complete system

Having designed the complete circuit, after successfully simulating it in SPICE the prototype was built. A photo can be seen in Figures 4.16 and 4.17. Everything worked at the first try. Please refer to Appendix D for a complete list of the main components (resistors not listed).

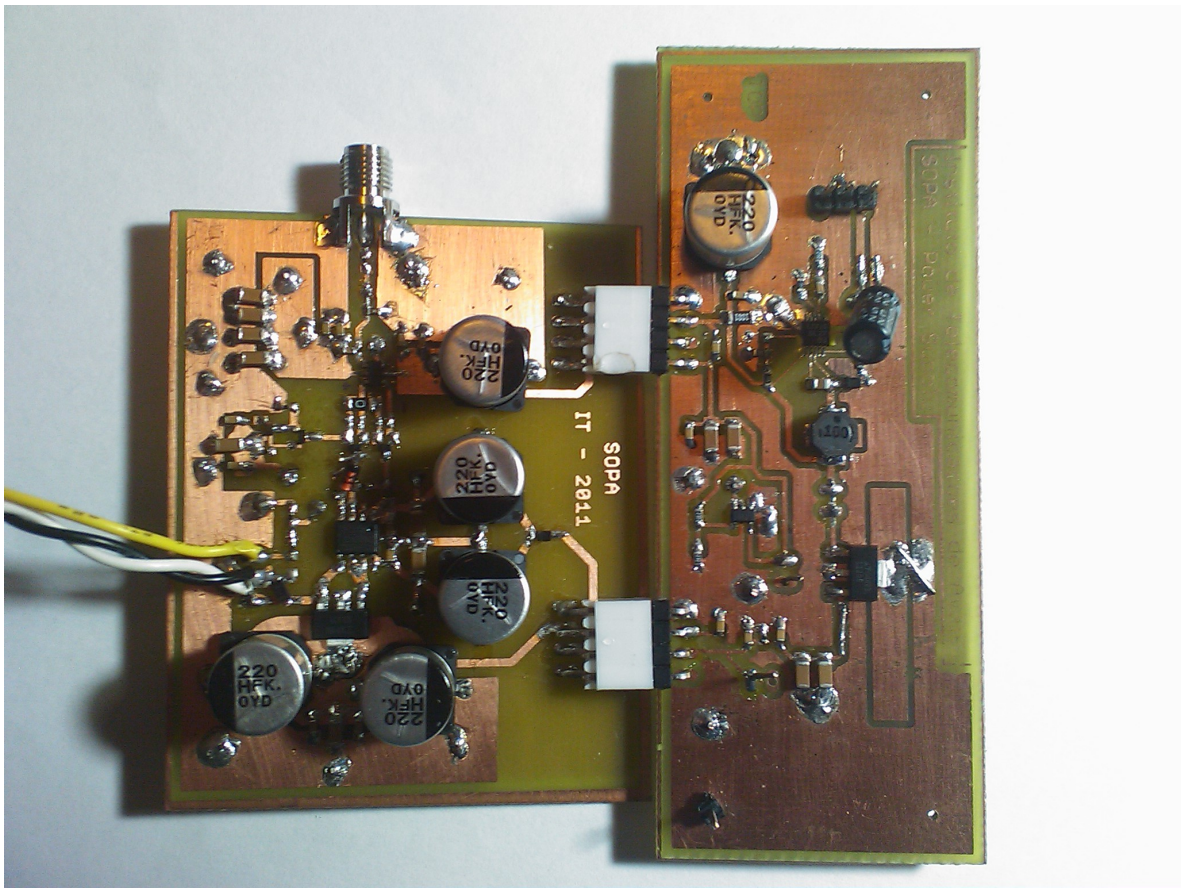


Figure 4.16: Prototype photograph. The right-hand side is the power supply, and the left-hand side is the main circuit. The yellow wire is the feedback.

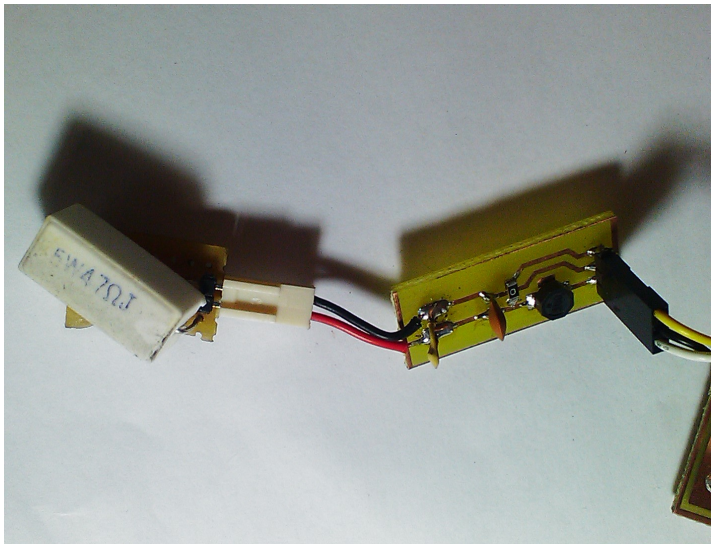


Figure 4.17: Photograph of the output filter, and the 47Ω load.

Chapter 5

Experimental Results

The experimental results were performed in two steps. This was due to the fact that the design of the output filter is dependant on the total propagation delay from the input to the output, and, to obtain the most accurate values, the propagation delay was measured prior to start designing the filter. Moreover, as will be seen, a fix was made in order to improve the propagation delay.

The propagation delay was measured in open-loop, without input low-pass filter, as well as without reconstruction filter (only the 47Ω load), and feeding the inverting and non-inverting inputs[1] with 0.5V and a [0V, 2V] 550kHz square wave, respectively. The duty-cycle of the input wave is approximately 65%.

This duty-cycle different from 50% was selected because some measurements required the use of both oscilloscope channels, making impossible the identification of the state of the output. This way, the larger pulse corresponds to a high output, whereas a smaller pulse corresponds to a low output.

Please recall the circuit, here replicated in Figure 5.1, where the relevant nodes are indexed by letters from A to I.

[1]Please note, as was referred in Chapter 4 (particularly in Figure 4.14), the effective inverting/non-inverting inputs of the complete system are inverted to those of the comparator. This is due to fact that gate driver has and inverting characteristic.

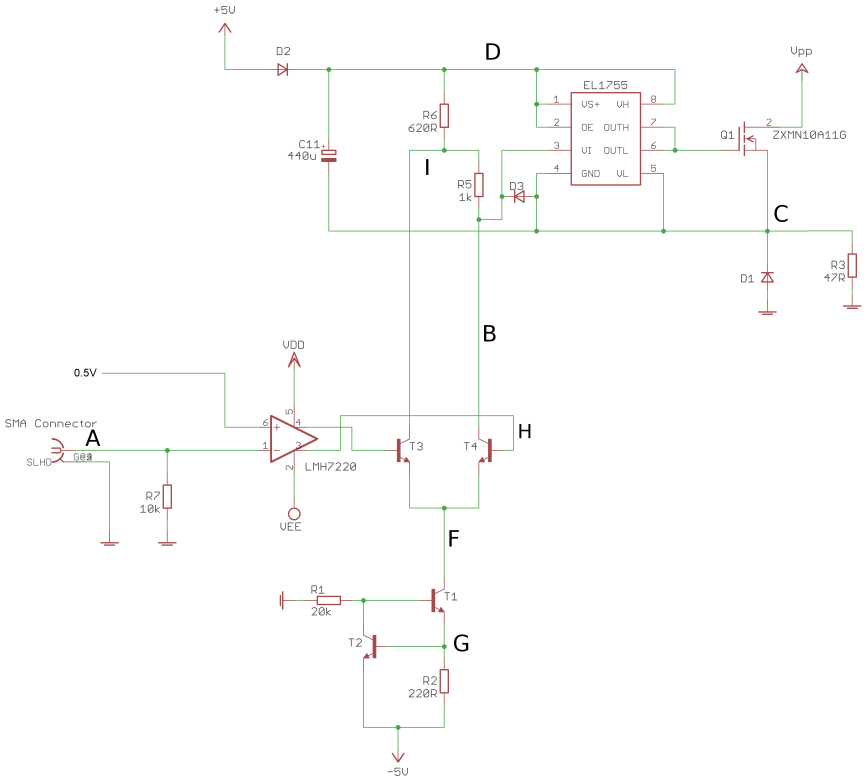
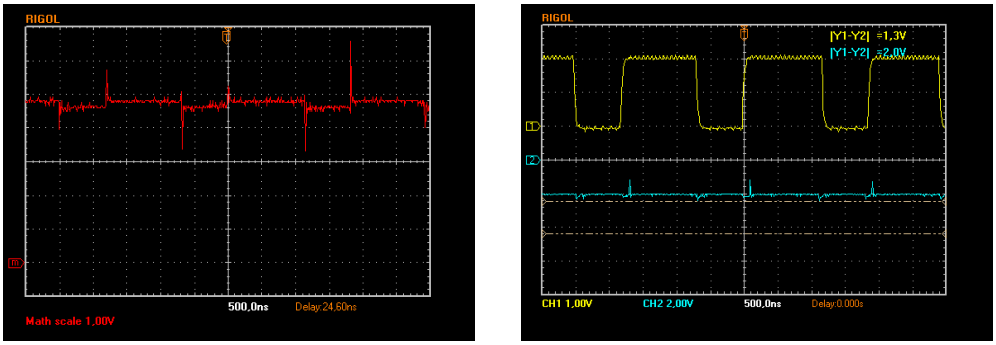


Figure 5.1: Adapted circuit without input low-pass filter, output filter, and feedback. Relevant nodes are indexed.

5.1 First system-check

After verifying that the system's output was switching between 0V and 16V, the first experimental step was to check whether the floating power supply (voltage between nodes **D** and **C**) was working as expected. In Figure 5.2a the resulting wave is depicted.

Moreover, the current source was also checked, to make sure that it was always in active mode. The voltage at **G** was constant and equal to 0.64V, and the voltage at **F** is plotted in Figure 5.2b. The vertical cursors are set to the minimum current source voltage, and to the voltage at node **G**. The resulting difference is 2V, which means that the BJT is always in the active mode.



(a) Floating supply voltage over time (b) Current source output voltage over time

Figure 5.2: Floating supply voltage and output voltage of current source, over time.

The Voltage ripple in the floating power supply ($0.2V_{pp}$) is acceptable. Since the duty-cycle of the output is larger than 50%, the larger pulse duration corresponds to the output high state.

The voltage spikes that are seen are very intriguing, because the positive one occurs when the floating supply rises above V_{pp} and the negative one when the floating supply goes down. If the cause was a capacitance from **D** to ground, the opposite would occur. Moreover, this effect was not observed in the SPICE simulation.

However, one must see that those edges are not only points where a high $\frac{dv}{dt}$ exists. In order to turn the MOSFET on and off quickly, the gate driver draws a lot of current to charge the gate of the MOSFET (according to SPICE simulation, the majority of the gate charge (2.5nC out of 3.3nC) is transferred in less than 15ns). That corresponds to a high $\frac{di}{dt}$, as can be seen in the SPICE plot of Figure 5.3. That suggests that the voltage spikes in the floating power supply are caused by strain inductance (Equivalent Series Resistance (ESR) in the capacitors would have a similar effect, but with much less intensity, and with symmetric signal). Adding as little as 1nH in series with the floating capacitor[2] was enough to yield similar results in SPICE.

From this, I conclude that if no efforts were made to minimize the distance between the decoupling capacitors and the gate driver, this effect could compromise the system. This is definitely a very important aspect, and any further version would have the coupling capacitors even closer to the gate driver.

[2]In the SPICE model designed, all parallel decoupling capacitors were lumped into one single element.

Another strain inductance worth to mention is the MOSFET source inductance, which causes some (visible in Figure 5.4) ringing at the output.

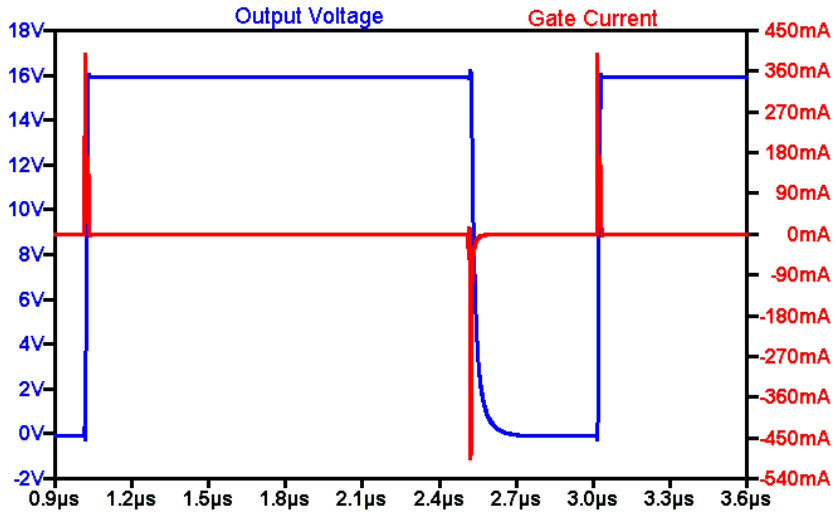


Figure 5.3: Gate current obtained by SPICE simulation.

Having checked the more complex parts of the circuit, the next step was to measure the propagation delay.

5.2 Propagation delay measurements

In Figure 5.4 the rising and falling edges of the input and output are seen.

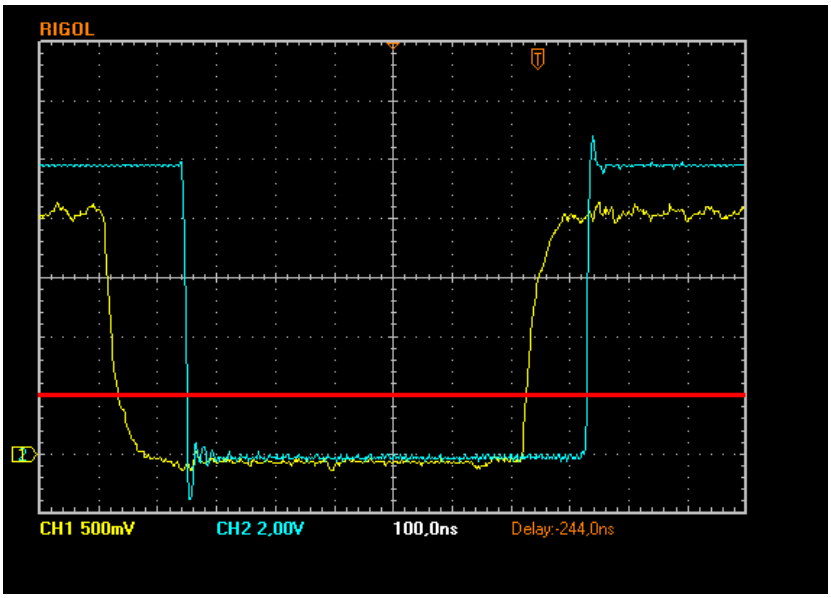


Figure 5.4: Input signal (Ch1) and output signal (Ch2). An artificial red line at $0.5V$ was drawn to shown the switching threshold of the input signal.

Defining as propagation delay the time interval between the crossing of the threshold, and half the voltage swing of the output signal, the measured delays are in Table 5.1.

The rising/falling time is defined as the time interval between 10% and 90% of the rising/falling edge.

	H	B	C (total propagation)
Low to High	12.0 ns (12.6 ns)	60 ns (137 ns)	107 ns (6.6 ns)
High to Low	10.4 ns (8.6 ns)	112 ns (223 ns)	118 ns (7.0 ns)

Table 5.1: Measured propagation delay between input and various nodes according to Figure 5.1. The rising/falling times are in parenthesis.

Please, note that the total propagation time is not the sum of the propagation times over the various nodes. That is because the thresholds of each stage are not at the centre. However, these figures are just for qualitative purposes.

With these figures, the node **B** is definitely responsible for the overall propagation time. However, in the SPICE simulation, the propagation time in that node is about 14 ns and 11 ns for High to Low and Low to High, respectively (refer to Figure 5.5).

The voltage measured at nodes **B** and **I** is plotted in Figures 5.6 and 5.7.

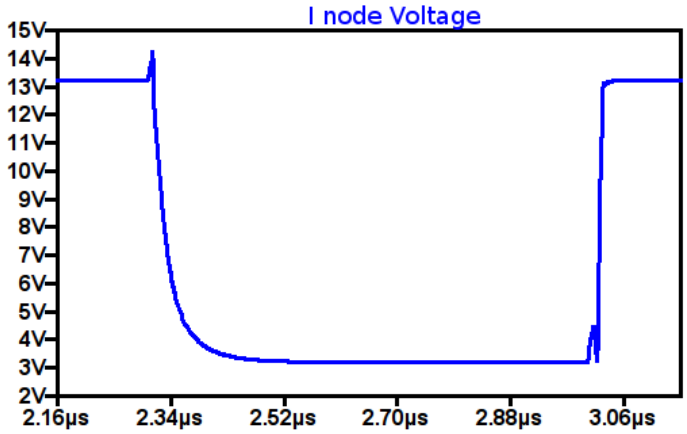
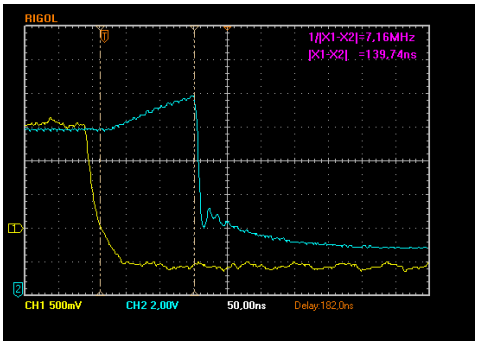
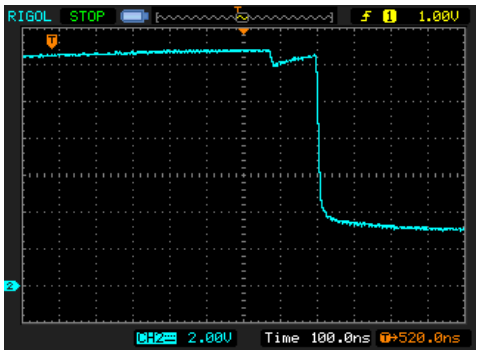


Figure 5.5: Voltage at node **I** in SPICE. A big discrepancy exists between laboratory data and simulated data, since this wave shows almost no propagation delay. That will be further inspected.

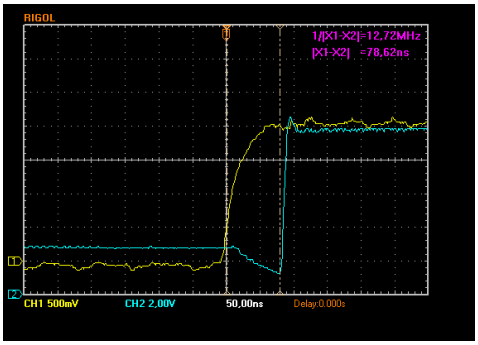


(a) Voltage at node **B** in SPICE.

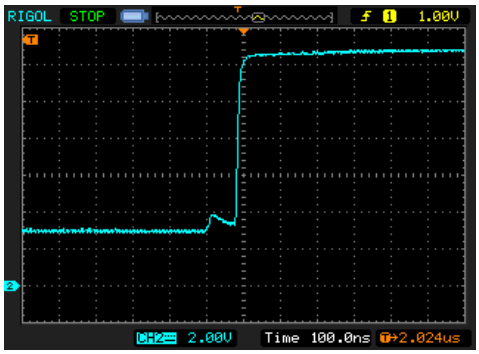


(b) Voltage at node **I** in SPICE.

Figure 5.6: Voltage at nodes **B** and **I** at High to Low transition.



(a) Voltage at node **B** in SPICE.



(b) Voltage at node **I** in SPICE.

Figure 5.7: Voltage at nodes **B** and **I** at Low to High transition.

The voltage in node **I** should be always 3V above the MOSFET source voltage. However, before the source falls to 0V, node **I** rises. That means that the current across R6 diminishes. Since the current source is working (as was confirmed in previous section), the only points where that current could be injected into the branch (so that it does not cross R6) is either from the gate driver IC input pin, or from the diode D3.

Inspecting the datasheet of the gate driver, the input impedance of the input pin is $50M\Omega$, and its capacitance is 3.5pF, which draws the attention out from the gate driver IC.

Looking at the diode datasheet, the capacitance is around 43pF. Inspecting the circuit, the input impedance seen from the diode into the node **B** is $1.62k\Omega$, which yields a time-constant $\tau = RC = 1620\Omega \cdot 43pF = 70ns$. This is a very high value, considering that it is possible to have less capacitance in the diode, if another choice was made.

Since the SPICE simulation did not gave the same results, I inspected the SPICE model of the diode, and figured out that the C_{JO} capacitance (the zero voltage junction capacitance) was set to 84fF. Downloading the spice model directly from a manufacturer[3], I figured out that the C_{JO} was 84.37pF, which is completely different. Using the new model, the simulation results were closer to those found in laboratory.

The simulated wave is plotted in Figure 5.8.

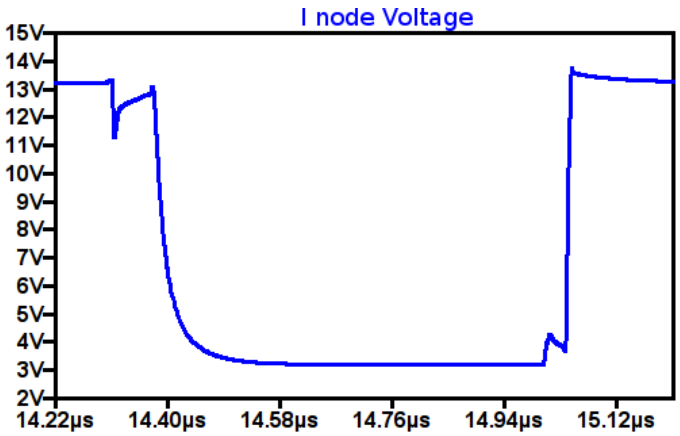


Figure 5.8: Voltage at node **I** in SPICE. Although the High to Low propagation delay is not 110ns as experimental data showed, 63ns were measured in simulation. Before this fix the propagation delay was much more discrepant, 11ns.

Since this diode raised an excessive capacitance problem, I switched the previous diode, PMEG4005EJ by a regular 1N4148. This choice was made because the diode capacitance of the 1N4148 is about 4pF, one tenth of the PMEG4005, and, yet, the reverse recovery time is short as well.

After replacing the diode, the new propagation times measured are in the Table 5.2, and the switching waveforms in Figure 5.9.

[3]The previous model was downloaded from an unofficial SPICE models pack. Fortunately, I only used one model from that pack.

	H	B	C (total propagation)
Low to High	12.0 ns (12.6 ns)	40 ns (79 ns)	49.6 ns (6.1 ns)
High to Low	10.4 ns (8.6 ns)	70 ns (130 ns)	48 ns (6.8 ns)

Table 5.2: Measured propagation delay between input and various nodes according to Figure 5.1 after changing the diode D3. The rising/falling times are in parenthesis.

5.3 Closed-loop DC measurements

Adding the output filter to the system, and closing the feedback path, the performance of the system was measured in terms of self-oscillation frequency vs DC input voltage, the DC transfer characteristic, the efficiency vs input signal, and the sinusoidal output for a sinusoidal input.

The closed-loop measurements were performed with a power supply voltage V_{PP} of 16V, in order to drive more power into the load.

To perform the SPICE simulations, a MATLAB script was written to automatically simulate and register data.

The graphical data is plotted in Figures 5.10, 5.11, and 5.13. The theoretical curves were calculated using 49ns as overall propagation time.

The theoretical model fitted almost perfectly in the experimental results. The largest difference is that the Figure 5.10 is asymmetric, unlike the theoretical prediction. That is probably due to the fact that the V_{PP} source has finite output resistance, hence, to yield a larger mean value the duty-cycle must be larger, leading to a lower frequency.

Likewise, efficiency results are also different between measured experimental data and SPICE simulation data. It is worth to mention that the SPICE model did not include the power supply designed to provide the necessary voltages, hence, the difference is caused by the power dissipated in the power supply, which has an efficiency around 80%

As for the Figure 5.11, the SPICE data fitted in theoretical data, and experimental data exhibited an NMSE equal to 0.006 (-44.4370dB).

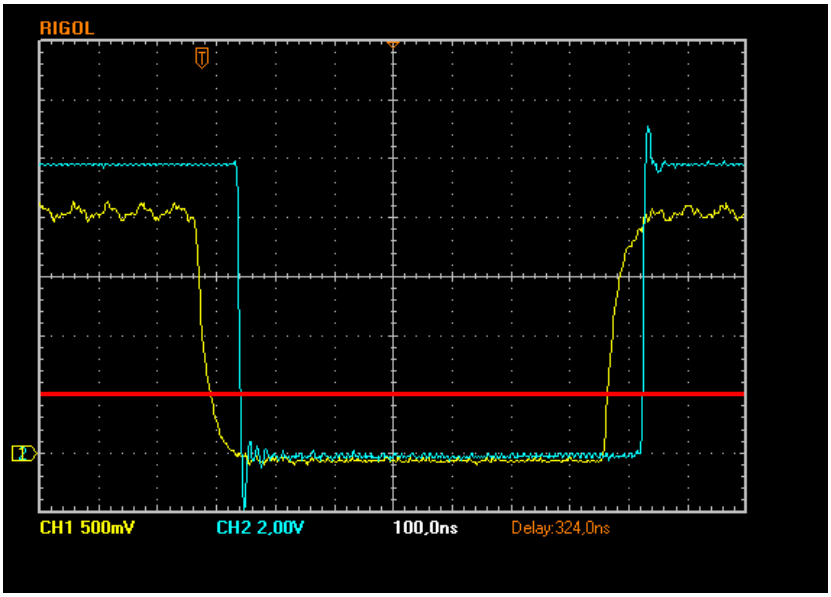


Figure 5.9: Input signal (Ch1) and output signal (Ch2) after changing the diode after changing the diode D3. An artificial red line at 0.5V was drawn to shown the switching threshold of the input signal.

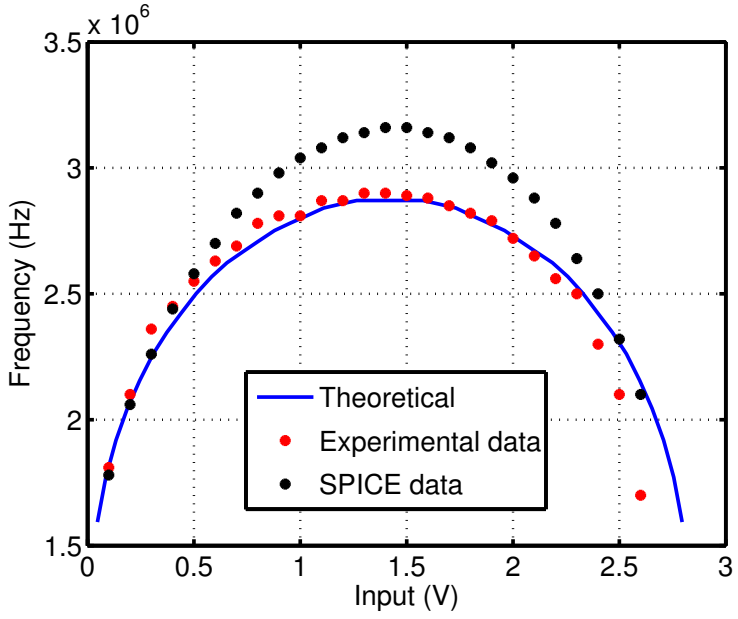


Figure 5.10: Self-oscillating frequency vs DC input amplitude, theoretical prediction, and SPICE simulation.

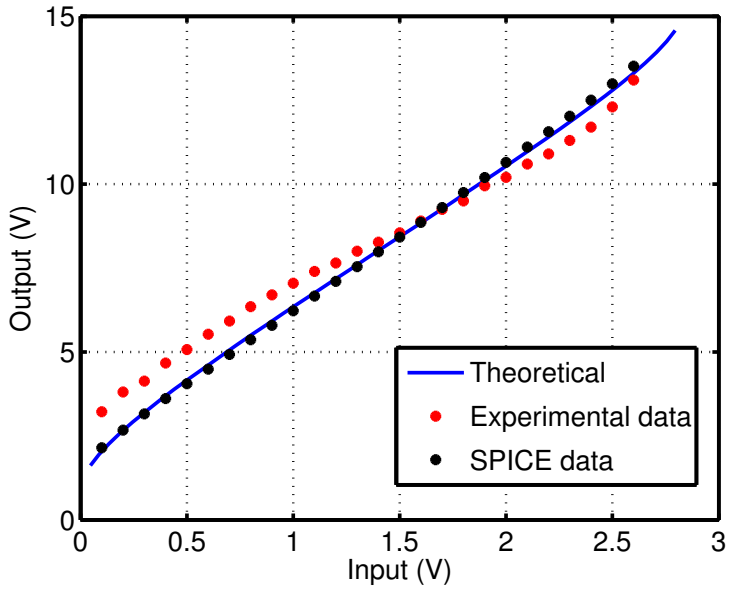


Figure 5.11: Vo(Vi) characteristic of the experimental prototype, theoretical prediction, and SPICE simulation.

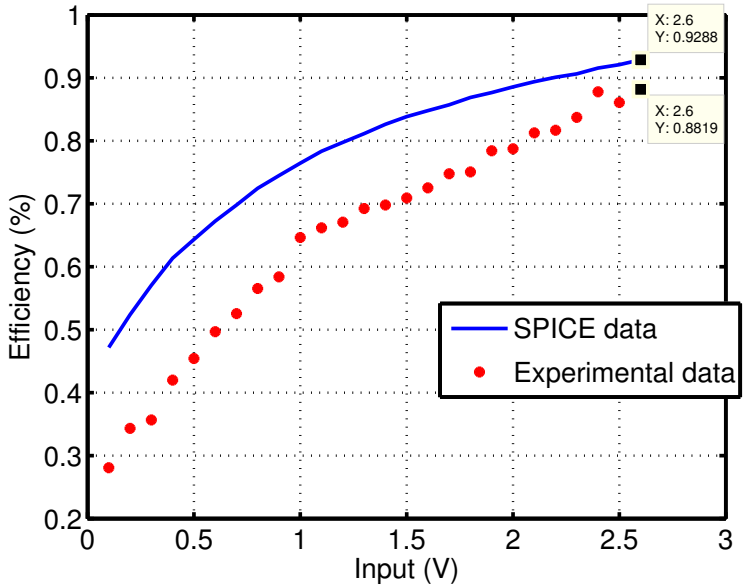


Figure 5.12: Efficiency of the experimental prototype and SPICE simulation.

5.4 Closed-loop sinusoidal-input measurements

In order to quantify the non-linear distortion, the signal was fed with a DC input plus a sine wave. The DC amplitude is 1.3V since it corresponds to the input which yields the 50% duty-cycle (the maximum frequency, from Figure 5.10). The noise floor during measurements was -30dB, so the third harmonic is only plotted above that threshold. Moreover, the second harmonic never had more than -30dB, so it is not plotted. Moreover, simulations with MATLAB were made, using the measured quasi-static Vo(Vi) characteristic to predict the first, second and third harmonics.

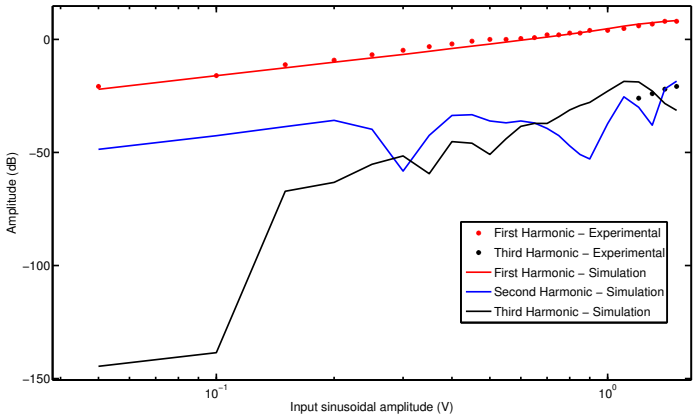


Figure 5.13: Measured and simulated output harmonics for a sinusoidal input. Simulations were performed considering the Vo(Vi) characteristic measured previously.

Another important characteristic, is the Adjacent Channel Power Ratio (ACPR). In order to predict it, the measured and theoretical quasi-static Vo(Vi) characteristics were used in MATLAB simulation, considering a multi-sine input, having 1kHz as maximum frequency. The resulting output spectrum is plotted in Figure 5.14.

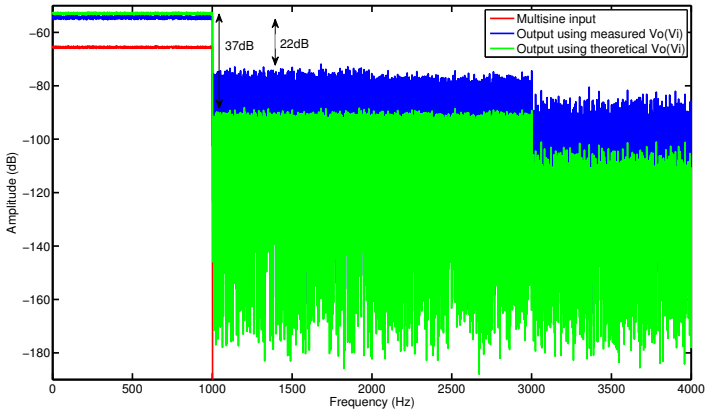


Figure 5.14: Input and Output spectrum, for a multisine input. Measured and theoretical quasi-static characteristics are used.

The ACPR of the quasi-static Vo(Vi) characteristic measured is 22dB, and using the theoretical characteristic, only 37dB are possible. This is too low for what modern communication standards demand. This means that pre-distortion should be employed, in order to linearise the system. The linearity also increases if the ration between the oscillating frequency and the cut-off frequency of the filter increases, however, that reduces the bandwidth of the system, and is likely to be a bad option if the amplifier is supposed to have the maximum bandwidth allowed by the technology.

Chapter 6

Final Conclusions

In this work a lot of information was gathered in order to understand existing methods to reach efficient amplification of RF signals, in particular, on self-oscillating amplifiers.

This kind of amplifiers are very interesting, and do not require high-order low-pass filters in order to oscillate. Te use of a propagation delay and hysteresis was exposed here, and a set of necessary conditions was derived, that predict the self-oscillation frequency of a zeroth-order self-oscillating power amplifier as well the quasi-static transfer characteristic. Moreover, an hypothesis was made, concerning negative hysteresis. Hence, a negative hysteresis relay was designed and simulated, in order to test, with success, a particular set of solutions given by the mathematical model.

Moreover, one self-oscillating power amplifier, oscillating at 2.8MHz, with a bandwidth of 180kHz and capable of delivering up to 15W was designed, where all the major aspects of the design of this type of system were described.

The mathematical conditions have shown to be capable of accurately predicting the system-level simulations, as well the experimental data with an acceptable degree of accuracy.

Although the experimental prototype does not have enough bandwidth to cope with modern high-frequency base-band signals, neither linearity, the purpose of this design was to experimentally validate the mathematical model.

This Thesis was successfully completed, since the whole work included the derivation of a mathematical model, system-level simulation, design of a functional amplifier, and finally the mathematical model was tested against experimental data.

6.1 Future work

Having being awarded with the 2010 MTT-S Undergraduate/Pre-Graduate Scholarship, the particular SOPA of this work will be employed in a Class-E RF amplifier, and subsequently the loop will be closed using the envelope of the RF output signal obtained using an envelope detector. This is an innovative approach, and will constitute a proof-of-concept.

Another topic left open is negative hysteresis. This kind of hysteresis should be inspected, for the purpose of SOPA, to check if it has any practical advantage over regular relays namely in terms of linearity.

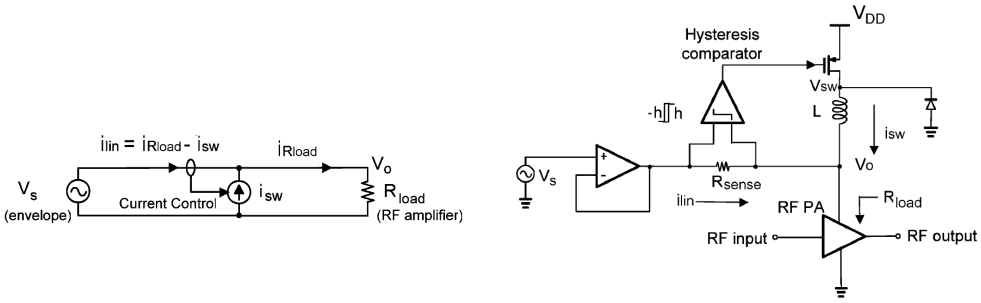
Appendix A

Analysis of quasi-linear envelope amplifier

In this appendix, a insight of the quasi-linear envelope amplifier, a hybrid between switching-mode and linear amplifiers presented in [22], will be given.

This system was analysed mainly to understand if that system uses the same principle of self-oscillation, as the one studied throughout this work.

The system-level schematic, as well the circuit-level, are shown in Figure A.1.



(a) System-Level (b) Circuit-level

Figure A.1: System presented at [22].

The working principle of this system is manly the amplification of signal by the self-oscillating switching stage, and the correction of the error by the linear amplifier. Error of switching amplifiers is lower when the switching frequency is higher than the signal, the linear amplifier will only amplify the error for high-frequency signals.

This is done simply by making the SOPA's input error signal (i.e. the signal fed to the comparator) equal to the output current of the linear stage.

First of all, in order to get the essence of the system, the resistor R_{sense} will be neglected. That does not constitute a loss of accuracy if the comparator input is considered to be $I_{lin}-I_{sw}$ or, at the circuit-level, the feedback of the linear amplifier is taken from the node V_o. This step is not necessary, but enlightens the fact that the output V_o has no ripple, since it is

surpassed by the linear stage, which ensures that V_o is a replica of the input signal V_i.

This can be proven by developing the linear system equations in Laplace

$$I_{lin}(s) = \frac{V_s(s) - V_o(s)}{R_{sense}}$$

$$V_o = R_{load} \cdot \left[I_{lin}(s) + \frac{1}{sL} \left(V_{sw}(s) - V_o(s) \right) \right]$$

which yields

$$V_o(s) = \frac{\frac{R_{load}}{sL} V_{sw}(s) + \frac{R_{load}}{R_{sense}} V_s(s)}{\frac{1}{R_{sense}} \left[R_{sense} + R_{load} \left(\frac{R_{sense}}{sL} + 1 \right) \right]}$$

and finally

$$\lim_{R_{sense} \to 0} V_o(s) = \frac{\frac{R_{load}}{sL} V_{sw}(s) + \frac{R_{load}}{R_{sense}} V_s(s)}{\frac{1}{R_{sense}} \left[R_{sense} + R_{load} \left(\frac{R_{sense}}{sL} + 1 \right) \right]} = V_s$$

Continuing the analysis without R_{sense}, thus making $V_o = V_s$, the non-linear stage can be redrawn as is depicted in Figure A.2. Note that the second sum models the dependency of the slope of I_{sw} with V_o, which is the independent variable (in contrast with the former topologies, where the only independent value was injected in the input of the comparator). Moreover, note that this SOPA works in current mode, and that it is not aimed at the output (R_{load}), but at the current of the linear-stage. They work as two separate entities.

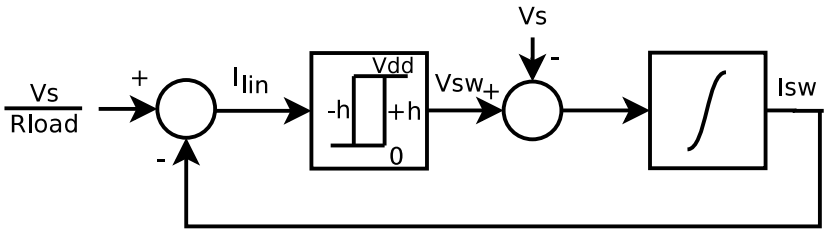


Figure A.2: Switching stage system-level description of F.Wang's Hybrid-EER amplifier

To calculate the self-oscillation frequency of this system, the propagation-delay effect will not be considered, only the hysteresis of the comparator, which has the thresholds $+h$ and $-h$. Being the output of the comparator V_{sw} equal to V_{DD} or 0, then, when I_{sw} increases, the slope shall be $\frac{1}{L}(V_{DD} - V_s)$, and when I_{sw} decreases, the slope is $-\frac{1}{L}V_s$. This makes the period of the self oscillation equal to

$$T_{osc} = \frac{2hL}{V_{DD} - V_s} + \frac{2hL}{V_s}$$

thus the frequency shall be

$$F_{osc} = \frac{V_s(V_{DD} - V_s)}{2hLV_{DD}} \tag{A.1}$$

which exactly assembles the frequency dependency of [13], meaning that the modulation scheme is the same as the presented there.

By this, it is possible to conclude that this system can be analysed without the theory presented in this work, mainly because the time-domain analysis is enough.

Appendix B

Analysis of a first-order self-oscillating modulator

In this appendix a modulator with a first-order reconstruction filter, propagation delay τ, and unitary feedback, will be analysed, and the analytical expressions for the frequency and output duty-cycle dependency over input will be derived.

This analysis shall be done, since the rest of the thesis is based on numerical equations to maintain applicability over a wide range of systems, from where is not possible to derive an analytical equivalent. However, this particular system which works on the same basis, can be fully analysed from time-domain, yielding full analytical expressions.

First of all, the system under analysis is depicted in Figure B.1.

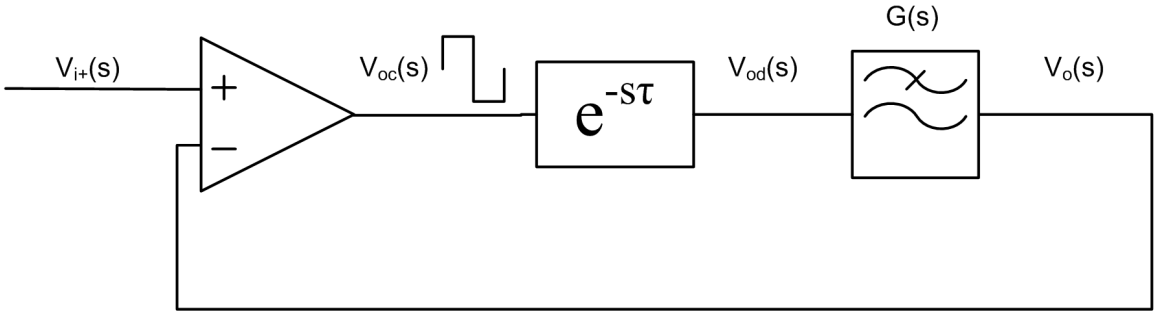


Figure B.1: First-order feedback system. G(s) represents a first-order low-pass filter.

The first step shall be the derivation of the oscillation frequency, and then, the input-to-duty-cycle characteristic.

B.1 Deriving the oscillation frequency

The step-response of a first-order filter, with a time-constant T_p is given by,

$$V(t) = L + (V(0) - L) \cdot e^{-\frac{t}{T_p}} \quad , t \in (0, +\infty) \tag{B.1}$$

Where L depicts the amplitude of the step and $V(0)$ is the initial condition. Since it is a first-order system, the output necessarily follows the only state-variable, thus, the output fully represents the state of the system[1].

Considering the input $V_{in}(t) = V_{in}$, $\forall t$, that means that the modulator can be considered to be in a stationary state. Considering that the relay switched from $+L$ to $-L$ at $t = 0$, so that the output at $t = 0$ is $V_o(0) = V_{in}$ since the relay switches when $V_o(t)$ crosses V_{in}, then, on all these conditions, the waves in the system should assemble the ones in Figure B.2.

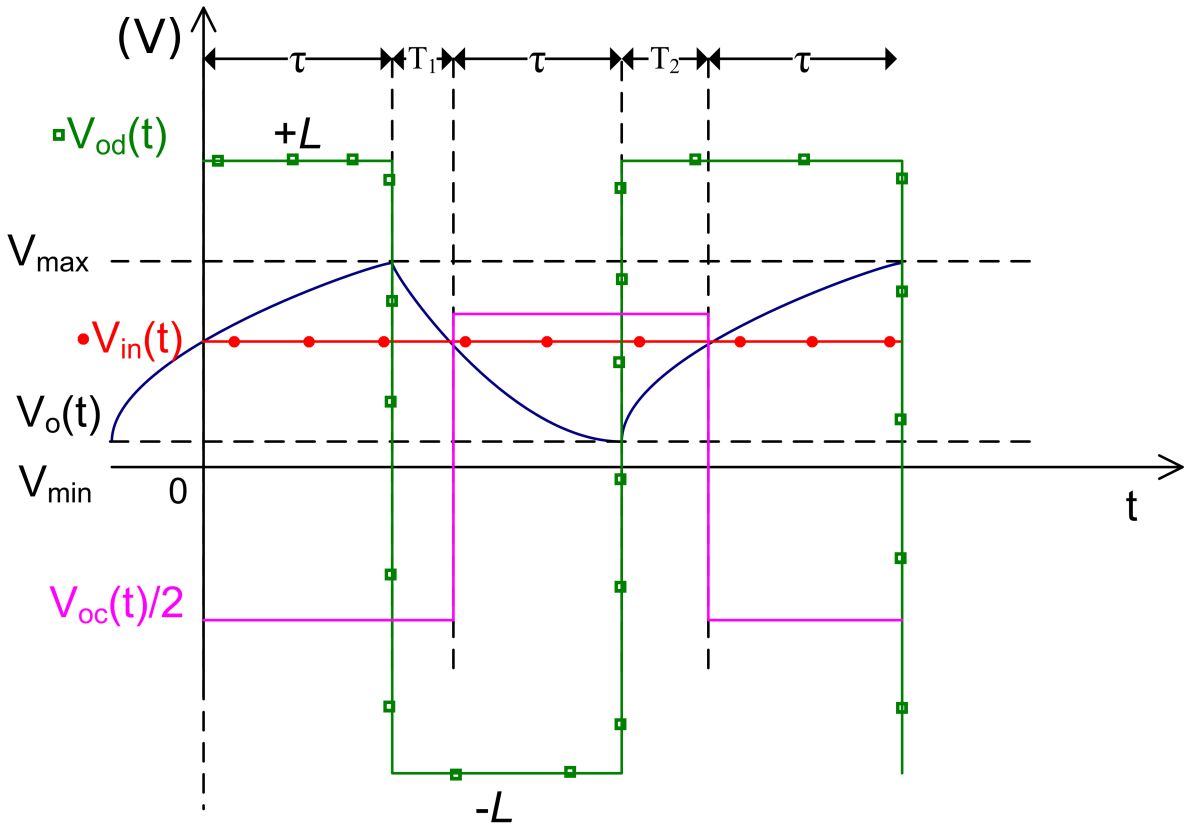


Figure B.2: Waves at the several nodes of the system, over time. The output of the relay V_{oc} is depicted with half the original amplitude, in order to clarify the graph.

In order to obtain the frequency oscillation, is necessary to obtain T_1 e T_2.

To achieve that, the system will be analysed in four phases:

- For $t \in [0, \tau)$, the output is given by

$$V_o(t) = L + (V_{in} - L) \cdot e^{-\frac{t}{T_p}}$$

At $t = \tau$, V_{od} switches to $-L$, since $V_{od}(t) = V_{oc}(t - \tau)$, and V_{oc} switched at $t = 0$. Since

[1]No direct transmission from input to output will be considered, to keep simplicity. Although the output can be a superposition of the input and the state-variable, since the input is known, there is no loss of generality.

the derivative of the output of the filter $V_o(t)$ is the same as the input $V_{od}(t)$, at $t = \tau$ the output $V_o(t)$ reaches a maximum, which shall be called V_{max}.

From that, one can conclude that $V_{max} = L + (V_{in} - L) \cdot e^{-\frac{\tau}{T_p}}$.

- For $t \in [\tau, 2\tau + T_1)$, the output $V_o(t)$ is given by $V_o(t) = -L + (V_{max} + L) \cdot e^{-\frac{t-\tau}{T_p}}$.

  Since the relay switches when $V_o(t) = V_{in}$, T_1 is obtained by solving the equation $V_{in} = -L + (V_{max} + L) \cdot e^{-\frac{t-\tau}{T_p}}$, which yields:

$$T_1 = -T_p \cdot \ln\left(\frac{V_{in} + L}{V_{max} + L}\right) \tag{B.2}$$

  After τ, V_{od} switches due to the propagation delay τ. For the same reasons as before, the output of the filter at that point will be called V_{min}.

  In order to obtain V_{min}, which occurs for $t = 2\tau + T_1$, and since $V_o(\tau + T_1) = V_{in}$, the calculation can be simplified, by solving from $t = \tau + T_1$, since the past of the system is fully described by its state.

$$V_{min} = -L + (V_{in} + L) \cdot e^{-\frac{\tau}{T_p}}$$

- For the interval $t \in [2\tau + T_1, 3\tau + T_1 + T_2)$, V_{od} switches at $t = 2\tau + T_1$ to $+L$, and the output of the filter rises again. This way, it is necessary to calculate the rising time, before the relay switches again, which is noted as T_2.

  The output is given by:

$$V_o(t) = L + (V_{min} - L) \cdot e^{-\frac{t-(2\tau+T_1)}{T_p}}$$

  solving $V_o(t) = V_{in}$ in order of t, T_2 is obtained

$$T_2 = -T_p \cdot \ln\left(\frac{V_{in} - L}{V_{min} - L}\right) \tag{B.3}$$

Having derived all these expressions, which characterize the system waves over one period, the oscillation frequency can be easily obtained just by substitution of V_{max} and V_{min} in T_1 and T_2 expressions, and then calculating $\frac{1}{2\tau+T_1+T_2}$ which is the frequency of each period.

The final form of T_1 and T_2 is

$$T_1 = T_p \cdot \ln\left(\frac{2L + (V_{in} - L) \cdot e^{-\frac{\tau}{T_p}}}{V_{in} + L}\right)$$

$$T_2 = T_p \cdot \ln\left(\frac{-2L + (V_{in} + L) \cdot e^{-\frac{\tau}{T_p}}}{V_{in} - L}\right)$$

After some algebraic manipulation, F_{osc} yields

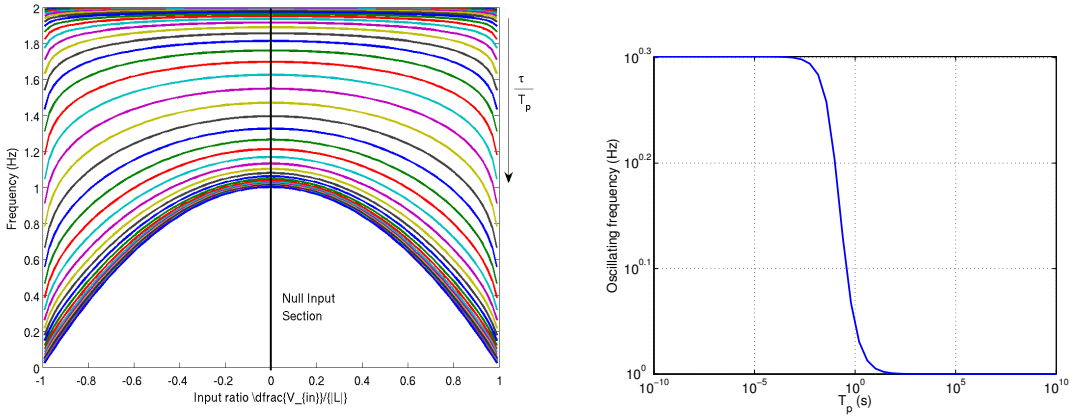
$$F_{osc} = \frac{1}{\left(2\tau + T_p \cdot \ln\left(\frac{2L+(V_{in}-L)\cdot e^{-\frac{\tau}{T_p}}}{V_{in}+L}\right) + T_p \cdot \ln\left(\frac{-2L+(V_{in}+L)\cdot e^{-\frac{\tau}{T_p}}}{V_{in}-L}\right)\right)} \tag{B.4}$$

which, considering that $V_{in} \leq L$, can be further simplified to

$$F_{osc} = \frac{1}{\left(2\tau + T_p \cdot \ln\left(\frac{+4L^2-4L^2 e^{-\frac{\tau}{T_p}}+(L^2-V_{in}^2)e^{-\frac{2\tau}{T_p}}}{(L^2-V_{in}^2)}\right)\right)} \tag{B.5}$$

which shows the frequency dependency with $(L^2 - V_{in}^2)$, and that the frequency decreases when $|V_{in}|$ approaches L.

That dependency is depicted in Figure B.3.



(a) Frequency dependency over input and T_p, for a first-order feedback network

(b) Frequency dependency over T_p for a null input, for a first-order feedback network

Figure B.3: Oscillating frequency in order of $\frac{V_{in}}{|L|}$ for several $\frac{\tau}{T_p}$, keeping $\tau = \frac{1}{4}(s)$: in a) $\frac{\tau}{T_p}$ is diminishing from top to bottom towards the denser curve, as is clearer in b).

From this, one can conclude the following:

- The frequency dependency approximately follows the $D \cdot (1 - D)$ dependency described in [13].
- When τ is kept constant, by making $\frac{\tau}{T_p}$ approach zero, the propagation delay is negligible and the idle frequency is the same as for an ideal integrator, thus $F_{osc} = \frac{1}{4\tau} = 1Hz$. On the other side, when $\frac{\tau}{T_p}$ is higher than 10×10^4, the frequency reaches it's maximum at $F_{osc} = \frac{1}{2\tau} = 2Hz$. At this frequency, however, as is intuitive, no modulation occurs, since the dithering signal is the square wave directly from the relay's output.

B.2 Quasi-static input-to-output characteristic

Since the purpose of this system is to translate a quasi-static input to the output in the form of a DC component, it is important to calculate the relation between both. Since the

first-order filter is supposed to be linear, and it is a low-pass filter, the output mean-value is the same as the rectangle-wave mean value.

Recalling the Figure B.2, one can see that the output mean-value is given by

$$\widehat{V_o} = F_{osc} \cdot L(T_2 - T_1)$$

Since for practical purposes $\tau \ll T_p$ (in order to keep ripple low, and make the dithering shape assemble a triangle wave due to the near-pure-integrator behaviour of the low-pass filter) the exponential functions may be approximated, making $\exp x \approx 1 + x$ and $ln(x) \approx x - 1$. From these assumptions, (B.2) and (B.3) can be further simplified, yielding

$$T_1 \approx \frac{\tau(L - V_{in})}{L + V_{in}} \tag{B.6}$$

$$T_2 \approx \frac{\tau(L + V_{in})}{L - V_{in}} \tag{B.7}$$

Turning F_{osc} and $T_2 - T_1$ into

$$F_{osc} = \frac{1}{2\tau + T1 + T2} \approx \frac{L^2 - V_{in}^2}{4\tau L^2} \tag{B.8}$$

$$T_2 - T_1 \approx \frac{\tau \cdot 4LV_{in}}{L^2 - V_{in}^2}$$

Calculating $\widehat{V_o}$ from these expressions leads to

$$\widehat{V_o} \approx \frac{L \cdot (L^2 - V_{in}^2)}{4\tau L^2} \cdot \frac{\tau \cdot 4LV_{in}}{L^2 - V_{in}^2} = V_{in} \quad , \tau \ll T_p \tag{B.9}$$

Which shows that when $\tau \ll T_p$ the output is equal to the input.

Appendix C

Details about the derivation of Oscillation Condition

C.1 Development of Mathematical expressions of Section 3

This appendix is meant to show the intermediate algebraic manipulations of Section 3.

Firstly, to obtain (3.5), the square wave previously described should be transformed to the frequency domain. Lets call $\hat{V}_c(f)$ the frequency domain transform of $V_c(t)$.

$$\hat{V}_c(f) = \frac{1}{T}\int_0^T V_c(t)e^{-2\pi jft}\,dt$$

where T is the period of the wave. From the definition of $V_c(t)$ in (3.2), which shall be replicated here for convenience, the integral can be expanded:

$$V_c(t) = \begin{cases} 1 & \text{for } t \in [0+kT, DT+kT], k \in \mathbb{Z} \\ -1 & \text{for } t \in (DT+k, T+kT), k \in \mathbb{Z} \end{cases}$$

Thus, the integral results in

$$\hat{V}_c(f) = \frac{1}{T}\left(\left[\frac{1}{-2\pi jf}e^{-2\pi jft}\right]_0^{DT} - \left[\frac{1}{-2\pi jf}e^{-2\pi jft}\right]_{DT}^{T}\right)$$

$[\bullet(t)]_B^A$ is a notation for $(\bullet(A) - \bullet(B))$. Expanding yields

$$\hat{V}_c(f) = \frac{1}{-2\pi jfT}\left[\left(e^{-2\pi jfDT} - 1\right) - \left(e^{-2\pi jfT} - e^{-2\pi jfDT}\right)\right]$$

Since $V_c(T)$ is periodic over T, f only takes discrete values in the form $f = \frac{n}{T}, \quad n \in \mathbb{Z}$, thus, the expression can be further simplified to

$$\hat{V}_c(n) = \frac{1}{-2\pi jn}\left[\left(e^{-2\pi jnD} - 1\right) - \left(1 - e^{-2\pi jnD}\right)\right], \quad n \neq 0 \tag{C.1}$$

$$\hat{V}_c(0) = 2D - 1, \quad n = 0 \tag{C.2}$$

simplifying only for $n \neq 0$ yields

$$\hat{V}_c(n) = \frac{1}{-2\pi jn}\left[e^{-\pi jnD}\left(e^{-\pi jnD} - e^{\pi jnD}\right) - e^{-\pi jnD}\left(e^{\pi jnD} - e^{-1\pi jnD}\right)\right], \quad n \neq 0$$

since $\left(e^{\pm\pi jnD} - e^{\mp 1\pi jnD}\right)$ yields $\pm 2jsin(\pi nD)$, the expression turns into

$$\hat{V}_c(n) = \frac{1}{-2\pi jn}\left(-4jsin(\pi nD)e^{-\pi jnD}\right), \quad n \neq 0$$

$$\hat{V}_c(n) = \frac{2sin(\pi nD)}{\pi n}e^{-\pi jnD}$$

thus, transforming back to time-domain, the final expression is obtained simply from the integral

$$V_c(t) = \int_{-\infty}^{+\infty} \hat{V}_c(n)\delta(f - \frac{n}{T})e2\pi jft, df$$

where $\delta(x)$ is the well known Dirac-Delta function.

$$V_c(t) = (2D - 1) + \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} \hat{V}_c(n)e^{2\pi j\frac{n}{T}t}$$

Appendix D

Component list of the prototype

Here is the list of the main components used in the prototype.

Component Identifier	Component Description	Component Reference
IC1	LT: Micropower Low Dropout Regulators	LT1129CST-5
IC2	LT: 55V, 1.2A Step-Down Regulator	LT3991EMSE
IC3	LT: LDO Negative Micropower Regulator	LT1964ES5-SD
D1	NXP: 0.5A very low VF Schottky barrier rectifier	PMEG4005EH
L1	Bourns: Shielded SMD Power Inductor	SRU5018-100Y

Table D.1: List of main components used in the power-supply.

Component Identifier	Component Description	Component Reference
LMH7220	National: High Speed Comparator with LVDS Output	LMH7220
T[1-4]	NXP: Fast 40 V, 500 mA NPN transistor	PBSS2540E
D1	NXP: 0.5A very low VF Schottky rectifier	PMEG4005EH
D[2-3]	NXP: 0.5A very low VF Schottky rectifier (small)	PMEG4005EJ
EL1755	Intersil: High Performance Pin Driver	EL1755
Q1	Diodes.inc: N-channel enhacement-mode MOSFET	ZXMN10A11G
L1	Bourns: Shielded SMD Power Inductor	SRU5018-100Y

Table D.2: List of main components used in the circuit.

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