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Synchronous and Asynchronous Sequential Symbol Synchronizers

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Abstract

In this work, we present two synchronizer groups: the synchronous and the asynchronous.

The synchronous group is based in forward logic with flip flops and the asynchronous group is based in forward logic with delay line feedback.

In each group we consider two versions: the manual and the automatic.

The main objective is to study the two groups, each one with two versions and to observe its jitter performance as function of the noise.

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

The final system quality depends strongly of the synchronizer performance [1, 2, 3, 4, 5, 6, 7, 8, 9].
The synchronizer samples the data at the optimum point and retimes the bit duration [10, 11, 12, 13, 14, 15, 16].

There is a great variety of synchronizers, but here we go present a prototype based on the comparison between a variable pulse area Pv and a fixed pulse area Pf. The area difference Pr is the error signal, that corrects the position of the VCO (Voltage Controlled Oscillator) toward the optimum point. This point is the maximum opening eye diagram and corresponds normally to the bit center.

The following figure (Fig.1) shows the configuration of the synchronizer based in pulses area comparison.

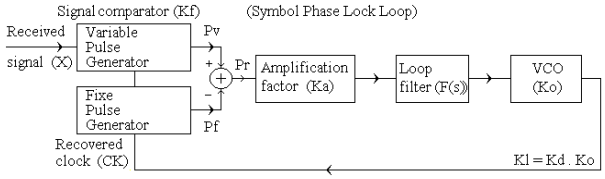

Fig.1 Configuration of the synchronizer based on two pulses (Pv,Pf)

The Kf is the signal (phase / frequency) comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the control parameter of the loop gain, that acts in the locus root providing the desired characteristics.

We will implement the above blocks based in two different technologies originating two distinct groups which are the synchronous and the asynchronous. The synchronous is based in logic with flip flops and the asynchronous is based in logic with feedback.

The following figure (Fig.2) illustrates the basic difference between a synchronous and asynchronous system.

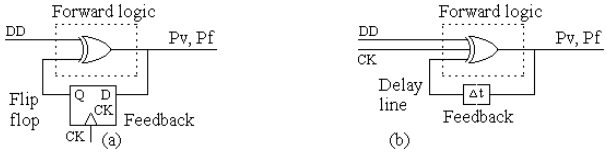

Fig.2 Aspect of the synchronous (a) and asynchronous (b) type

Each group has two versions, which are the manual and the automatic.

In the manual version, the fixed pulse generation is based in a delay line that needs human adjusting. Oppositly, in the automatic version the fixed pulse generation is based in a flip flop dispensing the human adjusting.

The following figure (Fig.3) illustrates the basic difference between the manual and automatic versions.

Fig.3 Aspect of the manual (a) and automatic (b) version

Next, we present separately, the two groups of synchronizers, firstly the synchronous synchronizers and after the asynchronous synchronizers. Each group has two versions which are the manual and automatic.

After, we test the two groups with their two versions manual and automatic.

Then, we present the results and we make some comparisons.

Finally, we present some conclusions.

II. SYNCHRONOUS SYNCHRONIZERS

We begin presenting the synchronous synchronizer based on flip flops with logic. We distinguish the manual and the automatic versions [1, 2, 3, 4].

Fig.4 shows the synchronous type manual version

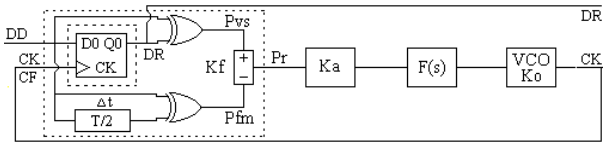

Fig.4 Manual synchronous symbol synchronizer (tx1sm)

The manual version is based on the comparation between the phase comparator Pvs and manual reference pulse Pfm.

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Fig.5 shows the synchronous type automatic version

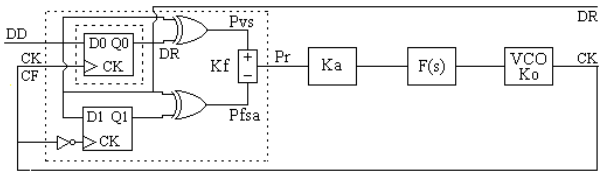

Fig.5 Automatic synchronous symbol synchronizer (tx1sa)

The automatic version is based on the comparation between the phase comparator Pvs and the automatic reference pulse Pfsa.

III. ASYNCHRONOUS SYNCHRONIZERS

Now, we present the asynchronous synchronizers based on logic with delay line feedback. We distinguish the manual and the automatic versions [6, 7, 8, 9, 10].

Fig.6 shows the asynchronous type manual version.

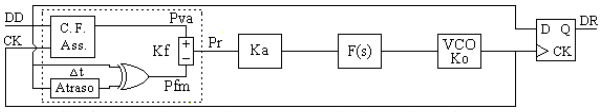

Fig.6 Manual asynchronous symbol synchronizer (tx1am)

The manual version is based on the comparation between the asynchronous phase comparator Pva and the manual reference pulse Pfm.

Fig.7 shows the asynchronous type automatic version.

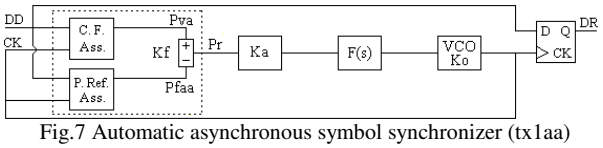

Fig.7 Automatic asynchronous symbol synchronizer (tx1aa)

The automatic version is based on the comparation between the asynchronous phase comparator Pva and the automatic reference pulse Pfaa.

Fig.8 shows the implementation of the asynchronous phase comparator Pva.

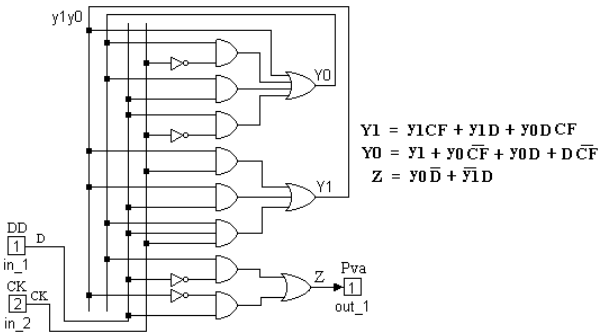

Fig.8 Aspect of the asynchronous variable pulse generator

Fig.9 shows the implementation of the asynchronous reference pulse Pfaa.

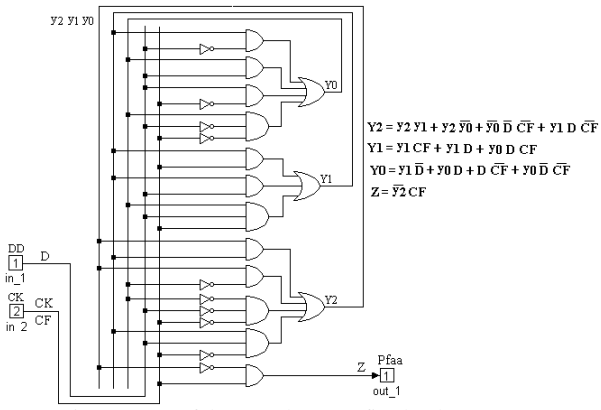

Fig.9 Aspect of the asynchronous fixed pulse generator

This asynchronous phase comparator and reference pulse was projected by asynchronous methods.

IV. TESTS, DESIGN AND RESULTS

We will present the tests, the design and the results of the referred synchronizers [5].

A. Tests

The following figure (Fig.10) shows the setup that was used to test the various synchronizers.

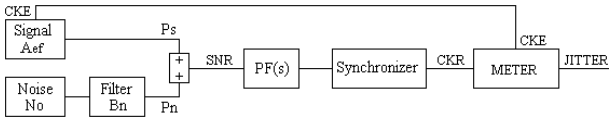

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

B. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE).

This relative random phase variation is the recovered clock jitter (Fig.11).

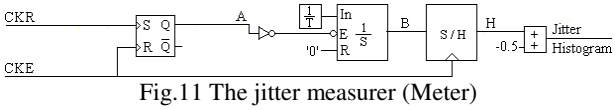

Fig.11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

C. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the amplification control factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal to noise ratio SNR related with the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so it is SNR = $A^2_{ef}/(No.Bn)$. But No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for analog synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)
$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi$ (3)

For hybrid synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)
$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi$ (4)

For combinational synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)
$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04$ (5)

For sequential synchronizers (present case), the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)
$(Ka*1/2\pi*2\pi)/4 =0.02 \rightarrow Ka=0.08$ (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.
For analog PLL the jitter is
$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$
For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

D. Results

We present, the synchronizers jitter behavior as function of the noise.

Fig. 12 shows the jitter - noise curves of the four synchronizers (tx1sm, tx1sa, tx1am, tx1aa).

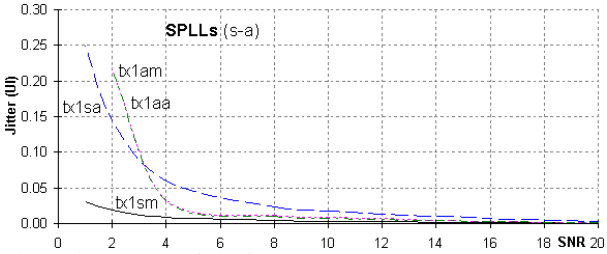

Fig.12 Jitter curves of the four SPLLs (tx1sm, tx1sa, tx1am, tx1aa)

We note that generically in all the synchronizers the jitter UIRMS diminishes when the signal to noise ratio SNR increases.

We verify that the manual synchronous is always the best case for all SNR. For SNR>3 when all synchronizers are in lock, the automatic synchronous is the worst case and the two asynchronous prototypes have intermedium similar behavior. For SNR<3 the asynchronous prototypes lost the lock, causing a great increment of the jitter.

V. CONCLUSIONS

We studied four Sequential Symbol Synchronizers (tx1sm, tx1sa, tx1am, tx1aa).

The results show that the synchronous prototypes have different behavior but the asynchronous have equal behavior.

For SNR>3 with all synchronizers in perfect lock the manual synchronous is the best case and the automatic synchronous the worst case. The asynchronous prototypes have an intermediate behavior. For SNR<3 the two asynchronous prototypes, begin with synchronism problems and the jitter increases suddenly. This is caused by noise that passes through the gates and provokes races in the circuits.
This is comprehensible since the output jitter depends on the input noise and the error state of the phase comparator.
In the synchronous manual only the phase comparator is sequential (memory) and has contribution to error state, the reference pulse is combinational.

In the synchronous automatic, the phase comparator is sequential causing error state, the reference pulse is also sequential causing error state and there is still the error propagation effect from the first to the second.

In the asynchronous manual and automatic cases, the phase comparator and reference pulse are projected independently. Then each one has its own error state, but is avoid the error propagation from the first to the second. Then this results in an intermedium jitter behavior. The phase comparator is more opened to the noise than the reference pulse, then its effect is predominant and the jiiter is equal in the two cases.

VI. ACKNOWLEDGMENTS

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