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Deterministic and Random Phase Synchronizers

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Abstract

This work study two groups of synchronizers, namely the Deterministic Phase Synchronizer and the Random Phase Synchronizer. The difference between them is only inside of the phase comparator.

In the first group, the VCO (Voltage Controlled Oscillator) synchronizes with the input deterministic phase of an expected periodic transition. In the second group the VCO synchronizes with the input random phase of an unexpected no periodic transition.

Each group is studied under four topologies (analog, hybrid, combinational and sequential).

The objective is to evaluate the two synchronizers groups with the four topologies and to observe their jitter behaviors with the noise.

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

The synchronizer recoveries the clock that is used to sample the data at the optimum point and retimes the bit duration of the data [1, 2, 3, 4, 5, 6, 7, 8, 9].

Basically, the synchronizer consists on a VCO, that is able to follow the phase and frequency of the input signal. This input signal can be a deterministic signal or a random signal.

This work study two groups of synchronizers, namely the deterministic phase synchronizers and the random phase synchronizers [10, 11, 12, 13, 14, 15, 16, 17].

In the first group, the phase comparator compares the VCO periodic phase with the input deterministic phase of a periodic signal (deterministic regular wave). In the second group, the phase comparator compares the VCO periodic phase with the input random phase of a no periodic signal (random irregular data sequence).

Each group has four topologies, which are the analog, the hybrid, the combinational and the sequential.

Fig.1 shows the block diagram of the general synchronizer.

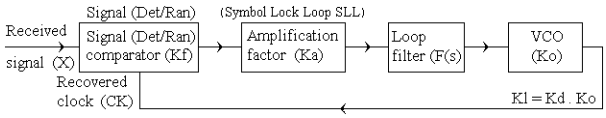

Fig.1 General deterministic or random synchronizer

F(s) is the loop filter, Ko is the VCO gain, Kf is the phase comparator gain and Ka is the amplification gain that acts in the locus root determining the desired characteristics.

Next, we present separately the two synchronizers groups, beginning with the deterministic group and after the random group. Each group has four types, namely the analog, the hybrid, the combinational and the sequential.

After, we test the four types of each group with a signal corrupted by noise.

Then, we present the results and with some comparisons.

Finally, we present the conclusions.

II. DETERMINISTIC PHASE SYNCHRONIZERS

In this synchronizers group, the periodic VCO synchronizes with an input deterministic signal which is a periodic regular wave. Depending on the deterministic phase comparator block, since the other blocks are equal, we will consider four synchronizer types which are the analog, the hybrid, the combinational and the sequential [1, 2].

Fig.2 shows the analog type, whose phase comparator is based on the analog ideal switch (multiplier).

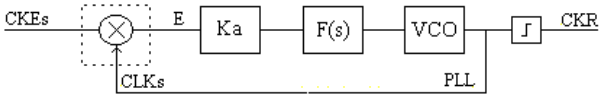

Fig.2 Analog deterministic phase synchronizer

The two inputs at the phase comparator are both analog, so we have the analog type (full-analog). So we have the analog deterministic phase synchronizer.

This deterministic phase comparator is a device without memory because the ideal multiplier is an analog component without memory.

Fig.3 shows the hybrid type, whose phase comparator is based on an hybrid real switch.

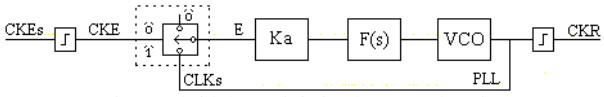

Fig.3 Hybrid deterministic phase synchronizer

The entered input is digital and the entered VCO is analog so we have the hybrid type (semi-analog). So we have the hybrid deterministic phase synchronizer.

This deterministic phase comparator is a device without memory because the real switch is an hybrid component without memory.

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Fig.4 shows the combinational type, whose phase comparator is based on an exor gate.

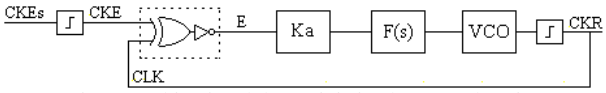

Fig.4 Combinational deterministic phase synchronizer

The two inputs at the phase comparator are both digital, the phase comparator output is only function of the inputs. So we have the combinational (digital combinational) deterministic phase synchronizer.

This deterministic phase comparator is a device without memory because the exor gate is a combinational component without memory.

Fig.5 shows the sequential type, whose phase comparator is based on a flip flop.

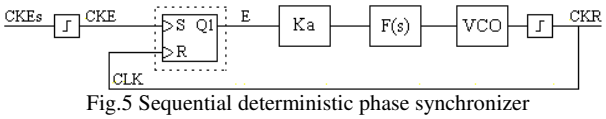

Fig.5 Sequential deterministic phase synchronizer

The two inputs at the phase comparator are both digital and the phase comparator output is simultaneously function of the inputs and its state. So we have the sequential (digital sequential) deterministic phase synchronizer.

This deterministic phase comparator is a device with memory because the flip flop is a sequential component with memory.

III. RANDOM PHASE SYNCHRONIZERS

In this synchronizers group, the periodic VCO synchronizes with an input random signal which is a no periodic irregular data sequence. Depending on the random phase comparator block, since the other blocks are equal, we will consider four synchronizer types which are the analog, the hybrid, the combinational and the sequential [3, 4].

Fig.6 shows the analog type, whose phase comparator is based on analog ideal switches.

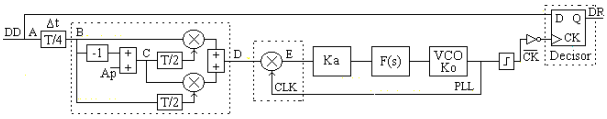

Fig.6 Analog random phase synchronizer

The two inputs at the random phase comparator are both analog, so we have the analog type (full-analog). So we have the analog random phase synchronizer.

This random phase comparator is a device without memory because the ideal multiplier is an analog component without memory.

Fig.7 shows the hybrid type, whose phase comparator is based on an hybrid real switch.

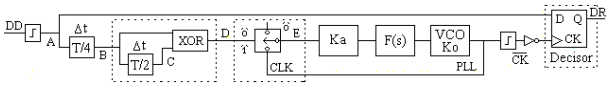

Fig.7 Hybrid random phase synchronizer

The entered input is digital and the entered VCO is analog so we have the hybrid type (semi-analog). So we have the hybrid random phase synchronizer.

This random phase comparator is a device without memory because the real switch is an hybrid component without memory.

Fig.8 shows the combinational type, whose phase comparator is based on an exor gate.

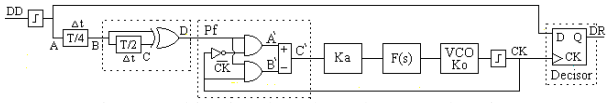

Fig.8 Combinational random phase synchronizer

The two inputs at the phase comparator are both digital, the phase comparator output is only function of the inputs. So we have the combinational (digital combinational) random phase synchronizer.

This random phase comparator is a device without memory because the exor gate is a combinational component without memory.

Fig.9 shows the sequential type, whose phase comparator is based on a flip flop and additional logic gates.

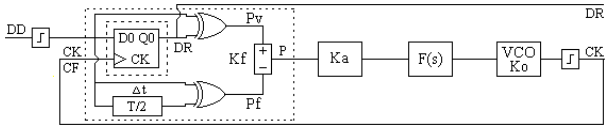

Fig.9 Sequential random phase synchronizer

The two inputs at the phase comparator are both digital and the phase comparator output is simultaneously function of the inputs and its state. So we have the sequential (digital sequential) random phase synchronizer.

This random phase comparator is a device with memory because the flip flop is a sequential component with memory.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [6].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)

$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi$ (3)

For the hybrid synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)

$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi$ (4)

For the combinational synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)

$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04$ (5)

For the sequential synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)

$(Ka*1/2\pi*2\pi)/4 =0.02 \rightarrow Ka=0.08$ (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For analog PLL the jitter is

$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

The following figure (Fig.10) shows the setup that was used to test the various synchronizers.

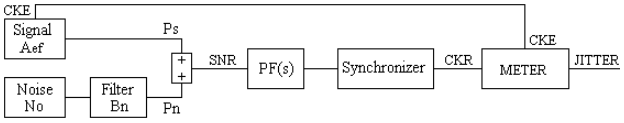

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

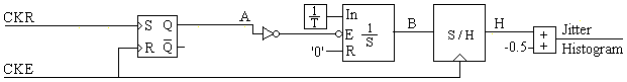

Fig.11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram. Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present separately the results of the two synchronizer groups beginning with the deterministic group and after the random group.

First, we show the curves of the jitter UI-RMS (Unit Interval Root Mean Square) as function of the signal-noise SNR (Signal to noise ratio) for the deterministic group, considering its four types: analog (ana-d), hybrid (hib-d), combinational (cmb-d) and sequential (seq-d) (Fig.12).

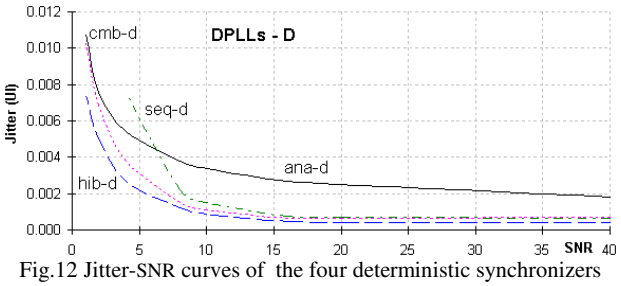

Fig.12 Jitter-SNR curves of the four deterministic synchronizers (a,h,c,s)

We verify, that for high SNR, the synchronizers without input limiter (ana) is disadvantageous over the others with input limiter (hib, cmb, seq). However for low SNR the synchronizer with intern memory (seq) is slightly disadvantageous on the others without intern memory (ana, hib, cmb). This disadvantage can be minimized with a prefilter.

After, we show the jitter-SNR curves of the random synchronizer group considering its four types: the analog (ana-r), the hybrid (hib-r), the combinational (cmb-r) and the sequential (seq-r) (Fig.13).

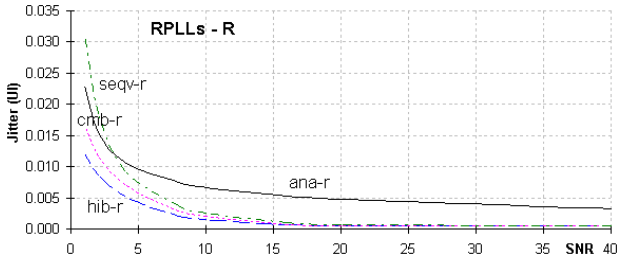

Fig.13 Jitter-SNR curves of the four random synchronizers (a,h,c,s)

We verify that for high SNR the synchronizers without input limiter (ana) is disadvantageous over the others with input limiter (hib, cmb, seq). However, for low SNR the synchronizer with intern memory (seq) is slightly disadvantageous over the others without intern memory (ana, hib, cmb). This disadvantage can be minimized with a prefilter.

V. CONCLUSIONS

We studied two synchronizers groups, which are the deterministic phase synchronizers and the random phase synchronizers, according to their phase comparator.

Each group has four types: the analog (ana), the hybrid (hib), the combinational (cmb) and the sequential (seq).

We verify that for high SNR, the synchronizer without input limiter (ana) is disadvantageous over the others with input limiter (hib, cmb, seq). This is comprehensible, because the limiter noise margin ignores low noise spikes.

However, for low SNR the synchronizers without input limiter (ana) becomes advantageous over the others with input limiter (hib, cmb, seq). This is comprehensible since the limiter provokes random gate commutations spikes. In the sequential type, this spikes cause also random state transitions which increases slightly the jitter. Anyway this last disadvantage can be minimized with a prefilter. However, the sequential type, due to its intern memory, has particular potentialities to provide automatic versions and frequency operation at submultiples of the transmission rate.

VI. ACKNOWLEDGMENTS

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