Effects of the Previous Pulse Shift and Filter on the Symbol Synchronizer PLL

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Abstract

We will study the effects of the shift of the previous pulse temporal position (between P1 and P2) on the symbol synchronizers jitter behavior.

Each pulse temporal position (P1 and P2), with the same previous filter, forms a group with four different carrier PLL (Phase Lock Loop) namely the analog, hybrid, combinational and sequential.

The main objective is to study the synchronizers output jitter UIRMS (Unit Interval Root Mean Squared) as function of the input SNR (Signal to Noise Ratio).

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

This work study the shift effects of the previous pulse temporal position on the jitter of two synchronizers groups.

When occurs a positive data transition, for sequences '1' and '0' alternated, is produced two types of pulses P1 or P2, each one with half period duration T/2.

The pulse P1 (duration T/2) begins in the positive data transition delayed half period and finishes in the next negative data transition [1, 2, 3, 4, 5, 6, 7, 8, 9, 10].

The pulse P2 (duration T/2) begins in the positive data transition and finishes in the positive data transition delayed half period [11, 12, 13, 14].

These pulses (P1 or P2) increases the energy at the transmission rate and excites the tuned filter (tank circuit) that selects the fundamental harmonic that is equal to the transmission rate. This harmonic of poor quality is improved by the carrier PLL (CPLL) in a VCO of high quality. Each pulse P1 or P2 and filter is followed of four CPLL types, namely the analog, hybrid, combinational and sequential.

Fig.1 shows the aspect of the symbol synchronizer based on the pulse and filter followed of the PLL.

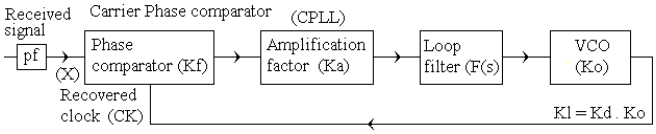

Fig.1 Aspect of the synchronizer based on filter with CPLL

Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification factor that controls the root locus and the loop desired characteristics.

Following, we present the production of the two previous pulse generators P1 and P2 and respective waveforms.

After, we present the pulse generator P1 followed of filter with the four PLL types (analog, hybrid, combinational and sequential).

Next, we present the pulse generator P2 followed of filter with the four PLL types (analog, hybrid, combinational and sequential).

Then, we present the design and tests of the synchronizers.

After, we present the results.

Finally, we present the conclusions.

II. TWO PREVIOUS PULSE GENERATORS P1 AND P2

When a positive data transition occurs in a data sequence of '1' and '0' alternated, we choose two processes to generate the previous pulse of half period (T/2). This pulse passes through the filter that selects the fundamental harmonic of the data rate (Fig.2).

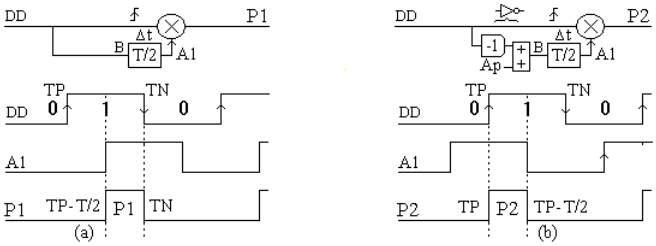

Fig.2 Previous pulse P1 (a) and previous pulse P2 (b)

In the first case the pulse P1 begins in the positive data transition delayed T/2 and finishes in the next negative data transition (Fig.2a).

In the second case, the pulse P2 begins in the positive data transition and finishes in the positive data transition delayed of T/2 (Fig.2b).

The difference between the two groups is in the pulse generator P1 or P2.

Then each one of the two pulse generators P1 or P2 is followed of filter with the four CPLL types. The CPLL types are the analog, hybrid, combinational and sequential.

III. PULSE P1 AND FILTER WITH THE FOUR CPLL

This group involves the pulse generator P1 and filter with the four CPLL types, namely the analog, the hybrid, the combinational and the sequential [3, 4].

The difference between the four CPLL types is inside of the phase comparator. The filter F(s) and VCO (Voltage Controlled Oscillator) are equal for all synchronizers.

A. Pulse P1 and filter with analog CPLL

The synchronizer consists of the pulse generator P1 and filter with the analog CPLL. The analog phase comparator is based on the ideal multiplier (Fig.3).

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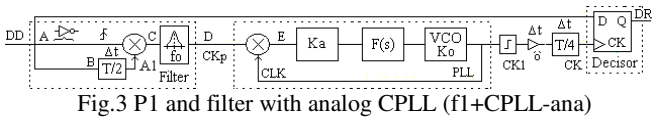

Fig.3 P1 and filter with analog CPLL (f1+CPLL-ana)

This carrier phase comparator inputs (main input and VCO output) are both analog (full-analog). The output is function of the inputs.

B. Pulse P1 and filter with hybrid CPLL

The synchronizer consists of the pulse generator P1 and filter with the hybrid CPLL. The hybrid phase comparator is based on the switch (Fig.4).

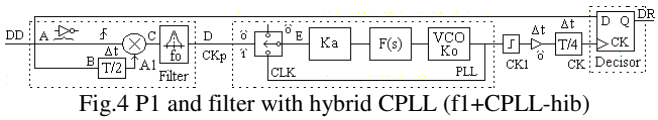

Fig.4 P1 and filter with hybrid CPLL (f1+CPLL-hib)

The carrier phase comparator main input is digital but the input from VCO output is still analog (semi-analog). The output is function of the inputs.

C. Pulse P1 and filter with combinational CPLL

The synchronizer consists of the pulse generator P1 and filter with the combinational CPLL. The combinational phase comparator is based on the exor gate (Fig.5).

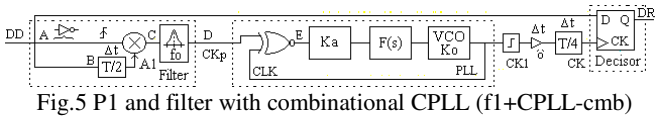

Fig.5 P1 and filter with combinational CPLL (f1+CPLL-cmb)

The carrier phase comparator inputs (main input and VCO output) are both digital. The output is only function of the inputs (without intern memory).

D. Pulse P1 and filter with sequential CPLL

The synchronizer consists of the pulse generator P1 and filter with the sequential CPLL. The sequential phase comparator is based on the flip flop (Fig.6).

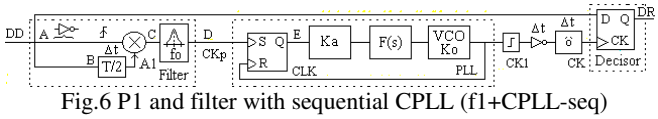

Fig.6 P1 and filter with sequential CPLL (f1+CPLL-seq)

This carrier phase comparator inputs (main input and VCO output) are both digital. The output is simultaneously function of the inputs and of its state (with intern memory).

IV. PULSE P2 AND FILTER WITH THE FOUR CPLL

This group involves the pulse generator P2 and filter with the four PLL types, namely the analog, the hybrid, the combinational and the sequential. [3, 4].

The difference between the four PLL types is inside of the phase comparator.

A. Pulse P2 and filter with analog CPLL

The synchronizer consists of the pulse generator P2 and filter with the analog CPLL. The analog phase comparator is based on the ideal multiplier (Fig.7).

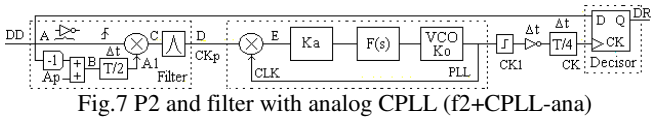

Fig.7 P2 and filter with analog CPLL (f2+CPLL-ana)

This carrier phase comparator inputs (main input and VCO output) are both analog (full-analog). The output is function of the inputs.

B. Pulse P2 and filter with hybrid CPLL

The synchronizer consists of the pulse generator P1 and filter with the hybrid CPLL. The hybrid phase comparator is based on the switch (Fig.8).

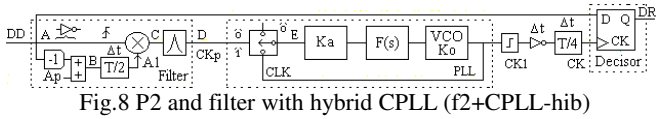

Fig.8 P2 and filter with hybrid CPLL (f2+CPLL-hib)

The carrier phase comparator main input is digital but the input from VCO output is still analog (semi-analog). The output is function of the inputs.

C. Pulse P2 and filter with combinational CPLL

The synchronizer consists of the pulse generator P1 and filter with the combinational CPLL. The combinational phase comparator is based on the exor gate (Fig.9).

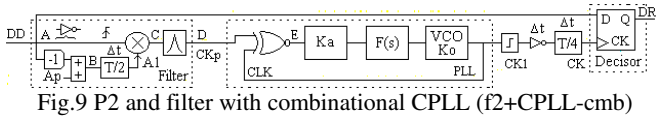

Fig.9 P2 and filter with combinational CPLL (f2+CPLL-cmb)

The carrier phase comparator inputs (main input and VCO output) are both digital. The output is only function of the inputs (without intern memory).

D. Pulse P2 and filter with sequential CPLL

The synchronizer consists of the pulse generator P1 and filter with the sequential CPLL. The sequential phase comparator is based on the flip flop (Fig.10).

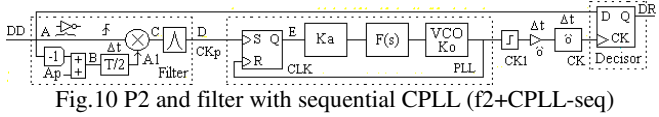

Fig.10 P2 and filter with sequential CPLL (f2+CPLL-seq)

This carrier phase comparator inputs (main input and VCO output) are both digital. The output is simultaneously function of the inputs and of its state (with intern memory).

V. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [6].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)

$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi$ (3)

For the hybrid synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)

$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi$ (4)

For the combinational synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)

$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04$ (5)

For the sequential synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)

$(Ka*1/2\pi*2\pi)/4 =0.02 \rightarrow Ka=0.08$ (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For analog PLL the jitter is

$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

The following figure (Fig.11) shows the setup that was used to test the various synchronizers.

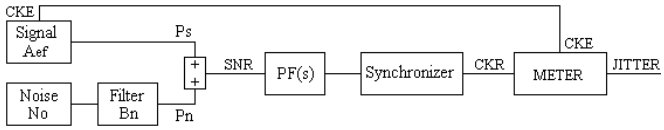

Fig.11 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.12).

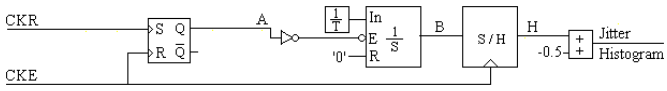

Fig.12 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram. Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present separately the results (output jitter UIRMS versus input SNR) for the P1 and P2 synchronizers groups.

Fig.13 shows the jitter-SNR curves of the first group P1 and filter with its four PLL types: analog CPLL (f1+CPLL-ana), hybrid CPLL (f1+CPLL-hib), combinational CPLL (f1+CPLL-cmb), sequential CPLL (f1+CPLL-seq).

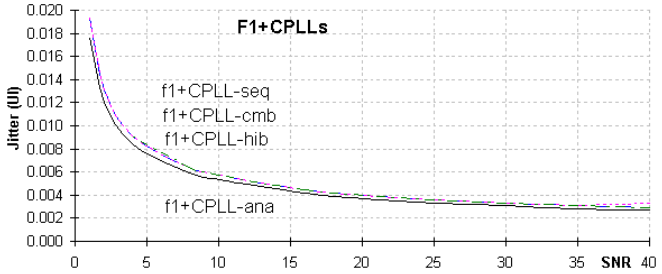

Fig.13 Jitter-SNR curves of the P1 with the four CPLLs (a,h,c,s)

We verify, that the jitter diminishes with the SNR increasing. The previous filter is determinative over the CPLLs and then the four symbol synchronizers have similar jitter-SNR curves.

Fig.14 shows the jitter-SNR curves of the second group P2 and filter with its four PLL types: analog CPLL (f2+CPLL-ana), hybrid CPLL (f2+CPLL-hib), combinational CPLL (f2+CPLL-cmb), sequential CPLL (f2+CPLL-seq).

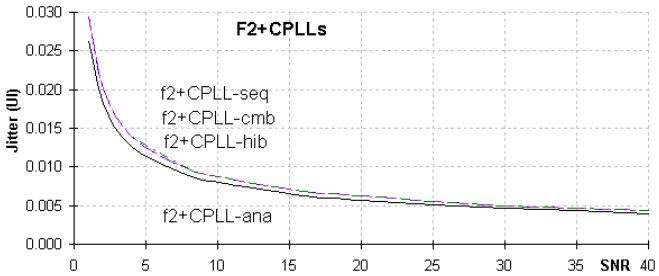

Fig.14 Jitter-SNR curves of the P2 with the four CPLLs (a,h,c,s)

We verify, that the jitter diminishes with the SNR increasing. The previous filter is determinative over the CPLLs and then the four symbol synchronizers have similar jitter-SNR curves. Also the 1st and 2nd groups are similar.

VI. CONCLUSIONS

We studied two symbol synchronizers groups, one based in the pulse P1 and the other based in the pulse P2.

In the first group P1 and filter, we considered four CPLL types (f1+CPLL-ana, f1+CPLL-hib, f1+CPLL-cmb, f1+CPLL-seq). In the second group P2 and filter, we considered also the same four CPLL types (f2+CPLL-ana, f2+CPLL-hib, f2+CPLL-cmb), f2+CPLL-seq).

We noted, that in the 1st group the previous filter is determinative and for this reason all the four symbol synchronizers present similar jitter-SNR curves. Also, in the 2nd group the previous filter is determinative and for this reason all the four symbol synchronizers present similar jitter-SNR curves.

We concluded, that this similarity of eight synchronizers is comprehensible since the previous filter is determinative and the subsequent CPLL types improve equally the quality.

VII. ACKNOWLEDGMENTS

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