Prefilter Bandwidth Effects in Sequential Symbol Synchronizers based on Clock Sampling by Positive Transitions

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Abstract - **This work studies the effects of the prefilter bandwidth in the sequential symbol synchronizers based on clock sampling by positive transitions.**

The prefilter bandwidth B is switched between three values, namely B1=∞, B2=2.tx and B3=1.tx, where tx is the bit rate. The synchronizer has two variants, one discrete and other continuous. Each variant has two versions, one manual and other automatic.

The objective is to study the prefilter bandwidth with the four synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).

Key words: **Prefilter, Digital Communication Systems**

I. INTRODUCTION

This work studies the effects of three prefilter bandwidths in the jitter-SNR curves of four sequential symbol synchronizers [1, 2, 3, 4, 5, 6].

The Butterworth prefilter, applied before the synchronizer, varies its bandwidth between three different values, namely first B1=∞, after B2=2.tx and next B3=1.tx.

The symbol synchronizer has a phase comparator based on clock sampling by positive transitions. The synchronizer has two variants, one discrete with two versions namely the manual (d-m) and the automatic (d-a) and other continuous with two versions namely the manual (c-m) and the automatic (c-a) [7, 8, 9, 10, 11, 12].

The difference between the four synchronizers is only in the phase comparator since the other blocks are equals.

The VCO (Voltage controlled oscillator) is the clock, whose performance determines, in great part, the system quality.

Fig.1 shows the prefilter followed of the synchronizer.

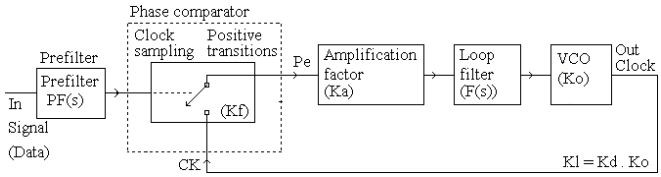

Fig.1 Prefilter with the symbol phase synchronizer

PF(s) is the prefilter. The synchronizer has various blocks, namely Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification factor that controls the root locus and loop characteristics.

In prior and actual -art state was developed various synchronizers, but it is necessary to know their performance.

The motivation of this work is to create new synchronizers and evaluate their performance with noise. This contribution increases the know how about synchronizers.

Following, we present the prefilter with their three different bandwidths (B1=∞, B2=2.tx, B3=1.tx).

After, we present the variant discrete with their versions manual (d-m) and automatic (d-a). Next, we present the variant continuous with their versions manual (c-m) and automatic (c-a).

After, we present the design and tests. Then, we show the results with comparisons. Finally, we show the conclusions.

II. PREFILTER BANDWIDTH EFFECTS

We apply a prefilter before the synchronizer, we change its bandwidth B between three values (B1=∞, B2=2.tx, B3=1.tx), then we study the effects on the four jitter-SNR curves. Fig.2 shows the prefilter with the three bandwidths.

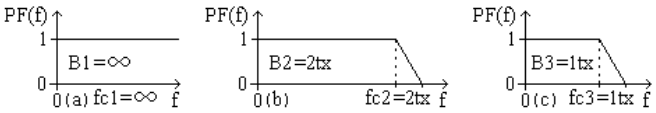

Fig.2 Three prefilter bandwidths: a) B1=∞; b) B2=2.tx; c) B3=1.tx

Following, we will describe each one of the three prefilter bandwidths (B1=∞, B2=2.tx, B3=1.tx).

A. Prefilter with Bandwidth equal infinite (B1=∞)

This prefilter (Fig.2a) means a bandwidth equal infinite (B=∞). We will see this bandwidth effects on the four synchronizers (ana, hib, cmb, seq).

B. Prefilter with Bandwidth equal two tx (B2=2.tx)

This prefilter (Fig.2b) means a bandwidth equal two times the transmission rate (B=2.tx). We will see this bandwidth effects on the four synchronizers (ana, hib, cmb, seq).

C. Prefilter with Bandwidth equal one tx (B3=1.tx)

This prefilter (Fig.2c) means a bandwidth equal one time the transmission rate (B=1.tx). We will see this bandwidth effects on the four synchronizers (ana, hib, cmb, seq).

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II. DISCRETE SYNCHRONIZER TOPOLOGIES

The discrete topology has a pulse error Pe that advances discreetly until the equilibrium point, without to disappear. This topology has the following manual and automatic versions [1, 2].

A. Discrete topology and manual version

The manual version is based on a delay line that needs a previous human adjustment to produce Pf. This delay isn't critical, but only determines the charge pulse area Pf (Fig.3).

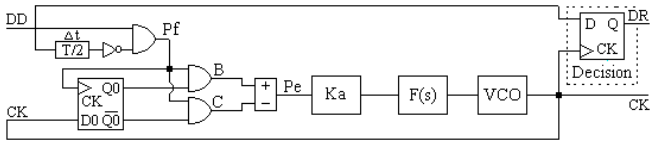

Fig.3 Synchronizer discrete and manual (d-m)

The delay T/2, NOT with 1st AND produces a fixed area pulse Pf that determines the charge rhythm.

B. Discrete topology and automatic version

The automatic version is based on a flip flop that automatically provides the delay and variable pulse Pv. This delay determines the charge pulse area Pv (Fig.4).

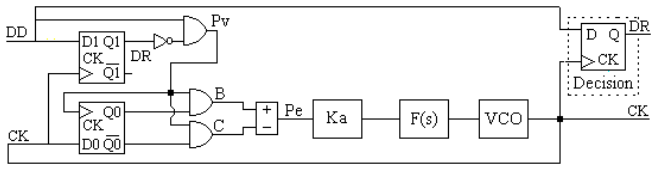

Fig.4 Synchronizer discrete and automatic (d-a)

The flip flop 1, NOT with 1st AND produces a variable pulse Pv that determines the charge rhythm.

III. CONTINUOUS SYNCHRONIZER TOPOLOGIES

The continuous topology has a pulse error that advances continuously to the equilibrium point, can change its direction and disappear. This topology has the following manual and automatic versions [3, 4].

A. Continuous topology and manual version

The manual version is based on a delay line that needs a previous human adjustment to produce the fixed pulse Pf.. This delay isn't critical, but only determines the initial charge pulse area A (Fig.5).

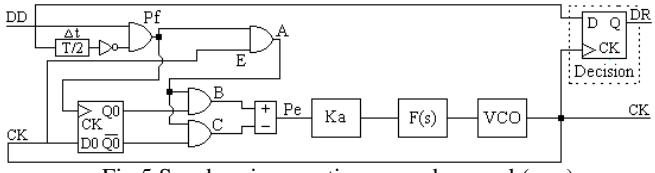

Fig.5 Synchronizer continuous and manual (c-m)

The delay T/2, NOT with the 1st AND produces the fixed pulse Pf and the 2nd AND produces the variable pulse A that determines the charge rhythm.

B. Continuous topology and automatic version

The automatic version is based on a flip flop that automatically provides a delay and the variable pulse Pv. This delay determines the initial charge pulse area A (Fig.6).

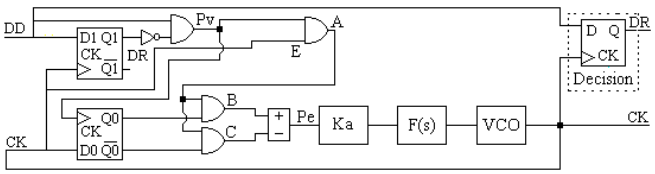

Fig.6 Synchronizer continuous and automatic (c-a)

The flip flop 1, NOT with 1st AND produces a variable pulse Pv and the 2nd AND determines the charge rhythm A.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the $SNR = A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling $\Delta\tau=1/Samp$, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)

$$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi \quad (3)$$

For the hybrid synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)

$$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi \quad (4)$$

For the combinational synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)

$$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04 \quad (5)$$

For the sequential synchronizers, the loop bandwidth is
$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)

$$(Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08 \quad (6)$$

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.
For analog PLL the jitter is
$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$
For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

Following Fig.7 shows the setup that was used to test the various synchronizers.

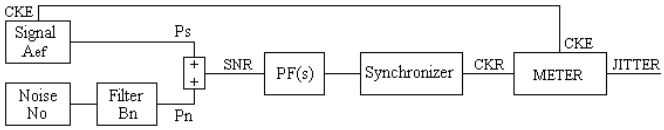

Fig.7 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.8).

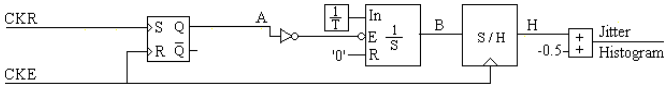

Fig.8 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.
Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (output jitter UIRMS versus input SNR) for the prefilter with the four synchronizers.

Fig.9 shows the jitter-SNR curves of the prefilter bandwidth B1=∞ with the four symbol synchronizers namely discrete manual (d-m), discrete automatic (d-a), continuous manual (c-m) and continuous automatic (c-a).

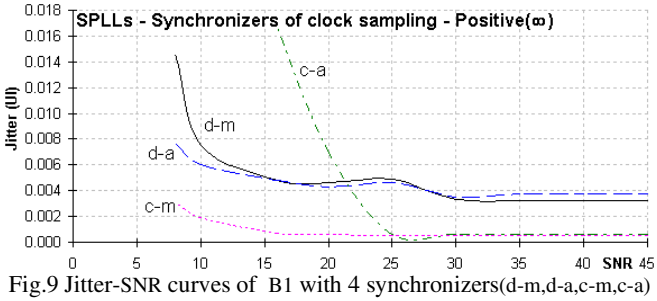

Fig.9 Jitter-SNR curves of B1 with 4 synchronizers(d-m,d-a,c-m,c-a)

We observed that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing.

For the prefilter B1=∞, for high SNR, the four curves tend to be similar, but with some advantage of the continuous topologies (c-m, c-a). However, for low SNR, the continuous manual (c-m) is the best, followed of the discrete topologies (d-m, d-a) and the continuous automatic (c-a) is the worst.

Fig.10 shows the jitter-SNR curves of the prefilter bandwidth B2=2.tx with the four symbol synchronizers namely discrete manual (d-m), discrete automatic (d-a), continuous manual (c-m) and continuous automatic (c-a).

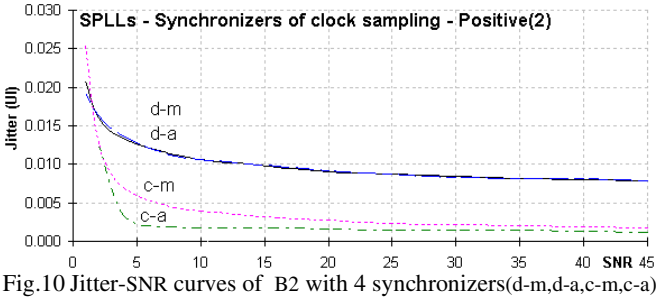

Fig.10 Jitter-SNR curves of B2 with 4 synchronizers(d-m,d-a,c-m,c-a)

For the prefilter B2=2.tx, we verify that, for high SNR, it is malefic and degrades slightly the jitter - SNR curves. However, for low SNR, it is beneficial and improves significantly the jitter-SNR curves becoming them more similar one another.

Fig.11 shows the jitter-SNR curves of the prefilter bandwidth B3=1.tx with the four symbol synchronizers namely discrete manual (d-m), discrete automatic (d-a), continuous manual (c-m) and continuous automatic (c-a).

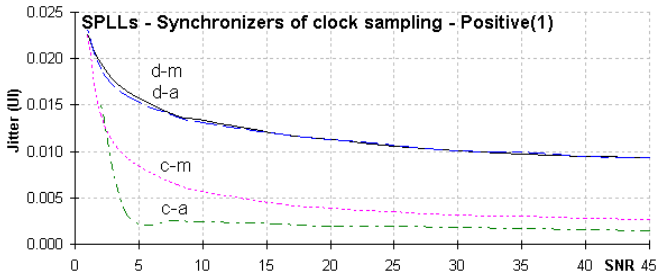

Fig.11 Jitter-SNR curves of B3 with 4 synchronizers(d-m,d-a,c-m,c-a)

For the prefilter B3=1.tx, we verify that, for high SNR, it is malefic and degrades more slightly the jitter - SNR curves. However, for low SNR, it is beneficial and improves less significantly the jitter-SNR curves and become them more similar one another.

V. CONCLUSIONS

We studied the effects of the prefilter bandwidth (B1=∞, B2=2.tx, B3=1.tx) on four synchronizers, two have discrete operation with versions manual (d-m and automatic (d-a) and two have continuous operation with versions manual (c-m) and automatic (c-a). Then, we tested their output jitter UIRMS versus input SNR.

We observed that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing.

For the prefilter with B1=∞, we verified that, for high SNR, the four synchronizers jitter curves tend to be similar, but with a slight advantage of the continuous topologies (c-m, c-a). This is comprehensible since the error pulse Pe, in the discrete topologies don't disappear at the equilibrium point, only changes its direction. However, for low SNR, the continuous manual (c-a) is the best, this is comprehensible since the error pulse Pe diminishes gradually and disappear at the equilibrium point. The discrete topologies (d-m, d-a) have an intermedium jitter performance since their error pulse Pe don't disappear at equilibrium point. The continuous automatic (c-a) has the worst jitter performance since its error pulse Pe has no symmetric positive and negative contributions, what degrade the jitter.

For the prefilter with B2=2.tx, for high SNR, the prefilter degrades slightly the jitter - SNR curves. However, for low SNR, it improves significantly the jitter - SNR curves and become them more similar between themselves.

For the prefilter with B3=1.tx, for high SNR, the prefilter degrades more slightly the jitter - SNR curves. However, for low SNR, it improves less significantly the jitter- SNR curves and become them still more similar between themselves.

So, we ascertain that the prefilter is prejudicial for high SNR and beneficial for low SNR.

In the future, we are planning to extend the present study to other types of synchronizers.

ACKNOWLEDGMENTS

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REFERENCES

[1] J. C. Imbeaux, "performance of the delay-line multiplier circuit for clock and carrier synchronization", IEEE Jou. on Selected Areas in Communications p.82 Jan. 1983.

[2] Werner Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Trans. on Communications com-30 Nº10 pp.2297-2304. Oct 1982.

[3] H. H. Witte, "A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrat. Output Signal", Electronics Letters, Vol.19, Is.21, pp.897-898, Oct 1983.

[4] Charles R. Hogge, "A Self Correcting Clock Recovery Circuit", IEEE Tran. Electron Devices p.2704 Dec 1985.

[5] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "A New Technique to Measure the Jitter", Proc. III Conf. on Telecommunications pp.64-67 FFoz-PT 23-24 Apr 2001.

[6] Marvin K. Simon, William C. Lindsey, "Tracking Performance of Symbol Synchronizers for Manchester Coded Data", IEEE Transactions on Communications Vol. com-2.5 Nº4, pp.393-408, April 1977.

[7] J. Carruthers, D. Falconer, H. Sandler, L. Strawczynski, "Bit Synchronization in the Presence of Co-Channel Interference", Proc. Conf. on Electrical and Computer Engineering pp.4.1.1-4.1.7, Ottawa-CA 3-6 Sep. 1990.

[8] Johannes Huber, W. Liu "Data-Aided Synchronization of Coherent CPM-Receivers" IEEE Transactions on Communications Vol.40 Nº1, pp.178-189, Jan. 1992.

[9] Antonio D'Amico, A. D'Andrea, Reggianni, "Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR", IEEE Jou. on Sattelite Areas in Comm. Vol.19 Nº12 pp.2320-2330, Dec. 2001.

[10] Rostislav Dobkin, Ran Ginosar, Christos P. Sotiriou "Data Synchronization Issues in GALS SoCs", Proc. 10th International Symposium on Asynchronous Circuits and Systems, pp.CD-Ed., Crete-Greece 19-23 Apr. 2004.

[11] N. Noels, H. Steendam, M. Moeneclaey, "Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers", Proc. IEEE Int Conf. on Comm.(ICC'06) pp.2946-2951, Ist.-TK, 11-15 Jun 2006.

[12] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "Effects of the Prefilter Type on Digital Symbol Synchronizers", Proc. VII Symposium on Enabling Optical Network and Sensors (SEONs 2009) pp.35-36, Lisboa (Amadora)-PT 26-26 June 2009.