2010 Fifth International Conference on Systems and Networks Communications

Prefilter Bandwidth Effects in Data Symbol Phase Synchronizers of Open Loop

António D. Reis[1,2] and José P. Carvalho[1]
Dep. Física / Unidade D. Remota
[1]Universidade da Beira Interior, 6200 Covilhã, Portugal
adreis@ubi.pt, pacheco@ubi.pt

José F. Rocha[2] and Atílio S. Gameiro[2]
Dep. Electrónica e Telecom. / Instituto Telecom.
[2]Universidade de Aveiro, 3810 Aveiro, Portugal
frocha@det.ua.pt, amg@det.ua.pt

***Abstract* - This work studies the effects of the prefilter bandwidth on the open loop symbol synchronizers. We consider three different prefilter bandwidth, namely, B1=∞ (infinite), B2=2.tx and B3=1.tx, where tx is the transmission rate. We consider also four open loop symbol synchronizers, namely, the tank (tank), the SAW (SAW), the monostable (mon), and the astable (ast). The objective is to study the prefilter bandwidth with the four open loop symbol synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).**

Keywords - Prefilter; Synchronizers; Communication systems.

I. Introduction

This work studies three prefilter bandwidth effects on the jitter SNR (Signal to Noise Ratio) behavior of four open loop symbol synchronizers.

The Butterworth prefilter, applied before the synchronizer, varies their bandwidth between three values: first B1=∞, next B2=2.tx and after B3=1.tx, tx is the transmission rate value [1, 2].

The open loop symbol phase synchronizers has four types namely the tank (tank), the SAW (SAW), the monostable (mon) and the astable (ast) [3, 4].

The tank and the SAW are analog circuits whereas the monostable and the astable are digital circuits [6, 7, 8].

In the analog circuits, the output is a filtered harmonic of the input symbols. In the digital circuits, the output is a rectangular wave controlled by the input symbols [9, 10].

Fig.1 shows the prefilter followed of the synchronizer.

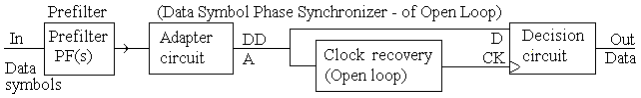

Fig. 1 Prefilter with the symbol synchronizer of open loop

The open loop synchronizer, without loop, has some jitter quality limitations, but can work at very high speed.

Next, we present the state of the art. Then, we present the prefilter with three bandwidths (B1=∞, B2=2.tx, B3=1.tx).

Next, we present the four open loop synchronizers, namely the tank (tank), SAW (SAW), monostable (mon), and astable (ast). After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. State of the Art, Problem and Solution

In the prior and actual state-of-the-art various synchronizers were developed, but their performance was not satisfactory or not clrealy known.

The motivation of this work is to create new synchronizers and evaluate their performance with noise. This contribution increases the knowledge about synchronizers [11, 12].

The problem is that, the synchronizers output jitter increases when the input SNR decreases. To solve or to minimize the problem, we can use a prefilter that attenuates the noise, but distorts slightly the signal.

Prefilter Bandwidth Effects

The prefilter applied before the synchronizer, filters the noise but disturbs slightly the signal. The prefilter bandwidth B switches between three values (B1=∞, B2=2.tx, B3=1.tx).

Fig. 2 shows the prefilter with their three bandwidths.

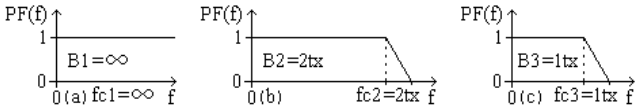

Fig. 2 Three prefilter bandwidths: a) B1=∞; b) B2=2.tx; c) B3=1.tx

a) First, the prefilter (Fig.2a) has a bandwidth equal to infinite (B1= ∞).

b) Second, the prefilter (Fig.2b) has a bandwidth equal to times the transmission rate (B2 = 2.tx).

c) Third, the prefilter (Fig.2c) has a bandwidth equal to the transmission rate (B3 = 1.tx).

We will evaluate the three bandwidth effects (B1, B2, B3) on the jitter-SNR curves of the four carrier synchronizers.

Four Synchronizers of Open Loop

We will present four closed loop symbol synchronizers, namely the tank circuit (tank), SAW circuit (SAW), monostable circuit (mon) and astable circuit (ast) [1, 2, 3].

A. *Tank circuit*

The tank circuit is a LC tuned filter with narrow band to the data rate that selects the symbols fundamental harmonic. This harmonic is the recovered clock (Fig. 2).

978-0-7695-4145-7/10 $26.00 © 2010 IEEE
DOI 10.1109/ICSNC.2010.73

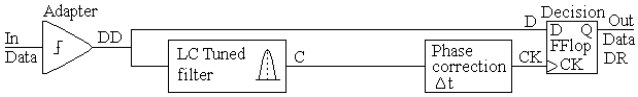

Fig. 2 Tank circuit

The adapter provides a signal with appropriate voltage level to excite the tuned circuit. The LC tuned filter selects the symbols fundamental harmonic that is the recovered clock. The phase correction gives, to the clock, the correct phase to sample appropriately the data symbols.

The decision (flip flop) samples the data at the appropriate time and retimes the bits duration.

B. SAW circuit

The SAW circuit is a crystal tuned filter with narrow band to the data rate to select the symbols fundamental harmonic.

The SAW has a piezoelectric transducer that is excited by data transitions and provides waves but only the fundamental (clock) is propagated and reaches the output filter (Fig.4).

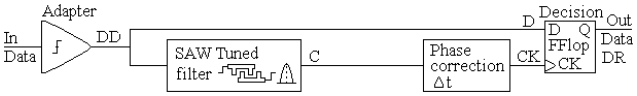

Fig. 4 SAW circuit

The adapter gives the appropriate signal level to excite the following blocks.

The SAW tuned filter selects the fundamental harmonic that is the recovered clock.

The phase correction gives to the clock the correct phase to sample appropriately the data symbols.

The decision (flip flop) samples the data at the appropriate time and retimes the bits duration.

The dielectric resonator (tuned microstrip lines) has similar behavior with SAW, therefore isn't described here.

C. Monostable circuit

The monostable circuit is a digital circuit that has two states one no-stable and other stable, where normally it is. The monostable is excited by the data transitions. The monostable maintains its oscillation, feedbacking the output pulse that takes effect only if no data transitions occur (Fig. 5).

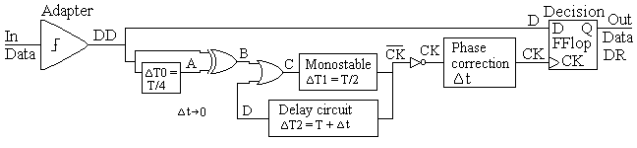

Fig. 5 Monostable circuit

The adapter provides the appropriate signal level to excite the next blocks.

The monostable, in the beginning, is in the stable state. When occurs a data transition, the delay ΔT0 and exor produces a pulse B that excites the monostable ΔT1 producing a positive pulse /CK. This pulse is feedbacked to the entered taking effect only if B don't occurs.

Then, successively, the pulse B or pulse /CK construct the clock /CK. The NOT gate gives the correct phase CK.

The phase correction gives the correct phase to the clock to sample appropriately the data. In this case the phase correction isn't need.

The decision (flip flop) samples the data at the appropriate time and retimes the bits duration.

D. Astable circuit

The astable circuit is a digital circuit that has two states, but both no-stable (multivibrator). The astable wave phase, if necessary, is corrected by the data transition pulses. The astable has its own oscillation tuned to the data rate (Fig.6).

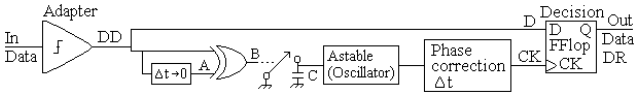

Fig.6 Astable circuit

The adapter provides the appropriate signal level to excite the next blocks.

The astable is tuned to oscillate at the data rate. The data transition pulses B are used only to correct the phase of the clock CK.

The phase correction gives the correct phase to the clock to sample appropriately the data. In this case, the phase correction isn't need.

The decision (flip flop) samples the data at the appropriate time and retimes the bits duration.

DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then, although the different nature, it is necessary to design all the loops with identical linearized parameter conditions

The general loops must have similar parameters, that permits the desired characteristics. In open loop, the tuning band Bs must be similar with the loop bandwidth, where the loop gain Kl=Kd.Ko=Ka.Kf.Ko, (Kf is the phase comparator gain, Ko is the VCO gain and Ka is the amplification factor that determines the desired characteristics).

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn =

5Hz and a normalized bandwidth Bl = 0.02Hz. This is equivalent to a filter bandwidth (tuning band) Bs=0.02Hz. In the monostable, we use a delay Δt=T/100=0.01s. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension is

- Tuning loops:

The tuning frequencies fo for the analog circuits (tank, SAW) and digital circuits (monostable, astable) can be given by the following formulas. So, for the tank

$$fo= \frac{1}{2\pi LC} \quad (1)$$

and for the monostable

$$fo=-\frac{1}{2\ln(0.5)RC}=\frac{1}{2*0.7RC} <---(0.5=1*e^{-\frac{t}{\tau}}|t=T/2) \quad (2)$$

For the SAW and astable, we must see the manufacturer datasheets.

B. Tests

Fig. 7 shows the setup that was used to test the various synchronizers.

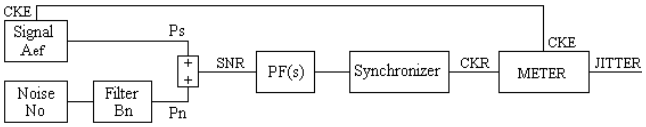

Fig. 7 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter Measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.8).

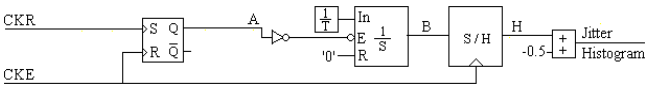

Fig. 8 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We studied two analog synchronizers (tank, SAW) and two digital synchronizers (monostable, astable).

However, we only present the results (output jitter UI-RMS versus input SNR) of one analog synchronizer (tank) and one digital synchronizer (monostable) since the jitter behavior of the SAW is similar with the tank's and the astable is similar with the monostable's.

Fig. 9 shows the jitter UIRMS - SNR curves of the prefilter bandwidth B1=∞, with the analog synchronizer (tank) and digital synchronizer (mon).

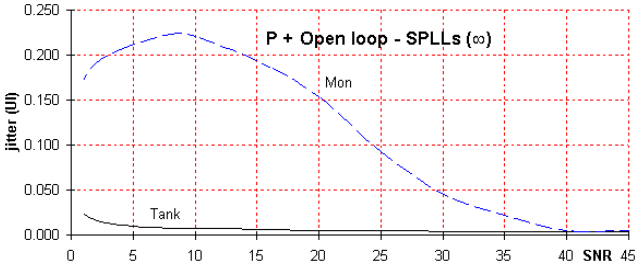

Fig. 9 Jitter-SNR curves of B1 with the tank and mon. (tank, mon)

We verify that, for high SNR (SNR>40), the digital synchronizer (mon) becomes slightly advantageous over the analog synchronizer (tank) due to the noise margin of their gates. However, for low SNR (SNR<40), the analog synchronizer (tank) is widely advantageous over the digital synchronizer (mon) due to the fortuitous random commutations of the monostable gates.

The monostable begins with operation problems for SNR<30, what increases the jitter.

Fig.10 shows the jitter UIRMS - SNR curves of the prefilter bandwidth B2=2.tx, with the analog synchronizer (tank) and digital synchronizer (mon).

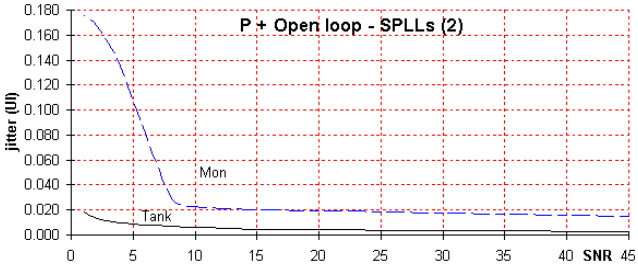

Fig. 10 Jitter-SNR curves of B_2 with the tank and mon.(tank, mon)

For high SNR (SNR>10), the analog synchronizer (tank) is slightly advantageous over the digital synchronizer (mon),

due to the noise margin of their gates. However, for low SNR (SNR<10), the analog synchronizer (tank) is widely advantageous over the digital synchronizer (mon) due to the fortuitous random commutations of the monostable gates.

The monostable begins with operation problems for SNR<10, what increases greatly the jitter.

Fig. 11 shows the jitter UIRMS - SNR curves of the prefilter bandwidth B3=1.tx, with the analog synchronizer (tank) and digital synchronizer (mon).

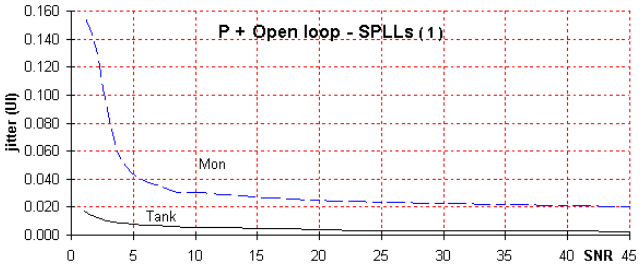

Fig. 11 Jitter-SNR curves of B_3 with the tank and mon.(tank, mon)

For high SNR (SNR>5), the analog synchronizer (tank) is slightly advantageous over the digital synchronizer (mon), due to the noise margin of their gates. However, for low SNR (SNR<5), the analog synchronizer (tank) is widely advantageous over the digital synchronizer (mon) due to the fortuitous random commutations of the monostable gates.

The monostable begins with operation problems for SNR<5, what increases greatly the jitter.

CONCLUSION AND FUTURE WORK

We studied the prefilter with three bandwidths (B1=∞, B2=2.tx, B3=1.tx) followed of four open loop symbol synchronizers: two analog (tank, SAW) and two digital (monostable, astable).

We know that the analog types (tank and SAW) have similar jitter-SNR curves and the same happens with the digital types (mon and ast).

Then, we tested only the jitter-SNR behavior of one analog synchronizer (tank) and one digital synchronizer (mon).

For the prefilter with B1=∞, we verified that, only for high SNR (SNR>40) the digital synchronizer (mon) becomes slightly advantageous over the analog synchronizer (tank), because the tank filter hasn't noise margin whereas the monostable gates have noise margin. However, for low SNR (SNR<40) the analog synchronizer (tank) is widely advantageous over the digital synchronizer (mon), because the tank filters the noise and the monostable gates are randomly commutated by the noise spikes.

So, in brief, for high SNR (>40), we can use the monostable but for low SNR (<40) we must use the tank.

The digital type (mon) has the digital robustness and the unnecessary rigorous tuning.

For the prefilter with B2=2.tx, the two jitter-SNR curves becomes more similar for the range SNR>10, because the monostable operation problems begins for SNR<10.

For the prefilter with B3=1.tx, the two jitter-SNR curves becomes still more similar for the range SNR>5, because the monostable operation problems begins for SNR<5

So, we observe that the prefilter tends to approximate the synchronizer jitter-SNR curves.

In the future, we are planning to extend this study to other new synchronizer types.

ACNOWLEDGMENT

The authors are grateful to the FCT (Foundation for sCience and Technology) / POCI2010.

REFERENCES

[1] J. C. Imbeaux, "Performance of the delay-line multiplier circuit for clock and carrier synchronization", IEEE Jou. on Selected Areas in Communications p. 82 Jan. 1983.

[2] W. Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Trans. on Communications com-30 Nº10 pp. 2297-2304. Oct 1982.

[3] H. H. Witte, "A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrat. Output Signal", Electronics Letters, Vol.19, Is.21, pp. 897-898, Oct 1983.

[4] Ch. R. Hogge, "A Self Correcting Clock Recovery Circuit", IEEE Tran. Electron Devices p.2704 Dec 1985.

[5] A. D. Reis, J. F. Rocha, A. S. Gameiro, and J. P. Carvalho "A New Technique to Measure the Jitter", Proc. III Conf. on Telecommunications pp. 64-67 FFoz-PT 23-24 Apr 2001.

[6] M. K. Simon, and W.C. Lindsey, "Tracking Performance of Symbol Synchronizers for Manchester Coded Data", IEEE Transactions on Communications Vol. com-2.5 Nº4, pp. 393-408, April 1977.

[7] J. Carruthers, D. Falconer, H. Sandler, and L. Strawczynski, "Bit Synchronization in the Presence of Co-Channel Interference", Proc. Conf. on Electrical and Computer Engineering pp.411-417, Ottawa-CA 3-6 Sep. 1990.

[8] J. Huber and W. Liu "Data-Aided Synchronization of Coherent CPM-Receivers" IEEE Transactions on Communications Vol.40 Nº1, pp. 178-189, Jan. 1992.

[9] A. D'Amico, A. D'Andrea, and P. Reggianni, "Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR", IEEE Jou. on Sattelite Areas in Comm. Vol.19 Nº12 pp. 2320-2330, Dec. 2001.

[10] R. Dobkin, R.Ginosar, and Ch. P. Sotiriou "Data Synchronization Issues in GALS SoCs", Proc. 10th International Symposium on Asynchronous Circuits and Systems, pp.CD-Ed., Crete-Greece 19-23 Apr. 2004.

[11] N. Noels, H. Steendam, and M. Moeneclaey, "Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers", Proc. IEEE Int Conf. on Comm.(ICC'06) pp. 2946-2951, Ist.-TK, 11-15 Jun 2006.

[12] A. D. Reis, J. F. Rocha, A. S. Gameiro, and J. P. Carvalho "Effects of the Prefilter Type on Digital Symbol Synchronizers", Proc. VII Symposium on Enabling Optical Network and Sensors (SEONs 2009) pp. 35-36, Lisboa (Amadora)-PT 26-26 June 2009.