Sequential Symbol Synchronizers based on Pulse Comparison Operating by Positive Transitions at Quarter Rate

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Abstract - **This work presents the sequential symbol synchronizer based on pulse comparison by positive transitions at quarter rate (txp/4). Their performance is compared with a reference synchronizer by both transitions at the rate (tx).**

For the reference and proposed synchronizer we consider two versions which are the manual (m) and the automatic (a).

The objective is to study the four synchronizers and evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).

Keywords **– Synchronism, Digital Communications**

I. INTRODUCTION

This work studies the sequential symbol synchronizer, based on pulse comparison by positive transitions at quarter rate. Their jitter performance is compared with the reference synchronizer operating by both transitions at bit rate [1, 2].

For both, reference and proposed synchronizer, we consider the versions manual and automatic [3, 4, 5, 6, 7].

The difference between the proposed and reference synchronizer is in the symbol phase synchronizer since the others blocks are similar. The phase comparator compares a variable pulse Pv with a fixed pulse Pf and the error pulse Pe synchronizes the VCO [8, 9, 10, 11, 12].

The synchronizer VCO (Voltage Controlled Oscillator) follows the input data. The VCO is the good quality clock, that samples the input data and retimes its bit duration.

Fig.1 shows the blocks of a general symbol synchronizer.

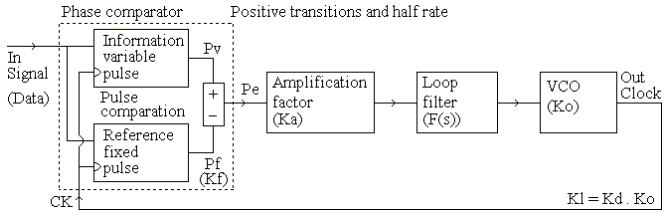

Fig.1 Synchronizer based on pulse comparison

Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop amplification factor that controls the root locus and then the loop characteristics.

In priori and actual-art state was developed various synchronizers, now is necessary to know their performance.

The motivation of this work is to create new synchronizers and to evaluate their performance with noise. This contribution increases the knowledge about synchronizers.

Following, we present the reference synchronizer with their manual (b-m) and automatic (b-a) versions.

After, we present the proposed synchronizer with their manual (p-m/4) and automatic (p-a/4) versions.

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. REFERENCE SYNCHRONIZER BY BOTH AT RATE

The reference synchronizer based on pulse comparison operating by both transitions at bit rate has two versions which are the manual (b-m) and the automatic (b-a) [1, 2].

A. Manual version of the reference synchronizer

The flip flop 0 with exor 0 produces a variable pulse Pv between the input bits and VCO. The manual adjustment delay with exor 1 produces a manual fixed pulse Pf (Fig.2).

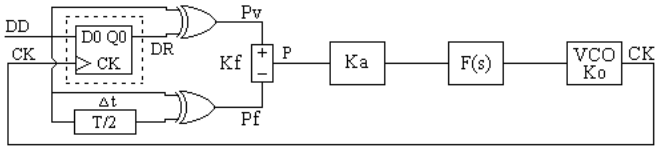

Fig.2 Synchronizer both at the rate and manual (b-m)

The comparison between the pulses Pv and Pf provides the pulse Pe that forces the VCO to follow the input data bits.

Fig.3 shows the waveforms of the manual version of the reference synchronizer by both transitions at bit rate.

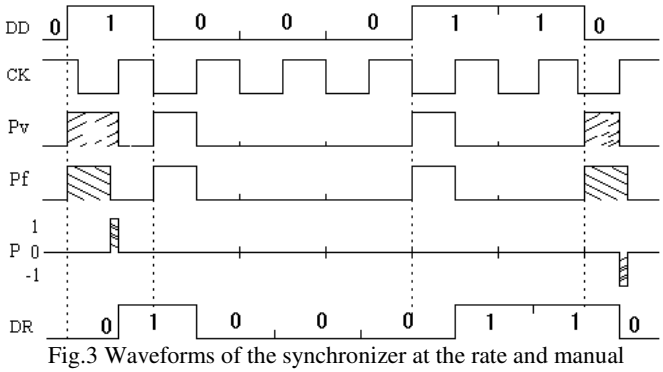

Fig.3 Waveforms of the synchronizer at the rate and manual

The error pulse Pe diminishes during the synchronization and disappear at the equilibrium point.

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B. Automatic version of the reference synchronizer

The flip flop 0 with exor 0 produces a variable pulse Pv between the input bits and VCO. The second flip flop with exor 1 produces an automatic fixed pulse Pf (Fig.2).

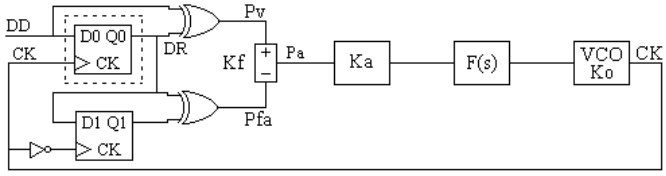

Fig.4 Synchronizer both at the rate and automatic (b-a)

The comparison between the pulses Pv and Pf provides the pulse Pe that forces the VCO to follow the input data bits.

Fig.3 shows the waveforms of the automatic version of the reference synchronizer by both transitions at bit rate.

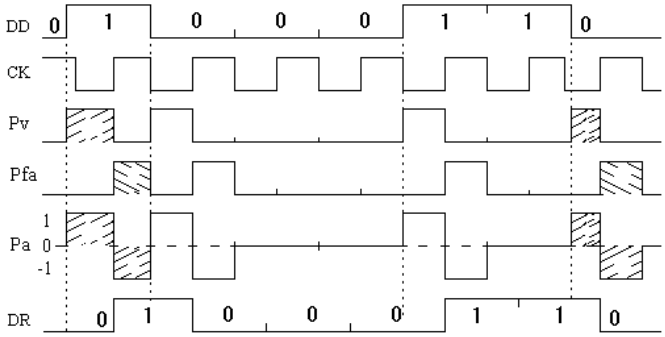

Fig.5 Waveforms of the synchronizer at the rate and automatic

The error pulse Pe don't disappear, but the variable area Pv is equal to the fixed Pf at the equilibrium point.

III. PROPOSED SYNCHRONIZER AT QUARTER RATE

The proposed synchronizer based on pulse comparison operating by positive transitions at quarter rate has also two versions the manual (p-m/4) and automatic (p-a/4) [3, 4].

A. Manual version of the proposed synchronizer

The flip flops group 0 with AND0 produces a variable pulse Pv between the input bits and VCO. The manual adjustment delay with exor 1 produces a manual fixed pulse Pf (Fig.6).

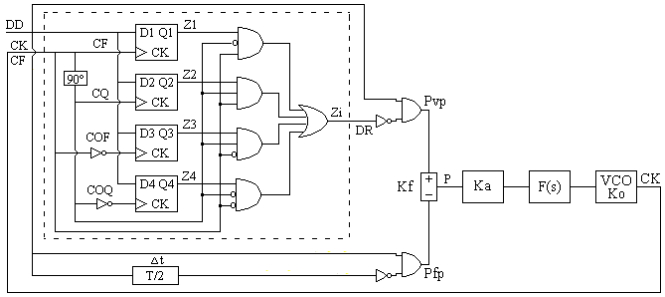

Fig.6 Synchronizer positive at quarter rate and manual (p-m/4)

The comparison between the pulses Pv and Pf provides the pulse Pe that forces the VCO to follow the input data bits.

Fig.7 shows the waveforms of the manual version of the proposed synchronizer by positive transitions at quarter rate.

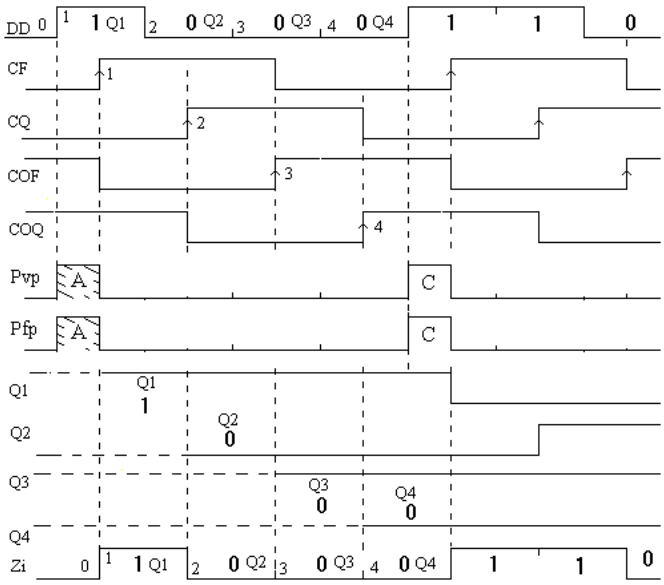

Fig.7 Waveforms of the synchronizer at quarter rate and manual

The error pulse Pe diminishes and disappear at the equilibrium point.

B. Automatic version of the proposed synchronizer

The flip flops group 0 with AND0 produces a variable pulse Pv between the input bits and VCO. The second flip flops group with AND 1 produces an automatic fixed pulse Pf (Fig.8).

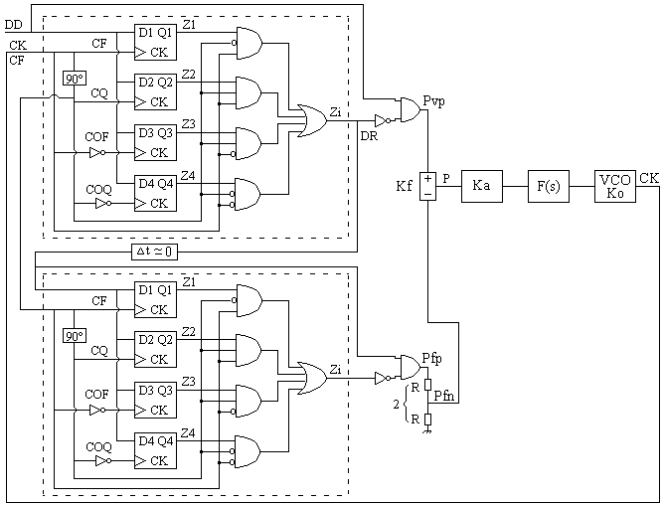

Fig.8 Synchronizer positive at quarter rate and automatic (p-a/4)

The comparison between the pulses Pv and Pf provides the pulse Pe that forces the VCO to follow the input data bits.

Fig.9 shows the waveforms of the automatic version of the proposed synchronizer by positive transitions at quarter rate.

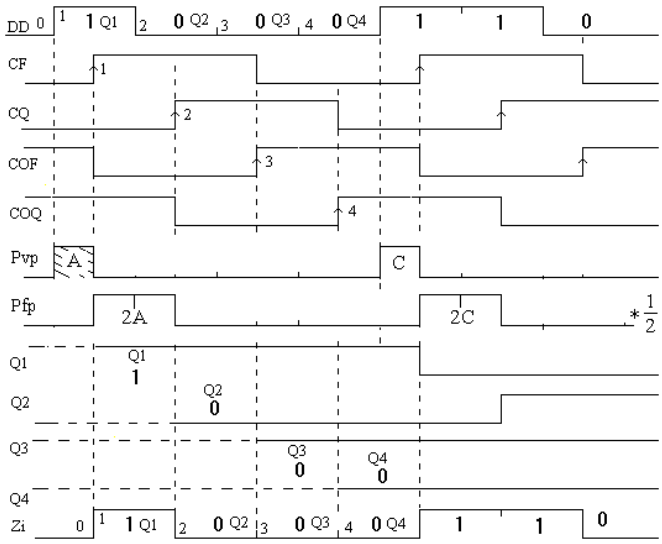

Fig.9 Waveforms of the synchronizer at quarter rate and automatic

The error pulse Pe don't disappear but the positive area is equal to the negative at the equilibrium point.

IV. DESIGN, TESTS AND RESULTS

We present the design, tests and results of the referred synchronizers [5].

A. Design

To get guaranteed results, all the synchronizers must be compared in equal conditions. Then, it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko, where Kf is the phase detector gain, Kd is the phase comparator gain, Ko is the VCO gain and Ka is the loop amplification factor that controls the root locus and desired characteristics.

To facilitate the analysis, we use a normalized transmission rate tx=1baud, giving normalised values to others parameters. So, we choose a normalized clock frequency fCK=1Hz, an extern noise bandwidth Bn=5Hz and a loop noise bandwidth Bl=0.002Hz. Then, we applie a signal power Ps= A^2_{ef} and a noise power Pn= No= $2\sigma n^2.\Delta\tau$, where σn^2 is the noise standard deviation and $\Delta\tau$ =1/fSamp is the sampling period.

The relation between SNR and noise variance σn is SNR= $A^2_{ef}/(No.Bn)=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn)=0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, for each synchronizer, we observe its output jitter UI as function of the input SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s=0)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times greater than Bl=0.02Hz) eliminates only the high frequency, but maintain loop characteristic. The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

So, for the analog synchronizers, with (Km=1, A=1/2, B=1/2, Ko=2π) and loop bandwidth Bl=0.002, we obtain Ka

$$Bl=(Ka.Kf.Ko)/4=(Ka.Km.A.B.Ko)/4 \rightarrow Ka=0.08*2/\pi \quad (3)$$

For the hybrid synchronizers, with (Km=1, A=1/2, B=0.45, Ko=2π) and loop bandwidth Bl=0.002, we obtain Ka

$$Bl=(Ka.Kf.Ko)/4=(Ka.Km.A.B.Ko)/4 \rightarrow Ka=0.08*2.2/\pi \quad (4)$$

For the combinational synchronizers, with (Kf=1/π; Ko=2π) and loop bandwidth Bl=0.002, we obtain Ka

$$Bl=(Ka.Kf.Ko)/4=(Ka*1/\pi*2\pi)/4 \rightarrow Ka=0.04 \quad (5)$$

For the sequential synchronizers, with (Kf=1/2π; Ko=2π) and loop bandwidth Bl=0.002, we obtain Ka

$$Bl=(Ka.Kf.Ko)/4=(Ka*1/2\pi*2\pi)/4 \rightarrow Ka=0.08 \quad (6)$$

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.
For the analog PLL, the jitter is

$$\sigma_\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2 \quad (7)$$

For the others PLLs, the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

Following Fig.10 shows the setup that was used to test the various synchronizers.

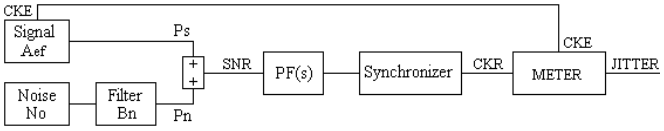

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (M) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

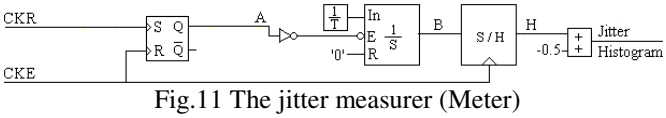

Fig.11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by a given program, providing the RMS and peak to peak jitter.

D. Results

We present the results in terms of output jitter UIRMS versus input SNR (graphics UIRMS-SNR). Fig.12 shows the jitter UIRMS-SNR curves of the reference synchronizer by both transitions at rate manual (b-m) and automatic (b-a) and the proposed synchronizer by positive transitions at quarter rate manual (p-m/4) and automatic (p-a/4).

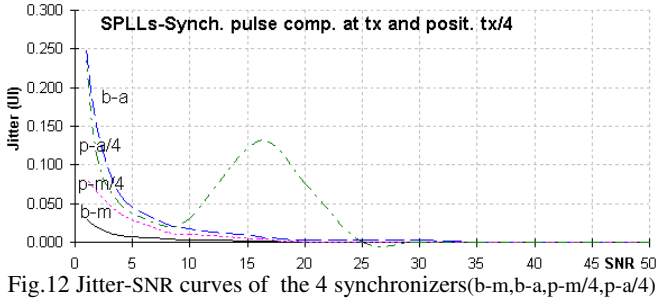

Fig.12 Jitter-SNR curves of the 4 synchronizers(b-m,b-a,p-m/4,p-a/4)

We see that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing. However, the positive quarter rate automatic (p-a/4) has some irregularities.

For high SNR, the four synchronizer jitter curves tend to be similar. However, for low SNR, the manual versions (b-m, p-m/4) are significantly better than the automatic versions (b-a, p-a/4). The reference synchronizer by both transitions at rate manual (b-m) is slightly the best. Also, for SNR (SNR≅16), the proposed synchronizer by positive transitions at quarter rate automatic (p-a/4) has significant perturbations with losses of synchronism what increases strongly the jitter.

V. CONCLUSIONS

We studied four synchronizers with one reference variant operating by both transitions at rate that has two versions namely the manual (b-m) and automatic (b-a) and other proposed variant operating by positive transitions at quarter rate that has two versions namely the manual (p-m/4) and automatic (p-a/4). Then, we tested their jitter - noise curves.

We observed that, in general, the output jitter curves decreases gradually with the input SNR increasing. However, the proposed synchronizer positive quarter automatic (p-a/4) has some irregularities.

We verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since all the synchronizers are digital with equal noise margin. However, for low SNR, the manual versions (b-m, p-m/4) are significantly better than the automatic versions (b-a, p-a/4), this is comprehensible since the automatic versions have more digital states with greater error state propagation. The reference version both transitions at rate manual (b-m) is slightly the best because has less digital states. Also, for a SNR (SNR≅16), the proposed synchronizer positive transitions at quarter rate automatic (p-a/4) has a significant jitter perturbation due to some losses of synchronism.

In the future, we are planning to extend the present study to other types of synchronizers.

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