Base Station Transceiver Design in a Digital Wireless Local Loop System

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Abstract

During the past ten years the mobile radio communications industry has significantly grown. The miniaturization technologies has allowed to achieve smaller and smaller portable terminal radio equipment. People throughout the world have been adhering to the wireless communications methods and services mainly to those of the public cellular mobile network. The digital cellular mobile networks already implemented all over the world such for instance, the GSM, PDC and IS-95 provide a very low bit rate which is inefficient for data and video services. Higher bit rate mobile networks have nowadays been under research and development. This paper describes a base station transceiver for a higher bit rate digital wireless local loop communications system.

1. Introduction

Future forecasts show that the fixed telephone handset will eventually disappear and will be replaced by mobile equipment [1]. However, mobile subscribers' demands for multimedia services such as the global information exchange and videotelephony require higher capacity networks. This paper describes a full duplex communications system and examines the base station design. Figure 1 shows the base station block diagram.

Asymmetric transmission bit rates have been adopted, 2Mbps (2.56 Mbps with channel coding) in the downlink and 64kbps in the uplink. This system operates at 1.5 GHz band and a QPSK modulation scheme is used in the base and mobile terminals. A direct sequence code division multiple access (DS-CDMA) is implemented in the subscribers.

Phase differences between multipath reflections and the portable unit movements produce amplitude fluctuations and Doppler shifting. Channel equalization [2] is then needed in both links to compensate for the time-varying phenomenon caused by multipath fading. Portable units can be cost reduced by moving equalization function to the base station. Therefore a precoding architecture is discussed.

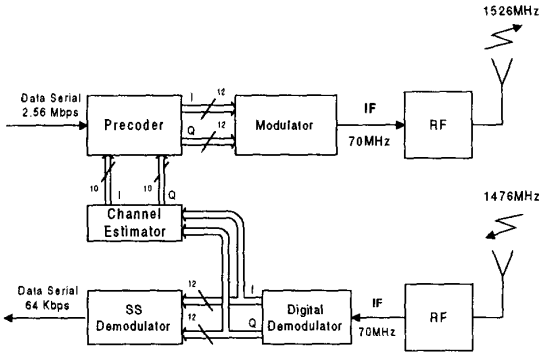

Fig. 1. Base Station Block Diagram

This paper is divided in the following sections. Firstly, section 2 discusses the precoding implementation considerations. Then, section 3 deals with the solution for digital modulation and mobile channel access. Section 4 discusses the front end RF modules as well as the QPSK modulation. Finally, in section 5, some conclusions and future work are addressed.

2. Precoding Architecture

As explained in the previous section, downlink channel equalization is implemented in the base station by the Precoder and Channel Estimator blocks (see Figure 1). The Precoder is an Infinite Impulse Response (IIR) filter whereas the channel model is a (Finite Impulse Response) FIR filter. As the modulation scheme is QPSK, filter coefficients are complex numbers. A digital signal microprocessor from Texas Instrument TMS320C31 [3] deals with FIR filter coefficient reestimation characterizing the nonstationary radio channel. This information concerning the channel is

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fed into the Precoding block which consists of a Tomlinson's modulo arithmetic inverse filter [4]. This is implemented by an Altera CPLD [5] and a Logic FIR [6] devices. To eliminate completely the possibility of instability, a modulo-N adder is used instead of the conventional adder in the IIR filter [4]. The inverse modulo-N operation is carried out in the mobile receiver. The Precoder filter is then given by,

$$H_p(z) = \frac{1}{1+\sum_{i=1}^{N} a_i z^{-k}} \bmod N$$

and the model of the radio channel is,

$$H_c(z) = \sum_{i=1}^{N} b_i z^{-k}$$

where the coefficient vector $\mathbf{b}=[b_0, b_1, \ldots b_N]^T$ is estimated by the least square solution, $\mathbf{b}=\mathbf{R}_{xx}^{-1}\,\mathbf{r}_{yx}$. $\mathbf{R}_{xx}$ is the autocorrelation matrix of the training data **x** transmitted by the mobile and $\mathbf{r}_{yx}$ is the cross-correlation vector between the training data **x** and the corresponding received data **y**.

The product of both above mentioned filters must provide a unit gain. Therefore, each Precoder filter coefficient is divided by the first channel filter coefficient,

$$b_i = a_i / b_0, \qquad i = 1,2,\ldots,N$$

and before sending to the QPSK modulator, the in-phase I and quadrature Q signals are divided by b_0.

3. QPSK Demodulation and DS-CDMA

Led by the Global Positioning System (GPS), the spread spectrum concept has emerged from secure military communications to many commercial applications. Of the many potential uses for spread spectrum communications in this area, opportunities in wireless LANs, wireless local loops, automated data collection, personal communication networks, and digital cellular radios are some well-known examples.

Spread spectrum systems, due to the nature of their signal characteristics, have the following important performance attributes considered to be potential benefits in commercial applications: [7]

- Low probability of intercept (LPI).
- Anti-jamming capability and resistance to intentional or unintentional interference.
- Privacy.
- Resistance to multipath.
- High time resolution.
- Sharing of a common radio frequency band by multiple users (multiple access) through Code Division Multiple Access (CDMA).

CDMA offers numerous advantages over the TDMA and FDMA such as the simplification of system planning, enhanced privacy and bandwidth on-demand but the most important is the potential increase in system capacity. Even though the capacity in a CDMA system is interference limited, the introduction of each additional channel raises the overall level of interference to the base-station receivers hence a graceful performance degradation results as the number of users increase as opposed to the fixed capacity of a TDMA system.

3.1 Spread Spectrum Digital Demodulator

A DS-CDMA transmitter uses a locally generated pseudo noise (PN) code *c(t)* running at a much higher rate than the data rate to encode digital data *b(t)* to be transmitted. Data for transmission is simply logically modulo-2 added (an XOR operation) with the faster pseudo noise code and then is used directly to modulate the carrier in QPSK producing DS-SS QPSK signal *s(t)*:

$$s(t) = Ab(t)\left[c_1(t)\sin(2\pi f_c t + \theta) + c_2(t)\cos(2\pi f_c t + \theta)\right]$$

where *A* is the amplitude of the signal, $c_1(t)$ and $c_2(t)$ correspond to the in-phase and quadrature chips of the PN code.

The DS-CDMA receiver [8] uses a locally generated replica of the PN code and a receiver correlator or matched filter to separate only the desired coded information from all possible signals. To achieve discrimination between users the receiver responds only to SS signals with identical matched signal characteristics and encoded with the same pseudo noise code. Figure 2 shows a typical SS demodulator block diagram.

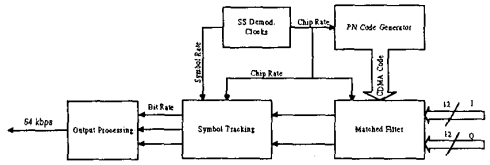

Fig. 2. SS Demodulator Block Diagram

To allow the system to sample the incoming signal asynchronously at the I.F. sampling rate with respect to the PN spreading rate, the Matched Filter is designed to operate with two signal samples per chip. A front end processor operating on both the I and Q channels averages the incoming data over each chip period by adding each incoming baseband sample to the previous one. The Matched Filter computes the cross-correlation between the I and Q channel signals and the locally stored PN code at the baseband sampling rate, which is twice per chip. These I and Q channel Matched Filter outputs are then fed into the Symbol Tracking Unit. Ideally, this output will have a high peak value once per symbol, i.e. once per PN code cycle, when the code sequence of the received signal in the Matched Filter is aligned with the same reference code used in the

Matched Filter. At that instant the I and Q channel outputs of the Matched Filter are, theoretically, the optimally despread I and Q symbols. Because the receiver is operating in QPSK mode, the data received is processed in pairs of bits, one bit for the in-phase (I) channel and one for the quadrature (Q) channel. Single-bit I/O data is converted from this format by the Output Processor, producing the serial 64 kbps data output.

3.2 QPSK Digital Demodulator

The digital demodulator [9] used in receiver accepts an IF 70MHz input QPSK signal that is amplified and filtered by a SAW filter centered at the IF frequency, which reduces the signal bandwidth to less than half the sampling frequency for sampling and digitalization. The filter used is selected for the symbol rate to minimize adjacent channel interference and signal distortion, which results in inter-symbol interference.
The filtered IF signal is then amplified and sampled at a clock rate sufficiently high to avoid aliasing. The AGC logic at the output of the ADC senses whether the signal is above or below the nominal operating point of the receiver. The digital signal is afterwards applied to an integrator whose output is fed back to the gain of the IF amplifiers. The AGC loop also guaranties that the signal is scaled optimally to the ADC range.

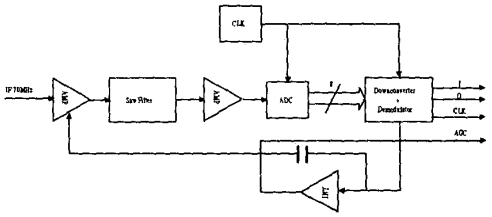

Fig. 3. The AGC Amplifier, ADC and Digital Demodulator

In the Downconverter and Demodulator Block, the IF signal is digitally mixed with the quadrature signals and the products are filtered with a digital I&D filter (see Figure 4). The outputs of the filter are baseband I and Q components which are fed into the Bit Synchronizer. A phase lock loop is included to perform bit synchronization, using an NCO to generate the dump clock that samples the I&D filters. A carrier discriminator function is also provided, which generates either a frequency or phase discriminator signal, used as a feedback to the loop filter to assist in carrier tracking, from the synchronized I and Q outputs.

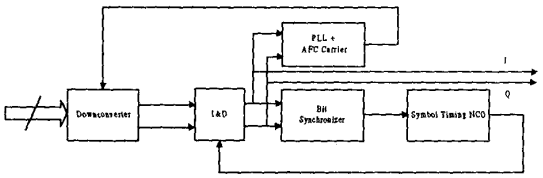

Fig. 4. Digital Demodulator and Downconverter Details

4. QPSK Modulator and RF Design

Technological advances continue to expand the range of usable frequencies. It is well known that transmission characteristics in the range from a few hundreds of Megahertz to a couple of Gigahertz are especially attractive for many fixed and mobile services. The air interface of this system operates at two distinct frequencies around 1.5GHz. These frequencies were assigned by the ICP (Portuguese Institution of Communications) for experimental field trial. The bandwith used is 4MHz in each link.

4.1-The Transmitter

Figure 5 shows the block diagram of the base station transmitter implemented by several commercially available devices. After modulation the IF signal is converted to the RF frequency (1476MHz at the mobile terminals and 1524MHz at the base station), amplified and filtered. The specified output power assuming no power control at the subscriber is 0.5W. The QPSK modulator from Mini-circuits [10] is driven by a 70MHz synthesized oscillator [11] which is controlled by a 14 MHz crystal oscillator. To eliminate spurious response of the QPSK modulator a band pass filter is used. The RF signal is achieved by mixing the IF modulating signal with the 1546 MHz carrier. The carrier signal is obtained through a frequency synthesizer from Motorola [12] which makes use of a reference crystal of 6.0390625 MHz.
After mixing the IF signal and RF carrier signal the resulting signal is filtered by a microstrip line filter and amplified. The design of this filter is critical since the IF is much lower than RF. A rejection of 20dB is achieved at the image frequency.
Finally, the power amplifier adjusts the power transmitted at the base station. At maximum level the emitter power is 27dBm obtained from a commercial MMIC circuit [13].

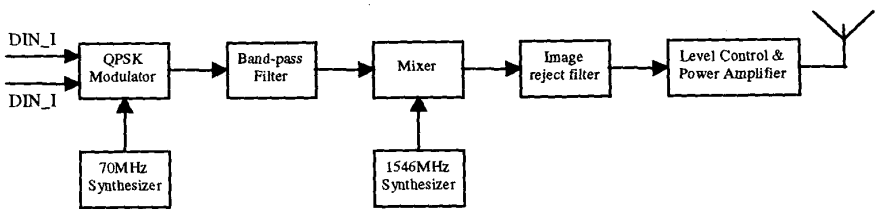

Fig. 5. Block Diagram of the Base Station Transmitter

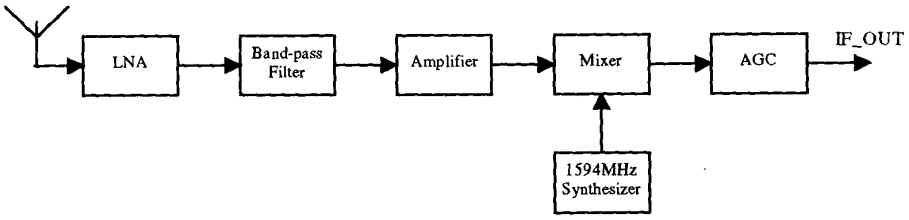

Fig. 6. Block Diagram of the Base Station Receiver

4.2 The Receiver

In the reception path the blocks perform the opposite functions and are implemented using available devices from the companies mentioned in the last section. The first module is the LNA and is designed to provide a sensitivity of -80dBm which means a distance between the base station and the mobile of up to 8km. It has been constructed microstrip patch antennas of 10dB gain. The signal is then fed to a band pass filter and linearly amplified by a MMIC device. This rejection image filter is design in microstrip technology. The overall gain of this two stage amplification is 44dB, and some care must be taken to avoid oscillations. The signal after amplification is downconverted to the IF of 70MHz. The 1594 MHz oscillator is implemented following the same principles of that in the transmitter. At the IF stage, an AGC amplifier which is designed to provide a dynamic range of about 30dB keeps the IF signal at a constant level in the input of the demodulator.

5. Conclusions

This paper describes a base station design for wireless digital communications at 64 kbps. Uplink and downlink channel equalization is performed at the base station through spread spectrum and precoding respectively. A digital signal microprocessor deals with channel parameter estimation. QPSK modulation scheme has been used in both base and mobile stations. Transmiter and receiver RF stages have been carefully designed. Channel coding will be included in the base station. Final tests have been carried out on the system.

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