Bandwidth Aspects in Second Generation Current Conveyors

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Abstract. This paper discusses bandwidth problems associated with second–generation current conveyors (CCII). In particular, our work is centered in high-capacitance applications, and has been oriented for wireless optical links and applied physics. We discuss techniques for improving bandwidth in these CCIIs, and develop a new CCII structure with larger bandwidth than traditional circuits. These circuits are then compared in terms of their noise and dynamic range characteristics. A test circuit was developed to verify these different bandwidth behaviors.

1. Introduction

Optical sensors are currently an area where increasing bandwidths are sought, in applications such as wireless communications (both LANs and line-of-sight links) and physics particle detection (imaging devices, e.g.). Traditionally, the optical interface in these systems is composed of a photo-detector (PD) and a transimpedance amplifier, a topology preferred by their global compromise between bandwidth and gain. Increasing the bandwidth in a transimpedance amplifier is not easy to accomplish with large PDs. Several factors contribute to this difficulty: 1) the amplifier input impedance, together with the large intrinsic PD capacitance (which is generally imposed by optical signal level considerations), set a dominant pole on the system bandwidth; 2) the high transimpedance gains (required for high sensitivity) limit the maximum achievable input dynamic range, placing strong restrictions on the detected signals; 3) system noise places a lower bound to input signal levels, and constrains both input dynamic range and system bandwidth: decreasing system noise with increasing system bandwidth is, in general, an unfeasible task to accomplish. As a net result, given a specific PD, compromises between gain, bandwidth, input dynamic range and noise, are usually required [1].

In the last years, current-mode techniques have proved to be adequate to the design of systems with wide-gain bandwidth products ([2, 3, 4]). In particular, second generation current conveyors make possible the implementation of arbitrarily small input impedances [6, 7]. Decreasing the amplifier input impedance seems to be a necessary step to increase bandwidth in systems with low cost optical sensors. The product of the PD (large) intrinsic capacitance and the (traditionally large) front-end input impedance establishes a dominant pole in most optical transimpedance front-ends [5]. As the PD is generally defined by global system requirements, it becomes crucial minimizing this front-end input impedance. A differential current buffer for optical wireless applications, based on this strategy was already presented in [4]. It was also shown in [4] that this buffer could provide a 30% increase in system bandwidth when placed between the photo-detector and the amplifier - even without a custom-designed transimpedance amplifier.

In this paper we discuss in section 2 critical factors affecting bandwidth improvement in current techniques applied to photodiode-based applications. These current circuits are seen as buffer interfaces between the optical transducer and simple transimpedance amplifiers. In section 3, we

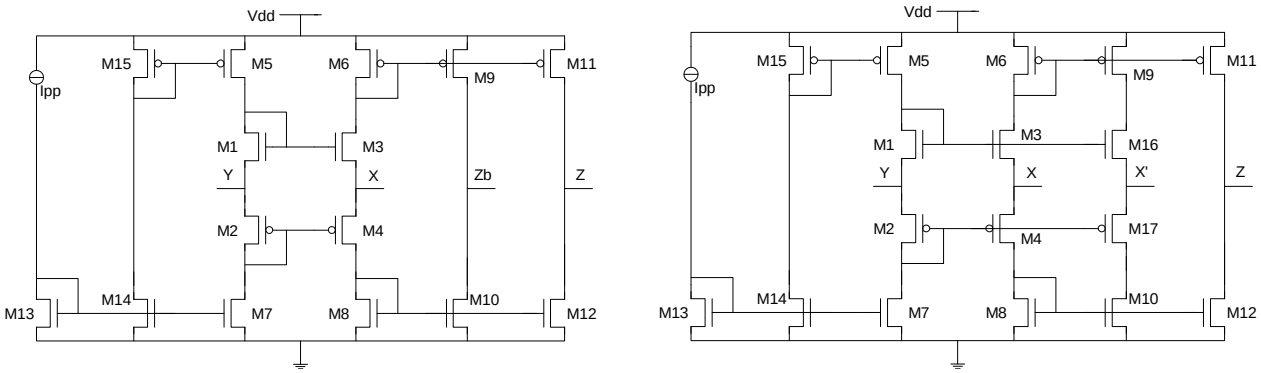

Fig. 1 Second-generation current conveyors: a) traditional version, b) bandwidth enhanced version

propose some modifications on traditional class AB current conveyors ([8, 9]), which associated with the technique referred in [6], provide a better frequency behavior of these current circuits in optical systems. Some guidelines regarding bandwidth, current gains and equivalent input noise are also drawn, and circuit optimization for large bandwidth applications are discussed on section 4, based on simulations. Section 5 shows experimental results of a test chip produced, and the conclusions are presented in Section 6.

2. CCII: Frequency performance

The input impedance of optical wireless interfaces has to be extremely low for high bandwidth systems. Second generation current conveyors (CCII) appear in this context as optimal candidates, since it is well known that its input impedance can be reduced using techniques such as [6]. Thus CCII seemed to be adequate as input current amplifiers for optical-sensors systems. However, high-frequency effects in CCII pose specific problems for system performance in our target applications, which could impair its usage.

Traditional CCII structures may be designed in several different forms. The typical approach over the literature uses differential pairs configured as unit gain amplifiers. This approach exhibits small bandwidths due to the use of differential pairs, and thus is completely unsuitable for our purposes. One other approach reported, with somewhat larger bandwidths, employs current mirrors; unfortunately, this technique produces CCIIs with restricted input dynamic ranges and poor noise performance. Thus for our target applications we used CCIIs based on another technique, a translinear loop (Fig. 1a). This approach seems to be able to produce satisfactory results on all critical aspects for our target applications: large bandwidths associated with good dynamic range and noise performance.

2.1 CCII characteristics

A second generation current conveyor (Fig. 2) can be adequately described by the following equation:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} g_y & 0 & 0 \\ A_v & r_x & 0 \\ 0 & A_i & g_z \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \qquad (1)$$

The elements inside the system matrix represent the relevant parameters of the current conveyor, which are frequency dependent. A_v represents the voltage gain between the input nodes X and Y; A_i represents the current gain between the X input and one generic Z output. In order to include both the effect of the inputs (X and Y) and the output (Z), the system matrix takes into account the impedances (admittances) at port X, Y and Z. Although the system matrix can be considered to consist ideally of two nonzero parameters only (A_v and A_i), and the impedance (r_x) and admittances (g_y, g_z) values are usually very low, their frequency dependency requires them to be taken into account for high frequency analysis.

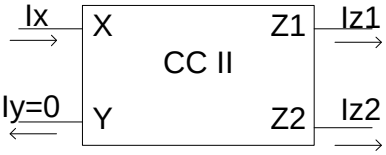

Fig. 2. Second generation Current Conveyor

2.2 Input impedance control

CCII input impedance can be controlled by the circuit depicted in figure 3 (this figure also includes models for the input PD parasitic capacitance and the current conveyor load). Z_b is a dummy output with characteristics identical to the Z output. The conveyor terminals Y and Z_b have been connected to a control resistance (R_{comp}), grounded to a fixed potential. This feedback scheme promotes a decrease in the input impedance viewed at terminal X [6]. When this scheme is applied, the effective input impedance at terminal X, using equation 1, is given by:

$$r_{xcomp} = r_x - \frac{A_v A_i R_{comp}}{1+\left(g_y + g_z\right) R_{comp}} \qquad (2)$$

Equation 2 shows that it is possible to reduce the effective input impedance to arbitrarily small values with this feedback scheme. Considering voltage and current gains near unity, a value of R_{comp} near r_x makes possible to synthesize a zero input impedance. However the non-ideal high frequency behaviour of the conveyor makes these matrix parameters frequency-dependent, creating complex input impedances. This frequency dependency may create two undesirable behaviours: oscillations or current gain peaking. Both effects are related with the input impedance peaking (r_x) at high frequencies.

2.3 Measuring the system bandwidth

When using a traditional CCII (depicted in Fig. 1a) as a current buffer, its bandwidth suffers severe restrictions imposed by the PD intrinsic capacitance (seen in the left side of Fig. 3). From a modelling point-of-view, this intrinsic capacitance removes part of the converted photocurrent from the CCII input. For large values of the intrinsic capacitance (low-cost PDs) this imposes a system bandwidth limitation; however, for small values of the same capacitance, tuning effects may appear that promote small increases in system bandwidth. This tuning effect is due to the complex nature of the CCII input impedance.

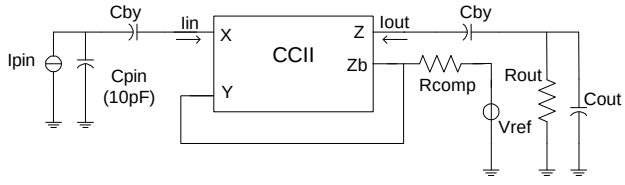

Fig. 3. CCII current amplifier

A clear distinction must be made between system bandwidth and CCII bandwidth. Figure 4 shows the frequency response of an amplifier using the traditional CCII in Fig. 1a) with a compensation resistance R_{comp} of 400Ω. This figure shows the achieved bandwidth without the presence of the intrinsic PD capacitance. These results show a current gain near unity over a bandwidth of 550MHz, while the input impedance was near 90Ω with a peaking behavior for frequencies larger than 1GHz. (This peaking behavior illustrates that r_{xcomp} has to be modeled as an impedance). This result can be obtained in a similar manner if we measure the amplifier transfer function, that is, observing the ratio between output current I_{out}, and the amplifier input current I_{in}.

However when using a PD at the input of the CCII it is advisable to observe the system's bandwidth instead. This bandwidth can be measured taking the transfer function as the ratio between the output current I_{out}, and the PD current I_{pin}. This is the

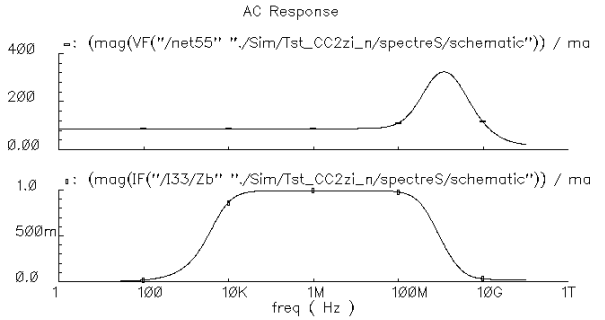

Fig. 4 Amplifier's frequency response: current gain (bottom), input impedance (top)

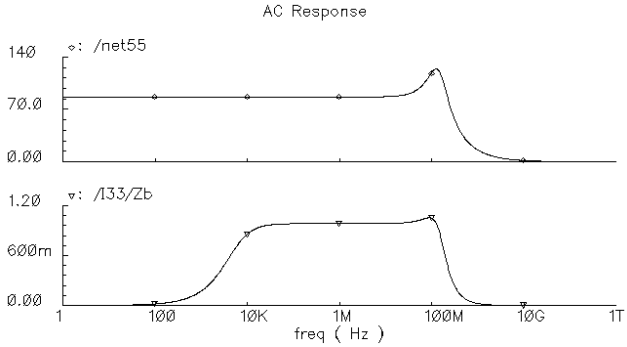

Fig. 5 System's frequency response: input impedance (bottom), current gain (top)

important parameter for performance analysis, as the other value is unrealistic (note that even with input current sources other than PDs, parasitic elements will always be present at the input of the CCII). Figure 5 shows this simulated system's frequency response. The measured bandwidth was of 175MHz (about half the previous value!), with a similar input impedance near 90Ω, but now showing a peaking behavior for frequencies of 130MHz (when the intrinsic PD capacitance becomes relevant compared with the CCII input impedance).

As we shall discuss later, larger bandwidths can be achieved with both CCIIs depicted in Fig. 1, without redesigning the circuits. In fact bandwidths larger than 600MHz can be achieved even with traditional CCII. The major drawback is that these values occur only for small (below 1pF) and unrealistic values of the intrinsic capacitance.

2.4 Increasing the bandwidth

There are four major limitations on the achievable bandwidth of a current amplifier based on a CCII with this feedback structure: 1) the polarization currents, 2) the transistors themselves, 3) the compensation resistance R_{comp}, 4) and naturally the photo-detector intrinsic capacitance.

The PD intrinsic capacitance is generally a consequence of system requirements (PD, polarisation voltage, area, etc…) and is usually set as low as possible, to support larger bandwidths. Nevertheless it is usually possible to increase its value in order to reduce the amplifier's bandwidth (without the need of changing other parameters in the circuit), if convenient.

The polarization currents on traditional class AB CCII (as those of Fig. 1) can be used to increase or decrease the bandwidth of the amplifier. As the current is increased, bandwidth naturally increases. However, this also affects the input impedance: the input impedance suffers a reduction with this increase, which can eventually lead to oscillatory behaviours. These oscillatory behaviours can be avoided if R_{comp} suffers a small increase (leading to smaller input impedances, as can be deducted from equation 2). These two effects create an optimum value of the polarization current. Above this optimum value, the bandwidth no longer increases with increasing polarisation currents, as some transistors leave their optimum operating region.

Regarding transistor sizing, our studies for maximizing system bandwidth showed that there is an optimum value for the dimensions of the transistors in the CCII. With values above an optimum width W_{opt} for the transistors in the translinear loop (M1 to M4, in both configurations in Fig. 1), the bandwidth is limited by parasitic capacitances, and decreases with increasing dimensions. This value W_{opt} is near 80μm in our target 0.8μm technology. These transistors should also be larger than the transistors in the current mirrors. Furthermore, it was found that the output stage also imposes restrictions on system behaviour at large bandwidths.

3. Bandwidth Enhanced CCIIs

Our studies showed that the frequency-dependent effects of the impedance compensation scheme on the CCIIs could be minimized if the characteristics of the output Z_b and the input X were similar. This scheme applies an effect similar to a reshaping of both the magnitude and the frequency response of the current gain A_i between input X and the dummy output Z_b, and thus allows for increased bandwidths through the "compensation" of the effects of the intrinsic PD capacitance at the input.

We developed a modification on the traditional CCII topology to incorporate this effect, and compared its behaviour with traditional CCIIs. Figure 1 presents the two CCIIs used in this study: the traditional CCII (Fig. 1a) and the proposed modified version (Fig. 1b). Both these structures use the same translinear loop, composed by transistors M1 to M4.

The major difference between the two circuits is the construction of the dummy output (Z_b for the traditional CCII and X' to the modified one). This dummy output is used with a resistance R_{comp} in a feedback configuration (such as depicted on Fig. 3), to implement a means of controlling the input impedance. It is readily seen that the current gain between input X and output Z_b on the traditional CCII can be very different from the gain between input X and output X' on the modified CCII, due to the inclusion of transistors M16 and M17. These new transistors have to be perfectly matched with the transistors on the translinear loop because small

mismatches (in the order of 10%) can cause severe behavior modifications.

3.1 Noise behavior

A previous study [9] states that the equivalent input noise in class AB current conveyors is proportional to the square of the transconductance of the transistors in the current mirrors and inversely proportional to the transconductance of the transistors in the translinear loop. Our simulations lead to the same conclusion. We followed two different strategies for noise minimization: 1) designing the circuit with the aspect ratios of the transistors M1 to M4 superior to the other transistors; 2) decreasing the bias current (I_{pp}). The first strategy is consistent with the ideas stated above, when considering bandwidth maximization aspects. The same is not true for the second strategy; decreasing I_{pp} also decreases the bandwidth, decreasing the total output noise. Our simulations showed also that R_{comp} has an important role in the noise behaviour of the current amplifier. As discussed, R_{comp} can be used as a means to control the bandwidth of the amplifier; this same control is obviously true for noise performance because increasing the bandwidth generally increases rms noise levels.

3.2 Effective input dynamic range

The linear input range in these two CCIIs is determined by the operation of the translinear loop. Writing the loop equations reveals that:

$$\begin{cases} I_{D4} = I_{D3} + I_x \\ V_{gs1} + \left|V_{gs2}\right| = V_{gs3} + \left|V_{gs4}\right| \end{cases} \quad (3)$$

Considering that all transistors operate under the saturation condition, equation 3 can be solved in order to the currents I_{D3} and I_{D4}, resulting:

$$I_{D3,4} = kI_{pp}\left(1 \mp \frac{I_x}{4kI_{pp}}\right)^2 \quad (4)$$

where I_{pp} is the bias current, I_x is the input current at node X and k is an aspect ratio between the dimensions of transistors M1 (M2) and M3 (M4). This result is valid only for values of I_x between $-4kI_{pp}$ and $4kI_{pp}$: these are the maximum values of the input current (in a first approximation) where the amplifier maintains a linear gain dependence on the input current. Equation 4 states that it is possible to control the input dynamic range through a rescaling in the transistors of the translinear loop. Still, as our target applications do not require linearity (they are mainly related with pulse detection), our effective dynamic range is larger.

4. Simulation Results

In our simulations we used a reference set-up consisting of two current amplifiers: i) the first using the traditional CCII presented in figure 1a), ii) the second using the modified CCII of figure 1b). Multiple design aspects were analysed: the effect of R_{comp}, the transistor ratios, the bias current, and the intrinsic photo-detector junction capacitance.

The results shown use the suffix ‘a’ for the first configuration and ‘b’ for the second. Both circuits were designed in a 0.8µm double-poly, double-metal technology to meet a compromise between bandwidth, noise and power consumption, optimised for optical pulse detection. All the NMOS transistors have parameterised ratios W/L of W2/1.2µm, except M1 and M3 that were designed with a parameterised ratio of W1/1.2µm. The default values were 70µm (W1) and 20µm (W2). All the PMOS transistors have aspect ratios 1.4 times larger than the NMOS devices.

Both circuits were simulated with a PD with an intrinsic capacitance of Cpin, with 10pF as default (low-cost, large area photodiodes). The output load was a parallel association of a 50Ω resistor with a 10pF capacitance, much larger than required if further signal amplification is performed. The polarization current I_{pp} had a default value of 600µA. Two 1nF capacitors (C_{by}) are used for offset input current cancellation and flicker noise reduction. Finally, R_{comp} was always optimized in order to allow a peaking of 5% in the system’s current gain frequency response; this is the default value for each configuration (220Ω for the traditional CCII and 390 Ω for the enhanced version). For graphical simplicity, only simulations with typical parameters are shown.

Figures 6 and 7 show the expected variations of the bandwidth and the input impedance of the amplifier, using as control parameter the resistance R_{comp}. Figure 6 shows that, with the reference set-up, the modified CCII can attain larger bandwidths than

the traditional structure. Figure 7 shows that the input impedance can be nullified in both configurations, as stated in section 2.3. An interesting result is the possibility of generating negative resistances using CCIIs with this impedance control. However, and not showed in these graphics, the frequency response of the current gain presents large overshoots for values of R_{comp} near the CCII's X input impedance (without feedback). In these situations the system oscillates and the "predicted bandwidths" are not attainable. This is the reason we have limited our "optimum" frequency response values to situations where the maximum overshoot was 5%. In practice, with positive input impedances, the modified CCII presents always better bandwidths (almost 30% better) than the traditional design.

Figures 8 and 9 illustrate the effect of transistor sizing on the maximum achievable bandwidth (using the 5% overshoot constraint!). Once more we can conclude that our proposed CCII permits larger bandwidths. We conducted two different studies: i) the sizing of the transistors in the translinear loop (modeled by W1); ii) the sizing of the transistors on the current mirrors and output stage (modeled by W2). Special care must be taken when varying W2, because these transistors have great influence on the noise performance (see Fig. 12 below). Optimum design value for W2 is near 20μm (Figure 8). This is especially important in the modified configuration, where the frequency compensation-effects are more relevant for circuit performance. On the other side, we confirmed that, after a given maximum value, sizing W1 (Figure 9) affects principally the input dynamic range, particularly if some design ratio is introduced (as discussed on section 3.2).

Figure 10 shows the effect of the polarization current I_{pp} over the maximum achievable bandwidth.

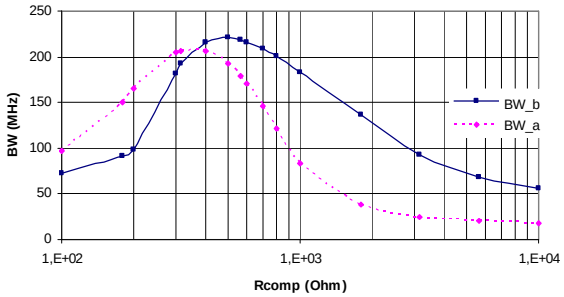

Fig. 6. Bandwidth versus R_{comp}

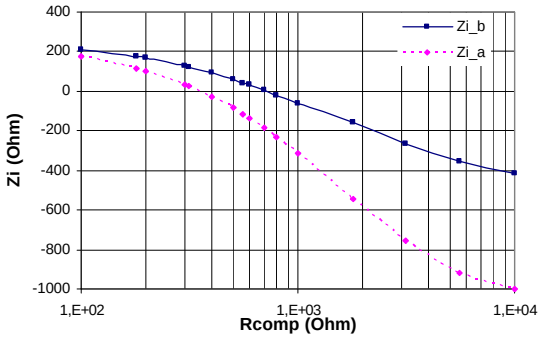

Fig. 7. Input impedance versus R_{comp}

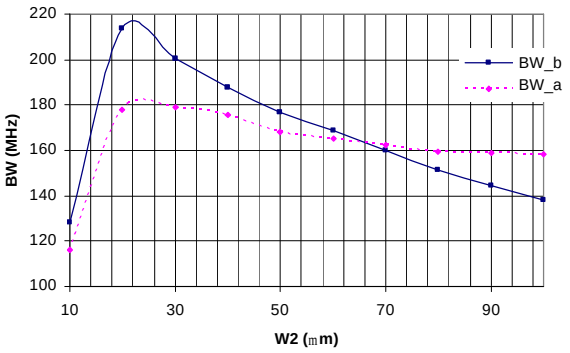

Fig. 8. Bandwidth versus W2

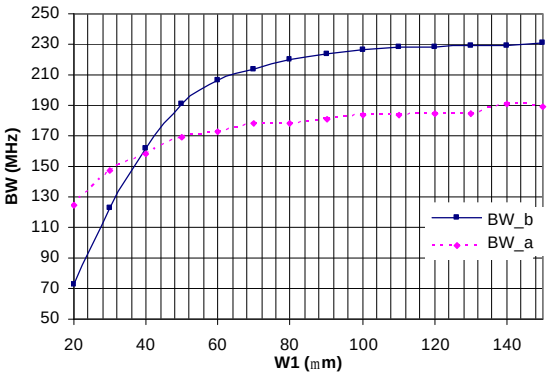

Fig. 9. Bandwidth versus W1

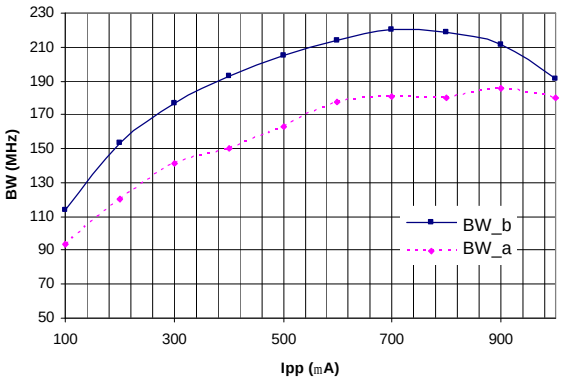

Fig. 10. Bandwidth versus I_{pp}

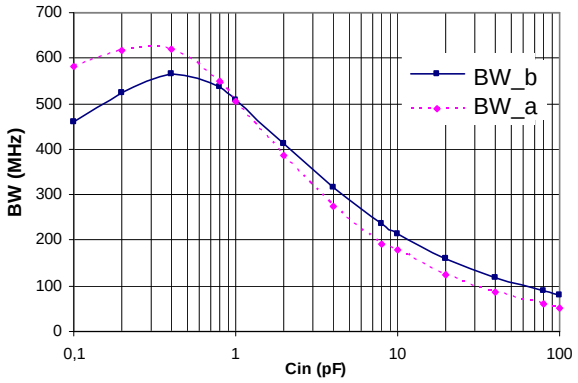

Fig. 11. Bandwidth versus C_{pin}

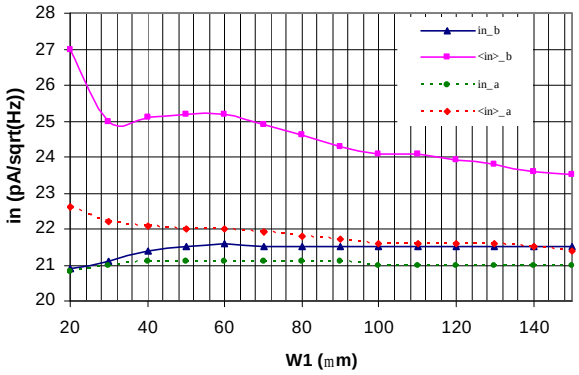

Fig. 13. Noise versus W1

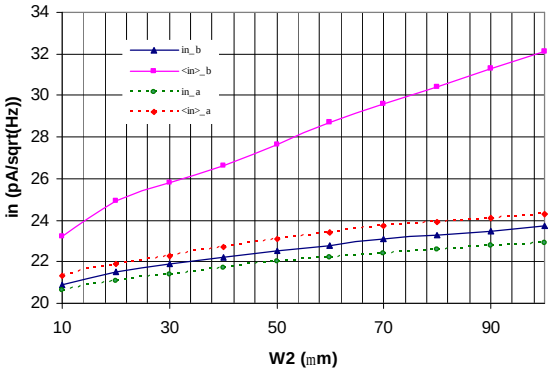

Fig. 12. Noise versus W2

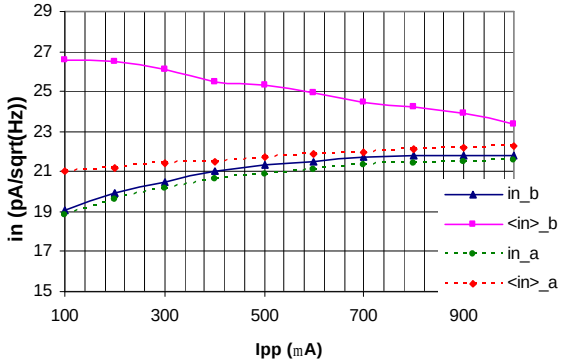

Fig. 14. Noise versus Ipp

For the simulated I_{pp} values the modified CCII always exhibits larger bandwidths than the traditional CCII. The optimum value for the polarization current was near 700µA, which motivated our smaller default value of 600µA. This simulation allows the definition of maximum "useful" power consumption in the CCII.

Figure 11 shows the effect of the PD intrinsic capacitance over the maximum achievable bandwidth. The effect of this capacitance on the maximum achievable bandwidth is different for smaller values than for larger values (typically around 1pF). For large values of the intrinsic capacitance (above 1pF) the bandwidth decreases as expected: this suggests that the time constant created by this capacitance and the input impedance of the amplifier plays a significant role on the system bandwidth. However for values below 1pF the system bandwidth exhibits larger values than the obtained for the amplifier without this capacitance, suggesting a tuning effect between this capacitance and the amplifier input impedance. This tuning effect is more pronounced on the amplifier using the traditional CCII; in fact, with this structure, values of 620MHz for the maximum achievable bandwidth can be reached without oscillations. For our target applications the realistic intrinsic capacitances are far above 1pF (this is a typical input pad capacitance!) so we can conclude that our modified CCII shows better bandwidth performance in our applications.

Another design challenge in these circuits is the noise minimization problem. The noise behavior of the amplifier imposes a lower bound on the input dynamic range. Several simulations were carried out in order to confirm the design guides discussed on section 3.1. Figures 12, 13 and 14 show the system noise, when the design parameters W2, W1 and I_{pp} are varied from the default values. These graphics show, for the two CCII structures, both the minimum input equivalent noise current observed (in_x) and the medium value of the same current inside a test bandwidth, (<in>_x) (This bandwidth was taken as 2MHz to 70MHz for the modified CCII and 2MHz to 50Mhz for the traditional CCII).

Our total simulation results show that minimizing

noise in these CCII can be accomplished by: i) increasing W1 (the sizes of the transistors in the translinear loop); ii) reducing W2 (the size of the transistors in the current mirrors and output stage; iii) reducing the polarization current I_{pp}. These results support also the conclusion that minimizing noise and maximizing the system's bandwidth are in general two exclusive tasks to accomplish. Another important conclusion is that the noise performance of the amplifier with the traditional CCII exhibits slightly better results than our proposed CCII, mainly due to smaller bandwidths.

5. Test Circuit Results

We implemented the two current conveyor topologies (the traditional version and our improved version) in a typical double-metal, double-poly, 0.8µm CMOS technology, in order to confront their relative performance with the expected results presented in section 4. Both current conveyors were designed with the reference values discussed in section 4, with W1 = 70µm and W2 = 40µm. Other NMOS transistors had a width of 20µm, and the PMOS transistors have always a design ratio 1.4 larger than the NMOS. All transistors had a 1.2 µm length. The current conveyors were followed by a set of current mirrors [10] at the outputs, able to provide a total gain of 6dB, through proper mixing of currents. Notice that the layout of these circuits (in particular the bandwidth-improved version) was critical. Besides the matching requirements already mentioned, the parasitic capacitances imposed by the interconnecting lines of transistors M16-17 in the bandwidth-improved CCII had a non-neglectable impact on its bandwidth.

The circuits were designed targeting wireless optical applications [1], and as such, for operation with input capacitances above 10pF. Target input currents would be on the 10nA-10µA range, with polarisation currents around the 500µA range.

Tests were made using a Network Analyser (HP4195A), with a voltage to input conversion (by a 10KΩ resistor) at the input of the circuit. The test circuit follows closely Fig. 3, with 50Ω adaptation at the input and output, and 22nF bypass capacitors. The compensation resistance was variable, and was adjusted to the overshoot criteria discussed before

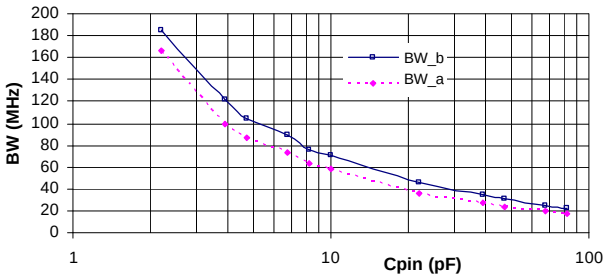

Fig. 15. .Measured bandwidth versus C_{in}.

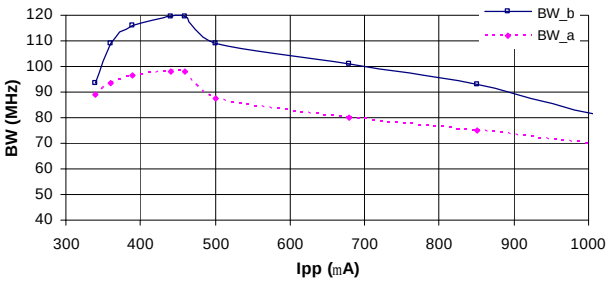

Fig. 16. .Measured bandwidth versus I_{pp}

(typical compensation resistance values would be on the 300Ω range).

Frequency measurements presented some difficulties, due to the low gain, low signal levels and the required voltage to current conversion resistor. At these low signal levels, with the chip packaging used (CLCC), the existence of pass-through signals at the test board level is common, and impaired a simple automated measurement of the frequency response of both circuits. Nevertheless, with prior adequate characterization of all these pass-through effects, we achieved the results presented in Fig. 15 e Fig. 16. (Noise performance was not possible to measure due to these pass-through signal problems on the test board.) A further test problem was the need for adjusting the frequency response peaking at each measure, in order to assure the same conditions for every point measured. This could only be achieved approximately in practice.

The results differed from the simulations, presenting smaller bandwidths. This is not completely unexpected as previous experiences with this technology showed us that "typical" to "slow" behaviour is to be expected. Taking this aspect in consideration, our tests are quite near the simulations, and our modified current conveyor does outperform the traditional CCII.

6. Conclusions

We discussed design guidelines for second generation current conveyors, focusing on bandwidth aspects, but also considering associated dynamic range and noise issues. These design guidelines have been validated by simulation on two different CCII structures, a traditional class AB translinear loop and a proposed bandwidth-improved version of this second-generation current conveyor. We can conclude that this conveyor shows a better control of the input impedance (when configured as a current amplifier between nodes X and Z) than previous high dynamic range proposals, presenting larger bandwidths. It is usually preferable over the traditional structure, and most especially in applications with photo-detectors with large junction capacitance. However this structure presents critical implementation issues, due to matching requirements and parasitic capacitances effects.

A test circuit was also developed to compare frequency behaviours of both current conveyors. The experimental results showed that the proposed modification to the classical CCII does improve its bandwidth for capacitive input loads.

7. References

[1] R.L. Aguiar, A. Tavares, J.L. Cura, E. Vasconcelos, L.N. Alves, R. Valadas, D.M. Santos, "Considerations on the design of transceivers for wireless optical LANs", IEE Electronics & Communications, Colloquium on Optical Wireless Communications, London, England, Jun. 1999.

[2] T. Ruotsalainen, P. Palojärvi, J. Kostamovaara, " A Current-Mode Gain-Control Scheme with Constant Bandwidth and Propagation Delay for a Transimpedance Preamplifier", IEEE Journal of Solid State Circuits, Vol. 34, February 1999.

[3] C.H. Lee, J. Cornish, K. McClellan, J. Choma Jr., "Current-Mode Approach for Wide-Gain Bandwidth Product Architecture", IEEE Trans. Cir. Sys. II, Vol. 45, May 1998.

[4] L.N. Alves, R.L. Aguiar, "A Differential Current-Conveyor Based Buffer for High-Bandwidth Low-Signal Applications", ICECS99, Paphos, Cyprus, Sep. 1999.

[5] E. de Vasconcelos, J.L. Cura, R.L. Aguiar, D.M. Santos, "A Novel High-Gain, High-Bandwidth CMOS Differential Front-End for Wireless Optical Systems", ISCAS99 Orlando, Florida, May 1999.

[6] G. Palumbo, S. Pennisi, "A Technique for the Reduction of the Input Resistance of Current-Mode Circuits, ISCAS98 Monterey, Florida, May 1998.

[7] Fabre, H. Barthelemy, "Composite Second-Generation Current Conveyor With Reduced Parasitic Resistance", IEE Electronics Letters, Vol. 30, Mar. 1994.

[8] T. Kurashina, S. Ogawa, K. Watanabe, " A High Performance Class AB Current Conveyor", ISCAS98 Monterey, Florida, May 1998.

[9] E. Bruun, "Noise Properties of CMOS Current Conveyors", ISCAS96, Atlanta, May 1996.

[10] Luís Nero Alves, Rui L. Aguiar, "Maximizing Bandwidth in CCII for Wireless Optical Applications", ICECS'2001, 8th IEEE Conference on Electronics, Circuits and System, Malta, Sep 2001.