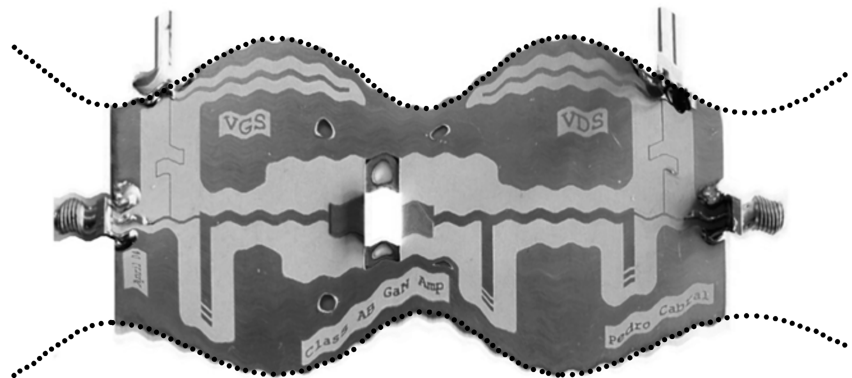
Universidade de Aveiro Departamento de Electrónica, Telecomunicações e Informática
2006

Pedro Miguel da Silva Cabral

Modelação Não-Linear de Transístores de Potência para RF e Microondas



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Pedro Miguel da Silva Cabral

Modelação Não-Linear de Transístores de Potência para RF e Microondas

Nonlinear Modelling of Power Transistors for RF and Microwaves

tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Dr. José Carlos Pedro, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e sob a co-orientação científica do Dr. Nuno Borges Carvalho, Professor Associado do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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palavras-chave

Amplificadores de Potência, Modelação Não-Linear, Modelo de Circuito Equivalente, Nitreto de Gálio, Rádio Frequência.

resumo

Esta tese insere-se na área de electrónica de rádio-frequência e microondas e visa a formulação, extracção e validação de um modelo não-linear de transístores de elevada mobilidade electrónica (HEMT), baseados na tecnologia emergente de Nitreto de Gálio (GaN).

Nos últimos anos, tem-se assistido a um rápido desenvolvimento de tecnologias de semicondutores capazes de restringir, ainda mais, o domínio dos tubos de vazio. Em particular, nos sistemas de telecomunicações, tem-se procurado substituir os amplificadores a TWT por amplificadores do estado sólido capazes de oferecer características competitivas de frequência de operação, potência de saída, rendimento e linearidade.

Neste sentido, a muito recente utilização de novas ligas semicondutoras, como é o caso do GaN, parece ser bastante promissora, já que combina uma elevada banda proibida com uma também elevada mobilidade electrónica. Se a primeira característica é essencial a uma tensão de disrupção elevada, e, consequentemente, grande capacidade de potência por unidade de área, a segunda é fundamental na extensão da frequência de operação. Espera-se, por isso, que, nos anos mais próximos, transístores de GaN venham a desempenhar papel determinante na amplificação de potência de RF e microondas.

No entanto, para que isso seja possível, é necessário dispor de um conhecimento preciso da tecnologia e, assim, de modelos matemáticos dos dispositivos, actividades que só agora estão a dar os primeiros passos.

Esta tese visa a obtenção de uma topologia de circuito equivalente de transístores HEMT a GaN encapsulados seguida pela extracção dos valores dos elementos deste modelo para uma fina rede de pontos de repouso. Passar-se-á então ao estudo das características DC e AC de sinal forte (em especial de distorção harmónica), formulando descrições funcionais convenientes para a corrente e carga acumulada no canal em função das tensões aplicadas. Tal modelo, servirá para estudar os efeitos de memória provocados pela malhas de adaptação e polarização empregues em circuitos deste género.

O modelo será validado pelo projecto e teste de um amplificador de potência de microondas que, para além da validação do modelo não-linear, proporcionará, ainda, uma antevisão das reais capacidades deste tipo de dispositivos a nível do compromisso entre rendimento e linearidade.

keywords

Equivalent Circuit Model, Gallium Nitrade, Nonlinear Modelling, Power Amplifiers, Radio Frequency.

abstract

This thesis belongs in the radio frequency and microwave electronics area and is intended to formulate, extract and validate a nonlinear model of high electron mobility transistors (HEMT), based on the Gallium Nitride (GaN) emerging semiconductor technology.

In the past few years, we have seen a fast development of new semiconductors capable of further reducing the use of the bulky, expensive and inefficient vacuum tubes. The idea is to replace the old TWT amplifiers by solid-state devices providing competitive performance figures of operation frequency, output power, power added efficiency and linearity.

It seems particularly promising the use of new semiconductor compounds as GaN, since it combines very wide bandgap with also surprisingly high electron mobility. If the former is determinant to the offered breakdown voltage, and thus to the available output power capabilities, the latter is fundamental to get reasonable amounts of gain at very high frequencies. Therefore, the scientific community is expecting that those transistors will play a significant role in RF and microwave power amplifier applications.

However, to make this dream a reality, it is of paramount importance that the technology is precisely known, and so that accurate nonlinear models for those devices are proposed, scientific activities which are just now taking the first steps.

This thesis aims at proposing an appropriate equivalent circuit model topology for encapsulated GaN HEMTs. Then, the element values of this small signal equivalent circuit will be extracted for a fine grid of quiescent points.

Afterwards, the devices' DC and large-signal AC data (obtained via harmonic distortion measurements) will be studied in order to produce convenient nonlinear descriptions of the FET's channel current and accumulated charge as a function of the applied voltages. The model will be applied to study the memory effects due to matching networks and bias circuitry expected to impair the linearity of GaN amplifier circuits.

This GaN HEMT nonlinear model will be validated by the design and test of a microwave power amplifier that, beyond the model validation, will provide a first preview of the real capabilities that these devices can offer in terms of the crucial compromise between power added efficiency and linearity.

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List of Acronyms

ac	Alternating Current
AlGaN/GaN	Aluminium Gallium Nitride/Gallium Nitride
AM	Amplitude Modulation
AM/AM	Amplitude Modulation to Amplitude Modulation
AM/PM	Amplitude Modulation to Phase Modulation
PM	Phase Modulation
BJT	Bipolar Junction Transistor
Bw	Bandwidth
CAD	Computer Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
CW	Continuous Wave
dc	Direct Current
DUT	Device Under Test
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSM	Global System for Mobile Communications
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFET	Heterojunction FET
IM3	3rd Order IMD
IMD	Intermodulation Distortion
IMR	Intermodulation Distortion Ratio
IR	Impuslse Response
IV	Current-Voltage
JFET	Junction Transistor
LDMOS	Laterally-Diffused MOSFET
LED	Light Emmiting Diode
LNA	Low Noise Amplifier

ME	Memory Effects
MESFET	Metal Semiconductor Field-Effect Transistor
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NLTF	Nonlinear Transfer Function
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
Pin	Input Power
Pout	Output Power
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
SDD	Symbolic Defined Device
Si	Silicon
SiC	Silicon Carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
TF	Transfer Function
VNA	Vector Network Analyser
VSA	Vector Signal Analyser
VHF	Very High Frequency
W-CDMA	Wideband Code Division Multiple Access

1. Introduction

The electronics era started with scientists like Maxwell, Hertz, Faraday, and Edison, in the 1800's, when the control of electricity was made possible. After that, and until today, there has been an unprecedented set of discoveries that is yet to finish.

So, let us start in the beginning of the twentieth century when, in 1904, based on the work of Thomas Edison, sir John Ambrose Fleming invented the thermionic valve, or diode. Three years later, in 1907, Lee De Forest filed in a patent on a triode vacuum tube, the first electronic device capable of amplification.

However, the most important achievement was still to come. Only in 1947, John Bardeen, Walter Brattain and William Shockley discovered the transistor effect and developed the first device at Bell Laboratories.

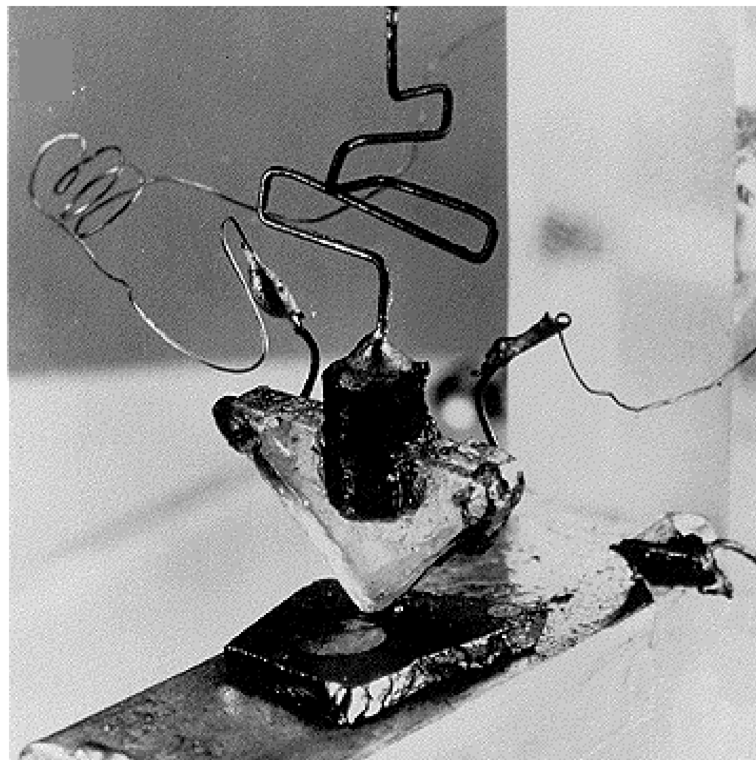

Fig. 1. Photograph of the first working transistor replica.

A generic name for the new invention was needed: "Semiconductor Triode", "Solid Triode", "Surface States Triode", "Crystal Triode" and "Iotatron" were all considered, but "Transistor" won the Bell Laboratories internal voting. The following extract of the company's Technical Memoranda, calling for votes, explains the reasons for the chosen name.

Transistor. This is an abbreviated combination of the words "transconductance" or "transfer", and "varistor". The device logically belongs in the varistor family, and has the transconductance or transfer impedance of a device having gain, so that this combination is descriptive.

Fig. 2. Extract of the Bell Telephone Laboratories Technical Memorandum, [1].

The importance of this work was proved, in November 1956, with the attribution of the physics Nobel Prize to those three men. Bardeen would go on to win a second Nobel in physics, one of only two people to receive more than one in the same discipline, for his work on the exploration of superconductivity.

Later, from 1948 until 1951, William Schockley, at Bell Labs, conceived and presented the first working junction field effect transistor (JFET).

The metal-oxide semiconductor field-effect transistor (MOSFET) was invented, in 1962, by Steven Hofstein and Fredderic Heinman, at Princeton. Although slower than the bipolar junction transistor (BJT), a MOSFET was smaller, cheaper and used less power.

In the 1970s, the introduction of gallium arsenide (GaAs) metal semiconductor field-effect transistors (MESFETs) revolutionized the radio frequency (RF) and microwave market. GaAs monolithic microwave integrated circuits (MMICs) brought integration capability.

In the 1980s, the complementary metal-oxide semiconductor (CMOS) field effect transistor (FET) started to have a significant impact on the electronics field. Today, the advancement of CMOS has made it competitive with bipolar technology. Nowadays, silicon laterally diffused MOS (LDMOS) devices are used in power amplifiers for Global System for Mobile Communications (GSM) base stations.

In the 1990s a variety of new solid-state devices, including high-electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) were introduced.

Many advances on design and power amplifier active device technology have been made public. In this respect, and despite of its recognized device processing infancy, one of the most promising technologies is the one based on wide bandgap materials, like Gallium Nitride (GaN), already exceeding the best results reported by many other materials.

The study of wide bandgap semiconductors started over 30 years ago. However, only in the late 1980s, for Silicon Carbide (SiC), and in the mid-1990s, for GaN, occurred significant breakthroughs. The first commercial applications were blue Light Emitting Diodes (LEDs) fabricated from SiC, and later from GaN-related materials. The first GaN metal semiconductor field-effect transistor (MESFET) was only reported in 1993 [2], and the first Aluminium Gallium Nitride/Gallium Nitride (AlGaN/GaN) HEMT one year later, [3].

Nowadays, there is a very wide range of application fields for GaN that goes from Power Management to Military and Medical fields. Fig. 3 presents some of those applications.

Fig. 3. Examples of GaN application fields.

Table 1 presents a summary of relevant semiconductor material properties to the electronic device performance for Silicon (Si), GaAs, SiC and GaN [4-8].

Table 1. Material properties for several semiconductors.

Property	Units	Si	GaAs	SiC	GaN
Energy Bandgap Ability to support internal electric fields before breakdown. Determines the upper temperature limit of device operation.	eV	1.1	1.42	3.26	3.49
Critical Electric Field Maximum electric field that can be supported internally to the device before breakdown. Determines the highest operating voltage of a transistor for a given device design and channel doping, and thus limits the RF power swing in the device.	$\times 10^6\ V/cm$	0.3	0.4	3.0	3.0
Dielectric Constant Indication of the capacitive loading of a device affecting the transistor terminal impedance.	-	11.8	12.8	10.0	9.0
Thermal Conductivity Determines the ease with which heat generated from unconverted DC power can be removed from the device.	$W/(cm-K)$	1.5	0.5	4.5	>1.5
Electron Mobility Speed of the electrons in the material under the influence of relatively weak electric fields.	$cm^2/(V\cdot s)$	1500	8500	700	1000-2000
Saturated (peak) Electron Velocity Maximum speed the electrons are capable of reaching under the influence of a relatively strong field.	$\times 10^7\ cm/s$	1.0 (1.0)	1.3 (2.1)	2.0 (2.0)	1.3 (2.1)

The combination of high energy bandgap, high critical electric field, low dielectric constant and high thermal conductivity may ultimately lead to devices, based on wide bandgap materials, capable of handling higher power densities in a more efficient way than devices fabricated from other semiconductor materials. Remarkable results have already been reported. Actually, a Continuous Wave (CW) output power density of 32.2 W/mm, with a power added efficiency (PAE) of 54.8%, at 4 GHz was already obtained, [9]. In addition, the total output power and PAE have continuously increased their figures, as it can be seen in [10-16], where it is possible to find PAs delivering from 100W until 500W, with efficiencies above 45%. Furthermore, noise figures of 0.6dB at 10 GHz have already been reported, [17, 18].

While the impact, of the above studied material properties', on the overall device performance is relatively straightforward, the electron transport characteristics that permit high frequency operation are much more delicate.

The transport of electrons in a semiconductor typically depends on two factors, known as electron mobility and saturation electron velocity. The electron mobility in GaN is better than in SiC but still lower than in GaAs, although the saturated electron velocities are comparable. However, those numbers can be misleading. When AlGaN is grown on top of a layer of a similar crystal, a Heterojunction is formed between the two different crystals, contributing to the GaN's outstanding high frequency characteristics, already presenting devices with cut-off frequencies of hundreds of GHz, [4, 19, 20].

However, there have been many reports of some performance limitations, due to several physical effects associated with the semiconductor material: e.g. current decrease [21], RF stress [22] and premature gain compression [23]. This is mainly due to the material growth immaturity and solutions to these problems are emerging every day.

Different substrates have been used for growing of GaN such as: Sapphire, SiC and Si. Most of the reported work is carried out on sapphire that is relatively cheap, is offered in large diameter wafers and provides an excellent low-loss microwave substrate. However, the thermal conductivity of Sapphire is extremely poor and will severely limit the power density and total power performance of devices fabricated on it. SiC has more promising characteristics in terms of lattice matching and thermal conductivity and is also an excellent microwave substrate, but has some severe disadvantages like cost, wafer size, and material defects. Si substrates offer new possibilities in terms of using large size wafers, maintaining good thermal properties with very low cost [7, 24].

1.1. Motivation

The deployment of modern digital telecommunication systems, with continuously increasing capacity and, using more and more complex modulation schemes, has demanded a steady improvement of the RF front-end's performance. Fig. 4 presents the block diagram of a typical wireless communications receiver link.

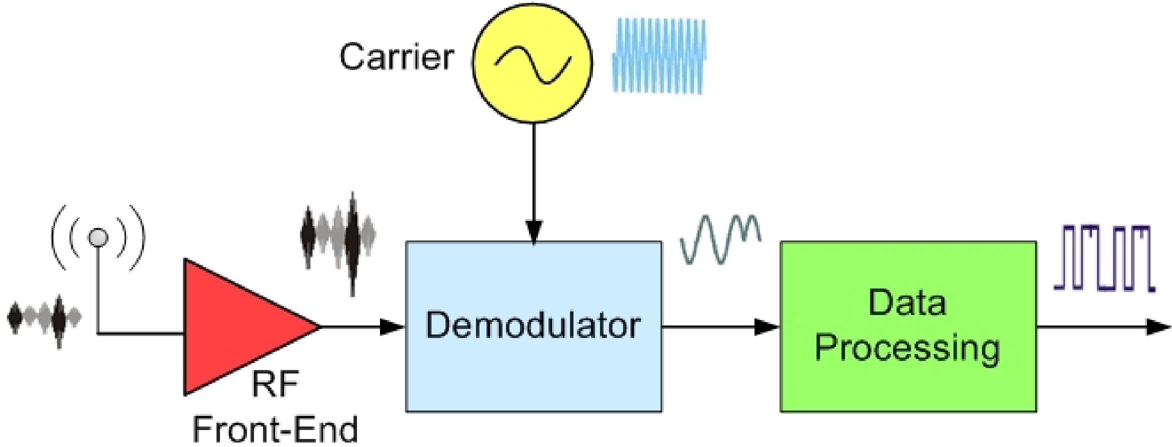

Fig. 4. Block diagram of a typical wireless communications receiver link.

Looking now to the transmitter part of the wireless link, Fig. 5, we can see that power amplifiers (PAs) are the last active blocks in the system, handling the highest levels of RF signal and supply power.

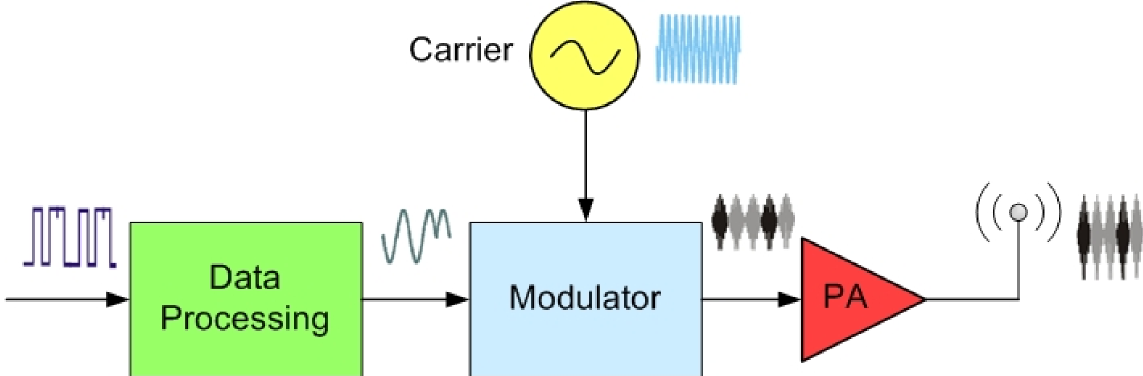

Fig. 5. Block diagram of a typical wireless communications transmitter link.

The PAs' performance is usually evaluated with the help of some figures of merit such as: output power (Pout), gain, PAE, bandwidth (Bw), or even nonlinear distortion. The overall amplifier performance will be a compromise between all the above mentioned parameters. On one hand, if a highly linear performance is desired, the PA has to operate with sufficient power back-off in order to confine the input-signal envelope variation within the region of linear amplification. On the other hand, a highly efficient PA will work in a region where the input-signal envelope's peaks are strongly clipped, thus producing a highly distorted output signal. As a result, there must be a linearity-efficiency trade-off in order to satisfy both requirements.

In what the linearity characteristics are concerned, linearization enforcing techniques relying on either adding external circuitry to the PA, or simply improving its design [25], are necessary. The first set of methods, known as external linearization [26], is illustrated in Fig. 6.

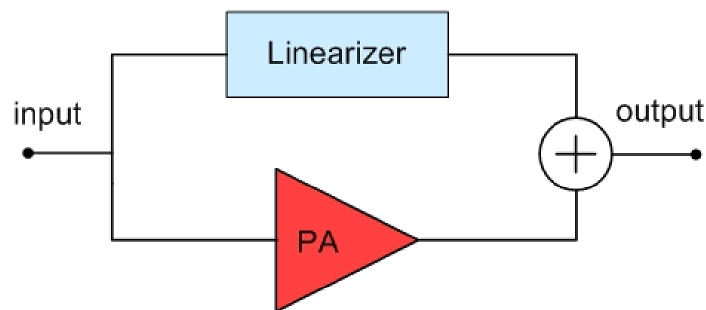

Fig. 6. General external linearization arrangement.

This scheme, although of the feedforward type, presents a general external linearization arrangement that can be applied to any linearization structure (pre- or pos- distortion). In fact, since it is a conceptual diagram, it represents the intermodulation distortion (IMD) compensation between the PA and Linearizer.

External linearization involves several drawbacks like cost, size, effective bandwidth or difficulty of adjustment and can be severely affected by the so-called Memory Effects (MEs). Section 1.1.2 presents a brief introduction to this topic.

In order to circumvent these limitations, there has been a growing interest in directly optimizing the actual PA linearity. One possible way to achieve this design goal is to rely on certain bias points and power operating conditions, the so-called large-signal IMD sweet-spots, which lead to improved intermodulation distortion ratio (IMR) near the zones where the Pout and PAE are maximized [25, 27].

In an IMD versus input power (Pin) plot, they can take many forms from a barely noticeable decrease in the IMD slope to mild valleys or even sharp deeps in the IMD characteristic, see Fig. 7 a, b and c, respectively.

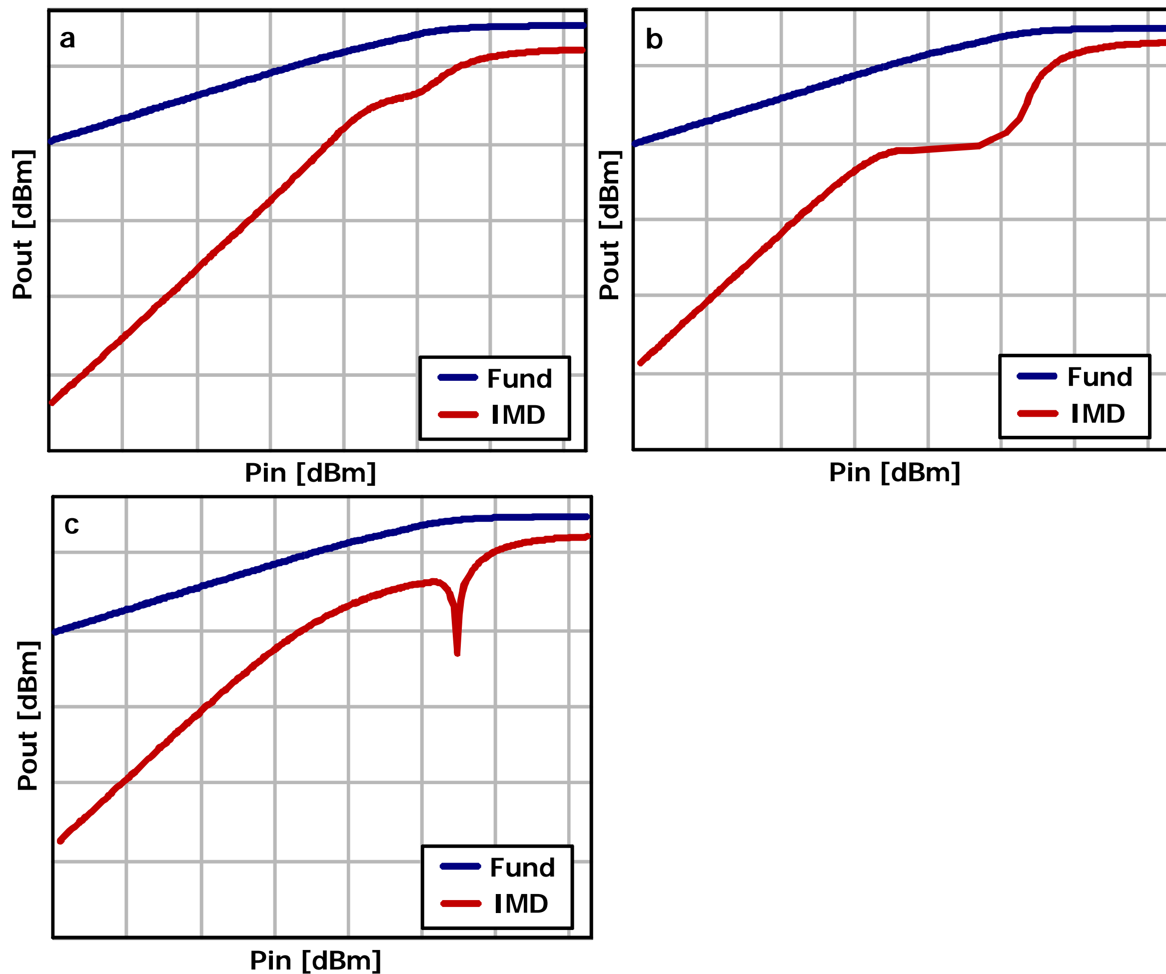

Fig. 7. IMD vs Pin plot with a) barely noticeable decrease in the IMD slope; b) mild valley or c) sharp deep in the IMD characteristic.

Unfortunately, the critical dependence of these IMD valleys on almost unsuspected issues like: out-of-band terminations [28, 29], strong and mild device nonlinearities [25, 27] and quiescent point (not unusually in ranges of only a few tenths of Volt) have raised the needs for high-quality PA design methodologies and nonlinear device models.

Using recent developments in the PA IMD understanding under small- and large-signal regimes, it is possible to conclude that large-signal IMD sweet-spots are not particular to a specific transistor, or PA topology, but are inherent to a large variety of PA circuits and active device technologies. This topic will be studied in more detail in Section 1.1.1.

In what the nonlinear device model is concerned, it is known, from Volterra series analysis, that adjacent channel distortion (see Fig. 8), or close side-band IMD description, over moderate signal levels requires a model capable of accurately reproducing the I/V and Q/V characteristics, at least up to 3rd order. On the other hand, alternate channel distortion level description (see Fig. 8) would need, at least, 5th order detail. In mathematical terms, this implies that 3rd or 5th order derivatives of I/V and Q/V functions must be carefully extracted and modelled.

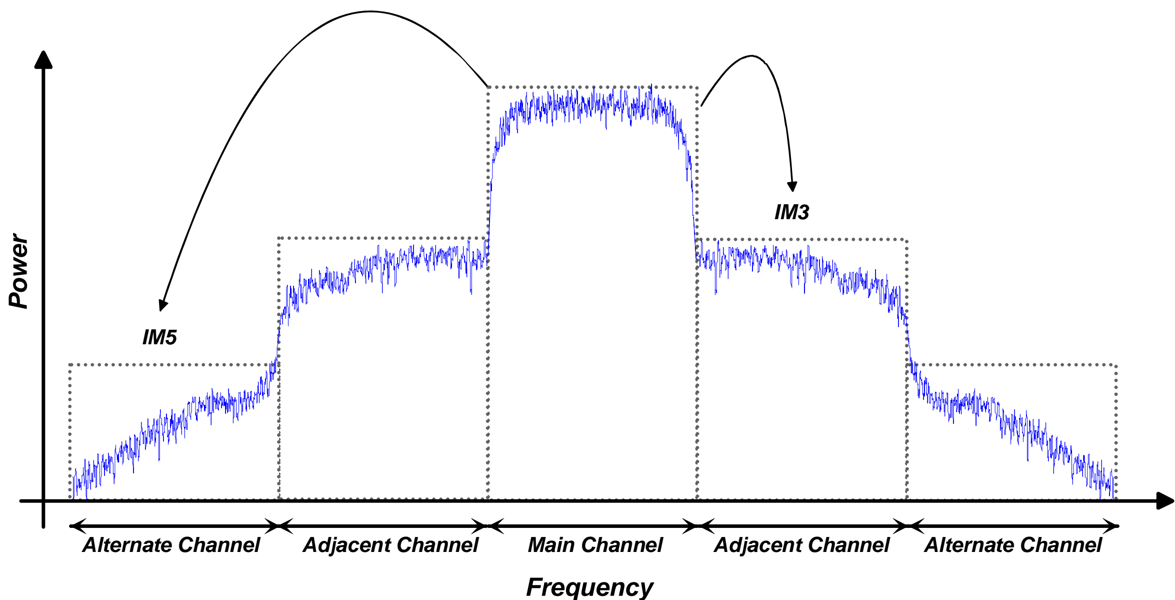

Fig. 8. Off-channel leakage caused by intermodulation due to 3rd and 5th order PA nonlinearity.

Unfortunately, such a local model is not capable of reproducing the full range of large-signal device characteristics. For that, an accurate description of the device's strong nonlinearities like saturation to triode-zone transition, current cut-off, gate-channel diode conduction and gate-channel breakdown are also required. This leads to the necessity of a nonlinear global model.

1.1.1. Self-Linearization Effects in Different PA Technologies

Power amplifier's intermodulation distortion varies dramatically with the amplifier's operation class, traditionally defined with the help of the conduction angle concept, 2θ, expressing the waveform period percentage in which the device is on. This definition is based on an idealized piece-wise linear form of the active device's transfer function (TF), which is the transformation of the known nonlinear bi-dimensional dependence of the output current, $i_O(t)$, on the input and output control voltages, $v_I(t)$ and $v_O(t)$, $i_O[v_I(t), v_O(t)]$, into an one-dimensional model, $i_O[v_I(t)]$, assuming a determined output boundary condition imposed by the load impedance.

Using this traditional conduction angle concept, if $2\theta < 180°$ the amplifier is said to be in class C, if $2\theta = 180°$ it is in class B, if $180° < 2\theta < 360°$ in class AB, and if $2\theta = 360°$ the PA is said to operate in class A, [26]. Besides the typical piece-wise approximation of the active device's TF, Fig. 9 illustrates the input voltage and output current waveforms, for each of the above mentioned operation classes.

As shown in Fig. 9, this traditional conduction angle concept assumes an unsaturated piece-wise approximation to the device's turn-on, defining an ideal threshold voltage, V_T. If $v_I < V_T$ then $i_O = 0$, if $v_I > V_T$, $i_o = G_1 \cdot v_I$, in which G_1 is the device's transconductance, herein assumed independent of bias or excitation amplitude.

Unfortunately, this is an oversimplified model of operation because, as illustrated in Fig. 10, no actual device presents such a discontinuous behaviour (V_T is, in fact, undefined). The assumed linear zone still presents some residual nonlinearity, and can not go on forever, but tends to saturate when v_I looses control over the output current, transferring it to v_O (a FET enters the triode region and a BJT or HBT enters in saturation).

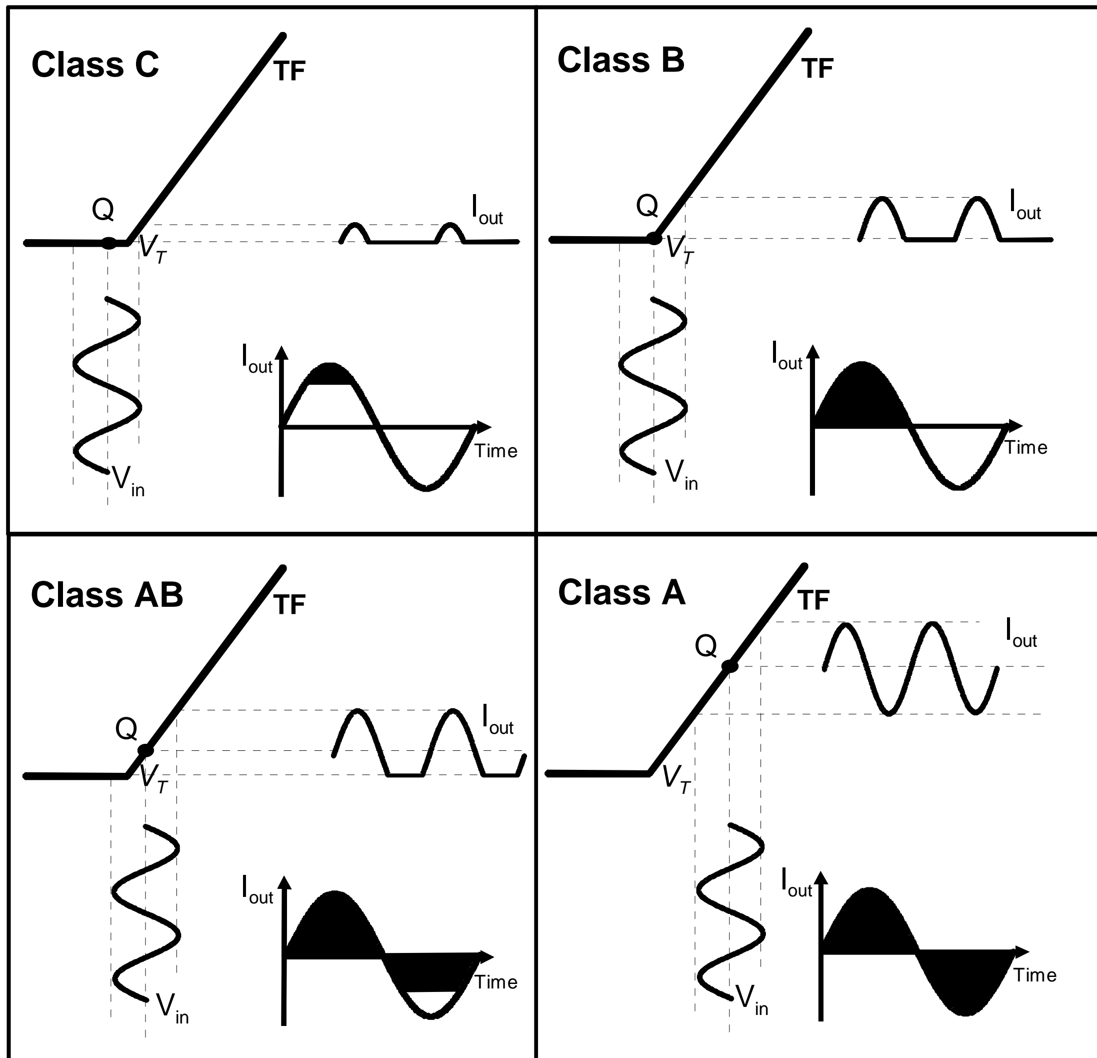

Fig. 9. Typical piece-wise approximation of an active device's TF and corresponding v_{in} and i_{out} for classes C, B, AB and A.

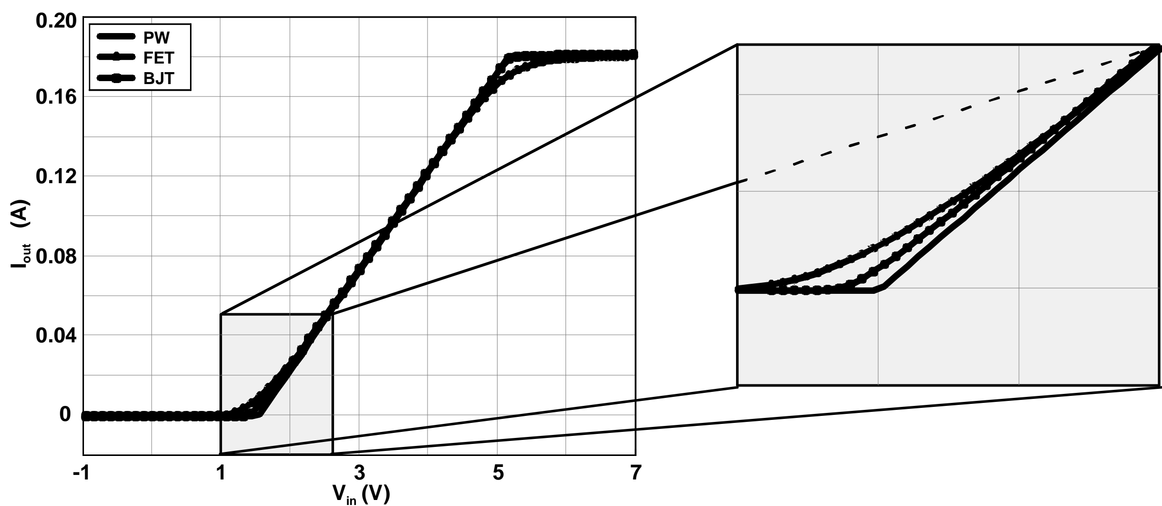

Fig. 10. Typical TF of a FET, a bipolar and their piece-wise approximation, magnified near turn-on.

Therefore, before starting any explanation of the IMD characteristics versus PA operation class, we need to revisit the definition of PA operation regimes, keeping in mind these observed smooth TFs. Indeed, provided saturation of the TF is included, any increase in model detail will not be paid back in terms of the prediction of fundamental Pout or PAE (reason why this model has been left unquestioned for so long); however, only when the TF's soft turn-on is described, it is possible to accurately model IMD. Moreover, despite the variability in nonlinear device models and the levels of detail we are dealing with, a large range of device technologies share a very similar set of IMD characteristics.

So, let us start by comparing the two most important and distinct groups of active device technologies used in nowadays microwave PAs: BJTs and FETs.

If the TF characteristic of a bipolar device were given in terms of the dependence of collector current on base-emitter voltage, $i_C[v_{BE}]$, it would be approximately exponential [30].

This is in contrast with a FET whose drain-source current dependence on gate-source voltage, $i_{DS}[v_{GS}]$, is only approximately exponential in the sub-threshold region, and then shows a quadratic zone near turn-on, which is further linearized due to non-uniform channel doping profile and short-channel effects [31].

However, this situation changes dramatically if the TF of the BJT were not given as $i_C[v_{BE}]$ but as $i_C[v_S]$, where v_S is no longer the intrinsic, but the extrinsic base-emitter control voltage. Because the voltage drop in the total series resistance of the base-emitter mesh (both base and emitter parasitic resistances and input generator internal impedance) is proportional to base current (also an exponential function of intrinsic v_{BE}), the overall effect is an exponential TF near turn-on followed by a linearized characteristic imposed by the series resistance [25], which is much more similar to the FET's TF.

In fact, as illustrated in Fig. 10, the resemblance between the TF curves originated from FETs or BJT devices is so evident that they can be approximated by the same global equivalent model.

In order to obtain an unambiguous and consistent definition of the various PA operation classes, we will use a low order Volterra series of the output current of an active device, or its memoryless subset, the Taylor series:

$$I_{out}\left[v_{in}(t)\right] = I_{out\ DC} + G \cdot v_{in}(t) + G_2 \cdot v_{in}(t)^2 + G_3 \cdot v_{in}(t)^3 + \ldots \qquad (1)$$

Fig. 11 presents the variation of these three small-signal coefficients, with bias point, for a real active device introduced in a PA circuit. The variation of G_3 with bias indicates that the small-signal 3rd order IMD (which is directly related to the PA's 3rd harmonic and gain compression or expansion) will change with bias point, not only in amplitude, but also in phase (the sign of G_3 in our memoryless nonlinearity).

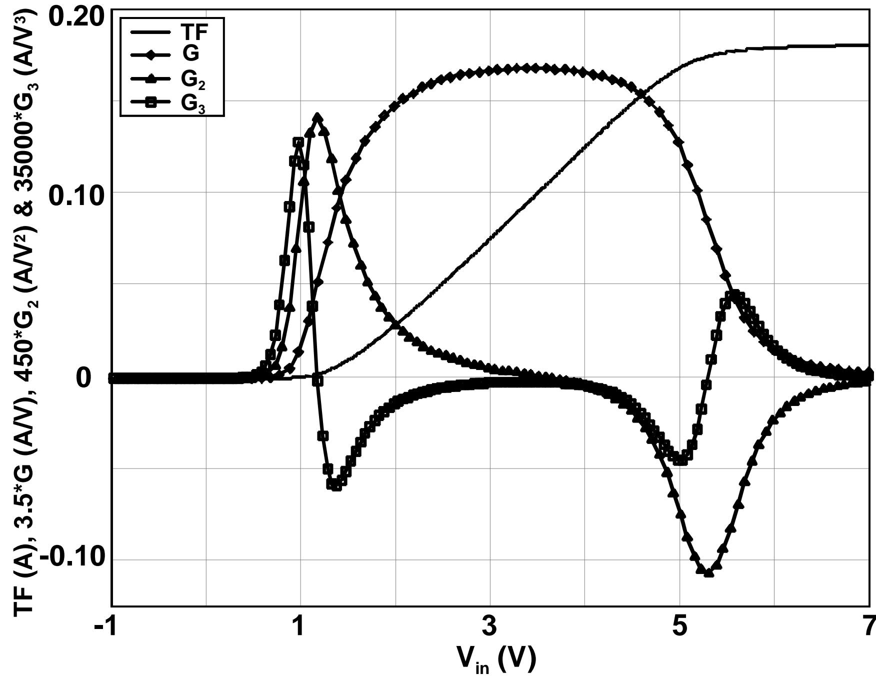

Fig. 11. Active Device TF and its first three coefficients of the Taylor series expansion: G, G_2 and G_3 of an active device introduced in a PA circuit.

Comparing Fig. 10 and Fig. 11, we conclude that we can find a null in the $G_3(V_I)$ characteristic close to the position of the ideal threshold voltage, V_T. So, biasing the PA at that point implies a null in the output 3rd order IMD. This result is consistent with the one obtained if the ideal PA were biased exactly at the break point of the piece-wise approximation, i.e. at V_T, originating the so-called linear (for odd order distortion) class B PA.

This observation leads to the desired and more precise definition of a generalized cut-off voltage, and thus of PA operation classes, if the bias point of this G_3 null (the so-called small-signal IMD sweet-spot [32]) is taken as the ideal V_T. Class C would then be the operating regime of a PA biased below that bias point, class B would correspond to a PA biased exactly at the null, and classes A and AB would be the operating regimes of PAs biased above that point.

This refinement of PA operation class is still consistent with every other property of the circuit, as it is shown in Fig. 12. As a matter of fact, this figure presents a comparison between the first four Fourier waveform normalized expansion coefficients vs generalized conduction angle, obtained from three PA active device approximations: a FET based PA, a BJT based PA and the ideal piece-wise model [25].

The similarity of the three curve families is obvious except for the region close to $2\theta = 360^{\circ}$ (class A). This is an indication that, contrary to the piece-wise linear model that only represents the devices' strong nonlinearities, the actual devices also manifest mild nonlinearities. So, they still show some residual distortion even when operated in the ideally linear class A regime.

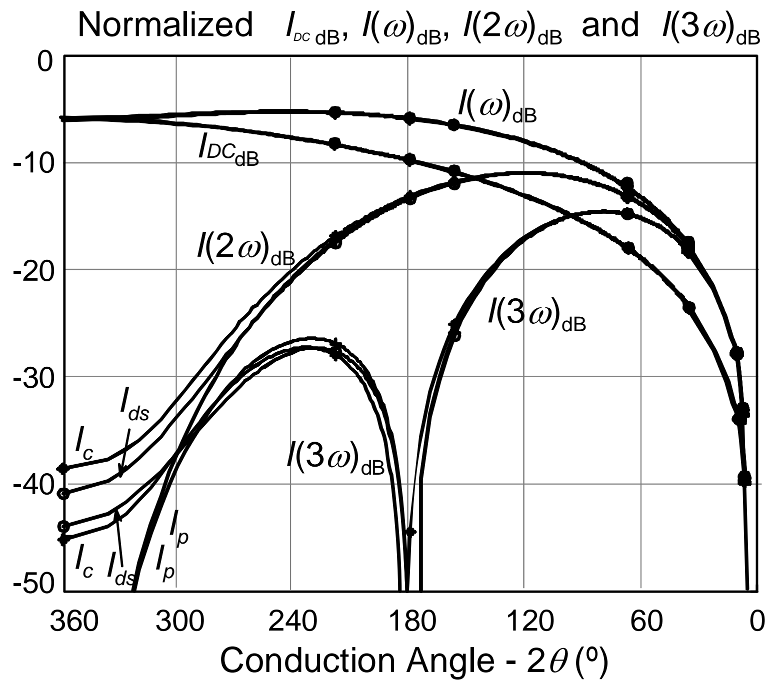

Fig. 12. Comparison of FET, BJT and piece-wise models, presented in [25].

With the PA operation classes precisely defined, we can focus our attention on the large-signal IMD sweet-spots. So, it is convenient to study small- and large-signal nonlinear characteristics separately.

In an IMD vs Pin plot, using logarithmic scales, small-signal 3rd order IMD (IM3) presents a slope of 3dB/dB, its phase is determined by the TF local derivatives and it can be controlled by changing the active device's bias point. So, as seen in Fig. 11, the small-signal IMD, determined by the coefficients of (1), can be either in phase with the fundamentals (a symptom of small-signal gain expansion), in opposition (gain compression), or of null amplitude. This last situation would correspond to highly linear class A, or class B, regimes, as previously reported in [32].

Under large-signal operation, the nonlinear response is determined by the PA energy balance considerations. As the PA becomes short in supply power, the phase of the large-signal IMD sidebands tends to a constant value of 180º [27], describing the inevitable gain compression.

Now, three different scenarios, corresponding to the three discussed PA operation classes, are possible:

In the first one, the PA is biased for class C, in which small- and large-signal IMD phases are in opposition, as illustrated in Fig. 13a. So, at the on-set of PA saturation the IMD must reverse its phase and there will be at least one IMD null (a large-signal IMD sweet-spot), as depicted in Fig. 13b.

In the second scenario, the PA is biased for class A. As seen in Fig. 14a, small- and large-signal IMD phases are now coincident, and no large-signal IMD sweet-spot can occur (Fig. 14b).

In the third and last scenario, the PA is biased for class AB, a more or less imprecise region of quiescent points just above the G_3 null. Despite small- and large-signal IMD phases are still coincident, depending on the difference between the contribution of the positive lobe of G_3, and the negative one (see Fig. 11), it can be proved that a transition from 180º to 0º can occur for low values of output power [33, 34] (Fig. 15a) generating an unexpected IMD sweet-spot. Beyond this signal level, the IMD presents an opposite phase to the one imposed by the large-signal asymptote, and thus a new IMD sweet-spot will have to appear at the on-set of saturation. So, in this case, and depending on the PA quiescent point, two sweet-spots can be generated (Fig. 15b). Fager et al. in [33, 34] give further details on the theoretical explanation of this behaviour.

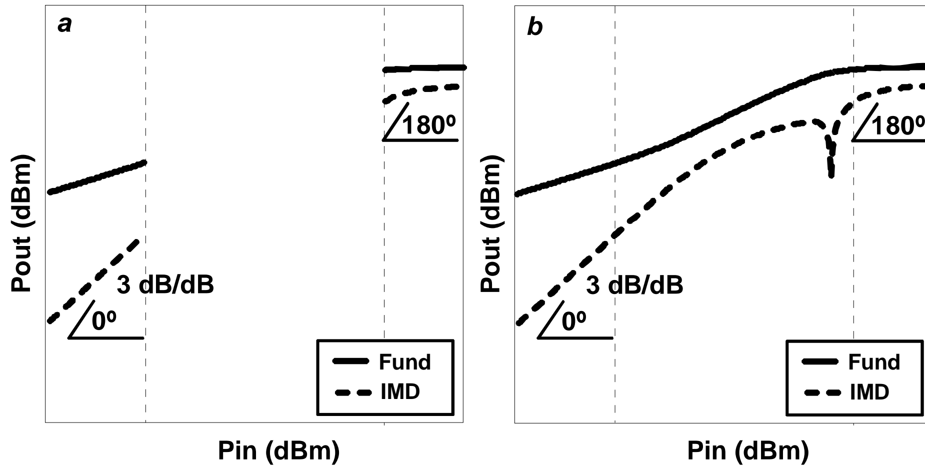

Fig. 13. Typical Pout and IM3 vs Pin characteristic for different small- and large-signal IMD phases (Scenario 1).

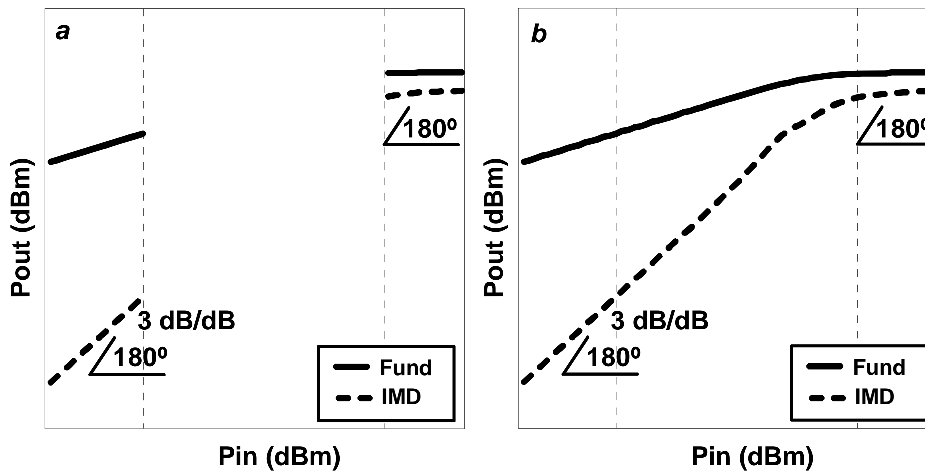

Fig. 14. Typical Pout and IM3 vs Pin characteristic for equal small- and large-signal IMD phases (Scenario 2).

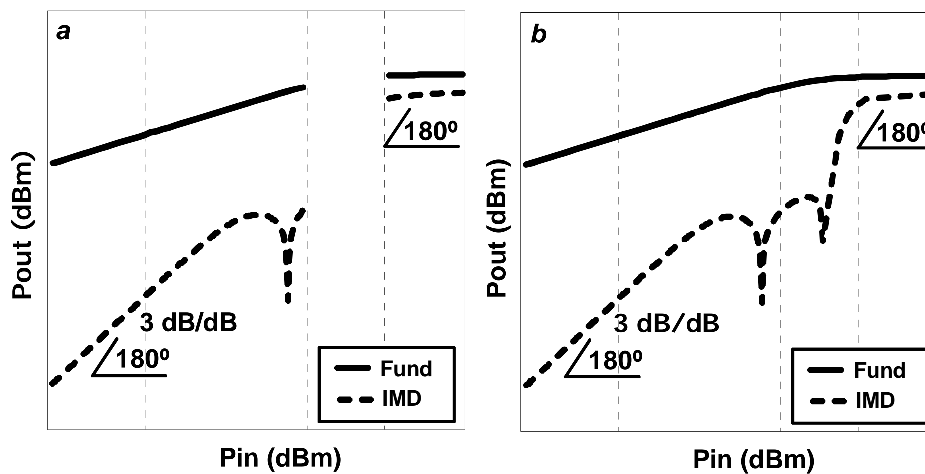

Fig. 15. Typical Pout and IM3 vs Pin characteristic for equal small- and large-signal IMD phases (Scenario 3).

In order to illustrate the ability of this analysis in describing IMD behaviour in several PA technologies, various harmonic balance (HB) simulations of PAs biased for classes C, AB and A were performed. The models used were: BSIM3v3 model [35] for Si MOSFET, Fager et al. [33] for Si LDMOS, Angelov-Zirath [36] for GaAs-AlGaAs HEMTs, Pedro [37] for GaAs MESFETs and the Gummel-Poon [30] for the Si BJTs.

As we want to analyze each of the above mentioned PA technologies, in three different operation classes, the simulated IMD results will be presented in the form of IMR vs Pin for class C, AB and A, instead of the usual IMD vs Pin, since this enables a faster and more obvious comparison between them.

A. Si MOSFET

From Fig. 16 it is possible to see that, for this Si MOSFET based PA, a large-signal IMD sweet-spot appears at class C, for high values of input power, while a double IMD sweet-spot appears at class AB, and no sweet-spot is visible in class A [34], as predicted.

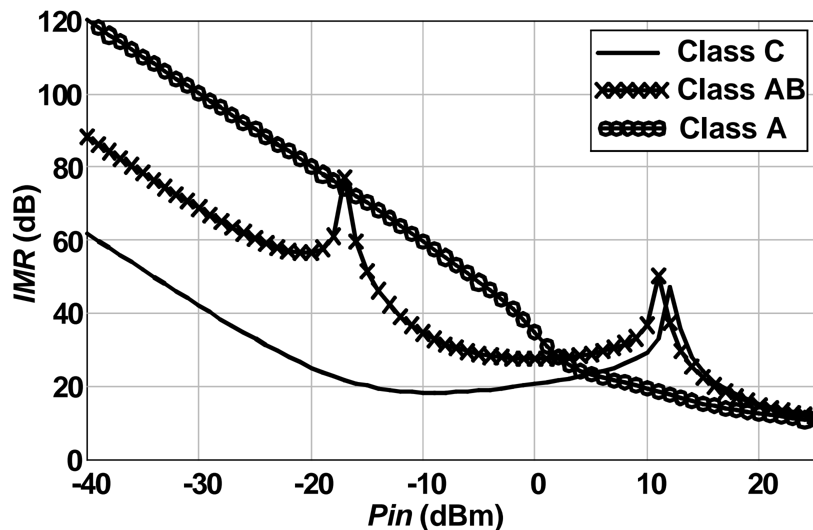

Fig. 16. Simulated IMR for a Si MOSFET PA at three operation classes: C, AB and A.

B. Si LDMOS

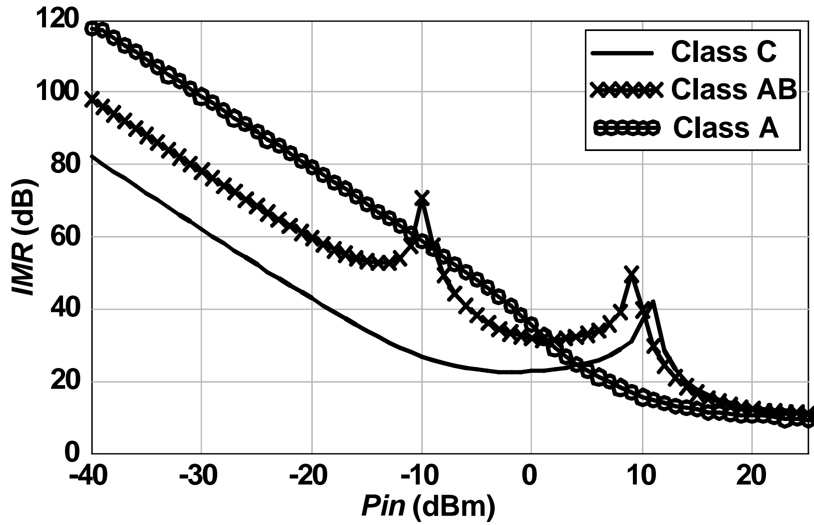

Fig. 17. Simulated IMR for a Si LDMOS PA at three operation classes: C, AB and A.

As depicted in Fig. 17, this Si LDMOS based PA presents similar results to the ones shown by the Si MOSFET PA [33].

C. GaAs-AlGaAs HEMT

Fig. 18 shows the results for this GaAs-AlGaAs HEMT based PA. These plots are similar to the ones already obtained for Si MOSFET and Si LDMOS.

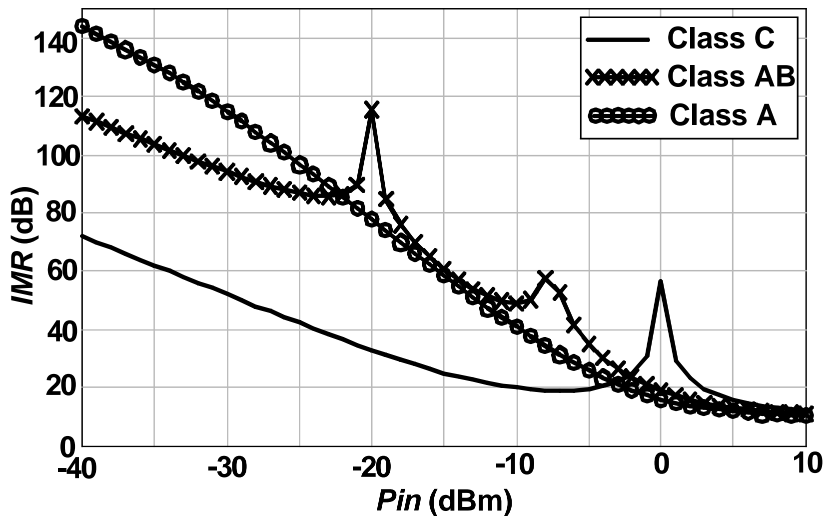

Fig. 18. Simulated IMR for a GaAs-AlGaAs HEMT PA at three operation classes: C, AB and A.

D. GaAs MESFET

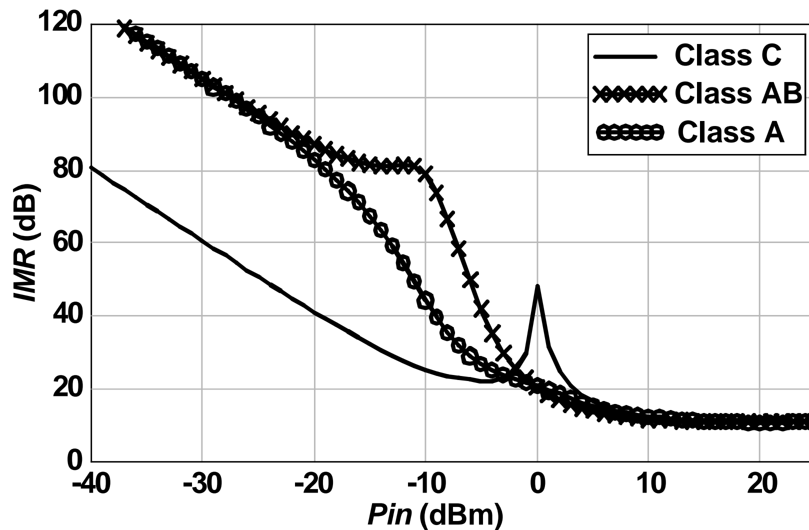

Fig. 19. Simulated IMR for a GaAs MESFET PA at three operation classes: C, AB and A.

Fig. 19 shows the results obtained for this GaAs MESFET based PA [38], in which IMR for classes A and C present the same aspect as seen before. However, class AB no longer has two peaks, but a rather smoother one. That slight increase in IMR at medium signal level regime can be attributed to an interaction between the negative G_3 and the positive higher orders' contributions. Nevertheless, they were found not strong enough to generate the previous phase reversal, and thus neither a strong IMR maximum at medium signal excursions is visible, nor there is any large-signal IMD sweet-spot.

E. Si BJT

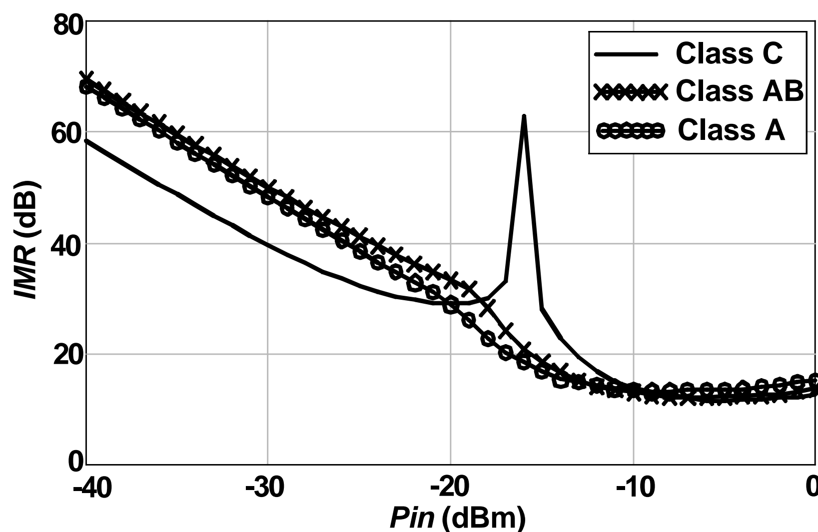

Fig. 20. Simulated IMR for a Si BJT PA at three operation classes: C, AB and A.

As seen from Fig. 20, the results obtained for the Si BJT based PA are similar to the ones observed for the GaAs MESFET.

As it is possible to see from Fig. 16 up to Fig. 20, class A presents the best small-signal linearity. But, for high values of input power, IMR in classes AB and C is better than in class A. This fact, associated with the low gain and PAE recognized for microwave PAs biased in deep class C, justifies their use in class AB where optimized linearity and efficiency can be simultaneously obtained.

In order to provide experimental illustration of these simulated predictions, Fig. 21 and Fig. 22 present measured results for two-tone IMR performance of a Si CMOS and, a GaAs MESFET based PAs in classes C, AB and A at 950 MHz, and 2 GHz, respectively.

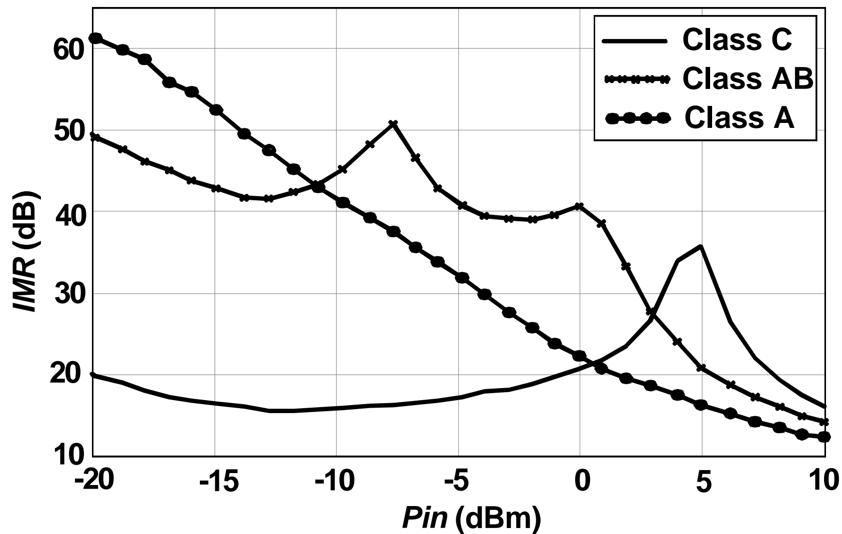

Fig. 21. Measured IMR for a Si CMOS PA at three operation classes: C, AB and A.

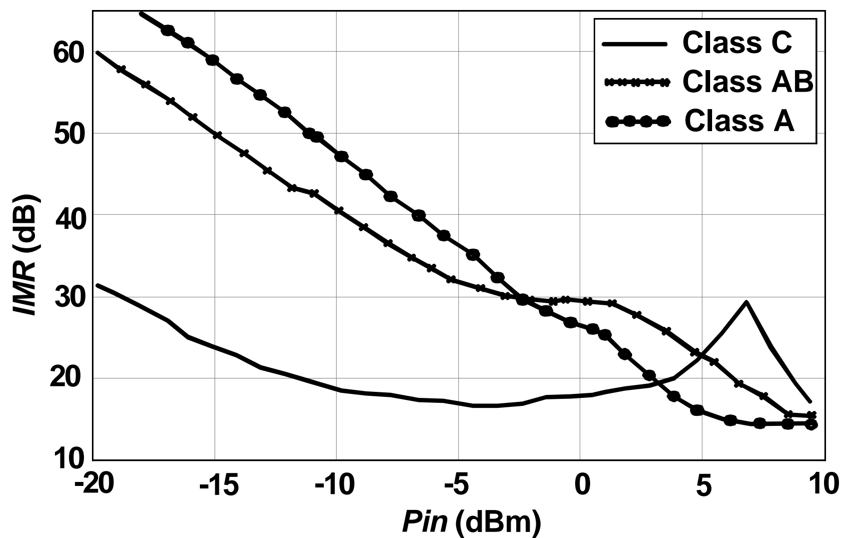

Fig. 22. Measured IMR for a GaAs MESFET PA at three operation classes: C, AB and A.

The experimental observations clearly support the simulated predictions shown in Fig. 16 and Fig. 19 for the corresponding PA technologies, validating the unified IMD theory above presented.

The measured IMD is always a summation of several contributions. When a sweet-spot occurs, this means that there was an exact cancellation between all involved components (memoryless PA). However, memory effects jeopardize this compensation by introducing an extra IMD component that will not be compensated. This prevents the presence of the sharp sweet-spots and a rather smoother version, similar to a valley, will be obtained, instead.

This is especially significant in linearization schemes that rely on cancellation mechanisms. So, a brief overview of these memory effects is presented in the next section.

1.1.2. Memory Effects in PA Circuits

The use of more complex signals, with higher bandwidths and envelope variations, has further increased the amplifier design constraints, demanding special attention to the PA's dynamic effects. These, usually known as memory effects (MEs) are properties of nonlinear dynamic systems in which circuits, presenting an almost static behaviour for small-signal (i.e., for their linear characteristics), show evident memory when driven into their nonlinear regimes. [25]

Memory effects are usually divided into two different types, depending on the time constants involved.

Short term MEs involve time constants of the order of the period of the microwave excitation and are caused by both the reactive components of the active device and the input and output matching networks. Since these MEs are much shorter than the information time scale, a PA presenting only short term MEs will behave as static for the information signal, reason why it is usually treated as being memoryless. The output response of a PA, presenting these effects, depends on the actual value, on the past samples, of its input and at the RF time scale, leading to an impulse response (IR) with short time tail, as illustrated in Fig. 23.

Fig. 23. Impulse response of a PA presenting short term memory effects, presented in [39].

On the contrary, long term MEs are low frequency phenomena (from dc to a few kHz or MHz) involving time constants that are comparable to the information time scale. Thus, they can press dynamic effects onto the envelope being processed. In this case, the impulse response of a PA presenting these effects depends on the actual value of its input and on the past samples at the envelope time scale, leading to a IR with long time tail behaviour, as depicted in Fig. 24.

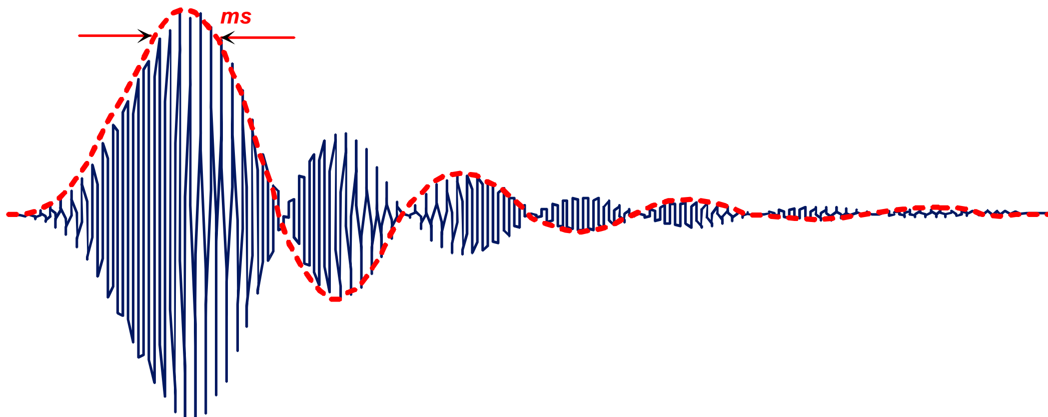

Fig. 24. Impulse response of a PA long term memory effects, presented in [39].

These long term MEs can only arise from some form of dynamic nonlinearity. They can be attributed to characteristics inherent to the active device: thermal effects and charge carrier traps; or imposed by external circuitry: bias networks. Fig. 25 presents a representation of the possible origins of long term memory effects in a generic PA circuit.

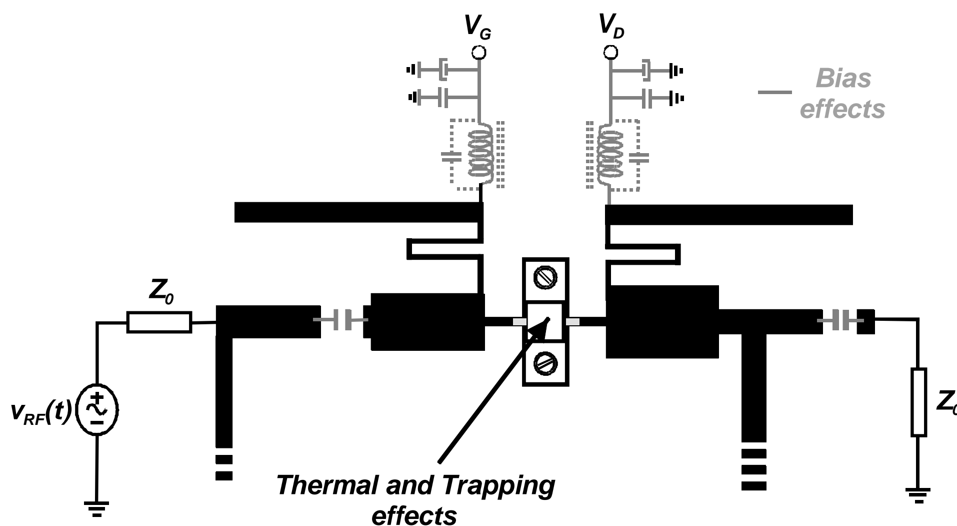

Fig. 25. Representation of the possible origins of long term memory effects in a generic PA circuit, adapted from [39].

In fact, the most striking factor for the baseband impedance variation are the bias networks. If the information bandwidth spans from dc to a few MHz and the impedance of the baseband matching network changes over that frequency range, the PA response over that same bandwidth will present some kind of memory effects. Fig. 26 presents a generic schematic used for bias networks and its typical S_{11} variation.

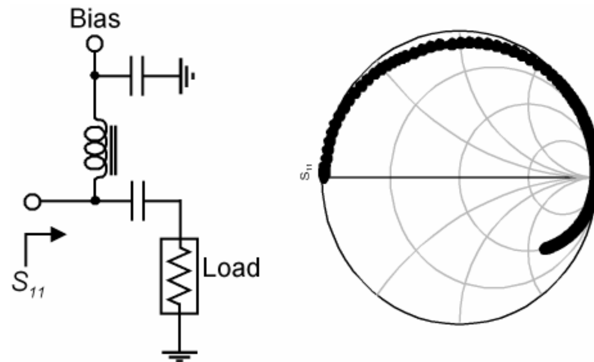

Fig. 26. Generic schematic used for bias networks and its typical S_{11} variation from dc to a few MHz.

From a behavioural viewpoint, these long term MEs show up as hysteresis in the Amplitude Modulation to Amplitude Modulation and Amplitude Modulation to Phase Modulation (AM/AM and AM/PM) plots, different two-tone IMD characteristics for varying tone spacing, IMD asymmetry, or even transient step response of an On-Off CW modulation test rending inoperative any conventional PA linearizer circuit conceived for static AM/AM and AM/PM nonlinearities.

This fact explains why the bias networks should be designed with great care if a highly linear PA is to be achieved.

1.2. State of the Art of GaN Power HEMT Modelling

Although various nonlinear global models have been proposed for many different microwave device types [25], GaN power HEMT modelling activities are still making their first steps so that, to the best of the authors' knowledge, no nonlinear model conceived to reproduce distortion properties has ever been published. Indeed, Green et al. [40] and Lee et al. [41] introduced a Curtice Cubic nonlinear model which has very poor IMD prediction capabilities [42, 43]. More recently, Raay et al. [44] used the Angelov-Zirath model but no IMD data have also been presented.

As this device uses a HEMT structure, the first choice for the nonlinear functional description of $i_{DS}(v_{GS},v_{DS})$ is the standard Chalmers, or Angelov-Zirath, Model [36], commonly accepted for GaAs HEMT devices. Its major advantage resides on its capability for reproducing the typical bell-shaped transconductance of heterojunction field effect transistor (HFET) devices, usually explained by the so-called "parasitic MESFET" behaviour, observed at high channel currents.

The complete $i_{DS}(v_{GS},v_{DS})$ model is given by:

$$i_{DS}(v_{GS},v_{DS}) = I_{pk} \cdot \{1+\tanh[\psi(v_{GS})]\} \cdot (1+\lambda\, v_{DS}) \cdot \tanh(\alpha\, v_{DS}) \tag{2}$$

I_{pk} is the drain current at which there is a maximum transconductance, subtracted the output conductance contribution. λ is the channel length modulation parameter and α is the saturation voltage parameter.

$\psi(.)$ is a power series function centred at V_{pk} with v_{GS} as a variable, i.e.

$$\psi(v_{GS}) = P_1(v_{GS}-V_{pk}) + P_2(v_{GS}-V_{pk})^2 + P_3(v_{GS}-V_{pk})^3 \tag{3}$$

where V_{pk} is the gate voltage for maximum transconductance and P_1, P_2 and P_3 are constants.

Using this model, we tried to evaluate its capabilities in predicting the fundamental output power and IMD of GaN devices. Keeping the transistor in three different operation classes (C, AB and A), a two-tone signal (f_1 and f_2), centred at 900 MHz with a frequency separation of 10 MHz, was applied to the transistor's input.

Fig. 27 up to Fig. 29 present the comparison between measurements and model predictions of the two fundamentals (f_1 and f_2) and IMD components ($2f_1$-f_2 and $2f_2$-f_1) for the above referred bias operation points.

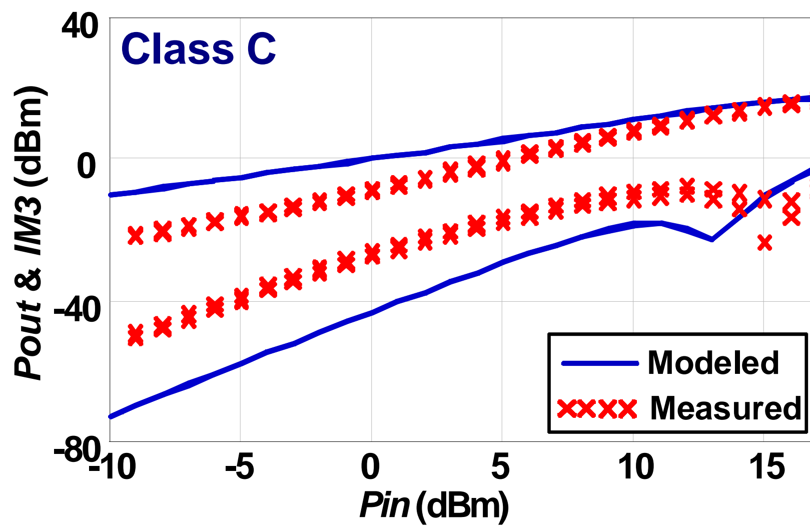

Fig. 27. Measured and simulated Pout and IM3 vs Pin for class C operation.

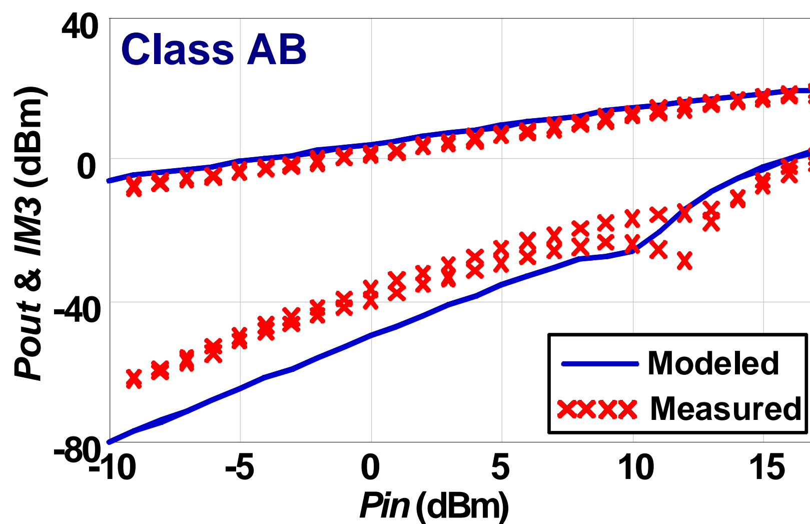

Fig. 28. Measured and simulated Pout and IM3 vs Pin for class AB operation.

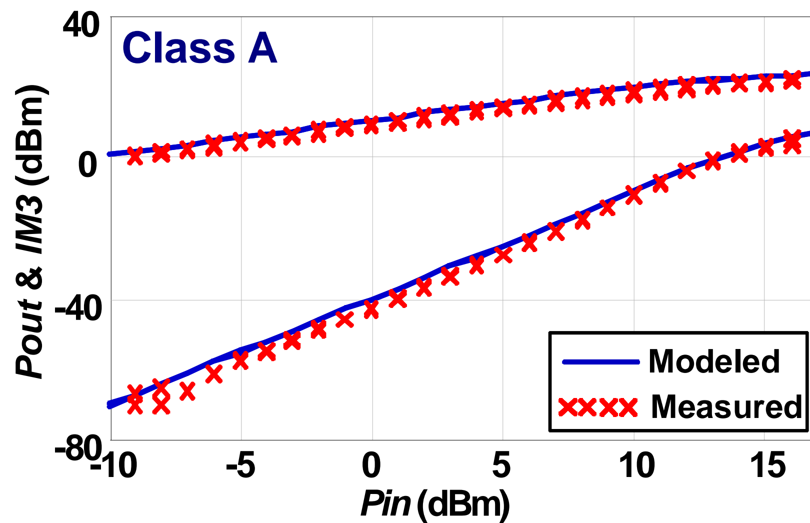

Fig. 29. Measured and simulated Pout and IM3 vs Pin for class A operation.

Trying to find out an explanation to these observed discrepancies, we discovered that, the best fit provided by the Chalmers model to the measured $G_m(v_{GS})$ and $G_{ds}(v_{GS})$, for a constant V_{DS} in the saturation zone, is the one presented in Fig. 30 and Fig. 31, respectively.

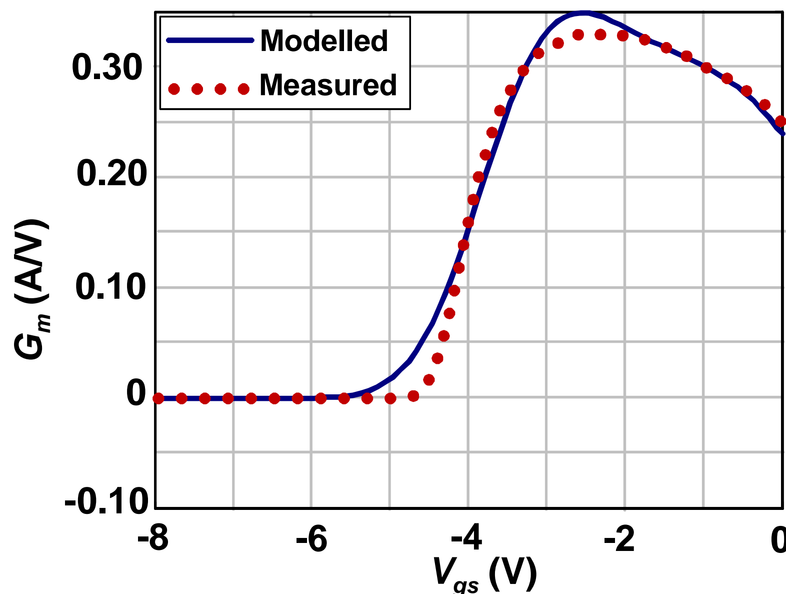

Fig. 30. G_m **measured and modelled with the Chalmers Model, for a constant** V_{DS} **of 6 V.**

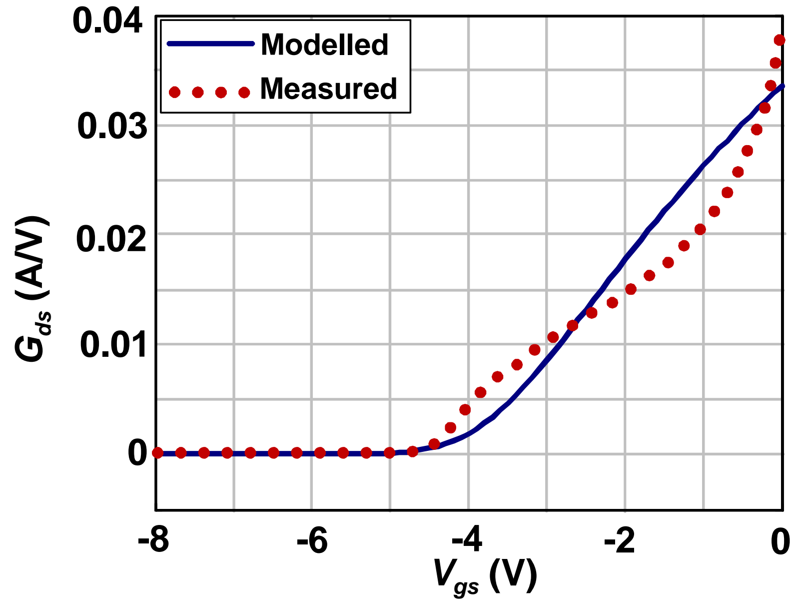

Fig. 31. G_{ds} **measured and modelled with the Chalmers Model, for a constant** V_{DS} **of 6 V.**

Although these results may not be considered dramatically bad, in a mean square error sense, they were considered unacceptable as they completely failed the $G_m(v_{GS})$ higher order derivatives: $G_{m2}(v_{GS})$ and $G_{m3}(v_{GS})$, in particular $\frac{\partial^3 i_{DS}}{\partial v_{GS}{}^3}$, as seen in Fig. 32 and Fig. 33. Hence, this compromises the model's accuracy in predicting the in-band intermodulation [25].

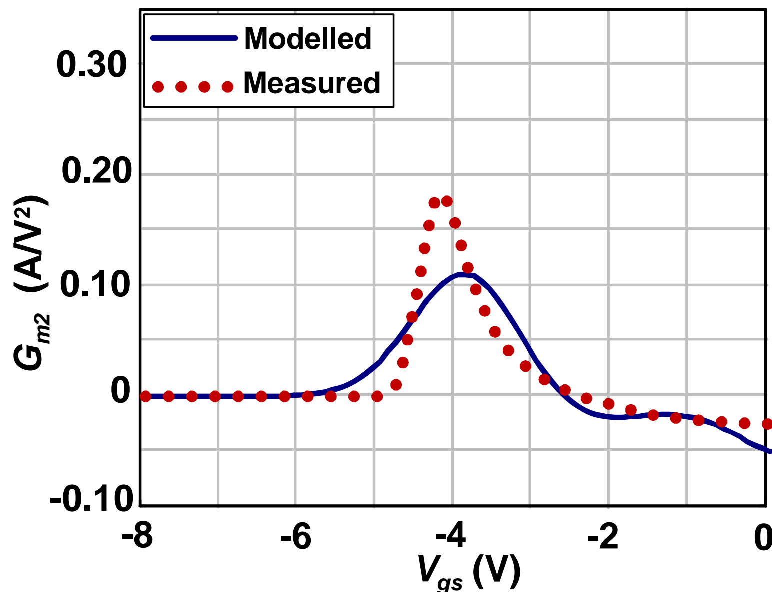

Fig. 32. G_{m2} **measured and modelled with the Chalmers Model, for a constant** V_{DS} **of 6 V.**

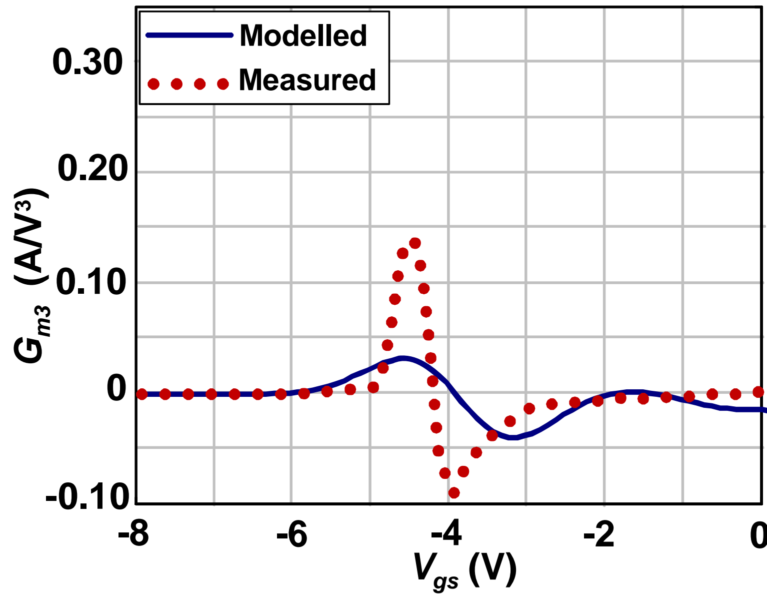

Fig. 33. G_{m3} **measured and modelled with the Chalmers Model, for a constant** V_{DS} **of 6 V.**

A detailed study of these disappointing results led us to the puzzling conclusion that this difficulty of the Chalmers Model in reproducing this HEMT I/V characteristic probably also comes from its referred main advantage: it tends to produce pronounced bell-shaped $G_m(v_{GS})$ forms. In fact, as it basically describes the $i_{DS}(v_{GS})$ dependence as an hyperbolic function, it tends to produce $G_m(v_{GS})$ of a distinct $\text{sech}(v_{GS})^2$ form. As it is widely known, this is a symmetric function across the transconductance's peak, notoriously different from the one extracted from S-parameter measurements, and shown in Fig. 30.

This being the case, and since there are no other models capable of predicting the IMD characteristics of these new GaN devices, there is a real need to develop a model meeting these requirements,

Furthermore, this need was, indeed, felt by one of GaN HEMT foundries, Nitronex Corp., when they contracted our group exactly for that purpose.

1.3. Objectives

This thesis deals with the nonlinear modelling activities directed to an emergent active device technology: GaN HEMTs. GaN is expected to play a key role in future power amplifier applications of microwave and wireless digital telecommunication systems. This, in turn, justifies all the time spent on improving their accurate nonlinear representation.

It is now clear that nonlinear modelling is crucial, not only for power amplifier design, taking advantage of large-signal IMD sweet-spots, but also for the detection and compensation of memory effects arising from intrinsic or extrinsic sources.

As stated in the previous sections, GaN modelling is making its first steps and there is not a model capable of accurately predicting the nonlinear distortion characteristics that, as shown before, have common roots and share similar origins with other technologies.

So, the main objective of this thesis is to formulate, extract, implement and test a nonlinear equivalent circuit model for Gallium Nitride HEMTs, capable of accurately predicting their Pout, AM/AM and AM/PM conversions, PAE and IMD characteristics.

In order to accomplish this main goal we sub-divided it into four other intermediate goals:

- Characterize the GaN devices and detect similarities/differences with devices from other technologies;
- Adjust an existing, or propose a new model, and its required parameter extraction methodology;
- Validate the nonlinear model at the transistor level and under a real application environment;
- Evaluate the robustness of the proposed GaN HEMT model, considering the observed variability of GaN device performance;
- Show the new model's applicability with the study of the AM/AM and AM/PM conversions.

1.4. Summary

To fulfil the above mentioned objectives, this thesis was organized as follows:

Chapter 1 provides the motivation to this work and introduces the most important wide bandgap semiconductor material properties and their relationship with the device performance. In addition, the state-of-the-art is presented, the prime objectives are explained and the main contributions, to the RF and microwave nonlinear modelling area, are addressed.

Chapter 2 presents the most important characteristics of the devices used and addresses the formulation and extraction procedure of a nonlinear equivalent circuit model for a microwave power GaN HEMT, amenable for integration into commercial harmonic balance or transient simulators. All the steps taken to extract its parameter set are explained.

Chapter 3 validates the model addressing its predictive capabilities by comparing measured and simulated broadband S-parameters, AM/AM and AM/PM conversions, Pout, PAE and IMD data, at the transistor level and using a PA circuit (real application environment).

Chapter 4 studies the robustness of the proposed GaN HEMT model, for a new set of GaN devices, all from the same manufacturer, evaluating its capabilities of representing the Pout and IMD behaviour of the whole set of available devices;

Chapter 5 applies the model to a comprehensive study of the memory effects, arising from different in-band and out-of-band load terminations impact, on the AM/AM and AM/PM conversions.

Finally, **Chapter 6** concludes this thesis by summarizing its most important achievements and opens the door for the research topics to be addressed in the future.

1.5. Original Contributions

The thesis is believed to represent an important contribution in what GaN active device modelling is concerned. The nonlinear equivalent circuit model, arising from this work, was the first one capable of predicting the intermodulation distortion characteristics, observed on real GaN HEMT power devices.

The extensive model extraction procedure presented eases the optimization needs when dealing with this type of nonlinear models and the model robustness test verifies its usefulness and reliability. Additionally, it also sheds light into the development stage already achieved by these devices.

The detailed and extensive comparison, between experimental and modelled results, is also very valuable, and it can be used as a good benchmark for comparing future modelling work on GaN devices.

Moreover, the use of this model to study the different in-band and out-of-band load terminations impact, on the overall AM/AM and AM/PM conversions, can help PA designers to understand and compensate the static and dynamic effects.

Proving this work original contributions', it is next presented a list of the already published material in international conferences and journals:

Papers in International Conferences:

Pedro M. Cabral, Nuno B. Carvalho and José C. Pedro, "An Integrated View of Nonlinear Distortion Phenomena in Various Power Amplifier Technologies", *European Microwave Conference Dig.*, Munich, Germany, pp. 69-73, Oct. 2003. *(invited paper)*.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "New Nonlinear Device Model for Microwave Power GaN HEMTs", *IEEE MTT-S Int. Microwave Symp. Dig.*, Fort-Worth, Texas, United States, pp. 51-54, Jun. 2004.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Nonlinear Model with AM/AM, AM/PM and IMD prediction capabilities for GaN HEMTs", *Int. Workshop on Electronics and System Analysis Proc. CDROM*, Bilbao, Spain, Oct. 2004.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Modeling AM/AM and AM/PM Conversions in Microwave Power Amplifier Circuits", *Integrated Non-linear Microwave and Millimetre-wave Circuits Workshop Proc.*, Rome, Italy, pp. 139-142, Nov. 2004.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Highly Linear GaN Class AB Power Amplifier Design", *Asia Pacific Microwave Conference Proc. CDROM*, New Delhi, India, Dec. 2004.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Extraction Procedure and Validation of a Large-Signal Model for GaN HEMTs", *XX Conference on Design of Circuits and Integrated Systems Proc. CDROM*, Lisbon, Portugal, Nov. 2005.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Dynamic AM-AM and AM-PM Behavior in Microwave PA Circuits", *Asia Pacific Microwave Conference Proc.*, Suzhou, China, vol. 4, pp. 2386-2389, Dec. 2005.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Bias Networks Impact on the Dynamic AM/AM Contours in Microwave Power Amplifiers", *Integrated Non-linear Microwave and Millimetre-wave Circuits Workshop Proc. CDROM*, Aveiro, Portugal, Jan. 2006.

Nuno B. Carvalho Pedro M. Cabral and José C. Pedro, "Modeling Strategies and Characterization Techniques for Microwave GaN Power Amplifiers", *Microwave Technology and Techniques Workshop: Enabling Future Space Systems' Proc. CDROM*, ESTEC, Noordwijk, The Netherlands, 15-16 May 2006.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Envelope Time Domain Characterization of Microwave Power Amplifiers", *Mediterranean Microwave Symposium Proc. CDROM*, Genova, Italy, 19-21 Sept. 2006. *(invited paper)*.

Papers in International Journals:

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Nonlinear Device Model of Microwave Power GaN HEMTs for High-Power Amplifier Design", *IEEE Trans. Microwave Theory Tech.,* vol. 52, pp. 2585-2592, Nov. 2004.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "A Unified Theory for Nonlinear Distortion Characteristics in Different Amplifier Technologies", *Microwave Journal*, pp. 62-78, Apr. 2005.

George D. Vendelin, José C. Pedro and Pedro M. Cabral, "Amplifier and Transistor Gains Revisited: GP, Av, Ai, Gm and Zm", *Microwave Journal*, pp. 80-92, Apr. 2005.

Pedro M. Cabral, José C. Pedro and Nuno B. Carvalho, "Modeling Nonlinear Memory Effects on the AM/AM, AM/PM and Two-Tone IMD in Microwave PA Circuits", *Int. Journal of RF and Microwave Computer-Aided Engineering*, vol. 16, pp. 13-23, Jan. 2006.

2. GaN Nonlinear Model Formulation and Extraction

This chapter is dedicated to the GaN nonlinear device modelling activities. Here, it is possible to find information concerning the GaN device characteristics, model formulation and extraction. All these steps will be discussed having in mind the nonlinear analysis, from a distortion prediction point of view.

Mathematical representations of real active devices can be divided into two major groups: physical and empirical modelling, [25]. Fig. 34 presents a summary of their most important characteristics.

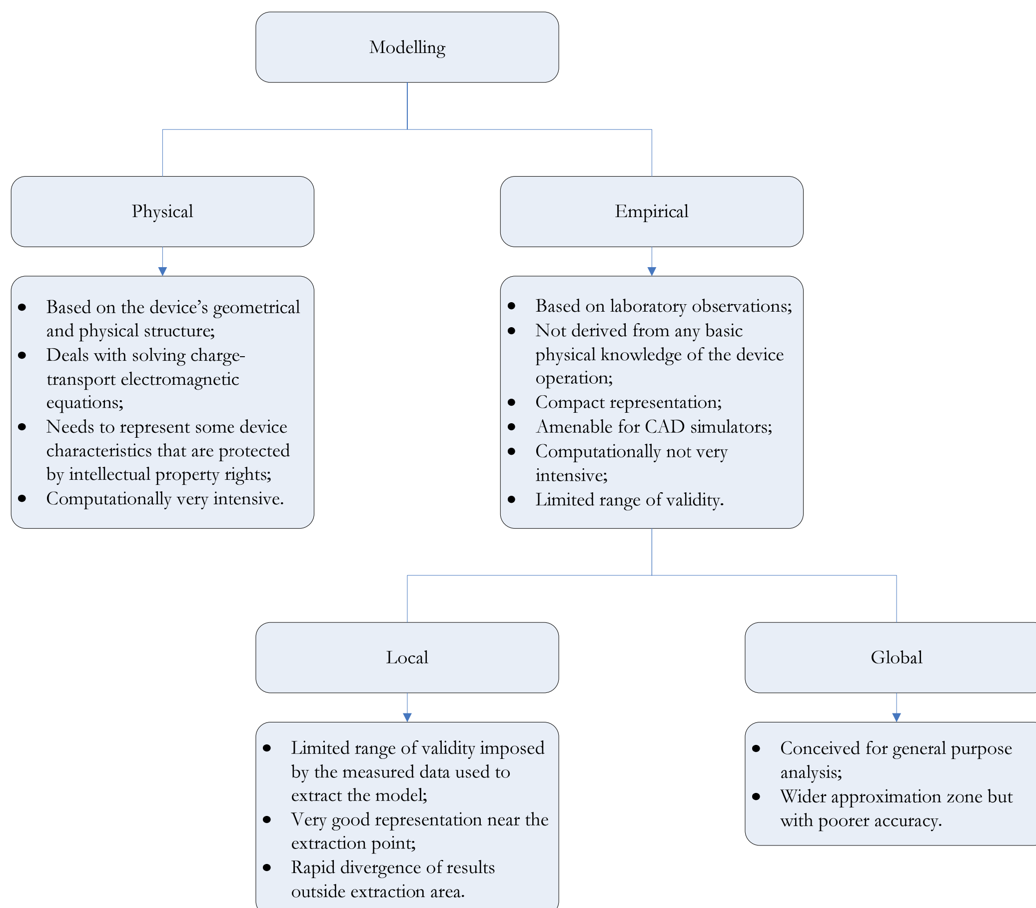

Fig. 34. Modelling classification.

Nonlinear models, used in circuit simulations, are mostly based on equivalent circuits that are neither pure physical, nor even empirical models, but a combination of both.

Based on the knowledge of the device physical characteristics, the equivalent circuit model is characterized by a specific topology, particular for that type of devices. On one hand, the equivalent circuit model includes elements that provide a lumped approximation to some aspect of the device and, on the other hand, it also uses functional descriptions taken from measured I/V or Q/V data.

Nowadays, all computer aided design (CAD) circuit simulators can accept equivalent circuit models. They are easy to implement and computationally very efficient. These factors are very important, particularly for circuit optimization, where several simulation interactions are required and for large scale integrated circuit analysis. However, the increasing complexity needed to accurately describe high frequency circuits, is a severe drawback to their implementation.

Another factor, that limits the usefulness of equivalent circuit models, is the difficulty in relating circuit element values to physical and process parameters, such as geometry, mobility, doping profile, carrier types, etc. Consequently, when there is a need to design and develop new, or improved devices, it is preferable to use physical models.

However, in this case, since we were interested in a relatively low frequency and computationally efficient model, we adopted an equivalent circuit approach. Furthermore, the physical characteristics of the devices were protected by intellectual property rights and we had no possibilities of accessing them.

2.1. GaN Device Characteristics and Measurement Setup

The devices used were GaN HEMTs on Si substrate with 2mm gate periphery (Unit Cell), encapsulated in a standard high power microwave package. Fig. 35 shows the packaged device and Fig. 36 a magnified version of its interior.

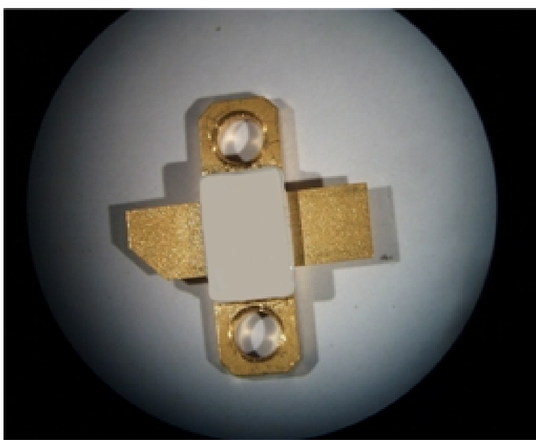

Fig. 35. 2mm packaged GaN HEMT.

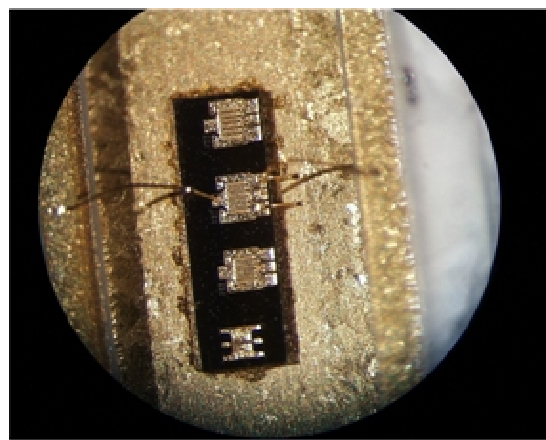

Fig. 36. Magnified version of the packaged device showing the chip inside.

The HFET device structure is schematically represented in Fig. 37, taken from [45].

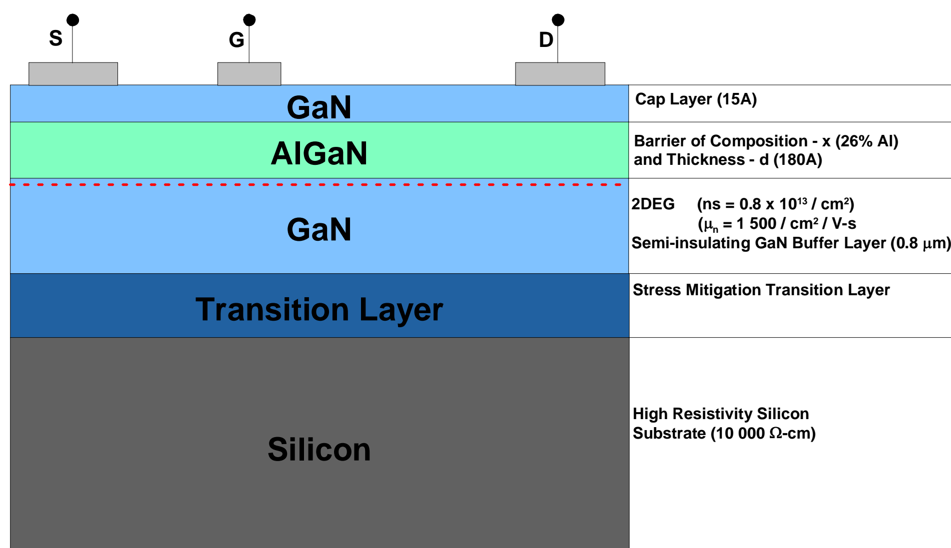

Fig. 37. HFET Device Structure, taken from [45].

Fig. 38 shows measured I_{DS} *vs* V_{DS} characteristics, under static conditions, for six different V_{GS} biases and Fig. 39 depicts its transfer characteristic and transconductance for a fixed V_{DS} of 6 V.

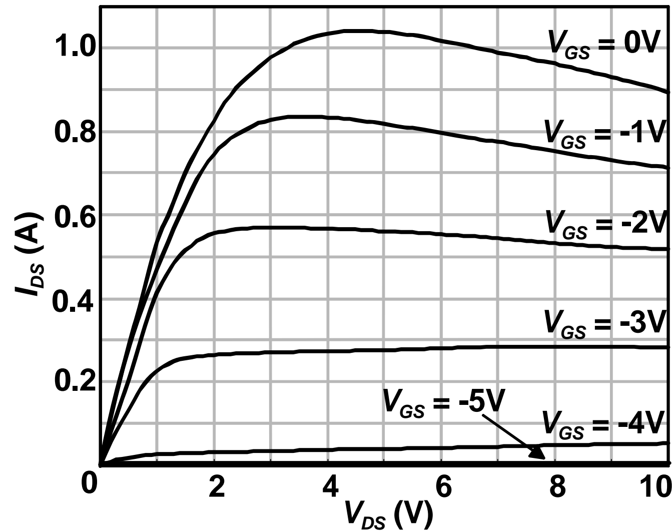

Fig. 38. Typical I_{DS} vs V_{DS} curves measured under static conditions, for six different V_{GS} biases.

As seen, this is a depletion mode transistor with a $V_{pinch\ off}$ of -4.3 V, a I_{DSS} of 1 A and a $G_{m\mathrm{MAX}}$ of 330 mS.

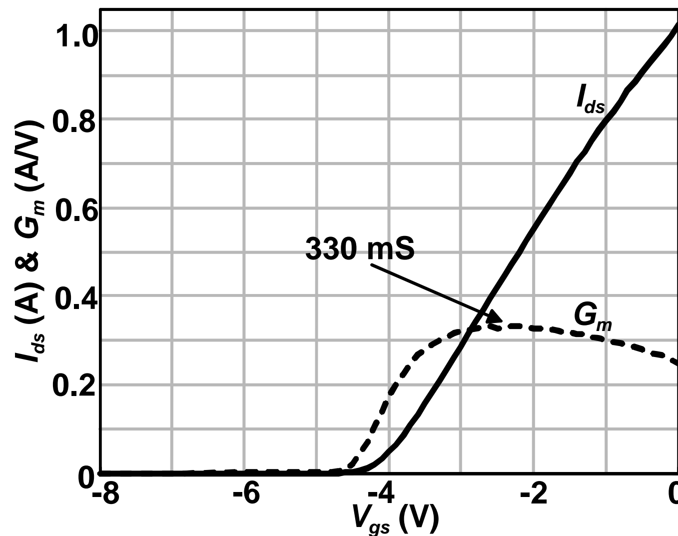

Fig. 39. $i_{DS}(v_{GS})$ transfer characteristic and $G_m(v_{GS})$ for a fixed V_{DS} of 6 V.

Since we are working with power devices, it is necessary to pay a special attention to the transistor mounting. Fig. 40 presents the GaN transistor embedded in a copper base (serves as physical structure and as heatsink) and placed on a printed circuit board (PCB).

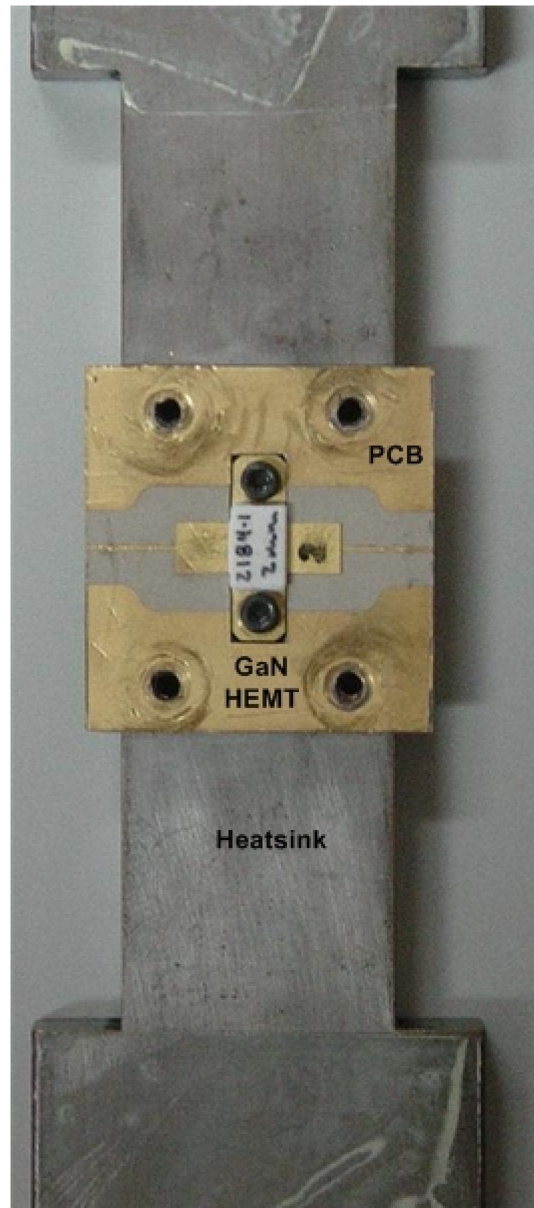

Fig. 40. GaN transistor embedded in a copper base and placed on a PCB.

In order to re-use the GaN HEMTs, a special setup was designed that allows changing the active device, without damaging it, using a TEFLON piece screwed in the copper base that presses the transistor leads to the PCB board, see Fig. 41.

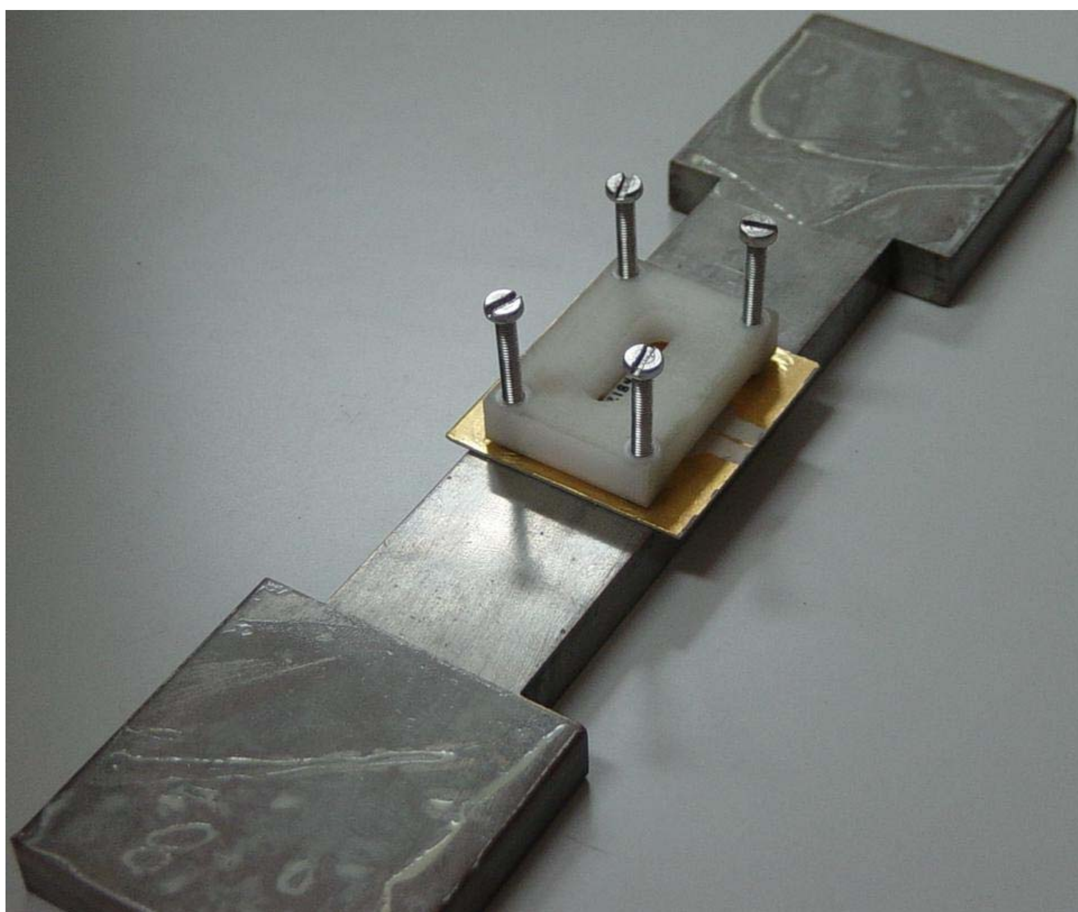

Fig. 41. Flexible setup that allows changing the transistor without damaging it.

The complete setup implementation used during the model extraction is presented in Fig. 42. An Anritsu Universal Test Fixture was used to attach the setup to SMA connectors and two positioners sustained the all set.

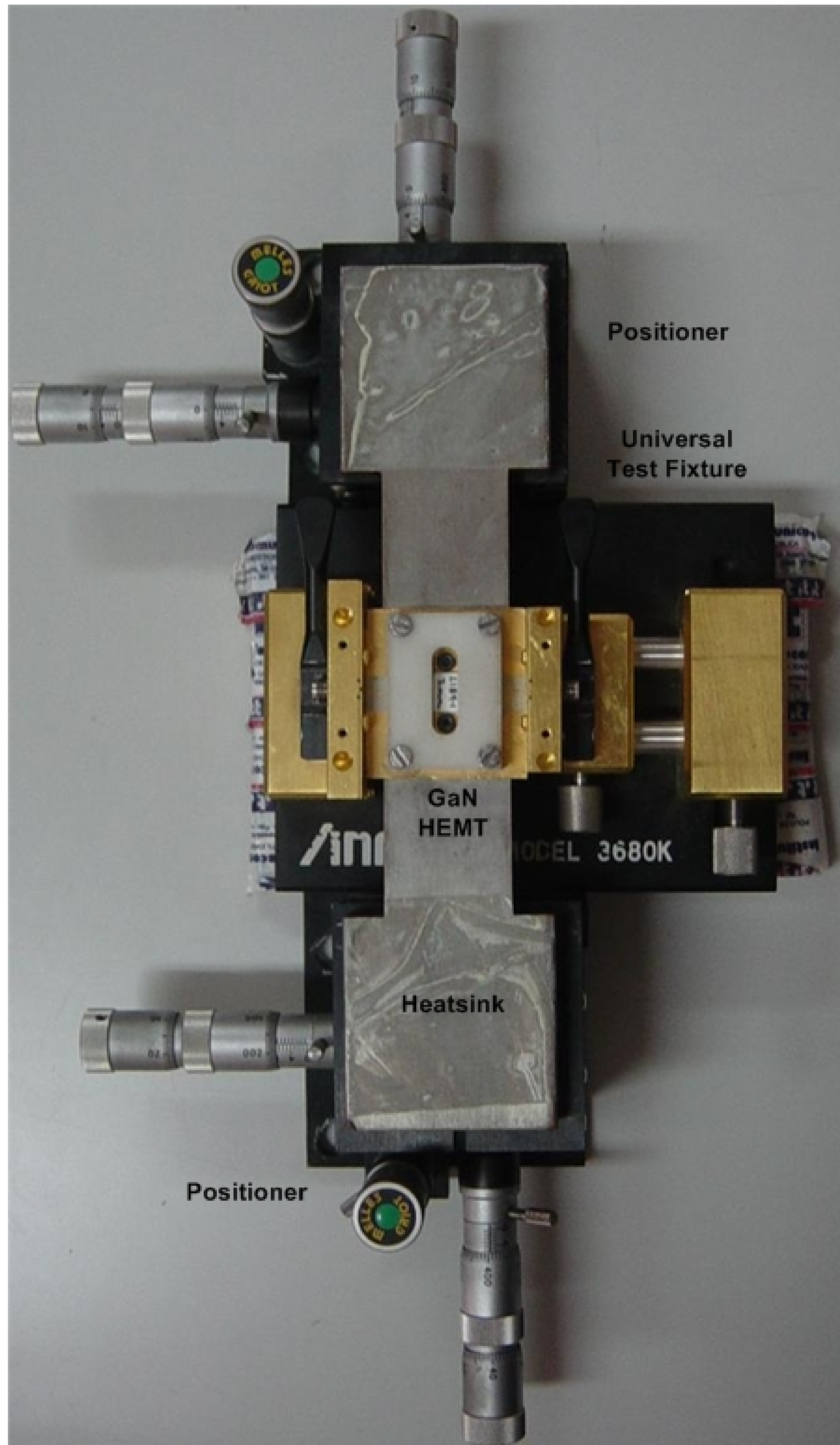

Fig. 42. Complete setup implementation used during the model extraction.

2.2. Model Formulation and Extraction

This section presents a large-signal empirical model amenable for integration into any standard harmonic balance or transient simulator.

The model is based on the equivalent circuit topology shown in Fig. 43, which includes both extrinsic (parasitic to the device's ideal behaviour), and intrinsic elements (specific to the device operation) that try to represent electromagnetic effects caused by the particular device structure, discussed in more detail in the next sections.

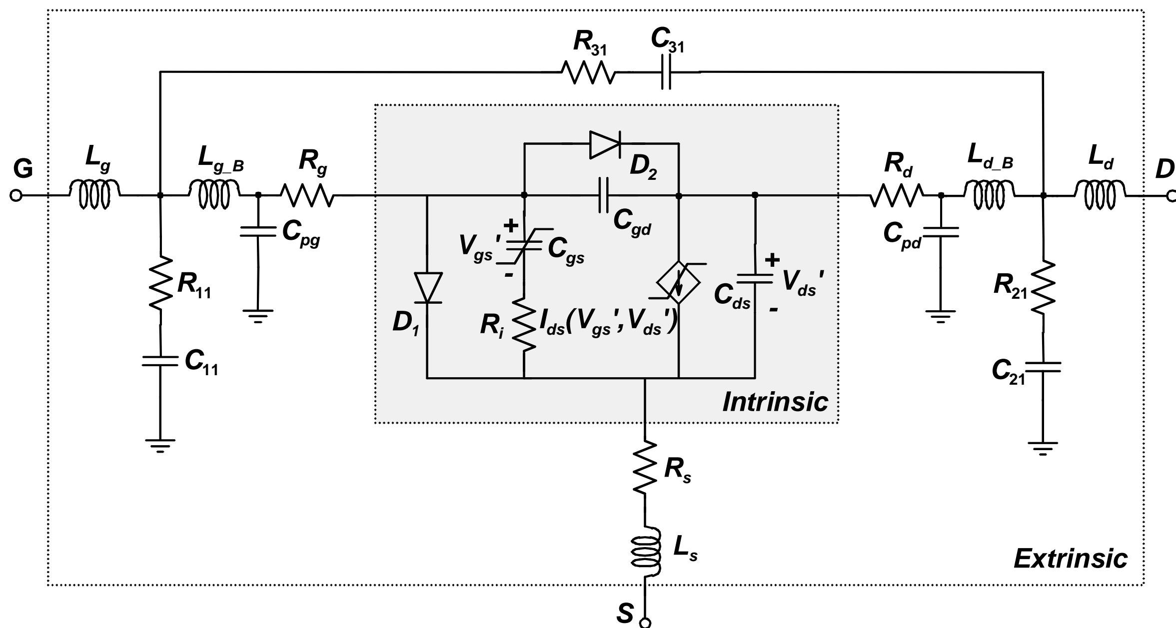

Fig. 43. Equivalent circuit model topology used.

The extrinsic elements can be considered linear, and so, they will maintain their values constant, independently of bias, or even, applied signal. On the other hand, the intrinsic elements are usually considered as nonlinear, and so, they will be dependent on the applied signal or bias. Nevertheless, and depending on the sought application, some intrinsic elements can also be considered as linear since their variation will have a small impact on the overall model prediction capabilities.

The nonlinear elements will require a convenient functional description that, not only has to guarantee a minimum error between the measured and modelled device characteristics but, more important than that, has to present a good approximation of the curve shape, achieved fitting the curve's higher order derivatives.

2.2.1. Extrinsic and Linear Intrinsic Elements

The extrinsic part is mainly dependent on the device's external environment and is usually composed by lumped elements trying to emulate actual distributed effects. In this case, R_g, R_d and R_s represent contact and semiconductor bulk resistances; L_g, L_{g_B}, L_d, L_{d_B}, and L_s contact and bond-wire inductances, while C_{pg} and C_{pd} model distributed effects caused by the gate and drain chip pads, respectively. Fig. 44 shows the metal-ceramic package terminology, presented in [46].

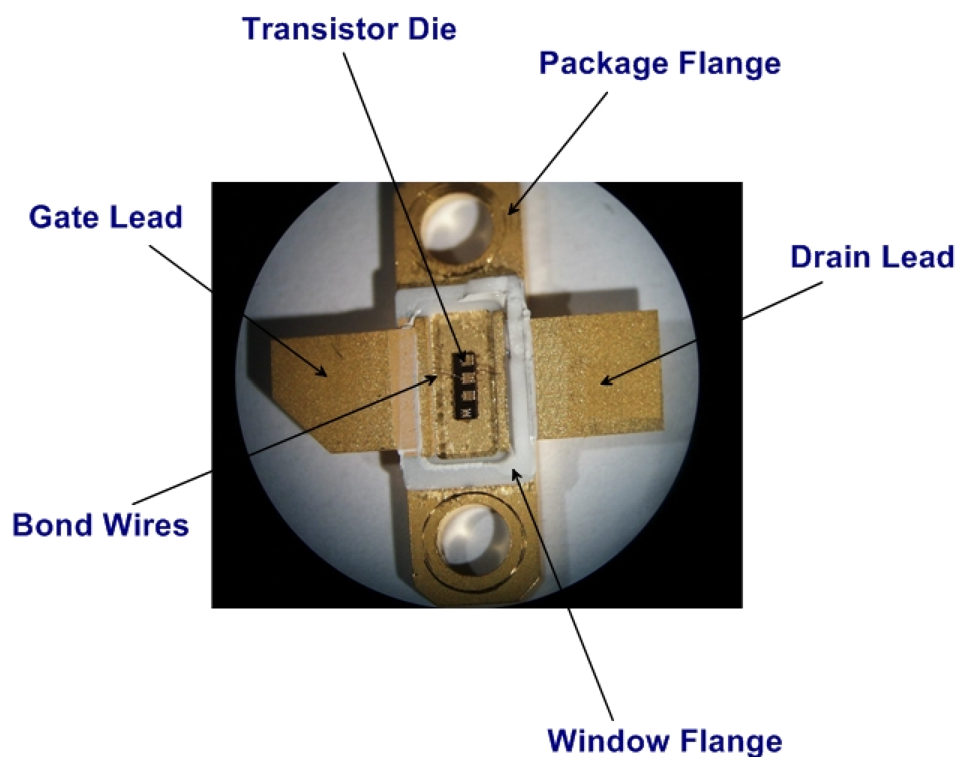

Fig. 44. Metal-ceramic package terminology, presented in [46].

Besides the usual extrinsic FET elements, the equivalent circuit of Fig. 43 includes three *R-C* series networks: one at the gate (R_{11} and C_{11}), one at the drain (R_{21} and C_{21}), and another connecting both ports (R_{31} and C_{31}). These fairly low quality factor networks were first introduced by Chumbes et al. in [47] and then by Manohar et al. in [48]. They are meant to reproduce the impact of the lossy p-Si/GaN/metal structure on the S-parameters, especially a pronounced resistive component observed under channel current cut-off (cold FET operation).

The determination of all series resistances and inductances was performed using S-parameter measurements (from 30 kHz up to 3 GHz), taken under forward gate bias conditions, as described by Dambrine et al. in [49] and, more recently by Lai et al. in [50]. This was possible since, as reported in [48], the transversal *R*-*C* networks have minimum effect on the Z-parameters measured under this 0 V V_{DS} operating mode.

The remaining extrinsic elements' values were extracted from an optimization of the cold FET (V_{DS}=0V, V_{GS}=-8V) S-parameter data, using a linear microwave CAD tool.

The extrinsic element values, finally obtained, are shown in Table 2.

Table 2. Extrinsic element values.

Elements	Value
R_g	1.67 Ω
R_d	0.9 Ω
R_s	0.1 Ω
L_g	0.9 nH
L_d	1.7 nH
L_s	0.1 nH
L_{g_B}	0.7 nH
L_{d_B}	1.0 nH
C_{pg}	0 pF
C_{pd}	0 pF
R_{11}	20 Ω
C_{11}	2.3 pF
R_{21}	70 Ω
C_{21}	1.2 pF
R_{31}	5 Ω
C_{31}	0.1 pF

In what the intrinsic elements are concerned, R_i, models the distributed resistance of the semiconductor region under the gate, between the source and channel, usually known as intrinsic resistance, or even, charging resistance. Its inclusion in the equivalent circuit model is primarily due to improvements in the S_{11} match. This resistor value is very difficult to extract and its physical significance is questionable, [51, 52].

The drain source capacitance, C_{ds}, represented in the equivalent circuit model as the intrinsic output capacitance, can be separated in two different parts: one invariant, originated from the capacitive coupling between source and drain and, another one, bias dependent on the channel carrier distribution, [51, 52].

The gate-channel junction was split into two independent voltage controlled current sources and corresponding voltage controlled charge sources. The latter are represented in the equivalent circuit of Fig. 43 by the diode symbols, a nonlinear (depletion capacitance) $C_{gs}(v_{GS})$ and linear (constant depletion capacitance) C_{gd} that model the change in the depletion charge, with respect to the gate-source and gate-drain voltages, respectively.

Both C_{ds} and R_i were taken as bias-invariant elements. Furthermore, since such devices are primarily intended for highly efficient and low distortion power amplifier applications, and are thus usually kept in the saturation region, C_{gd} was also assumed to be approximately linear.

In order to determine all the linear intrinsic elements, the methods, presented in [49] and [50], were again used. The obtained values are shown in Table 3.

Table 3. Invariant intrinsic element values.

Element	Value
R_i	5 Ω
C_{gd}	0.3 pF
C_{ds}	3.0 pF

Considering the intended microwave PA application, a quasi-static global model is now needed for each of the nonlinear intrinsic elements: drain-source current and gate-channel junction current and stored charge.

2.2.2. Nonlinear Drain-Source Current Model

The drain-source current global model should be capable of reproducing the device's strong nonlinearities but also nonlinear details, i.e., meeting the local modelling criteria. Therefore, the selected model should be one of the traditional large-signal models seen in all harmonic-balance or SPICE like simulators, but still capable of reproducing, at least, the first three derivatives of the major source of HEMT nonlinearity: the gate-source and drain-source voltage dependent channel-current, $i_{DS}(v_{GS},v_{DS})$.

A convenient way to elaborate such a mathematical representation is to rely on a global model that may be expressed as:

$$i_{DS}(v_{GS},v_{DS}) = \beta \cdot f_g(v_{GS},v_{DS}) \cdot f_d(v_{DS},v_{GS}) \tag{4}$$

$f_g(.)$ and $f_d(.)$ are the functions responsible for representing the dependence of i_{DS} on v_{GS} and v_{DS} while β is simply a scaling factor. Moreover, this model must produce accurate coefficients of the two-dimensional Taylor series expansion defined by:

$$\begin{aligned} &i_{DS}(v_{GS},v_{DS}) = \\ &I_{DS} + G_m v_{gs} + G_{ds} v_{ds} + G_{m2} {v_{gs}}^2 + G_{md} v_{gs} v_{ds} + G_{d2} {v_{ds}}^2 + G_{m3} {v_{gs}}^3 + G_{m2d} {v_{gs}}^2 v_{ds} + G_{md2} v_{gs} {v_{ds}}^2 + G_{d3} {v_{ds}}^3 \end{aligned} \tag{5}$$

where v_{gs} and v_{ds} are the incremental deviations of the terminal voltages v_{GS} and v_{DS} around the quiescent point V_{GS} and V_{DS}.

The asymmetric behaviour of G_m, seen in Fig. 39 (sudden rise near turn-on followed by a smooth decrease towards 0 V), directed our attention to the in-house FET model previously proposed, in our research group, by Fager et al. for Si LDMOS [33]. Intended for detailed nonlinear distortion description, it relies on behavioural device data, of both dc and small-signal $i_{DS}(v_{GS},v_{DS})$: first derivative in order to v_{DS}, G_{ds}, and first, second and third order derivatives in order to v_{GS}, G_m, G_{m2} and G_{m3}, respectively.

This drain-to-source nonlinear current model is defined by a set of equations, each one representing one specific device operation region. The overall expression is obtained by the combination of the individual control functions. The obvious, and thus most common way of dealing with such a problem, is to perform a blind nonlinear optimization of the overall model parameters. From my point of view, this approach is not the appropriate one, since it is very time consuming and the user has a very limited control over the model extraction procedure. The chosen approach breaks the overall problem into smaller sections related with the device operation regions. Furthermore, this method enables a fast model readjustment. In order to illustrate the nonlinear drain-source current model parameter extraction procedure, a study of the individual expressions will be performed and, after that, a step by step $i_{DS}(v_{GS},v_{DS})$ fitting is presented. In each step, the present stage versus the final function will be shown. We will start with the model's dependence on v_{GS}.

Threshold Location

The threshold voltage, V_T, [unclear in $i_{DS}(v_{GS})$ due to the FET's soft turn-on] can be precisely extracted from the $G_{m2}(v_{GS})$ peak or $G_{m3}(v_{GS})$ null, [25].

$$v_{GS1}(v_{GS}) = v_{GS} - V_T \tag{6}$$

This linear function, responsible for the threshold location, is illustrated in Fig. 45, for three different values of V_T, (V_{T1}=-2, V_{T2}=-1 and V_{T3}=0).

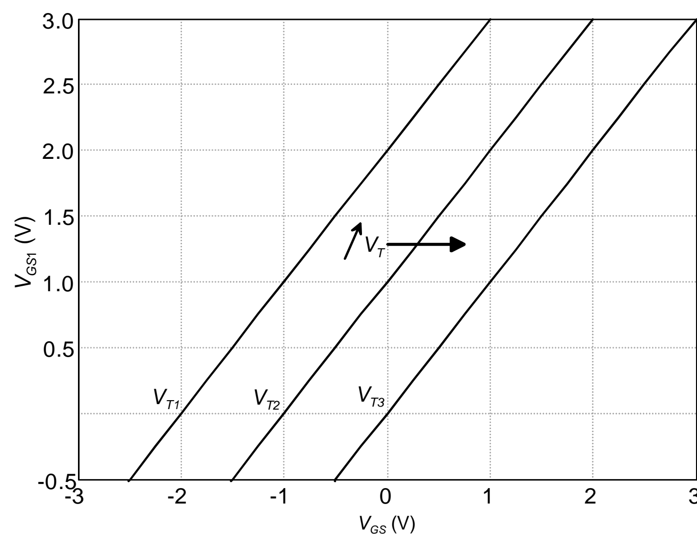

Fig. 45. Variation of the threshold voltage, for three different values of *VT*, (V_{T1}=-2, V_{T2}=-1 and V_{T3}=0).

Saturation Smoothness

This second step, responsible for the $i_{DS}(v_{GS})$ saturation smoothness, for high values of v_{GS}, and for the important transconductance decrease, observed in these HFETs, was previously proposed in the MET model, [53].

$$v_{GS2}(v_{GS}) = v_{GS} - \frac{1}{2}\left(v_{GS} + \sqrt{(v_{GS} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2} \right) \tag{7}$$

The control function, v_{GS2}, depends on both VK and Δ. In order to study the importance that each parameter has on the overall function, two different situations were considered: the first one studies the effect of VK when Δ is zero and, the second one, the effect of Δ when VK is zero.

So, setting Δ to zero, we can re-write (7) as:

$$v_{GS2}(v_{GS}) = v_{GS} - \frac{1}{2}\left(v_{GS} + |v_{GS} - VK| - |VK| \right) \tag{8}$$

Fig. 46 presents the variation of v_{GS2}, when Δ equals zero, for three different values of VK, (VK_1=0, VK_2=2 and VK_3=4).

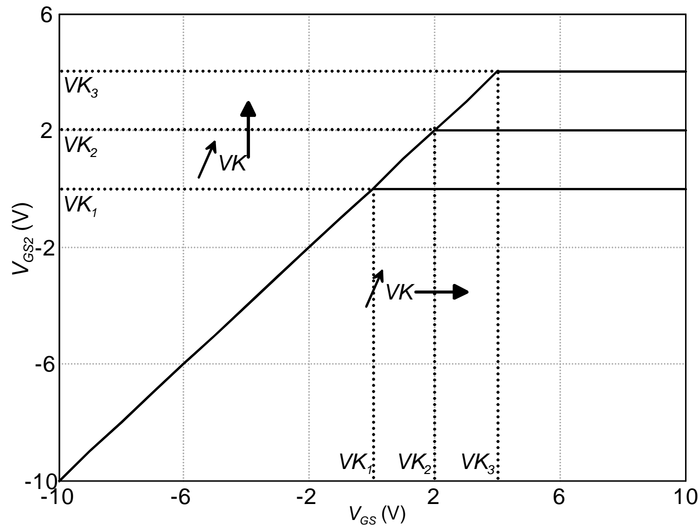

Fig. 46. Variation of the effective voltage when Δ =0, for three different values of *VK*, (*VK*$_1$=0, *VK*$_2$=2 and *VK*$_3$=4).

As it is possible to see, *VK* represents the gate voltage at which the device becomes saturated.

Now, re-writing (7) for the case where *VK* equals zero, we will get:

$$v_{GS2}(v_{GS}) = v_{GS} - \frac{1}{2}\left(v_{GS} + \sqrt{{v_{GS}}^2 + \Delta^2} - |\Delta|\right) \tag{9}$$

Fig. 47 presents the corresponding variation of v_{GS2}, for three different values of Δ, (Δ_1=0, Δ_2=2 and Δ_3=4).

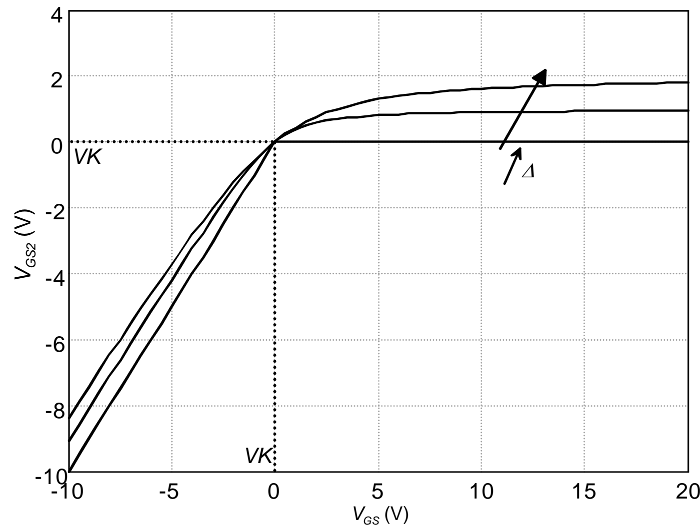

Fig. 47. Variation of the effective voltage when *VK*=0, for three different values of Δ, (Δ_1=0, Δ_2=2 and Δ_3=4).

As it is possible to see in Fig. 47, Δ controls the saturation smoothness. If Δ is zero, we will have a sharp transition between the linear region and saturation but, as Δ becomes greater than zero, this transition becomes much more soft.

After considering these two limit situations (*VK*=0 and Δ=0), it is now easy to understand that, when both parameter values are different from zero, both effects will work together. However, the behaviour principles just presented will be kept.

Turn-on Abruptness

For accurately describing the FET's sub-threshold conduction and soft turn-on, the expression used is a smoothed version of the usually assumed piece-wise characteristic.

$$v_{GS3}(v_{GS}) = VST \cdot \ln\left(1 + e^{v_{GS}/VST}\right) \tag{10}$$

This expression, first proposed in [54] for MESFETs and, after that, used for Si LDMOS in [55] and [33], provides a smooth and continuously differentiable approximating function to the device turn-on.

The only parameter involved, VST, controls the effective gate voltage, v_{GS3}, exponential increase rate. This is illustrated in Fig. 48, for three different values of VST, (VST_1=0.1, VST_2=0.3 and VST_3=0.5).

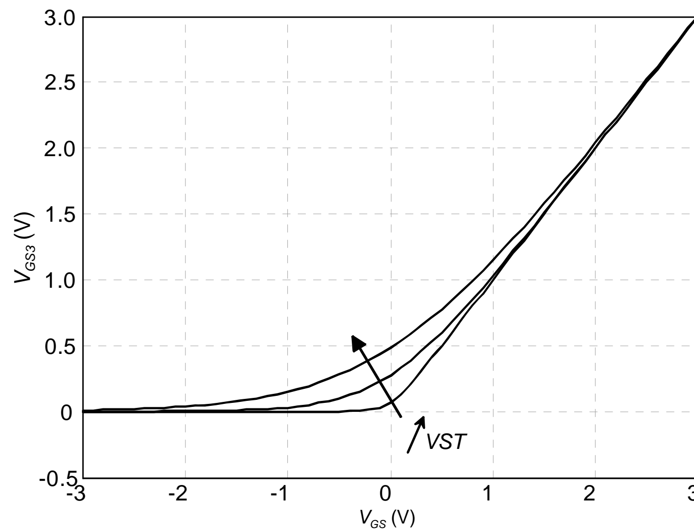

Fig. 48. Variation of the effective voltage, for three different values of *VST*, (*VST*1=0.1, *VST*2=0.3 and *VST*3=0.5).

If we take a closer look at (10) and at Fig. 48, we can se that v_{GS3} will asymptotically tend to v_{GS} or to zero for high or low v_{GS} values, respectively.

Transition between Turn-on and Saturation

$$i_{DS1}(v_{GS}) = \beta \cdot \frac{v_{GS}^{2}}{1 + \frac{v_{GS}^{plin}}{V_L}} \tag{11}$$

As is well known, short channel FETs present an exponential turn-on followed by the typical FET quadratic region, which, for high v_{GS} voltage, becomes smoothly linearized. This expression is used to control the regions of the referred $i_{DS}(v_{GS})$ quadric and linear regions. Indeed, when *plin* is close to zero the $i_{DS}(v_{GS})$ behaviour is always quadratic. When *plin* is close to one this $i_{DS}(v_{GS})$ dependence asymptotically tends to the short channel linearized region for v_{GS} values higher than the constant V_L. The other parameter involved, β, is simply a scaling factor.

$f(v_{GS}, v_{DS})$ Construction

Basically, the various fitting parameters are used to set the transitions in the different regions and their relative abruptness. This allows an almost one-by-one first parameter set extraction. Unfortunately, since there is no absolute orthogonality, the final parameter set must be obtained from a fine optimization of the modelled and measured G_m, G_{ds}, G_{m2} and G_{m3} functions. The error function used was defined as follows:

$$\varepsilon = \frac{\left|G_{m\,meas} - G_{m\,\mathrm{mod}}\right|}{\max\left(G_{m\,meas}\right)} + \frac{\left|G_{ds\,meas} - G_{ds\,\mathrm{mod}}\right|}{\max\left(G_{ds\,meas}\right)} + \frac{\left|G_{m2\,meas} - G_{m2\,\mathrm{mod}}\right|}{\max\left(G_{m2\,meas}\right)} + \frac{\left|G_{m3\,meas} - G_{m3\,\mathrm{mod}}\right|}{\max\left(G_{m3\,meas}\right)} \tag{12}$$

The nonlinear equations (6), (7), (10) and (11) can now be combined to create (13)-(16), defining the complete nonlinear current equations, as a function of v_{GS}. For each intermediate expression, we will present the current stage and the final function, Fig. 49 up to Fig. 52.

$$v_{GS1}(v_{GS}) = v_{GS} - V_T \tag{13}$$

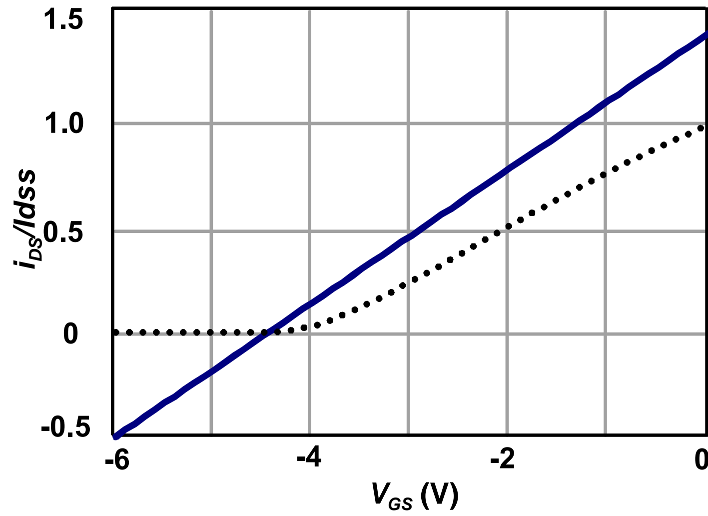

Fig. 49. First stage current (—) and final function (•••).

$$v_{GS2}(v_{GS1}) = v_{GS1} - \frac{1}{2}\left(v_{GS1} + \sqrt{(v_{GS1} - VK)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right) \tag{14}$$

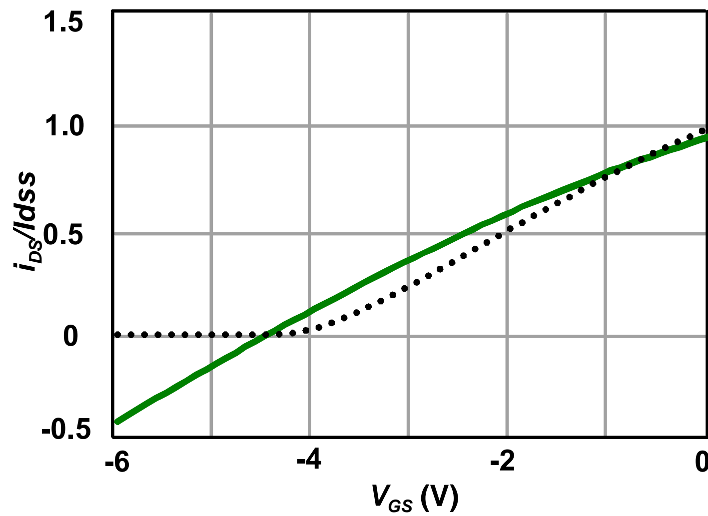

Fig. 50. Second stage current (—) and final function (•••).

$$v_{GS3}(v_{GS2}) = VST \cdot \ln\left(1 + e^{v_{GS2}/VST}\right) \tag{15}$$

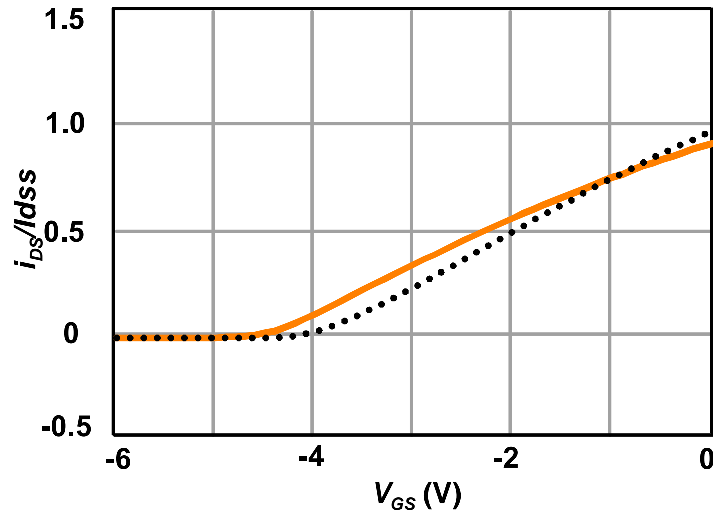

Fig. 51. Third stage current (—) and final function (•••).

$$i_{DS1}(v_{GS}) = \beta \cdot \frac{v_{GS3}{}^{2}}{1 + \frac{v_{GS3}{}^{plin}}{V_L}} \tag{16}$$

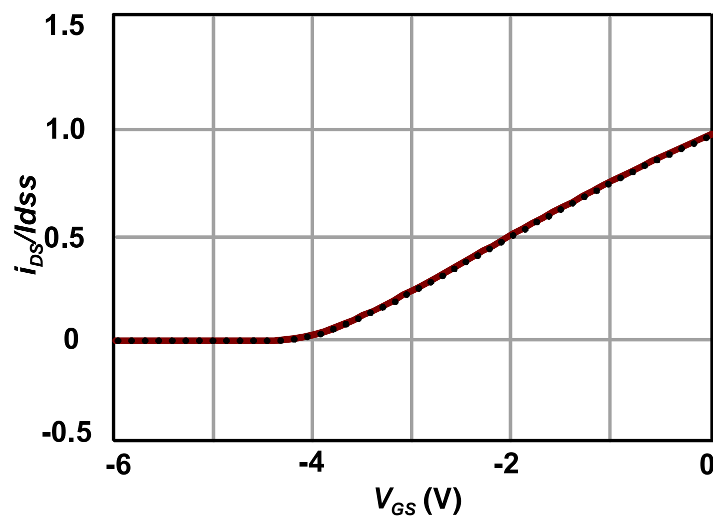

Fig. 52. Comparison between measured and modeled $i_{DS}(v_{GS})$ values.

i_{DS} Dependence on v_{DS}

In what the $i_{DS}(v_{DS})$ dependence is concerned, the model relies on the traditional Curtice hyperbolic tangent function to set the linear to saturation regions' transition, beyond a linear factor to account for the non-null G_{ds} in saturation. However, the argument of the $\tanh(v_{DS})$ was modified to reproduce the displacement of the knee voltage with v_{GS}.

$$i_{DS}(v_{GS},v_{DS}) = i_{DS1}(v_{GS}) \cdot (1 + \lambda \cdot v_{DS}) \cdot \tanh\left(\frac{\alpha \cdot v_{DS}}{v_{GS3}{}^{psat}}\right) \tag{17}$$

Both α and λ can be easily extracted from the pulsed current-voltage (IV) curve slopes in the linear region and saturation, respectively or from $G_{ds}(v_{GS},v_{DS})$. The parameter *psat* sets the dependence on v_{GS} of the transition from the triode to saturated region.

It is also necessary to consider the dependence of V_T with V_{DS}, which can be acquired from several third order harmonic or intermodulation tests. For each V_{DS}, the V_{GS} value in which an IM3 null occurs gives the value of V_T. Then, the parameter γ can be extracted to fit these measured $V_T(v_{DS})$:

$$V_T(v_{DS}) = V_T + \gamma \cdot v_{DS} \tag{18}$$

This in-house model, although able of also reproducing the desired bell-shaped transconductance of an HEMT, is capable of a much more flexible $i_{DS}(v_{GS})$ fit. Indeed, and contrary to the $\{1+\tanh[\psi(v_{GS})]\}$ form of the Chalmers Model, this new $f_1/[1+f_2(x)]$ current saturating function, in which x is another saturating function of v_{GS}, has the ability of allowing a more independent control on the $G_m(v_{GS})$ turn-on abruptness, subsequent $G_m(v_{GS})$ saturation smoothness and transconductance peak broadness.

Table 4 presents the obtained $i_{DS}(v_{GS},v_{DS})$ model parameter set.

Table 4. In-House $i_{DS}(v_{GS}, v_{DS})$ model parameter values.

Parameter	Value
β	0.40 A/V^2
V_{T0}	-4.425 V
VST	0.15 V
VK	4 V
Δ	5 V
V_L	1.35 V
λ	0.0256 V^{-1}
α	0.40 V^{-1}
$psat$	-0.62
$plin$	1
γ	0

Fig. 53 up to Fig. 56 show the resulting prediction of the small-signal $G_m(v_{GS})$, $G_{ds}(v_{GS})$ and the corresponding $G_m(v_{GS})$ higher order derivatives: $G_{m2}(v_{GS})$ and $G_{m3}(v_{GS})$ for a constant V_{DS} in the saturation zone.

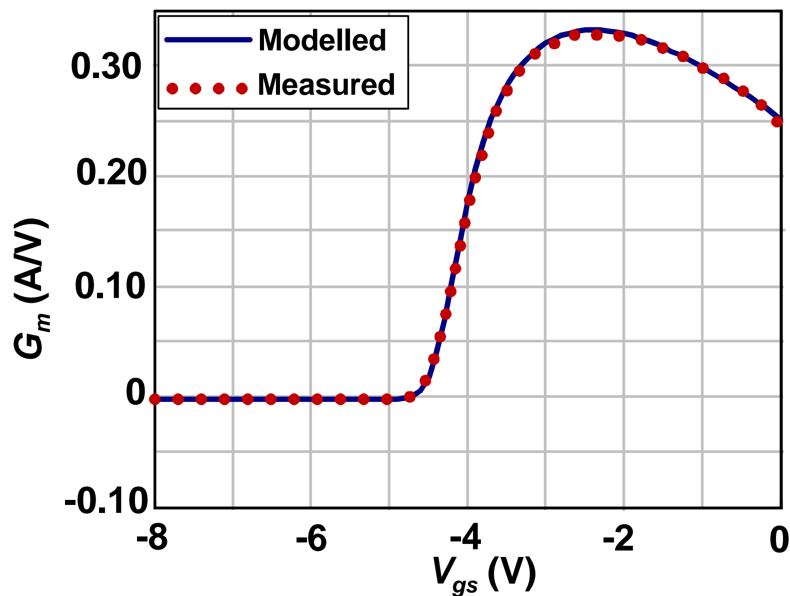

Fig. 53. G_m measured and modelled with the In-House Model, for a constant V_{DS} of 6 V.

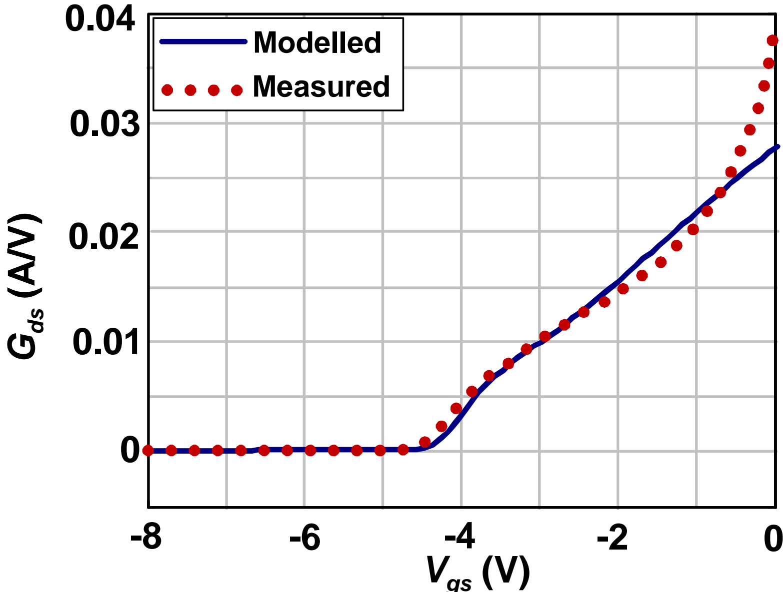

Fig. 54. G_{ds} **measured and modelled with the In-House Model, for a constant** V_{DS} **of 6 V.**

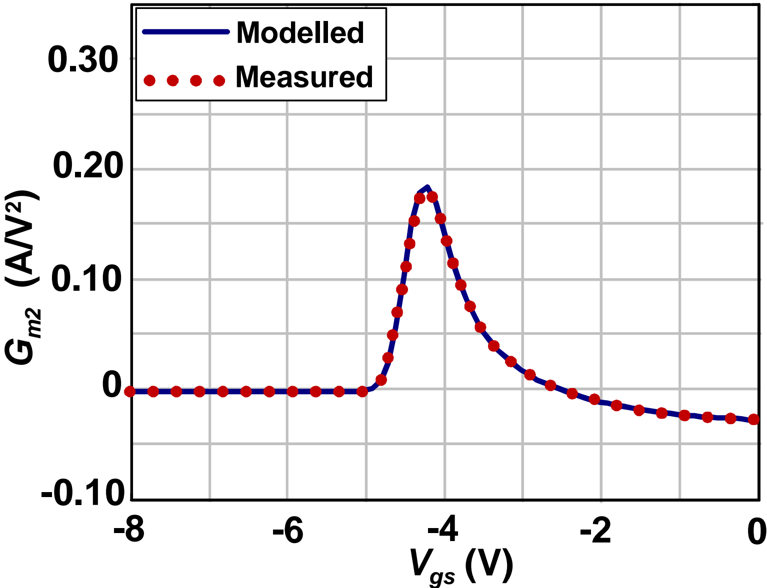

Fig. 55. G_{m2} **measured and modelled with the In-House Model, for a constant** V_{DS} **of 6 V.**

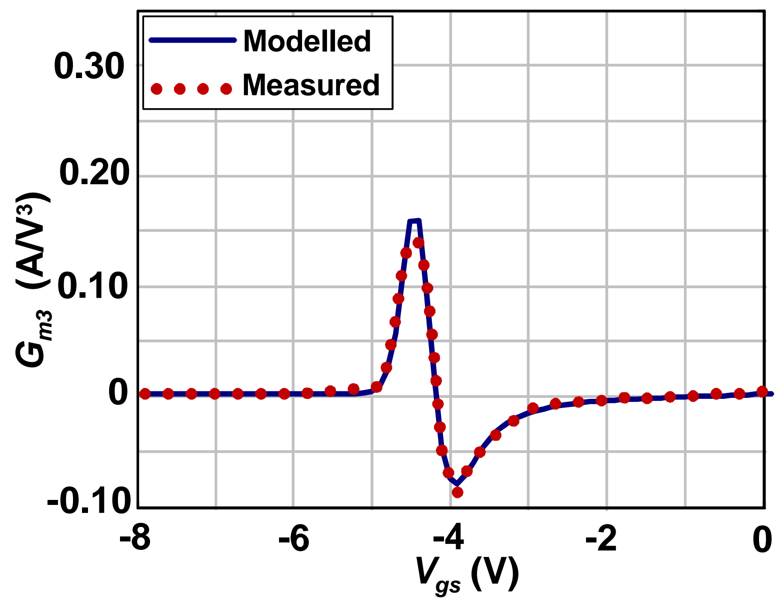

Fig. 56. G_{m3}**, measured and modelled with the In-House Model, for a constant** V_{DS} **of 6 V.**

Note the remarkable good agreement, up to 3rd order, obtained with this $i_{DS}(.)$ model.

2.2.3. Gate-Source Capacitance Nonlinear Model

For the nonlinear gate-source capacitance, $C_{gs}(v_{GS})$, we used the model proposed in [33].

$$C_{gs}(v_{GS}) = C_{gs0} + \frac{A_{C gs}}{2} \cdot \left(1 + \tanh\left[K_{C gs} \cdot \left(v_{GS} - V_{C gs}\right)\right]\right) \qquad (19)$$

As expressed in (12), a constant (C_{gs0}) plus a hyperbolic tangent are used to describe C_{gs} behaviour with v_{GS}, which determines a ramp plus a $\ln\left[1+e^{v_{GS}}\right]$ charge. As in the $i_{DS}(.)$ model, the parameters of (12) are used to control the position (V_{Cgs}) and the abruptness (K_{Cgs}) of the transition between the residual C_{gs0} and the actual depletion capacitance.

Fig. 57 shows the comparison between modelled and measured $C_{gs}(v_{GS})$ values (obtained from the S-parameter data previously collected, using the method explained in [49]).

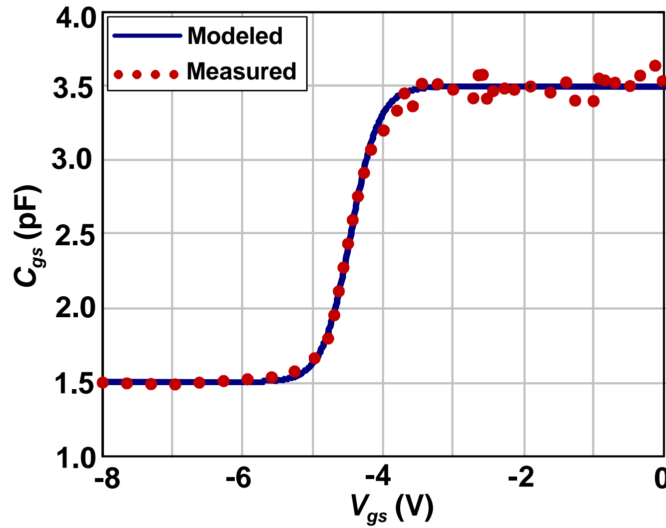

Fig. 57. Comparison between measured and modelled $C_{gs}(v_{GS})$ values.

The complete $C_{gs}(v_{GS})$ parameter set is shown in Table 5.

Table 5. In-House $C_{gs}(v_{gs})$ model parameters.

Parameter	Value
C_{gs0}	1.5 pF
A_{Cgs}	2.0 pF
K_{Cgs}	2.0 V^{-1}
V_{Cgs}	-4.5 V

2.2.4. Schottky Junction Nonlinear Model

Finally, the gate-source and gate-drain diodes were considered as approximately equal and modelled by the conventional Schottky formula.

$$I_G = I_S\left(e^{\frac{v_{GS}}{\eta V_T}} - 1\right) \quad (20)$$

Where:

I_G is the diode current,

I_S is a scale factor called the saturation current,

v_{GS} is the voltage across the diode,

V_T is the thermal voltage,

and η is the ideality coefficient.

The thermal voltage V_T is approximately 25.9 mV, at room temperature (approximately 25ºC or 298K), given by:

$$V_T = \frac{kT}{e} \quad (21)$$

where:

e is the electron charge,

k is Boltzmann's constant,

T is the absolute temperature of the p-n junction.

The inverse saturation current, I_S, and ideality factor, η, were extracted from measured I_G versus v_{GS} data, when source and drain were short-circuited.

Fig. 58a shows the I/V characteristic of the Schottky diode, in cartesian coordinates, and Fig. 58b the same characteristic plot now on semilog axis and, superimposed to it, the best regression line.

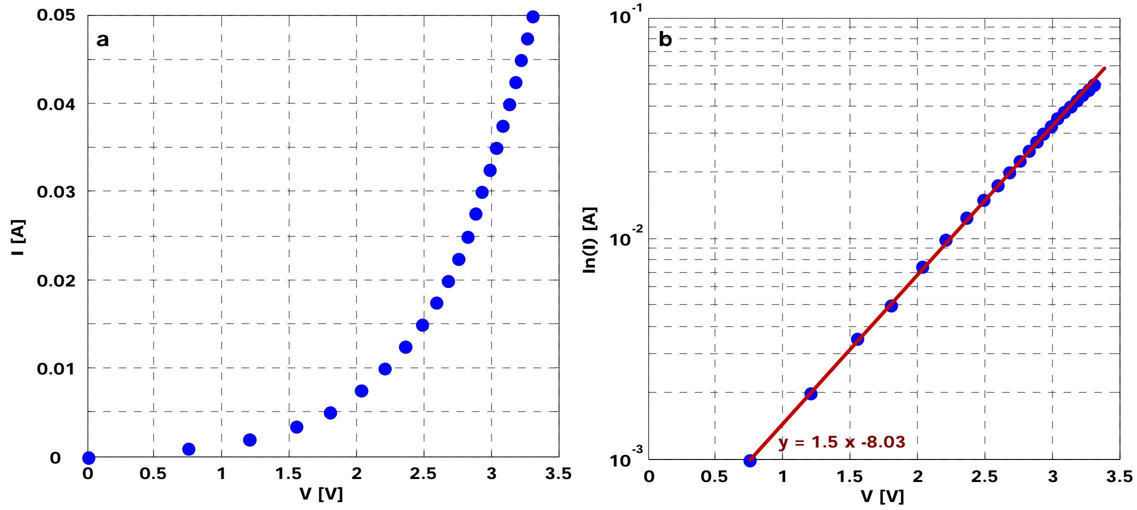

Fig. 58. a) I/V characteristic of the Schottky diode in cartesian coordinates and b) the same characteristic plot on semilog axis.

That led to the parameters shown in Table 6.

Table 6. Gate-Channel junction model parameters.

Parameter	Value
I_S	3.25e-4 A
η	26

A note on these values is obviously required as they seem well far from the ordinary ones observed in similar GaAs or Si based MES junctions. They are a direct consequence of the measured low currents for comparably large applied voltages. In fact, currents on the order of a few mA could only be observed for applied forward voltages of nearly 1.5 V, while 100 mA were measured for unexpected values of around 3.5 V. Furthermore, the rather large I_s value was verified against the diode currents measured under reverse bias. Although some process variation was observed for those values, they all seemed to be much larger than the ones of GaAs and Si devices. If such a trend is confirmed in other GaN technologies, this could be an indication that such wide bandgap HEMTs allow a very high input voltage excursion before gate-channel junction clamping takes place.

2.3. Conclusions

In this chapter, the GaN devices used were presented. Besides that, an equivalent circuit nonlinear global model was formulated and extracted for the 2mm GaN power HEMT. Modelling studies proved that the form now adopted for the $i_{DS}(v_{GS},v_{DS})$ characteristic was found more flexible than the standard HEMT model developed for GaAs devices. That allowed a precise fitting of measured small-signal $G_m(v_{GS})$, $G_{ds}(v_{DS})$ and thus of $i_{DS}(v_{GS})$ higher order derivatives $G_{m2}(v_{GS})$ and $G_{m3}(v_{GS})$.

3. GaN Nonlinear Model Validation

This chapter is dedicated to the GaN nonlinear device model validation stage, performed at the transistor level and using a real PA. The tests used in this comparison were: small-signal S-parameters, AM/AM and AM/PM conversions and large-signal one- and two-tone measurements.

At this stage, the nonlinear model previously extracted had to be implemented in a standard harmonic balance simulator (Agilent's Advanced Design System, [56]), enabling the comparison between measurements and results obtained with the model, when the overall measurement setup is carefully reproduced in the simulator.

The $i_{DS}(v_{GS},v_{DS})$ and $C_{gs}(v_{GS})$ nonlinear equations were introduced in the simulator, using a two-port symbolic defined device (SDD), that enables the creation of equation based, user-defined, nonlinear components specifying algebraic relationships between port voltages, currents, and their derivatives.

Fig. 59 shows the SDD and the equations used for the drain-source current and gate-source capacitance (defined in its charge form).

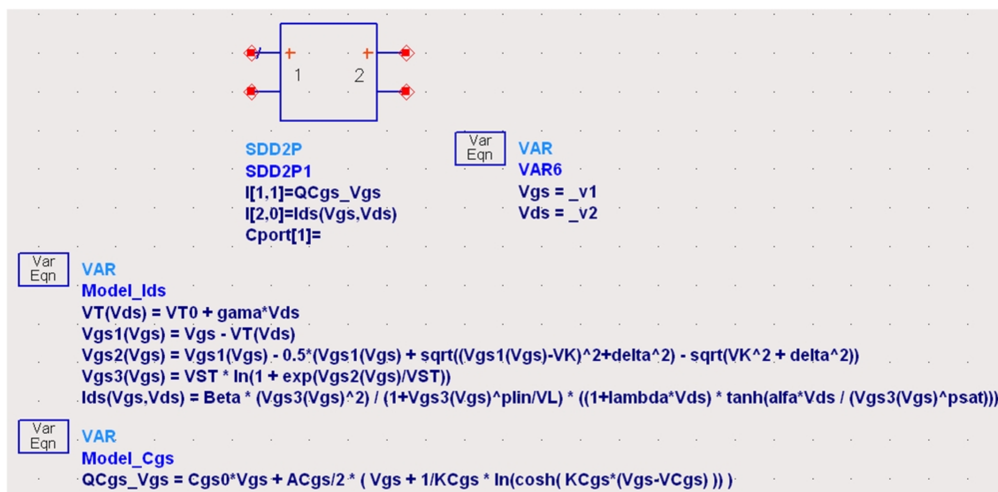

Fig. 59. SDD and the equations used for the drain-source current and gate-source capacitance (defined in its charge form).

The other equivalent circuit elements were then added to the schematic. Fig. 60 presents the complete nonlinear equivalent circuit model implementation in that simulator and Fig. 61, the correspondent sub-circuit component.

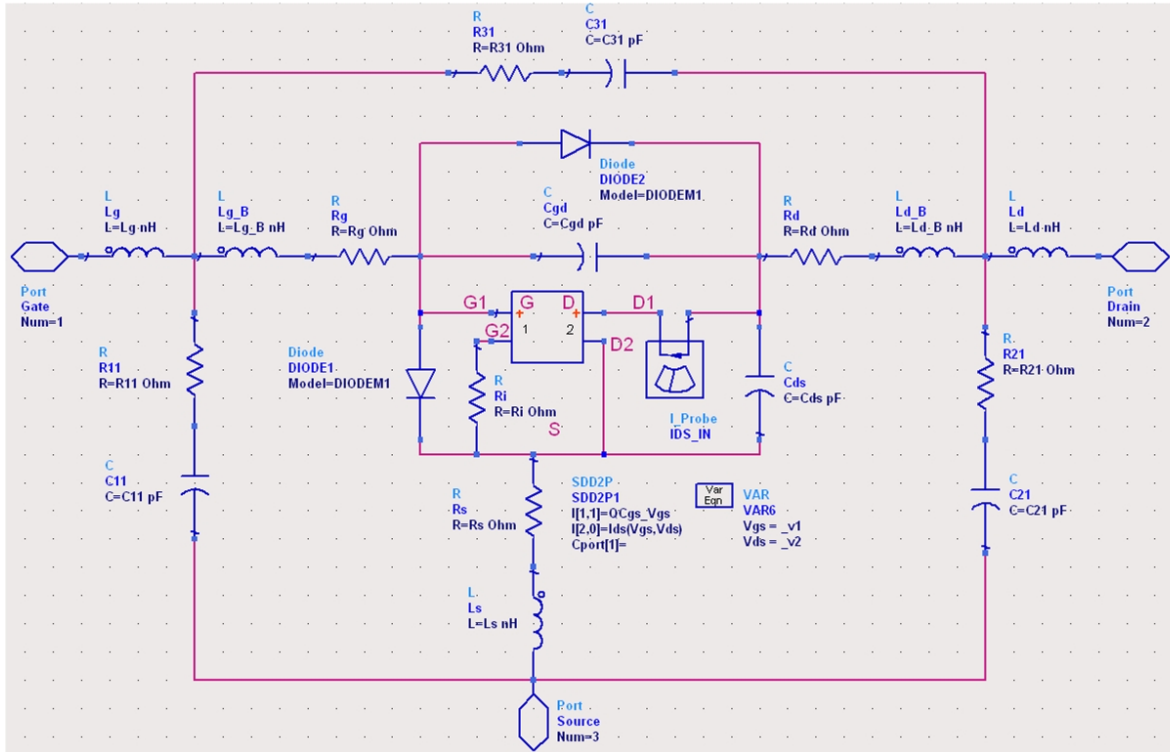

Fig. 60. Nonlinear equivalent circuit model implementation in Agilent's Advanced Design System.

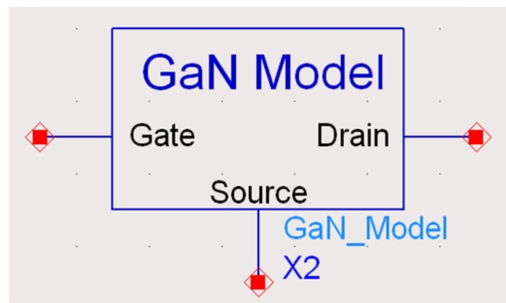

Fig. 61. Sub-circuit component.

3.1. Model Validation at the Transistor Level

The first model validation phase was performed at the transistor level. Fig. 62 shows the actual setup implementation.

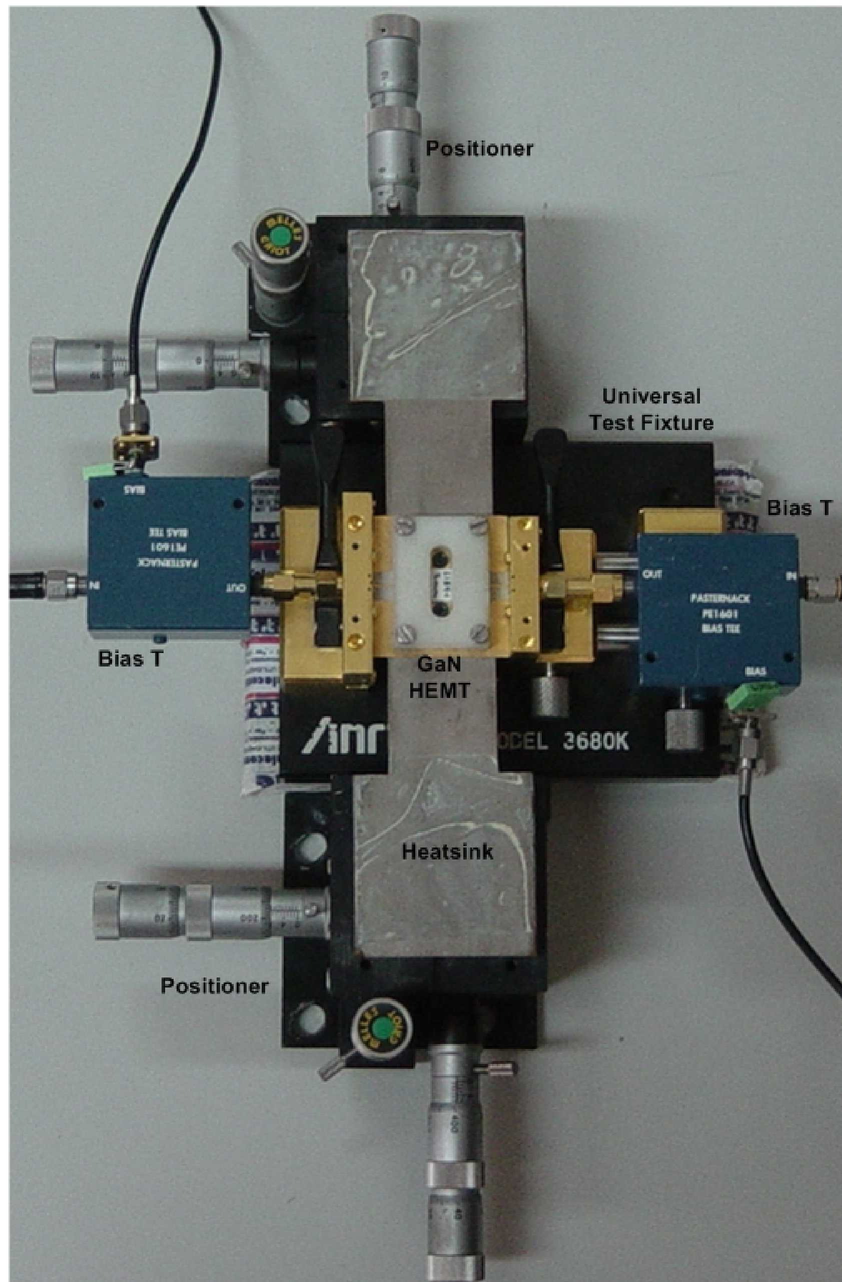

Fig. 62. Actual setup implementation used during the model validation at the transistor level.

3.1.1. Small-Signal S-parameter Measurements

The first validation tests consisted in the comparison of modelled and measured, broad band small-signal S-parameter measurements, from 1 MHz to 1 GHz, taken for three different bias points: a quiescent point below V_T, a quiescent point slightly above V_T, and another one well above V_T (corresponding to what would be respectively classified as Class C, AB and A in a power amplifier application), see Fig. 63.

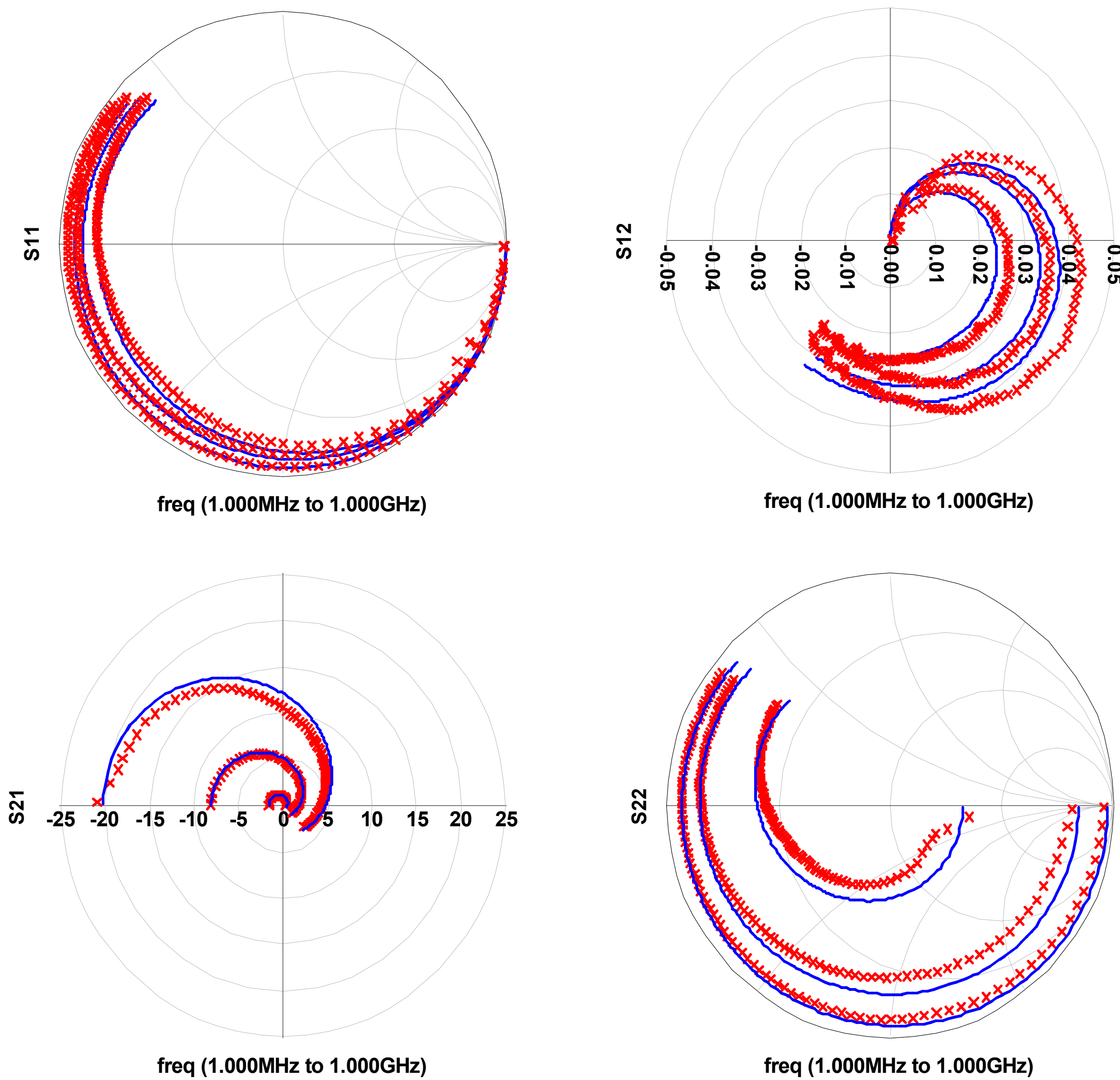

Fig. 63. S-parameters measured (x) and simulated (–) with the In-House Model for 3 different bias points corresponding to Class C, AB and A operation.

As it is possible to see, the results obtained with the In-House Model can be considered very good, especially if one realizes the parasitics introduced by the transistor mounting and large package. These were, in fact, responsible for the frequency limitations.

3.1.2. AM/AM and AM/PM Measurements

Since these wide bandgap transistors are primarily intended for PA applications in the emerging terrestrial and spatial communication systems, which use complex modulation schemes, several AM/AM and AM/PM conversion measurements were conducted. The transistor was biased to operate under class AB (v_{GS}=-4.20V), while V_{DS} was kept constant at 6V. This bias point provides the best compromise between Pout, IMD and PAE, [25], often required in PA applications.

Fig. 64 and Fig. 65 show static AM/AM and AM/PM conversion measurements and HB simulations, obtained with a 900 MHz CW excitation.

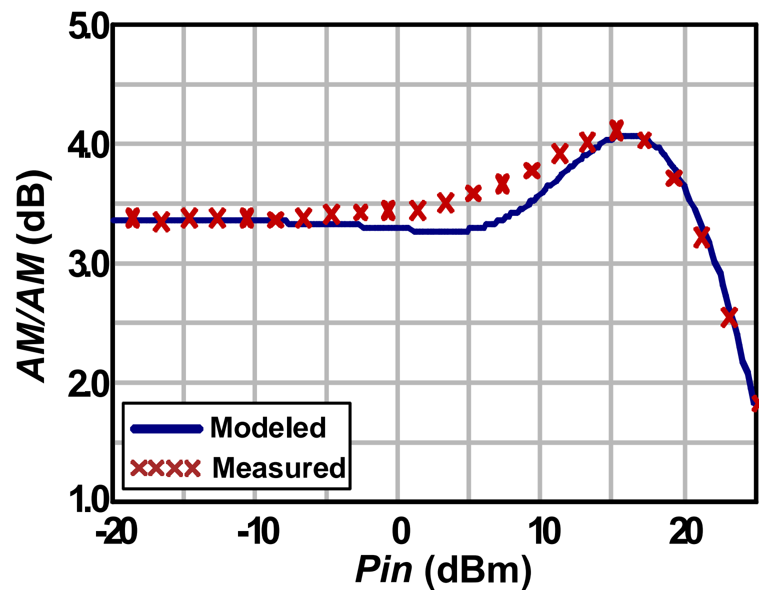

Fig. 64. Modelled and measured AM/AM conversion.

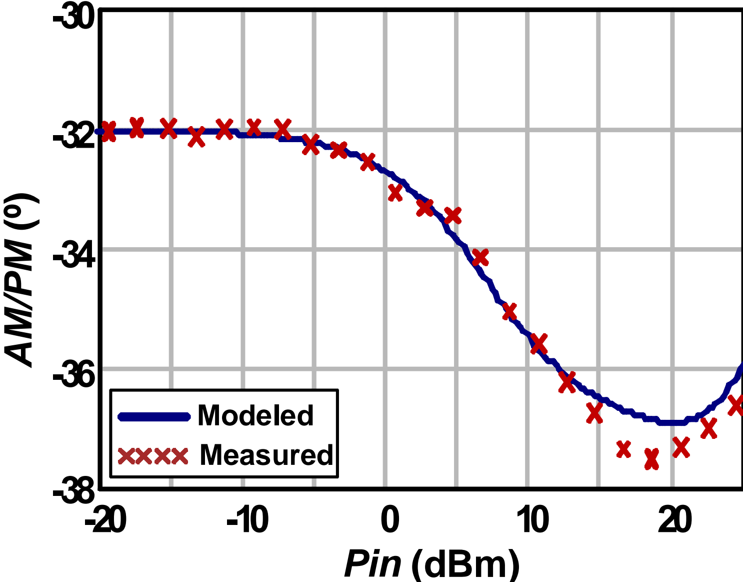

Fig. 65. Modelled and measured AM/PM conversion.

Looking into Fig. 64 and Fig. 65, it is possible to see that, not only the comparison between absolute values of measurements and simulations is quite good, but also the patterns are well reproduced throughout the whole input drive level.

3.1.3. Large-Signal Two-Tone Measurements

Afterwards, the model's IMD performance was evaluated. Keeping the transistor in Class AB (v_{GS}=-4.20V), a two-tone signal, centred at 900 MHz with a frequency separation of 10 MHz, was applied to the transistor's input. Fig. 66 presents the large-signal two-tone measurement setup.

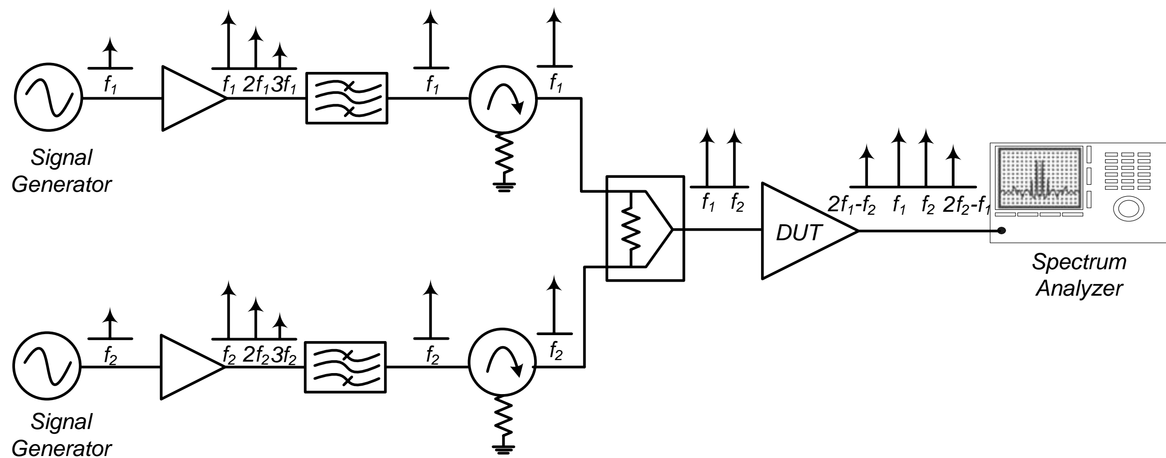

Fig. 66. Large-signal two-tone measurement setup.

The tone's power was swept from small- to large-signal regimes. Fig. 67 shows measurements and the model's predictions of the two fundamentals (f_1 and f_2) and IMD components ($2f_1$-f_2 and $2f_2$-f_1) for the above referred bias operation point.

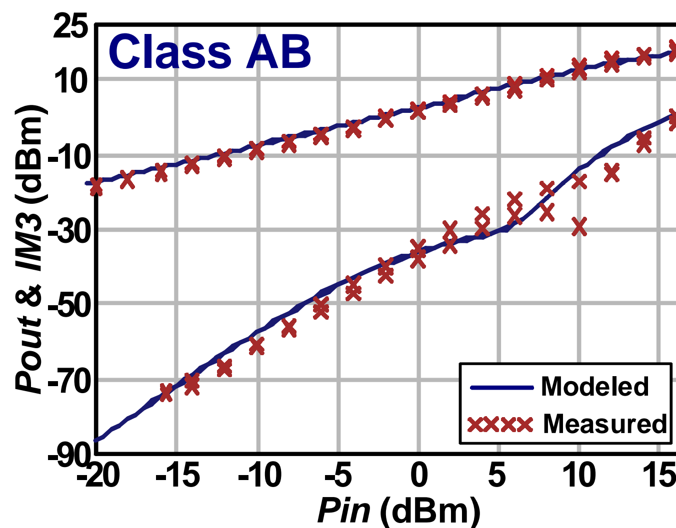

Fig. 67. Measured and simulated Pout and IM3 vs Pin for class AB operation (v_{GS}=-4.20V).

As it is possible to see, there is again a good agreement between the predicted and observed results.

A handy and practical property of these GaN HEMTs can be observed at class AB (Fig. 67). The presence of a notorious distortion valley in the IMD vs Pin pattern, can be used as an important tool to design highly efficient wireless PAs of also very good linearity, since it is known that, in this operation class, the device tends to present its optimized values of Pout and PAE. Previous studies, conducted for other FET device types [27, 33], led to the conclusion that those valleys, or, sometimes, even double minima, can be explained as the interaction of small- and large-signal IMD. Their prediction is thus determined by the model's ability in precisely describing the $i_{DS}(v_{GS},v_{DS})$ higher order derivatives [25, 42, 43].

More important than predicting the observations of a particular bias point is the model's capability of reproducing the dramatic variations of IMD vs Pin when there is a change of bias. Indeed, Fig. 68 and Fig. 69 show the two fundamentals (f_1 and f_2) and IMD components ($2f_1$-f_2 and $2f_2$-f_1) for classes C (v_{GS}=-4.50V) and A (v_{GS}=-3.0V), respectively.

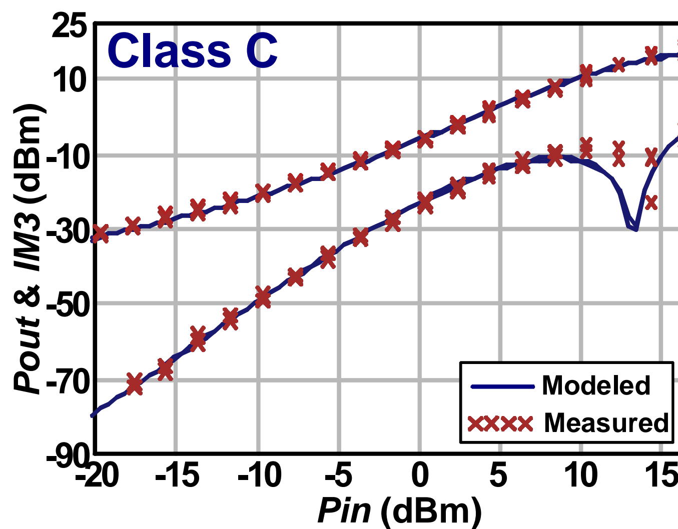

Fig. 68. Measured and simulated Pout and IM3 vs Pin for class C operation (v_{GS}=-4.50V).

For class C, in addition to a very good small-signal IMD description, the model can also predict, with very good accuracy, the observed large-signal IMD sweet-spot [8].

In class A, no large-signal IMD sweet-spot is either predicted by the model or observed in the measurements.

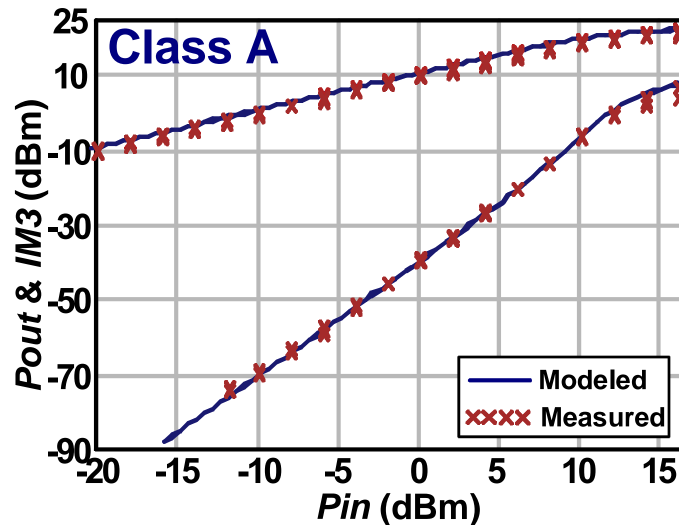

Fig. 69. Measured and simulated Pout and IM3 vs Pin for class A operation, (v_{GS}=-3.0V).

As seen in Fig. 67 up to Fig. 69, measured and simulated results compared remarkably well. Indeed, not only the general Pout and IMD behaviour is represented, as the details of the IMD versus Pin pattern are accurately described, allowing a thorough study of the model performance for various PA operation classes.

3.2. Model Validation under a real PA Application

In order to test the model in a real application environment, the next validation step was the comparison between measured and simulated results of a real PA circuit. For that, and using the GaN nonlinear device model previously extracted, we will now present the PA design stage.

Although the equivalent circuit model parameters had been extracted for a constant V_{DS} of 6 V, we decided to move it up to 20 V to take full profit of the device's output voltage and current excursion capabilities.

V_{GS} bias (PA operation class) was selected to simultaneously maximize Pout, IMR and PAE. After a few tests around V_T (i.e., close to class B and AB) it became clear that best performance could be achieved when the device presented double-minima in the IMD vs Pin pattern. This led to a quiescent point of about V_{GS1} = -4.20 V or 4% of I_{DSS}.

The output matching network design, for maximum output power, can be achieved using two different methods: load-pull or load-line approximation (Cripps method, [57]). The load-pull method provides a mapping between load impedance and output power level. From the obtained load contours, the PA designer can choose the optimum load impedance. Using the Cripps method, maximization of Pout and PAE demands a careful selection of the Cripps load-line and fine tuning of the even harmonics [57]. In what the choice of the fundamental class AB PA load line is concerned, [57], shows that:

$$R_{opt} = \frac{V_{DSQ} - V_{knee}}{\frac{I_{MAX}}{2}} \tag{22}$$

where:

V_{DSQ} is the drain supply voltage;

V_{knee} is the transistor knee voltage;

I_{MAX} is the maximum drain current.

These values are obtained from the I_{DS} versus V_{DS} plot, illustrated in Fig. 70.

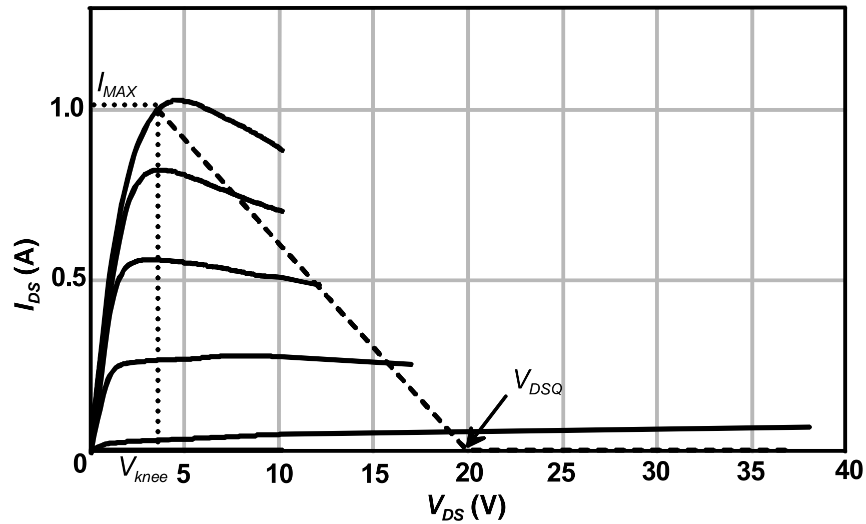

Fig. 70. (-) Measured i_{DS} vs v_{DS} characteristics, for six different v_{GS} values and (--) desired drain load line.

Fig. 71 shows the schematic used to determine the output matching network requirements in order to achieve drain constraints.

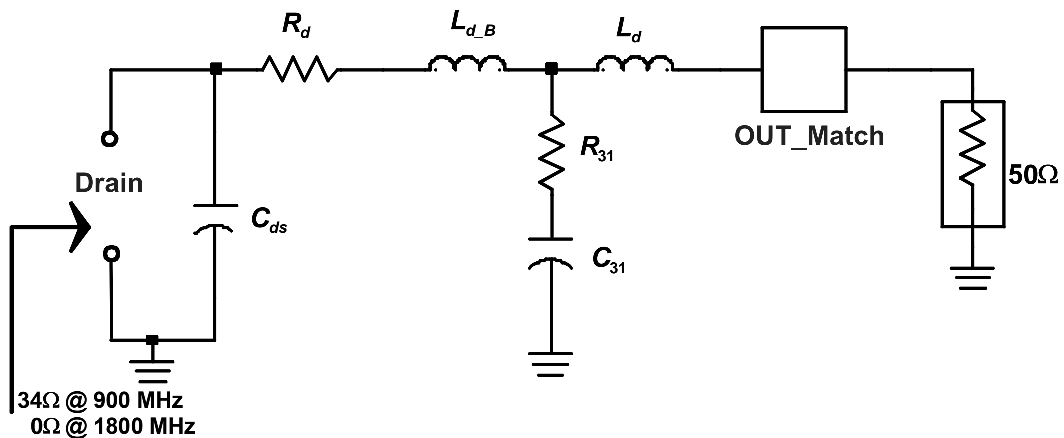

Fig. 71. Schematic used to determine the output matching network requirements.

A two-stub output matching network was designed to guarantee the calculated intrinsic 34Ω load-line at 900 MHz (central frequency) and a short-circuit at 1.8 GHz (2nd harmonic), see Fig. 71. Fig. 72 shows the simulated output match response at the drain from 900 MHz to 1800 MHz.

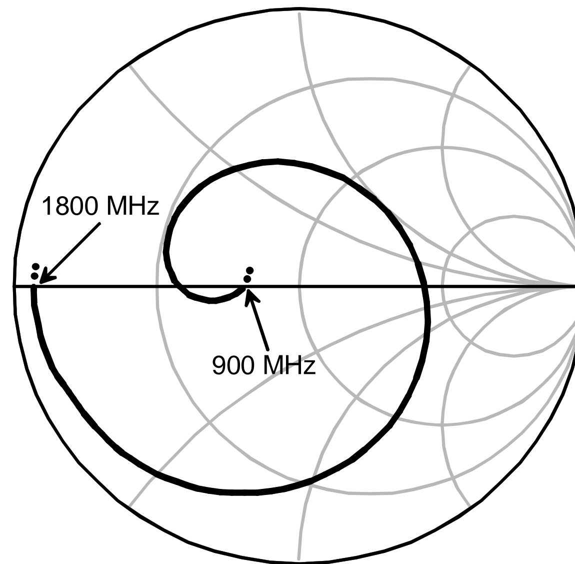

Fig. 72. Simulated output match response seen at the drain from 900 MHz to 1800 MHz.

After designing the output network, the next stage was to conceive an input network capable of providing possible source matching and optimized gain, without in-band instability. As it is known, that is important to compensate for the expected gain loss caused by the PA output mismatch. After this, a broad band stability analysis was conducted which showed potential problems at very high frequency (VHF). This was solved by the design of convenient lossy gate and drain bias networks.

However, since it is known that the bias circuitry also determines the device terminations at the envelope frequencies and thus nonlinear distortion performance, they were retuned to guarantee very low impedances at most of the envelope bandwidth (4 MHz).

Fig. 73 shows the simulated output match response at the drain from 30 kHz to 4 MHz.

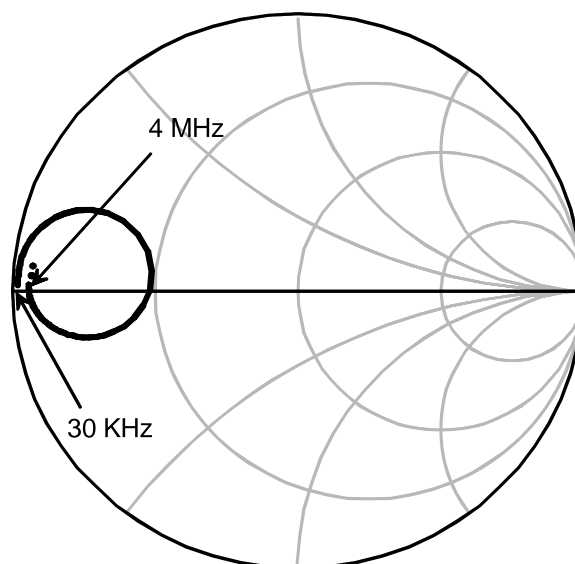

Fig. 73. Simulated output match response seen at the drain from 30 kHz to 4 MHz.

Fig. 74 shows the simulated i_{DS} vs v_{DS} characteristics, for six different V_{GS} biases and, superimposed to it, the desired and obtained drain load line.

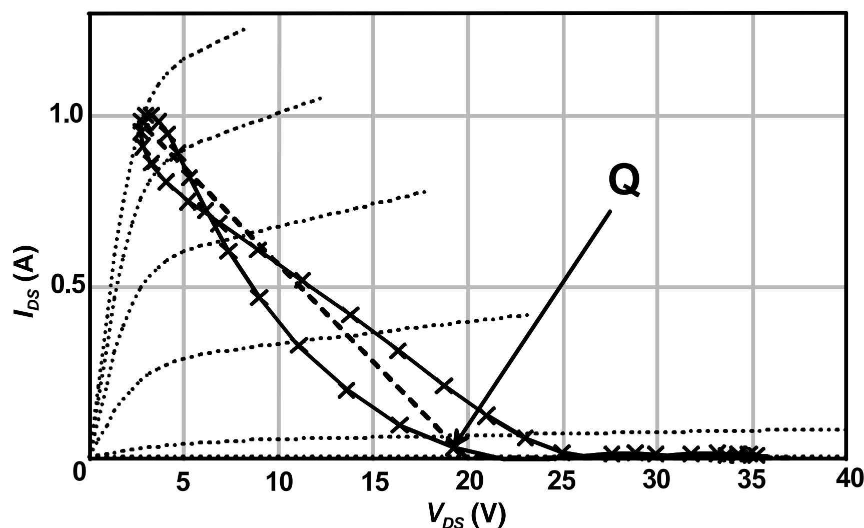

Fig. 74. (-) Simulated i_{DS} vs v_{DS} characteristics, for six different v_{GS} values, (--) desired and (-x-) obtained dynamic drain load line.

Comparing the I_{DS} vs V_{DS} characteristics, presented in Fig. 38 and predicted i_{DS} vs v_{DS} data of Fig. 74, it is possible to see that the simulated curves do not decrease. This was expected since, conceived to describe dynamic behaviour, and extracted to fit measured RF G_m and G_{ds},

the model does not include any self-heating or trapping effects. Although this will obviously affect the model predictions at dc, it will not compromise the primarily sought ac Pout and IMD characteristics.

The PA was implemented in MIC technology using a RT/Duroid high frequency laminate with a $\varepsilon_r = 10.2$. Fig. 75 and Fig. 76 show the final output and input matching networks schematics with all component values.

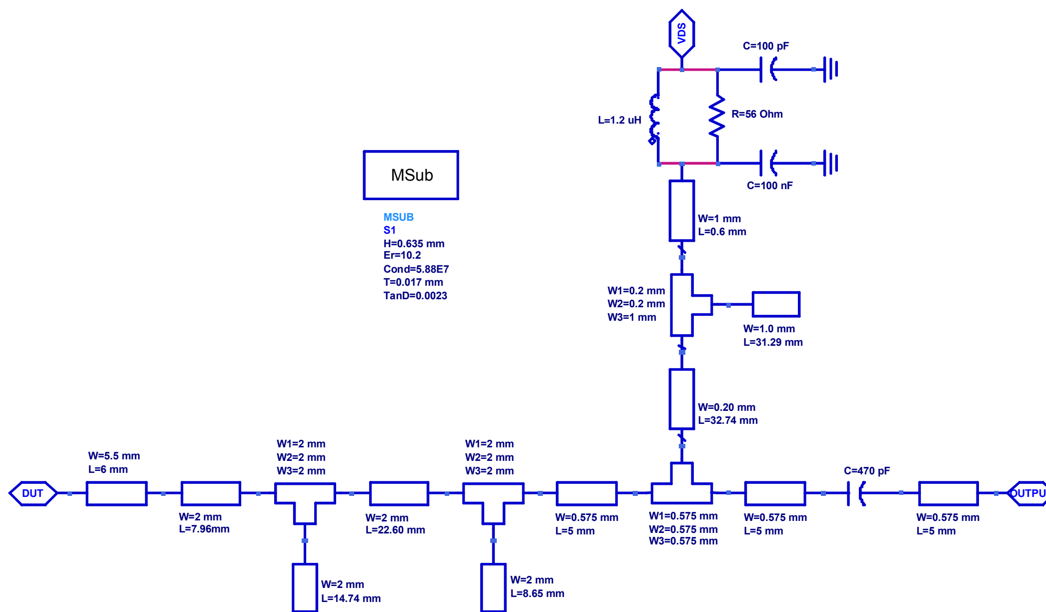

Fig. 75. Output matching network schematic with all component values.

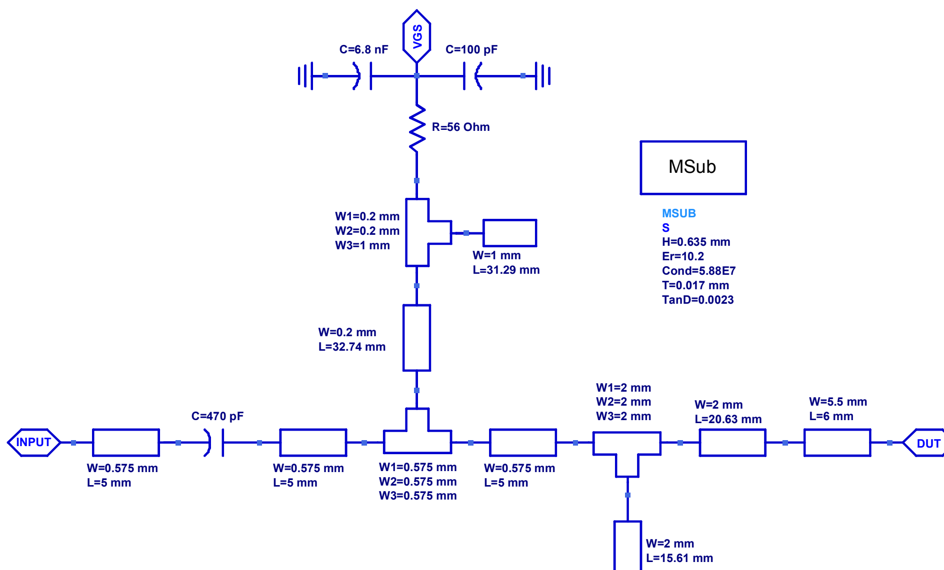

Fig. 76. Input matching network schematic with all component values.

Fig. 77 shows a photograph of the implemented amplifier board.

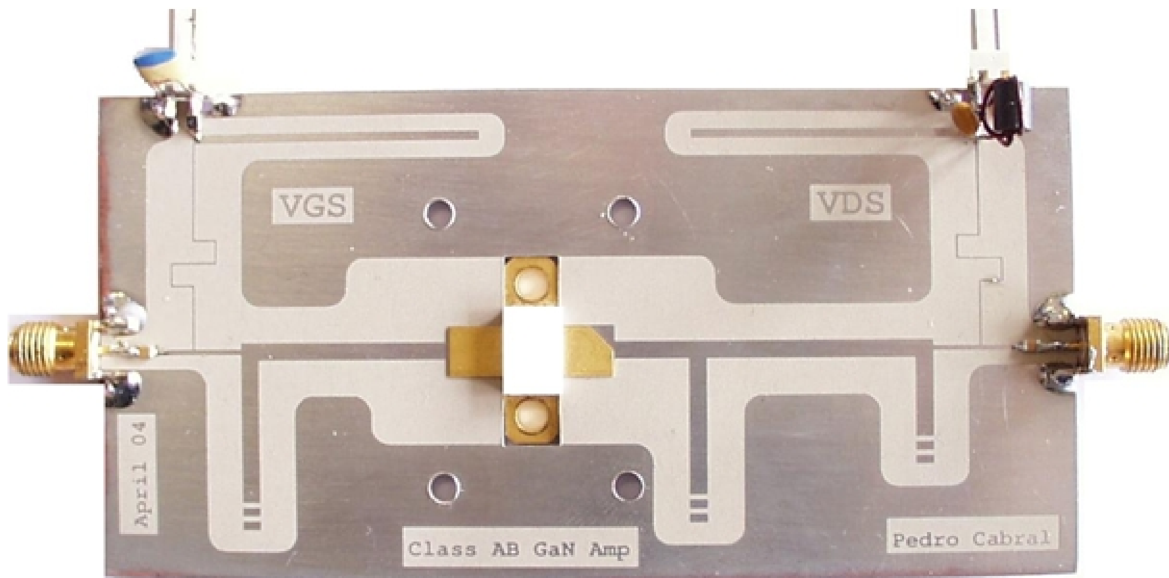

Fig. 77. Photograph of the implemented PA MIC board.

3.2.1. Small-Signal S-Parameter Measurements

Using the PA previously constructed, we passed to the comparison between measured and modelled broadband S-parameters. Fig. 78, Fig. 79 and Fig. 80 show those comparisons for $|S_{11}|$, $|S_{21}|$ and $|S_{22}|$, respectively.

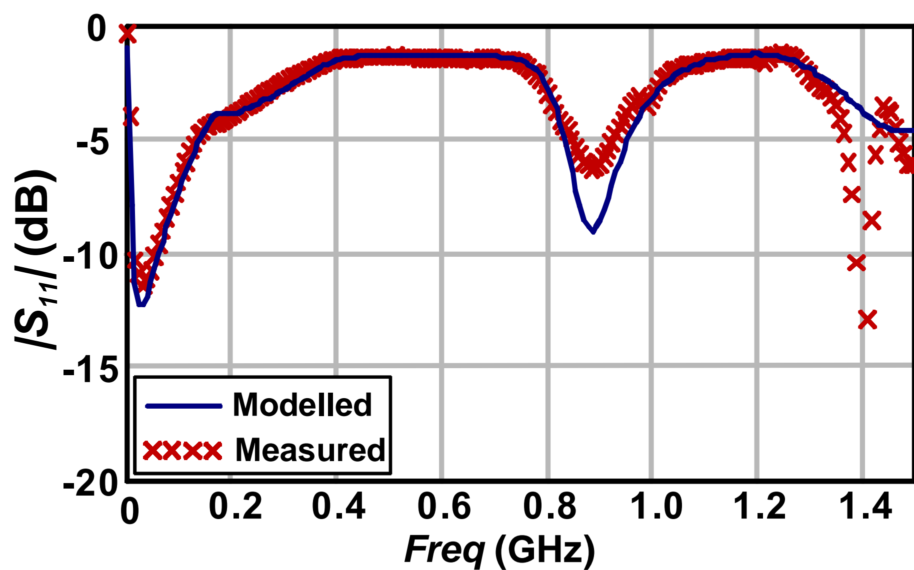

Fig. 78. Measured and modelled PA $|S_{11}|$.

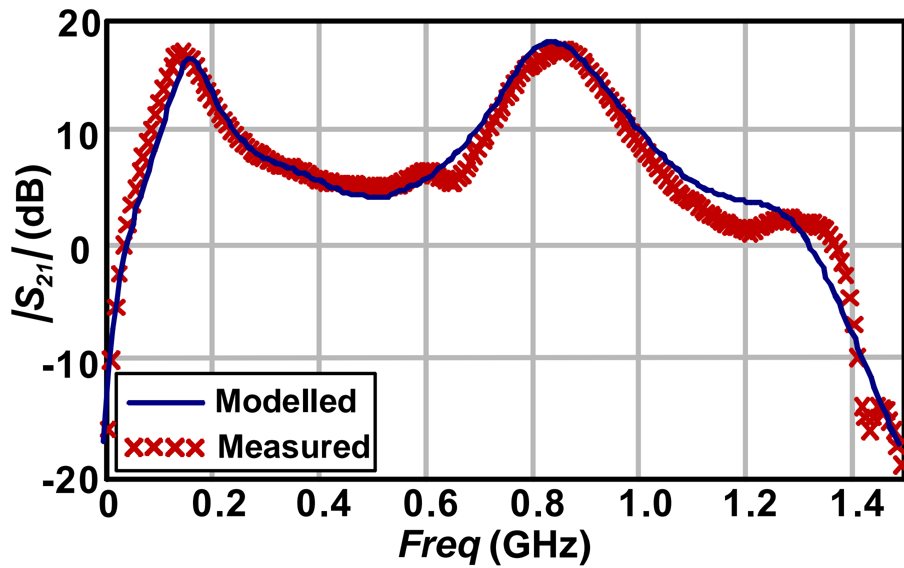

Fig. 79. Measured and modelled PA |S21|.

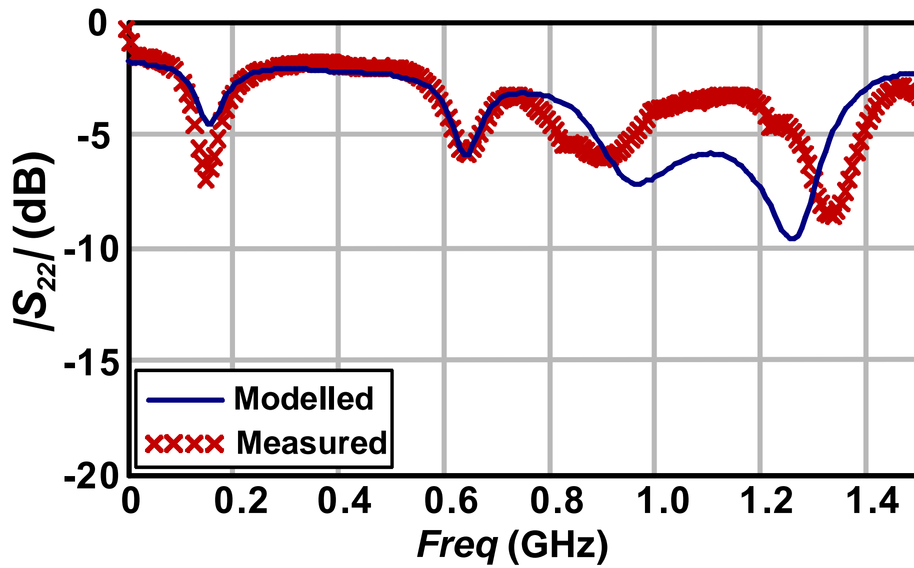

Fig. 80. Measured and modelled PA |S22|.

There is a reasonable good agreement between measured and modelled results. This attests the quality of the model's small-signal predictions, both in terms of the nonlinear functions' consistency and equivalent circuit element extraction. The discrepancy in the $|S_{22}|$ of Fig. 80 is estimated to be caused by the difference between V_{DS} values used in model extraction (6 V) and in amplifier design (20 V). Even so, the general shape of the curves is similar.

3.2.2. Large-Signal One-Tone Measurements

The second test step consisted in several 900 MHz CW experiments to evaluate the model capabilities of predicting transducer power gain, Pout and PAE versus input drive level.

The transistor was set to operate under class AB, operation (V_{GS}=-4.20 V) while V_{DS} was kept constant at 20V.

The setup used is presented in Fig. 81.

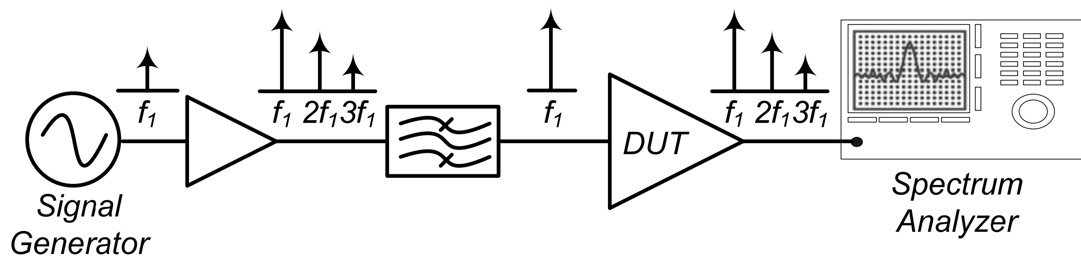

Fig. 81. Large-Signal one-tone measurement setup.

As seen in Fig. 82, the PA presents a 1dB compression point of 2 W with an associated Gain of 15 dB and a PAE of nearly 32 %.

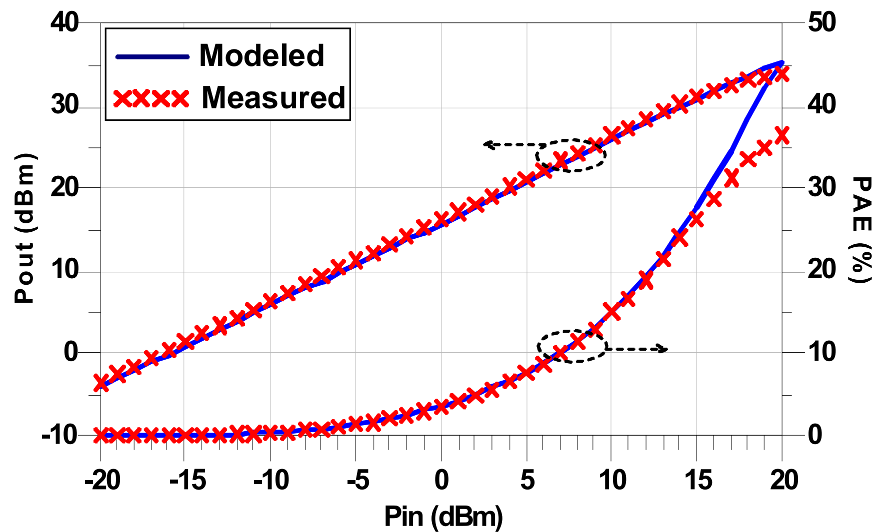

Fig. 82. Measured and modelled Pout and PAE under CW operation.

Nevertheless, one remarkable result that should be pointed out is the correct prediction of the Gain vs Pin pattern, Fig. 83, despite its rather complex behaviour. First, for small-signal levels, the PA presents gain compression, which is then followed by gain expansion, to end up again in gain compression, for very large-signal. This is a direct consequence of the selected bias point, and is consistent with the double minima IMD pattern aimed at the PA design phase [25].

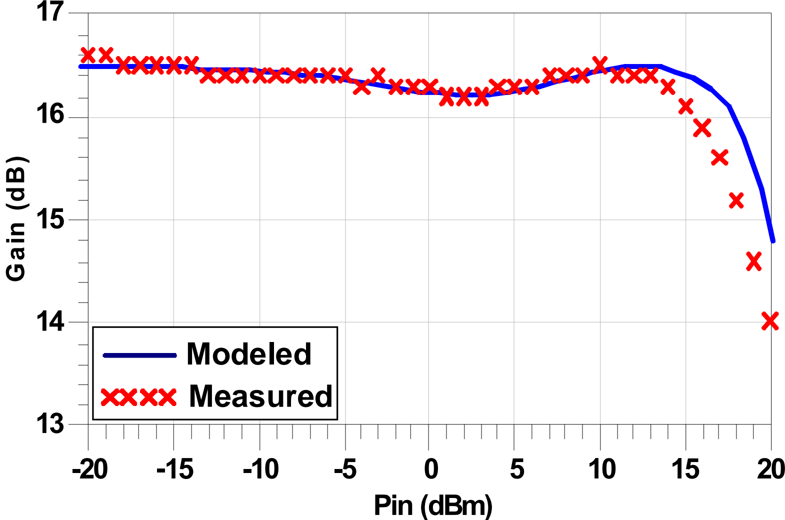

Fig. 83. Measured and modelled Gain vs Pin under CW operation.

Compared to the model predictions, it is clear that the efficiency came somewhat lower than expected, while the Pout and Gain deviations were within the measurement error.

3.2.3. *Large-Signal Two-Tone Nonlinear Distortion Measurements*

Afterwards, PA IMD performance was tested. The excitation was a two-tone centred at 900 MHz, with the tones separated by 100 kHz and the transistor was kept constant at the same bias point used in the previous section (V_{GS1}=-4.20 V and V_{DS}= 20V). The setup used was similar to the one presented in Fig. 66.

Fig. 84 presents the comparison between the two fundamentals (f_1 and f_2) and IMD components ($2f_1$-f_2 and $2f_2$-f_1), measured and modelled, for the above referred bias operation point.

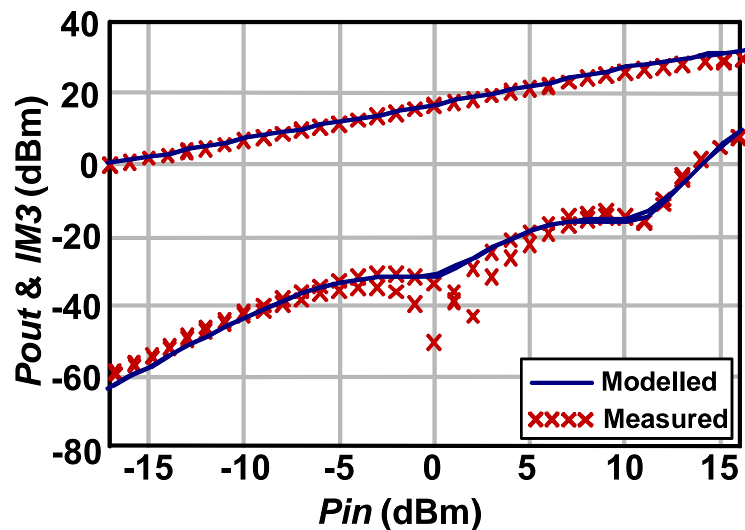

Fig. 84. Measured and simulated PA Pout and IM3 vs Pin for V_{GS1}.

As seen from the data depicted in Fig. 84, there is a good agreement between the predicted and observed results. More important than the capacity of accurately predicting the observations of a particular bias point, is the model's capability to reproduce the dramatic variations of IMD versus Pin pattern when there is a change of bias. Indeed, Fig. 85 and Fig. 86, show measurements and simulations taken for two more bias points still under class AB operation (V_{GS2}=-4.15 V and V_{GS3}=-4.10 V).

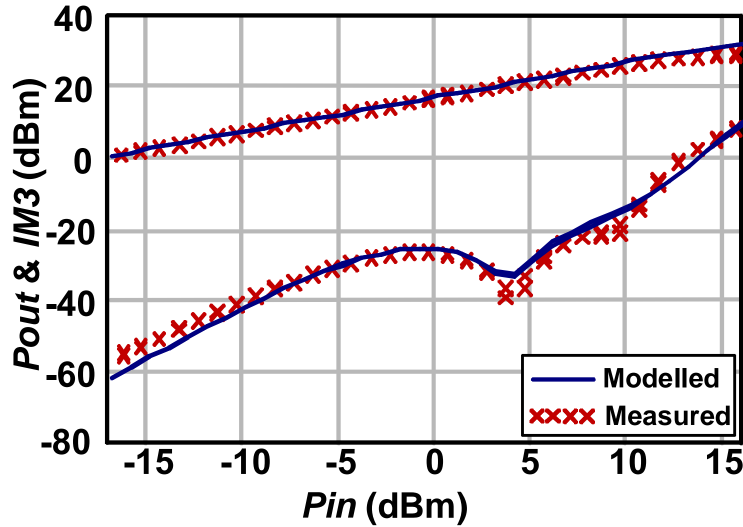

Fig. 85. Measured and simulated PA Pout and IM3 vs Pin for V_{GS2}.

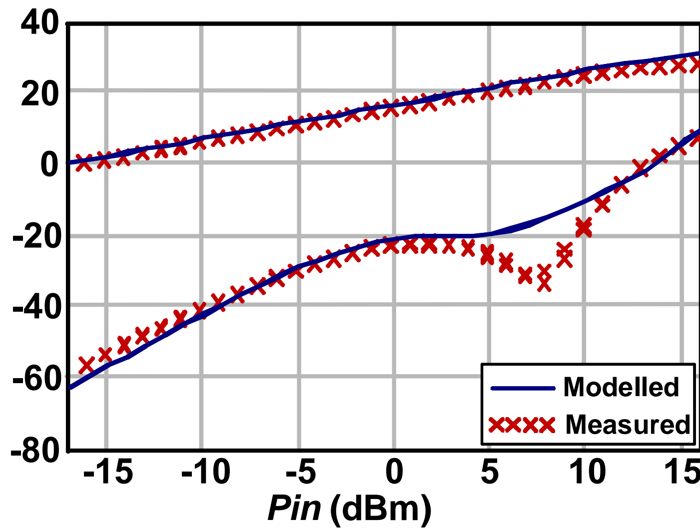

Fig. 86. Measured and simulated PA Pout and IM3 vs Pin for V_{GS3}.

Note the possibility of changing the double minima position to achieve broader or narrower Pin zones of high signal to IMD ratio. That is important for real signal operation since, nowadays, communication systems use disparate modulation schemes and wideband signals which present a statistical amplitude distribution that is quite different from the one of a simple CW or two-tone excitation [58].

3.3. Conclusions

This chapter was dedicated to the model validation. This task was divided into two different stages. In the first one, at the transistor level, the model gave a very accurate prediction of the device's output power, AM/AM and AM/PM conversions and intermodulation distortion characteristics. Indeed, the remarkable good agreement obtained between measured and simulated Pout and two-tone IM3, in a practical class AB 2W power amplifier circuit (second part), validated the developed nonlinear GaN HEMT model and clearly showed its value for nonlinear microwave computer aided design.

4. GaN Model Robustness

Sceptics usually argue that equivalent circuit models, extracted from one device, are always linked to it and are unable to predict, with the desired accuracy, the observed behaviour of other devices, even from the same family. In order to assess those claims and, since this thesis is devoted to GaN modelling, in terms of distortion prediction, a preliminary robustness test was conducted to evaluate the model capabilities in representing, not a single transistor, but a certain set of similar devices, from the same manufacturer.

Moreover, since we are using GaN devices, this test is even more important. Those transistors have already demonstrated to be capable of producing very high Pout devices, with very good characteristics, but these results are not consistently obtained and the RF behaviour varies from device-to-device and from run-to-run, [23]. This is especially true in large-signal operation, where the devices suffer from a series of physical phenomena limiting their performance, already discussed in Chapter 1. Fortunately, the device fabrication processes have been improving very fast in the latest years [59-62] so that a lot of ground has already been conquered.

4.1. GaN Device Characteristics

The second set of devices used were more recent and already commercial, 2mm GaN HEMTs on Si substrate (eleven samples), encapsulated in a standard high power microwave package, different from the one used in the first set described in Chapter 2. Fig. 87 shows the packaged device and Fig. 88, a magnified version of its interior.

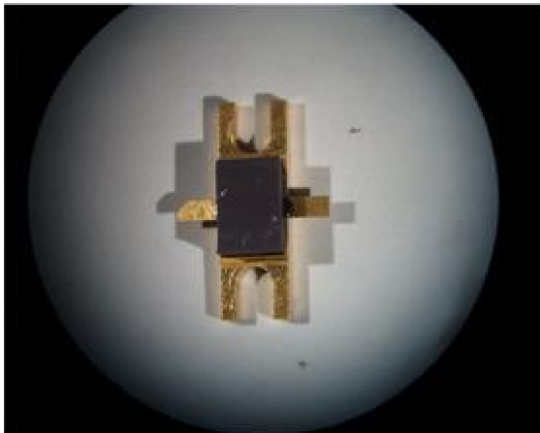

Fig. 87. 2mm packaged GaN HEMT.

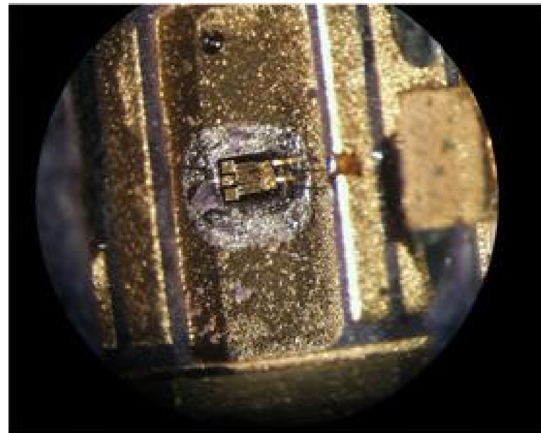

Fig. 88. Magnified version of the packaged device showing the chip inside.

Fig. 89 shows measured I_{DS} versus V_{DS} characteristics, under static conditions, for seven different V_{GS} biases (from -3V to 0V).

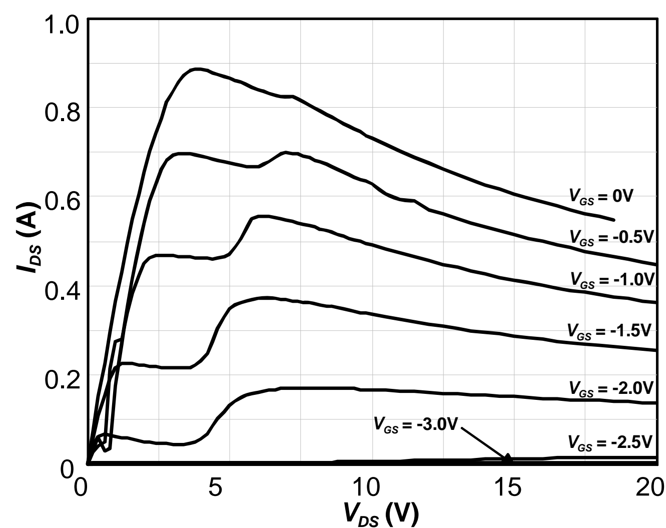

Fig. 89. I_{DS} vs V_{DS} curves measured under static conditions, for seven different V_{GS} biases .

As it is possible to see in Fig. 89, the I_{DS} *vs* V_{DS} curves present some quick increases of the drain current, in the saturation region, for a given value of drain voltage (V_{kink}), in our case, V_{kink}=5V. This phenomenon, usually known as kink effects, already seen for GaN devices is, according to the literature, possibly due to impact ionization or even trapping effects, [63]. Since the device operation area, defined by the PA load line, will fall outside the affected region (see Fig. 90 for a typical Class AB PA design), no special attention was directed to model those effects.

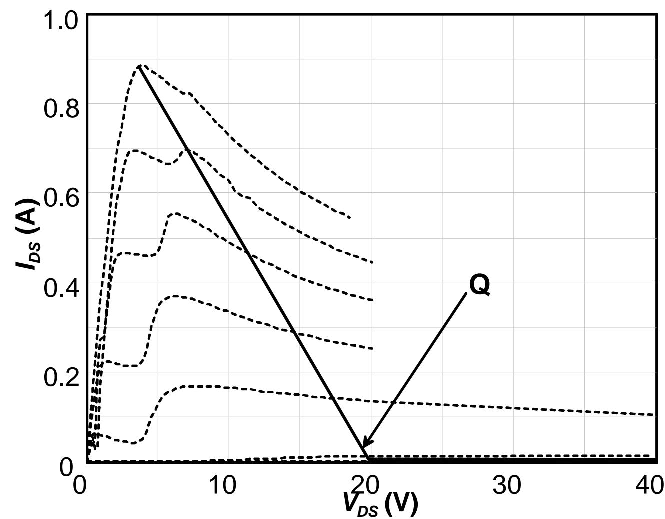

Fig. 90. (--) Measured I_{DS} vs V_{DS} curves under static conditions, for seven different V_{GS} biases and (-) typical class-AB PA load line.

4.2. Comparison between different devices

The objective of this chapter is to study the model robustness in predicting the behaviour of a set of different GaN devices, all coming from the same manufacturer. Due to the technology immaturity, a preliminary device performance variation test was conducted in all available transistors. This was done by the comparison between the fundamental output power and IMD measurement results, obtained from two-tone tests.

Using the measurement setup already presented in Fig. 66, all the available transistors were excited with a two-tone signal, centred at 900 MHz, with a frequency separation of 100 kHz. The drain bias was kept constant at 20V and the gate bias was swept, from deep class C (V_{GS}=-3V) up to Class A (V_{GS}=0V).

Fig. 91 illustrates the three-dimensional Fundamental output power and IMD variation with gate voltage and input power, obtained for one of the devices tested, randomly selected from the set.

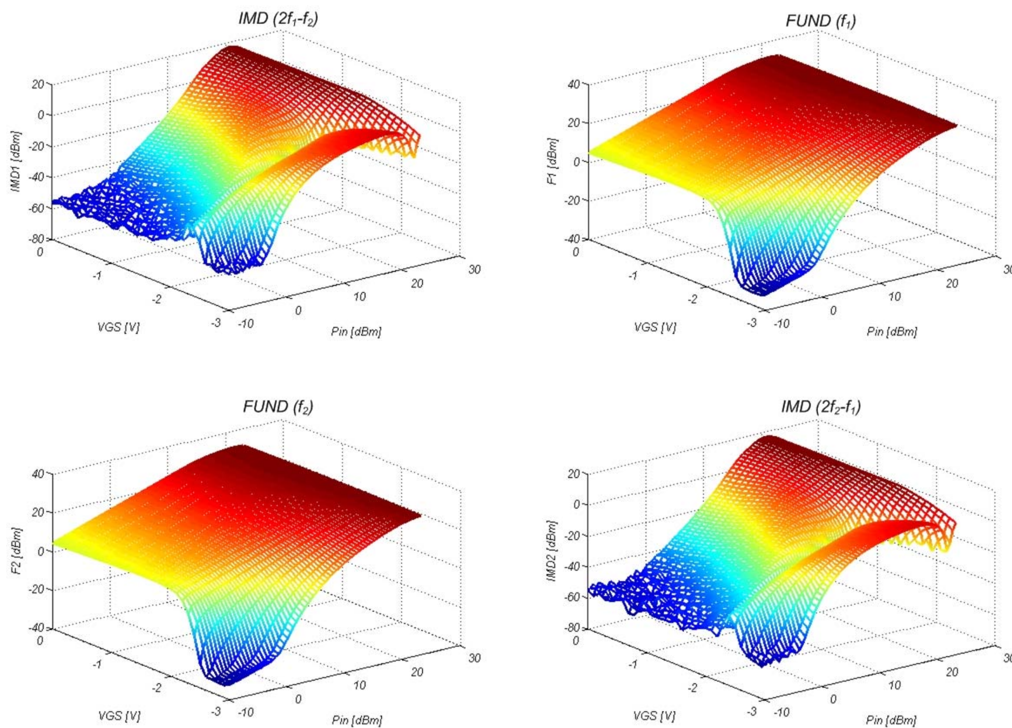

Fig. 91. Three-dimensional variation of the Fundamental (f_1 and f_2) and IMD ($2f_1$-f_2 and $2f_2$-f_1) components with gate bias and input power, measured for one of the devices, randomly selected.

The transistors were found very similar. The only detected difference was a 0.2V variation in the threshold voltage, which is also very common in transistors manufactured in more mature technologies.

This variation was easily identified by comparing the obtained IMD characteristics since, as it was already explained in Chapter 1, when the active device is biased near class-AB, it will present a double sweet-spot IMD pattern.

In order to illustrate this variation, a root mean squared error, ε, was determined for each one of the measurements (two fundamental output power and two IMD components) by the following expression:

$$\varepsilon = \frac{1}{N}\sum_{n=1}^{N}\sqrt{\frac{\left|P_n - \overline{P}\right|^2}{\left|\overline{P}\right|^2}} \tag{23}$$

N is the number of measured transistors;

P_n is the fundamental or IMD component, in watt;

$\overline{P}$ is the eleven devices mean response, calculated by the following expression:

$$\overline{P} = \frac{1}{N}\sum_{n=1}^{N} P_n \tag{24}$$

Fig. 92 presents the root mean squared error results, obtained for the two fundamental output power and IMD components, as a function of bias and input power. If we take a closer look to both 3D IMD plots, it is very easy to see that the maximum error occurs near V_{GS}=-2.1V, which, unsurprisingly, corresponds to the device's threshold voltage.

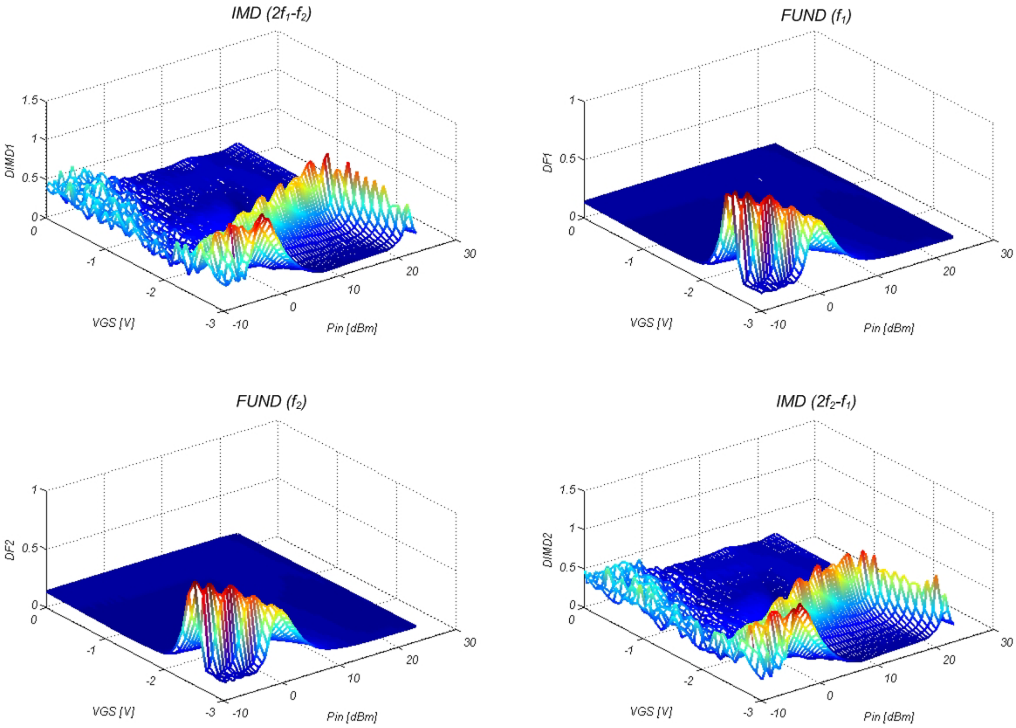

Fig. 92. Root mean squared error between each set of measurements and the corresponding mean response.

4.3. Nonlinear Model Extraction and Validation

Using the methodology explained in Chapter 2, we proceeded with the extraction of the nonlinear equivalent circuit model, for one of the new devices, randomly selected from the set. The obtained model parameters are listed from Table 7 to Table 10.

Table 7. Extrinsic element values for the second set of transistors.

Elements	Value
R_g	2.20 Ω
R_d	1.0 Ω
R_s	0.1 Ω
L_g	1.0 nH
L_d	0.5 nH
L_s	0.11 nH
L_{g_B}	0 nH
L_{d_B}	0 nH
C_{pg}	1.4 pF
C_{pd}	1.4 pF
R_{11}	60 Ω
C_{11}	0.9 pF
R_{21}	300 Ω
C_{21}	0.9 pF
R_{31}	20 Ω
C_{31}	0 pF

Table 8. Invariant intrinsic element values for the second set of transistors.

Element	Value
R_i	1 Ω
C_{gd}	0.35 pF
C_{ds}	0.5 pF

Table 9. In-House $i_{DS}(v_{GS}, v_{DS})$ model parameter values for the second set of transistors.

Parameter	Value
β	0.85 A/V^2
V_{T0}	-2.12 V
VST	0.07 V
VK	1 V
Δ	3.2 V
V_L	2.4 V
λ	0.0026 V^{-1}
α	0.40 V^{-1}
$psat$	-0.742
$plin$	1
γ	-0.01

Table 10. In-House $C_{gs}(v_{gs})$ model parameters for the second set of devices.

Parameter	Value
C_{gs0}	0.8 pF
A_{Cgs}	3.75 pF
K_{Cgs}	5 V^{-1}
V_{Cgs}	-2.5 V

Afterwards, the model's IMD performance was evaluated. A two-tone signal, centred at 900 MHz and with a frequency separation of 100 kHz, was applied to the transistor's input. The drain bias was kept constant at 20V and the gate bias was swept, from deep class C (V_{GS}=-3V) up to Class A (V_{GS}=0V), using the same measurement setup already presented in Fig. 66.

Due to the large number of points involved, the measurements were only compared with the model prediction for three cases, for each of the operation classes (C, AB and A).

The comparison between measurements and model predictions, for all nine cases, is presented in Fig. 93 for Class C (V_{GS}=-3.0V, V_{GS}=-2.6V and V_{GS}=-2.2V); Fig. 94 for Class AB (V_{GS}=-2.1V, V_{GS}=-2.0V and V_{GS}=-1.9V) and, finally, in Fig. 95, for Class A (V_{GS}=-1.1V, V_{GS}=-0.5V and V_{GS}=-0.1V).

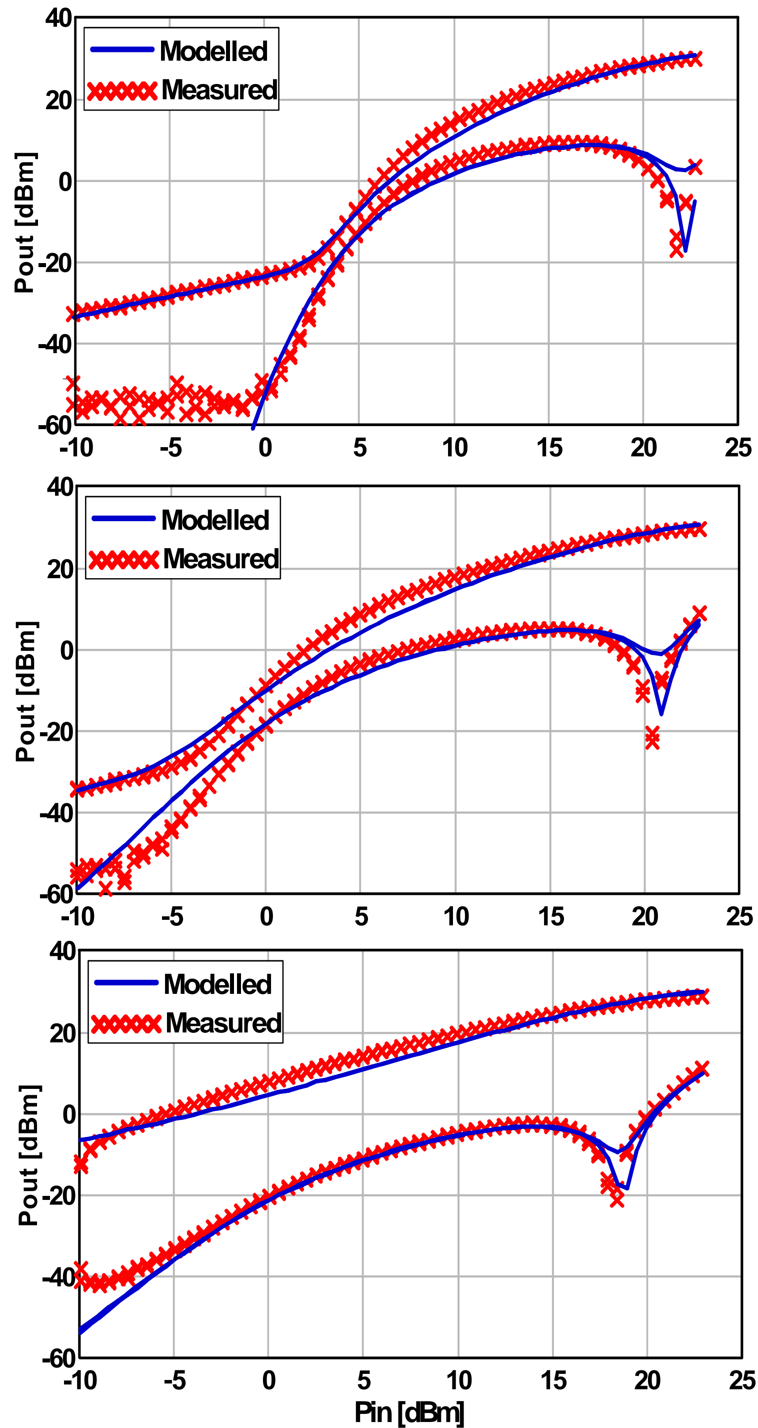

Fig. 93. Measured and simulated PA Pout and IM3 vs Pin, for three different points under Class C operation, (V_{GS}=-3.0V, V_{GS}=-2.6 and V_{GS}=-2.2V).

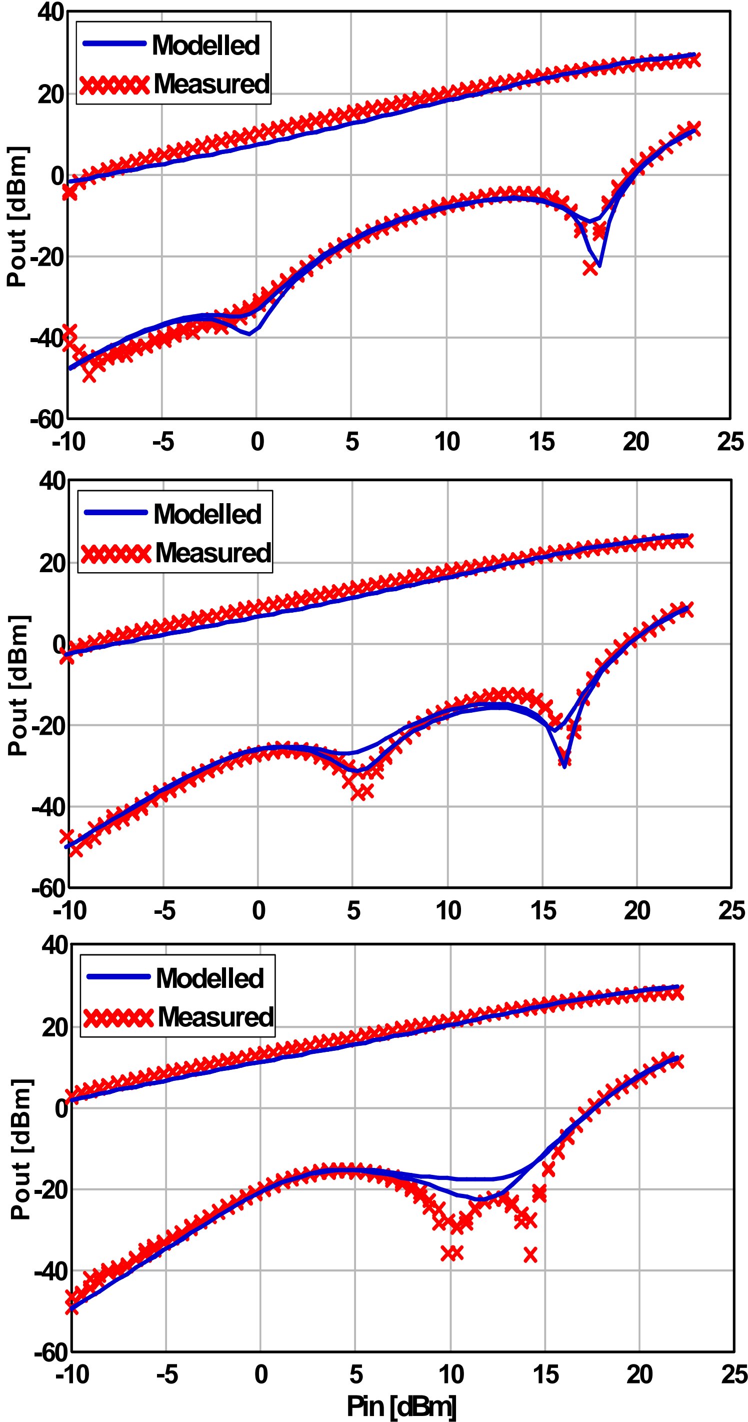

Fig. 94. Measured and simulated PA Pout and IM3 vs Pin, for three different points under Class AB operation, (V_{GS}=-2.1V, V_{GS}=-2.0 and V_{GS}=-1.9V).

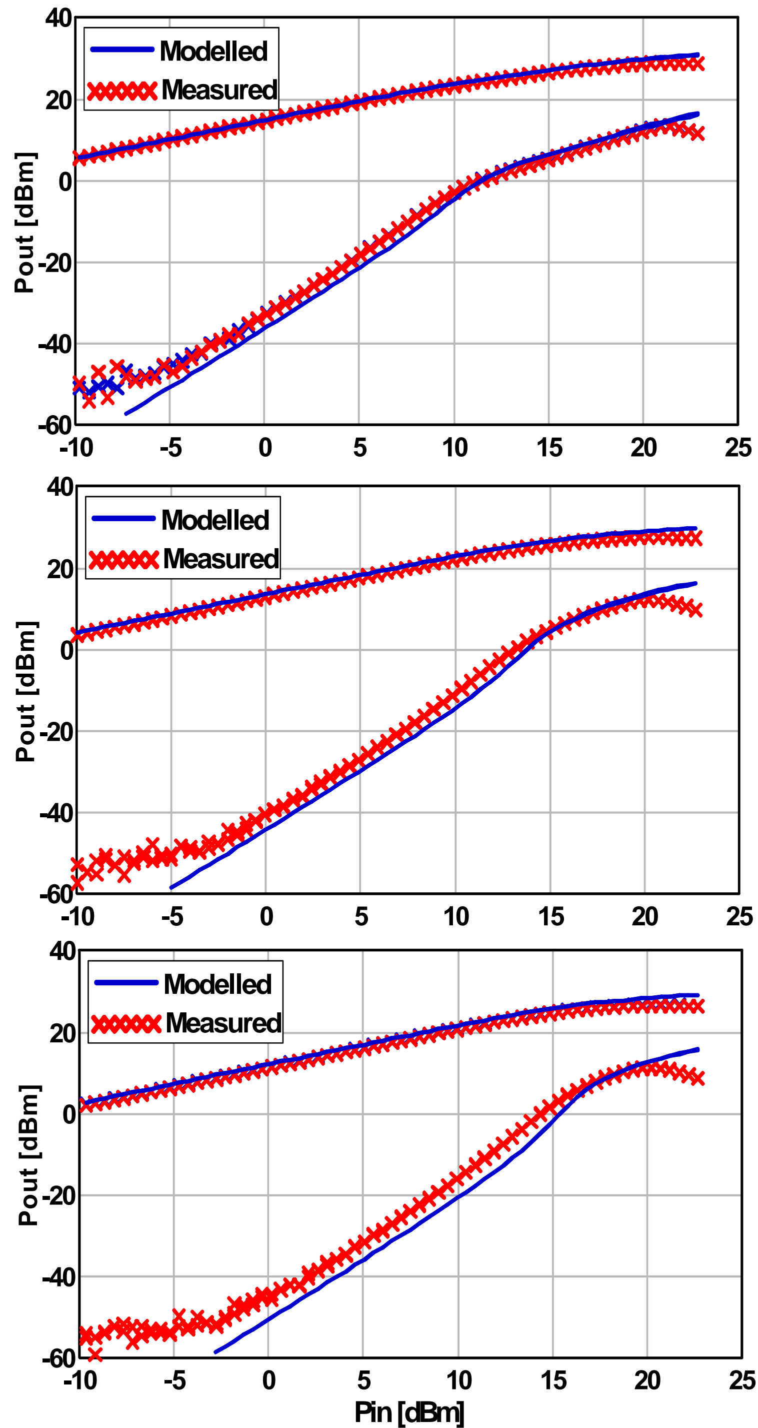

Fig. 95. Measured and simulated PA Pout and IM3 vs Pin, for three different points under Class A operation, (V_{GS}=-1.1V, V_{GS}=-0.5 and V_{GS}=-0.1V).

As it is possible to see, there is a very good agreement between measured results and simulations.

In Class C, the large-signal sweet-spot position is very well predicted. For Class AB operation, not only the presence of the two minima is well represented, but also their position evolution is also captured. For Class A, both the fundamental output power and IMD components are well predicted throughout the complete input drive level.

4.4. GaN Model Performance

In order to evaluate the model performance, when predicting the behaviour of GaN devices, different from the one used to extract it, we compared the two-tone fundamental output power and IMD characteristics, obtained with the nonlinear model, with the ones obtained from the mean response of all devices, previously stored.

Once again, due to the large number of points involved, the comparison between measurements and model predictions was performed, for three cases for each of the operation classes (C, AB and A). Fig. 96 presents the results obtained for Class C (V_{GS}=-2.8V, V_{GS}=-2.6V and V_{GS}=-2.5V); Fig. 97 for Class AB (V_{GS}=-2.3V, V_{GS}=-2.2V and V_{GS}=-2.0V) and, finally, Fig. 98, for Class A (V_{GS}=-1.1V, V_{GS}=-0.4V and V_{GS}=-0.3V).

After the results presented in Section 4.2, stating that there was a threshold voltage variation of 0.2V between all devices tested, we tried different correction factors and the results presented were obtained with that voltage shift.

A first look at those comparisons indicates that there is a fairly good agreement between the fundamental output power and IMD measurements and modelled results. Furthermore, the model could still predict the intermodulation distortion characteristic patterns of the mean device response, which re-enforces all efforts made to use this kind of equivalent circuit models when dealing, not only with a specific transistor, but also with a complete family of devices.

After this, a closer look at the fundamental measurements taken from the device heavily tested with the model extraction and validation, revealed a 1.5 dB decrease in the output power, when compared with all the other devices. This could be an indication of RF stress since the device was tested under strong amplitude signals.

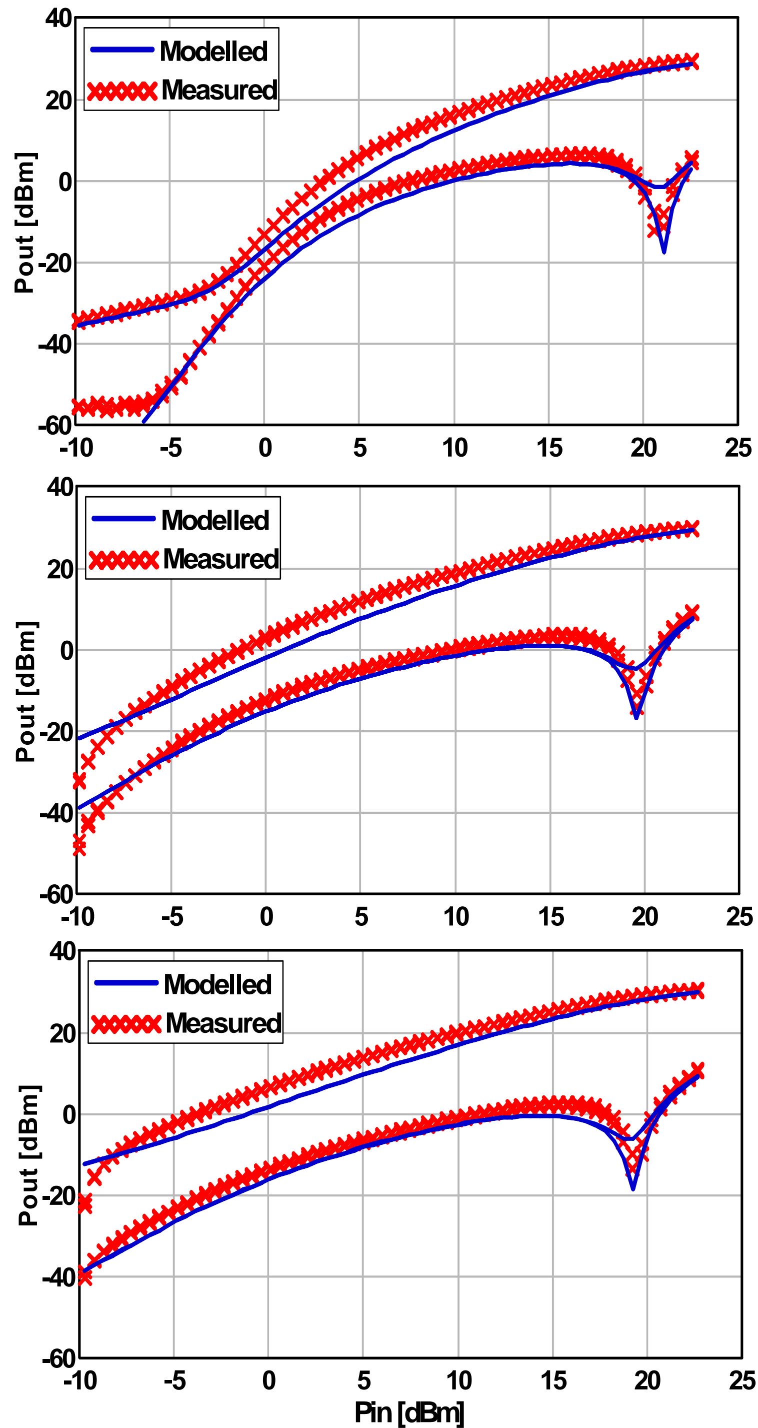

Fig. 96. Pout and IM3 vs Pin, for three different points under Class C operation, obtained with the nonlinear model and with the mean response of all devices, (V_{GS}=-2.8V, V_{GS}=-2.6V and V_{GS}=-2.5V).

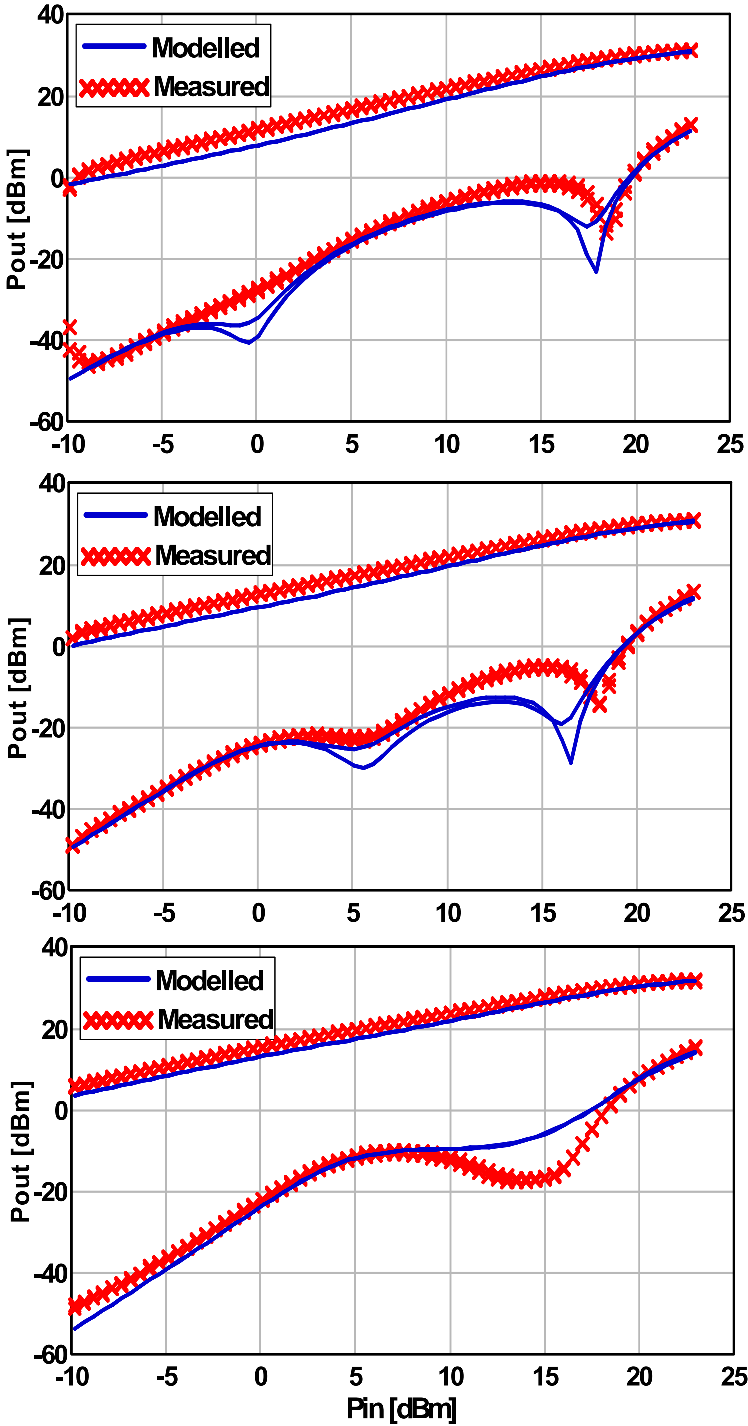

Fig. 97. Pout and IM3 vs Pin, for three different points under Class AB operation, obtained with the nonlinear model and with the mean response of all devices, (V_{GS}=-2.3V, V_{GS}=-2.2V and V_{GS}=-2.0V).

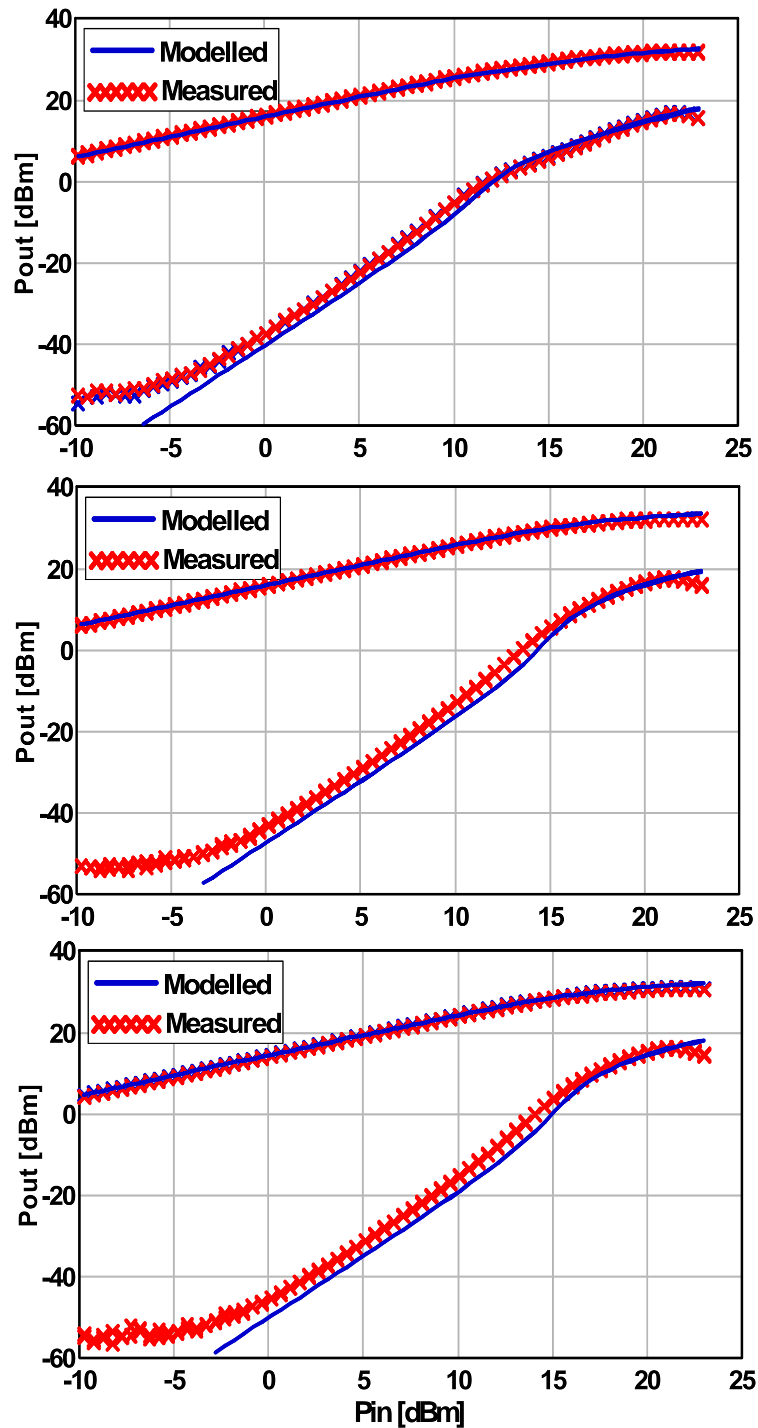

Fig. 98. Pout and IM3 vs Pin, for three different points under Class A operation, obtained with the nonlinear model and with the mean response of all devices, (V_{GS}=-1.1V, V_{GS}=-0.4V and V_{GS}=-0.3V).

4.5. Conclusions

In this chapter, a simple model robustness test was conducted. Eleven transistors were measured under exactly the same conditions and their fundamental output power and IMD characteristics compared. The results obtained showed a 0.2V variation in the threshold voltage.

After that, we extracted the nonlinear equivalent circuit model for one device randomly selected. The model validation tests gave, once again, very good results.

The comparison between the fundamental output power and IMD characteristics predicted by the model and obtained from a mean device of all the available transistors showed that this model is very robust being indeed able to represent not only one transistor, but the whole family of available devices.

5. GaN Model Application: Study of AM/AM and AM/PM Conversions

Due to their significance in PA linearization techniques, the AM/AM and AM/PM conversions are very important characterization measurements. They consist in the transformation, by the nonlinear active device, of the input amplitude variations, AM, into variations of the output amplitude or phase, AM or PM, respectively.

AM/AM conversion is particularly important in systems based on amplitude modulation; while AM/PM has its major impact in non-constant envelope phase modulation formats.

Fig. 99 shows a 64-quadrature amplitude modulation (QAM) constellation diagram where it is possible to see the amplitude and phase conversions' impact in the symbol decoding.

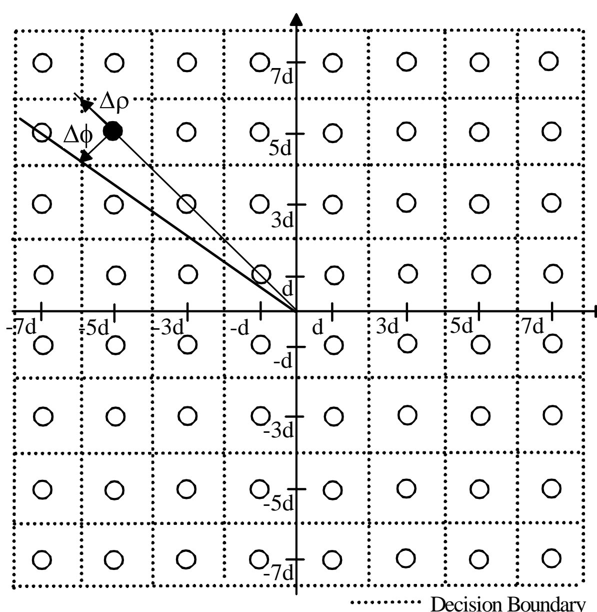

Fig. 99. 64-QAM constellation diagram.

Such performance measurements are usually obtained via a CW test using a vector network analyser, (VNA), and thus, correspond to a static analysis, from the envelope (or long term dynamics) viewpoint. So, they can not provide any information regarding the dynamic effects that can impair the slowly varying modulating signals.

One alternative way to overcome this limitation is to use real excitation signals through the use of a vector signal analyzer, (VSA). Despite some problems interpreting the raw measurements obtained from this piece of equipment [64], there are already several important studies helping to achieve the dynamic amplitude and phase characteristics [65].

This Chapter presents an application for the GaN model, previously formulated and extracted, providing a comprehensive study of the PA's in-band and out-of-band output terminations' impact on the static and dynamic signal distortion impairments: AM/AM and AM/PM conversions.

Section 5.1 describes the load impedance impact on the above referred conversions. This study is done theoretically, using Volterra series analysis and, in practice, with envelope simulations of the nonlinear model, with different load terminations.

Finally, section 5.2 is devoted to analyze the bias networks' impact on the dynamic AM/AM contours in microwave PAs and, using that knowledge, to give an interpretation of the hysteretic paths shape.

5.1. Load Impedance Impact

Fig. 100 presents the PA equivalent circuit model, a simplified version of the GaN HEMT based PA prototype, presented in Chapters 2 and 3.

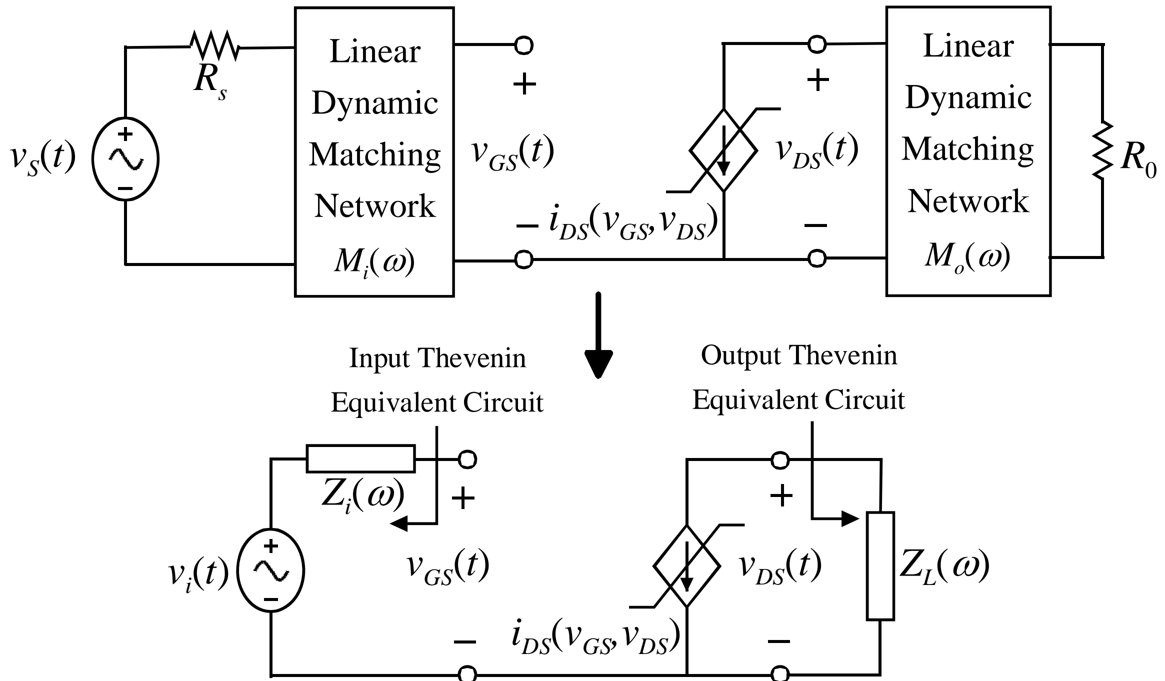

Fig. 100. Simplified FET based PA circuit used for the nonlinear analysis.

As it is possible to see in Fig. 100, $i_{DS}(v_{GS}, v_{DS})$ is a nonlinear function, dependent on two control voltages: v_{GS} and v_{DS}. Using a low order Taylor series expansion we get:

$$i_{DS}(v_{GS}, v_{DS}) = I_{DS} + G_m v_{gs} + G_d v_{ds} + G_{m2} v_{gs}^2 + G_{md} v_{gs} v_{ds} + G_{d2} v_{ds}^2 + G_{m3} v_{gs}^3 + G_{m2d} v_{gs}^2 v_{ds} + G_{md2} v_{gs} v_{ds}^2 + G_{d3} v_{ds}^3 \quad (25)$$

Applying a mildly nonlinear Volterra series analysis to this circuit (where $v_{gs}(t)$ and $v_{ds}(t)$ are the input and output, respectively), we can obtain the first three Volterra frequency domain nonlinear transfer functions (NLTFs): $H_n(\omega_1, ..., \omega_n)$ with n=1…3 [66].

Defining the auxiliary function $F_C(\omega)$ as:

$$F_C(\omega) = \frac{Z_L(\omega)}{1 + G_{ds} \cdot Z_L(\omega)} \tag{26}$$

The generic NLTFs are presented in the following expressions:

$$H_1(\omega_1) = -G_m \cdot F_C(\omega_1) \tag{27}$$

$$H_2(\omega_1, \omega_2) = -F_C(\omega_1 + \omega_2) \cdot \left\{ G_{m2} + \frac{1}{2} G_{md} \cdot \left[H_1(\omega_1) + H_1(\omega_2) \right] + G_{d2} \cdot \left[H_1(\omega_1) \cdot H_1(\omega_2) \right] \right\} \tag{28}$$

$$\begin{aligned} H_3(\omega_1, \omega_2, \omega_3) = -F_C(\omega_1 + \omega_2 + \omega_3) \cdot \Big\{ & G_{m3} + \frac{1}{3} G_{m2d} \cdot \left[H_1(\omega_1) + H_1(\omega_2) + H_1(\omega_3) \right] \\ & + \frac{1}{3} G_{md2} \cdot \left[H_1(\omega_1) \cdot H_1(\omega_2) + H_1(\omega_2) \cdot H_1(\omega_3) + H_1(\omega_1) \cdot H_1(\omega_3) \right] \\ & + G_{d3} \cdot \left[H_1(\omega_1) \cdot H_1(\omega_2) \cdot H_1(\omega_3) \right] + \frac{1}{3} G_{md} \cdot \left[H_2(\omega_1, \omega_2) + H_2(\omega_2, \omega_3) + H_2(\omega_1, \omega_3) \right] \\ & + \frac{2}{3} G_{d2} \cdot \left[H_1(\omega_1) \cdot H_2(\omega_2, \omega_3) + H_1(\omega_2) \cdot H_2(\omega_1, \omega_3) + H_1(\omega_3) \cdot H_2(\omega_1, \omega_2) \right] \Big\} \end{aligned} \tag{29}$$

Although the validity of these transfer functions for large-signal analysis is questionable, they can still be used to qualitatively explain the physical origins of the PA AM/AM and AM/PM distortions.

Considering a two-tone input excitation, with amplitudes $|V_{gs}(\omega_1)|$ and $|V_{gs}(\omega_2)|$, the time domain signal corresponds to:

$$x(t) = \mathrm{Re}\left\{ \left| V_{gs}(\omega_1) \right| \cdot e^{j(\omega_1 t)} + \left| V_{gs}(\omega_2) \right| \cdot e^{j(\omega_2 t)} \right\} \tag{30}$$

In order to express the input excitation as a cosine carrier modulated, in amplitude, by the purely real $2\left|V_{gs}(\omega)\right|\cdot\cos\left(\frac{\Delta\omega}{2}t\right)$ envelope, we need to re-write (30) as:

$$x(t)=\mathrm{Re}\left\{\left[\left|V_{gs}(\omega)\right|\cdot e^{-j\left(\frac{\Delta\omega}{2}t\right)}+\left|V_{gs}(\omega)\right|\cdot e^{j\left(\frac{\Delta\omega}{2}t\right)}\right]\cdot e^{j(\omega_c t)}\right\} \tag{31}$$

where:

$$\omega_c=\frac{\omega_1+\omega_2}{2} \tag{32}$$

and

$$\Delta\omega=\omega_2-\omega_1 \tag{33}$$

The output time domain waveform will be given by:

$$\begin{aligned} y(t)=\mathrm{Re}\Big\{&\left|V_{ds}(2\omega_1-\omega_2)\right|\cdot e^{j((2\omega_1-\omega_2)t+\theta_{o3})}+\left|V_{ds}(\omega_1)\right|\cdot e^{j(\omega_1 t+\theta_{o1})}\\ &+\left|V_{ds}(\omega_2)\right|\cdot e^{j(\omega_2 t+\theta_{o2})}+\left|V_{ds}(2\omega_2-\omega_1)\right|\cdot e^{j((2\omega_2-\omega_1)t+\theta_{o4})}\Big\}\end{aligned} \tag{34}$$

where θ_{o1}, θ_{o2} are the fundamental and θ_{o3}, θ_{o4} the IMD phase variations at the output, and:

$$V_{ds}(2\omega_1-\omega_2)=3H_3(\omega_1,\omega_1,-\omega_2)\cdot V_{gs}(\omega_1)\cdot V_{gs}(\omega_1)\cdot V_{gs}(\omega_2)^* \tag{35}$$

$$V_{ds}(\omega_1)=\left[H_1(\omega_1)+3H_3(\omega_1,\omega_1,-\omega_1)\cdot\left|V_{gs}(\omega_1)\right|^2+6H_3(\omega_1,\omega_2,-\omega_2)\cdot\left|V_{gs}(\omega_2)\right|^2\right]\cdot V_{gs}(\omega_1) \tag{36}$$

$$V_{ds}(\omega_2)=\left[H_1(\omega_2)+3H_3(\omega_2,\omega_2,-\omega_2)\cdot\left|V_{gs}(\omega_2)\right|^2+6H_3(\omega_2,\omega_1,-\omega_1)\cdot\left|V_{gs}(\omega_1)\right|^2\right]\cdot V_{gs}(\omega_2) \tag{37}$$

$$V_{ds}(2\omega_2-\omega_1)=3H_3(\omega_2,\omega_2,-\omega_1)\cdot V_{gs}(\omega_2)\cdot V_{gs}(\omega_2)\cdot V_{gs}(\omega_1)^* \tag{38}$$

Therefore, using (32)-(33), we can re-write (34) as:

$$y(t)=\mathrm{Re}\left\{\left[\left|V_{ds}(2\omega_1-\omega_2)\right|\cdot e^{-j\left(\frac{3\Delta\omega}{2}t+\theta_{o3}(\omega,\Delta\omega)\right)}+\left|V_{ds}(\omega_1)\right|\cdot e^{-j\left(\frac{\Delta\omega}{2}t+\theta_{o1}(\omega,\Delta\omega)\right)}\right.\right.$$
$$\left.\left.+\left|V_{ds}(\omega_2)\right|\cdot e^{j\left(\frac{\Delta\omega}{2}t+\theta_{o2}(\omega,\Delta\omega)\right)}+\left|V_{ds}(2\omega_2-\omega_2)\right|\cdot e^{j\left(\frac{3\Delta\omega}{2}t+\theta_{o4}(\omega,\Delta\omega)\right)}\right]\cdot e^{j(\omega_c t)}\right\} \tag{39}$$

Contrary to the usual way of identifying AM/AM and AM/PM from a time variation of the input and output envelopes, now we have to look for these in (34), via their Fourier representation. Amplitude modulation can be described by a real envelope, while phase modulation must involve a complex envelope. So, the presence of the envelope harmonic components at the power amplifier output (the IMD side-bands) describes the envelope amplitude distortion and is thus AM/AM. On the contrary, AM/PM, or output phase modulation, requires an envelope with a non null imaginary part, or a base-band modulation whose spectrum does not obey the complex conjugate symmetry of purely real signals. So, AM/PM must be identified from the asymmetric amplitudes or phases of the fundamental and IMD components.

As seen from (32)-(39) and (29), all $\left|V_{ds}(2\omega_1-\omega_2)\right|$, $\left|V_{ds}(\omega_1)\right|$, $\left|V_{ds}(\omega_2)\right|$, $\left|V_{ds}(2\omega_2-\omega_1)\right|$ and, θ_{o3}, θ_{o1}, θ_{o2}, θ_{o4} depend on both ω_c and $\frac{\Delta\omega}{2}$, which means that, in general, we should expect AM/AM and AM/PM variation with the short and long-term dynamics on the amplifier via ω_c and $\frac{\Delta\omega}{2}$, respectively.

It is this long-term dynamics, shown in (39) by the dependence on $\frac{\Delta\omega}{2}$, that explains the hysteretic AM/AM and AM/PM characteristics observed in the studied PA examples.

5.1.1. Practical Example

Since the quasi-static approximation implies that i_{DS} is a memoryless nonlinearity, it can only present AM/AM conversion. However, the different phase contributions, introduced by the device parasitic reactances and dynamic load impedance $Z_L(\omega)$, through the dependence of i_{DS} on v_{DS}, will finally establish the overall PA AM/AM and AM/PM conversions.

The impact of the load terminations on the above referred conversions was studied using a non-ideal bias-T, Fig. 101, at the active device's output, followed by one of four alternative loads.

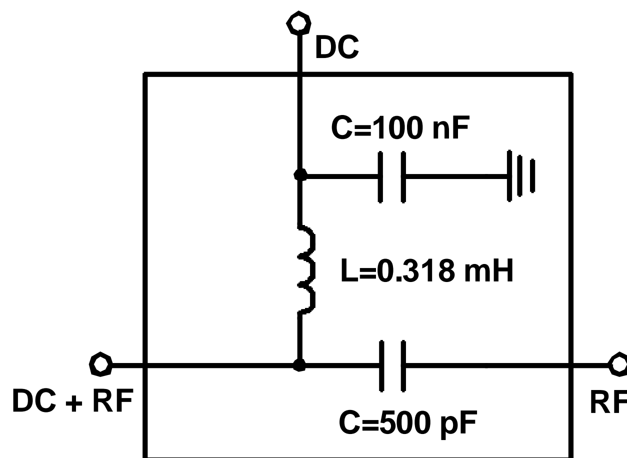

Fig. 101. Non-ideal bias-T.

Several envelope simulations [67, 68] were performed using time-varying envelope stimulus (two-tone signals) with different separation frequencies, carefully chosen knowing the PA's output impedance at the base-band components, $\frac{\Delta\omega}{2}$ (a short circuit, $\Delta F_1/2$ =50 Hz, or two different reactive terminations, $\Delta F_2/2$ =5 kHz and $\Delta F_3/2$ =25 kHz, Fig. 102).

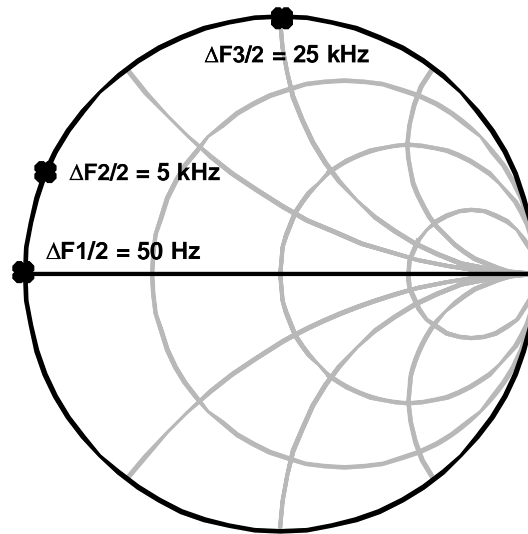

Fig. 102. Base-band impedances at three different two-tone separation frequencies ($\Delta F_1/2$, $\Delta F_2/2$ and $\Delta F_3/2$).

The tests made with tone separation ΔF_1 correspond to a static analysis since the bias-T terminated with the load presents a short circuit to the base-band components. So, in this case, there will be no long-term memory effects visible on the AM/AM, or even, on the AM/PM conversion plot.

For the other separation frequencies (ΔF_2 and ΔF_3) $\frac{\Delta\omega}{2}$ long-term dynamics will explain the hysteretic AM/AM and AM/PM conversions. If that is the case, the power amplifier will not respond instantaneously to its envelope input, and the output amplitude and phase will no longer be single valued functions of the instantaneous excitation amplitude. They will also depend on the amplifier's state, or input history. This issue will be studied in more detail in the next section.

The first load, our reference case, will be purely resistive, Load L_1. Fig. 103 shows the load and its impedance, at the frequencies of interest.

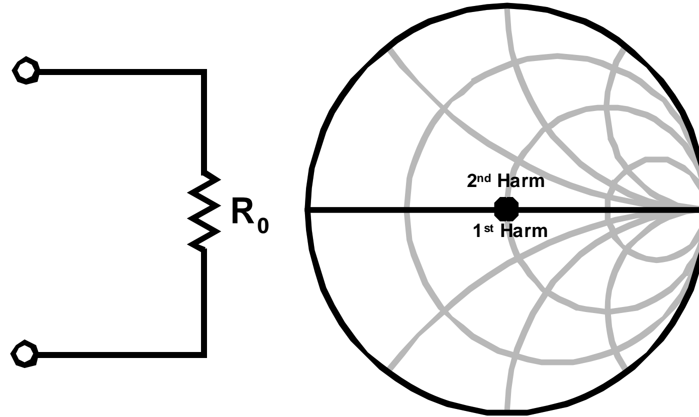

Fig. 103. Load L_1 and its impedances, at the frequencies of interest.

Using the band-pass characteristics of our nonlinear model, we can define:

$$\omega_1 \approx \omega_2 \Rightarrow H_1(\omega_1) \approx H_1(\omega_2) \approx H_1(\omega) \text{ and } H_1(2\omega_1) \approx H_1(2\omega_2) \approx H_1(\omega_1 + \omega_2) \approx H_1(2\omega) \quad (40)$$

Since Load L_1 is purely resistive, from (27)-(29) and (40) we can see that $H_1(\omega_1) = H_1(\omega_2)$, $H_3(\omega_1, \omega_1, -\omega_1) = H_3(\omega_2, \omega_2, -\omega_2)$ are all real values and that $H_3(\omega_1, \omega_2, -\omega_2) = H_3(\omega_2, \omega_1, -\omega_1)^*$ and $H_3(\omega_1, \omega_1, -\omega_2) = H_3(\omega_2, \omega_2, -\omega_1)^*$.

From the previous expressions and from (35)-(38), it is possible to see that the envelope harmonic components, at the power amplifier's output, will be non null. So, there will be AM/AM. Furthermore, as it was theoretically explained, since $V_{ds}(\omega_1) = V_{ds}(\omega_2)^*$ and $V_{ds}(2\omega_1 - \omega_2) = V_{ds}(2\omega_2 - \omega_1)^*$, no AM/PM conversion will occur. Several envelope simulations of the active device model, terminated with Load L_1, for the three different separation frequencies (ΔF_1, ΔF_2 and ΔF_3), were conducted. The AM/AM and AM/PM conversion plots obtained are shown in Fig. 104, where the proposed theoretical explanations are fully validated.

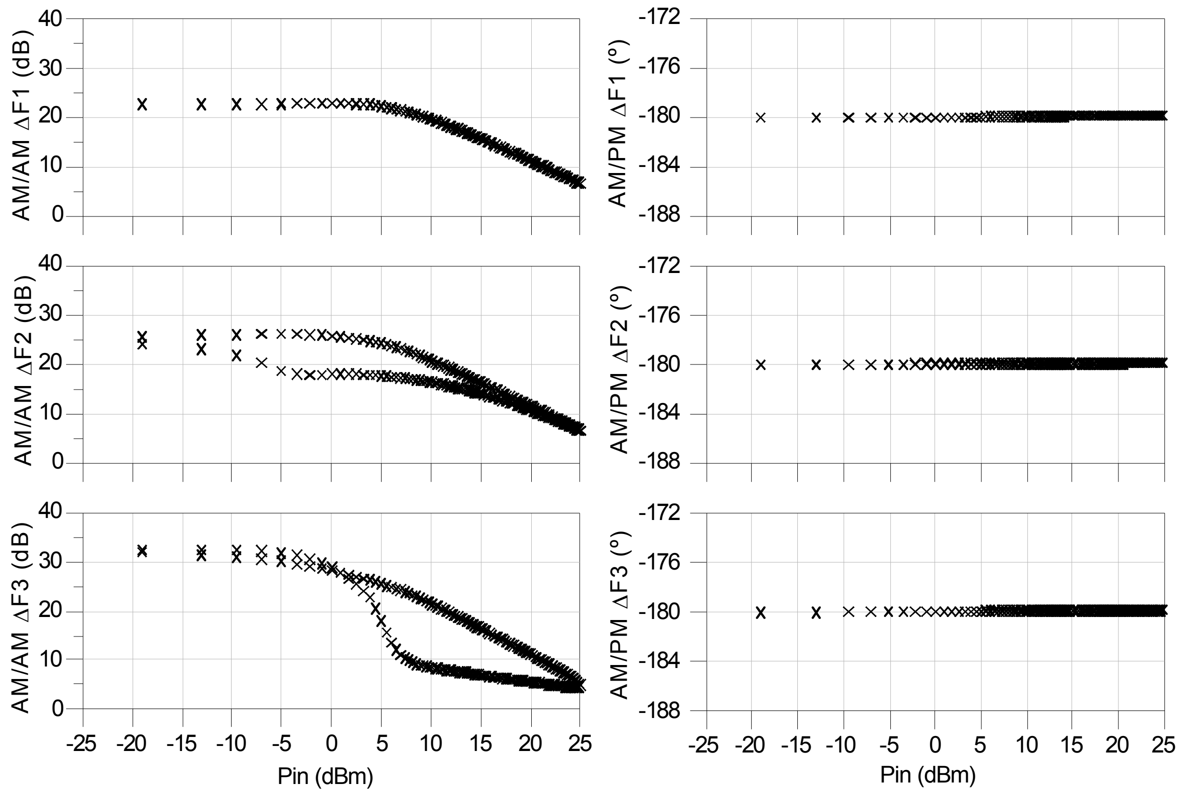

Fig. 104. AM/AM and AM/PM conversions when the active device model is terminated with a non-ideal bias-T and with Load L_1, for three input tone separations (ΔF_1, ΔF_2 and ΔF_3).

The next step was to terminate the active device model with Load L_2 (resistor in parallel with a capacitor and stub tuned to short circuit $Z_L(2\omega)$). Fig. 105 shows the load and its impedance, at the frequencies of interest.

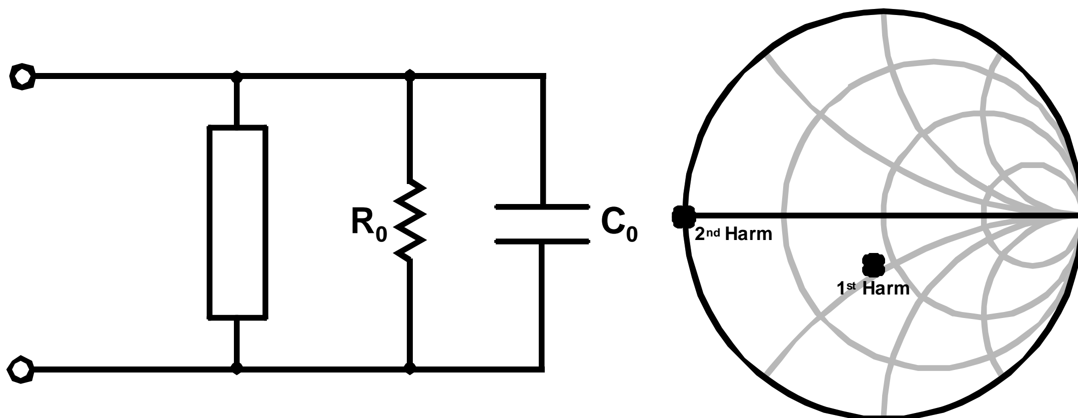

Fig. 105. Load L_2 and its impedances, at the frequencies of interest.

Observing Fig. 105, and from (27)-(29) and (40), it is possible to see that, contrary to the previous case, in spite of $H_1(\omega_1) = H_1(\omega_2)$ and $H_3(\omega_1, \omega_1, -\omega_1) = H_3(\omega_2, \omega_2, -\omega_2)$, these are no longer real quantities and $H_3(\omega_1, \omega_2, -\omega_2) \neq H_3(\omega_2, \omega_1, -\omega_1)^*$.

Once again, the envelope harmonic components, at the power amplifier's output, will be non null. So, AM/AM will still occur. Besides that, as it was theoretically explained, since $V_{ds}(\omega_1) \neq V_{ds}(\omega_2)^*$, there will also be AM/PM conversion.

Fig. 106 shows the AM/AM and AM/PM conversions, obtained from several envelope simulations of the active device model, terminated with Load L_2, for the three different separation frequencies (ΔF_1, ΔF_2 and ΔF_3), where the proposed theoretical explanations are fully validated.

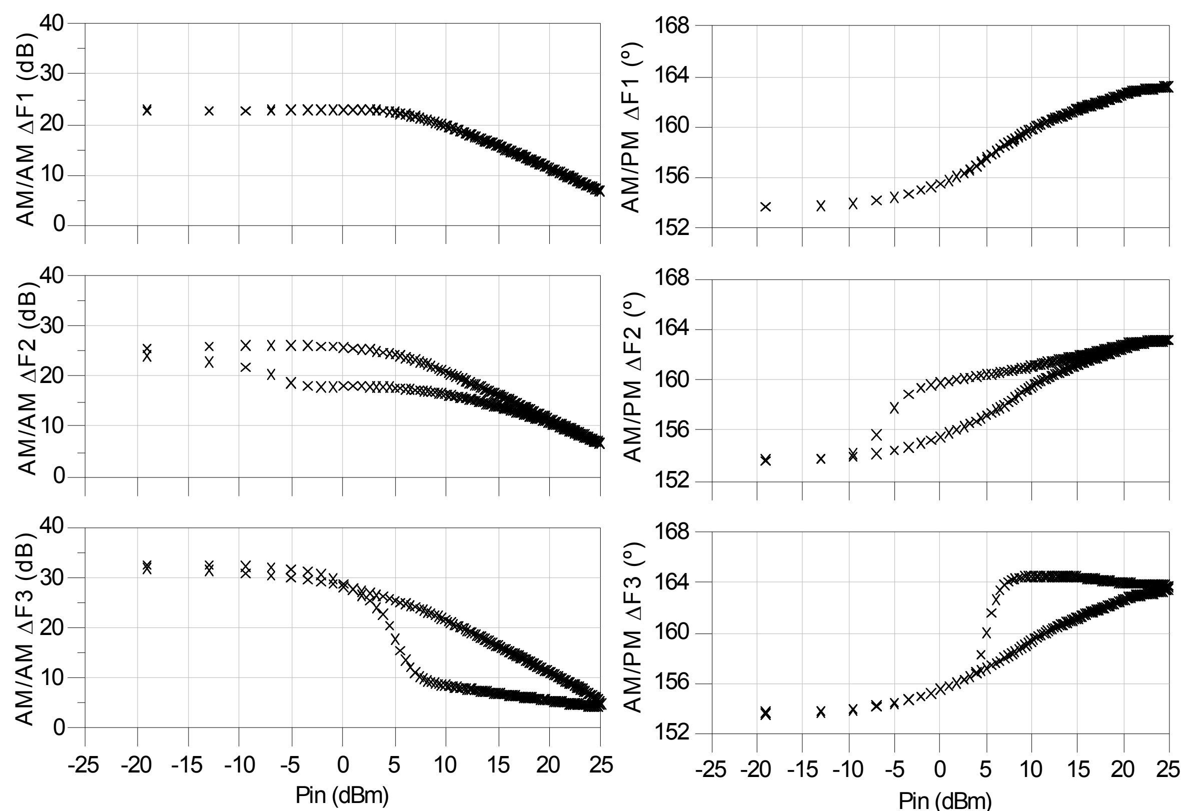

Fig. 106. AM/AM and AM/PM conversions when the active device model is terminated with a non-ideal bias-T and with Load L_2, for three input tone separations (ΔF_1, ΔF_2 and ΔF_3).

After that, in order to evaluate the $Z_L(2\omega)$ contribution, a parallel inductance was used to reset the impedance at the fundamental to 50Ω, but leaving a reactive second harmonic termination (Load L_3). Fig. 107 shows the load and its impedance, at the frequencies of interest.

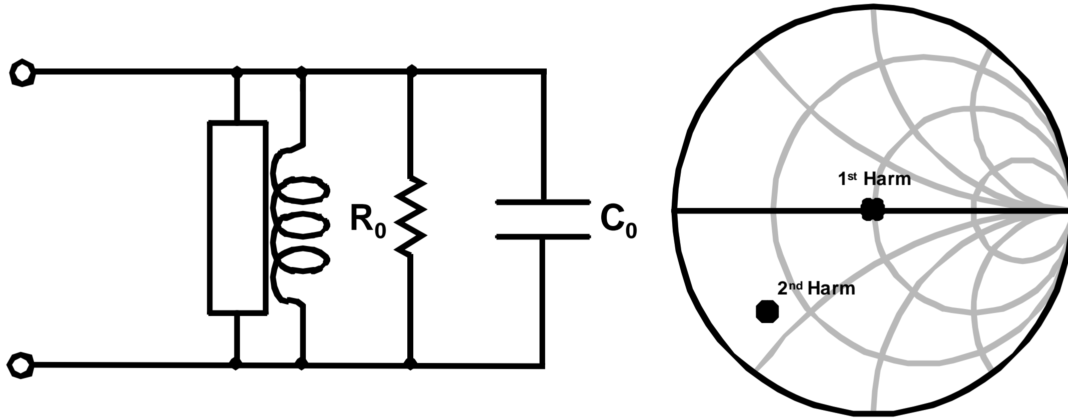

Fig. 107. Load L_3 and its impedances, at the frequencies of interest.

Once again, from (27)-(29) and (40) it is possible to see that, $H_1(\omega_1)=H_1(\omega_2)$ are real values. On the contrary, $H_3(\omega_1,\omega_1,-\omega_1)=H_3(\omega_2,\omega_2,-\omega_2)$ are not real quantities. Besides that, the dependence on 2ω implies that $H_3(\omega_1,\omega_2,-\omega_2)\neq H_3(\omega_2,\omega_1,-\omega_1)^*$.

For the reasons previously explained, this PA circuit will manifest AM/AM and, since $V_{ds}(\omega_1)\neq V_{ds}(\omega_2)^*$, there will also be AM/PM conversion.

Fig. 108 shows the AM/AM and AM/PM conversions obtained, from several envelope simulations of the active device model, terminated with Load L_3, for the three different separation frequencies (ΔF_1, ΔF_2 and ΔF_3).

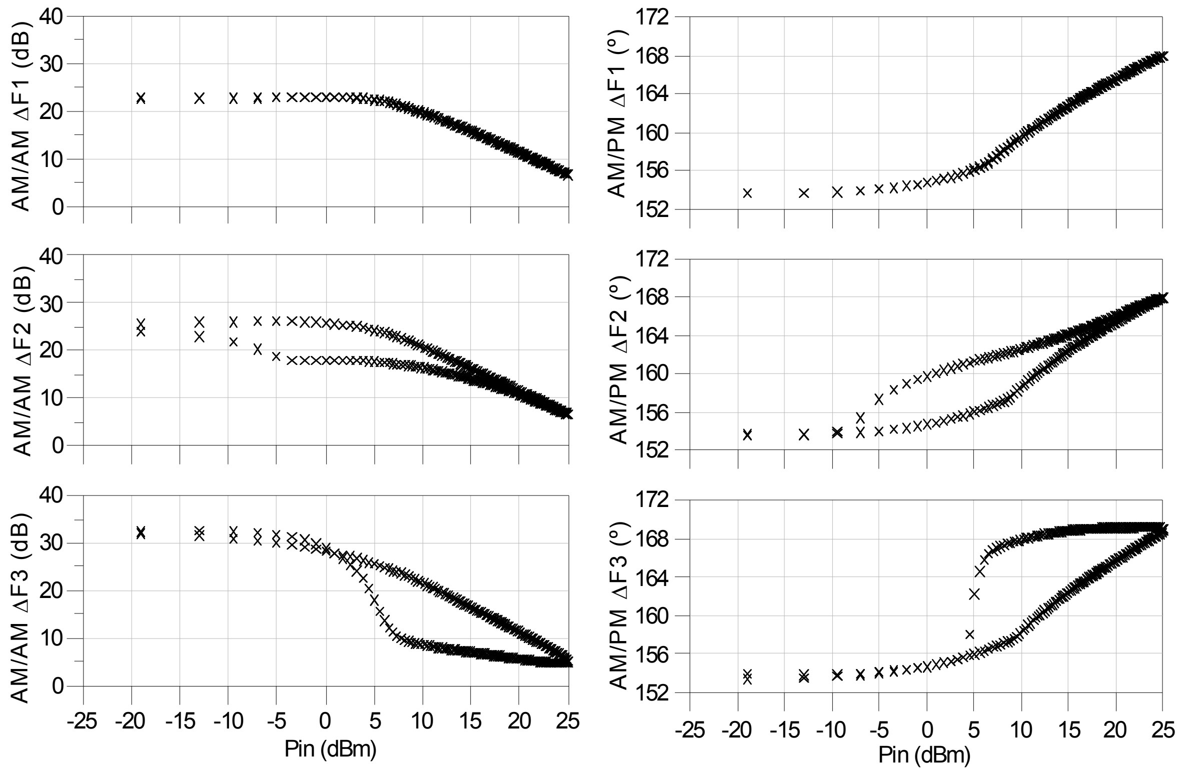

Fig. 108. AM/AM and AM/PM conversions when the active device model is terminated with a non-ideal bias-T and with Load L_3, for three input tone separations (ΔF_1, ΔF_2 and ΔF_3).

Finally, we loaded the active device with Load L_4. This is only a resistor in parallel with a capacitor, which provides a reactive termination to both the fundamental and the second harmonic. Fig. 109 shows the load and its impedance, at the frequencies of interest.

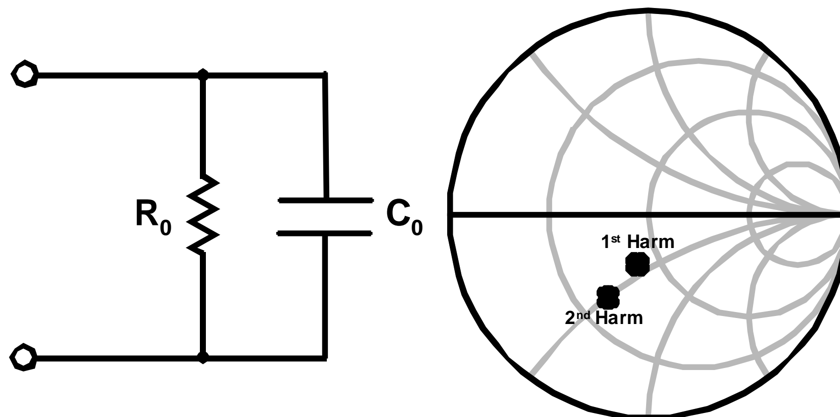

Fig. 109. Load L_4 and its impedances, at the frequencies of interest.

Fig. 110 shows the AM/AM and AM/PM conversions, obtained from several envelope simulations of the active device model terminated with Load L_4, for the three different separation frequencies (ΔF_1, ΔF_2 and ΔF_3). As expected from the previous analysis, since this case is the aggregate of the last two, we will once again have AM/AM and AM/PM conversions.

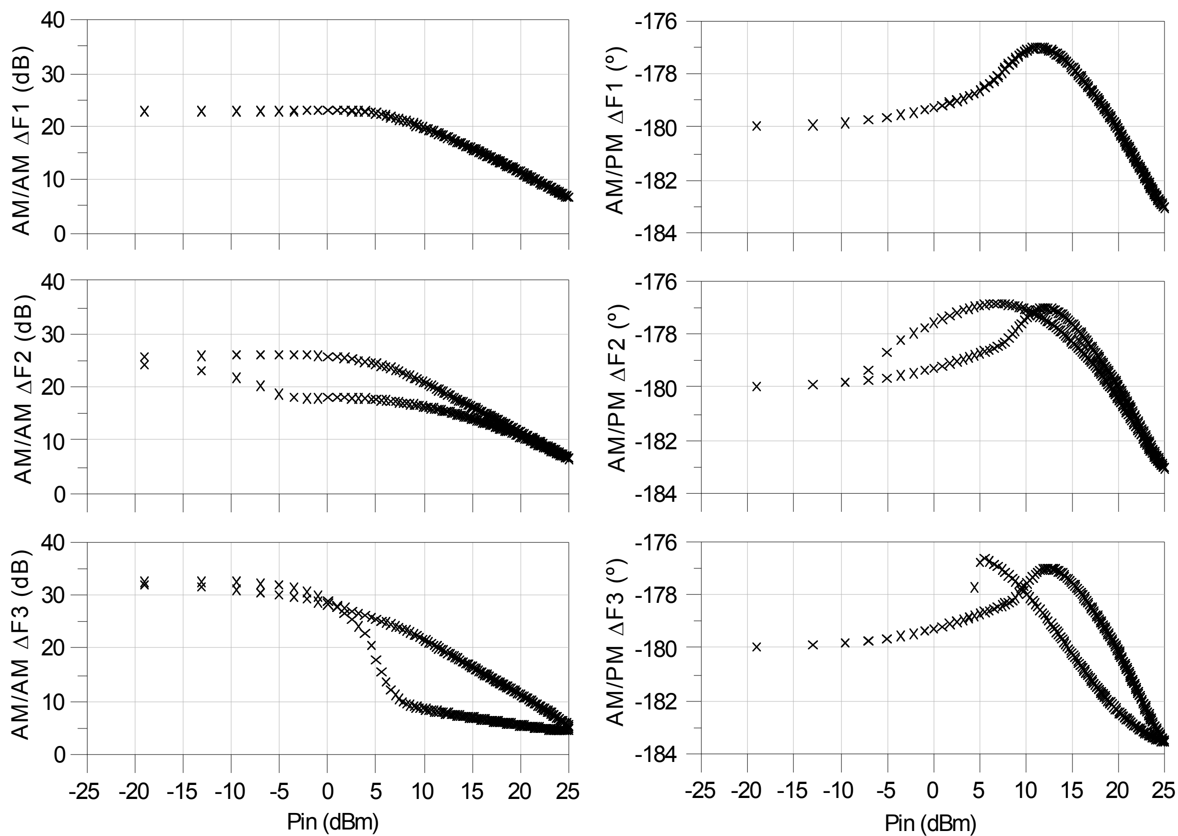

Fig. 110. AM/AM and AM/PM conversions when the active device model is terminated with a non-ideal bias-T and with Load L_4, for three input tone separations (ΔF_1, ΔF_2 and ΔF_3).

Summarizing, four different loads were considered and several two-tone input signals, with different separation frequencies, were used. This allowed, on the one hand, the isolation of the fundamental and second harmonic contributions for the overall AM/AM and AM/PM conversions and, on the other hand, it also enabled a first study of the long-term memory effects that arise from the presence of reactive based-band terminations that will be studied in more detail in the next section.

5.2. Baseband Terminations Impact

In this section, we will focus our attention on the memory effects arising from bias networks. Neither thermal nor trapping related effects will be directly studied, although the conclusions herein derived are valid for general dynamic nonlinear systems, regardless of the physical sources of the memory effects and the nonlinearity.

The dynamic AM/AM conversion plots will be obtained from envelope-driven harmonic balance simulations and their shape, and time evolution, will be related with the output bias network (impedance presented to the transistor's output).

Fig. 111 presents the output PA equivalent circuit, presented in Section 5.1, which will be used for our theoretical study. It comprises the non-ideal bias-T of Fig. 101, connected to a linear dynamic matching network. For the sake of simplicity, it is assumed that this matching network presents a short circuit to all envelope components and has a much wider bandwidth than the signals processed - i.e., its low-pass equivalent is memoryless.

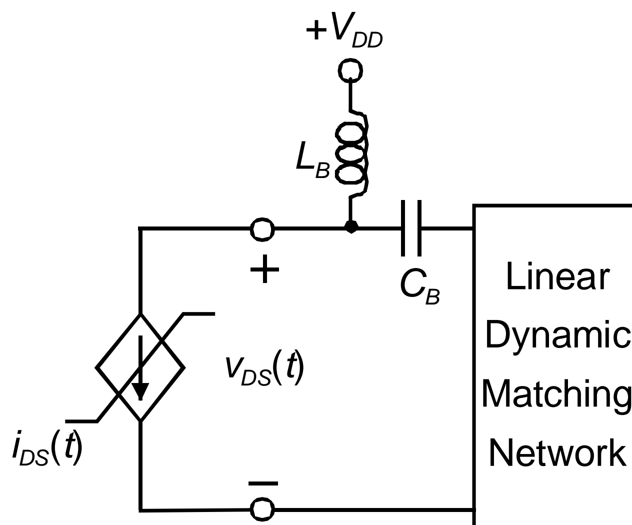

Fig. 111. Simplified output PA circuit.

We will assume an input RF signal composed by a carrier at ω_c, modulated by a complex envelope:

$$v_{in}(t,\tau) = \mathrm{Re}\left[r(\tau)\cdot e^{j\phi(\tau)}\cdot e^{j\omega_c t}\right] \tag{41}$$

in which $r(\tau)$ and $\phi(\tau)$ are the modulating complex envelope's amplitude and phase, respectively.

Similarly, the output will be given by a sum of all harmonic components of the envelope and the carrier:

$$v_{DS}(t,\tau) = \sum_{k_1=-K_1}^{K_1}\sum_{k_2=-K_2}^{K_2}\mathrm{Re}\left[r_{k_1k_2}(\tau)\cdot e^{j\phi_{k_1k_2}(\tau)}\cdot e^{jk_2\omega_c t}\right] \tag{42}$$

Looking into Fig. 111, and performing a simple circuit analysis, it is possible to derive a set of differential equations that governs the $v_{DS}(t)$ and $i_{DS}(t)$ envelope dynamics, $v_{DS}(\tau)$ and $i_{DS}(\tau)$:

$$v_{DS}(\tau) = V_{DD} - L_B\,\frac{d\,i_{L_B}(\tau)}{d\,\tau} = -\frac{1}{C_B}\int_0^{\tau} i_{C_B}(\tau)\;d\tau - v_{C_B}(0) \tag{43}$$

$$i_{DS}(\tau) = i_{L_B}(\tau) + i_{C_B}(\tau) \tag{44}$$

This analysis indicates that the PA dynamic behaviour will be strongly affected by the baseband impedance presented to the transistor, which must be shown by the AM/AM plots. Indeed, as it is shown next, if the output envelope signal frequency range coincides with a zone where the output impedance, seen by the transistor, is resistive, inductive or capacitive, the dynamic AM/AM contours will reflect these different types of induced long-term memory.

5.2.1. Practical Example

In order to illustrate these hypotheses through a practical example, we considered the simplified amplifier schematic shown in Fig. 112.

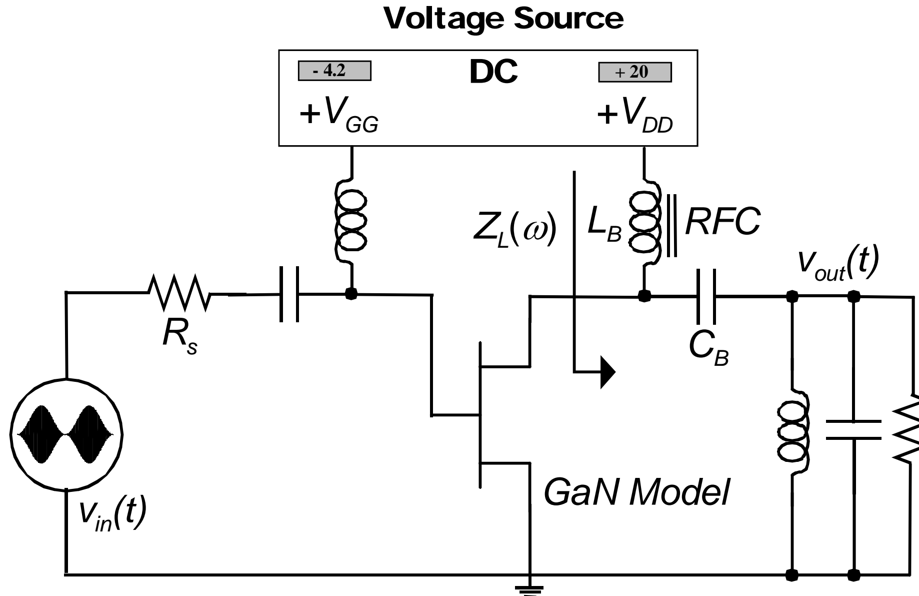

Fig. 112. Simulated PA circuit example.

The PA used in this example is a simplified version of the GaN HEMT based PA prototype previously presented in Chapter 3. The non-ideal output drain bias-T is composed by a RFC inductor, L_B=0.318mH, plus a dc blocking capacitor, C_B=500pF and the output matching network presents a short circuit to all envelope components and has a much wider bandwidth than the signals processed. Finally, the input excitation is an AM signal, with unity modulation index.

$$v_{in}(t) = A \cdot [1 + \cos(\omega_m t)] \cdot \cos(\omega_c t) \tag{45}$$

where $\omega_m = 2\pi \cdot f_m$ and $\omega_c = 2\pi \cdot f_c$.

The carrier frequency was kept constant (f_c=900MHz) and four different modulation frequencies were carefully chosen (f_{m1}=10Hz, f_{m2}=10kHz, f_{m3}=250kHz and f_{m4}= 1MHz). The first one corresponds to a static regime: C_B behaves as an open circuit $1/(\Delta\omega \cdot C_B) >> \Delta\omega \cdot L_B$ while L_B appears as a short-circuit $Ldi_{L_B}(\tau)/d\tau << V_{DD}$. For the second, third and fourth cases, the drain bias-T can be seen as a dynamic bias path (either inductive or capacitive), as depicted in Fig. 113.

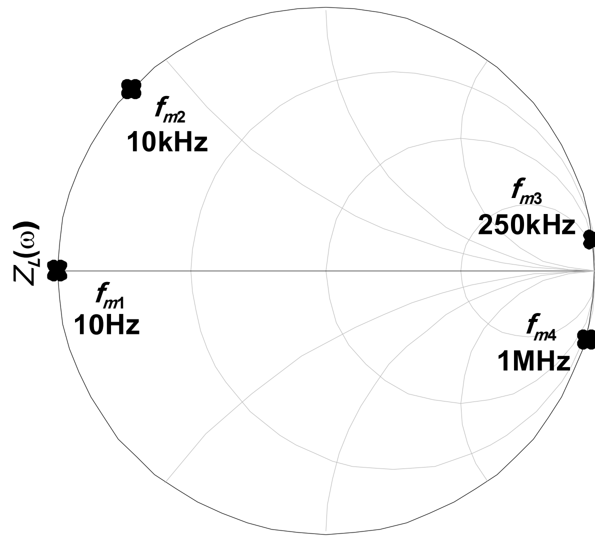

Fig. 113. Impedance presented to the transistor's output when the modulation frequency is f_{m1}, f_{m2}, f_{m3} and f_{m4}.

Several envelope-driven harmonic balance simulations, of the above circuit, were conducted.

According to what was shown in [69], the AM/AM plots can not show any long-term memory effects both in small- or large-signal regimes. This means that, in those regions, the AM/AM plots will show no hysteresis. Furthermore, the lower input level asymptote will be constant, while, in deep saturation, the AM-AM gain plot will tend to a straight line asymptote with a -1dB/dB slope.

Since we are not considering thermal or trapping effects, the presence of long-term memory (visible in the AM/AM curves as hysteresis) in the input power mid-range will only depend on the baseband impedance presented to the transistor's output.

Fig. 114 presents the observed input and output time domain waveforms, $v_{in}(\tau)$ and $v_{DS}(\tau)$, obtained for the case when the modulation frequency is f_{m1}.

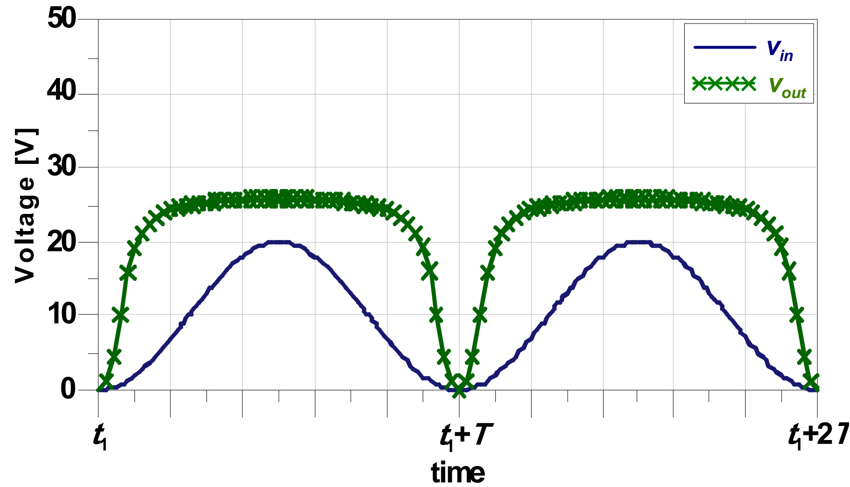

Fig. 114. Time domain input and output waveforms for f_{m1}.

The resulting dynamic AM/AM conversion plot is shown in Fig. 115.

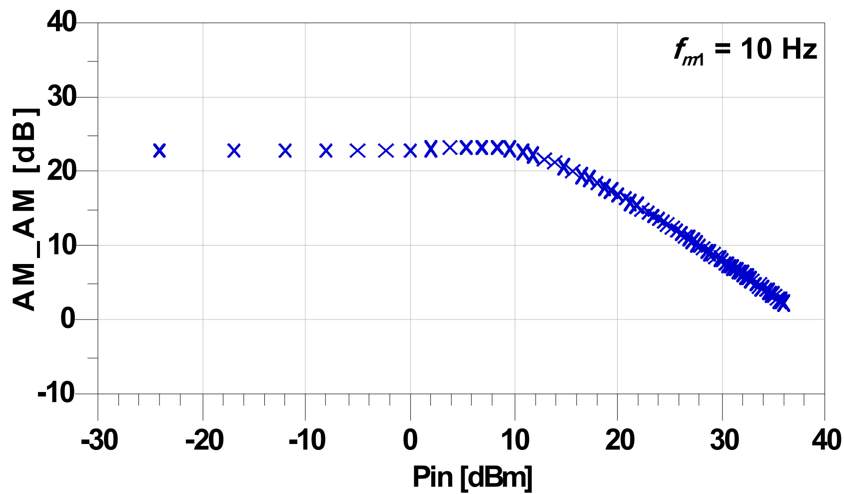

Fig. 115. Dynamic AM/AM obtained with f_{m1}.

As it is possible to see in Fig. 113, this first case study corresponds to a static analysis and, thus there are no memory effects visible on the AM/AM plot presented in Fig. 115.

In the other three cases, as seen in Fig. 113, the impedance presented to the transistor's output is no longer a short circuit. As a matter of fact, f_{m2} corresponds to a clearly inductive termination, f_{m4} to a capacitive one and f_{m3} will correspond to a mixed behaviour, since the impedance, presented to the transistor's output, has harmonic envelope components on both

the inductive and capacitive sides of the Smith chart. Hence, not only the obtained AM/AM curves will show a hysteretic behaviour, but also the plots can display a clockwise or counter-clockwise time evolution. Whenever these effects are present in the plots, their dynamic progress in time will be indicated in the figures by arrows.

In the case of f_{m2} envelope, an increase in excitation level corresponds to a smaller gain. In fact, since $di_{L_B}(\tau)/d\tau$ is positive, $v_{DS}(\tau)$ will be lower than its small-signal value (V_{DD}), the FET's dynamic load-line enters the FET's triode region and the output starts to compress. If we now have a decrease in input level, the behaviour will be opposite to this one. So, f_{m2} corresponds to a counter-clockwise time evolution. Indeed, this is the behaviour observed in Fig. 116 and Fig. 117.

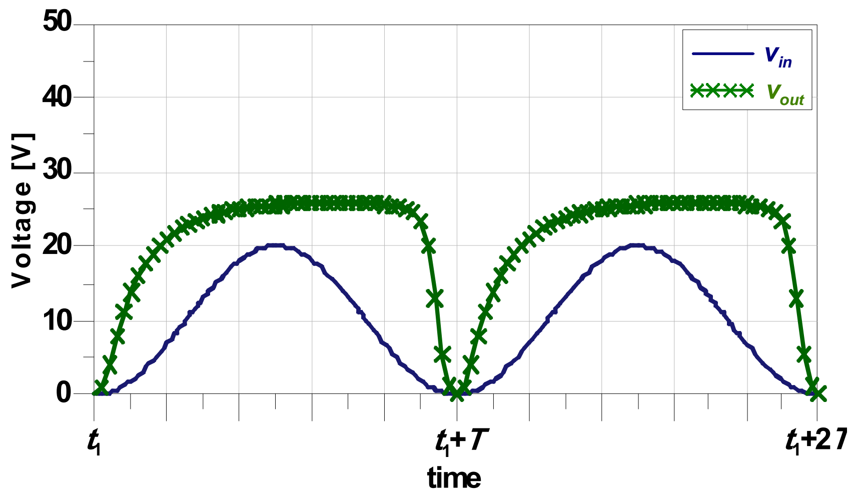

Fig. 116. Time domain input and output waveforms for f_{m2}.

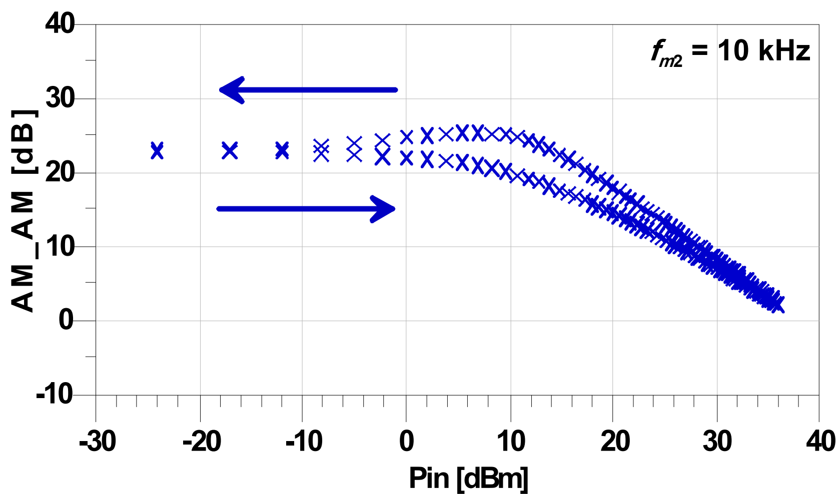

Fig. 117. Dynamic AM/AM obtained with f_{m2}.

On the other hand, when the envelope has f_{m4} frequency, an excitation level increase leads to a higher gain. In fact, since, at these higher frequencies, i_{L_B} tends to remain constant at its I_{DS} bias value, $\int_0^\tau i_{C_B}(\tau)d\tau$ is negative. Hence, (43) indicates that $v_{DS}(\tau)$ becomes higher than its small-signal value (V_{DD}). Once again, in this same operating regime, but for a decreasing input level, the behaviour will be opposite to the one previously explained. This corresponds to a clockwise time evolution.

Fig. 118 presents the observed input and output time domain waveforms, obtained for the case when the modulation frequency is f_{m4}.

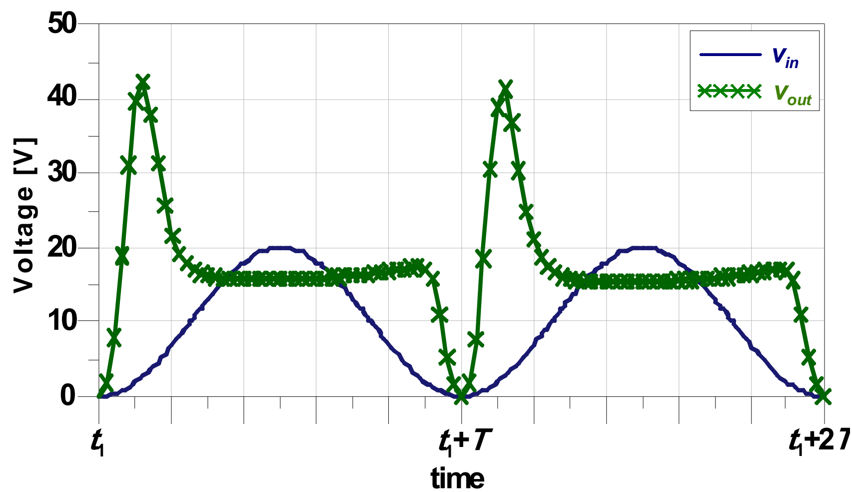

Fig. 118. Time domain input and output waveforms for f_{m4}.

The resulting dynamic AM/AM conversion plot is shown in Fig. 119.

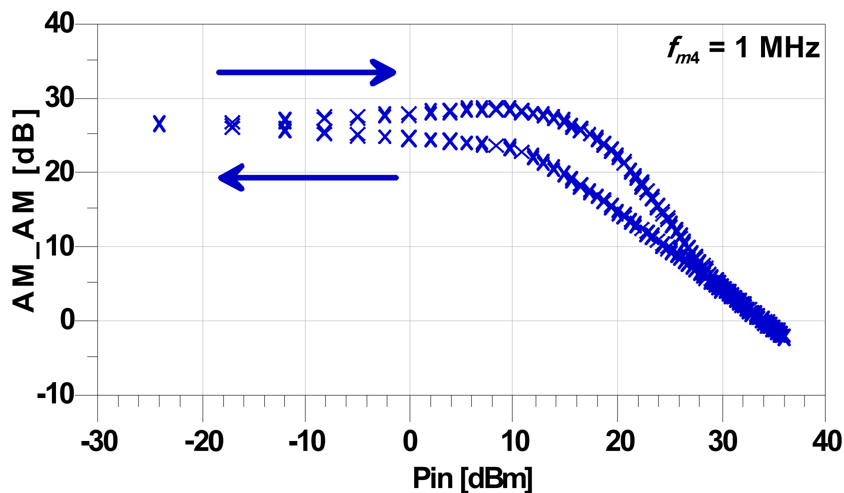

Fig. 119. Dynamic AM/AM obtained with f_{m4}.

Finally for f_{m3}, since the distorted output signal envelope will have some harmonic components in the inductive part and some others in the capacitive part of the Smith chart, (contrary to what was observed with f_{m2} and f_{m4} where all the relevant envelope harmonic components stand on the inductive or capacitive part, respectively), the AM/AM plot will have a mixed behaviour between these two.

Fig. 120 presents the observed input and output time domain waveforms, obtained for the case when the modulation frequency is f_{m3}.

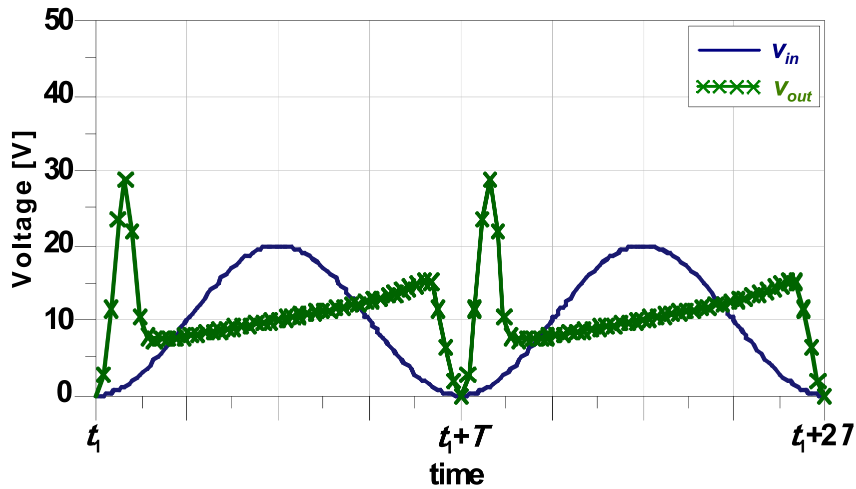

Fig. 120. Time domain input and output waveforms for f_{m3}.

The resulting dynamic AM/AM conversion plot is shown in Fig. 121.

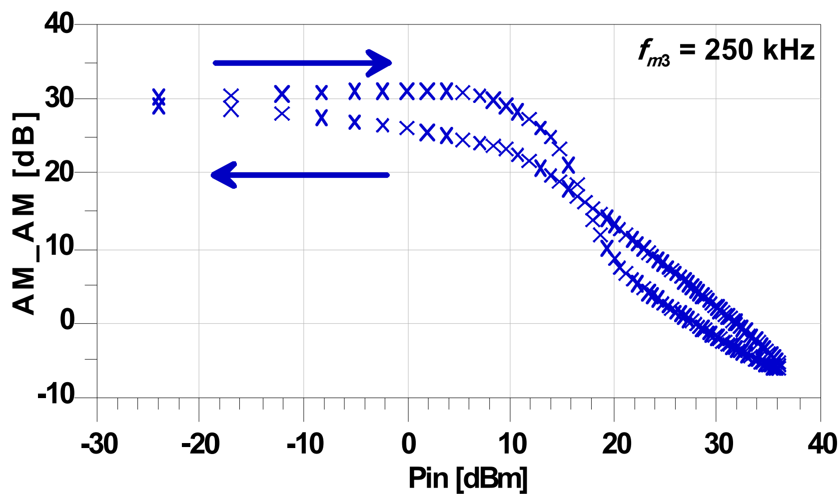

Fig. 121. Dynamic AM/AM obtained with f_{m3}.

Summarizing, when the output signal envelope spectrum is concentrated in a region where the transistor sees an inductive impedance, the AM/AM contour will follow a counter-clockwise path. If the impedance, seen by the transistor, is capacitive, the curve will follow a clockwise path. In between, i.e., when some of the envelope harmonic components see inductive behaviour while many others see a capacitive termination, we will have a mixed behaviour.

This led to the identification of specific contours for each modulation frequency, which could be explained through the different baseband output impedances seen by the transistor.

5.3. Conclusions

This chapter presented an application, of the previously extracted GaN equivalent circuit nonlinear model, to the AM/AM and AM/PM conversions study. The simulated results, obtained with the model, provided a comprehensive analysis of the baseband, fundamental and second-harmonic terminations impact in the static and dynamic AM/AM and AM/PM conversions, helping PA designers to understand and possibly prevent such amplitude and phase signal impairments, recurring to the proper load termination and bias tee design.

6. Discussions and Conclusions

Throughout this thesis, an overview of the partial results was presented at the end of each chapter. This final section summarizes the most important outcomes, explaining the main difficulties and successes obtained during this work. In addition, it also provides some clues for future research activities.

This thesis has been organized into six different chapters. Chapter 1, besides the motivation and state-of-the-art, provided an introduction to all main issues, giving special attention to the wide bandgap material characteristics and their influence on the overall RF device performance. The linearity-efficiency compromise was also addressed. The large-signal intermodulation distortion sweet-spots, very well known self-linearization points, visible in an IMD vs Pin logarithmic plot, were looked into in different PA technologies. One of the most important limiting factors in external linearization techniques, the so-called memory effects, were also presented and briefly discussed.

In Chapter 2, an equivalent circuit nonlinear global model was proposed and its extraction procedure explained, step by step, for a 2mm GaN power HEMT on Si substrate. Modelling studies proved that the expression adopted for the $i_{DS}(v_{GS},v_{DS})$ characteristic is very flexible and of intuitive extraction since it can be broken into several other smaller expressions, related with specific device operating regions, easing up the parameter extraction process.

Moreover, with this nonlinear, equivalent circuit based, large-signal model, an accurate prediction of the device's AM/AM and AM/PM conversions, output power, power added efficiency and intermodulation distortion was obtained, at the transistor level, and with a practical class AB 2W power amplifier circuit. All this, presented in Chapter 3, validated the proposed nonlinear GaN HEMT model and clearly showed its value for nonlinear microwave computer aided design.

Chapter 4, proved the robustness of the proposed GaN HEMT model. A new extraction procedure was conducted for eleven new GaN sample devices (commercially available) and the results obtained verified the model capabilities of representing the Pout and IMD behaviour of the whole set of available devices.

Finally, in Chapter 5, as an application of the nonlinear model, a comprehensive study of the different in-band and out-of-band load terminations' impact on the AM/AM and AM/PM conversions was performed. The possibility of using a nonlinear model in a commercial simulator, led to a fast and intuitive way of determining whether a certain PA circuit can present memory effects, when dealing with input signals with time-varying envelopes.

Four years ago, when this work started, the GaN devices were still in a very immature development stage. This was a very important issue since, after working with other transistor technologies, this was the first time I contacted with devices that were not yet ready to be lunched into the market.

Furthermore, since we were dealing with power transistors, the obtained samples were all packaged devices with wide gate and drain leads. This can be easily seen looking into the setup photographs presented throughout the whole thesis. From my experience, it is now obvious that this kind of modelling studies should be conducted with devices on chip, which would allow extending the model's frequency range of validity. Nevertheless, this solution has also some problems related with the transistor's power dissipation and with the power handling capabilities of the probing station itself.

Another issue I would like to address, that already produced some very interesting discussions in the scientific community, is related with the negative output conductance obtained in the IV characteristics, when performing static measurements, for high drain voltage values. Unfortunately, pulsed IV measurements are not sufficient to overcome this problem since, the thermal issues that originate those effects, also influence S-parameter measurements, affecting the extraction of G_m and jeopardize the overall nonlinear model. From my point of view, RF device modelling should evolve and use pulsed S-parameter data when extracting models for high power devices.

6.1. Future Work

In modern base-stations, due to reasons like thermal management, reliability and cost, power amplifiers have to be highly efficient. This, coupled with other requirements, such as high output power, gain, bandwidth, and linearity, puts big challenges in PA design.

Moreover, since modern communication signals, such as wideband code division multiple access (W-CDMA), have high peak-to-average ratios, during operation over that wide range of instantaneous powers, PA efficiency comes degraded. Furthermore, multiple carriers must be amplified simultaneously, resulting in very high bandwidths. So, if we add up all these strict requirements, it is easy to see that conventional RF power amplifiers can not respond properly.

Actually, one of the hottest research topics, within the field of power amplifier performance enhancement methods, is the use of new transmitter architectures in which the RF PA is working as a switch processing only the RF PM signal and the envelope is introduced via an AM modulated power supply, producing highly efficient PAs. The envelope elimination and restoration [70] or envelope tracking [71] techniques are very good examples of these new polar transmitter topologies.

The already reported results of power amplifier systems employing those techniques leave no doubts about the way to proceed clearly indicating the road towards future.

In such architectures there are many possible contributions to the undesirable signal distortion such as finite bandwidth of the envelope path or different time delay between phase and envelope paths, just to mention two widely known examples. Besides that, the power transistor itself can originate distortion. Particularly, the AM variations introduced by the modulated power supply can also produce undesired PM in its output signal.

The best way of studying all of these contributions it is to simulate those, more or less, complicated systems. For that, large-signal nonlinear active device models are crucial and can help PA designers to identify possible problems and to improve their system designs. The difficulty that now arises is concerned with the difference between the PA operation modes, in these new architectures, and the ones nowadays assumed for PAs, which determines a certain number of assumptions that influence the nonlinear model's extraction.

Conventional PAs, which I will denominate as non-switching PAs, usually operate in class C, B, AB or A and the above mentioned techniques use switching-mode amplifiers, usually operating in class E, F or D. In the new operation classes, the active device is either OFF (in the cutoff region) or ON (in the triode region). Under this ideal switching operation, the output voltage and current waveforms do not exist simultaneously. Therefore, power dissipation within the device is zero, leading to a theoretical power conversion efficiency of 100%. It is obvious that the conventional model extractions usually disregard the triode region which will now be crucial in the PA operation.

All this leaves a very big question mark in whether the formulations previously used can now be applied to the switched PAs and, I think, deserves to be studied.

Moreover, in order to exploit all the wide bandgap possibilities, already studied in this thesis, it is important to design circuits that can make use of all their unique properties. One of the hottest properties of GaN devices is the high breakdown voltage, which determines the highest operating voltage of a transistor, for a given device design and channel doping, and thus limits the RF power swing in the device. In this work, this limit region was not studied and so, in order to take advantage of all the potential of these devices should be included on the device model.

Conclusion

From a scientific point of view, this work was very challenging and was a wonderful opportunity to work on the RF active device modelling area, in a state-of-the-art technology, as it is, at this moment, GaN. Moreover, it enabled the contact with several companies, not only in the USA but also in South Korea (where I stayed working for one month), providing an industrial experience that I appreciated very much. As a matter of fact, the model presented in this thesis is already being used by two of the major GaN foundries (Nitronex Corp. and Cree Inc.) to simulate their devices, which is, I believe, one of this work's major success indicator.

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