DTIP of MEMS & MOEMS 9-11 April 2008

A Low-cost Through Via Interconnection for ISM WLP

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***Abstract*-WLP (Wafer level packaging) for image sensor device has the advantage of small size, high performance and low cost. In WLP technology, in order to establish electrical interconnection from image sensor contact pad to the backside of the wafer, several structures have been developed, such as T-contact and TSV (Through Silicon Via). In this paper, a wafer level package of image sensor with new type TSV electrical interconnection for image sensor pad is presented. The target of this development is to reduce process cost and difficulty, and to increase yield of image sensor packaging. Key fabrication processes include glass protecting wafer bonding, device wafer thinning, backside through via etching, via passivation layer deposition, pad oxide opening, via filling and backside re-routing layer formation, etc. Compared to large opening area of tapered via on the backside of CMOS image sensor wafer, only small opening area is needed for making via interconnection with vertical sidewall presented in this paper. A fillet structure at bottom corner of via holes can help to reduce sequent process difficulty, so that low-cost and simplified unit processes are successfully adopted in the fabrication process for through via formation. The through via interconnection shows good electrical connection performance, and high-quality photo images are obtained by packaged image sensor device.**

I. INTRODUCTION

With rapid development of information technology, ISM (Image Sensor Module) becomes more and more widely adopted in all kinds of mobile digital devices, especially cellular phones. Market of built-in image sensor module has also kept growing for many years. However, with the trend of miniaturization, multifunctionality, and increasing competition in market, new generation mobile devices have higher requirements for ISM, such as high performance, small form factor and low cost. Conventional ISM package, such as COB (Chip On Board) and COF (Chip On Flexible), will have difficulties to meet all those requirements due to their limitations in packaging methods. WLP (Wafer Level Packaging) Technology becomes very promising and has been studied for years for image sensor packaging [1].

WLP (Wafer level packaging) for image sensor devices has the advantage of small size, high performance and low cost. In order to form electrical interconnection from image sensor contact pad to the backside of the wafer, several structures have been developed such as T-contact and TSV (Through Silicon Via) [2][3]. T-contact type image sensor WLP has very complicated fabrication process, and it needs large pad pitch and scribe line width. However, the pad pitch and scribe line width of CMOS image sensor device wafer will continue to decrease with the development of IC technology and motivation of cost reduction. TSV type image sensor packaging is obtaining more advantages in fabrication process and cost reduction.

In this paper, a wafer level package of image sensor with novel TSV electrical interconnection for image sensor pad is presented. The target of this development is to reduce process cost and difficulty, and to increase yield of image sensor packaging. Compared to large opening area of tapered via on the backside of CIS wafer, only small opening area is needed for making the via interconnection that is presented in this paper. Vertical via etching and DFR (Dry Film Resist) lamination process can achieve lower cost and lower process difficulty than tapered via etching, spray coating and deep photolithography processes. The via bottom notch problem caused by over etch and wafer thickness non-uniformity can also be overcome by remaining a fillet structure at the bottom of vias, instead of over etch. The fillet structure can give better insulation layer and seed layer deposition yield inside the vias, without influence to bottom insulation layer opening process.

II. FABRICATION PROCESS OVERVIEW

Structure of the image sensor packaging with TSV interconnection is shown in fig. 1. Key fabrication processes includes glass protecting wafer bonding, device wafer thinning, backside through via etching, via passivation layer deposition, pad oxide opening, via filling and backside re-routing layer formation, solder ball formation, and dicing, as shown in fig. 2. All the process steps are performed at temperature lower than 200 Celsius degree, because low-temperature processes are preferred for the protection of the sensor device and micro-lens.

The image sensor WLP is composed of a 4-inch CIS (CMOS Image Sensor) wafer, a polymer bonding layer and a 4-inch glass cap wafer with thickness of 250um. The CIS

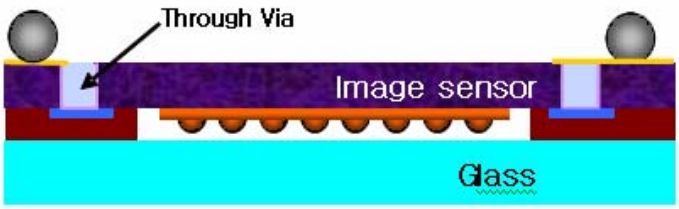


Fig. 1. Structure of ISM WLP with TSV interconnection.

ISBN: 978-2-35500-006-5

wafer and glass wafer are bonded with each other through the polymer bonding layer. After thinning the CIS wafer to a target thickness of 100um, vertical via holes with 50um-diameter are etched by DRIE process from backside of the wafer to the SiO/SiN composite insulation layer under the contact pads of the image sensor. After deposition of a SiO layer on the backside of the device wafer as well as inside the through vias for passivation, the SiO/SiN insulation layer at bottom of Al pads is etched and the Al pads are exposed for interconnection. Then via holes are filled by Cu electroplating, and backside redistribution layers and solder balls are formed.

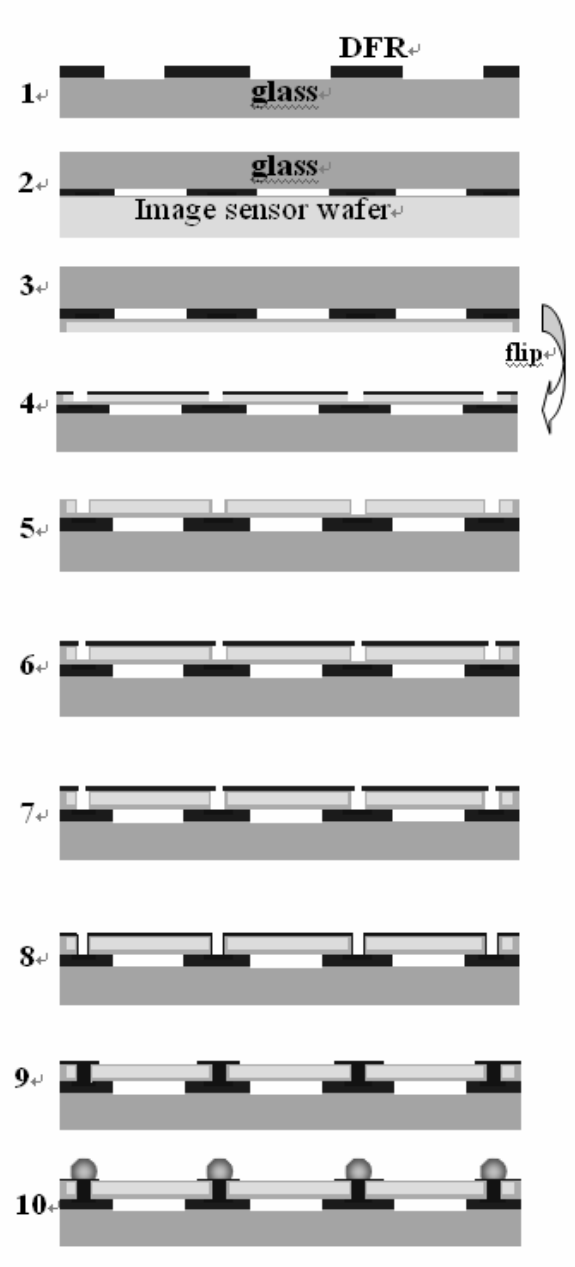


Fig. 2. Fabrication process of ISM WLP.
1. DFR patterning. 2. Adhesive bonding. 3. Wafer thinning. 4. via etching. 5. passivation layer deposition. 6. DFR lamination. 7. passivation layer etch for pad opening. 8. Seed layer deposition. 9. via filling by electroplating. 10. Solder ball formation

III. Through Via Interconnection Formation

TSV (Through Silicon Via) formation process presented in this paper includes process steps of via etch by DRIE, SiO insulation layer by low-temperature PECVD, DFR (Dry Film Resist) lamination and photolithography, Al pad opening by laser drilling, metal seed layer sputtering, and via filling by Cu electroplating, as shown in fig. 2. Key processes are explained below in detail.

3.1 Through via etch

A 6um-thick photoresist layer is coated and patterned on backside of the device wafer as etching mask for through via formation after bonding process of glass cap wafer. DRIE process is used to form vertical vias from the wafer backside surface to the insulation layer at the bottom of Al pads. Via diameter is 50um and aspect ratio is optimized as 2.0 for an optimum balance of process capability requirement between via etch process and passivation layer deposition process, as shown in fig. 3.

Through via with vertical sidewall is adopted in this design for reducing via etch process difficulty and increasing process

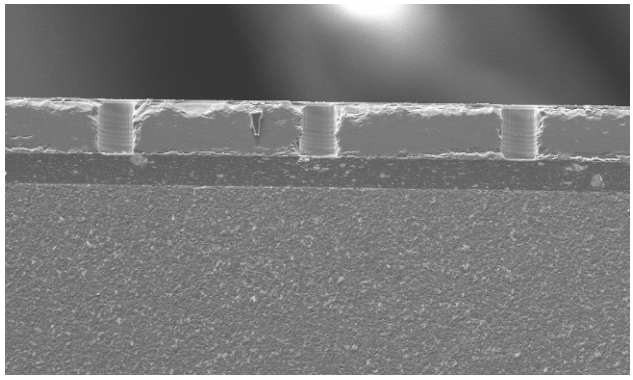


Fig. 3. Cross-sectional view of via holes

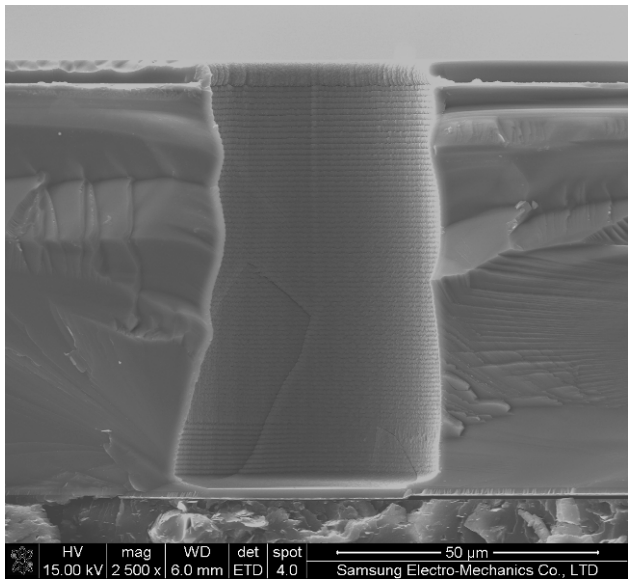


Fig. 4. Cross-sectional view of via hole with fillet structure at bottom corner

 ISBN: 978-2-35500-006-5

yield. When the insulation layer under Al pad is exposed with enough area (diameter>30um in this design) during via etch, a fillet structure with various size remains at the bottom corner of the via holes, as shown in fig. 4. This fillet structure can help to prevent notch problem when etching the bottom of via holes, so that coverage of insulation layer and metal seed layer at the bottom of via holes can also be improved with this structure.

With DRIE process for via etching, scallop on via sidewall can seriously affect insulation layer deposition result on the sidewall, and cause current leakage with deficient insulation layer coverage inside via holes. Process parameters are optimized to minimize the scallop to an acceptable size good for sequent passivation process. Notch-free process for via etch is also tested in this research as an alternative for the process with fillet structure at the bottom of via. Both HF (high frequency) and LF (low frequency) processes are used in the via etch step to get benefit of both good etch rate and notch-free process. Optimized scallop (<200nm) and notch (<1um) are achieved, as shown in fig. 5.

3.2 Backside passivation layer deposition

A SiO passivation layer is deposited on wafer backside and inside via holes by low-temperature PEVCD process at 100 Celsius degree. The process is optimized for good step coverage, sufficient passivation thickness and acceptable deposition rate. A 1um-thick passivation layer at via bottom and sidewall is achieved to provide sufficient passivation effect for sequent via filling process. Multi-step deposition process is used for film stress compensation and wafer warpage control. Fig. 6 shows the passivation layer after deposition process.

3.3 Al pad opening (Via bottom insulation layer etch)

The composite insulation layer under Al pads of image sensor device includes multiple layers of SiO and SiN. At the bottom of the via holes, this layer needs to be etched to expose Al pads for formation of electrical interconnection to backside of the device wafer. Etching process must be

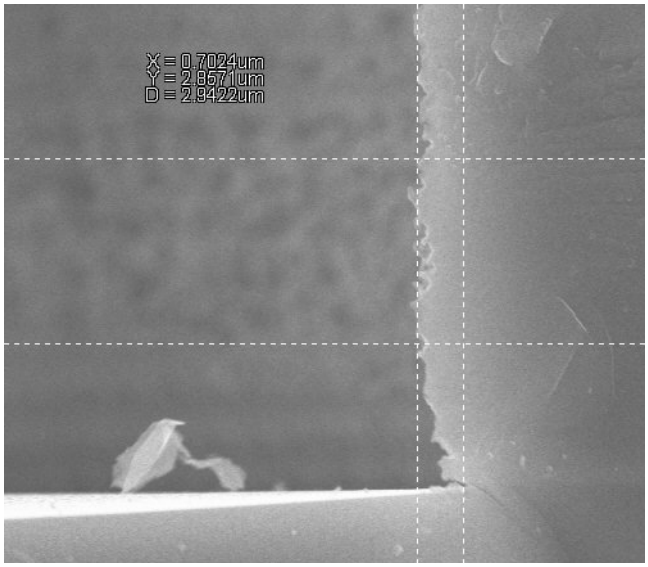
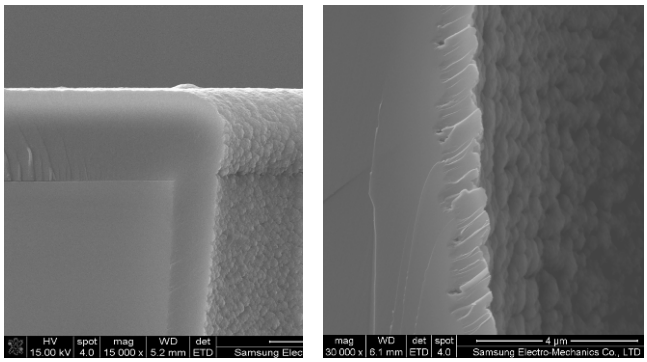


Fig. 5. Via bottom etch result with optimization of scallop and notch.



(a) Top of via hole (b) Sidewall of via hole

Fig. 6. SiO passivation layer deposition result.

carefully optimized to provide sufficient etching depth to ensure a clear opening area under Al pad, also without damage of Al pad and passivation layer on via sidewall and fillet structure at the bottom corner of the via.

Two etching processes, dielectric dry etch and laser drilling, are tested in this research. For dry etch process, a DFR layer is laminated and patterned on the backside of image sensor device wafer as etching mask. Opening with 30um diameter is formed above each via hole. Since via hole diameter is 50um, the etching mask with 30um-diameter opening can help to etch the via bottom insulation layer in the center of via bottom surface, without damaging the passivation layer on the fillet structure. However it is difficult

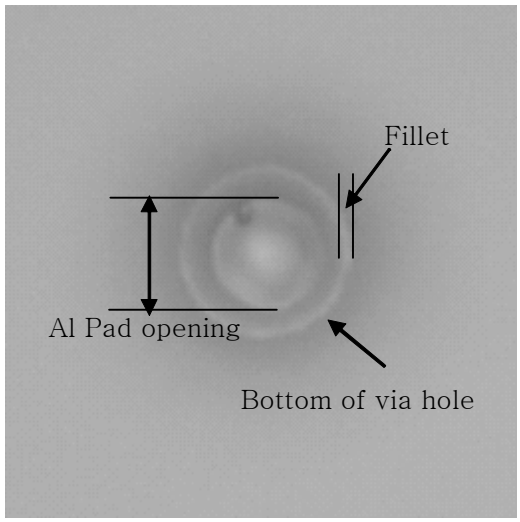


Fig. 7. Bottom of via hole after dry etch of Al pad opening.

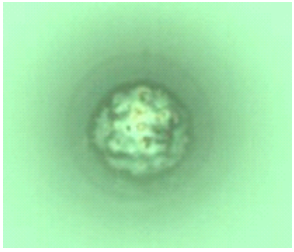


Fig. 8. Al pad opening etched by laser drilling.

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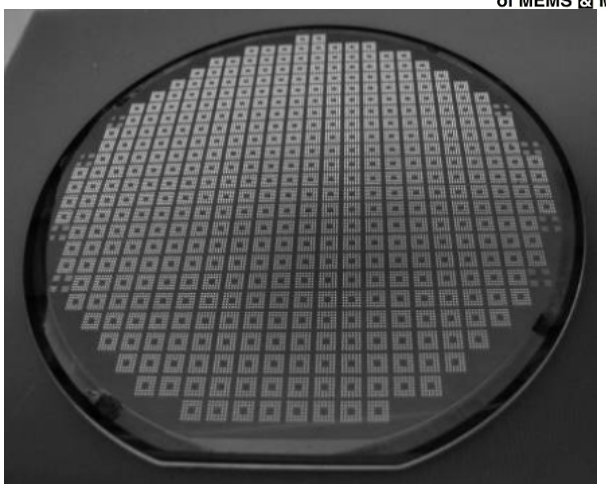

Fig. 9(a). CMOS Image sensor wafer after WLP (Backside)

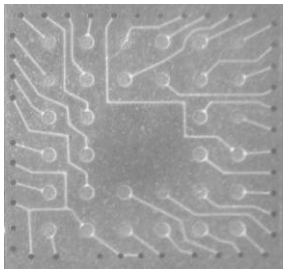

Fig. 9(b). Backside of image sensor package chip.

to control dielectric dry etch process to stop at a proper end point because the Al pad layer is very thin and easily damaged. So yield of the dielectric dry etch process for pad opening is very low. The process result is shown in fig. 7. Laser drilling process is also tested to make openings in the insulation layer under Al pads. Etching selectivity between SiO/SiN layer and Al pad layer is very important to prevent damage of Al pad. Excimer laser shows good selectivity with carefully selected wave length and energy. Fig. 8 shows the pad opening result after laser drilling.

After seed layer deposition and Cu electroplating, electrical interconnection is established from Al pad of image sensor device to the backside of the wafer. GND-to-GND resistance of 2.5ohm is achieved by this TSV interconnection.

IV. Wafer Fabrication Result

The CIS wafer after wafer level packaging with the TSV interconnection is diced and tested, as shown in fig. 9. Final package size is 3.67mm X 3.42mm X 0.39mm, which is the same size as the image sensor chip. Resolution and color test result is shown in fig. 10. High-quality photo images are also obtained during test. The through via interconnection adopted in this image sensor package shows good electrical connection performance. The fillet structure helps to reduce process difficulty, so that low-cost and simplified unit processes are successfully adopted in the fabrication process for through via formation, including vertical via DRIE, SiO PECVD, DFR lamination, laser drilling, and so on.

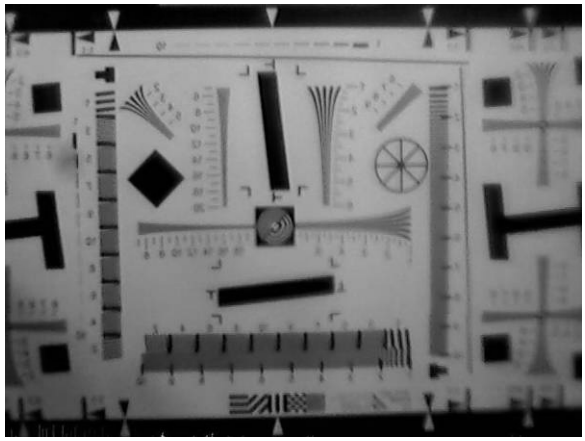

Fig. 10(a). Resolution test for image sensor package.

Fig. 10(b). Color test for image sensor package.

V. Conclusion

A low-cost through via interconnection is developed for CMOS image sensor WLP. The process steps used for fabrication are based on the consideration of low cost and good processablity. Image sensor package using this through via interconnection shows good electrical performance and it can gives good working result. This research demonstrates the performance and fabrication validity of the low-cost through via interconnection with fillet structure and laser drilling process for Al pad opening, and shows that this technology is suitable for the application of ISM wafer level packaging.

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