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Evaluation of Border Traps and Interface Traps in HfO_2/MoS_2 Gate Stacks by Capacitance - Voltage Analysis

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Abstract Border traps and interface traps in HfO_2/few-layer MoS_2 top-gate stacks are investigated by C-V characterization. Frequency dependent C-V data shows dispersion in both the depletion and accumulation regions for the MoS_2 devices. The border trap density is extracted with a distributed model, and interface traps are analyzed using the high-low frequency and multi-frequency methods. The physical origins of interface traps appear to be caused by impurities/defects in the MoS_2 layers, performing as band tail states, while the border traps are associated with the dielectric, likely a consequence of the low-temperature deposition. This work provides a method of using multiple C-V measurements and analysis techniques to analyze the behavior of high-k/TMD gate stacks and deconvolute border traps from interface traps.

Keywords: transition metal dichalcogenides (TMDs), border traps, interface traps, HfO_2 / MoS_2, capacitance - voltage (C-V)

Introduction Recently, transition metal dichalcogenides (TMDs) have attracted wide attention due to their unique properties [1]. The "2-dimensional" structures, and energy bandgaps that are comparable to Si [2], make these materials promising for field effect transistor (FET) applications and possible deep scaling beyond Si [3]. TMD-based transistors, such as single-layer to few-layer MoS_2 transistors, have been demonstrated with high mobility, low subthreshold slope, and excellent on/off ratios [4,5]. Also, flexible electronics is a promising application for these TMD materials, considering their extraordinary mechanical properties [6]. The relatively inert surface of MoS_2, however, prevents the formation of a uniform dielectric layer on the MoS_2 [7], which makes sub-10 nm high-k layer deposition difficult without proper surface preparation. A promising surface functionalization method – exposing the TMD surface to UV-O_3 [8,9] – has been reported, to enable the deposition of a smooth, pin-hole-free sub-10 nm high-k dielectric layer on TMDs. However, the low temperature high-k deposition process is anticipated to result in border traps as well, which are defined as near-interfacial oxide traps [10].

Capacitance - voltage (C-V) measurements are a relatively fast and robust electrical characterization method to probe interface traps and dielectric border traps. To apply C-V techniques to few-layer TMDs, a gated area large enough to ensure a good signal-to-noise ratio is required, and series resistance [11] must also be considered to enable reliable measurements and analysis. Frequency-dependent C-V has been reported recently [12–14] to extract the interface trap density (D_{it}) in back-gated [12] and top-gated [13,14] MoS_2 devices, but the characterization and analysis of border traps associated with such high-k/MoS_2 devices by C-V techniques has not been reported previously.

In this work, border traps and interface traps in HfO_2/few-layer MoS_2 top-gate stacks are investigated by C-V characterization. Frequency dependent C-V data shows "dispersion" in both

the depletion and accumulation regions of C-V curves. A model of distributed border traps [15–17] (commonly used in III-V/high-k devices) is used to fit the MoS_2 C-V data and explain the dispersion in accumulation. Furthermore, the interface traps (D_{it}) and trap time constant (τ_{it}) in HfO_2/MoS_2 gate stacks are analyzed [13,18] to demonstrate a procedure to identify and differentiate those various trap effects based on C-V measurements of MoS_2 devices.

Experiments Few-layer MoS_2 transistors were used as the test structure [19] for the electrical characterization in this work. The MoS_2 thicknesses studied here ranged from 5-10 layers (3-6 nm). A detailed procedure of flake selection and device fabrication has been reported in our previous work.[19,20] MoS_2 flakes were mechanically exfoliated [4] from a commercial synthetic crystal and transferred onto SiO_2/Si substrates, where the thickness of thermal SiO_2 was 270nm. By using conventional photolithography, Au/Ti (100/20 nm) source/drain (S/D) regions were deposited by e-beam evaporation at 2×10^{-6} Torr, followed by a lift-off process. An ultra-high vacuum anneal was performed to remove contaminants from the MoS_2 surface [20]. Prior to HfO_2 deposition, the MoS_2 surface was treated by UV-O_3 [8] to enable a smooth, pin-hole-free high-k dielectric layer. A 9.3 nm HfO_2 layer (measured by ellipsometry) was deposited at 200˚C with atomic layer deposition (ALD) immediately after the treatment without breaking vacuum. The gate was formed by photolithographic definition and Au/Cr (100/20nm) metal deposition with a lift-off procedure. A 400˚C forming gas (5% H_2 in a balance of N_2) anneal was performed for 60 minutes to complete device fabrication [20]. Electrical measurements in this work were performed using a Keithley 4200 Semiconductor Characterization System and an Agilent E4980A LCR meter at room temperature (25˚C) in a shielded probe station. The source and drain of a transistor were connected together as the negative electrode and the gate was the positive

electrode with the back-gate disconnected from the measurement (Fig. 1a). Variable frequency C-V measurements were conducted to investigate the high-k gate stacks.

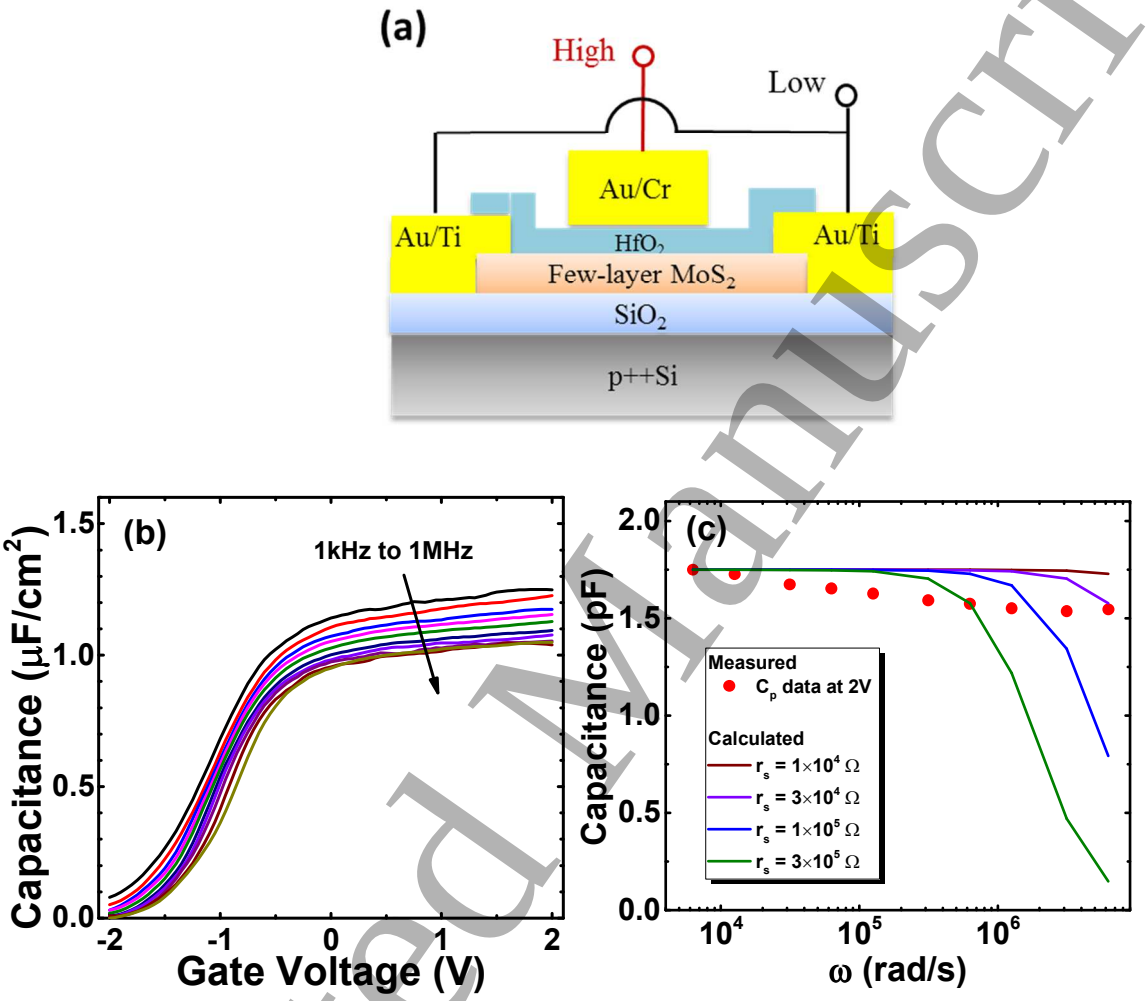


Figure 1. C-V characterization on an HfO_2/MoS_2 top-gated stack. Gated area: 1.02×10^{-6} cm^2 (W×L = 10.6 μm × 9.6 μm). (a) Schematic cross section of the top-gated MoS_2 device in this work. (b) Measured capacitance in the frequency range 1kHz to 1MHz. (c) C-V data and series resistance model. Multiple r_s values are assumed, but they cannot fit the observed dispersion.

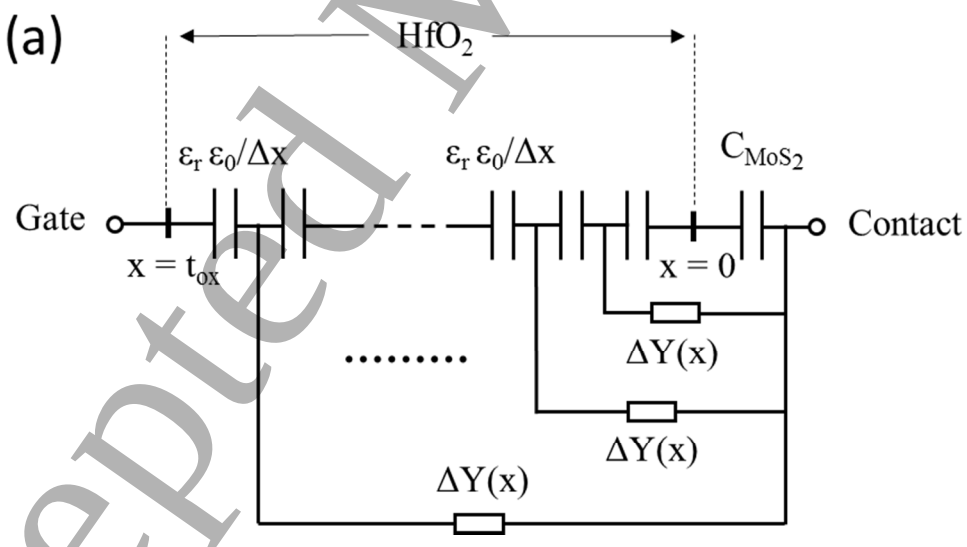
Results and Discussion A frequency-dependent C-V plot for a HfO_2/MoS_2 gate stack is shown in Fig. 1b. The gated area is 1.02×10^{-6} cm^2 (W×L = 10.6 μm × 9.6 μm). The

corresponding I-V characteristics of this transistor are shown in supplementary data Fig S.1. The capacitance measured from 1 kHz - 1 MHz shows n-type (electron) response, with the accumulation region in a voltage range from -0.5 V to 2 V. The few-layer MoS_2 flake is fully depleted at about -2V, with flat C-V curves shown in high frequencies at -2V. Note that the C-V curves show an apparent frequency dispersion in the accumulation region. The separation between each curve is almost constant with each decade of frequency, the same as that detected for III-V/high-k devices [21–23]. Thus, a traditional three-element model [24] cannot explain this frequency-dependent behavior (Fig. 1c.), where the capacitance is supposed to drop rapidly with an ω^{-2} dependence due to series resistance and dielectric leakage. Yuan et al. reported a distributed border trap model [15,16] to explain the dispersion in accumulation. In that model, border traps *in the dielectric a relatively short distance from the interface* [10] can capture carriers in the semiconductor after a tunneling process. Since the tunneling time constant exponentially increases with the separation between border traps and the interface, the applied frequency can significantly affect the impedance response. This distributed border trap model is applied to the MoS_2 devices in our work by the equivalent circuit shown in Figure 2a that includes border trap effects in the measured admittance through the differential equation [16]

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon_r\varepsilon_0} + \frac{q^2 N_{bt} \ln\left(1+j\omega\tau_0 e^{2\kappa x}\right)}{\tau_0 e^{2\kappa x}};\ \kappa = \sqrt{2m^* E_b}/\hbar \qquad (1)$$

where N_{bt} is the density of border traps (in #/cm^3/Joule), $\omega=2\pi f$ is the measurement frequency, τ_o is the trap time constant at the interface, κ is the attenuation coefficient, ε_r and m^* are the relative permittivity and effective electron mass in HfO_2, respectively, and E_b is the conduction band offset of the dielectric/semiconductor interface. By solving this differential equation, the capacitance and conductance can be extracted from the admittance Y. The experimentally

measured data and the simulations from this model are compared in Figs. 2b and 2c. With the parameters shown in Table 1, the measured capacitance and conductance at 2V are able to provide a robust fit to the measured data, with a border trap density of $N_{bt} = 3.2\times10^{20}$ $cm^{-3}eV^{-1}$. This is in the same range of reported N_{bt} values in high-k/III-V gate stacks [25]. The low-temperature ALD may be the cause of the N_{bt} in the HfO_2 dielectric layer. The distributed border trap model provides a reliable way of N_{bt} extraction of TMD-based devices with high-k dielectrics. The model is valid from accumulation to near flat-band voltage [16]. The border trap density is extracted in the accumulation region where they have the largest impact in this work. In the depletion region, because the tunneling time would be extremely large due to low electron density, the border traps have minimal impact.



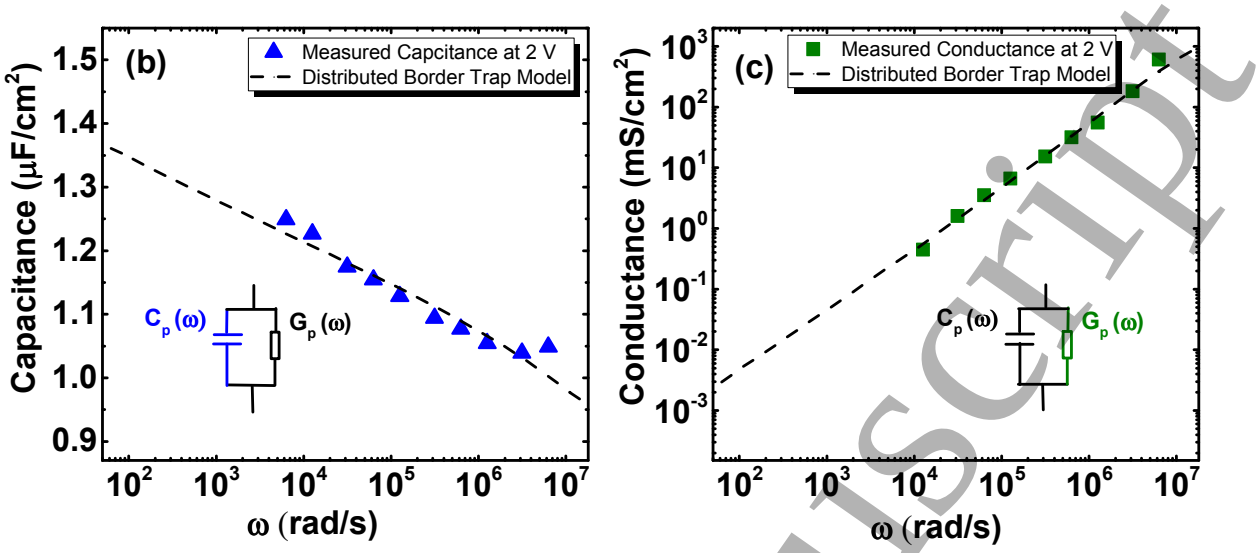
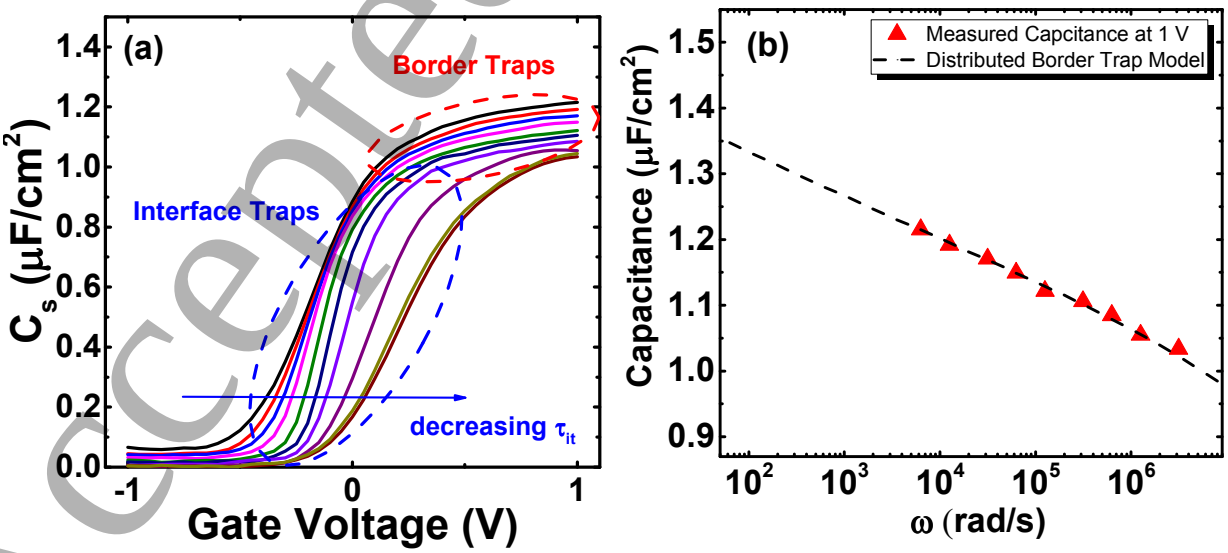


Figure 2. Border trap density extraction from capacitance and conductance. (a) Equivalent circuit of admittance measurement including border trap effect; (b), (c) Capacitance and conductance modeling and data fitting with distributed border trap model. $N_{bt} = 3.2\times10^{20}$ cm^{-3} eV^{-1} is extracted.

Table 1. Parameters used in distributed border trap model

τ_0 (s)	ε_r [26]	m* (× m_0) [27]	E_b (eV) [7]	κ (nm^{-1})	t_{ox} (nm)	C_{MoS2} (μF/cm^2)
1.0×10^{-7}	13	0.15	2.1	2.9	9.3	3.3



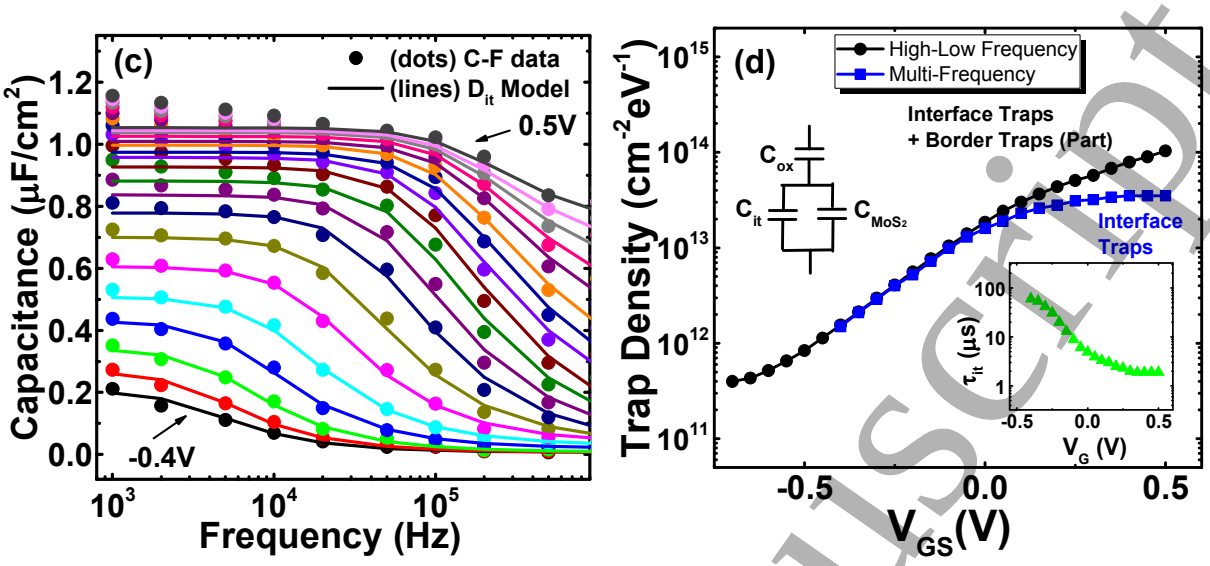


Figure 3. Extraction and deconvolution of N_{bt} and D_{it}, from C-V characterization. Gated area: 1.09×10^{-6} cm^2 (W×L = 12.4 μm × 8.8 μm). (a) Frequency dependent C-V showing response of N_{bt} and D_{it}. (b) N_{bt} = 2.9×10^{20} $cm^{-3}eV^{-1}$, extracted by distributed border trap model at V_{GS}=1 V. (c) D_{it} and τ_{it} extraction using the multi-frequency method. This C-F figure clearly shows a transition frequency at each voltage, suggesting interface trap time constants. At low frequencies and positive V_{GS}, response of border traps dominates, resulting in imperfect fit. (d) High-low frequency method and multi-frequency method comparison. The difference in trap density shown between 0 V to 0.5 V is caused by border trap response at lower frequencies. The inset figure shows the extracted τ_{it}.

Next, we show a method to differentiate the effects between interface traps and border traps. Capacitance of another sample fabricated with the identical process is shown in Fig.3a. The gated area is 1.09×10^{-6} cm^2 (W×L = 12.4 μm × 8.8 μm). In the accumulation region, a border trap response is observed; the capacitance linearly changes with log (ω) at a given voltage. The distributed model is used with the same parameters (Table1), and N_{bt} = 2.9×10^{20} $cm^{-3}eV^{-1}$ is extracted (Fig. 3b), which is very close to that extracted from the first sample (Fig.2). In the

depletion region (-0.5 V to 0.5 V), however, the frequency dependent response in the C-V does not follow the border trap model. At a given voltage (e.g. 0 V), the capacitance dispersion is much larger in a certain range of frequency (e.g. 50 kHz-200 kHz) than in other frequency ranges. Fig. 3c shows the capacitance as a function of frequency from -0.4 V to 0.5 V. Usually in MOSCAPs with defective interfaces, interface traps capture/release electrons and generate an interface trap capacitance, C_{it}, at low frequency. At high frequencies, they no longer respond to the small AC signal and C_{it} is 0. The transition frequency, where a sharp decrease of capacitance is seen in Fig. 3c, is determined by the interface trap time constant, τ_{it}. Similar C-V response for MoS_2 devices was also reported by other researchers [13]. An equivalent circuit including C_{it} is shown in the inset of Fig. 3d, where C_{it} is given below, considering a distribution of defect levels in the bandgap [28]:

$$C_{it} = qD_{it} \cdot (\omega\tau_{it})^{-1} \cdot tan^{-1}(\omega\tau_{it}) \quad (2)$$

where D_{it} is the density of interface traps (in #/cm^2/eV). The calculated capacitance is compared with the measured 1k-1MHz data in Fig. 3c, utilizing D_{it} and τ_{it} both as fitting parameters. The extracted peak D_{it} is 3.5×10^{13} cm^{-2} eV^{-1} for this device, and τ_{it} ranges from 1 to 100 μs range, depending on the gate voltage (Fig. 3d). The high-low frequency method [24] is also used to extract the trap density D_t (Fig. 3d) using

$$C_t = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1};\ D_t = C_t/q \quad (3)$$

where C_t is the capacitance of traps, C_{LF} and C_{HF} are the measured capacitances at the lowest and highest frequencies used in the measurements. The high-low frequency method detects all traps (e.g. interface traps, border traps, bulk traps) that can be electrically stimulated by the AC signal within the ranges of the applied frequency and voltage. The extracted trap density overlaps with

the above "multi-frequency extracted" D_{it} from -0.5 V to 0V but deviates from it between 0 V and 0.5 V. In fact, if one considers all the four figures together (Fig. 3a-d), one can find that in Fig. 3a, the C-V curves start to have an additional low-frequency response from 0 V to 0.5 V due to the existence of border traps. The measured capacitance continues to increase with decreasing frequency indicating that border traps begin to dominate the C-V frequency response when V_{GS} is greater than 0V. In the case of the high-low frequency method, where capacitance at only two frequencies are utilized, the results contain an extracted trap density that is comprised of D_{it} in addition to all of the N_{bt} that can respond to the 1kHz-1MHz AC signals. The multi-frequency model, on the other hand, simultaneously fits many more than two frequencies. To accurately fit the measured capacitance in the high frequency range (Fig. 3c), only D_{it} is utilized since border trap response is minimal at those frequencies. However, the measured low-frequency data deviates from the low-frequency simulation using the D_{it}-only multi-frequency model. The difference between the measured and modeled data therefore provides an estimate of the border trap density. This can be seen in Fig. 3d, where both extraction methods provide quite similar D_{it} values in the regime where D_{it} dominates (Fig. 3a, between -0.5 V to ~0 V). Then, the deviation between the D_{it}-only multi-frequency and high-low methods (between ~0 V to 0.5 V) can be used to estimate the N_{bt} contribution that responds at lower frequencies.

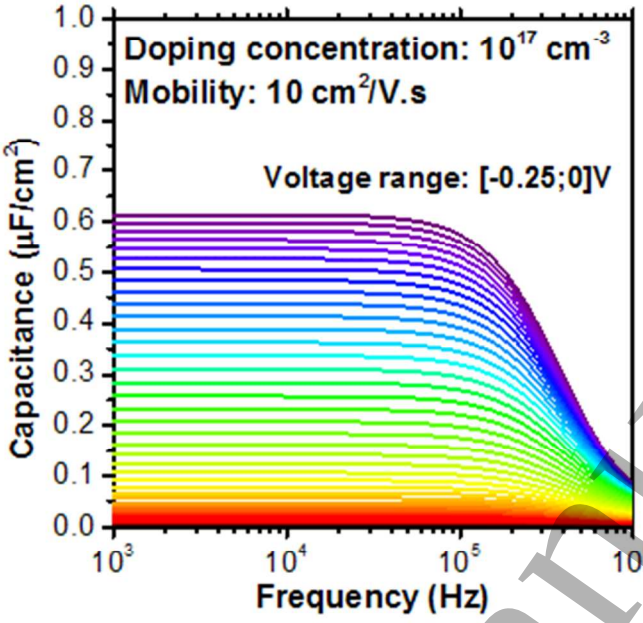


Figure 4. TCAD simulation [31] to study the channel resistance. C-F response in the depletion region for a trap-free MoS_2 transistor with μ=10 $cm^2/V{\cdot}s$ and n_{doping} = 10^{17} cm^{-3} is shown. The C-F trends have a significant difference than the trends caused by D_{it} (figure 3c). Furthermore, the locus of the corner frequency, as the bias moves from depletion to accumulation in the simulations, is opposite to what is seen experimentally. More details are provided in Figure S4.

Since a distributed channel resistance [29,30] in thin flakes could exist, which usually causes C-V frequency dispersion and lead to an overestimation of the D_{it}. Thus, we study the resistance effect carefully using a model reported in the literature [30] and the continuum-based Synopsys TCAD simulator Sentaurus Device [31]. Details are shown in the supplementary figures S3 and S4. The simulated C – F shows a plateau region followed by a fast decrease in capacitance with log (F) with a clear -2 gradient for any mobility or carrier concentration (here only the case of μ=10 $cm^2/V{\cdot}s$ and n_{doping} = 10^{17} cm^{-3} is shown in figure 4). The capacitance decreases toward

zero fast at higher frequencies in both depletion and accumulation regions. The experiment data, on the other hand, shows a much slower decreasing trend of the capacitance vs. frequency, which is consistent with the D_{it} model rather than the channel resistance simulation. Also, the locus of the corner frequency as the bias moves from depletion to accumulation in the simulations is opposite to what is seen experimentally. The increase in the corner frequency in the experimental results to higher frequencies as the bias moves from depletion to accumulation is consistent with an interface state response. With the comparison between the simulation and the experimental results on C-V and C-F (Figure S4), it is clear that the channel resistance has little influence on the extraction of electrically active defects in our devices. The absence of the resistance effect can be attributed to a relatively high intrinsic doping (10^{18}-10^{19} cm^{-3}) due to defects and impurities, and possibly an intrinsic mobility that is higher than the field effect mobility which is usually a rough estimation. As better dielectric/TMD interfaces reduce the trap density, the effects of channel resistance could become more apparent; and therefore, have more of an effect in the analysis.

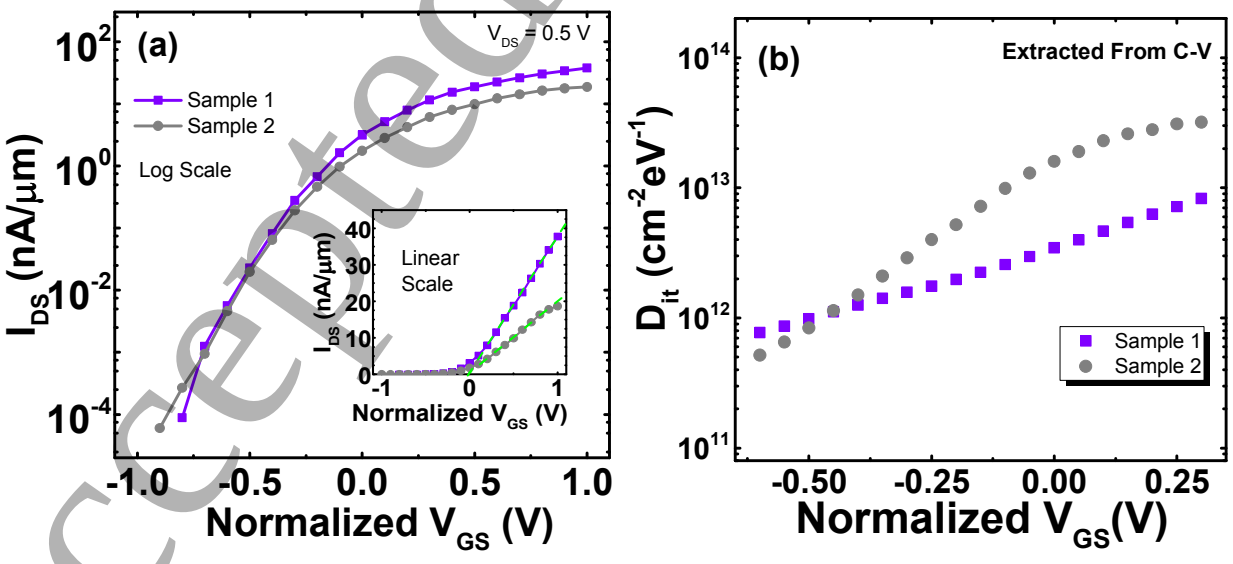


Figure 5. I-V characteristics and D_{it} extraction from C-V. (a) I_D-V_G curves for both samples. (b) D_{it} extracted from C-V characteristics.

The I_D-V_G characteristics are also studied for both transistors shown in this work, to further validate the D_{it} extraction. Fig. 5a shows the I_D-V_G curves of sample 1 and 2 (referred to C-V data in Fig.1 and Fig.3, respectively). The gate voltage is normalized to make these two transistors have the same threshold voltage. The field effect mobility is 0.63 $cm^2/V{\cdot}s$ and 0.32 $cm^2/V{\cdot}s$ for each sample, respectively. Fig. 5b shows the corresponding D_{it} extraction result from C-V characteristics. It can be clearly seen that the transistor which has lower D_{it} shows a better subthreshold slope (SS) and higher On current. However, to accurately calculate the D_{it} from SS, accurate knowledge of the capacitance of the MoS_2 channel (C_{MoS2}) is needed, which requires knowing the exact doping density. Without knowing the doping density, the SS should not be used to calculate the D_{it} value [24]. Further, since these two MoS_2 flakes are exfoliated from a crystal where unintentional doping may not be uniform, it is improper to compare the SS values quantitatively, as well. But semi-quantitatively, the D_{it} extracted from C-V, and the SS values, correspond to each other in good agreement, which validates the D_{it} extraction methods we use with C-V characterization.

Fig. 6 shows a schematic energy distribution of border traps and interface traps which can be detected by C-V in our work, in a HfO_2/MoS_2 energy band diagram. Since the border trap density is extracted from the accumulation capacitance, it only represents the density in a narrow energy range close to the MoS_2 conduction band edge. Although the distributed model [15,16] includes an assumption that the border trap density should be uniform through the dielectric film, the N_{bt} extracted in this work should mostly represent the trap density within about ~1.4 nm away from the HfO_2/MoS_2 interface due to the tunneling nature of these traps and the limited

frequency range (supplementary data S5). For D_{it} extraction, the methods used in this work are only valid when the whole flake is not fully depleted. The time constant τ_{it}, shown in Fig. 3d, decreases almost exponentially with increasing voltage, as the C-V detects shallower traps and the electron density is high in the conduction band, enabling faster capture/release of electrons. Meanwhile, the D_{it} increases from depletion to accumulation region in the C-V characteristics. A plausible explanation would be the existence of a band tail states [13] close to the conduction band.

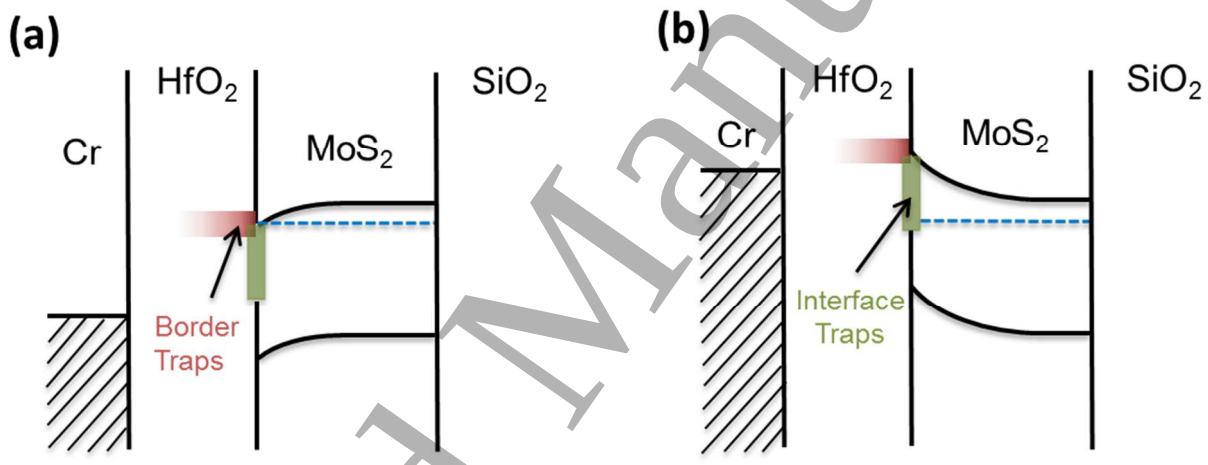


Figure 6. Schematic energy band diagram of $Cr/HfO_2/MoS_2$ with border traps and interface traps. (a) In accumulation region, Fermi-level of MoS_2 is close to border trap energy, causing C-V frequency dispersion. (b) In depletion region, Fermi-level of MoS_2 sweeps across interface traps. Shallower traps with shorter τ_{it}, are able to react with higher frequency AC signals.

The two devices shown in this work have similar border trap densities (Figs.2b and 3b) but different D_{it} distributions (Fig. 5b). Since these two MoS_2 flakes were exfoliated from the same synthetic crystal and underwent the same fabrication process, it can be inferred that the physical

origin of the interface traps are some pre-existing non-uniform impurities and/or defects [32] in these flakes, which can vary from device to device. Also, if those defects were sulfur vacancies, the distribution should be peaked [33], not uniform in energy. In the work by Takenaka et al.[12], the authors drew a similar conclusion that the D_{it} is due to defects in the MoS_2 itself rather than in the dielectric as they determined the D_{it} was independent of the dielectric layers used, although they did attribute the D_{it} response to sulfur vacancies based on their observed peaked distribution. On the other hand, there is minimal variation in the extracted border trap density for each MoS_2 flake because the HfO_2 layer is deposited simultaneously on both samples with the same process. The border traps are likely a consequence of the low ALD temperature, the deposition rate on MoS_2, and the lack of any post-dielectric anneal. There was no post-dielectric anneal in order to solely investigate the as-fabricated interfacial region after the in-situ UV-O_3, ALD HfO_2 deposition.

Conclusion In summary, border traps and interface traps in HfO_2/few-layer MoS_2 top-gate stacks are investigated by C-V characterization. With frequency-dependent C-V data, the border trap density is extracted with a distributed model and interface traps are analyzed using the high-low frequency and multi-frequency methods. The physical origins of interface traps appear to be caused by impurities/defects in the MoS_2 layers, performing as band tail states, while the border traps are associated with the dielectric, likely a consequence of the low-temperature deposition. This work provides a method of using multiple C-V measurements and analysis techniques to analyze the behavior of high-k/TMD gate stacks and deconvolute border traps from interface traps.

Supplementary Data I-V data and microscopic pictures corresponding to C-V characterization; Equivalent circuits for multi-frequency D_{it} analysis; Channel resistance; Calculation of the tunneling distance at 1 kHz for the border traps.

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