

High bandwidth density optically interconnected Terabit/s Boards

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ABSTRACT

Within the European Project TERABOARD, a photonic integration platforms including electronic-photonic integration is developed to demonstrate high bandwidth high-density modules and to demonstrate cost and energy cost target objectives. Large count high bandwidth density EO interfaces for onboard and intra-data center interconnection are reported. For onboard large count interconnections a novel concept based on optical-TSV interconnection platform with no intersections and no WDM multiplexing is reported. All input/output coupler arrays based on a pluggable silica platform are reported as well.

Keywords: Integration, 3D, Interconnection, Data center, PIC, EIC, Silica

1. INTRODUCTION

Application driven core photonic technology developments and optical communication for data centers require low-cost, energy-efficient photonic devices supporting radically new systems and network architectures, driven by the emergence of exa-scale cloud data centers. The focus is on optical inter- and intra-data center transmission, switching and interconnects facilitating Tb/s interface speeds and Pb/s network throughput.

The European project TERABOARD proposes the demonstration of a scalable, low power, low cost photonic technology to sustain the continuous increase of bandwidth density by leveraging on combination of scalability and low energy consumption. A complete solution for scalable low-energy optical interconnections is proposed, to be used in multiple application scenarios, ranging from intra-board through intra-data center communication, such as high-speed switch/router line cards, baseband processing units in 5G radio base stations, and next generation data center multi-server blades. From the system point of view, TERABOARD develops a new technology that enables very large aggregated bandwidth density (Tb/s/cm²) onboard.

Photonic integrated circuits (PIC) main application is for intra-board and edge optical interfaces. For this purposes we report onboard electro-optical (EO) interfaces based on high density silicon-germanium (SiGe) modulators at 1550 nm at 25 Gb/s data rate, intra-rack SiGe modulators driven at 56 Gb/s and intra-data center Si-based modulators at 1300 nm operating at 56 Gb/s data rate, all for ultra-high density and scalable in bandwidth, with low insertion loss and low energy consumption toward a target of energy cost for onboard operation of 2.5 pJ/bit. The intra-board communication exploits a novel concept based on a 3D passive interconnection platform with no intersections and no need of wavelength division multiplexing (WDM). All input/output coupler arrays based on a pluggable SiO₂ platform are reported as well.

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A further objective in TERABOARD is to add laser integration through a development a transfer bonding of III-V coupons on the silicon platform. It requires the development of the transfer process itself, the preprocessing of lasers on III-V wafers, the adaptation of the silicon photonics platform for integration of lasers. The devices will be optimized for uncooled operation and low coupling losses.

2. REQUIREMENTS, ARCHITECTURES AND SPECIFICATIONS

Next generation hardware platforms for 5G and data center systems will have a much increased processing capacity reaching tens of Tb/s in a single unit^{1,2}. To achieve that not only the signal data rate must increase from currently used 25 Gb/s to 50 Gb/s but the bandwidth density and the energy efficiency must also increase. In such conditions the optical interconnect technology based on packaged ASICs surrounded by a number of low channel count optical engines has to be replaced by highly integrated and more scalable technologies, which are developed in TERABOARD.

Two illustrative implementations have been considered with different interconnect requirements: the first is related to a future high capacity baseband processing unit (BBU) of 5th generation (5G) networks while the second deals with a packet switch unit for intra-data center networking.

The baseband processing units for 5G radio base stations is shown in Figure 1a. Four baseband processor ASICs accomplish the complex processing of user and control data. The ASICs communicate each other and to the electrical switch via high speed optical links with 500 Gb/s capacity. Traffic is also received by several radio interfaces optically connected to external radio units and/or other baseband units with a total external interconnect capacity of 1 Tb/s. The switch routes radio traffic from the baseband processing ASICs to the different radio interfaces. It is used for communication among different baseband units and for backhaul communication. The link length for internal interconnects is < 1 m while that of external link is < 10 km.

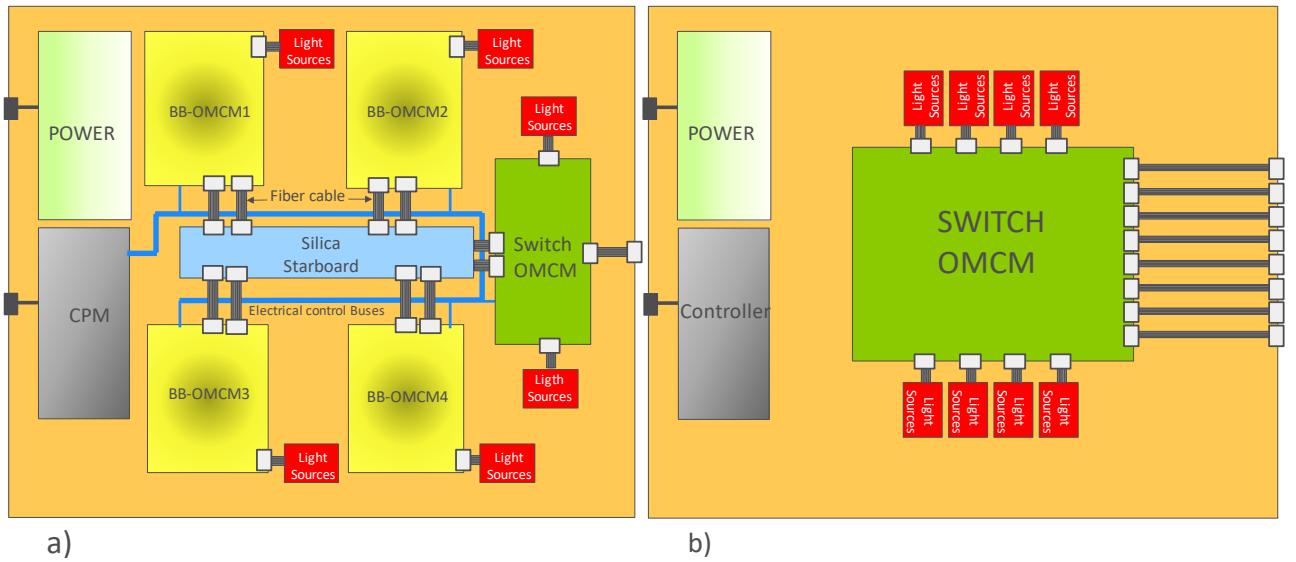


Figure 1. Schematic block diagrams of : a) a baseband processing unit (BBU) of a 5G radio base station and b) a packet switch unit for intra-data center networking.

The packet switch unit for intra-data center networking is shown in Figure 1b. Next generation electrical packet switch will have an aggregate switch capacity of 12.8 Tb/s (128 input and output ports at 50 Gb/s rate). Differently from the previous application, see fig1.a, in which a Terabit capacity is needed for both internal and external interconnect, here all the multi-Terabit bandwidth is used for external interconnects with a link length < 2 km. To meet the high demand of interconnect bandwidth density in the BBU and in the packet switch unit two key technologies are considered: optical multi-chip modules (OMCM) and a passive multilayer silica board to interconnect many OMCMs in the same card³, called Starboard, which is a key component in TERABOARD.

The OMCM includes, electrically connected by a multi-layer organic substrate, a high processing capacity electronic die in close proximity (< 2 cm) to a photonic integrated circuit (PIC) comprising a bank of high speed optical transceivers. The analog electronic integrated circuit (EIC) to drive the optical transceivers is 3D integrated on top of the PIC.

Through-silicon vias (TSV) are used to connect high speed electrical signals from the substrate through the PIC to the EIC and micro-bumps are used to connect EIC and PIC. The OMCM used for BBU is depicted in Figure 2a and it includes a high processing capacity ASIC and the PIC comprises forty optical transceivers at 50 Gb/s and its relative EIC. In Figure 2b the packet switch OMCM is shown with the 12.8 Tb/s switch chip surrounded by four PICs/EICs, each with 32 optical transceivers at 50 Gb/s. The carriers for the optical modulators are supplied to the OMCM by external optical sources: this simplifies the thermal management of the OMCM and allows to increase the maximum operating temperature of the module, since the lasers are highly sensitive at high operating temperatures ($>85^{\circ}\text{C}$) and both their performance and reliability can degrade.

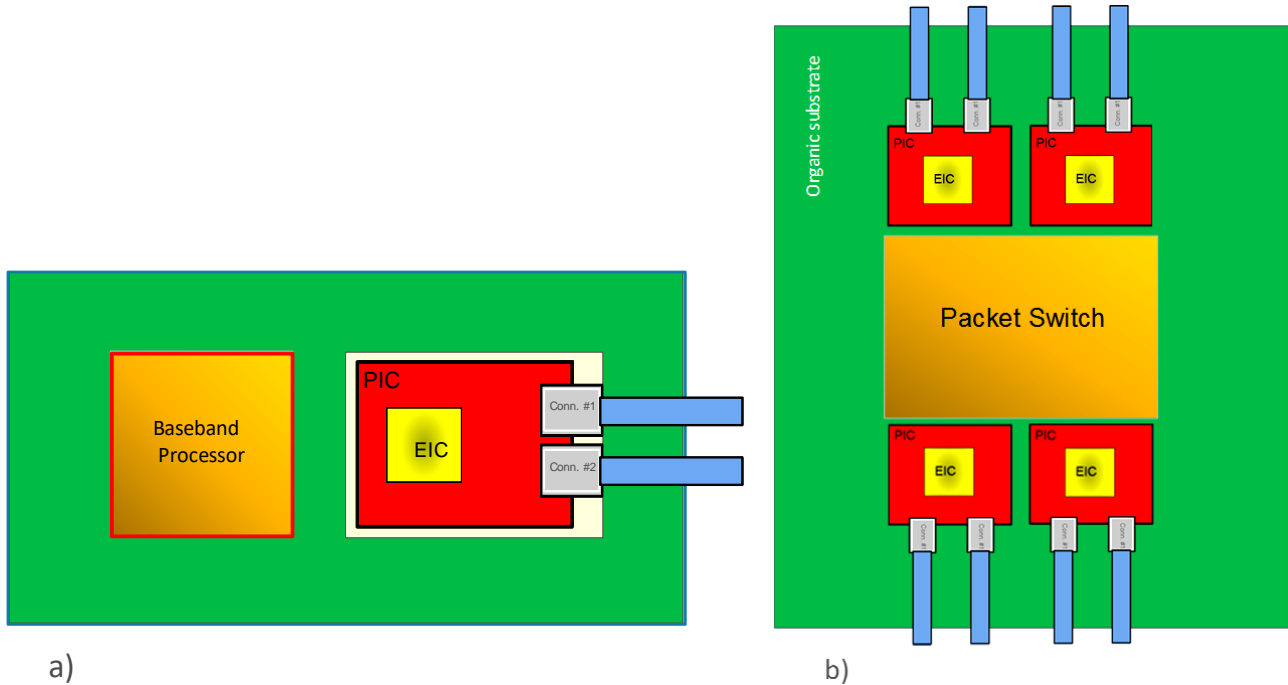


Figure 2. Optical multi-chip modules (OMCM) for: a) BBU and b) packet switch.

Connection between PIC and SM fiber arrays is pluggable. This is done on one end with a fixed part (called silica connector) mechanically attached to the organic substrate and optically connected to the PIC and on the other end by a removable part. The fixed part should be compatible with PCB soldering methods for ball grid array (BGA) devices based on soldering reflow processes consisting in keeping the OMCM in an oven for approximately 60 s at about 260°C . Alternatively, a single fixed coupling block including fiber array can be used. In this case the pluggability is achieved by including a MTP connector at the end of the fiber array.

The optical passive board, named 'silica Starboard' in Figure 1a, interconnects the different OMCMs on the BBU board. It comprises hundreds of low-loss optical connections made by optical waveguides routed horizontally in many layers with optical connection between layers through laser scribed vertical waveguides and micromirrors.

The loss requirements of the different blocks in the intra-board optical interconnect (BBU only) are set by the power budget at 50 Gb/s as for the scheme in Figure 3. It has been assumed to share the optical power of a single laser source for N optical modulators in order to reduce the cost and energy consumption. The optical carrier power coming from external distributed feedback (DFB) laser sources is coupled to the PIC by single polarization grating coupler (SPGC) arrays through short ribbon cables (<1 m) of polarization maintaining (PM) optical fibers and the optical connector. The connector is split into two parts, the fixed part is named 'glass coupler' and the movable part 'conn'. The optical power of each source is split into four channels and sent to the modulators before being coupled to the short output PM fiber cable of <10 cm length. The extinction ratio (ER) requirement for the optical modulator is 4 dB. The output coupler of the first transmitter is connected to Starboard that routes the signal to one of the ports. The output of Starboard is then connected with a connector to another PIC on the board for signal detection. This is done by using the same coupling

blocks used in the transmitter. The specifications of the energy consumption are set by the particular applications and the mechanics used for the hardware unit.

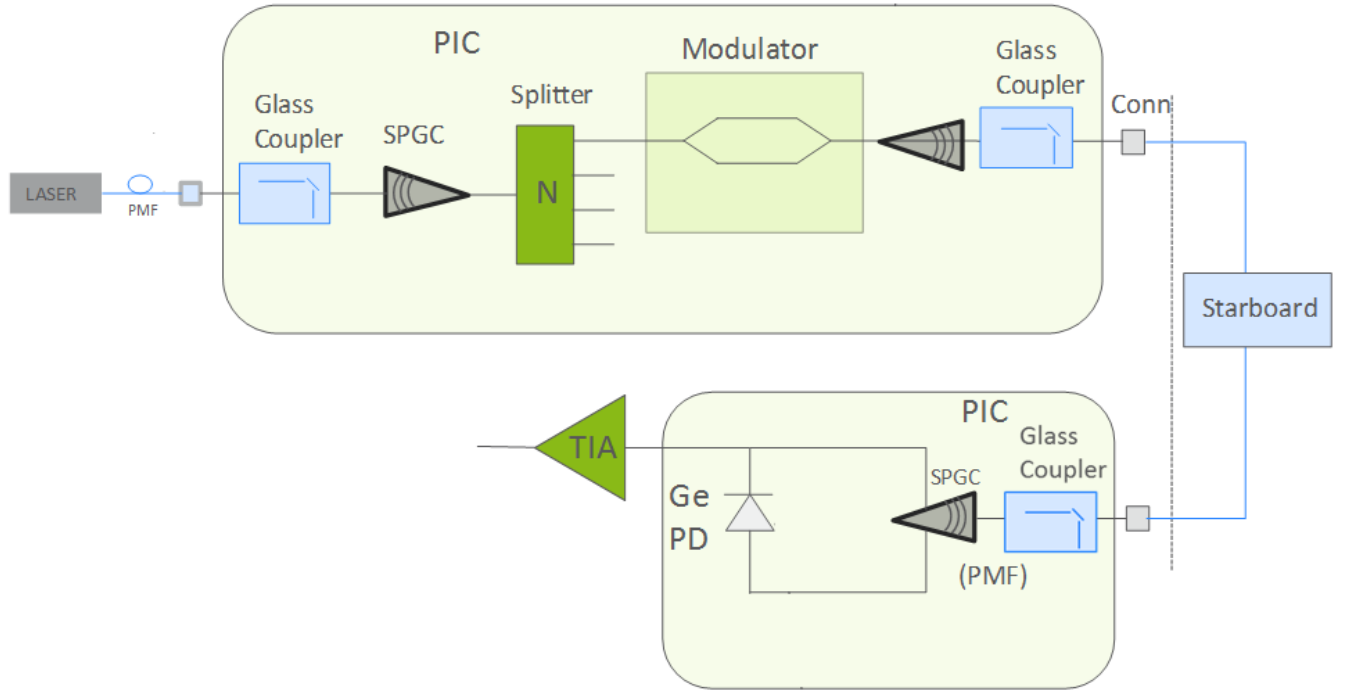


Figure 3. Typical example of scheme for internal interconnection links.

For the BBU presented in Figure 1a a maximum allowed power dissipation of 330 W has been assumed. Each of the five electronic chips dissipate 50 W thanks to the OMCM technology that allows a low loss chip-PIC electrical interconnect and additional power is dissipated by the common parts including power supply, controller, synchronization circuits etc.

The available room for optical interconnect is 30 W distributed as 20 W for the 100 internal interconnect links at 50 Gbps and 10 W for the 20 external links at 50 Gb/s (<10 Km). The resulting requirements for the energy consumption of the optical interconnect, including energy utilized by PIC and EIC, is <4 pJ/bit for the internal interconnects and <10 pJ/bit for the external interconnects.

3. PHOTONIC INTEGRATED CIRCUITS

In TERABOARD, silicon photonics interposer chips are fabricated on 200 mm silicon on insulator (SOI) wafers using a process based on imec's iSiPP50G 50 Gb/s silicon photonics platform⁵ and on 300 mm SOI wafers using imec's internal 300 mm development platform. These interposers contain photonic circuits based on passive and active photonic components in the 200 mm process. The 300 mm process extends these components with 10 μm x 100 μm TSVs for high-speed, low-parasitic interconnection to the package substrate.

3.1 Passive components

The passive components of the silicon photonics interposer chips included waveguides, directional couplers, multi-mode interference (MMI) splitters and fiber couplers. Components fabricated on 300 mm wafers benefited from the capabilities of deep UV (DUV) immersion lithography at a wavelength of 193 nm. This enabled the fabrication of very small features such as 100 nm gaps in directional couplers.

Fiber couplers were designed and fabricated for single wavelength operation in C-band (1550 nm) (Figure 4) and coarse wavelength demultiplexing (CWDM) operation in O-band at wavelengths spaced along a 20 nm grid (Figure 5). These designs included single polarization couplers for transmit circuits and polarization-diverse couplers for receiving circuits. Fabrication of these designs included shallow and intermediate etch depths in crystalline silicon as well as fully-etched patterns in a polycrystalline silicon overlay layer.

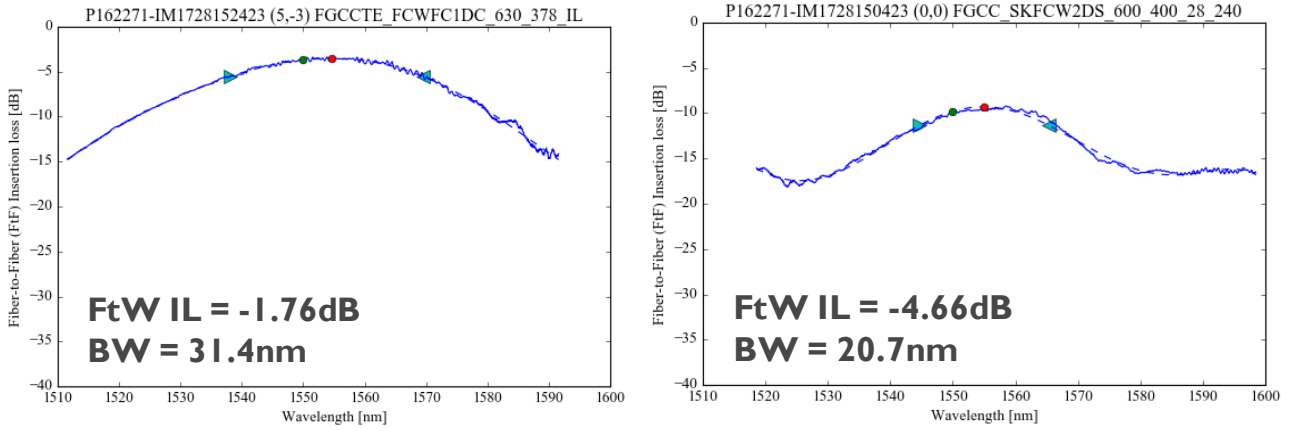


Figure 4. Single polarization (left) and polarization-diverse (right) fiber grating couplers for operating in C-band (FtW IL = fiber-to-waveguide insertion loss, BW = bandwidth).

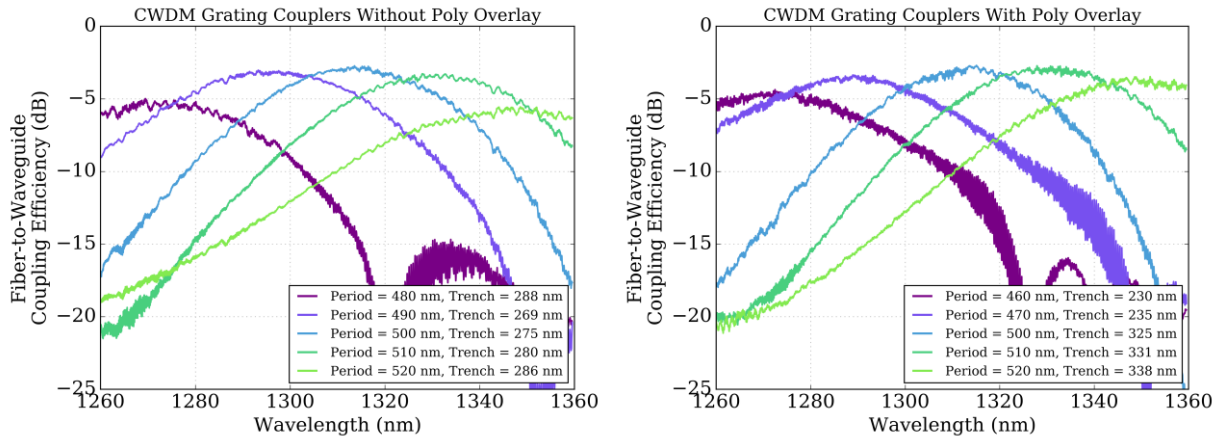


Figure 5. CWDM grating couplers fabricated without (left) and with (right) patterned polycrystalline silicon overlay layer.

3.2 Active Components

The active components of the silicon photonic interposers consisted of modulators and detectors. For C-band, electro-absorption modulators (EAMs) and photodiode detectors (PDs) were both fabricated using Si-doped germanium (Figure 6). Significantly, both the modulators and detectors were fabricated on the same wafer using a single epitaxial step. By changing the bias voltage of a given structure, its behavior could be changed from one to the other. The EAMs were driven with a peak-to-peak voltage of 2.5 V and the PDs were biased at -2.5 V. A test array of 16 channels was fabricated and back-to-back testing was performed with fiber coupling⁶. The EAM array showed a dynamic ER in the range of 2.7 dB to 3.3 dB. When combined with the PD array, the link signal-to-noise ratio (SNR) was in the range of 3.05 to 3.92. Furthermore, pseudorandom binary sequence (PRBS31) measurements verified open eyes for all channels at 56 Gb/s.

Whereas the GeSi PD can also be used for receiver circuits in O-band, a different modulator was required for the O-band transmitter circuits. In this case, a travelling wave Mach-Zehnder modulator (TWMZM) was chosen. This modulator was designed, fabricated and measured with a 2.5 V peak-to-peak drive voltage. An electro-optical S_{21} 3-dB bandwidth of 25 GHz was measured, indicating a Nyquist modulation rate of 50 Gbaud (Figure 7).

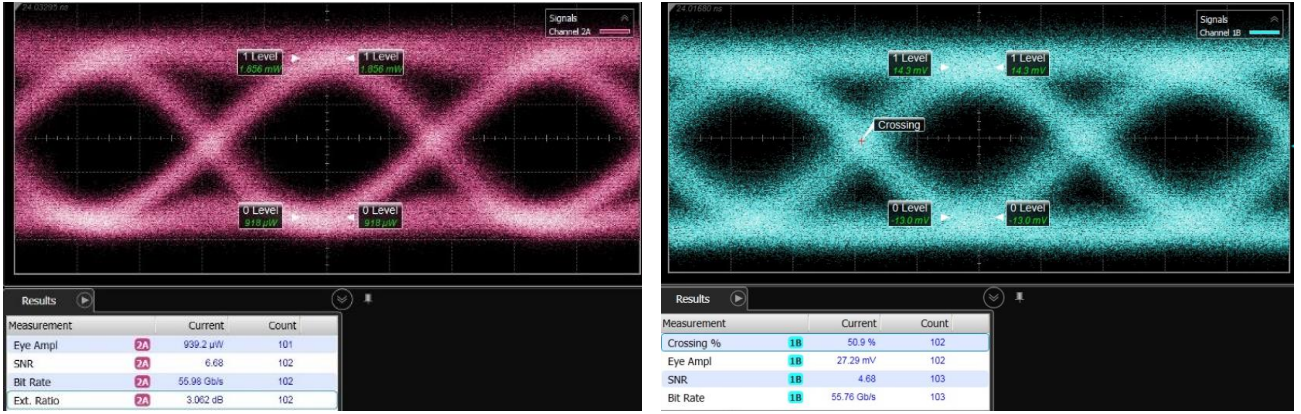


Figure 6. GeSi electro-absorption modulator (left) and waveguide photodiode detector (right) operating with open eyes at 56 Gb/s in C-band.

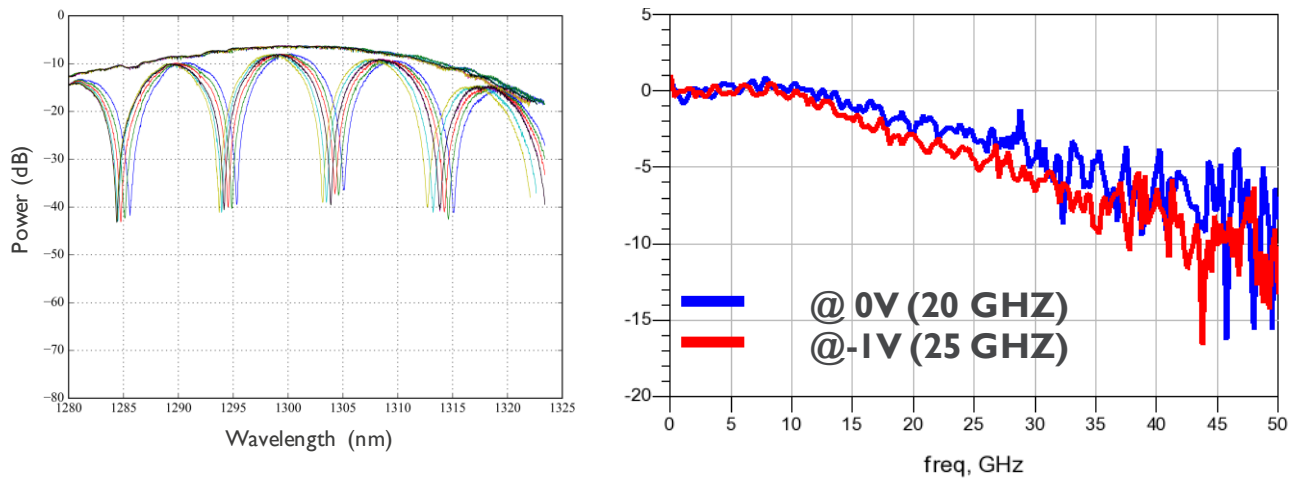


Figure 7. Si travelling wave Mach-Zehnder modulator (TWMZM) and reference grating coupler insertion loss spectra at bias voltages from -2 V to 0.5 V (left) and electro-optical modulation response with 25 GHz 3-dB bandwidth at a bias voltage of -1 V.

3.3 TSVs for 3D Integration

10 μ m x 100 μ m TSVs were fabricated using a TSV middle process on 300 mm SOI wafers. Void-free filling was achieved across entire wafers at TSV pitches of 20 μ m, 40 μ m and 60 μ m. Wafer thinning and TSV reveal were performed followed by backside passivation. Tests were then performed to determine the impact of the aforementioned processing on the photonic components. In particular, the impact of the TSV-induced stress, keep-out zone (KOZ) size and the thinned substrate on waveguide loss and grating coupler performance was measured. No significant change in waveguide loss was observed, and only a minimal impact to grating couplers with polycrystalline silicon overlay was measured.

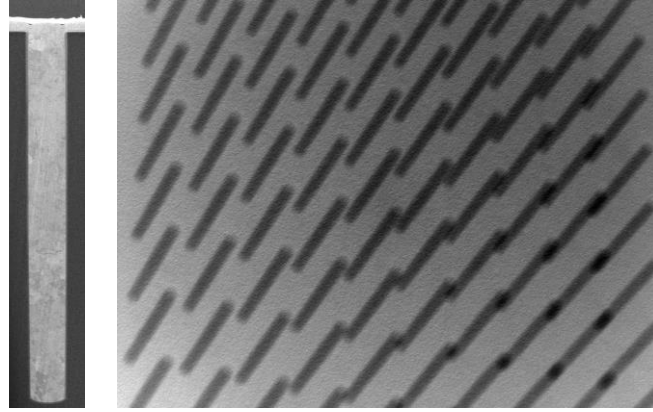


Figure 8. Cross-section scanning electron microscope (SEM) image of TSV showing void-free filling (left) and X-ray image of TSV array (right).

4. SILICA CONNECTING LEVELS

4.1 Silica interconnection devices

TERABOARD proposes an innovative approach to implement intra-node links by means of a device, named Starboard, which is a stack of several silica layers containing in the plane low index contrast SM integrated optics waveguides and vertical SM optical vias fabricated using femtosecond laser technology. The horizontal and vertical waveguides are coupled by integrated micromirrors. The combination of these three building blocks allows for a low loss horizontal propagation inside the layers of Starboard and a vertical interconnection between them.

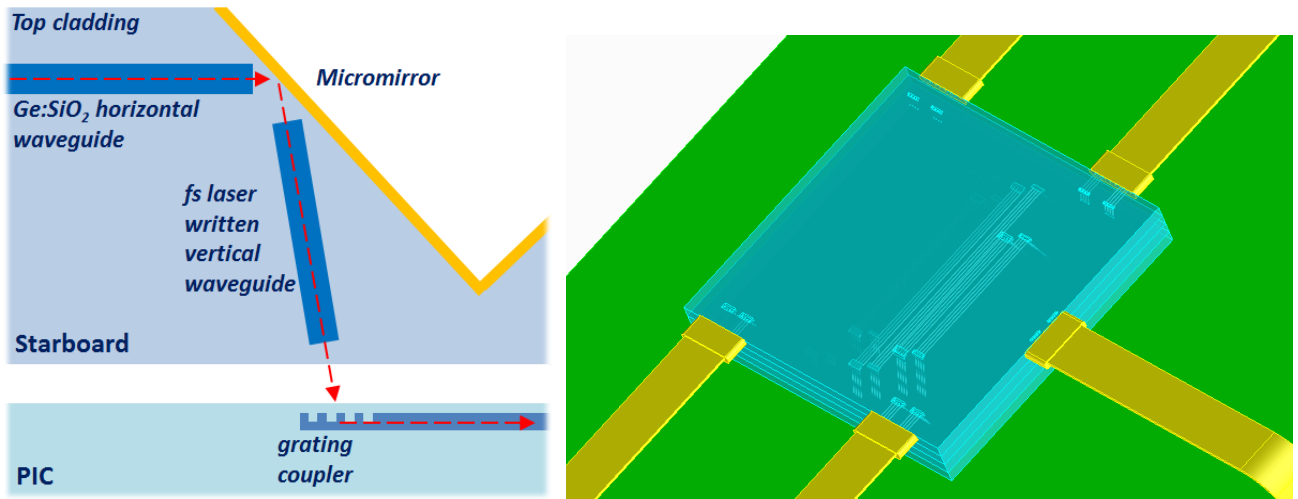


Figure 9. Left panel: a section of a layer of Starboard which is directly couplet to a PIC. Right panel: standalone Starboard with fiber ribbons for the interconnection of contiguous PICs.

Light can be coupled to Starboard to the edges or to the vertical waveguides at the bottom or top surface of the stack of layers. Starboard provides the possibility of connecting a large number of nodes to each other overcoming waveguide intersections and without resorting to WDM. In this way low loss and scalable solution is more easily achievable. Starboard can be used for the interconnection between PICs in two different ways. The first method consists in coupling the vertical waveguides of Starboard directly to the grating couplers of contiguous PICs. This approach is detailed in the left panel of Figure 9, in which a fs written vertical waveguide of a layer of Starboard is coupled to a grating coupler of a PIC. The angle of the vertical waveguides is designed in order to match the best coupling angle of the input/output grating couplers of the PIC. This coupling approach is highly compact, but presents some challenges in terms of thermal management of the consequent assembly. This issue is overcome by a second coupling method, illustrated in the right panel of Figure 9, that consists in using Starboard in a standalone configuration, with PM optical fiber ribbons coupled

between horizontal waveguides of Starboard and grating couplers of the PICs. The compactness of the system is still preserved since all the optical crossings are implemented inside Starboard, with low optical losses. In addition, Starboard can be placed anywhere in the package, thus making precious real estate available for other components or electrical routing paths.

The same technology of Starboard can be used to implement an optical connector to interface a PIC with an array of SM optical fibers. In this configuration the vertical waveguides are coupled directly to the grating couplers of the PIC and the horizontal waveguides are coupled to an array of SM optical fibers. The connector is a key component for the inter-board, inter-rack and inter-data center optical links. Starboard and connector require the development of same three building blocks: horizontal optical waveguides, micromirrors and vertical optical vias. The fabrication technology for these building blocks is described in the following paragraphs.

4.2 Horizontal waveguides

Ge:SiO₂ waveguides are a well-established technology for the fabrication of SM waveguides⁷. Index contrasts between 0.5% and 2.5% were achieved by varying the Ge content of the fiber core. The Ge:SiO₂ core was achieved by mixing GeH₄ and SiH₄ precursors in a Plasma Enhanced Chemical Vapor Deposition (PECVD). While PECVD Ge:SiO₂ fibers are commonly fabricated on silica-coated silicon wafer substrate, innovative Ge-doped waveguides fabricated on bulk silica wafers are proposed. A bulk glass-based substrate is required in order to enable the fabrication of vertical vias. However, deposition of PECVD layer on silica substrates poses a technological challenge because of the lower Young modulus ($E \cong 180$ GPa) and coefficient of thermal expansion ($CTE = 2 \cdot 10^{-6}$ K⁻¹) of silica with respect to that of silicon ($E = 80$ GPa; $CTE = 5 \cdot 10^{-5}$ K⁻¹). Silica wafers substrates required the development and implementation of several ad-hoc technological solutions. A high-temperature (1050°C) annealing and a low-roughness lithographic and etching techniques were implemented in order to reduce propagation losses in the PECVD-fabricated layers. The core thickness was 4.7 μm by design and required an overcladding of 10 μm or more. The material used for the overcladding was an engineered Boron and Phosphorous-doped Tetraethylorthosilicate (BPTEOS) layer deposited by PECVD.

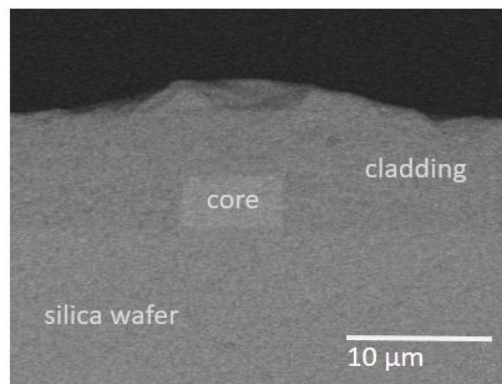


Figure 10. Ge:SiO₂ waveguide cross-section.

Figure 10 shows the cross-section of a silica waveguide fabricated with an optimized BPTEOS layer, after annealing. The BPTEOS layer also achieved partial planarization of the surface, which is desirable for the subsequent fabrication steps. The waveguide propagation loss was measured to be lower than 0.05 dB/cm.

4.3 Micromirrors

Micromirrors are implemented in order to couple the signal coming from the horizontal waveguide into the vertical optically-induced vertical waveguide (optical via). The coupling between the horizontal waveguide and the vertical via is carried out after the reflection on an integrated micromirror, whose angle is set by design. The horizontal and vertical waveguides are both weakly guiding, therefore coupling losses are strongly dependent on the coupling angle, which is determined by the angles of mirror and the optical via with respect to the horizontal waveguide. Simulations, carried out assuming that the angle between the horizontal and the vertical waveguide is set to its nominal value, show that a mirror angle with an accuracy of 0.25° or better is required in order to achieve a coupling loss below 0.15 dB;. A technique using a mechanically-etched V-shaped groove was implemented to fabricate the integrated turning mirror. This technique has the advantage of not requiring lithography or plasma etching, with the tradeoff of a reduced accuracy in

the positioning of the groove as opposed to advanced lithographic approaches. The design is more tolerant to in-plane alignment accuracy than to mirror angle, therefore this approach was suitable for this application. The mirror was fabricated by scoring the wafer surface with a custom dicing blade with a V-shaped edge. Micron-level positioning accuracy as well as $< 0.3^\circ$ accuracy on the resulting angle could be achieved and consistently demonstrated. However, the rough as-cut surface of the V-groove had to be smoothed with an additional PECVD-deposited layer in order to obtain a mirror-like planar surface. The effect of this additional processing step is shown in Figure 11.

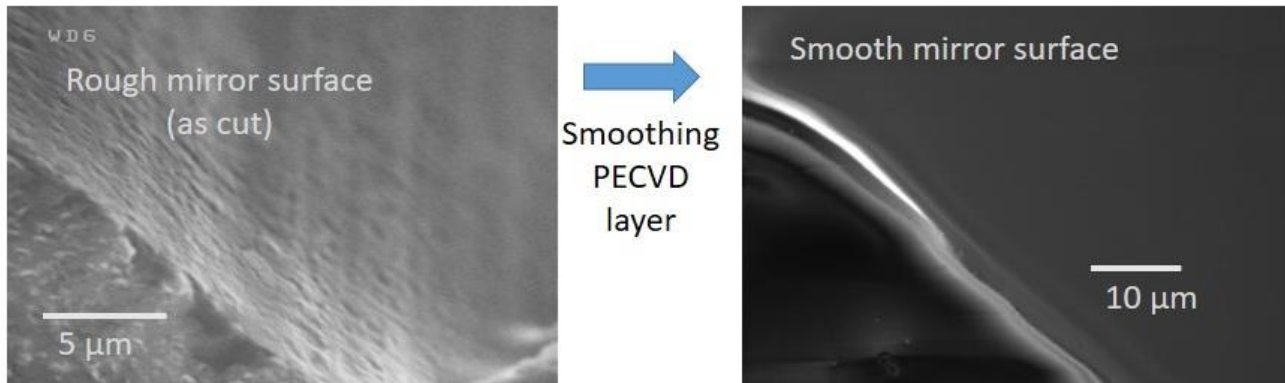


Figure 11. Detail of the V-groove mirror surface.

4.4 Vertical optical vias

For the fabrication of the vertical optical vias that will connect different silica layers femtosecond laser waveguide writing^{8,9} was exploited. The longitudinal irradiation geometry was used, where the waveguide is fabricated parallel to the direction of the writing laser beam, in order to create vertical optical waveguides perfectly aligned with the horizontal waveguides and turning mirrors. The longitudinal fabrication geometry is less commonly used in waveguide writing due to its limitations: the fabrication depth is limited by the working distance of the objective and the modification profile is highly dependent on the writing depth due to spherical aberrations¹⁰. Still, it provides naturally a symmetrical modification, and for writing vertical waveguides it enables fabrication in any position on the sample.

A Satsuma fiber laser (Amplitude Inc.) was employed, with 1030 nm wavelength, 210 fs pulse duration at a repetition rate of 1 kHz. The laser beam is focused by a long working distance (2.6 mm), 20× (0.5 NA) water-immersion objective to reduce spherical aberration. Waveguides with a refractive index contrast high enough for SM waveguiding at 1550 nm were fabricated. With the fs laser the depressed cladding of the waveguides is created moving the sample in an helical trajectory with the axis along the vertical direction. The waveguiding at 1550 nm occurs in the central, non-irradiated region that is surrounded by the irradiated material.

As it is reported in Figure 12a the waveguides present a “doughnut” profile, and guiding takes places in the central region embedded inside the irradiated ring, The profile of the optical guided mode at 1550 nm is quite symmetrical and has a full waist around 7.5 μm (see Figure 12b). The length of the waveguides is about 800 μm, that is the thickness of the quartz wafer. Insertion losses of the vertical waveguides as low as 0.6 dB were observed when coupled to optical fibers.

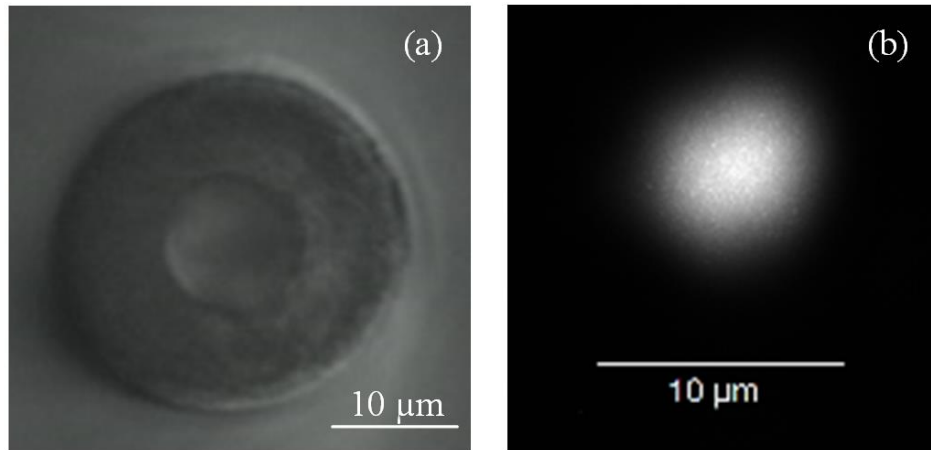


Figure 12. Panel a: detail of a waveguide which presents a “doughnut” profile. Panel b: profile of the optical guided mode at 1550nm

5. ELECTRONIC INTEGRATED CIRCUITS

High-speed optical transceivers require compact, multi-channel and low-power electronic driver and transimpedance amplifier (TIA) chips. Custom developments and co-design of photonic and electronic circuits are needed to achieve the very high bit rates for tomorrow’s optical interconnects. For this purpose, the design and simulation of optical transmitter and receiver front-ends need to include accurate models for the electronic circuits, the on-chip and off-chip interconnects, the electrical parasitics of the photonic devices, and the electro-optic response of the photonic devices. As such, the electronics design plays a very important role as, in the end, the electronic circuitry will largely determine the system performance (power consumption, bandwidth, sensitivity, signal quality...) for the given photonic devices and the required optical budget. In the following subsections the ongoing driver and TIA array developments in TERABOARD are introduced. Considering the very high bit rates, low-power analog equalization circuits are also key functions in the driver and receiver chips, whereas clock-and-data-recovery is outside the scope of the project.

5.1 Electro-absorption modulator driver array

The driver chip converts the incoming non-return to zero (NRZ) digital data signal into an appropriate voltage signal for the EAM. The EAM drive signal has a 2 V_{pp} amplitude and it is superimposed on a certain bias voltage to optimize the operating point of the modulator. The driver-EAM interface and all circuits in the datapath are DC-coupled for multi-rate operation (e.g. 28 or 56 Gb/s) and for avoiding low-frequency droop during identical consecutive digits. The driver circuit is designed such that the resulting optical waveform is an accurate representation of the digital data. Realizing such high-quality optical modulated waveforms is one of the main challenges of driver design, despite the E/O transfer function of the laser/modulator and the parasitics of the electrical interface between driver and laser/modulator. Analog equalization is introduced to enhance the signal quality of the incoming data waveform and to enlarge the bandwidth of the driver output stage. The EAM driver array features 4 channels, including on-chip EAM biasing (no external bias-tees needed). It is digitally reconfigurable via a Serial Peripheral Interface (SPI) to e.g. alter the bias voltage, modulation voltage, or equalizer coefficients. The driver test chip is currently being fabricated in a SiGe bipolar complementary metal oxide semiconductor (BiCMOS) process and the power consumption is expected to be around 1 pJ/bit.

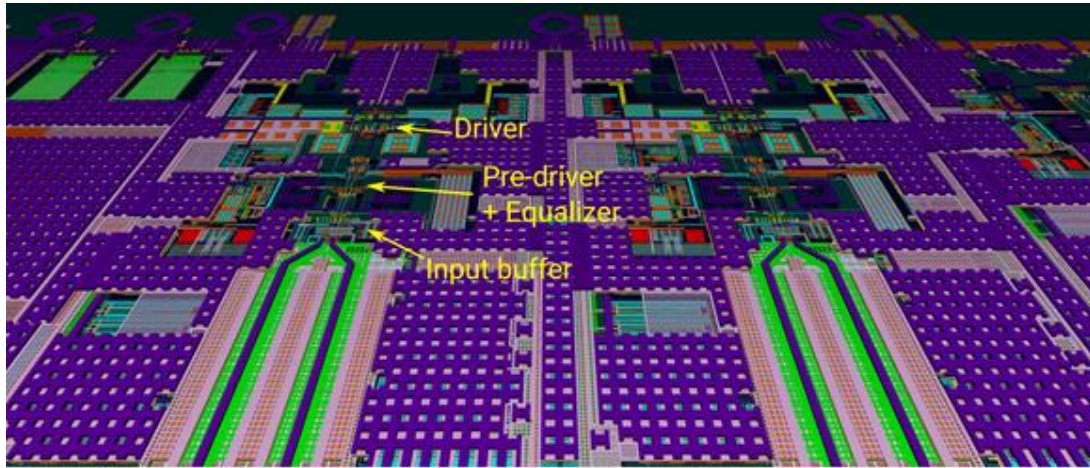


Figure 13. EAM driver array layout (data inputs at bottom, EAM outputs at top).

5.2 Transimpedance amplifier

At the end of the optical interconnect, the receiver must be capable of reconstructing the digital data from the optical waveform. As the received optical signal is typically weak due to losses in the optical interfaces (and in the optical modulator), a low-noise TIA is needed to convert the weak photodiode current into a voltage waveform which is strong enough for further processing. In this conversion process, a lot of challenges reside as the input signal strength is not known (it can be weak or relatively strong), while the input signal can be distorted by a low ER, jitter or inter symbol interference. As such the TIA circuits needs to adapt to the incoming optical signal (gain control, offset compensation), while providing sufficient bandwidth (around 40 GHz), low group delay variation and stable operation over the dynamic range. It is clear the TIA design involves many challenges and trade-offs, and as consequence, the power consumption heavily depends on the requirements (input signal, bandwidth, sensitivity, dynamic range, output voltage).

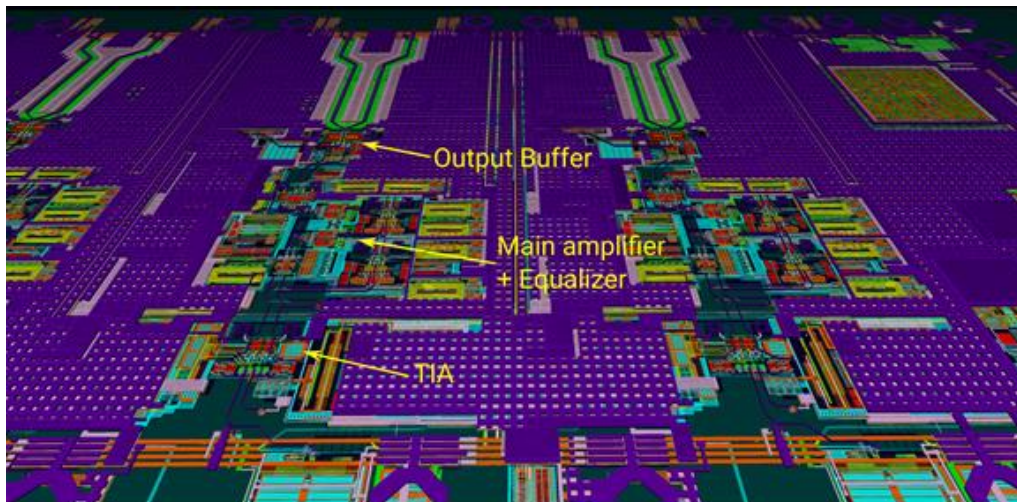


Figure 14. TIA array layout (input at bottom, TIA output at top).

Similar to the driver, the TIA array features 4 channels, including PD biasing, offset compensation, gain control, and it is also digitally reconfigurable via SPI. The TIA test chip is currently being fabricated in a SiGe BiCMOS process and the power consumption is expected to be around 1.5pJ/bit including postamplifier and 50 Ohm output buffer for testing.

6. LASER INTEGRATION

To achieve laser integration in TERABOARD, the lasers are pre-processed on their native III-V substrate, transfer printed¹¹ onto the target SOI and then post processed to add the metal tracks. For the purpose of this work, the transfer printing takes place in a trench etched in the buried oxide of the photonic chip, as shown in Figure 15. The thickness of the n InP puts the quantum wells to the same height as the silicon on the SOI side.

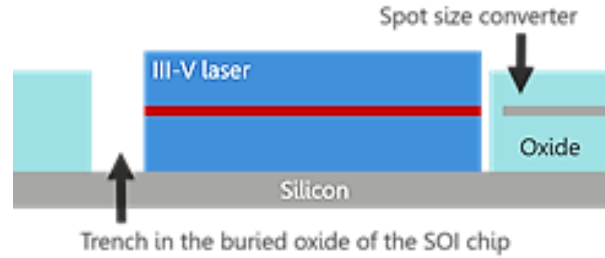


Figure 15. The laser coupon is transfer printed into a trench in the buried oxide of the photonic chip. Direct bonding to the silicon substrate improves heat dissipation. The light output is edge-coupled into a spot-size converter on the SOI side.

The pre-processing of the lasers includes the dry etch of the main mesa and the III-V waveguide below the quantum wells, followed by a PECVD deposition of nitride to protect the exposed quantum wells laterally. The dry etch is then continued until the release layer is reached. Next, the release layer is patterned and etched around the coupons, leaving pedestals atop of which the coupons rest. The n contacts are then deposited on both sides of the III-V waveguide. Finally, the coupons are encapsulated with photoresist and released by undercutting the release layer with a very selective wet etch. Figure 16 shows a top down view of the front and back sides of a coupon right before the release etch, as well as a schematic cross section of the structure.

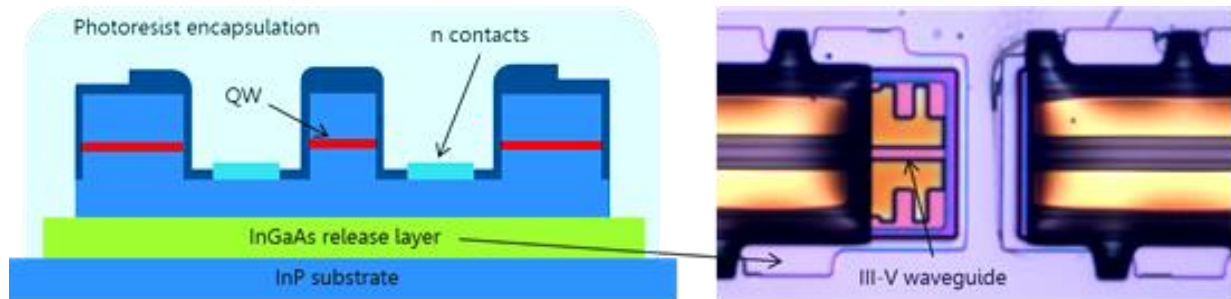


Figure 16. Left panel: cross section of the coupon before the release etch. The twin inner trenches inside the mesa define the III-V waveguide and provide a platform to deposit the n contacts. The release layer will be etched from underneath the coupon, leaving the coupon ready for transfer printing. Right panel: top-down view of the coupon before the release etch.

The coupons are transfer printed with sub-micron accuracy into the trenches of the photonic chip. The mean lateral misalignment is 400 nm with a standard deviation of 400 nm, whereas the mean longitudinal misalignment (distance between the laser facet and the spot-size converter) is 800 nm with a standard deviation of 130 nm. The mean misalignments can be corrected in subsequent printings by adjusting the center of the patterns set up in the pattern recognition software used to automatically align the coupons during printing.

After transfer printing, the chip is passivated with benzocyclobutene and vias are opened to access the top of the III-V waveguide and the n contacts. Finally, the metal tracks are deposited.

The output of the transfer printed coupons is successfully coupled into the spot-size converter and waveguide and the signal is measured through a grating coupler. Figure 17 shows the signal measured at the grating coupler.

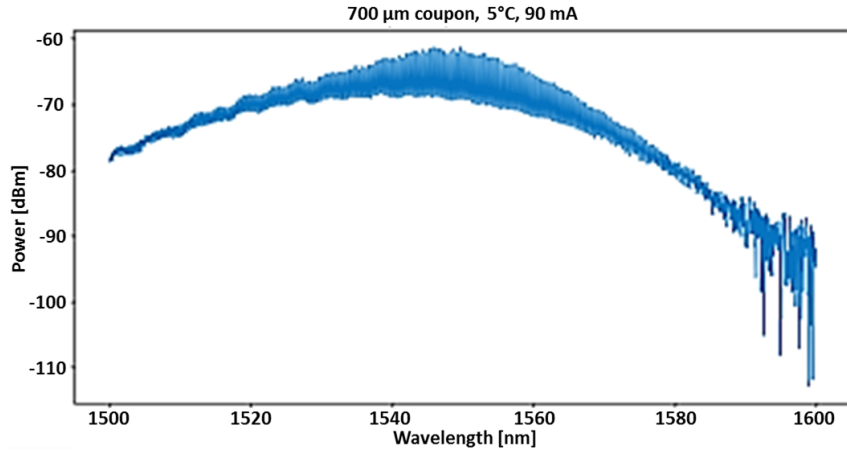


Figure 17. Signal coupled from the III-V coupon into the photonic circuit, as measured at the output grating coupler. The free spectral range of 0.5 nm is compatible with the length of the coupon (700 μm).

7. ASSEMBLY AND INTEGRATION

In TERABOARD, the most critical part of the 3D assembling and packaging regards the fabrication of the micro Tx/Rx arrays. Their structure, shown in Figure 18, is composed by the PIC with TSVs, the EIC bonded on top of it via copper pillars, and an organic substrate supporting both, to let them be easily handled. This structure was simulated to study the interactions between the silicon interposer die (PIC + EIC) and the organic substrate, after the interposer bottom die attach and the under fill (UF) curing at 150°C of the PIC on the substrate, and after the last 3D EIC attach and UF cure on the PIC. The scope of simulations was to evaluate the main regions of stress and package warpage during and after the assembly process.

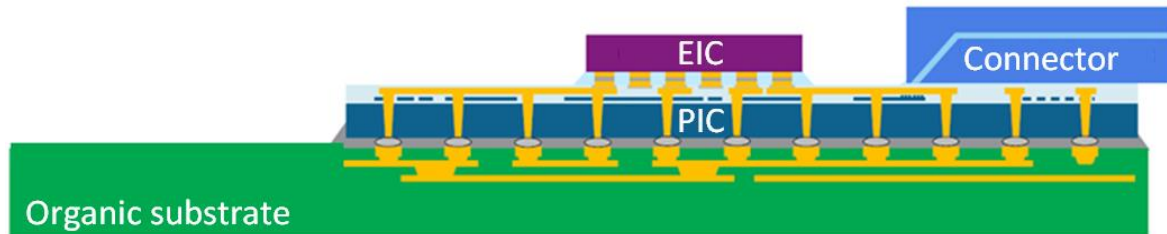


Figure 18. Assembly scheme of Tx/Rx with TSVs.

The final version of Tx/Rx with TSVs, which have to demonstrate the minimum power consumption of 2.5 pJ/bit for transmission at 56 Gb/s, as well as the minimum size, will be according to Figure 18. As a first step the top surface of the thick PIC wafers with TSV will be populated of copper pillars, then the wafer will be thinned to 100 μm and populated with the under-bump metallization (UBM) contacts on the bottom of the wafer. The thinned PIC will be soldered on a properly designed organic substrate. The EIC will be finally bonded via copper pillars onto the PIC.

7.1 Micro Tx/Rx integration on Starboard

For the integration of Starboard, two approaches are possible and are under evaluation from the process point of view. The first option is illustrated in Figure 19.

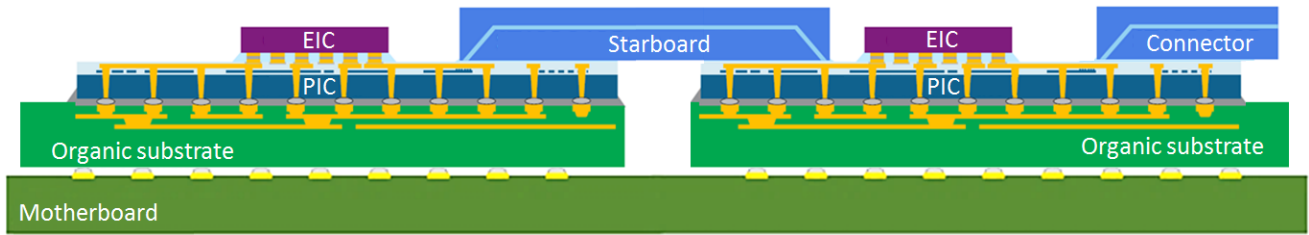


Figure 19. Single Starboard integration.

In this approach Starboard directly connects the two Tx/Rx. In terms of process development this approach is quite challenging because of all the constraints related to the overall dimensions and the necessity of micron level tolerances for the flip-chipping of the parts. Specifically, the flip-chip of each Tx/Rx over Starboard has to be performed, with Starboard which can be seen as a substrate. After each Tx/Rx is flip-chipped onto Starboard then such subassembly will be integrated on the motherboard. Given the high complexity and risks of this approach, an alternative solution was developed, it is shown in Figure 20.

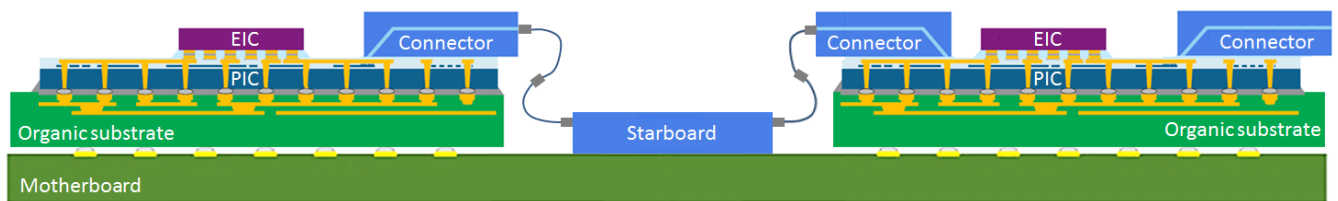


Figure 19. Multiple Starboard integration and ribbons.

In this case the basic idea is to use two connectors to be later interconnected with Starboard using ribbon fiber arrays. This approach is expected to be optimum in terms of stability and thermal dilatations issues. Moreover it simplifies the overall packaging of the system because a smaller connector is flip-chipped on the Tx/Rx in a more conventional way.

The alignment and the pigtailing by ribbon fiber arrays of the output side of connectors and Starboard will be done by traditional techniques.

8. CONCLUSIONS

Towards the 3D passive interconnection platform and the concept demonstration of silicon photonic chip pluggability, in TERABOARD, an innovative technology for the fabrication of low loss femtosecond laser written vertical waveguides was developed, together with reliable methods for the fabrication of micromirrors and low loss horizontal waveguides in bulk silica wafers. Important progresses have been accomplished on laser integration over the silicon photonic chips by means of transfer printing. Silicon photonics components efficiently operating up to 56 Gb/s were developed. Specific driver and TIA electronic integrated circuits have been designed with target specific consumption of 1pJ/bit and 1.5 pJ/bit. Finally the multi chip module (MCM) will be assembled. The arrays of micro Tx and Rx interfaces will be assembled at the edge of the high bandwidths electronic units to convert the signal from all electrical ports into optical signals through the EO interfaces.

The proposed 3D interconnection technology will support radically new data center architectures requiring a reduced number of boards and backplanes, consequently reducing the overall data center size and cost. These targets, once reached, will pave the way to Pb/s networks, enabled by scalable multi-Tb/s board interfaces for optical intra-data center transmission.

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