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Structure Based Compact Model for Output Capacitance of Trench Field-Plate MOSFET to Enable Power Loss Prediction

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Abstract

We propose a structure based compact model for output capacitance (C_{oss}) of trench Field-Plate MOSFET. Appropriate equations were considered for C_{oss} curves in three regions. Output charge (Q_{oss}) and stored energy (E_{oss}) that were calculated by the proposed model corresponded very well to TCAD results. In assumption of 10 A and 2 MHz operation, conduction loss of 1.0 W and output charge loss of 1.26 W were estimated.

1. Introduction

Various power devices contribute to reduce energy consumption in current electronics society. Among those, low-voltage power MOSFETs market are still growing. Especially, trench gate Field-Plate MOSFETs (FP-MOSFETs) have been applied in wide voltage ranged circuits from 12 to 250 V [1]-[2]. General power loss in power converters is given by the following components; the conduction loss (P_{CON}), the switching loss (P_{SW}), the gate drive loss (P_{GD}) and the output charge loss (P_{Qoss}) [3]. The FP-MOSFET which has ultra-low specific on-resistance ($R_{ON}A$) and gate-drain charge (Q_{gd}) can reduce the P_{CON} and the P_{SW} drastically. However, due to the featured device structure, the output capacitance (C_{oss}) which leads to the P_{Qoss}, especially in case of MHz switching, is significant issue compared to old-fashioned planar gate double-diffused MOSFET (D-MOSFET) and trench gate MOSFET.

In this paper, we propose a structure based compact model for the C_{oss}. The proposed model can be described by structural parameters such as device dimensions and impurity concentration, it does not need any measurement of the electrical characteristics. In this model, we considered the components of the C_{oss} in detail. It enables the power loss prediction of next generation FP-MOSFET.

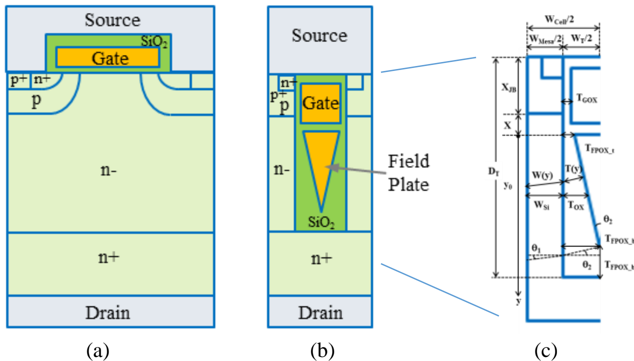


Fig. 1. Cross sectional device structures of (a) conventional D-MOSFET and (b) gradient FP-MOSFET. (c) Structural parameters of FP-MOSFET (half-cell structure) to describe capacitance model.

2. Device parameters and basic characteristics

In this study, we chose 100 V rating MOSFET as a motive device which applied to e.g. high performance server. As shown in Figs. 1(a) and 1(b), unit cell width (W_{Cell}) of the gradient FP-MOSFET, which is recognized current ideal FP structure [2], [4], can be narrower than that of D-MOSFET due to FP effect in the drift layer with maintaining sufficient breakdown voltage (V_B). Moreover, it can make drift layer concentration (N_D) ten times higher than conventional one as shown in Table I. Therefore, ultra-low $R_{ON}A$ can be achieved in the FP-MOSFET and it is approximately one-sixth of that of the D-MOSFET as simulated by TCAD (Table II).

Fig. 2(a) shows the drain voltage dependence of parasitic capacitances which are the input capacitance (C_{iss}), the reverse transfer capacitance (C_{rss}) and the C_{oss}. In the FP-MOSFET, the field plate connects to the source electrode, thus the C_{oss} includes two drain-source capacitance components (C_{ds1}, C_{ds2}) and gate-drain capacitance (C_{gd}). The C_{oss} is expressed as

$$C_{oss} = C_{ds1} + C_{ds2} + C_{gd}. \quad (1)$$

As an approach for the C_{oss} modeling in this complicated structure, we consider the capacitance curves divided to three regions shown in Figs. 2(a) and 2(b). Region (i), V_{ds} = 0~30 V, indicates depletion layer capacitance of plane pn-junction (C_j). Region (ii), V_{ds} = 0~60 V, includes FP-oxide capacitance (C_{OX}) and depleted mesa region capacitance (C_{Dep}) along the trench. In region (iii), V_{ds} = 60~100 V, trench bottom capacitance is added.

Table I. Structural parameters for D-MOSFET and FP-MOSFET.

Parameters		Symbol (unit)	D-MOSFET	FP-MOSFET
Drift layer concentration		N_D (atoms/cm^3)	2.8×10^{15}	3.0×10^{16}
Cell width		W_{Cell} (μm)	6.0	2.6
Gate width		W_G (μm)	3.4	N/A
Trench width		W_T (μm)	N/A	1.5
Trench depth		D_T (μm)	N/A	6.0
Gate oxide thickness		T_{GOX} (μm)	0.05	0.05
Field-plate oxide thickness	(top)	T_{FPOX_t} (μm)	N/A	0.1
	(bottom)	T_{FPOX_b} (μm)	N/A	075
P-base junction depth		X_{JB} (μm)	0.75	0.9

Table II. TCAD simulated static characteristics.

Characteristics	Symbol (unit)	D-MOSFET	FP-MOSFET
Breakdown voltage	V_B (V)	111.3	110.1
Threshold voltage	V_{TH} (V)	2.09	2.03
On-resistance	$R_{ON}A$ (mΩ.mm^2)	199.1	32.8

3. Description of compact model for C_{oss}

Junction capacitance ($C_{ds1} = C_j$)

In region (i), the depletion layer of the pn-junction extends down to vertical direction of the drift layer as increasing V_{ds}. The C_j is divided to C_{j0} and C_{j1}, those are given by

$$C_{j0} = \sqrt{\frac{qN_D\varepsilon_{Si}\varepsilon_0}{2(V_{ds}+V_{bi})}} \cdot \frac{W_{Mesa}}{W_{Cell}}, \ V_{ds} < 1, \quad (2)$$

$$C_{j1} = \frac{\varepsilon_{Si}\varepsilon_0}{y_0+X} \cdot \frac{W_{Mesa}-2W(V,y)}{W_{Cell}}, \ V_{ds} \geq 1, \quad (3)$$

where q is elementary charge, $\varepsilon_{Si}\varepsilon_0$ is permittivity of silicon, V_{bi} is built-in potential and other parameters are shown in Fig. 1(c) and Table I. *W(V,y)* is a depletion layer width in the mesa region along the sloping FP, and given by

$$W(V,y) = -\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y) + \sqrt{\left(\frac{\varepsilon_{Si}\cos\theta_1}{\varepsilon_{OX}\cos\theta_2} \cdot T(y)\right)^2 + \frac{2\varepsilon_{Si}\varepsilon_0}{qN_D} \cdot V_{ds}}, \quad (4)$$

where $\varepsilon_{OX}\varepsilon_0$ is permittivity of oxide. *W(V,y)* varies depending on T_{FPOX} and depletion layer depth of center of the mesa (y_0).

FP-oxide and depletion capacitance along the trench (C_{ds2})

In region (ii), when the V_{ds} is less than 1 V, initial value of the C_{ds2} nearly equals to the C_{OX} which is given by

$$C_{OX} = \frac{2\left(D_T-(X_{JB}+X+T_{FPOX_b})\right)\varepsilon_{OX}\varepsilon_0}{W_{Cell}(T_{FPOX_b}-T_{FPOX_t})} \cdot \ln\frac{T_{FPOX_b}}{T_{FPOX_t}}, \ V_{ds} < 1. \quad (5)$$

As can be seen in Fig. 2(b), the mesa region is depleted gradually in lateral direction by the FP effect and is linearly depleted in vertical direction because of the electric field uniformity [1]. Differential equation of *W(V,y)* expresses a voltage change of the electric charge in the region (ii). Therefore, the capacitance including the C_{OX} and the C_{Dep} is provided by

$$C(V) = \frac{2\cdot\int_{y_0}^{y_b} qN_D\frac{d}{dV}(W(V,y))dy}{W_{Cell}}, \ V_{ds} \geq 1. \quad (6)$$

Trench bottom capacitance (C_{ds3})

When the V_{ds} becomes approximately 60 V, the y0 reaches the almost same depth of bottom of the FP. For $V_{ds} >$ 60 V, the C_{ds2} decreases continuously in this model, therefore the trench bottom capacitance C_{ds3} has to add to total capacitance. This value is calculated as 3.3 nF/cm^2.

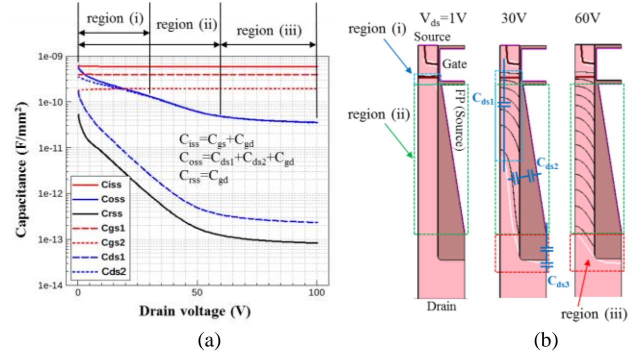
As a result, total C_{oss} is expressed by Eqs. (2), (3), (5) and (6) and the C_{ds3}. We confirmed that the C_{oss} model showed good agreement with simulated C_{oss} by TCAD (Fig. 3).

4. Validation and application of proposed model

By using the proposed model, output charge Q_{oss} and stored energy E_{oss} in the output capacitance are calculated as

$$Q_{oss} = \int C_{oss}dV, \quad (7) \qquad E_{oss} = \int C_{oss}V_{ds}dV. \quad (8)$$

The V_{ds} dependence of both the Q_{oss} and the E_{oss} are corresponded very well to TCAD results (Fig. 4). The capacitance of the D-MOSFET was modelled by similar manner of section 3. When products are designed for same R_{ON} = 10 mΩ, a die size of the FP-MOSFET is one-sixth of that of the D-MOSFET, as mentioned in section 2. In case of 50 V supply voltage, figure-of-merit (FOM) of $R_{ON}\cdot E_{oss}$ improves by 25 %. Assuming 10 A and 100 kHz to 2 MHz operation, main power losses were estimated as Fig. 5, e.g. P_{CON} = 1.0 W and P_{Qoss} = 1.26 W at 2 MHz. (About P_{OFF}, it was relatively small.)



(a) (b)

Fig. 2. Simulated (a) capacitance curves with drain voltage dependence and (b) potential contours (black lines) and depletion layer (white lines) at Vds=1V, 30V and 60V in the FP-MOSFET.

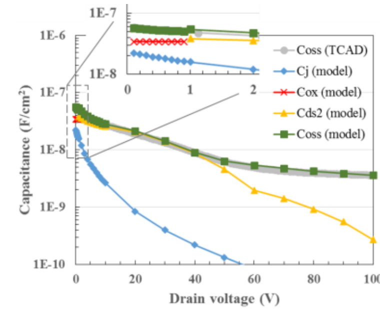
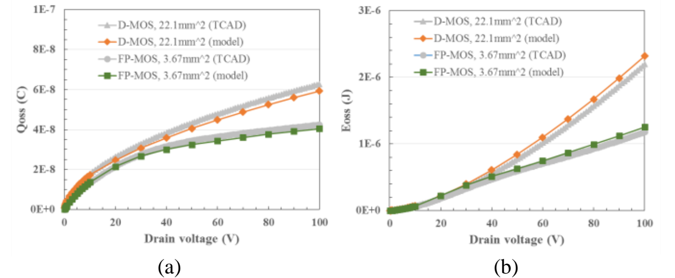


Fig. 3. Calculated output capacitance (C_{oss}) components of FP-MOSFET by compact model and simulated C_{oss} by TCAD.



(a) (b)

Fig. 4. Calculated (a) Q_{oss} and (b) E_{oss} of D-/FP-MOSFET by compact model compared to TCAD. Die size on same R_{ON} products.

5. Conclusions

We proposed the structure based compact model for the C_{oss} of the latest FP-MOSFET. The calculated Q_{oss} and E_{oss} corresponded very well to TCAD results, and we could discuss the FOM and the power loss. Regarding next generation FP-MOSFET, it is expected that the proposed compact model is useful for the device performance prediction.

References

[1] W. Saito *et al.*, *Proc. ISPSD* (2013) 241.

[2] K. Kobayashi *et al.*, *Proc. ISPSD* (2015) 141.

[3] R. Sodhi *et al.*, *Proc. ISPSD* (1999) 241.

[4] Y. Chen *et al.*, *Jpn. J. Appl. Phys.* **44** (2005) 847.

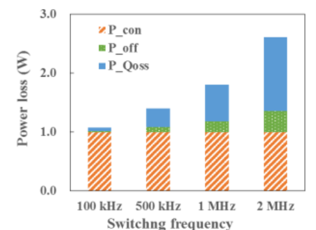


Fig. 5. Estimated power losses of FP-MOSFET in assumption of 10A and 100k to 2MHz operation.