An Automated Targeting Mechanism with Free Space Optical Communication Functionality for Optomechatronic Applications

by

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Dedicated to my rabbits, Cadburry and the late Ms. Binks and Hershey. Your grumpy, yet expressive demeanor will always bring a smile to my face.

Preface

The entirety of the efforts detailed in this dissertation have been granted by the Intelligent Sensor Platforms for Remotely Piloted Vehicles (INSPIRUS) project within the Faculty of Engineering at Memorial University of Newfoundland (MUN). During the course of project, the author has partnered with numerous individuals to theorize, share ideas and engage in collaborative design. Correspondingly, portions of the outcomes have appeared in peer-reviewed journals and conferences as co-authored publications. Most notably, Chapter 3 is an enhanced, combination of published works, referenced accordingly within the thesis. As well, a section of Chapter 4 pertains to control method ideas obtained from a co-authored journal paper. Furthermore, a version of Chapter 3 is currently in press.

Without the collaboration of the project team, the novel outcomes of this thesis would not be possible. In particular, while the author was predominately responsible for the majority of the research, validation of the specifications pertaining to the novel voice coil actuator, the parallel orientation manipulator structures and the printed circuit board designs containing the hardware devices and image sensing technologies were provided by other members. Additionally, the development of the hardware-based camera and the object recognition and parameter identification techniques were developed by another colleague. However, rigorous testing, code integration into necessary systems, the algorithm explanation, figures and code modification were completed by the author. Foremost, the author recognizes the principal investigator

of the INSPIRUS project, Dr. Nicholas Krouglicof, Dr. Taufiq Rahman, Mr. Dennis Fifield and Mr. Teng Wang as invaluable contributors of their knowledge, expertise and design capabilities.

Abstract

This thesis outlines the development of an agile, reliable and precise targeting mechanism complete with free space optical communication (FSOC) capabilities for employment in optomechatronic applications. To construct the complex mechanism, insight into existing technologies was required. These are inclusive to actuator design, control methodology, programming architecture, object recognition and localization and optical communication. Focusing on each component individually resulted in a variety of novel systems, commencing with the creation of a fast (1.3 ms^{-1}), accurate (micron range) voice coil actuator (VCA). The design, employing a planar, compact composition, with the inclusion of precision position feedback and smooth guidance fulfills size, weight and power (SWaP) characteristics required by many optomechatronic mechanisms. Arranging the VCAs in a parallel nature promoted the use of a parallel orientation manipulator (POM) as the foundation of the targeting structure. Motion control was achieved by adopting a cascade PID-PID control methodology in hardware, resulting in average settling times of 23 ms. In the pursuit of quick and dependable computation, a custom printed circuit board (PCB) containing a field programmable gate array (FPGA), microcontroller and image sensing technology were developed. Subsequently, hardware-based object isolation and parameter identification algorithms were constructed. Furthermore, by integrating these techniques with the dynamic performance of the POM, mathematical equations were generated to allow the targeting of an object in real-time with update rates of 70 ms. Finally, a FSOC

architecture utilizing beam splitter technology was constructed and integrated into the targeting device. Thus, producing a system capable of automatically targeting an infrared (IR) light source while simultaneously receiving wireless optical communication achieving ranges beyond 30 feet, at rates of 1 Mbits per second.

Acknowledgments

The pursuit of receiving a doctorate degree is not a task one achieves alone. Throughout the journey, numerous individuals were responsible in delivering the goals obtained within this dissertation. Thus, nearing its end, one must reflect upon the support, advice, knowledge and experience imparted by these admirable people.

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I must acknowledge my co-supervisor, Andy Fisher and supervisory committee member, Dr. Siu O'Young for their support nearing the end of this voyage. Their supervision and financial assistance ensured that focus and commitment to the research were my top priority. Without this support, the thesis would not have been finalized at such an accelerated rate, and for this I am forever appreciative.

I offer my sincerest regards to the wonderful and intelligent technical staff at Faculty of Engineering & Applied Science within Memorial University of Newfoundland (MUN). The ideas and advice put forth by their knowledge and experience were key to realizing the outcomes of the thesis. I thank Brian Pretty, Tom Pike, Greg O'Leary, Glenn St. Croix, Steve Steele and Don Taylor. Their enthusiasm and skillful nature ensured

even the most rudimentary request was fulfilled.

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To all graduate students, my friends, who have accompanied me on this path, I thank them. The knowledge, experience and advice they have provided were essential in the completion of this thesis. No matter the question or concern, there was always someone willing to help. My appreciation goes to Dennis Fifield, Taufiq Rahman, Migara Liyanage, Raju Hossain and Teng Wang. The talks and collaborations we've shared were fundamental to the accomplishments of this research. Their friendship will always be remembered.

I wish to acknowledge the generous financial support contributed by Memorial University of Newfoundland, the Research and Development Corporation of Newfoundland (RDC), the Atlantic Canada Opportunities Agency (ACOA) and the Boeing Company. Without them, these technologies would not have been realized.

I give love and thanks to my wonderful parents, Irene and Charlie Hicks. Their unwavering support has guided me through the many bumps along the road, allowing me to become the person I am today. Without their humble guidance and sacrifice, the pursuit of this degree would not have been possible.

With humble regards I express my deepest gratitude to my wife, Dana. Her love and moral support throughout the entire process has been a light guiding me down this path. With patience and selflessness she has encouraged me to press on, no matter how daunting the task may be. Words alone cannot express my thanks.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

Historically, mechanical and electrical systems and corresponding disciplines have been segregated, self-contained and independent. However, due to ongoing technological advancements, classifying a device as purely mechanical or electrical has become questionable. To this end, an encompassing, multi-domain nomenclature termed "mechatronics" may be selected when referring to electro-mechanical frameworks. Correspondingly, to further broaden the definition, mechatronics is the embodiment of knowledge contained within mechanical, electrical, computer, telecommunication and control engineering disciplines [1].

Integrating optical technologies into mechatronic systems has been a modern realization stemming from the desire for application specific active vision functionality [2]. A system resulting from the fusion of these technologies is termed "optomechatronics" or "optomechatronic technology" and has given rise to increasingly robust mechanisms with greater levels of performance, autonomy and intelligence [3]. Examples pertaining to optomechatronics include, but are not limited to object targeting [4], camera orientation control [5], image stabilization [6] and free space optical communication (FSOC) [7]. A singular system combining these capabilities gives rise to an abundance of applications in the aerospace and underwater sectors. In this regards, this thesis

pursues the development of a fast, reliable and precise targeting system complete with FSOC functionality for employment in optomechatronic applications. Note, to prevent tedium, when discussing the tracking and aiming (pointing) towards an object in motion, the thesis will refer to this process as automated targeting, with the device providing this functionality deemed an automated targeting mechanism (ATM).

1.1 Motivation

As advance military technology becomes a reality, so does the dependence on secure, high speed communication networks [8]. While wireless protocols such as radio frequency (RF) and Wi-Fi dominant many optomechatronic applications, they are prone to interception, lack high transmission rates and are constrained to short distances, respectively [8–10]. As an alternative, FSOC is a relatively undiscovered technology that is presently being pursued as an effective communication strategy. Fundamentally, FSOC involves pulsing light at extremely high rates, mimicking binary data flow and allowing for exceptionally fast transmission speeds. In addition, being application specific, it is applicable to long and short range communication links. However, to maintain a reliable data connection and prevent signal degradation, line-of-sight must exist between its transmitter and receiver. To aid in the situation, a mechanism capable of targeting the light source and directing a light absorbing sensor in line with its trajectory is of considerable value. To meet this objective, the thesis discusses the creation of a device, which by combining all of the following systems with beam splitter technology, a single light source is not only actively targeted, but also acts as a means of high speed data transmission. While systems are capable of extremely fast transmission rates (i.e., gigabits per second) and long ranges (i.e., hundreds of kilometers) [11, 12], due to time limitations, a FSOC system capable of

500 kbits per second at a range of 30 feet was desired.

Reliability, precision and speed are fundamental characteristics which form the foundation of any ATM. In addition, meeting the strict requirements of size, weight and power (SWaP) is vital when they are employed for use in optomechatronic applications. Furthermore, an ATM with the ability to align a receiving module with a transmission device, delivering data via an optical communication link is even more susceptible to these stringent conditions. While individual, commercially available components may be configured to produce such a mechanism, the integration of multiple parts may cause a loss of precision and robustness in the process. In contrast, designing each component with the specifications of the final mechanism in consideration is more effective in generating optimal results. Therefore, this thesis is motivated by the need to create an ATM with FSOC capabilities which conforms to strict performance requirements desirable for miniature optomechatronic applications. The majority of these requirements must be satisfied though the design of the actuators comprising the mechanism.

Voice coil actuators (VCAs) are readily employed in a number of mechatronic applications due to their relatively simple construction [6, 13, 14]. Resulting from their electro-mechanical nature, these devices are manufactured to generate linear motion in response to electrical stimulation. However, the commercially available renditions comprised of cylindrical coil windings (i.e., rotor) and permanent magnets (i.e., stator) are riddled with an assortment of limitations imposed on the end-user. These include lack of position sensing, absence of linear guidance and difficult integration with other mechanisms. The primary design goal was to remedy these concerns and boost functionality. Thus, a novel VCA was created employing a planar, compact composition, with the inclusion of precision position feedback and smooth guidance [15, 16]. By interconnecting multiple actuators to a mobile platform, small scale

parallel orientation manipulators (POMs) were formed and were utilized as the basis of the automated targeting system. Finally, a set of quantitative design metrics were identified via a commercially available system with the following specifications; a force constant of 3.6 N/A, voltage requirement of 48 V, weighs 236 g, dimensions of 78 mm x 56.6 mm x 20 mm, a moving mass of 40 g and is accurate in the micron range [17]. These parameters, along with the sub-system integration, are viewed as achievable goals for the novel VCA construction.

The robustness, reliability and precision of any motion-based mechanism is greatly dependent on its control architecture. Correspondingly, defining a suitable platform to implement the control loop is deterministic upon the specific application required. With respect to the ATM, comprised of the VCA technology, these conditions are extremely stringent due to its high dynamic capabilities and SWaP requirements. Though the traditional proportional-integral-derivative (PID) control architecture has many applications in real-world mechatronic systems [18], the rudimentary design limits it from employing precise control to systems with extreme dynamics. In addition, the slow, sequential computation of high-level programming languages and their compatible platforms are unable to cope with the agility of the VCA. To alleviate these restrictions, the thesis adopts a variation to the PID scheme defined as a cascade PID-PID controller fabricated in a hardware-based environment employing field programmable gate array (FPGA) technology. The corresponding architecture was compared and contrasted to a hardware PID loop as well as the more involved and powerful active disturbance rejection controller (ADRC) [19].

The construction of complex code in software-based environments is widely accepted as development times are short and programming resources are readily available. In many cases these designs provide optimal results with many mechatronic systems [20, 21]. However, considering the time-sensitive control schemes and strict

SWaP requirements of the targeting system, high-level programming languages are not suitable due to their sequential nature and large power specifications. While hardware desription languages (HDLs) have been present for many years [22, 23], they are essentially an exercise in manipulating digital circuitry and such, require longer development times, are restrictive in nature and have difficulty handling complex mathematics. These conditions have prevented HDL from being accepted by many developers compared to its software-based variation. However, despite these concerns, HDL code developed in conjunction with FPGAs promotes parallelism, reliability and high rates of processing, making it an ideal candidate for the POM architecture. However, readily available printed circuit boards (PCBs) comprised of FPGA technology are bulky and generalized, negatively affecting SWaP conditions. To this end, the thesis presents application specific PCBs containing electronics suitable for controlling multiple VCAs, with a larger set designed with image sensing abilities; ideal for developing the targeting system. In addition, a shared memory controller was designed in HDL and C, allowing the bi-directional communication link between an FPGA and microcontroller. This protocol has many benefits and was vital to the overall production of the ATM with FSOC functionality.

Visual object recognition has existed in literature for many years and persists in a number of applications [24, 25]. While there are many techniques to isolate and locate a particular region of interest, determining its characteristics requires more complex procedures, especially when the object is in motion. Though many algorithms are readily available for completing these tasks in high-level programming and near real-time, isolating a region of interest and generating a variety of identifying parameters in real-time requires high-speed processing capabilities. However, due to the parallel nature of the FPGA, it is an ideal candidate to perform these tasks. Furthermore, taking advantage of the application specific PCB, HDL based object isolation and

contour tracking methods were developed to produce real-time object recognition and parameter identification. Correspondingly, the object parameters determined by these algorithms were key to efficiently targeting an object in motion.

While there are a myriad of systems capable of localizing an object in motion within camera's field of view (FOV) [4, 5, 26], many employ mechanisms incapable of following high dynamic objects. Automatically targeting and maintaining a continual fix in real-time on such an entity is problematic due to the reliance of multiple devices and the extreme positioning and processing requirements. In addition, devising an accurate model relating the discrete locations of an actuator to the centralized target orientation is challenging in design. Nonetheless, integrating hardware-based control architectures and parameter identification within a single FPGA chip, while utilizing the power of design of experiment (DOE) methodology creates a solution to these issues. To this end, the thesis presents a small scale POM, capable of object recognition and targeting via HDL developed algorithms; in turn fulfilling SWaP requirements.

1.2 Statement of Co-Authorship

All research pertaining to this thesis has been achieved under the Intelligent Sensor Platforms for Remotely Piloted Vehicles (INSPIRUS) project situated within the Faculty of Engineering at Memorial University of Newfoundland (MUN). The scope of the INSPIRUS project was to theorize, design and manufacture high-speed, robust, reliable mechanisms for optomechatronic applications specifically relating to autonomous unmanned vehicles. Throughout the span of the venture, many individuals have contributed their knowledge, experience and time developing and refining the project outcomes. Additionally, during the course of the project, the thesis author has co-authored peer-reviewed journal articles and conference materials with other

members of the research team [15, 19]. Permission to include information from these publications has been obtained from the corresponding authors.

Without the collaboration of numerous partners, the results of this thesis would not be a reality. In particular, while the author was predominately responsible for the majority of the research, experimental validation of the force constant and open loop specifications of the novel VCA (Chapter 3), the POM architecture designs (section 3.3), the FPGA PCB realizations (sections 5.2 and 5.3) and the camera and tracking HDL designs (section 6.4) were primarily contributed by other project associates. Most noteworthy, the author recognizes Dr. Nicholas Krouglicof (the principal investigator of the INSPIRUS project), Dr. Taufiq Rahman, Mr. Dennis Fifield and Mr. Teng Wang as contributors of their knowledge, expertise and design capabilities, as invaluable participants to the results of this thesis.

1.3 Contributions of the Thesis

Due to the nature of optomechatronic design, a variety of systems must be realized to present a fully functional system. To this end, in the pursuit of a ATM with FSOC functionality, the systematic creation of individual components must be detailed to understand the structure as a whole. Therefore, the contributions of the thesis are not limited to the final outcomes, but are the result of the many puzzle pieces combining to form the final device. Correspondingly, the outcomes are inclusive to a wide selection of practical applications defined as follows:

Design of a high performance VCA for optomechatronic applications: A voice coil actuator which replaces the traditional cylindrical-based model of commercially available linear motors was designed. It addresses the limitations of current small-scale actuators by the inclusion of accurate feedback circuitry, a miniature

guidance system and self-contained drive electronics. In addition, the generic cylinder format was reshaped in planar fashion comprised of Halbach array magnetics acting as the stator and a printed circuit board fulfilling the role of the rotor. Validation of the entirety of the compact actuator gave confirmation to its proposed high-dynamic, precise operation.

Classification of hardware designed control structures for high dynamic mechanisms: Traditional, simplistic control architectures are incapable of dealing with the maneuverability of high dynamic mechanisms. As well, software-based compositions are unable to react to control adjustments quickly (i.e., rates in the MHz range), due to their sequential nature. While more complex schemes have been proven effective in an HDL environment, many times they are challenging to implement and are resource consuming. Alternatively, a well-established methodology, the cascade PID-PID control system, implemented in hardware may grant an adequate means of control while remaining uncomplex in design. To validate the theory, a comparison between hardware-based PID, cascade PID-PID and ADRC architectures was accomplished.

Development of application specific printed circuit boards containing bi-directional communication links for use in optomechatronic applications: Due to the bulky, generalized nature of off-the-shelf FPGA printed circuit boards, integrating them into existing hardware is cumbersome, resulting in reliability and robustness issues. To this end, two distinct, application specific designs were generated to overcome these concerns while being extremely adaptable in nature. Each were comprised of an FPGA and a microcontroller chip while the second, larger variation contained additional electronics providing image sensing and storage functionality. Furthermore, a bi-directional, shared memory control architecture was developed in

hardware and software to provide a stable, fast communication link between the FPGA and microcontroller. Each design was validated by the extended use in a variety of mechatronic systems.

Isolation and parameter identification of fast moving objects in images using hardware description language: The isolation and characteristic generation of a region of interest in real-time is difficult to accomplish with higher level programming languages due to their sequential nature. Therefore, algorithms capable of segregating an object's pixel information from its background data, while simultaneously calculating a set of identifying parameters was developed in HDL. The confirmation of the methods was accomplished by means of integration into already proven mechanisms.

Prototype implementation of an automated targeting system through the application of design of experiment methodology: Maintaining a localized fix on a maneuverable object in real-time is difficult to accomplish due to the extensive reliance on numerous subsystems, high actuation requirements and time-sensitive algorithms. Furthermore, developing a reliable means of relating linear motor positions to the orientation of the targeting platform is non-trivial in nature. However, taking advantage of the capabilities of the POM architecture and methods provided by DOE, a system of non-linear equations were generated to remedy these concerns. The equations were adopted into the FPGA memory control architecture to permit the complex mathematics to be accomplished in the microcontroller. The precision of the targeting mechanism was validated through rigorous, real world experimentation.

A hardware-based free space optical communication link for use with an automated targeting device: As technology advances, so does the dependence on secure, wireless data transmission, especially in high-risk sectors. While Wi-Fi and RF protocols are dominant in the industry, the use of FSOC in mechatronic systems has

begun to rise. To confer with this increase, a low powered, FSOC system adhering to SWaP conditions was developed in HDL. However, as its data link is entirely dependent on line-of-sight, small discrepancies in the locations of either the transmitter or receiver can result in communication loss. To this end, a ATM with FSOC capabilities was pursued, resulting in a conglomeration of all of the aforementioned technologies. To quantify the FSOC algorithm and validate the accuracy of the ATM, a number of real-time test scenarios were completed.

1.4 Organization of the Thesis

The following is an organization of the remainder of the thesis:

Chapter 2: provides a brief study of the literature pertaining to all systems related to the development of the ATM and FSOC architectures.

Chapter 3: discusses the design and experimental validation of a novel VCA. In addition, it details the construction of two POM structures for use in optomechatronic applications and their subsequent parameters.

Chapter 4: details the design of hardware orientated PID and cascade PID-PID control schemes. Correspondingly, the chapter provides the comparison results between these controllers and the more powerful ADRC when implemented by the high-dynamic VCA.

Chapter 5: documents the construction of two customized, application specific FPGA PCBs. Furthermore, it provides evidence of the importance of hybrid FPGA and microcontroller technology.

Chapter 6: highlights the development of hardware-based, object recognition and parameter identification algorithms for real-time applications.

Chapter 7: implements a precise, quick automated targeting device fulfilling SWaP requirements, comprised of the technologies discussed in previous chapters.

Chapter 8: features the design of a reliable, low-power FSOC system in HDL. Additionally, utilizing beam splitter technology, an FSOC capable ATM was proposed.

Chapter 9: offers concluding statements along with future research possibilities.

Chapter 2

Literature Review

2.1 Introduction

Employing a mechanism with the task of automated targeting and optically communicating with a mobile light source may be approached in many ways, as constructing a solution requires the integration of many stand-alone subsystems. Therefore, it is necessary to cover all aspects pertaining to such a complex device. This section describes the existing literature relating to each individual system and includes concepts, designs, theories and alternatives to the research proposed in this thesis. The following topics have been identified as the most pertinent in the development of the aforementioned automated targeting and communication mechanism.

2.2 Mechanisms for Employment in Targeting Systems

References to pointing systems have been present in the literature for many years [27]. Mechanisms of particular interest which have a variety of applications are gimbals, with Rue giving a brief description [28, p. 697]: *"Although a typical gimbal system usually*

consists of a series of separate axes that are mechanically linked in such a way that several degrees of angular freedom are provided, the identification and measurement of the misalignments associated with a single-axis system are illustrative."

There have been many gimbal systems created with the purpose of automated targeting applications in the literature [5, 29–32]. For example, Shim et al. have developed a precise pointing system for FSOC applications using a system of gimbal stages [30]. Likewise, Abughalieh *et al.* have created a compact, portable, object tracking system using off-the-shelf electronic components, computer vision algorithms and a gimbal system [5].

As indicated, gimbal-based automated targeting devices have been designed and function quite well. However, gimbals systems do contain a number of limitations. Sofka *et al.* states [33, p. 726]: *"Traditional gimbal systems benefit from the design intention of decoupled operation but suffer from singularity, relatively high inertia, cable routing difficulties, and limited range and accuracy."*

In constrast, a parallel kinematic mechanism (PKM) can be considered a suitable candidate to employ as a pointing mechanism as traditionally, when designing a device requiring the capabilities of automated targeting, many specifications must be considered. In particular, the kinematics, dynamics, precision and range of motion or workspace of the driving mechanism. Traslosheros *et al.* details the importance of accuracy when implementing these systems by stating how it is a crucial specfication for PKMs, especially those employed in machining, manufacturing and assembling of electroincs and other devices [27, p. 5637]. PKMs are closed-loop systems in which an end effector or mobile platform is connected to a stationary base by a minimum of two independent kinematic chains. Its advantages include an impressive payload-to-weight ratio due to multiple parallel chains, superior accuracy and speed, high structural stiffness due to the closed kinematic structure and simple resolution of the inverse

kinematics equations [34–37].

Though PKMs have many benefits and are excellent for employing in ATMs, they also contain weaknesses. One such issue relating to the PKM architecture corresponds to the small workspace they generally exhibit. Thus, reducing a pointing device's overall range of motion or potential field of view characteristics [34, 37]. Additionally, they suffer from difficult-to-solve forward kinematic solutions which may hinder the control of the device [34].

There are numerous linear actuators commercially available which often make it difficult to determine the optimal choice for utilization in PKMs. However, with the application of targeting a mobile object being the primary function, the actuator in question must be dynamic, responsive and accurate. A review of the literature produced two specific renditions which fit this criteria: voice coil actuators (electromagnetic motors) and piezoelectric motors.

Villgrattner and Ulbrich employ piezo-actuators for a camera orientation mechanism [38], while Dong et al. utilize them for trajectory tracking [35]. From the authors work [15], a novel voice coil system was produced which fulfills all of the requirements. It features little moving mass, a high force constant, accuracy in the submicron range and generates large velocity and acceleration. Positioning three of the novel VCAs in a specific configuration results in a highly dynamic PKM [19].

There are cases in literature of PKMs being employed as potential automated targeting devices [37, 38]. Fatehi *et al.* implement a large PKM for use in low orbit satellite tracking applications, which requires the fast, precise capabilities found within the PKM architecture [37]. Correspondingly, when considering PKMs which involve rotational motion only, they can be more accurately referred to as parallel orientation manipulators [39]. Furthermore, Villgrattner and Ulbrich propose a piezo-driven, two degree of freedom (DOF) camera orientation mechanism with a potential application

for artificial eye control in humanoid robots [38]. However, overall, there was little literature available regarding the development of PKMs comprised of VCAs being utilized as pointing devices for targeting and communication systems.

2.3 Hardware-Based Control for Highly Dynamic Systems

Developing a responsivie, robust control archtiecture to ensure positioning of the linear motors are percise, is an absolute requirement for the targeting system. Traditionally, many actuators are controlled via a single PID controller [18]. There are many advantages of using this algorithm, such as its simple, practical implementation [40]. While Huang, Bai and Zhu further the discussion by stating that PID controllers are still widely used in industrial control due to its robustness and tuning [41, p. 43]. However, due to the high dynamics of the novel voice coil developed in the authors work [15], a control algorithm capable of outperforming the single PID loop is required.

Thus, in response, a more complex rendition of the PID control scheme, deemed the cascade PID-PID controller, was considered a result of its relativity uncomplicated design, simple tuning configuration, fast response and strong disturbance rejection [42]. The cascade control system is comprised of a inner and outer loop which effect the performance of the method. In particular, the inner loop can eliminate disturbances in the system in a timely manner, improving the dynamic characteristics of the system [43, p. 1089]. Note, there are many alternative control methods throughout the literature utilized for accurate control such as state space model [44], fuzzy logic [45] and nonlinear control schemes [46, 47]. However, due to the cascade's similarity to PID control and time limitations, it was the primary control method chosen as the

focus of the thesis.

There are many exmaples pertaining to the ultization of cascade PID-PID control methods found within the literature [42, 48–52]. To elaborate, Mercorelli and Werner have developed a cascade PID-PID controller for use in automotive applications, resulting in a fast and accurate control system [48]. Another study employed the scheme for a de-superheating water system [49]. The algorithm was effective, despite the system being exceptionally coupled and containing non-linear parameters; issues which an appropriately tuned cascade controller can cope with. Finally, Pisano *et al.* have presented position and speed control of permanent magnet (PM) DC rotary motor drives [52]. This system is comprised of the cascade PID-PID control configuration and results in exceptional performance. Though the aforementioned authors proposed a rotary motor control solution, the literature provided little with respect to the control of highly dynamic linear motors with the cascade architecture.

2.4 FPGA and Microcontroller Hardware for Optomechatronic Applications

FPGA's are integrated circuits which are configured via HDL with many renditiions being defined as a system-on-a-chip (SoC). The FPGA architecture provides ample speed for compuatation, is tiny and compact, freeing space and reducing weight, exhibits low power consumption and promotes parallelism. Due to these specifications, they are well-suited for applications which require very high-speed processing [53].

FPGAs are becoming more prominent in the development of algorithms for a variety of engineering applications [20, 23, 54, 55]. Chen, Yang and Wong created an FPGA digital controller for boost conversion with power-factor-correction [20].

The chip was selected due to its versatility and parallelism. Furthermore, due to its advantages and the low cost requirements of an FPGA, Nguyen et al. generated a multiport memory controller for multimedia processing and other high bandwidth applications [55].

An ATM requires the creation of swift, accurate control algorithms and robust image processing techniques to achieve optimal positioning and target identification. To ensure these specifications are satisfied, implementing them via a HDL such as Verilog or very high speed integrated circuits (VHSIC) HDL (VHDL) is extremely important [18, 53, 56]. Jain *et al.* employed a Xilinx FPGA for the development of a robust median filter algorithm which enables a variety of image processing applications to be explored [56]. Addiontionally, another study created an FPGA-based PID controller for controlling direct current (DC) servo motors [18]. Furthermore, with industrial control applications under consideration, Monmasson *et al.* designed a sensorless motor controller using VHDL [53].

In addition to its difficulty in processing complicated mathematical functions, developing error-checking code within the framwork of an FPGA can be complex [57]. Therefore, another important device which can migate these issues and assist in the procedure of designing hardware-based applications is the microcontroller. These versatile chips are fast, require little power, are tiny and allow for the development of complex algorithms [22]. Due to the utility of the microcontroller, the literature frequently references its implementation in a varity of applications [58–60].

To utilize the capabilities of both devices, printed circuit boards encompassing an FPGA in addition to a microcontroller on the same chip, albeit a virtual, "soft" rendition, have become readily available. This allows for programming in higher level languages, such as C, with the microcontroller and VHDL code for the FPGA, with a maufacturer specific interface connecting the two languages [61]. Studies

have shown a wide varitey of designs employing this particular configuration [61–63]. Though this architecture has a number of advantages, virtual microcontrollers are very problematic to configure than their physical counterparts. Therefore, FPGAs which contain dedicated, "hard" processors, or microcontrollers, have recently been constructed, enabling direct connectivity to the FPGA [22]. This permits flexible and easy programming for both devices and ensures high speed data transmission between them [64]. However, the user is forced to develop code in the environment provided by the manufacturer, restricting the use of more user-friendly interfaces.

Due to the simplicity of the Arduino software enviroment, many researchers have combined the high efficiency of an FPGA with the robust functionality of a microcontroller to perform a variety of tasks [21, 65–67]. For example, Agrawal and Prakash have employed the benefits of combining an FPGA and microcontroller for temperature sensing [65]. To further illustrate, Salina and Malathi have created a faster, less complex sensor fusion system from an FPGA and Arduino-capable microcontroller for object localization in robotics [21].

While much of the literature focuses on FPGAs and microcontrollers located on separate circuit boards, others have joined them with exceptional results [63, 68–70]. However, there is very little information regarding the direct, onboard communication of an Arduino-capable microcontroller with an FPGA. A configuration of this design, would allow the FPGA and microcontroller to have immediate access to each device's functionality. This ensures fast, reliable data transmission between each device promoting the ability to manipulate complex mathematics in the microcontroller and transmit the results to an FPGA for parallel processing.

2.5 Hardware-Based Camera Systems for Object Isolation and Parameter Identification

FPGA devices are advantageous for use in camera systems due to their extreme design flexibility, high throughput and overall ability to complete image processing faster than that of a traditional software approach [71–73]. Wei *et al.* gives a definition of a "smart" camera as a vision based system with its fundamental purpose to garner a understanding of the information of an obtained image and gather detailed data for use in other systems [74, p. 826]. Furthermore, it can be recognized as "smart" due to its connecting with some form of processing unit which can extract application specific data from stored images [74, p. 826].

There are many FPGA-based camera technologies outlined in the literature which are utilized in a variety of applications such as, video camera systems [75, 76], range detection [77], mobile robotic applications [78] and road traffic surveillance [74]. Supplying an FPGA with pixel information enables many image processing techniques to be accompshied in real-time [73, 79, 80]. For instance, Hocenski et al. implement edge detection using convolution kernels in order to produce an automated ceramic tile defect detector [73]. In similar fashion, Dhanabal et al. take advantage of brightness and contrast manipulation, as well as thresholding to determine the number of coins in an image [80].

One application of particular interest is object tracking (i.e., identification) dependent upon a set of desired criterion [25, 81–83]. Husin *et al.* describe a shape detection algorithm for object tracking by separating an image into smaller sections and determining predefined shapes within each segment [25]. Other research details an edge detection process based on noise filtering, image smoothing and canny edge

detection [81]. Finally, Lu et al. deliver a modified, mean-shift, real-time object tracking system that boasts high accuracy and robustness [82].

Upon review of the literature, it was evident that tracking related problems were a commonly occurring issue [84–87]. However, when referring to the tracking of mobile objects specifically, only a few were relevant. Miller and Miller discuss the tracking of a quadrotor on the basis of bearing only observations [87]. This system uses a pseudo-measurement filter, as opposed to a more standard Kalman filter, to determine the position of a quadrotor based upon its trajectory. While, Yokoyama and Poggio describe a contour-based tracking algorithm for detecting and tracking moving targets [24].

Fully realized, custom FPGA boards containing image sensors are not uncommon in the literature [72, 75, 76]. Even those which interface this strcuture with a microcontroller have been developed [88, 89]. However, contour tracking algorithms for object isolation and parameter identification are uncommon in literature, particularly those based on FPGA and microcontroller architectures.

2.6 Targeting Models for Centering Identified Objects

Targeting (i.e., aiming, pointing) an object in motion has been a fundamental problem in engineering domain for many years [90]. In addition to a suitable mechanism, a precise and robust algorithm must be created to reliably aim towards a maneuvering object. The method must be capable of relating the location of the mechanim's driving devices to a set of object parameters defined via image processing techniques [5]. Additionally, to develop algorithms capable of real-time targeting, intensive computa-

tion is necessary, requiring high performance algorithms and reliable hardware [83]. Furthermore, an ideal target must be identified to ensure simple image segmentation exists.

Targeting IR light sources is a very useful technique as IR light is invisible to the naked eye, not sensitive to changes in background illumination, the source is generally small and easy to install and it works better than visible light in many environments [91]. Fu and Wang have implemented a full targeting system utilizing a micro, two-axis turntable with an infrared signal-detecting and processing device in conjunction with an IR active source. To date, this system has only been tested indoors but has demonstrated that an IR target is a viable method for targeting mobile objects [4].

Determining the optimal algorithm which relates a set of object parameters and mechanism positions to locations resulting in the centering of the object (i.e targeting) is required for the ATM. While a number of approaches may be taken, designing a model of the system and the transformation of coordinate systems were researched. For example, Li and Ding propose a visual servo system and object tracking algorithms for the targeting of unmanned aerial vehicles (UAVs) [92]. By obtaining a model of the system via dynamic analysis, angular positions of the servo mechanism are related to image coordinates of a mobile UAV in the camera's FOV. In contrast, by transforming the world coordinate system to a set of camera coordinates through mathematical means allow for the targeting relationship to be accomplished [93, 94]. However, these methods can be computationally intensive in HDL, requiring matrix manipulation in the transformation scenario and needing a significant amount of effort to generate results.

2.7 Free Space Optical Communication Systems

FSOC is a relatively new approach that has been gaining much interest in the engineering field [95]. It is described as the transmission of infrared or modulated visible light through the atmosphere, or "free-space," to obtain fast broadband communications over several kilometers of distance [9, 96–98]. To obtain speedy data transfer, a light source pulsing at high rates is required [99]. The transmitter may also include a booster amplifier to increase the power of the light source [7].

There are many benefits to an FSOC interface as opposed to the more commonly used RF and Wi-Fi methods. Due to "free-space" being within a license-free, unregulated spectrum, it provides a low cost alternative with high bandwidth and robust security features [8, 97]. Additionally, detecting and intercepting data transmitted via FSOC is difficult and the link is unaffected by RF signals [100, 101].

In contrast to its advantages, using light as a form of communication does have its limitations. As a result of turbulence in the atmosphere as well as temperature, the light transmission suffers from signal fading, scattering and is easily affected by weather conditions such as rain and fog [8–10, 102]. Many of these disadvantages have been researched and a number of solutions have been proposed. Zhu and Kahn recommend the use of maximum likelihood sequence detection and spatial diversity reception to overcome signal fading by atmospheric turbulence [9]. When communicating through fog, Corrigan *et al.* demonstrates that mid-infrared (MIR) (8-10 μm) sources and detectors are a viable alternative to those categorized as near-infrared (NIR) (0.7-1.6 μm) [10].

Since FSOC systems are more complicated to design, are more uncommon than standard RF or Wi-Fi methods and utilize light for transmission requiring line of sight, protocols must be developed in order to maintain reliable communication

between sender and receiver [98, 103–105]. Aghajanzadeh and Uysal determined that initiating automatic retransmission request (H-ARQ) protocols results in better FSOC performance [104]. Furthermore, other studies have explored the idea of implementing short length raptor codes due to their independence of channel misalignment caused by tracking errors [105]. The authors determined that, as a result of their independence and low complexity, they are a fitting choice for optical communications.

Some particularly interesting applications of FSOC systems are their facilitation of the communication between autonomous vechicles [102, 106, 107]. However, the literature primarily focuses on the challenges which arise with this application. Nonetheless, optical communication from a fixed ground station to a UAV has been readily discussed [7, 8, 105]. Hatziefremidis *et al.* illustrates the signal to noise ratio (SNR) and bit error rate (BER) when dealing with specific situations involving a UAV and motionless station [8]. The authors determined that a slanted path between the two systems produced an optimal BER compared to that of a horizontal redendition. Similarly, another study researched the potential of a high power optical amplifier and a low noise optical amplifier to produce better signal quality in a variety of environmental conditions [7].

2.8 Conclusions

The existing literature pertaining to the multiple subsystems necessary for the creation of an automated targeting device with optical communication capacity was reviewed. It was determined that to satisfy the strict dynamic conditions of the mechanism, a number of VCAs would be utilized to form a PKM or more specifically, a parallel orientation manipulator (POM) configuration. In addition, the control scheme would have to be precise and capable of coping with non-linearity, thus a hardware-based

cascade PID-PID was selected due to its similarity to the PID algorithm and time constraints. To ensure SWaP requirements are met and to allow for real-time update rates, the combined FPGA and microcontroller architectures were chosen as the optimal development hardware. As such, a hardware-based image sensing device would be required for real-time object recognition and parameter identification of a infrared target. Furthermore, the light source to be used with the FSOC system was selected to be in the MIR to NIR spectrum to avoid potential transmission issues. As simple targeting methods were scarce, a design of experiments approach was taken to fulfill this gap. Finally, due to time limitations a rudimentary transmission protocol was developed for the FSOC system to validate the functionality of an ATM with FSOC capabilities.

Chapter 3

Design of a Novel Voice Coil Actuator for Optomechantronic Applications

VCAs are electro-mechanical devices with the capacity to generate linear motion in response to electrical excitation. The generic cylindrical design of commercially available VCAs impose a number of limiting conditions upon the end-user. The most restrictive is the necessity to integrate multiple components to grant specific capabilities and increase performance. As a solution to these fundamental issues, a novel voice coil actuator was designed which replaces the standard configuration with one of a planar nature. The VCA contains rectangular magnets in a modified Halbach array arrangement to ensure compactness and an exceptionally intense, uniform magnetic field. The moving mass is substituted with a PCB which employs an abundance of current conducting traces. In addition, the board encompasses a linear rail and bearing system, unified drive electronics and highly adaptive position feedback circuitry resulting in a compact, highly dynamic and precise device. Two unique PKMs were constructed to utilize the performance of the novel VCA and pursue optomechatronic applications. The mobile platform of each PKM was restricted to rotational degrees of freedom and thus, can be referred to POMs. In particular, two structures were defined, 2-$\underline{P}$SS/U and 3-$\underline{P}$SS/S in order to constrain their payloads to two and three degrees of rotational freedom, respectively. The resultant manipulators are highly dynamic, precise and fulfill SWaP conditions required by the automated targeting mechanism.

3.1 Introduction

VCAs are simple electro-mechanical mechanisms which generate motion in response to an electrical input. They consist of a current conducting coil residing inside of an intense magnetic field produced by stationary permanent magnets [108, 109]. Though several linear actuators are commercially available, their generic cylindrical construction facilitates a variety of limitations while attempting to meet the special requirements of many optomechatronic applications. Most notably, it is the end-user's responsibility to integrate supplementary components to enable functionality and boost performance. These include position feedback devices, drive electronics and linear motion guidance systems. The incorporation of multiple components not only reduces the reliability of the mechanism, but makes packaging and system minimization problematic, negatively affecting its SWaP characteristics.

As a solution, a novel VCA was designed, replacing the tradiiontial cylindrical structure with one of a rectangluar nature through four fundametal alterations. First, planar mangets were arranged in a modified Halbach array [110] configuration and incorporated into the structure providing compactness and an exceptionally uniform, internally concentrated magnetic field. Second, the moving mass of the VCA was composed of a slim, lightweight printed circuit board with numerous current conducting traces ensuring a minimal gap exists between the Halbach arrays. Third, a position feedback system was created via a position sensitive detector (PSD) and highly adaptive signal conditioning circuitry, resulting in extremely precise actuation. Finally, taking advantage of the coil's geometry, miniature linear rails and bearings were integrated to its architecture to guarantee the smooth motion of the actuator.

In the pursuit of optomechatronic applications, the VCAs were arranged into a structure known as a parallel kinematic mechanism which displaces a mobile platform

in the same fashion as a freely suspended body. In particular two configurations were generated; the 3-PSS/S (3DOF) [111] and the 2-PSS/U (2DOF) [112] which limit the mobility of the platform to rotational motion, reclassifying the architectures as parallel orientation manipulators. The POMs were designed with SWaP requirements under consideration in hopes of defining the most suitable candidate for employment in the ATM.

3.2 Components Comprising the Novel Voice Coil Actuator

The force generated by a VCA, known as the Laplace (Lorentz) force [113, 114] is governed by equation 3.1,

$$F = BLI \tag{3.1}$$

where B is the magnetic field or flux density, L is the conductor length and I is the coil current. It is easily identified that the strength of the magnetic field, the current introduced to the coil and the length of the conductor is of utmost importance in generating an impressive force, a key performance metric pertaining to linear actuators. Therefore, the following sections detail the design of the magnetics, the PCB containing the conductor and all other necessary modifications, resulting in the realization of the highly dynamic, precise, novel VCA.

3.2.1 Magnetic Configuration

In comparison to conventional voice coil magnetics, a Halbach array magnetic configuration was utilized to enhance and direct the magnetic field of the VCA [115, 116]. A typical array is comprised of planar magnets of equal strength and size, arranged

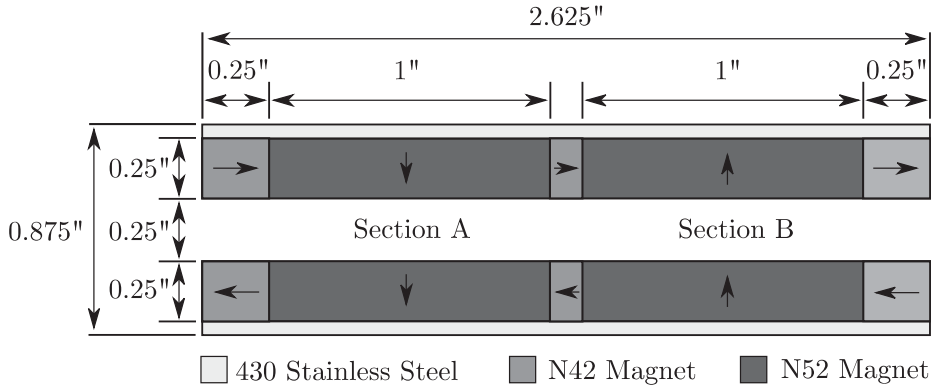


Figure 3.1: Modified Halbach array with pole orientations.

in a linear fashion. However, this formation results in large variations in magnetic magnitude over small distances [117, 118]. In contrast, an array composed of five neodymium magnets, of three varying sizes, with pole orientations arranged ideally results in a more robust design exhibiting high interior and low exterior field strengths. Placing two sets of these configurations $\frac{1}{4}$ inch apart, with the active area's facing one another results in the modified array, displayed in Fig. 3.1.

The one inch magnets are the primary source of the strong, uniform magnetic field experienced by the conductive traces of the PCB (discussed in section 3.2.2). Conversely, the $\frac{1}{4}$ inch magnets direct the field between their larger counterparts to prevent leakage of the magnetic flux. This not only significantly increases interior field strength and uniformity, but also greatly reduces the magnetism experienced by the external surroundings of the arrays. Finally, stainless steel plates were incorporated to the exterior of the array to further boost these enhancements.

Before physical construction, the modified design was configured and validated by way of the Finite Element Method Magnetics simulation software package (FEMM Version 4.2). FEMM is capable of producing a visual means to magnetic uniformity and field strength and was an essential tool in the design of the modified Halbach array.

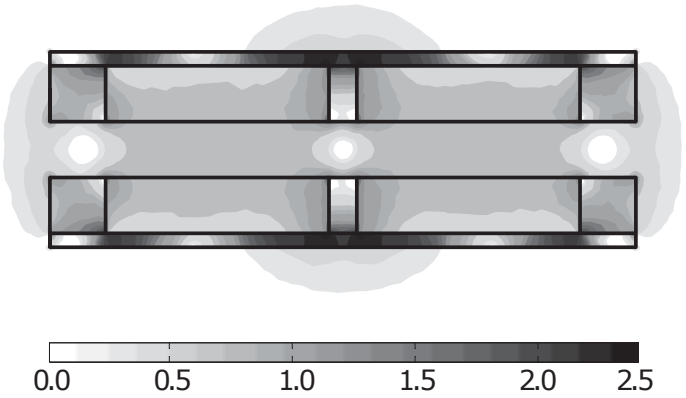


Figure 3.2: FEMM simulation of the magnetic magnitude in tesla.

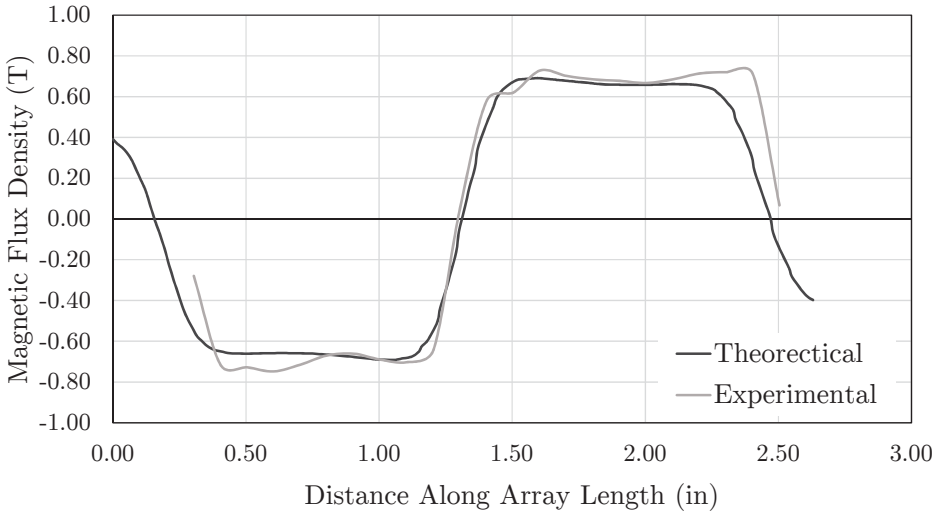


Figure 3.3: Simulated and experimental results of the magnetic flux density.

Fig. 3.2 illustrates the finalized design which resulted in an interior field strength of approximately 7000 gauss (0.7 tesla), while the exterior was significantly less (i.e., nearly non-existent along much of the array's structure). Furthermore, Fig. 3.3 highlights the physical realization's interior field strength with that of the FEMM simulation. As shown, the experimental flux essentially matches the theoretical (simulated) field, proving the validity of the physical rendition, with a maximum standard deviation of 0.286 tesla nearing the edge while the average was 0.056 tesla. Note, the experiment was accomplished by logging the normal flux density at the

mid-gap at 0.1 inch intervals via a gauss meter.

3.2.2 Printed Circuit Board Coil Design

The novel voice coil employs a PCB based approach, utilizing current conducting traces in place of traditional windings for its moving mass, introducing many unique benefits. To begin, increasing the number of windings (traces) is effortless and does not negatively impact its SWaP characteristics. Furthermore, the drive circuity and power regulation electronics were integrated into the PCB during construction. Finally, it's slim form factor ensures the Halbach arrays are positioned in close proximity, vastly improving the field strength experienced by the PCB.

As the pole orientations of the modified Halbach array are incapable of being altered without adversely affecting its magnetic flux, the PCB was designed to appropriately incorporate both regions(sections A and B) to ensure ideal Laplace force generation. Therefore, alternating, current conducting traces were configured on an eight layer board in a spiral pattern. Fig. 3.4 showcases the PCB along with the direction of force achieved when current is introduced to the system. In particular, this pattern ensures that the current flows in opposing fashion in sections A and B, corresponding to the alternating pole orientations present in the array. Thus, the forces generated by each section sum together, essentially doubling the force constant of the actuator. Note, it is imperative that neither trace enters the opposing sections of the array, otherwise they would negatively affect the force output. Furthermore, the movement of the actuator is not affected by the force generated by the upper and lower traces of the coil as they terminate each other.

The fiberglass material of the PCB design is very thin in nature, typically 62 mils, while each trace on the board is a nominal 6 mil thick with 14 mil spacing between;

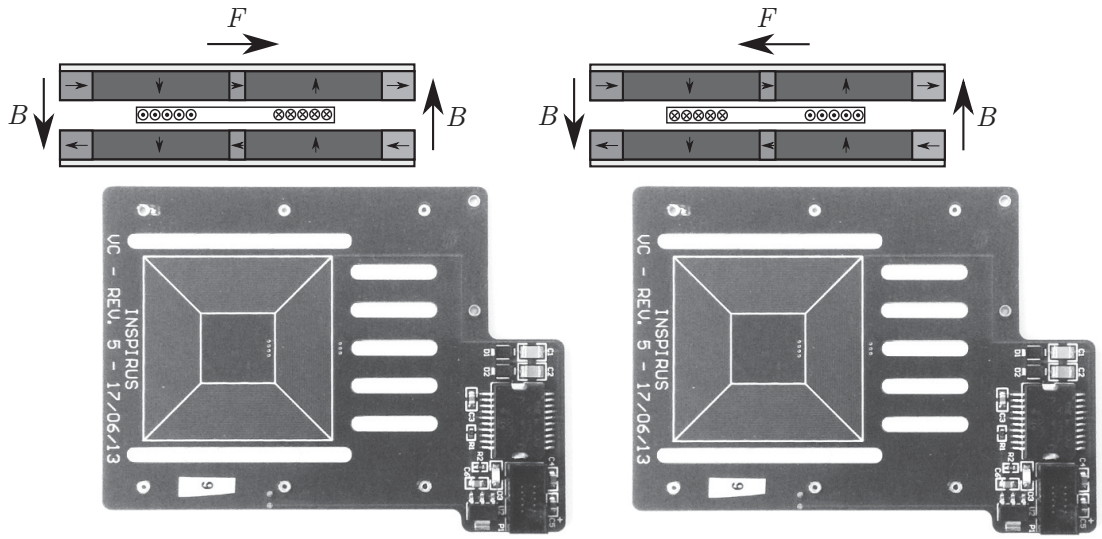


Figure 3.4: Eight layer PCB with current directions and resulting force generation.

tolerances specified by manufacturing. The design boasts an eight layer configuration containing 10.88 meters of current conducting trace, with a typical resistance of 20.44 Ω, in a tiny area of 2.62 square inches. However, as previously described, only half of this length, 5.44 meters, affects the force generated by the actuator. As displayed in Fig. 3.5, the constant has been experimentally determined to be approximately 6.9478 N/A, with a standard error of estimate equating to approximately 0.0625. The simple experiment consisted of increasing the load of the moving mass of the actuator and determining the current required to lift it.

3.2.3 Position Feedback System

In comparison to bulky position measuring devices including linear variable differential transformers (LVDTs) and linear encoders, a position sensitive detector is an optimal choice for VCAs. PSDs have many advantages compared to other displacement sensors, which include high resolution feedback, fast response time, simple operating circuits and are non-contact in design. Therefore, to achieve extremely precise feedback, a

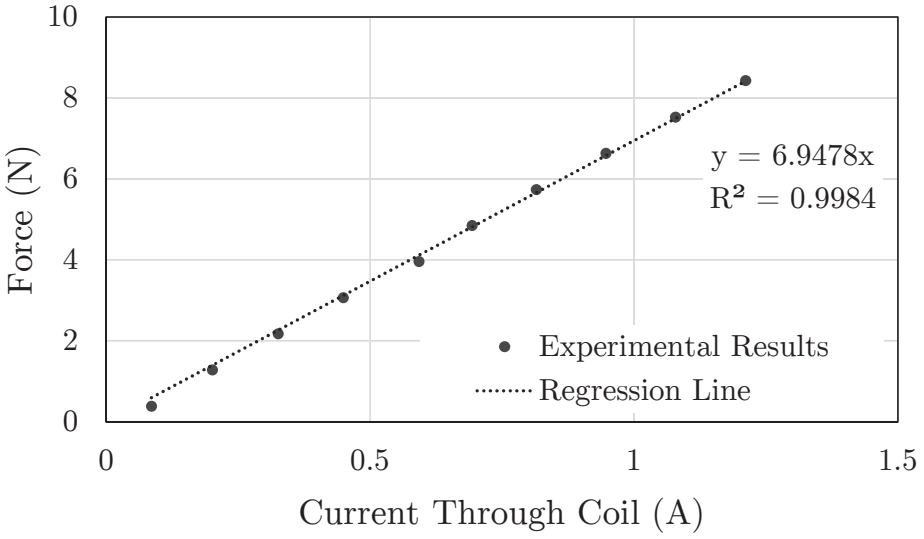


Figure 3.5: Experimental results of the force constant testing.

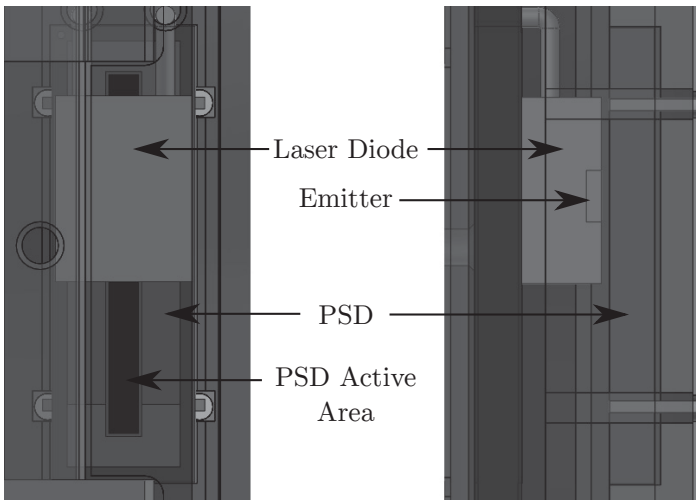


Figure 3.6: 3D model rendition of the PSD and VCSEL alignment.

one-dimensional (1D) PSD was used in conjunction with a vertical cavity surface emitting laser (VCSEL). In particular, the high resolution S3932 1D PSD [119], with an active area of 12 mm, and the OPV382 laser diode [120], capable of producing a high intensity light spot of less than 200 μm in diameter, were selected.

Unifying these two components, with signal conditioning circuitry, forms the foundation of the accurate, position sensing system. For ease of manufacturing and

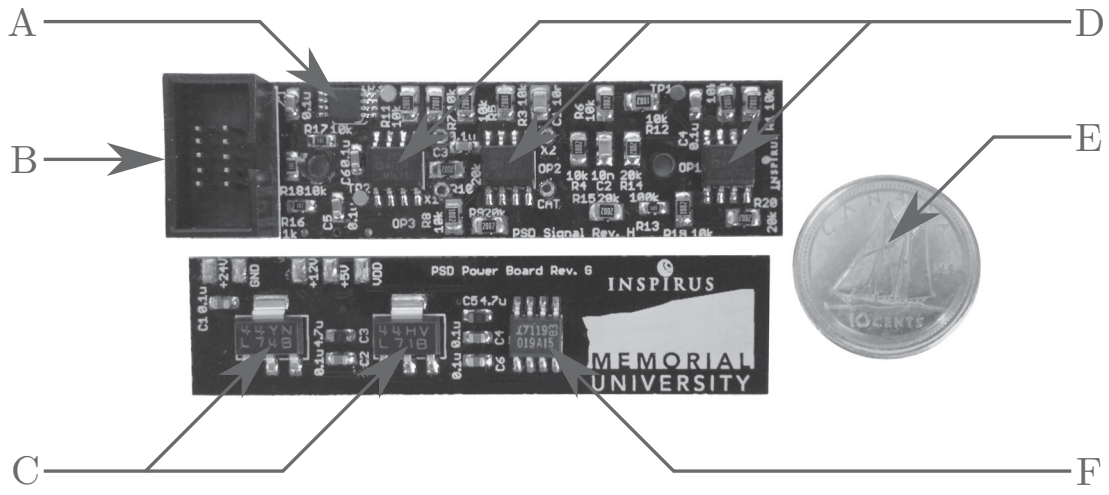


Figure 3.7: Physical realization of the signal conditioning electronics. A: 16-bit analog-to-digital converter. B: Ribbon cable connector. C: Power Regulation. D: Operational amplifiers. E: Canadian dime for size reference. F: Precision voltage reference.

design, the PSD was installed on the stator section of the actuator, while the diode was integrated within the confines of the moving mass. A 3D generated model of the alignment of the emitter with the PSD is highlighted in Fig. 3.6. To adhere to SWaP requirements, the signal conditioning circuit and the electronics providing regulated power to the coil were placed on separate circuits exhibited in Fig. 3.7. They are joined via multiple solder pads and held firmly in place by the body of the actuator.

When a light spot strikes the photosensitive surface of the PSD, two photocurrents are formed and driven through its two anodes, as shown in Fig. 3.8. Dictated by the uniform resistivity of its active surface, the PSD acts as a current divider with the magnitudes of the generated currents reliant upon the exact location of the light spot on the active region of the PSD. This distance is calculated using equation 3.2 [119],

$$x = \frac{L}{2}\frac{(I_2 - I_1)}{(I_1 + I_2)} \tag{3.2}$$

where x is the distance of the incident light from the center of the PSD, L is the

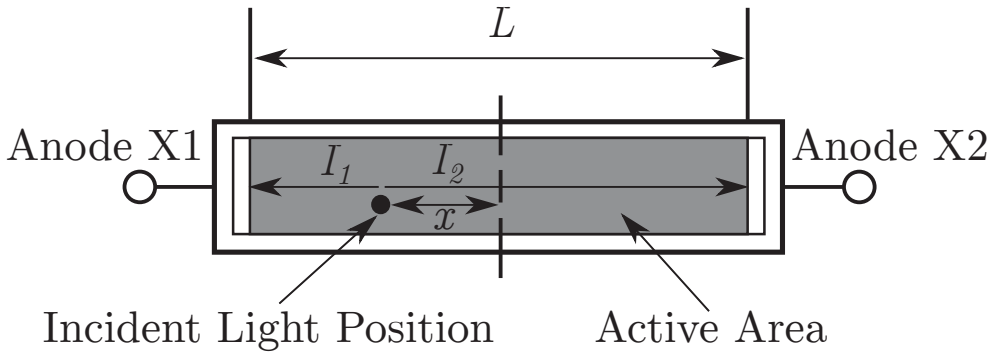


Figure 3.8: Incident light detection of a PSD.

length of the PSD's active area and I_1 and I_2 are the photocurrents through anodes one and two, respectively.

The calculation of equation 3.2 poses no issue for a digital computer or other computation device. However, the division operation is computationally expensive and may cause limitations in the speed of particular systems. While additional analog electronics can solve this issue, they may introduce noise and negatively impact the quickness of the circuit. As the sum of the photocurrents I_1 and I_2 are proportional to the quantity of light received by the PSD, it can be noted that keeping the incident light intensity consistent will in turn keep $I_1 + I_2$ constant. As shown in equation 3.3, this approach reduces 3.2 to a much simpler form, where L and the denominator are replaced by a constant K; the gain estimated by the calibration experiment described shortly.

$$x = K(I_2 - I_1) \tag{3.3}$$

By adopting an integral control strategy for the power output of the VCSEL diode, $I_1 + I_2$ will remain constant and equation 3.3 will hold true (see 3.2.5).

To garner a better understanding of its functionality, a step-by-step description of the inner workings of the feedback electronics is required. Furthermore, Fig. 3.9 highlights the topology of the overall signal conditioning circuit, providing a visual

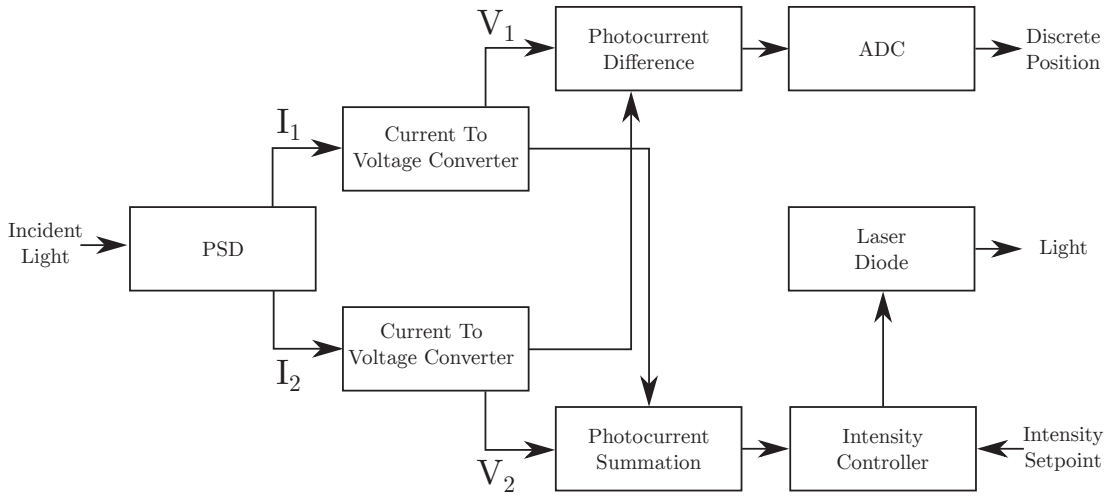


Figure 3.9: Topology of the signal conditioning circuit.

description of the system. The operation starts via the laser diode producing a focused beam which strikes the PSD's active region and generates two photocurrents, I_1 and I_2. These are swiftly transformed to their corresponding voltages, V_1 and V_2, by the current-to-voltage converters. Note, the first order filter composition of this circuitry introduces a time constant of 100 μs. Nonetheless, both voltages enter a non-inverting, differential amplifier which formulates their difference. The result is fed into the 16-bit analog-to-digital converter (ADC), digitizing the current position of the incident light spot. Furthermore, as previously detailed, the sum of V_1 and V_2 is calculated to ensure the power of the VCSEL diode remains constant via the integral control loop. To guarantee the operational amplifiers (op-amps) and ADC do not impose a bottleneck on the speed of the circuit, an op-amp (OP295 [121]) boasting a slew rate of 0.03 V/μs and an ADC (ADS8325 [122]) capable of sampling rates reaching 100 kHz were chosen.

Determining the precision of the feedback system is a necessity as it relates to a key performance metric of the VCA. The active area of the PSD is 12 mm, while the ADC incorporated into the position feedback circuitry transforms an input voltage into a

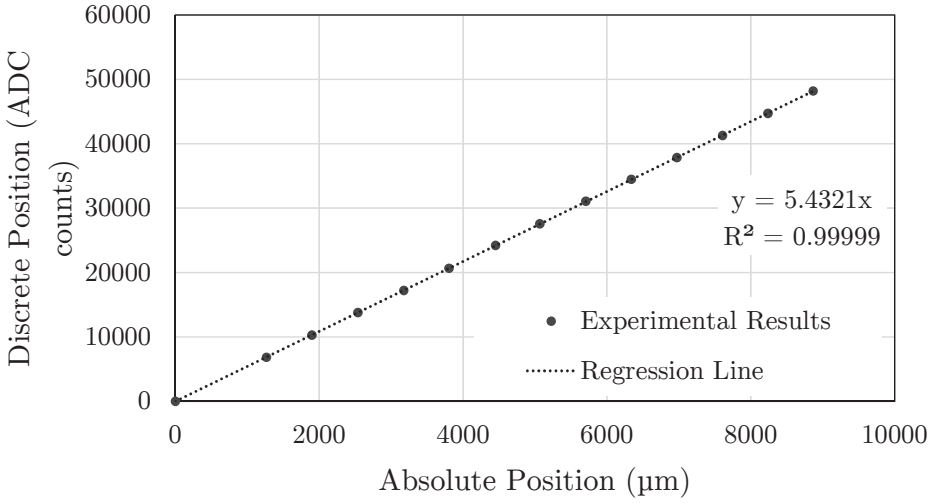


Figure 3.10: Experimental calibration data of the PSD relating discrete position to absolute.

16-bit discrete value. Therefore, the maximum theoretical resolution of the feedback system is calculated to be approximately 0.1831 μm per bit (ADC counts)(i.e., 12 mm/(2^{16}-1)). To determine its physical representation, the output of the circuitry was calibrated in conjunction with a precision linear gauge (LGF 0125L [123]) with a resolution of 0.1 μm. To conduct the experiment, the gauge provided the absolute position of the VCA, while the signal conditioning circuit generated the discrete quantification of its displacement. The data was gathered at a number of coil locations across approximately 9 mm of stroke distance. The total area (i.e., 12 mm) was not considered as manufacturing tolerances can cause the diode to be imperfectly mounted, resulting in the mid-stroke of the actuator not aligning with the midpoint of the PSD. Therefore, to avoid recording data which falls beyond the active area of the PSD, 1.5 mm on each side were not considered. Nonetheless, the values recorded were fitted with a simple, linear regression model to result in a resolution of approximately 5.431 ADC counts per micron (i.e., 0.1841 μm per bit), exhibited in Fig. 3.10. Note, the standard error of estimate was determined to be approximately 41.84. To minimize

the error in measurement, each position was sampled over 2,000 times, resulting in a worst case standard deviation of 2.723 ADC counts, or, ± 1 μm with a 95% confidence interval (CI).

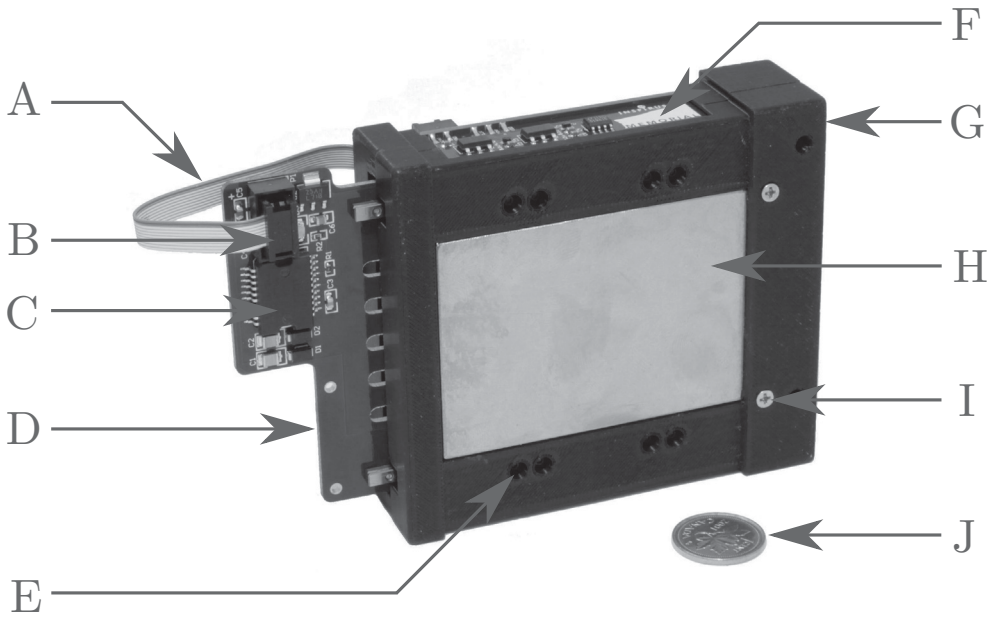
3.2.4 VCA Guidance and Housing

While actuating the moving mass, the VCA must exhibit accurate linear alignment while remaining near-frictionless to achieve high dynamics and precision. To ensure these conditions are delivered, off-the-shelf, ultra-miniature linear rails and ball bearing carriages were utilized. They provide a smooth displacement while maintaining a low profile, ensuring the VCA remains compact in design and stays within the confines of SWaP requirements.

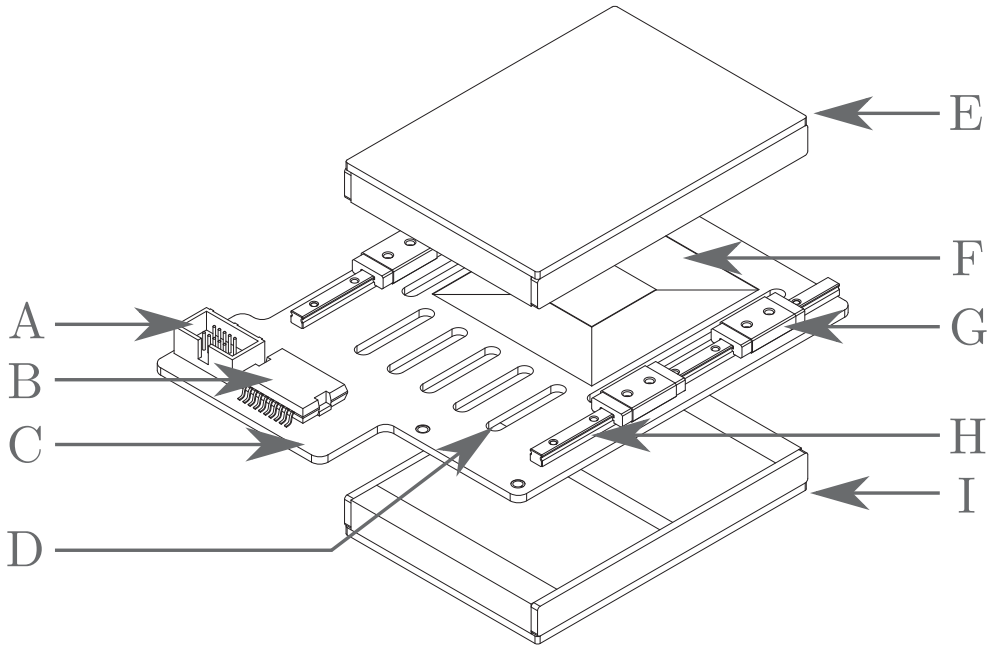
The VCA's stator is composed of two similar sections allowing for the effortless insertion of the modified Halbach arrays. In addition, it promotes simple fastening of the voice coil PCB, the carriages of the guidance system, the PSD and signal conditioning circuitry. To certify a lightweight, compact design, the housing was manufactured from polycarbonate-acrylonitrile butadiene styrene (PC-ABS) via a fused deposition modeling (FDM) machine. The two segments are held in place by the intense magnetic pull of the modified arrays. Furthermore, to withstand this compression, pillars were introduced to the top section for additional reinforcement. Its physical realization is displayed in Fig. 3.11a, followed by an exploded view of the actuator in Fig. 3.11b.

3.2.5 Experimentation and System Specifications

To validate the effect of the integral control circuitry on the signal conditioning electronics, an experimental study of both the open loop (i.e., no control) and closed



(a) Physical prototype of the novel VCA. A: Flexible ribbon cable for the transmission of power, data and control signals. B: Ribbon cable connector. C: Drive electronics. D: Voice coil PCB. E: Carriage fasteners. F: Signal conditioning PCBs. G: Magnet housing (VCA stator). H: Modified Halbach array. I: Fastening bolts. J: Canadian penny for size reference.



(b) Exploded view of the VCA assembly. A: Ribbon cable connector. B: Drive Electronics. C: Voice coil PCB. D: Removed section for pillars. E: Top Halbach array. F: Coil traces. G: Bearing carriages. H: Linear bearing rail. I: Bottom Halbach array.

Figure 3.11: Realization and exploded view of the novel VCA.

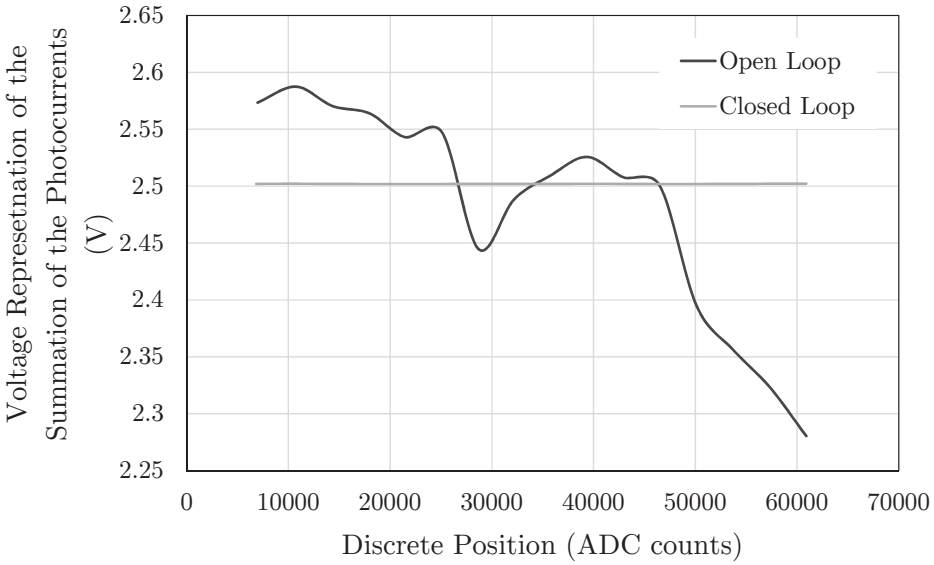
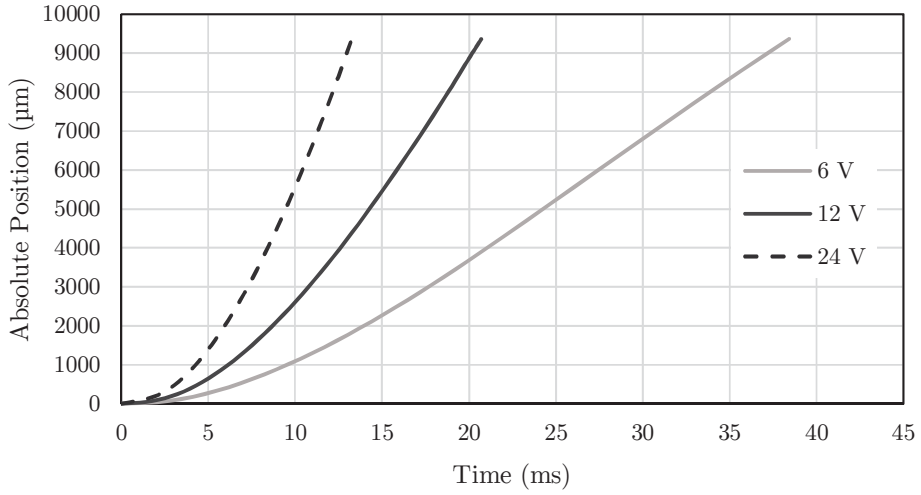


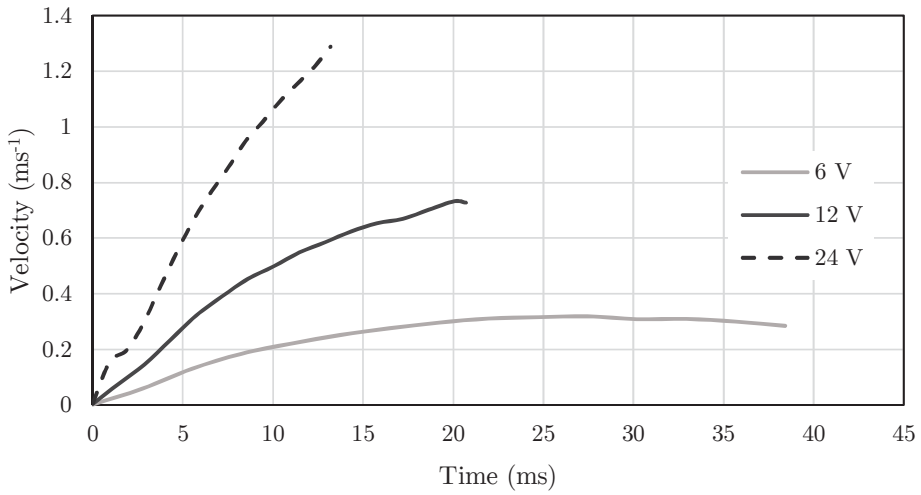
Figure 3.12: Performance validation of the signal conditioning circuit integral control loop.

loop (i.e., integral control) responses of the PSD were conducted. A dataset of 16 samples was recorded as a function of the discrete actuator position, versus the sum of the photocurrents in volts. To obtain the open loop control, a constant current was supplied to the VCSEL diode resulting in unfavorable fluctuations in the summation of the photocurrents. Conversely, the current-controlled diode performed significantly better with a minute standard deviation of approximately 93 μV. The results of the experimentation can be viewed in Fig. 3.12.

A performance metric pertaining to linear actuators is the open loop response to a step input at a variety of voltage magnitudes. Therefore, trials were conducted by exciting the drive electronics of the VCA at 6 V, 12 V and 24 V. At each voltage, the moving mass was accelerated against gravity with the position profile and velocity estimation recorded with respect to time. The experimental results are shown in Fig. 3.13. As detailed in the figures, the maximum velocity achieved was approximately 1.3 ms^{-1} for the 24 V step-input; indicating an impressive response for a short distance



(a) Absolute response of the VCA.



(b) Velocity estimation of the VCA.

Figure 3.13: Open loop responses of the VCA's moving mass against gravity at varying magnitudes.

with a low-voltage power source. Note, the average current draw of the VCA was found to be approximately 100 mA during normal operations.

In theory, if the VCA is displaced to a known discrete position, multiple times, its absolute location should remain consistent during each iteration. However, as a result of many factors including noise in the feedback circuitry, mechanical tolerances,

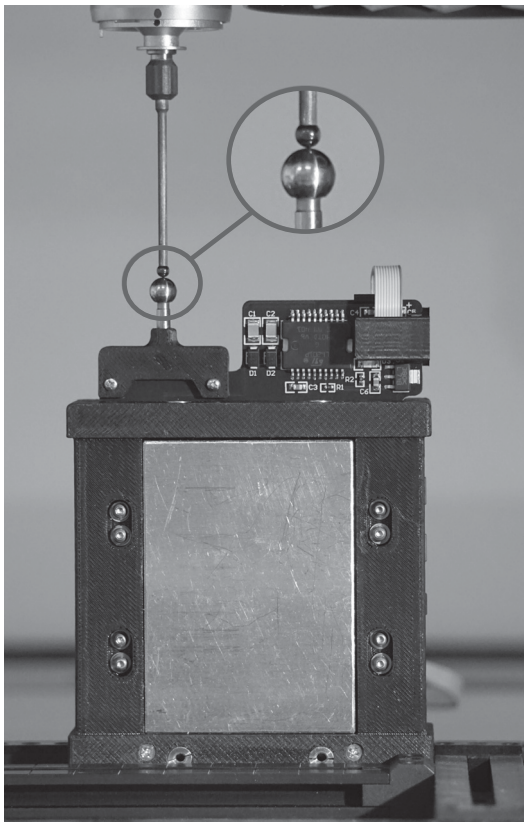


Figure 3.14: VCA repeatability experimental configuration.

thermal expansion and friction, the outcome may not be equivalent. Therefore, to obtain another performance parameter of the VCA, it is necessary to determine is repeatability characteristics. To categorize the repeatability of the linear motor, the variance, or standard deviation in the absolute position with respect to the identical discrete location can be utilized.

To discover this value, the coil assembly was firmly secured to a coordinate measuring machine (CMM) (Zeiss O-Inspect 442) as highlighted in Fig. 3.14. Upon fastening the mechanism, the moving mass was displaced to ten unique positions, covering a large section of the actuator's stroke. At each instance, within the calibrated workspace of the CMM, the x, y and z centerpoints of the $\frac{1}{4}$ inch, spherical tooling ball attached to the actuator were located and recorded. Note, the z coordinate was

Table 3.1: VCA repeatability results

Desired PSD Value (ADC counts)	PSD σ (ADC counts)	PSD σ (μm)	Absolute Position σ (μm)
5,000	4.69	0.86	4.40
11,111	4.77	0.88	3.91
17,222	5.90	1.09	4.18
23,333	5.89	1.08	3.67
29,444	6.03	1.11	4.11
35,556	5.51	1.01	3.14
41,667	5.12	0.94	2.51
47,778	3.74	0.69	3.27
53,889	2.15	0.40	2.75
60,000	1.18	0.22	3.05

the only value of importance as the VCA was accelerated in a linear fashion against gravity. To promote a varied dataset, the experiment was repeated five times in an up and down motion, resulting in 100 different points. The experimental outcomes of the trials are presented in Table 3.1.

As dictated by the high resolution of the PSD, the VCA cannot be controlled to absolute perfection at all times. Consequently, it did not settle at the exact discrete location during each experimental run. Therefore, the discrete position's standard deviation was logged to ensure it was not a cause of poor repeatability in the actuator. Converting the value into an absolute representation, resulted in an extremely low maximum deviation of approximately 1.11 μm, with the minimum equating to 0.22 μm. As indicated by the outcomes of the trial, inclusive to the slight variation in the discrete position, the worst case repeatability of the actuator resulted in a standard deviation of 4.40 microns, with a 95% CI range of $\pm$2.726 μm.

During the initial stage of repeatability testing, it was determined that the first set of experimental runs resulted in the data points being marginally higher (i.e., a maximum of two microns) than the values of the subsequent trials. It was identified to be the consequence of thermal expansion, as the temperature of the PCB increased

Table 3.2: Novel VCA specifications

Parameter	Value
Height (fully retracted) (mm)	113.97
Stroke (mm)	12 (nominal)
Width (mm)	82.80
Depth (mm)	25.40
Total mass (g)	520
Moving mass (g)	33
Positioning accuracy (μm)	$\pm$2.726 (95% C.I.)
Force constant (N/A)	6.9478
Back EMF constant (V-s/m)	6.9478
Static friction coefficient	0.500
Magnetic flux density (T)	0.704 (typical)
Coil resistance (Ω)	20.44 (typical)
Coil inductance (mH)	1.27 (typical)

while the drive electronics actuated the moving mass. Thus, additional testing was conducted to validate the repeatability at elevated temperatures.

Given that the PCB is located within the actuator assembly (i.e., between the Halbach arrays), it is problematic to heat through traditional means. Therefore, its temperature was raised by forcing the VCA to displace to an unreachable position (i.e., outside the bounds of the PSD active area), supplying the coil with high current, increasing its temperature through power dissipation. The system was left to endure until the VCA reached a minimum of 40 degrees Celsius. Upon, achieving the value, the tests were conducted in the same manner as before. However, prior to each movement the actuator was re-heated to ensure the temperature was consistently greater than its 40 degree restriction.

The outcomes of the trial determined that the absolute location of the moving mass increased by 29.8 μm in comparison to the original repeatability experiments. To ensure this was not a random occurrence, the test was completed once more and presented an average increase of 30.4 μm; a 0.6 micron difference from the first experiment. The variation in likely the result of the thermal expansion of the PCB and

PC-ABS of the housing. However, it was identified that upon reaching a steady-state temperature, the repeatability of the VCA remains on par with that of the initial results with a standard deviation of 5.50 microns. Finally, with a variety of experiments completed, Table 3.2 displays many of the key characteristics and performance metrics of the novel voice coil actuator.

3.3 Parallel Orientation Manipulators - Applications of the Novel Voice Coil

Parallel kinematic mechanisms are an assembly of links connected to a mobile platform, which is capable of providing desired displacement patterns. The platform experiences a number of degrees of freedom (DOF) proportional to the number of non-redundant actuators composing its design. Furthermore, when referring to PKMs which solely involve rotational motion, they can be more specifically referred to as a parallel orientation manipulators [39].

POMs have existed in industry for many years and are used in a vast selection of applications. In particular, systems utilized for optomechatronic purposes such as visual tracking, sense and avoidance, active vision and vibration isolation [37, 38]. When designing small-scale POMs for optomechatronic appplications, the actuators driving the mobile platform must be highly responsive, extremely accurate and compact. Unfortunately, commercially available linear motors often fall short of these requirements. However, the novel voice coil is an optimal fit for employment in POM technology. Therefore, to exploit the VCA's speed and precision, two distinct POM designs were pursued; one exhibiting 3DOF, while the other 2DOF. As these mechanisms were the result of an outside study [39], only a brief description and

notable characteristics of each POM will be discussed to validate the ideal candidate for the ATM.

3.3.1 POM Architectures

While there are an adbundance of configurations which can results in a 3DOF POM [124–126], considering the POM's utilization for optomechatronic applications, the 3-PSS/S was selected due to its compact design. Note, the P and S refer to prismatic (linear) and spherical (rotation) motions of the joints respectively. The kinematic structure, or truss model, and its three-dimensional (3D) computer aided design (CAD) representation are displayed in Fig. 3.15. The limbs A_iB_i correspond to the actuated prismatic joints while B_iC_i are intermediate links connecting the linear actuators to the mobile platform defined by $C_1C_2C_3$. The platform is attached to spherical joint O, which restricts its motion, resulting in tilt (roll), azimuth (pitch) and torsion (yaw) angular orientations. However, torsional rotation is not essential in many applications, especially those when the payload of the platform is axis symmetric (i.e., a laser device). Therefore, a torsion restricted, 2DOF POM was researched to minimize the number of actuators and thus reduce the weight, size and power requirements of the mechanism, boosting SWaP characteristics.

Though there are many examples of 2DOF orientation manipulators [112, 127–129], the 2-PSS/U, with U corresponding to a universal joint, configuration was ultimately selected as it most closely resembles the 3-PSS/S. Similar to the 3DOF mechanism, the kinematic representation of the torsion restriction variant is shown in Fig. 3.16 [39]. Links A_iB_i refer to the linear actuated limbs, mirroring the 3DOF structure. Similarly, the spherical joints B_i and C_i form the link between the prismatic joints and mobile platform, or link C_1C_2. However, the universal joint has been reconfigured into two

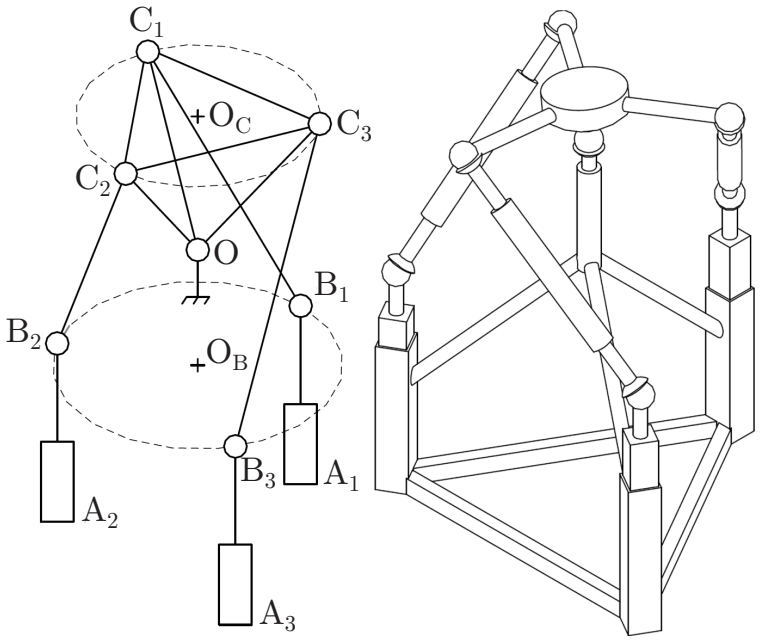


Figure 3.15: 3-PSS/S kinematic structure (left) and CAD representation (right).

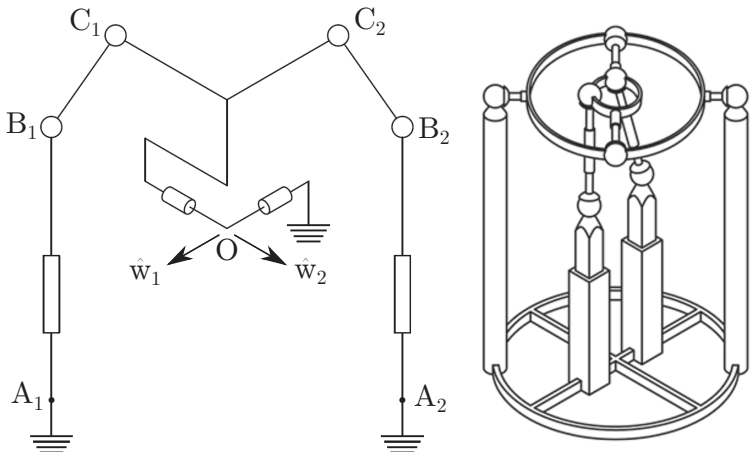


Figure 3.16: 2-PSS/U kinematic structure (left) and CAD representation (right).

revolute joints, $\hat{\mathbf{w}}_1$ and $\hat{\mathbf{w}}_2$, whose axes are perpendicular and intersect at point O.

While the 3DOF model closely resembles that of its kinematic structure, the 2DOF varies greatly as the revolute joints are designed to be ring-like in nature, due to its geometry. This design promotes a significantly less coupled system than the 3DOF, resulting in a nearly one-to-one relationship with respect to each actuator location

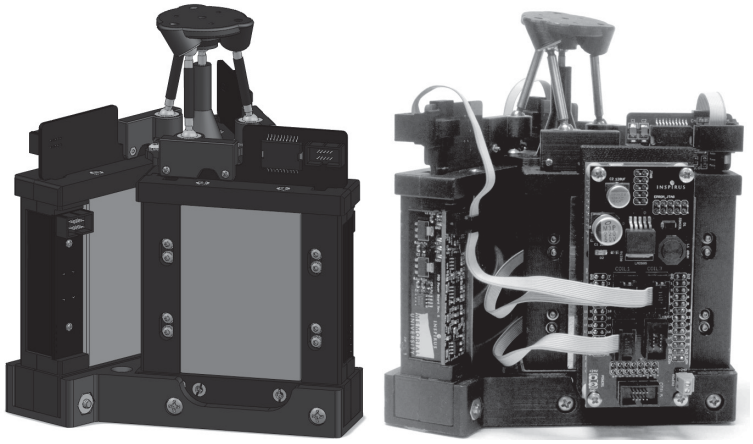


Figure 3.17: CAD Model (left) and physical realization (right) of the 3DOF POM.

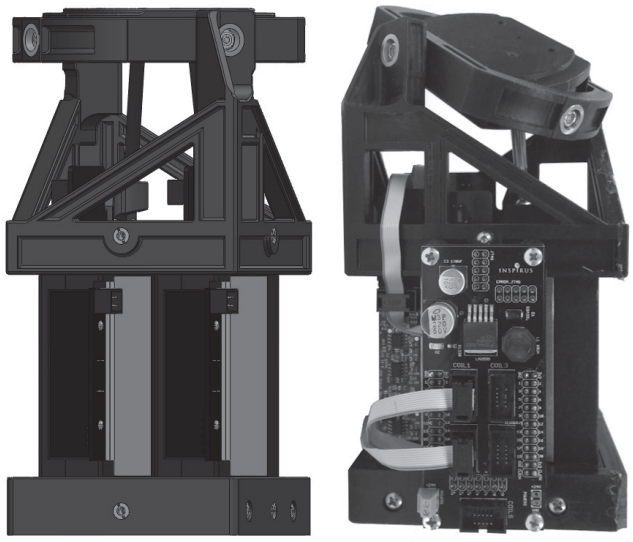


Figure 3.18: CAD Model (left) and physical realization (right) of the 2DOF POM.

and the tilt and azimuth angles.

Before physical construction commenced, well-defined, 3D models of both the POMs were implemented using SolidWorks CAD software to provide early visualization of the systems, as well as perform preliminary testing. The finalized CAD models alongside their physical realization are shown in Fig. 3.17 and 3.18.

3.3.2 POM Experimentation and Specifications

While there are a wide varitey of characteristics relating to each POM structure, a few performance metrics were selected to highlight the major variations in each architecture and to formulate a descision on the most viable configuration for employment in the ATM. The first parameter under consideration is the regular workspace of the mobile platform for both the 3DOF and 2DOF renditions. A POM's reachable workspace is the set of orientations which the moving platform can realize without violating any physical constraint (e.g., motion range of the joints, interference of links, etc.). However, the regular workspace of a POM is defined by the maximal geometric object (e.g., cube, sphere, etc.) that can be completely contained within the reachable workspace [130]. This is more often used to evaluate the angular range of a mobile platform. While each of the architectures performs very well, the 3DOF mechanism achieved slightly better results with a maximum angular tilt of 32 degrees as opposed to the 26 degrees of the 2DOF [39].

Another key metric is the repeatability of each system, which now encompasses potential error in the voice coil and any misalignment, tolerances and manufacturing issues relating to the kinematic links and the mobile platform. To determine this parameter for each mechanism, trials were conducted in similar fashion to the VCA investigation, with examples of the testing apparatus shown in Fig. 3.19.

However, to define an orientation in 3D space, a minimum of three points are required as opposed to the single required by the VCA. Thus, a mobile platform with three tooling balls was constructed and attached to each POM (Fig. 3.19). The experimentation consisted of orienting the test platform to 10 unique locations and repeating these motions five times to create a varied dataset. Furthermore, nine measurements were evaluated by the CMM (i.e., the x, y and z coordinates of each

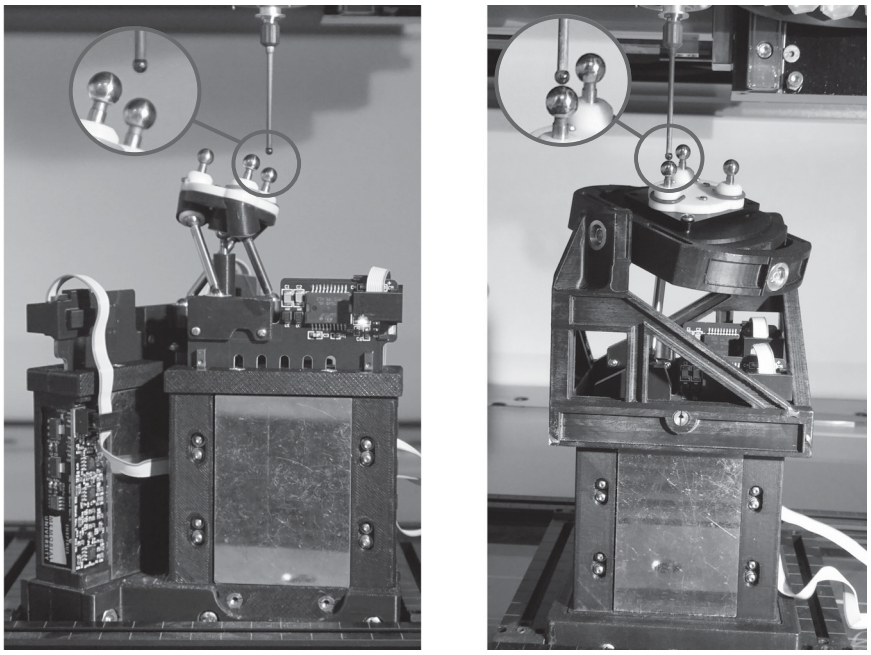


Figure 3.19: 3DOF (left) and 2DOF (right) POM repeatability experimental configurations.

ball) resulting in 450 locations to consider for each POM. Upon concluding the trials, the maximum standard deviation was formulated to be approximately 35.4 μm for the 3DOF mechanism, while the 2DOF resulted in a poorer outcome of 76.7 μm. The increased deviation found in the repeatability of the POMs, is likely due to the aforementioned tolerance issues. This is more prominent in the 2DOF rendition as its mobile platform contains more complex components. While these values are higher than the reported 4.4 μm of the VCA, they are quite impressive, especially for prototype mechanisms with many interconnecting links.

Finally, Table 3.3 denotes a number of key characteristics to consider when determining the ideal mechanism to be employed in the ATM. As indicated, the height of the 2DOF is greater in comparison with the 3DOF, primarily in relation to its mobile platform. Additionally, due to the removable of one actuator, the 2DOF dynamics has been negatively affected, reducing the overall agility of the mechanism. However, this results in the width, depth and weight being reduced significantly, which is extremely

Table 3.3: 3DOF and 2DOF POM specifications

Parameter	3DOF	2DOF
Width (mm)	136.7	97.3
Depth (mm)	136.7	79.8
Height (mm)	147.7	175.5
Weight (kg)	1.71	1.27
Max Angle (deg)	32	26
Typical Azimuth Speed (deg/sec)	1,500	1,000
Typical Tilt Speed (deg/sec)	1,500	800
Typical Torsion Speed (deg/sec)	1,000	-

critical for many optomechatronic applications as they generally invoke strict SWaP requirements. Therefore, with SWaP conditions being a priority and the outcomes detailed in Chapter 7, the 2DOF was ultimately selected as the optimal candidate for the ATM.

3.4 Conclusions

While pursing optomechatronic applications, a uniquely designed, highly dynamic, novel voice coil actuator has been constructed. The redesigned VCA package is lightweight and compact in comparison to traditional, off-the-shelf models while incorporating a miniature guidance system and high resolution positioning electronics. These unite to generate a VCA with low friction capabilities and extreme precision. Furthermore, the integrated coil is capable of producing an impressive force constant and large peak velocities. Utilizing the performance of the actuator, 3-PSS/S and 2-PSS/U POMs were developed. Both of these devices have the capacity of highly dynamic, precise orientation of a mobile platform and its payload. As a result of parameter identification, the 2DOF structure was chosen as the candidate architecture for employment in the ATM.

Chapter 4

Hardware-Based Controller Classification for Highly Dynamic Mechanisms

Creating a system capable of delivering adequate control to the extremely dynamic novel VCA is not a trivial matter. While the classic PID control architecture has many applications in mechatronics, its simple nature prevents it from providing precise control to agile mechanisms. In addition, the response rates of traditional, high-level programming languages are unable to cope with the maneuverability of the VCA. Therefore, a cascade PID-PID scheme was constructed in VHDL in hopes of remedying both of these issues. To ensure its place as a suitable candidate, the cascade system is compared not only to a hardware based PID loop, but the more powerful and complex ADRC. In order to evaluate the performance of each architecture a number of control parameters were chosen to quantify their response. Correspondingly, the logging of these parameters for multiple test cases was completed on each controller in is optimally tuned state. The final results concluded that while the ADRC was superior to both PID varieties, the cascade PID-PID performed extremely well for many scenarios, while consuming fewer hardware resources and providing less complex tuning conditions.

4.1 Introduction

Due to the high dynamics resulting from the novel VCA, developing a control architecture capable of generating precise actuation is not a simple exercise. Though the classic PID control scheme has been integrated into a plethora of mechatronic systems [18, 40, 41, p. 43], it's more simplistic nature inhibits its ability to provide accurate control to systems with great agility. In addition, the processing capabilities (i.e., update rates) of high-level programming languages are unable to adequately manage the quick maneuvers of the VCA. In response, a hardware-based cascade PID-PID scheme was theorized as a suitable candidate to grant a solution to both of these issues. To ensure its position as a capable controller for the novel VCA, the cascade system was compared not only to the hardware PID controller but to the powerful and complex ADRC. This algorithm has proven itself extremely effective, though its convoluted tuning conditions make fine-tuning problematic [19].

In order to evaluate the performance of each architecture, a number of metrics were selected to quantify the effectiveness of each steady state response in reaction to a step input. Correspondingly, the attributes were recorded from multiple experiments upon placing each controller in its optimally tuned state. The three most notable and commonly explained characteristics when rating the control of linear mechanisms are the amount of time required to reach its desired position, the output's long-term precision in absence of large oscillations and the measure of overshoot (undershoot) present in the transient response. These are generally referred to as settling time, steady state error and percent overshoot, respectively.

To obtain quantifiable conclusions on the capabilities of each controller, the parameters were numerically defined. In particular, the settling time was deemed as the time required for the response to come within two percent of the steady state

value and remain within this limit. Steady state error is simply the absolute difference between the settled and input positions. Finally, the percent overshoot is the highest (or lowest while the VCA is retracing) position achieved, divided by the setpoint. Experimental validation was undertaken by varying the moving mass of the actuator while exciting the voice coil to 100 unique positions for each control architecture.

4.2 Discrete Implementation of a VCA Control System

As aforementioned, the run time, or update rate, of the control procedure for the novel coil system must be considerable in order to maintain sufficient control of its agile design. Therefore, constructing a controller using HDL was critical as algorithms devised in hardware languages (i.e., VHDL, Verilog) are remarkably swift in contrast to high-level languages such as C#. Furthermore, as digitally designed code may be fitted onto an FGPA, additional benefits ensue. These are inclusive to its miniature size in comparison with traditional computing systems, its ability to run algorithms in parallel, its versatility and its exceptionally low power requirements [131], fulfilling the SWaP conditions set by the VCA. However, conceiving algorithms in VHDL is complex in contrast to high-level design as it involves register level modification and lacks access to functionally exploited by high-level code. Nonetheless, a PID control scheme was fashioned in VHDL, while taking advantage of the FPGA hardware.

Chapter 3 detailed a novel voice coil actuator and its performance metrics, but lacked any mention of control functionality. In response, the hardware architecture found in Fig. 4.1 highlights the presence of a control method in the actuation of the VCA. Correspondingly, the system identified as “control scheme” may be replaced

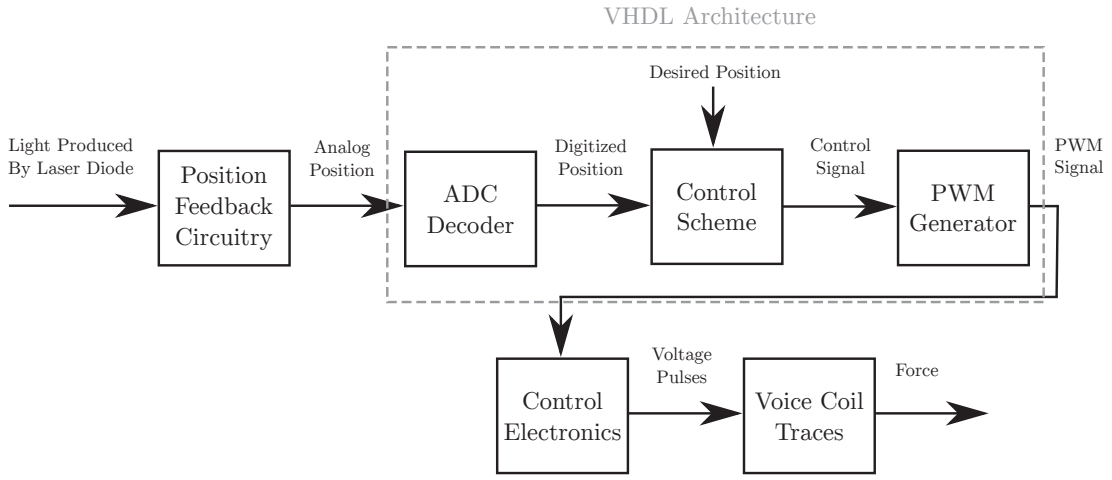


Figure 4.1: VCA topology with control scheme present.

by any of the aforementioned controllers (i.e., PID, cascade PID-PID, etc.). The architecture is also inclusive of analog to digital decoding and pulse width modulation (PWM) algorithms. Therefore, a systematic description of the actuation of the VCA's moving mass is summarized as follows:

- Light generated by the laser diode is converted by the feedback circuitry resulting in an analog representation of the actuator's position.

- The absolute location is decoded by a 16-bit ADC and digitally logged in VHDL.

- This discrete position is subtracted from the desired setpoint and is managed by the control loop, producing a control signal.

- The signal enters the PWM generator, transforming it into a series of pulses which are handled by the drive electronics, ultimately forcing the actuator to the desired location.

4.3 Digital PID Controller

4.3.1 PID Controller Fundamentals

To detail the workings of a cascade PID-PID control method, the fundamentals forming the PID controller must be initially discussed. As previously indicated, the development and implementation of PID control systems are abundant in literature and industry alike. These controllers are relatively simple to create and meet the standards of many mechanical and electical systems. Furthermore, they are defined by their control parameters (i.e, gains): proportional, integral and derivative, each of which must be adjusted precisely in order to obtain optimal performance [132].

The performance of a control procedure can be expressed in the characteristics of its transient response; specifically, settling time, steady-state error and percent overshoot. With respect to the PID algorithm, these conditions are significantly affected by the proportional, integral and derivative gains. Thus, in many cases, a system comprised of an individual gain has little worth as generally, the combination of the three gains result in ideal execution. Since each gain has a very specific impact on the response of a system, a straightforward demonstration of these effects can be achieved by introducing a simple step input into the controller and measuring its transient response. A block diagram representation of a generic PID controller layout is illustrated in Fig. 4.2.

The general workings of a PID are rather simplistic in design which is beneficial as it leads to shortened development cycles. The equation pertaining to a PID controller which ultimately defines the PWM signal is seen in equation 4.1,

$$u(t) = k_p e(t) + k_i \int_0^t e(\tau)d\tau + k_d \frac{de(t)}{dt} \tag{4.1}$$

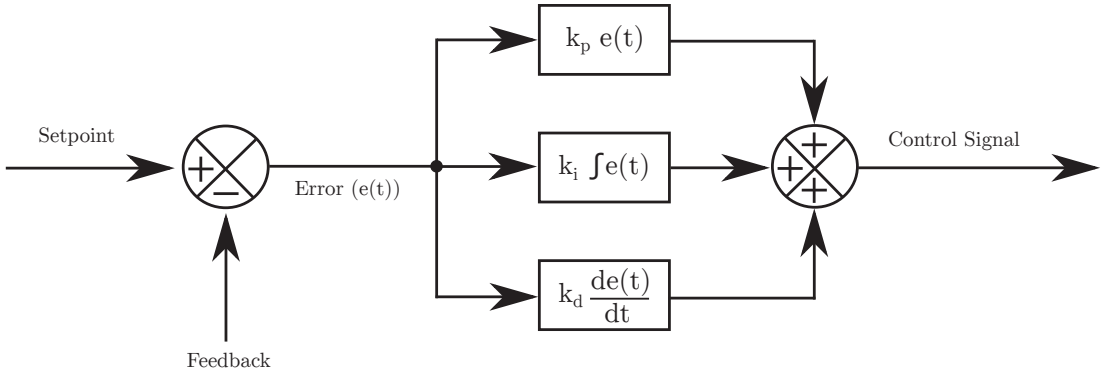


Figure 4.2: Generic PID control structure.

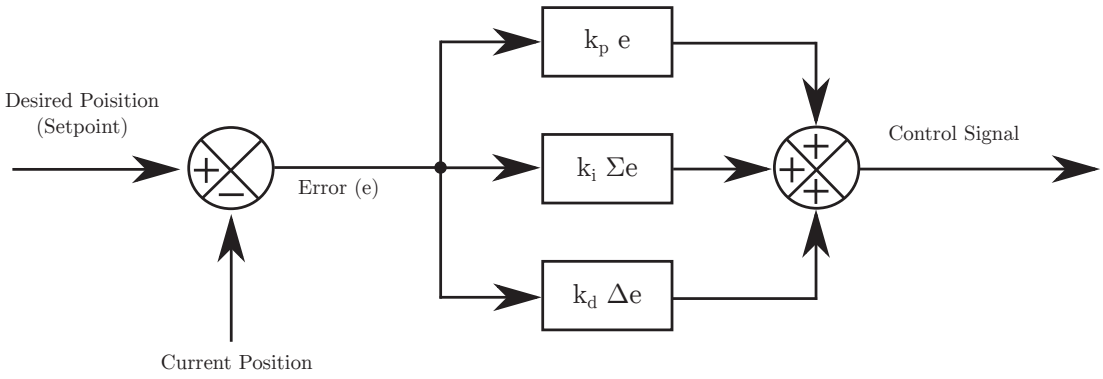


Figure 4.3: PID control architecture reconfigured for hardware development.

where k_p is the proportional gain (P gain), k_i the integral gain (I gain), k_d the derivative gain (D gain) and $e(t)$ is the error. However, for a minute sample time, the equation can simplified by replacing the integral and derivative components with summation and difference renditions giving rise to the configuration shown in Fig. 4.3. The representation of this architecture, equation 4.2, is straightforward to implement in VHDL and reduces hardware resource costs due to the removal of the complex mathematics. Note, to prevent integral windup, the integral term is limited by upper and lower bounds.

$$u(t) = k_p e(t) + k_i \sum_{i=1}^{t} e(t) + k_d(e(t) - e(t-1)) \tag{4.2}$$

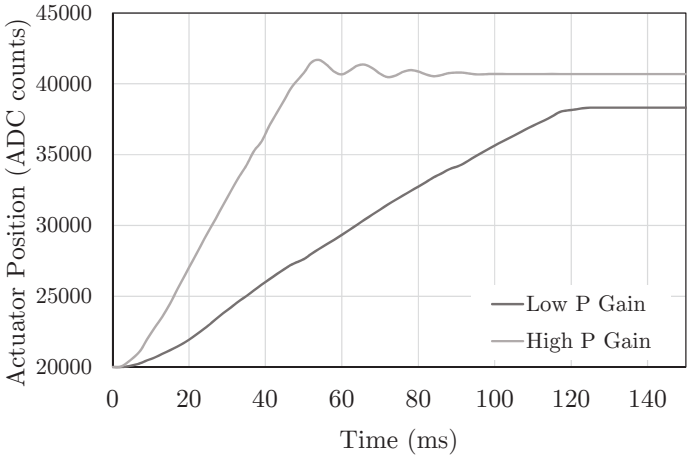


Figure 4.4: The proportional gain effect's on the step response of the novel VCA.

4.3.2 Gains and Their Effect on the Transient Response

The proportional term (i.e., $k_p e(t)$) can be regarded as the most important factor in the control scheme as it generally contributes to the greatest change in the system's transient response. It is a rudimentary term to calculate; a simplistic multiplication of the proportional gain with the current error found within the routine. Fig. 4.4 highlights the effect of P gain on the response of the VCA. This profile is generated from a step input of 20,000 ADC counts, with the discrete location of the VCA resting at 20,000 counts and being actuated to 40,000. To promote consistency, each test will adhere to these guidelines.

It can be seen that for a small proportional gain, the output of the system is lacking adequate control and starting from 20,000 ADC counts, it does not achieve the intended step input (i.e., 40,000 ADC counts), leading to a less sensitive system, referred to as overdamped. At an increased P gain, the rise time improves but at the cost of generating overshoot in addition to oscillations creating instability in the signal. This particular response to a step input is known as a underdamped system. To produce an optimal transient waveform (i.e., critically damped), additional gains

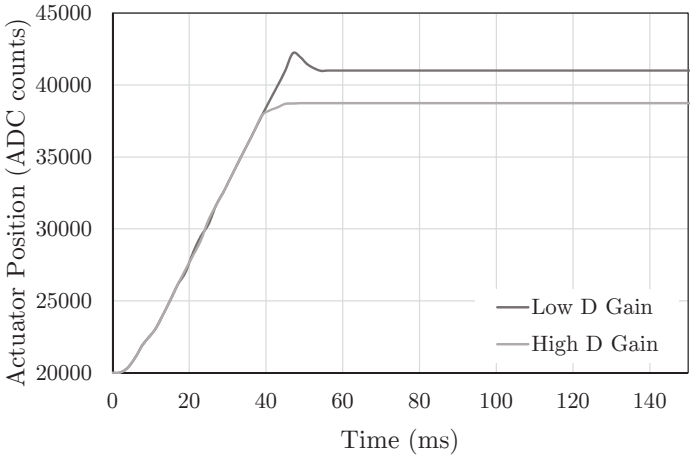


Figure 4.5: VCA response to high and low derivative gain values.

must be introduced to the control architecture.

Generally, overshoot and oscillations can be corrected by incorporating a derivative term (i.e., $k_d(e(t)-e(t-1))$ to the control method. This term is derived by subtracting the current error with the error of the previous state and dividing the outcome by the time required for state transition. However, in hardware design, the time may be disregarded as the term is simply formulated at each instance the loop is updated. Furthermore, the efficiency of the derivative term can be increased by calculating the differences of more than one previous state and applying the result. Nonetheless, it is multiplied by the derivative gain and added to the output of the controller. Freezing the proportional gain at a higher value and adjusting the D gain, the ensuing transient responses are viewed in Fig. 4.5.

As shown, the term is primarily used to stabilize the output. Most notably, the overshoot incurred by the single proportional term is significantly reduced while the derivative term is active. However, at higher gains, the response is unable to reach the setpoint, increasing the steady-error while decreasing response time; once again resulting in an overdamped system. Therefore, an extra term must be factored into

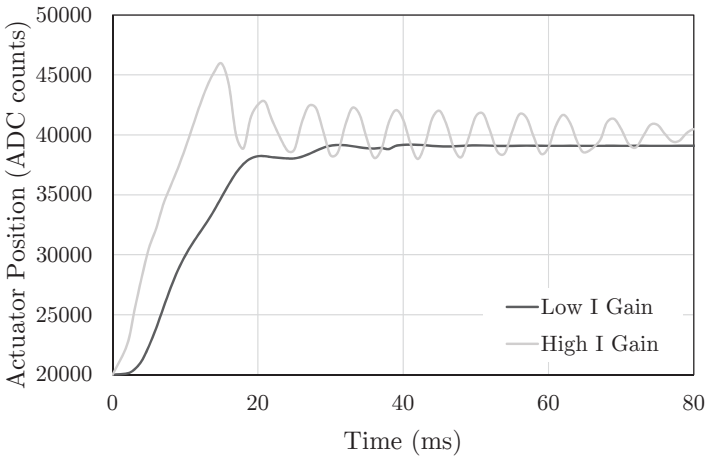


Figure 4.6: Transient response of the VCA to varying integral gains.

the control loop to provide a solution to these issues.

The integral term in a PID system exists to add long-term precision to a control signal by storing the previous states of the system (i.e., a summation of the error over time). The accumulation of error is multiplied by the integral gain and summed with the other two terms, allowing for the rectification of small errors in the response. Keeping the P gain and D gain consistent, large and small I gains were introduced to the control method and displayed in Fig. 4.6.

The figure indicates that the inclusion of high integral gain reduces stability of a control loop by introducing small, ongoing oscillations. While not visible in Fig. 4.6, the integral term is capable of causing increasing oscillations resulting in a signal which never fully settles. In contrast, providing the scheme with a low I gain results in a oddly formed, slow-to-rise, rough transition from rest to steady state.

To ensure the system responds optimally, summing all three terms and correctly adjusting each gain is obligatory. While tuning can be achieved via simple trial and error, the Ziegler-Nichols technique is a robust procedure which allows for the determination of starting values for the gains (in some cases, reaching optimal values)

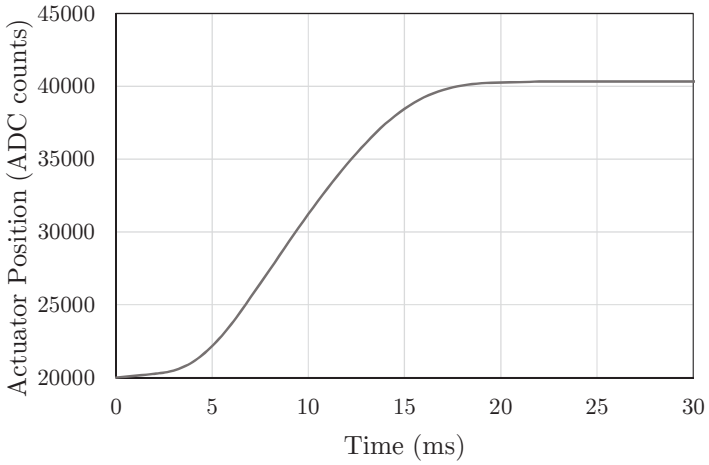


Figure 4.7: VCA transient response to an optimally tuned hardware-based PID controller.

[133]. This exercise promotes a step-by-step process which reliably determines the optimal gains of a particular system. Utilizing its functionally, favorable gains were selected, realizing a critically damped response of the tuned PID controller (Fig. 4.7). The PID algorithm, operating at a rate of 1 MHz, does generate an idealistic transient motion with a relatively small steady-state error of $\approx$ 300 ADC counts (55 μm). However, the controller has been tuned specifically for this particular transition and as a result, other motions do not generate transient responses nearly as precise. Section 4.6 details a more in-depth discussion corresponding to the PID controller's functionality for use with the novel VCA.

4.4 Hardware-Based Cascade PID-PID Control Architecture

While the initial findings of the optimally tuned PID controller seemed promising, the results dictated from additional testing proved otherwise (section 4.6). Thus, to fulfill the requirements of a nominal control system employed in conjunction with the VCA,

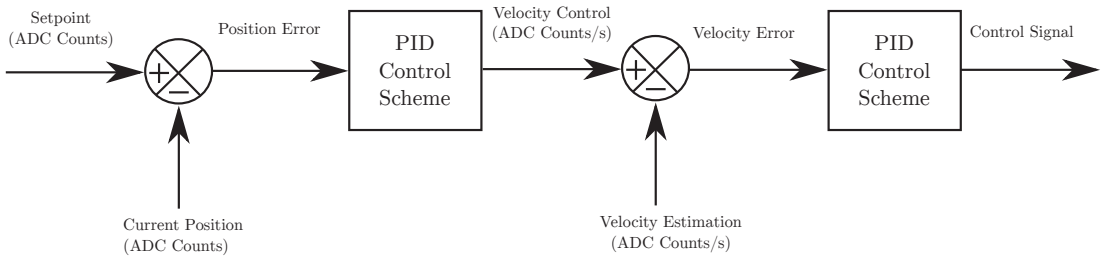
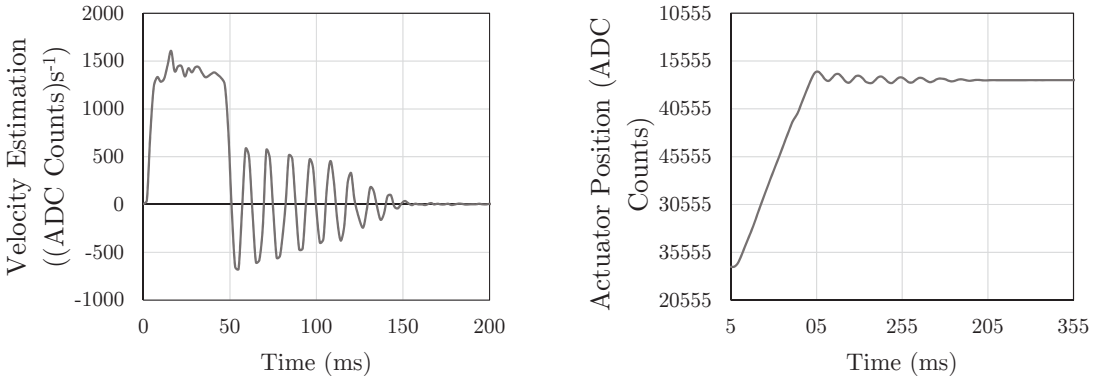


Figure 4.8: Topology of the cascade PID-PID control system.

a more advanced algorithm was pursued. A distinct advantage of PID control is the ability to cascade multiple PID loops comprised of the same architecture to yield a more satisfactory dynamic performance. In this layout, an outer (master) PID loop affects the output of the inner (slave) loop by generating a control signal and assigning it as the setpoint. In general, the outer loop rectifies the primary control parameter under consideration (i.e., discrete position) while the inner loop is responsible for the correction of faster changing conditions such as velocity or acceleration.

Achieving such a structure ensures disturbances are easily remedied and non-linearity is more readily compensated for, as position and velocity information is applied to the algorithm. In addition, it is of utmost importance that the inner loop runs three to four times faster than that of the outer, to ensure the slave has ample time to correct for disturbances before affecting the master loop. In this case, the outer loop updates at a rate of 1 MHz while the inner is set to run at 4 MHz. Fig. 4.8 represents the topology of a cascade PID-PID control architecture for implementing position control of the VCA. As highlighted, to provide adequate control of the linear motor's location, the PID-PID system requires both position and velocity data. Though the digital representation of the absolute position of the VCA is obtained by the position feedback system previously discussed (Chapter 3), velocity information is unaccounted for.

Though there are many readily available sensors capable of velocity measurement,



(a) Velocity estimation of the cascade PID-PID controller for fast (aggressively tuned) motion.

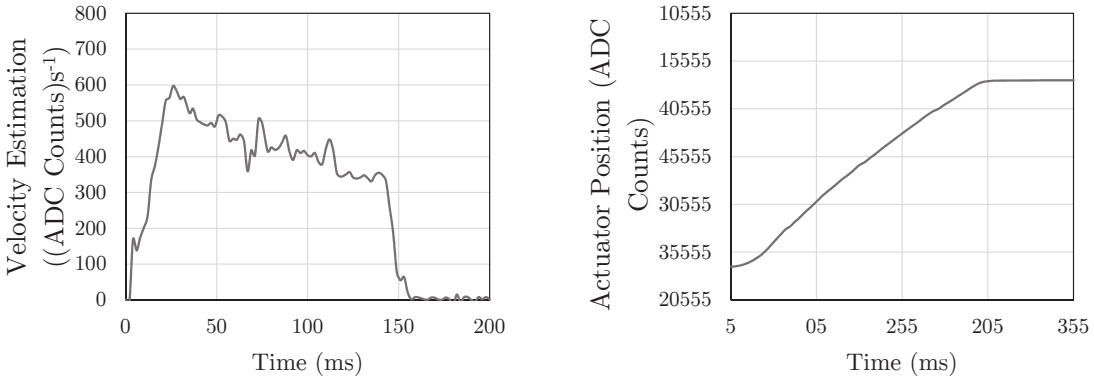
(b) Discrete position relating to the estimated velocity for reference.

Figure 4.9: Velocity estimation during the actuation of the VCA for agile displacement.

the inclusion of either device would negatively effect the SWaP characteristics of the already development VCA. Thus, without the use of a sensing device, the absolute velocity data must be estimated by numerical methods. While velocity can simply be determined by taking the difference of two position values over a set period of time, this generally leads to inaccuracies. Therefore, the five-point stencil numerical differentiation algorithm was implemented to determine the finite difference approximation of the derivative of the position (equation 4.3).

$$f'(x) \approx \frac{-f(x+2h) + 8f(x+h) - 8f(x-h) + f(x-2h)}{12h} \tag{4.3}$$

For the scenario in question, x is the discrete position data while h is the time between each sample, in this case approximately 4.17 μs (i.e., 241 kHz) as dictated by the update rate of discrete coil position. However, to limit the amount of resources consumed, a more digitally applicable equation was developed which takes advantage of VHDL's ability to manipulate registers, thus removing multiplication terms from the equation.



(a) Calculated estimation of velocity present during the actuation of the VCA for slow motion.

(b) Position profile generated for reference of the velocity estimation.

Figure 4.10: Velocity estimation profile during the displacement of the VCA utilizing a slow controller.

The output of the velocity estimator with respect to the change in discrete position over time for an aggressively tuned controller (i.e., high P and I gains) is highlighted in Fig. 4.9. Note, the starting point was 18,000 ADC counts, while the set point was set to 38,000 ADC counts. As indicated, the velocity profile is heavily influenced by the discrete position of the moving coil. As the location rapidly changes, so does the velocity information in response, most notably during the initial transition and the oscillations present when attempting to reach steady-state. The fluctuations present in the estimation are a result from the calculations, not the voice coil position. For this particular profile, the maximum velocity achieved was ≈1,600 (ADC counts)s^{-1}. The VCA motions presented in Fig. 4.9 were repeated with a less aggressively tuned controller, shown in Fig. 4.10. The velocity estimation now follows a smooth transition, with little fluctuations present in its profile; mirroring the movements of the position once more.

Tuning of the controller is slightly more complex than that of a single PID loop as it now involves three additional dependent gains. However, as cascade control

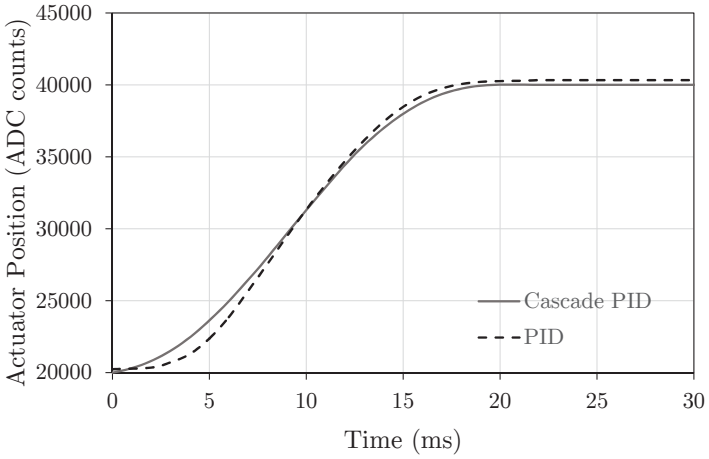


Figure 4.11: VCA transient response to an optimally tuned hardware-based cascade PID-PID control scheme with the PID response for reference.

has become more prominent, there has been much study into the optimal tuning method for determining each gain [134, 135]. While these techniques are proven, a more simplistic approach was taken to yield a reduction in development time. As such, the procedure simply promotes the tuning of the inner loop first, generally by way of simple proportional control and then constitutes the adjustment of the P, I and D gains associated with the master loop by using any tuning method for single control systems (e.g. Ziegler-Nichols).

Finally, mimicking the motions in Fig. 4.7 (PID), the fine-tuned cascade PID-PID controller's transient response, along with the PID's response, are displayed in Fig. 4.11. In contrast to the PID loop, the cascade rendition reaches the desired position while exhibiting less steady state error, $\approx$25 ADC counts (4.6 μm), and overshoot. A further comparison of these two control schemes is detailed in Section 4.6.

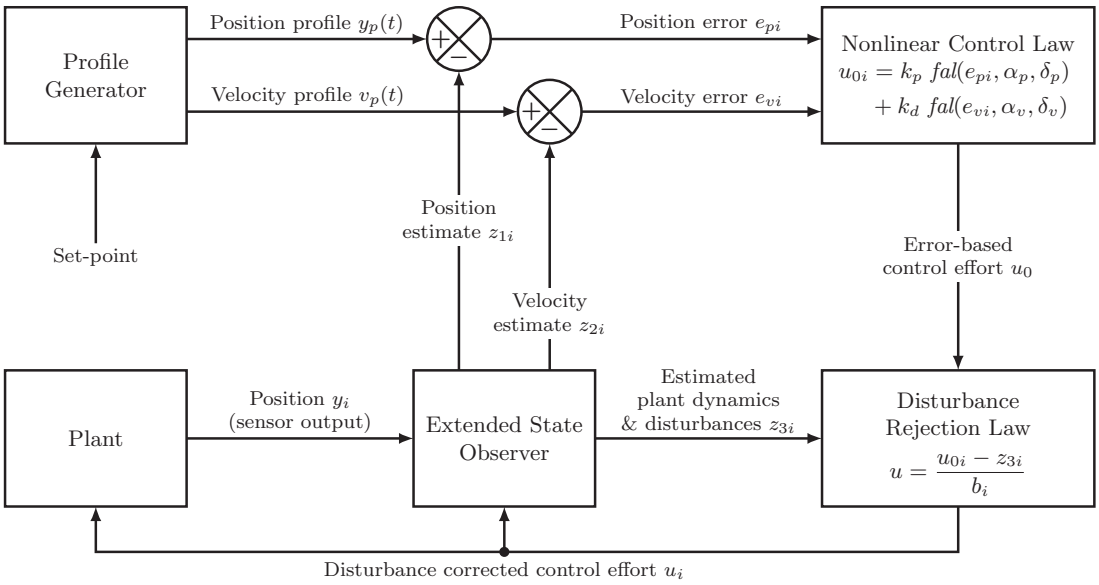


Figure 4.12: Topology of the ADRC architecture.

4.5 Active Disturbance Rejection Control

Though the cascade PID-PID architecture generates adequate control when properly tuned, increasing the moving mass of the actuator results in control issues that are prominent, especially considering the a highly dynamic nature of the VCA. Thus, the capabilities of ADRC were explored as means to provide validation to the cascade control system. Due to the scope and complexity of ADRC, this section will briefly describe its design and effect on the VCA's response. For an involved discussion of the hardware implementation of the ADRC methodology, please refer [19,39]. Nonetheless, to give light to the fundamental practices comprising the ADRC, the topology of the system is presented in Fig. 4.12 [19].

As shown, the design is comprised of four interconnecting sub-modules (representing systems of equations), which deliver a robust and reliable control signal to the plant; in this case the VCA. More specifically, these modules refer to a transient profile generator, a non-linear proportional-derivative (PD) controller, an extended state observer (ESO)

and a disturbance rejection module. Each of these systems are interdependent and vital to the deliverance of a highly adaptable control effort.

The profile generator is used to establish a trajectory for which the actuator can follow without going beyond its actuation limits [39]. A desired position is required to produce the curve which results in a velocity and displacement profile. These profiles are used in conjunction with the outputs from the ESO to provide accurate position and velocity errors to the non-linear controller.

The non-linear PD controller is unlike the aforementioned PID controller in key ways other than the lack of the integral term in its design. Its modified construction regulates a control signal based upon a set of parameters, of which its output depends on the extent of the position tracking error. This differs from a traditional PID loop as the non-linear PD generates a stronger signal for lower errors enabling more active steady state control without the use of the integral gain. Additionally, when large velocity error occurs, it compensates for a sudden spike in the control loop [39].

An extended state observer can be referred to as a model which estimates the state of a system by implementing a set of first order differential equations dependent on the inputs, outputs and states of a given system. For the VCA in particular, it is designed to estimate the total disturbance, or the combined effect of the actuator dynamics and any external disturbances, in real-time. It then sums the estimated position and velocity signals to the trajectories generated by the profile generator, in essence, eliminating disturbances from the system.

The disturbance rejection law module is simply an equation which governs the removal of disturbances from a system. It houses the control law which receives the estimated disturbances and state dynamics of the plant, as well as the error-based control signal from the non-linear PD controller. Through the mathematical structure, it is able to produce a control effort that nearly voids all disturbances in the plant as

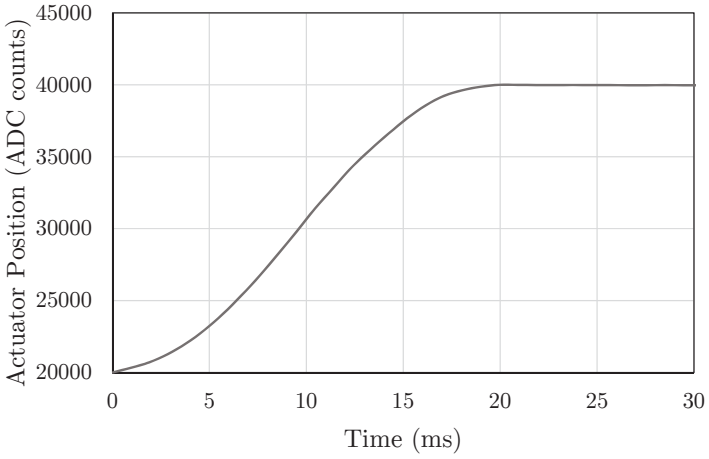


Figure 4.13: VCA transient response to an optimally tuned ADRC system.

well as produces a very low steady state error [19].

The combination of all of these factors allow ADRC to generate a very stable and precise control effort. However, tuning of the ADRC is quite complicated as it involves eight coupled tuning parameters which effect the functionality of each of the described modules. To this end, there are a number of resources in the literature which provide a systematic way of tuning [136–138], though it is still much more involved than a PID or cascade PID-PID controller. Nonetheless, when optimally tuned it provides a system response which is very fast, accurate and has strong holding force due to the disturbance rejection nature of its design. As a simple comparison to the PID systems, the response of the VCA with ADRC control in place is seen in Fig. 4.13, resulting in a steady state error of 5 ADC counts, or approximately 0.92 μm.

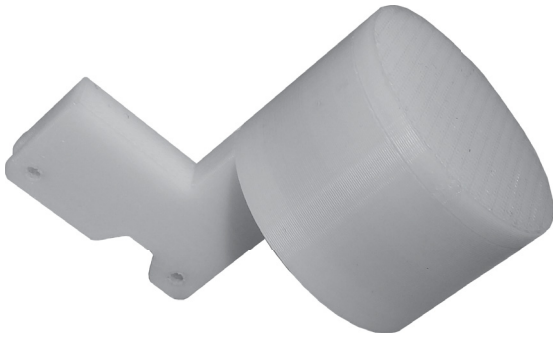
4.6 Controller Comparison

The previous sections gave an overview of three distinct control schemes which are used for a variety of applications; in this particular discussion, a novel voice coil

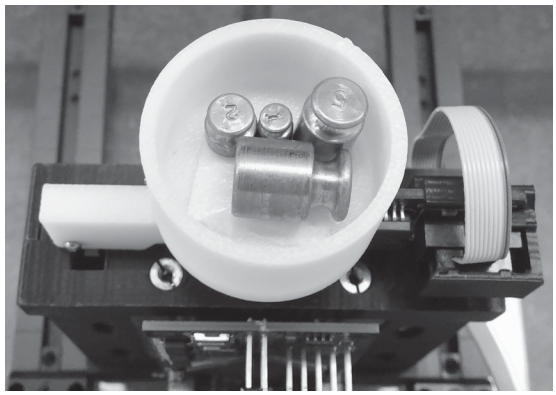
actuator. It is clear that each design exhibits benefits and drawbacks such as control ability, complexity of the controller and tuning parameter identification. However, to fully realize the potential of the control methodologies, a direct comparison of each was accomplished through a series of experiments involving the control of the VCA. In total, three different trials were conducted via increasing the moving mass of the actuator. Additionally, during each test, the transient motion of the VCA was recorded in response to a step input. To establish a baseline for comparison, all control methods were optimally tuned for a no load moving mass (i.e., the mass of the printed circuit board and electronics) accelerating against gravity. In each subsequent test, additional mass was added to the coil, increasing the payload by ≈50% and ≈100% or equating to 47.8 grams and 66 grams, respectively. To ensure accurate adjustments, the load was raised via precision weights held within a prototype container attached to the PCB of the actuator (Fig. 4.14). Note, to ensure the weights did not move or cause vibrations while inside the holder, they were held in place with strong, double sided tape.

To further validate their robustness, during each increase the VCA response was documented while employing the gain parameters for the no load mass. Finally, to guarantee the VCA's stator remained motionless and prevent disturbances to the system, it was securely fixed to the CMM in similar fashion to the repeatability experimentation in Chapter 3 (Fig. 4.15).

The ultimate aim of the experimentation was to gather sufficient information to showcase each controller's fundamental characteristics. The first, percent overshoot (undershoot), or the discrete value representing the percent which the voice coil actuator moves past its desired position. Second, the settling time, or the time required to achieve a steady state error of ±2% or less and remain within this boundary. Finally, as small fluctuations still exist within the system upon reaching steady state, the



(a) Realization of the rapid prototype weight holder.



(b) Experimental holder with various weights present.

Figure 4.14: Weight holder and its utilization in classifying the control systems.

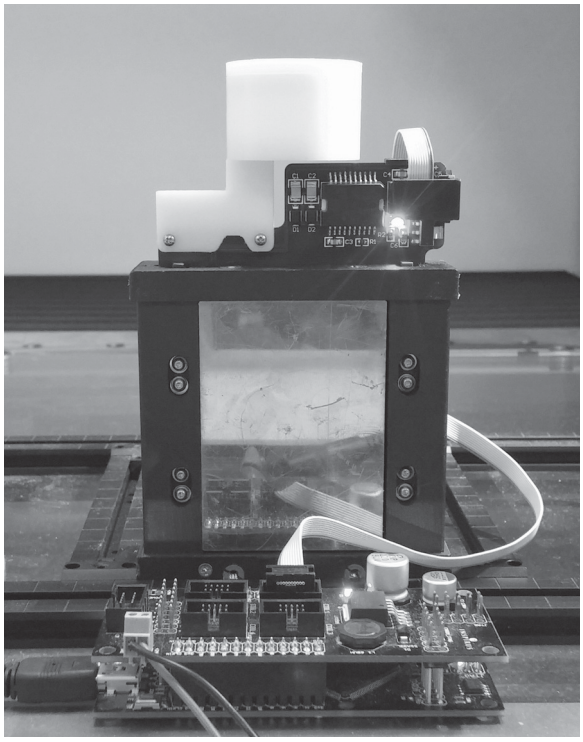


Figure 4.15: VCA with integrated weight holder during experimentation.

last performance metric is the discrete steady state error, or the absolute difference between the desired and settled positions. To ensure near-random data, 100 unique setpoints were generated by way of the Latin Hypercube implemented in Matlab. In addition, to prevent trivial motion, each displacement was restricted to no less than 2,000 ADC counts. Furthermore, to generate a more complete data set, each trial was repeated twice, resulting in 300 sample points per controller configuration. Table 4.1 showcases the results of each control scheme upon actuating the no load mass.

As theorized, ADRC outperforms both of the PID based control methods in all regards. However, considering the complexity of the ADRC, the cascade PID-PID worked very well in comparison. Note, it was recognized that the inwards (downwards) motion of the coil had a significantly negative impact on the PID controller's results. This is primarily due to the difficulty in realizing a single set of optimal gain parameters

Table 4.1: Transient response performance metrics identified via the actuation of the VCA in absnese of additional mass

Controller Architecture	Performance Metrics				
	Mean SSE	σ SSE	Mean ST	σ ST	Mean OS
PID	432	276.6	39	18.5	19.25
Cascade PID-PID	51	35.4	23	14.4	5.7
ADRC	18	12.9	21	5.9	0.23

SSE = Steady-state error (ADC counts), ST = Settling time (ms)
OS = Percent overshoot (%)

Table 4.2: Transient response performance metrics identified via the actuation of the VCA with an additional 14.8 g attached to its moving mass

Controller Architecture	Performance Metrics				
	Mean SSE	σ SSE	Mean ST	σ ST	Mean OS
PID	434	305.2	46	21.5	21.86
Cascade PID-PID	195	130.1	22	13.3	8.95
ADRC	29	21.6	20	5.8	0.52

SSE = Steady-state error (ADC counts), ST = Settling time (ms)
OS = Percent overshoot (%)

which can encompass actuation against and under the influence of gravity.

As described, the second test involved adding 14.8 g to the moving mass which is inclusive of the holder, in addition to the weights. The experiments were completed on each control architecture once more with the original gains in place. The results, displayed in Table 4.2, were similar to that of the first trial. However, the performance of the stand-alone PID is now greatly overshadowed by both the cascade rendition and the ADRC. Correspondingly, while the cascade PID-PID still performs well, it is beginning to lack the robustness of the ADRC.

For the final test, the payload was increased by approximately 33 grams, or twice the no-load mass and followed the routine established by the previous experiments. Finally, to determine the potential of the cascade PID-PID controller architecture, its gains were retuned with respect to the doubled payload and the experiment was

Table 4.3: Resource requirements of each controller system and the experimental results with the inclusion of 33 g to the moving mass

Controller Architecture	Performance Metrics				
	Mean SSE	σ SSE	Mean ST	σ ST	Mean OS
PID	486	325	55	26.1	21.8
Cascade PID-PID	277	190.5	23	9.3	9.8
ADRC	80	51.2	20	5.9	1.1
Retuned Cascade	125	87.6	23	9.3	8.6

SSE = Steady-state error (ADC counts), ST = Settling time (ms)
OS = Percent overshoot (%)

Table 4.4: Hardware resource requirements of each control system

Controller Architecture	Hardware Resources		
	Logic elements	Memory Bits	Multipliers
PID	2,670 (6.7%)	0 (0%)	4 (1.5%)
Cascade PID-PID	3,010 (7.6%)	0 (0%)	8 (3%)
ADRC	4,029 (10%)	315,392 (27%)	36 (14%)

completed once more. Table 4.3 contains all of the testing outcomes and in addition, Table 4.4 displays the hardware resources required by each methodology, to indicate both the scale and complexity of each system.

Once again, the data found in Table 4.3 proves the validity of ADRC, as it has widened the gap between it and the untuned cascade PID-PID architecture. Furthermore, the signal PID loop has now become ineffective at controlling the VCA in all aspects. The retuned cascade scheme's results prove that though the performance of ADRC is still ideal, they are significantly more comparable. Therefore, based upon the system and its characteristics, a cascade PID-PID may provide more than adequate control. However, a properly tuned ADRC algorithm will generate the most robust, ideal control effort, especially for mechanisms with extreme dynamics. Nonetheless, as the cascade PID-PID scheme has uncomplex tuning parameters and was readily available, it was selected as the candidate controller for utilization in the ATM.

4.7 Conclusions

In general, classifying the optimal control system for a highly dynamic mechanism is not trivial in nature, as its agility proves problematic with traditional control systems. In addition, adjusting the position of the novel VCA in a precise manner is a difficult task for high-level programming languages such as C# due to their slower update rates and sequential nature. As a solution, three control scheme's were developed in VHDL which promote a wide variety of advantages. While the capabilities of each control architecture may be quantified by the response of the system, other factors such as resource cost and complexity in tuning play a part in the ultimate decision. The results identify that the PID scheme was far outmatch by the cascade PID-PID and ADRC controllers, with the ADRC having more robustness and precision than the cascade controller for many test cases. However, this is at a cost of additional logic and abstract tuning parameters, leaving the definition of the ideal controller decided by the application. Nonetheless, due to the simple tuning parameters and the availability of the control architecture, the cascade PID-PID scheme was chosen for implementation in the ATM.

Chapter 5

FPGA and Microcontroller PCB Designs for Optomechatronic Applications

Suitable hardware must be selected to meet the strict SWaP demands and time-critical control schemes required by the novel VCA and POM structures. Traditional computer systems and high-level programming languages are not applicable for achieving SWaP conditions due to their size and speed. Due to its parallelism, exceptional speed and ability to fulfill SWaP requirements, the FPGA is favored as a reliable hardware system. However, integrating mass produced FPGA devices into existing architectures is problematic and reduces reliability as they are bulky, generalized and not application specific. To this end, a customized PCB containing an FPGA and applicable connections was created specifically for controlling multiple VCAs in parallel. In addition, a microcontroller was added to the PCB to remedy the FPGA's issue with resource consumption and complexity when processing complicated mathematical equations. Correspondingly, a shared memory controller was developed in VHDL to provide a parallel, bi-directional communication link between the microcontroller and FPGA. Finally, to support the proposed targeting and communication system, the PCB was fitted with hardware, capable of generating and manipulating pixel data via an image sensor and memory chips.

5.1 Introduction

Due to the high speed and precise nature of the novel voice coil actuator and POM architectures, suitable hardware must be employed to ensure appropriate functionality. Ideally, control algorithms must be capable of producing reliable, high frequency responses in order to quickly correct for the fast movements of the actuator (Chapter 3). To this end, among all available hardware options such as complex programmable logic devices (CPLDs), the field programmable gate array was chosen as the development device for the project due to its versatile design which provides exceptional capabilities for control of the VCA and POMs. These include its parallelism, its exceptional speed, low power consumption and miniature design; all of which fall within the confines of SWaP requirements. Furthermore, embedded designs far outperform traditional computer architecture for optomechatronic applications as they require minute overhead (i.e., operating systems, software), are compact and need very little cooling.

Fundamentally, an FPGA consists of digital logic circuits (i.e., AND, OR, XOR gates) and thus, developing computer code for them requires the manipulation and organization of logic elements. Fortunately, hardware description languages such as Verilog and VHDL, reduce much of the complexity associated with digital design by providing an integrated development environment (IDE) for constructing algorithms. In contrast to the sequential arrangement of software based languages such as C#, HDLs apply a parallel-based approach, granting exceptionally fast run times.

As mentioned previously, meeting SWaP requirements poses no issue for an FPGA. However, one of its most notable flaws is its struggle with complex mathematical functions and equations. Due to its digital nature, trigonometric and non-linear equations are very taxing on the available resources of an HDL design, greatly

limiting its capabilities. Recently, FPGA designers have been rectifying this issue by introducing microcontrollers into the FPGA architecture; whether it be a software [139], or hardware-based solution [22]. While this may resolve the problem, the only method of creating code for the microcontroller is within the manufacturer's IDE. Additionally, for these type of unique designs there are limited documentation and working examples available. These issues result in longer development times and unoptimized algorithms. Therefore, a more user friendly, versatile application to remedy this scenario is required.

Due to the exceptionally documented, simple to use Arduino IDE, an FPGA and Arduino compatible microcontroller were joined by way of multiple input-output (I/O) lines, hard-wired on a PCB. This configuration, along with a hardware based, dual-port memory controller forms the foundation of an FPGA-microcontroller PCB, deemed the F-Micro board. While the code generated for the architecture was developed within the Arduino interface, it is fully capable of functioning on any C compatible device, leading to a more robust design.

Constructing a printed circuit board with FPGA functionally customized for specific applications has many advantages over readily available, generic layouts created for development purposes. One of the most prominent characteristics of a tailored design is the ability to personalize the PCB to adhere to requirements of any device, a boon for optomechatronic mechanisms. Unnecessary electronics, IO connectors and interfacing circuitry may be disregarded, resulting in a vastly superior and robust PCB which fulfills SWaP specifications. With applications considered, two distinct versions of the F-Micro board were developed. The first, a VCA oriented, compact design, while the later a hardware camera capable rendition; each of which will be detailed in the upcoming sections.

5.2 F-Micro PCB Design

The primary purpose of the customized F-Micro board was to ensure it fulfilled the SWaP requirements established by the novel VCA; especially in comparison to consumer based development kits. This meant the construction of a PCB that was compact, lightweight, incorporated necessary components only and could be easily attached to the VCA and POM structures. As previously mentioned, the core functionality of the design stems from the inherit interconnectivity of the FPGA and microcontroller. To achieve the required specifications, the two devices chosen to fill these roles were the Altera Cyclone 3 FPGA [140] and the Atmel ATmega32u4 microcontroller [141]. The combination of these integrated circuits, along with key elements including power regulators, program interface hardware and LED indicators, form the foundation of the F-Micro board structure. Additionally, an abundance of external I/O pins and simple access to 3.3 V and 5 V logic promote the integration of external devices such as ADCs, encoders and lasers. Furthermore, the I/O pins of the FPGA were configured to reflect the 3.3 V low voltage transistor transistor logic (LVTTL) I/O standard. This results in a "'high" signal when a minimum of 1.7 V is present on the input line and a "low" response up to a maximum of 0.8 V. In addition, at this logic level, the voltage received on the input pins cannot exceed 3.6 V or damage to the chip may occur.

To create a physical realization of any PCB, it should first be represented in its digital form by way of an electrical schematic. Therefore, to generate these files, EagleCAD software was selected due to its practicality and simple-to-navigate user interface. Furthermore, it displays a visual representation of a component to scale (i.e., the correct size), ensuring the PCB is constructed in the most optimal, compact fashion. For the VCA specific configuration, the PCB was comprised of four separate

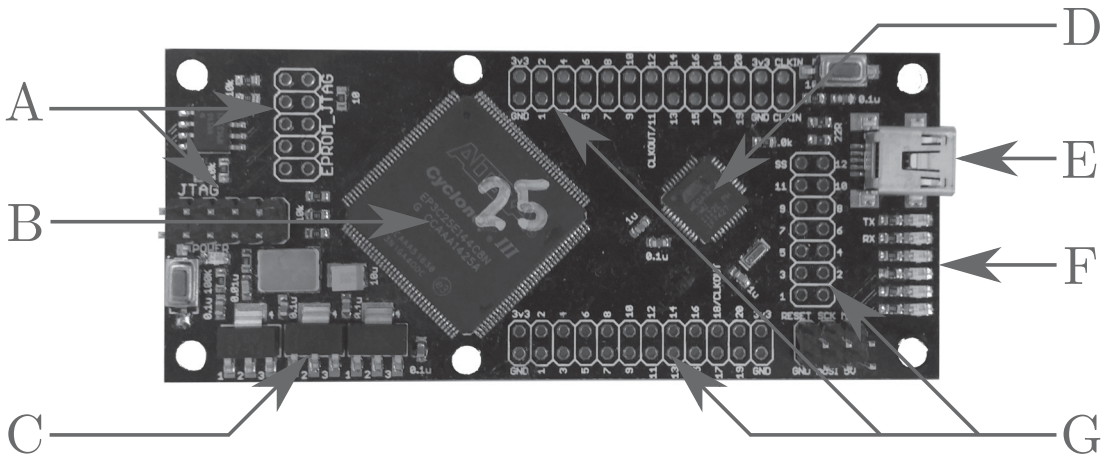


Figure 5.1: Physical realization of the F-Micro PCB. A: FPGA programming pins. B: Altera Cyclone 3 FPGA. C: Power regulation. D: Atmel ATmega32u4 microcontroller. E: Micro USB connector for supplying power and uploading code to the microcontroller. F: Indicator LEDs. G: FPGA and microcontroller I/O.

layers, measured 3.5 x 1.5 x 0.062 (thickness) inches and had a mass of ≈22 g after population of the electronics. The physical representation of the F-Micro board can be viewed in Fig. 5.1.

Via the numerous external I/O connections, the F-Micro board was crafted with the ability to interface multiple VCAs in parallel, permitting full control of the POM structures. Correspondingly, it features additional adapters allowing for the incorporation of extra I/O devices into the FPGA architecture. In particular, laser diodes for the implementation of a pointing mechanism, attaching a Future Technology Devices International (FTDI) chip granting communication abilities, temperature sensing devices and external position sensors (i.e., encoders). However, when joining multiple devices containing abundant I/O, it is inappropriate to do so with standard, copper wire to prevent unwanted soldering. Therefore, an additional PCB, designated the F-Con board (Fig. 5.2) was designed with quick-connect functionality via two 30-pin insulated modular connectors (i.e., terminal blocks). Furthermore, as the VCAs were to be attached and removed regularly, 10-pin headers, featuring 0.1 inch row

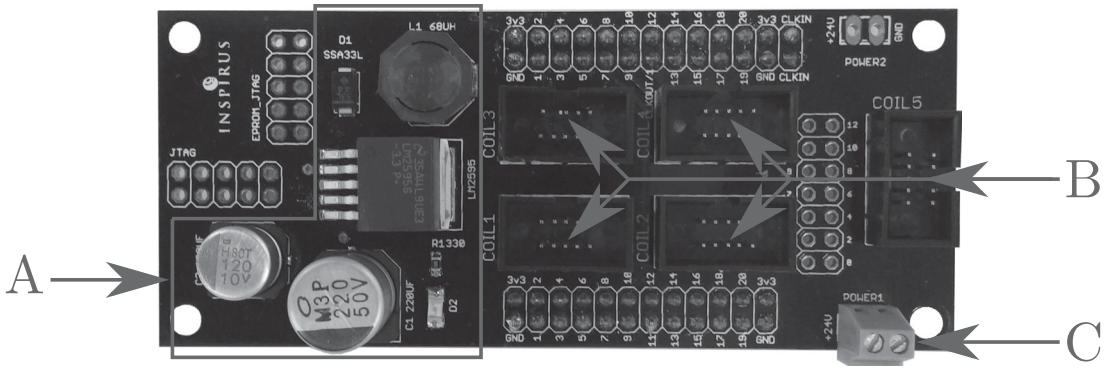


Figure 5.2: Physical realization of the F-Con PCB. A: Power regulation with switching voltage regulator. B: Ribbon cable connectors for VCA attachment. C: Termination block for power input.

and 0.05 inch center spacing, were integrated into the F-Con design for the purpose of delivering power, discrete position information and control functionality to the actuator.

The design vastly increases the reliability of the F-Micro and ensures each signal is properly insulated and isolated from its neighbors. Correspondingly, its performance is expanded by introducing adept power regulation (i.e., a switching regulator to aid in converting large voltages (a maximum of 45 V) to logic level renditions) for all connected VCAs in addition to the F-Micro board; allowing a single voltage source to energize the PCB and applicable devices. The union of the F-Micro and F-Con boards is shown in Fig. 5.3.

The entire package, capable of controlling five VCAs if required, is very compact, ≈1.25 inches including electronics, lightweight, have a combined mass of 47 g and is power efficient due to the switching voltage regulator. The combination of both boards has been integral to the development of a number of optomechatronic systems due to their exceptional reliability and robustness. Finally, Fig. 5.4 displays the F-Micro board fastened to the VCA to promote the seamless assimilation with the structure.

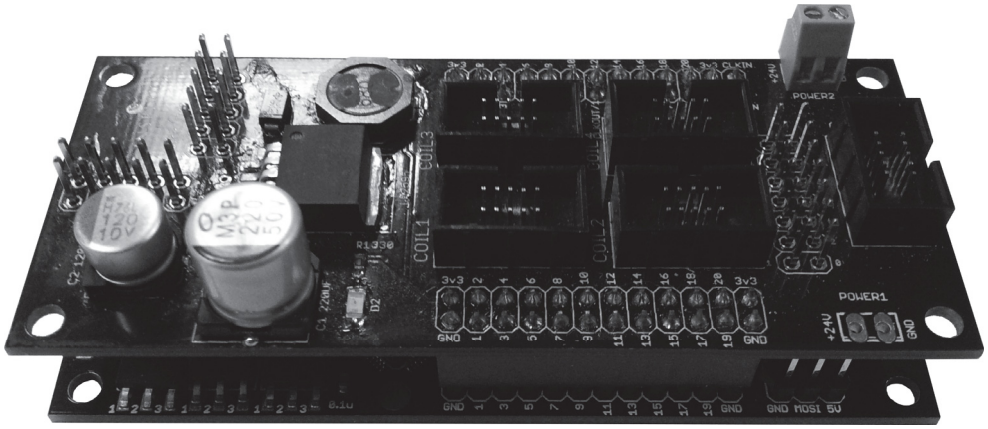


Figure 5.3: The united F-Micro and F-Con PCBs.

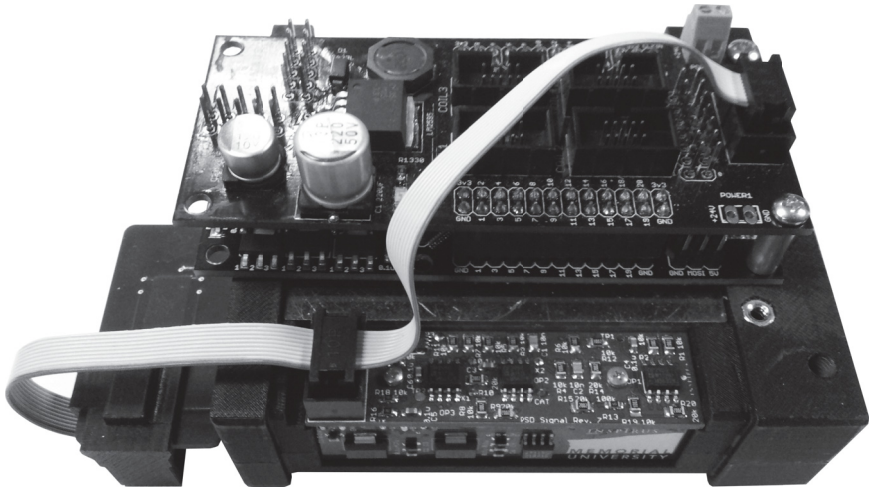
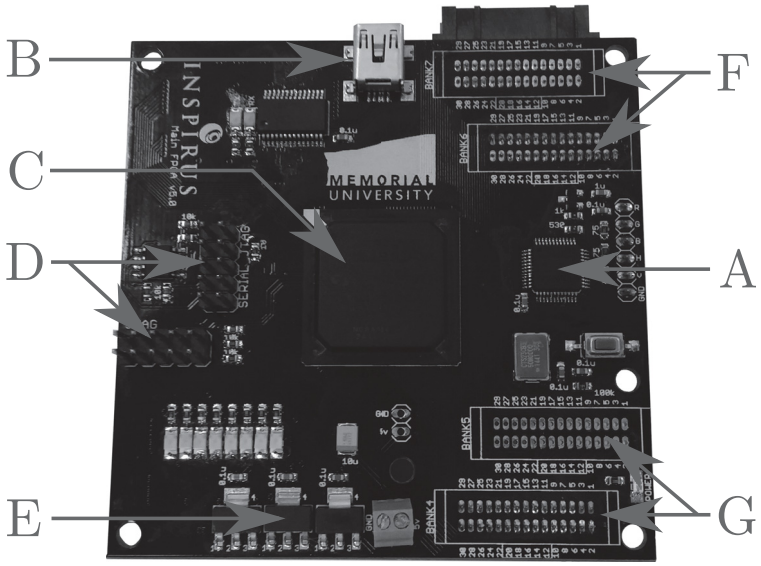


Figure 5.4: Integration of the F-Micro PCB with the novel VCA.

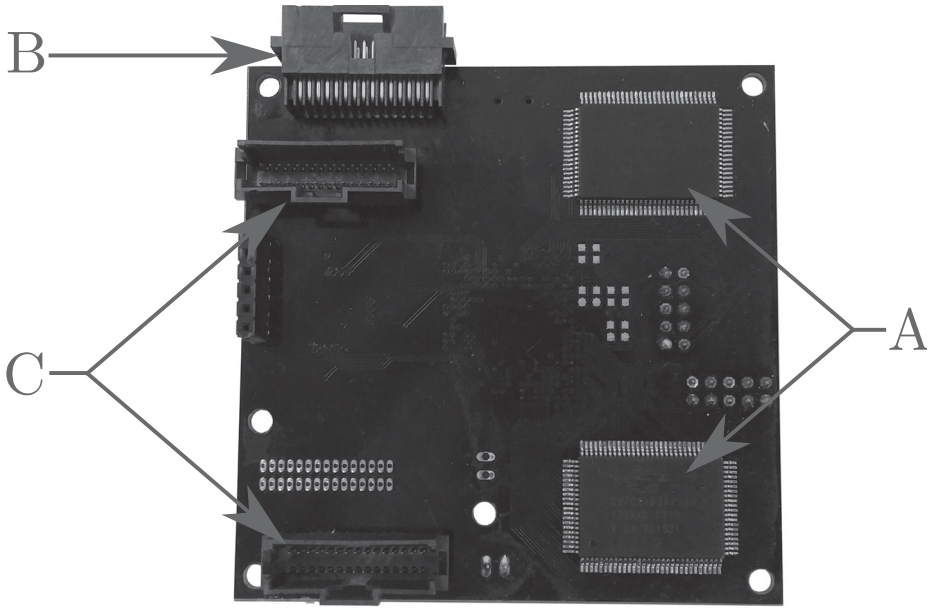
5.3 F-Micro Camera Adaptation

While the F-Micro PCB has been identified with multi-purpose capabilities, many optomechatronic applications require the presence of image sensing devices [4, 5]. In particular, the proposed visual based targeting mechanism requires not only image gathering functionality, but the ability to recognize and manipulate pixel data at high rates. Consequently, an image sensor, the Aptina Imagining MT9T031 [142], was integrated into the F-Micro architecture through short traces on the PCB ensuring high frequency noise remains at a minimum. This device assembles pixel information, stores, modifies and displays the result in real-time via onboard static random access memory (SRAM) and a video graphics array (VGA) adapter. The PCB, named the FC-Micro, was created in similar fashion to the aforementioned F-Micro board and promotes a slightly larger, but still tiny form factor of 3 x 3 x 0.062 inches, weighing 34 grams. The top and bottom physical representation of this PCB are highlighted in Fig. 5.5a and 5.5b. To ensure accurate pixel information is obtained swiftly and efficiently, a modular image storing system was produced in VHDL and is detailed in Chapter 6.

Similarly to the F-Micro construction, an adapter PCB was constructed to grant the FC-Micro access to extra circuitry, enhancing its functionality while retaining its compact form factor. It fastens to the FC-Micro board via four 20-pin headers to ensure all I/O are accounted for. The FC-Con layout is a modification of the F-Con PCB; however, it incorporates the microcontroller into its architecture as the image sensing hardware requires ample space. Furthermore, the image sensor and its hardware demand a significant amount of I/O, restricting the number of VCA connections to three. The top and bottom views of the FC-Con PCB are shown in Fig. 5.6a and Fig. 5.6b, respectively.

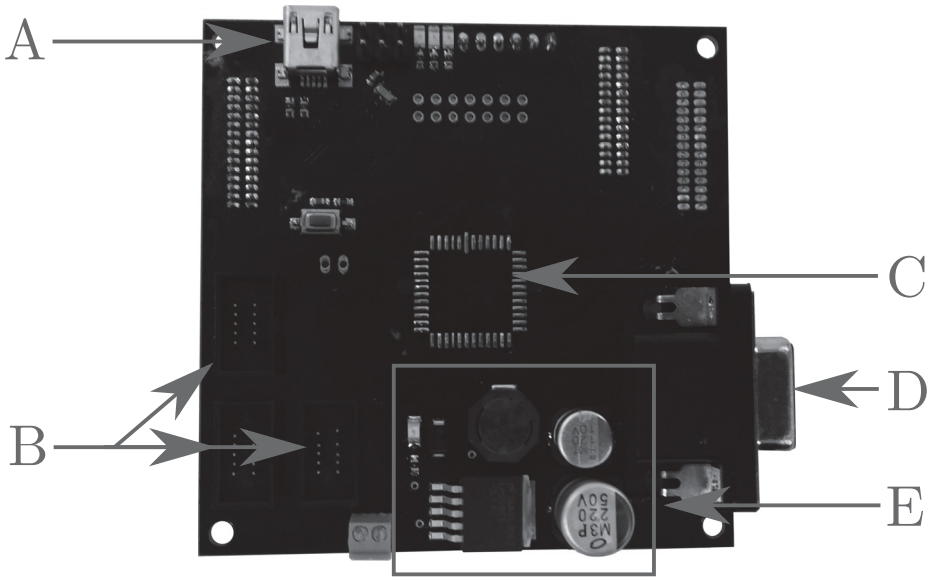


(a) FC-Micro PCB (top). A: Micro USB. B: Altera Cyclone 3 FPGA. C: FPGA programming pins. D: Power regulation. E: FPGA I/O pins. F: Video digital-to-analog converter (VDAC). G: FPGA I/O pins.

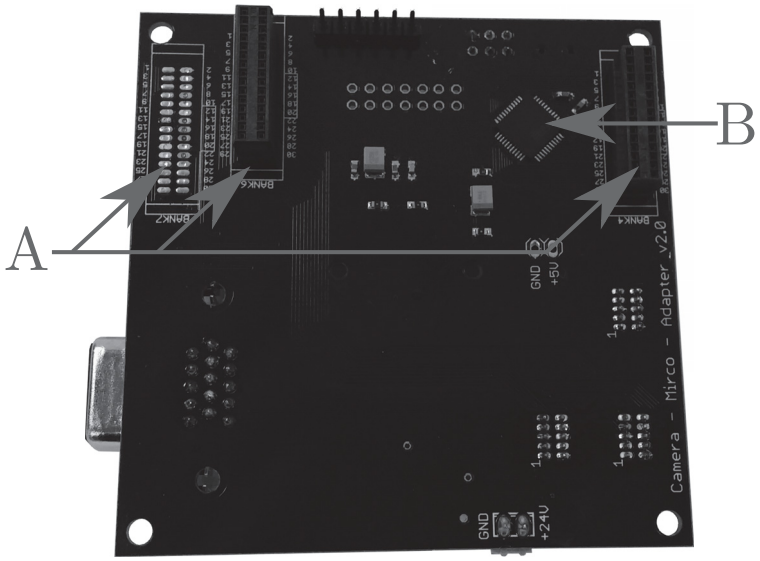


(b) FC-Micro PCB (bottom). A: Connector to external image sensor. B: Connectors for FPGA I/O. C: SRAM integrated circuits.

Figure 5.5: Realization of the FC-Micro PCB.

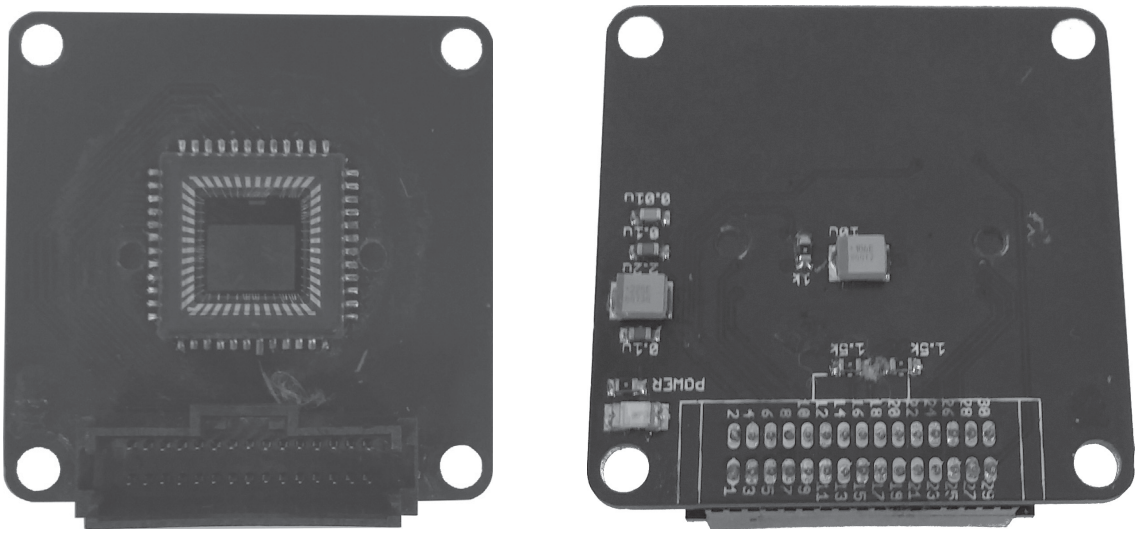


(a) FC-Con PCB (top). A: Micro USB. B: Ribbon cable connectors for interfacing VCAs. C: Surface mount soldering pads for onboard image sensor integration. D: VGA output. E: Power regulation.



(b) FC-Con PCB (bottom). A: Connectors for integration with FPGA I/O. B: Atmel ATmega32u4 microcontroller.

Figure 5.6: FC-Con PCB physical realization.

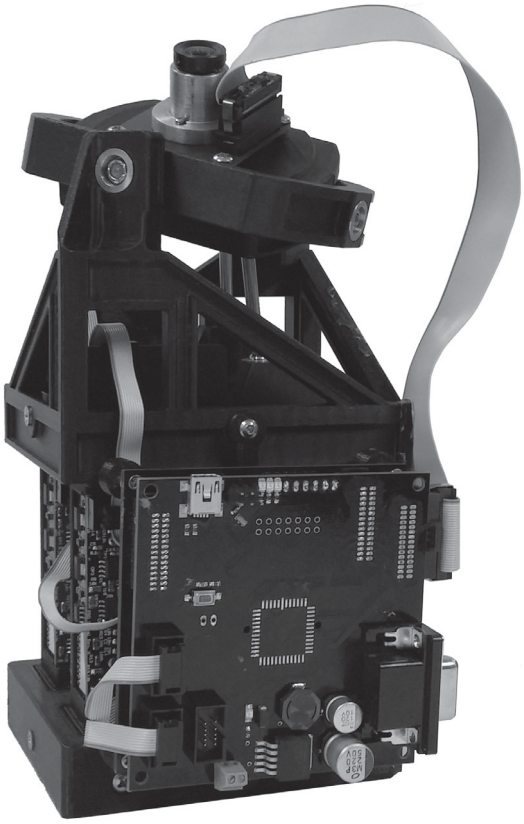


(a) Image sensing board (top). (b) Image sensing board (bottom).

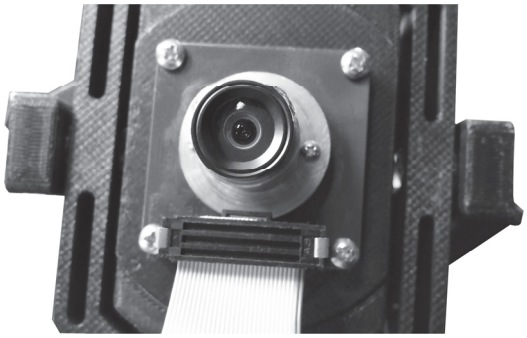
Figure 5.7: Miniature, stand-alone image sensing board.

To complement the camera adaptation of the FPGA board design, a stand-alone, miniature PCB consisting of the image sensor, 5 mm lens [143] and a small number of electrical components was developed (Fig. 5.7). It boasts a compact size of 1.5 x 1.5 x 0.62 inches and lightweight design (i.e., 32 grams with lens attached), further enhancing the FC-Micro PCBs capabilities.

Removing the image sensor from the FC-Micro rendition and attaching the stand-alone adaptation to the PCB via a 30-pin ribbon cable enables the effortless unification with a mobile platform. This is imperative for the automated targeting mechanism as higher payloads are extremely detrimental to the dynamics of the system. The detached board is incorporated into the moving platform of the 2DOF POM resulting in little moving mass as opposed to integrating the significantly larger FC-Micro board. The FC-Micro PCB fastened to the POM is highlighted in Fig. 5.8a. In addition, Fig. 5.8b showcases the miniature camera board with a lens positioned in front of the sensor attached to the platform of the 2DOF POM. Opting for this configuration



(a) 2DOF POM integrated with the image sensing board and combined FC-Micro and FC-Con PCB.



(b) 2DOF POM mobile platform with image sensing PCB attached.

Figure 5.8: Integration of 2DOF POM with image sensing technology.

ensures the POM can freely position the camera efficiently and still being highly dynamic while meeting SWaP requirements.

5.4 FPGA-Microcontroller Bi-Directional Communication

Interfacing an FPGA with a microcontroller is a routine that is becoming increasing popular in industry as the capabilities of both devices are complimentary. However, in many cases the connectivity between each is flawed with unintuitive application programming interfaces (APIs) resulting in development constraints and lack of reliability. Thus, the F-Micro communication protocol was envisioned to remedy many of these issues by instantiating a robust, easy to employ IDE to reduce programming complexity and design time.

In response, an Arduino-capable microcontroller was selected to permit C applicable programming, in addition to the Arduino's rendition of C, improving functionality. While the Arduino programming environment contains overhead which may reduce the speed of particular algorithms, it is still an ideal choice for implementing an abundance of useful tools, such as serial communication techniques. Correspondingly, as the data link between the FPGA and microcontroller results in a assortment of applications, it is crucial to promote versatility in its composition.

To establish a parallel, bi-directional communication protocol between the FPGA and microcontroller, both devices were interconnected via 20 distinct traces within the PCB. Only 20 connections could be utilized as the microcontroller was selected for its size characteristics (i.e., to ensure the F-Micro board remained compact), thus limiting its available I/O. Nonetheless, of the 20 links, eight traces were designated as data lines, an additional eight were responsible for handling address information and the final four connections were utilized as control signals to enable read and write operations between the FPGA and microcontroller. This resulted in a configuration

capable of communicating 8-bit values (i.e., 0 - 255) bi-directionally while storing each in 256 unique addresses. Note, the architecture was designed with the FPGA acting as a slave unit, while the microcontroller represents the master, essentially controlling the data flow.

5.4.1 Microcontroller Protocol

The microcontroller segment of the communication protocol was developed to grant simple read and write functions with the capacity to send and receive data to and from the FPGA. While the Arduino wrapper has the capability to assign values to I/O connections effortlessly, its large overhead reduces the update rate of the assignments; especially in comparison to standard C programming. Therefore, implementing digital logic techniques (i.e., logic encoder), a number of I/O pins were configured into equations which when correctly executed, ensured speedy read and write functionality.

Through vigorous testing it was determined that these equations boosted the frequency of the communication protocol by over 500% resulting in maximum transmission rates of ≈133 kbits/sec, with average, more reliable (i.e., a bit error rate of zero) of 100 kbits/sec. These values are limited primarily by the maximum clock speeds of both the FPGA (50 MHz) and more notably, the microcontroller (16 MHz). In addition, as previously discussed, if the PCB size was not a design constraint, a larger microcontroller with abundant I/O could be integrated with the FPGA to increase the number of communication lines, drastically amplifying the data rate. However, these values are still significantly lower than what serial peripheral interface (SPI) can achieve , with data rates reaching 20 Mbits per second ([144]). Nonetheless, this protocol was still utilized as it allows for numerous packets of data to be accessed by both the FPGA and microcontroller with ease. It also leaves the serial port of the

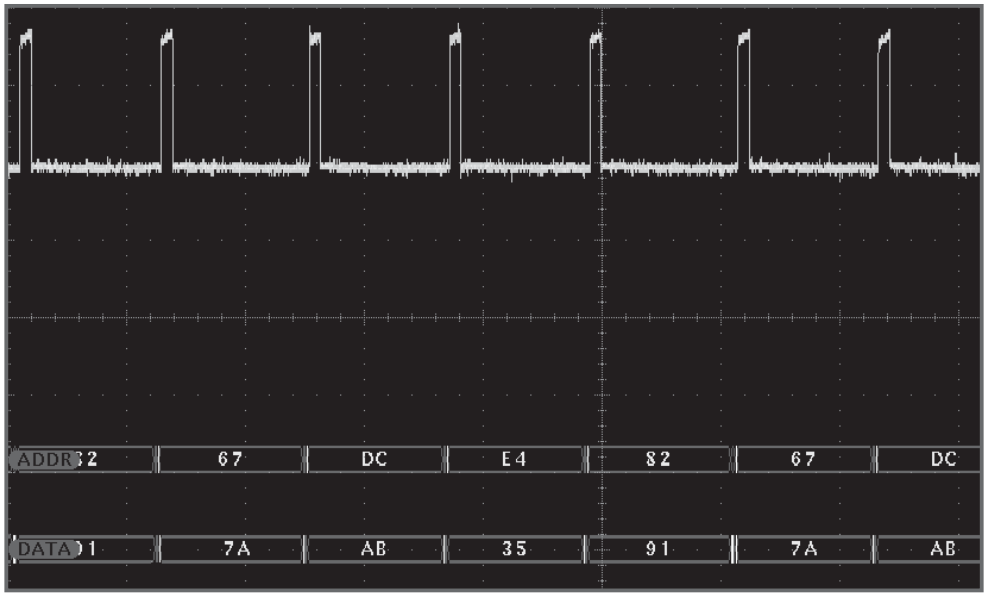


Figure 5.9: Data transmission example between the microcontroller and FPGA.

microcontroller free to be used with other devices, such as a computer as mentioned in the upcoming sections.

The code implemented with the strict purpose of generating the data flow is efficient and simple to employ. The write function requires two inputs; the data to be communicated and the address for storage in the FPGA memory; whereas the read method demands the memory address where the desired data is stored, resulting in an 8-bit number being received. These functions are incorporated in modular files, allowing for effortless integration into any C-based project. An example of the data flowing from the microcontroller to the FPGA was obtained by a digital oscilloscope and is shown in Fig. 5.9. The hexadecimal values *7A*, *AB*, *35* and *91* are being delivered to the FPGA in addresses *67*, *DC*, *E4* and *82* respectively, as indicated by the *DATA* and *ADDR* nomenclature on the digital oscilloscope screen capture. The square signal present at the top of the figure indicates the read/write command entering write mode.

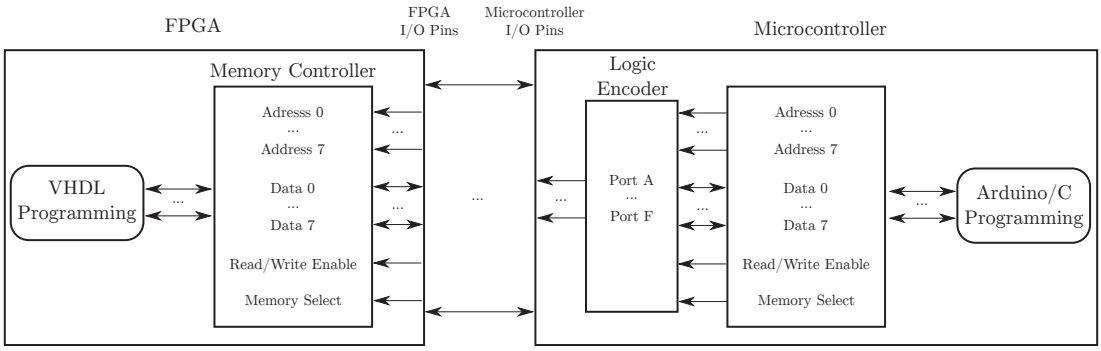


Figure 5.10: Bi-directional communication data flow between the FPGA and microcontroller.

5.4.2 FPGA Memory Controller

The communication protocol contained within the FPGA differs greatly from that of the microcontroller, as it hosts the shared, dual-port memory controller configured to store the information for both sides of the link. Excluding the architecture of the memory controller, no additional functionality is required to read and write within the FPGA; the only necessary action is to connect (i.e., wire) registers between modules in the FPGA and the designated memory. The design incrementally checks each address at a frequency of 50 MHz, with read and write modes switched after each cycle through the memory. This occurs at much higher frequency than the data rate of the microcontroller protocol, ensuring no data is lost between read and write commands. If the read mode is active, the FPGA assigns the 8-bit numbers stored in memory to any internal register requiring the data. Conversely, if writing, the data in memory is updated to reflect any changes in the register values, making them available to the microcontroller. The bi-directional communication allows data to manipulated in the FPGA, be stored in the memory and finally transmitted to the microcontroller. A visual representation of the multi-direction, parallel data flow is highlighted in Fig. 5.10.

To add further functionality to the memory structure, a graphical user interface

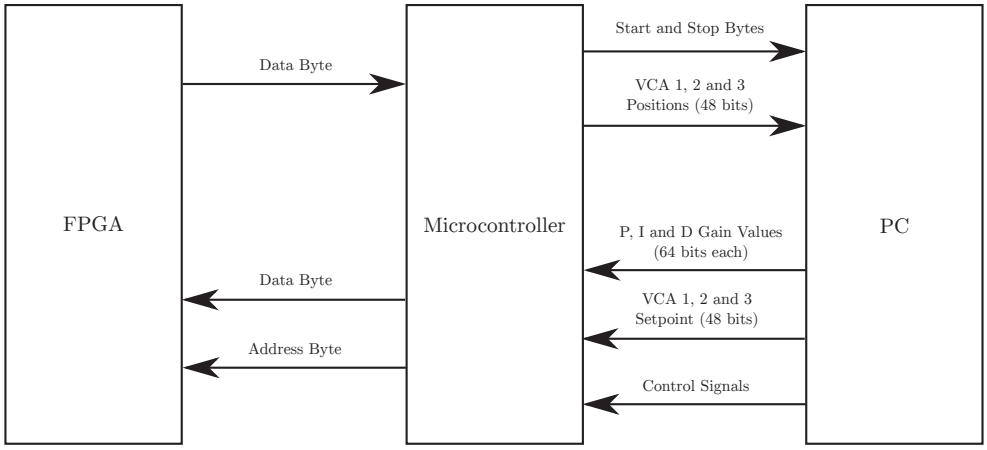


Figure 5.11: Data flow between FPGA, microcontroller and PC.

(GUI) was developed in the C# programming language. This modular design inserts a personnel computer (PC) into the communication link by way of serial communication between it and the microcontroller. This ultimately produces a bi-directional protocol between the FPGA, microcontroller and PC enabling data to be manipulated by the GUI, transmitted to the microcontroller and in turn delivered to the FPGA as shown in Fig. 5.11.

As indicated by the figure, information can be transmitted in the opposite direction as well, permitting communication between a FPGA and PC with the microcontroller acting as an intermediate data buffer. The PC algorithm is designed to update information (i.e., three VCA discrete positions) transmitted by the microcontroller in real-time, while simultaneously sending data back through the same channel. A major benefit of this arrangement is employing the GUI to modify data contained within registers on the FPGA. In particular, adjusting the values of multiple gains when attempting to fine-tune a control system. This ability greatly decreases design time, enabling simple, efficient tuning as the VHDL algorithm does not require rebuilding with each subsequent test. Note, reconfiguring VHDL code is an operation requiring ample time (i.e., minutes) depending upon the size of the project. Furthermore, in

regards to the VCA technology, the link also enables a graphical way of displaying its position sensor data, as the FPGA simply "streams" the information to the GUI. Finally, additional functionality such as sine wave and setpoint generation was added to the interface to showcase the speed and accuracy of the voice coil and its control system.

5.4.3 Conclusions

Dictated by the SWaP requirements and agile nature of the POM architecture, developing algorithms on large computer systems with high-level programming was not possible. To this end, due to its hardware based design and parallelism, an FPGA was selected as the most promising device to fulfill the SWaP conditions. However, as off-the-shelf FPGA boards are generally bulky and hard to incorporate into existing mechanisms, a small scale, application specific FPGA PCB was constructed with the ability to control multiple VCAs in parallel. Complimenting the design, a microcontroller was added to the PCB providing high speed, bi-directional communication between it and the FPGA via a shared memory controller developed in VHDL. To further increase its capabilities, an additional rendition with image sensing and storage functionality was developed. This version was integrated with the POM architecture for utilization in the ATM.

Chapter 6

Visual Recognition and Parametrization of Objects in Hardware Description Language

Localizing a region of interest and its characteristics in real-time are exercises requiring high-speed processing not typically found in traditional computing devices. To develop reliable, robust algorithms capable of undertaking these tasks, the FC-Micro PCB was utilized due to its embedded design and the parallel nature of VHDL. By performing image segmentation in VHDL on the grayscale representation of Red-Green-Blue (RGB) pixel data, the object of interest was isolated from its background. Using the newly configured pixel information, a contour tracking algorithm known as crack code was developed in hardware to define the parameters associated with the particular object. These characteristics are used to represent the object's location with respect to the coordinate system defined by the image sensor. Subsequently, the results determined by these methods allow the pursuit of a high rate targeting system.

6.1 Introduction

Localizing and determining the characteristics of an unknown object in real-time is problematic due to limitations in the processing capabilities of standard PC architecture. Furthermore, employing the microcontroller integrated within the FC-Micro board as a means to implement this functionality was not an option, as real-time image processing requires the manipulation a overwhelming amount of data. In response, object recognition and parameter identification algorithms were designed in VHDL, taking advantage of its parallelism and high speed capabilities ensuring the parameters of an object are classified at extremely high rates. Additionally, the FC-Micro board adaptation along with the stand-alone image sensor acted as the image sensing mechanism for the system.

To locate and identify a region of interest in real-time two specific image processing techniques were utilized, image segmentation (i.e., thresholding) and contour tracking. Segmenting a set of pixels allows for the isolation of an object from its background, essentially removing all unnecessary details from the image [145], while the procedure of determining the contour of a region of interest can provide a substantial amount of information towards classifying its parameters. Though these algorithms are fairly standard and generally simple to design in high-level programming languages (i.e., Matlab, C#), doing so in VHDL is more difficult, as mathematical functionally common to other languages is troublesome to design in hardware [57].

An image can be digitized by numerically representing each pixel at particular row and column position (I_{ij}). To simplify matters and reduce resource costs associated with image processing, the light intensity information of each pixel is synthesized from the full color, or the RGB image. This technique refers to the grayscale transformation of an image, as it converts discrete data from true color to one that is monochromatic

(i.e., displaying shades of gray) in nature. Reorganizing the data in such a fashion enables an optimized thresholding algorithm to be constructed as each pixel is represented by a single 8-bit intensity value ranging from zero (true black) to 255 (true white), in contrast to the RGB representation comprised of three 8-bit numbers.

Upon rearranging the image data, thresholding is accomplished by segmenting the image into a binarized representation, classifying the object as '1' with '0' being the background. With this configuration in place, a contour tracking algorithm known as the crack code technique was utilized to determine the boundary of the object [146]. While other techniques such as the Hough transform method are capable of this task [147], the power of crack code is its capability of defining a set of form parameters which can determine an object's area and centroid location [148, 149]; essentially tracking an object in the camera's FOV.

6.2 Isolation of an Object from its Background

In computer vision, thresholding is categorized under the term image segmentation, referring to image processing algorithms which partition a digital image into multiple sets of pixels (i.e., S_1,S_2,..). This is fundamental in highlighting important features contained within an image. Correspondingly, it allows for simpler analysis of the pixel information as each class of pixels encompasses some form of digital similarity (i.e., intensity, color).

For this particular application, thresholding refers to the transformation of a grayscale image to a binary representation, converting all intensity values to zero (black) and one (white). While this removes an abundance of information, it dissolves an image into its simplest form, allowing for the recognition and classification of objects. The most basic form of thresholding is implemented by simply replacing the

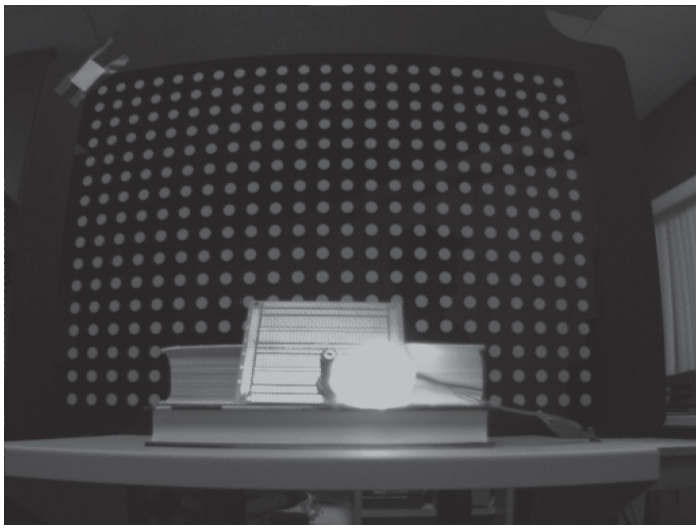


Figure 6.1: IR LED experiencing poor diffusion.

pixel intensity I_{ij} with '1' if greater than a specified threshold constant T, and '0' if equal to or less than T, as specified in equation 6.1.

$$I_{ij} = \begin{cases} 0, & I_{ij} <= T \\ 1, & I_{ij} > T \end{cases} \tag{6.1}$$

Determining the appropriate value of T which results in the ideal segregation of pixels can be achieved by a trial and error method. However, a more optimal approach involves generating the image's gray-level histogram, which is a graphical representation of the intensity distribution of an image as it quantifies the number of pixels for each intensity value. The histogram of a monochromatic image of size i and j, contains a x-axis ranging from zero to 255, with the y-axis representing the number pixels pertaining to each specific gray level. Fig. 6.1 showcases a grayscale image obtained from the FC-Micro hardware, containing a poorly diffused infrared (IR) light source for demonstration purposes.

Upon generating the histogram of the image (Fig. 6.2), the bi-modal nature of its

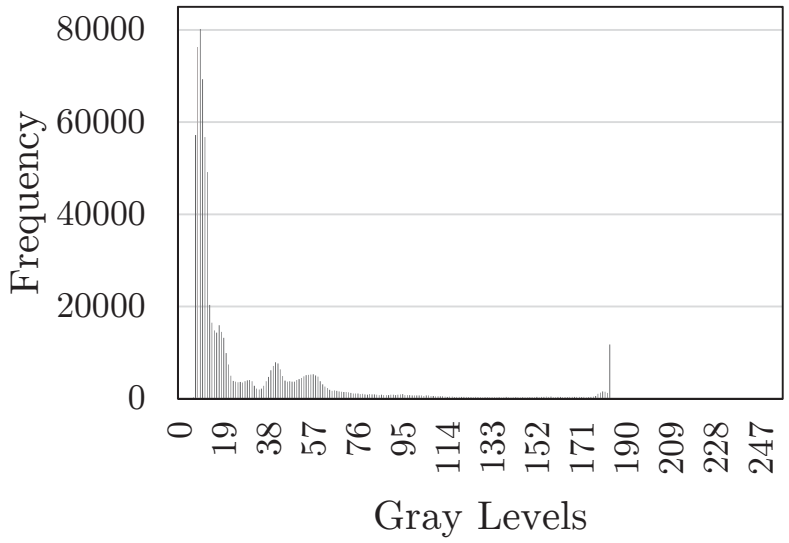


Figure 6.2: Historgram representation of the gray levels found in the image.

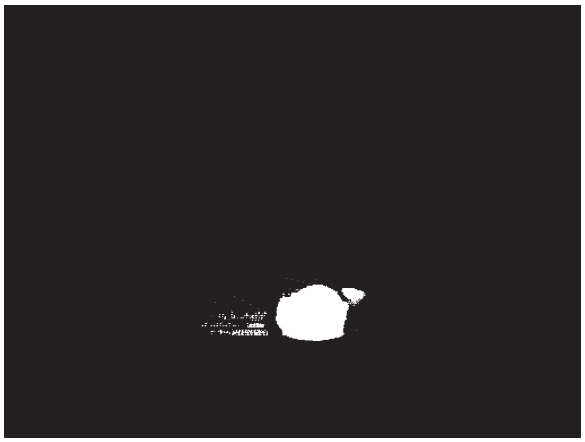


Figure 6.3: Thresholded image at optimal value obtained via manual thresholding.

configuration allows the optimal thresholding constant, T, to be determined by manual adjustments until the object in question is ideally isolated from the background. For this particular case, the left side of the plot contains most of the data, while few exist on the right indicating the image is primarily dark. Nonetheless, segmenting a IR light in an indoor test setting resulted in 181 as the ideal threshold. The segmented image under these conditions is displayed in Fig. 6.3. However, this value is only applicable in the environment which the experiments were undertaken and with a

(a) Improperly diffused IR LED with filter in front of the image sensor.

(b) Filtered IR light upon receiving thresholding.

Figure 6.4: The effects of an IR filter on image segmentation.

slight fluctuation in illumination, the T value would have to be adjusted to obtain the optimal segmentation. Furthermore, due to the poor nature of the diffusion, light is being reflected off its surroundings and even with the optimal threshold value, unwanted pixels still remain in the image.

Auto-thresholding techniques were developed in VHDL, in particular Otsu's method [150], enabling ideal segmentation. However, it was determined that placing an IR filter [151] in front of the image sensor removes a significant amount of background information, essentially performing pseudo-thresholding on the image as indicated by Fig. 6.4a. Therefore, the algorithm was not included in the final design as it added unnecessary complexity to the system. Nonetheless, exploiting the characteristics of filter, all wavelengths of light outside the constraints of filter's spectrum will be blocked. This ensures the pixel data relating to the IR light source will be white or near white, transforming all other pixels to black or near black. However, as residue light exists from the reflection of the IR light source, manual segmentation was still configured to optimally binarize the data, resulting in the image shown in Fig. 6.4b.

6.3 Classification of a Region of Interest

Upon determining the desired threshold value, a binarized rendition of the image can be generated to completely isolate the object (i.e., IR light spot) from the background. The resultant representation permits a variety of computer vision techniques to be implemented, with the outcome being a set of parameters defining an object's features. A powerful technique which provides optimal characterization of a region of interest is contour tracking (tracing); otherwise referred to as border following. This procedure identifies the pixels which are situated on the boundaries of an entity, essentially determining the location of an object within an image frame.

While a wide variety of of tracing algorithms exist ([152–154]), a form of contour tracking regarded as connectivity was researched for its parameter identification capabilities. More specifically, this algorithm aims to segment a discrete image into two classes, white pixels for regions of interest and black pixels for background, in order to generate high level descriptions of the various objects. There are two standard variations used to represent the perimeter, chain-code and crack-code, based upon 8-connectivity and 4-connectivity, respectively. As the crack code algorithm has been developed for other applications within the scope of the project, it will be addressed in this thesis. Connectivity refers to pixels which are next (connected) to one another [155, 156]. A small grid of pixels highlighting 4-connectivity in a binary image is shown in Fig 6.5. In this example P is connected to all four white pixels. However P_2, P_4, P_6 and P_8 are only connected to P directly when considering 4-connectivity.

Determining the equivalent classes of connected pixels in a binarized image (i.e., white pixels representing an object) can be referred to as connected component labeling. The image obtained from this algorithm results in a number of regions being labeled with a particular value. For example, a region identified as 1, the second 2, etc.

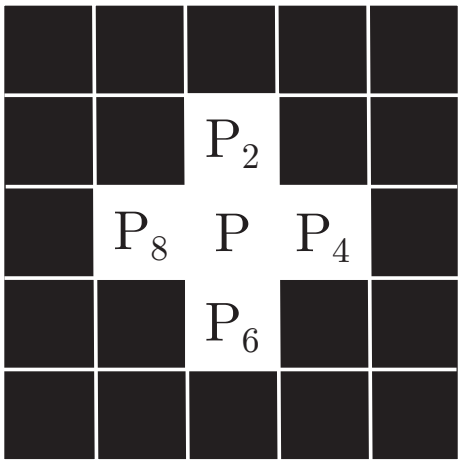


Figure 6.5: Small scale 4-connectivity example.

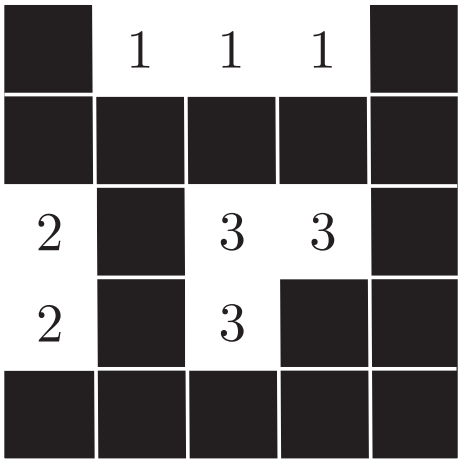


Figure 6.6: Connected componenet labeling of three small objects.

Fig. 6.6 presents an example of an image with multiple objects that has undergone connected component labeling. In this rudimentary example, three unique objects were identified and correspondingly labeled 1, 2 and 3.

The technique possesses the ability to locate each blob within an image on a single pass in a step-by-step process. Crack code requires a two bit value (i.e., 0,1,2,3) to define its codes and distinguishes the boundary of an object by considering the border of each pixel and outlining them appropriately as shown in Fig. 6.7.

A pixel P is identified as belonging to the class of objects (i.e., '1') in the image,

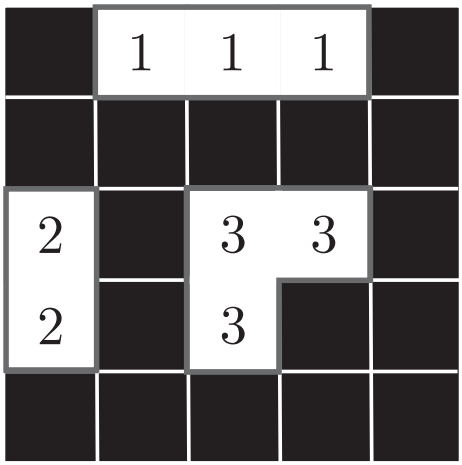


Figure 6.7: Object that has undergone border following and highlighting.

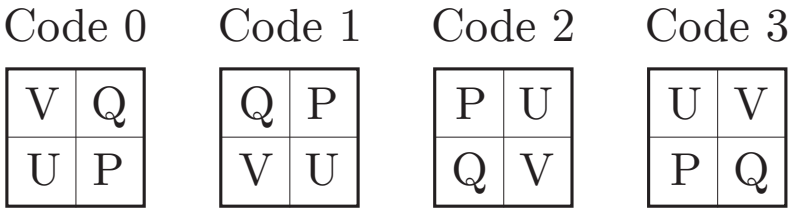


Figure 6.8: Determinataion of the crack code based upon a pixel's neighbors.

Table 6.1: Logic table for determining pixel locations, direction of tracing and new crack code.

U	V	P′	Q′	Turn	Code
X	1	V	Q	Right	Code - 1
1	0	U	V	None	Code
0	0	P	U	Left	Code + 1

while a neighboring pixel Q belongs to the background (i.e., '0'). The pixels U and V are specified based upon the position of Q relative to P (Fig. 6.8). Once the location of each pixel is recognized, one of the four codes are selected by evaluating the values of U and V as either '1' or '0'. These values also determine the next move, or the direction the algorithm should follow to continue along the boundary. A logic table representation of the algorithm is shown in Table 6.1.

Crack codes are used to describe regions of interest by separately coding each

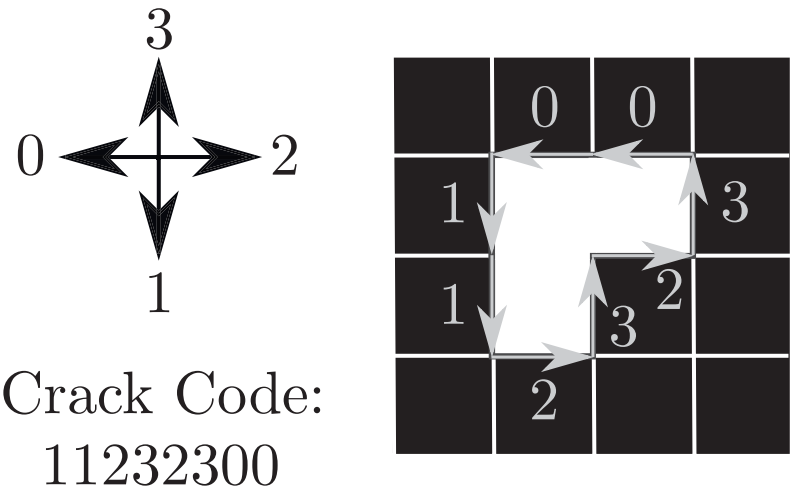


Figure 6.9: Results of the crack code algorithm on an object with little pixels.

connected component within the image. In addition, they are implemented as a means to determine the number of holes (black pixels surrounded by white) present. As mentioned, the navigation around the boundary of an object consists of moving in four directions, as a each pixel is represented as a square. In crack code, the code is determined not only by the direction, but by select pixels which neighbor the object. Fig. 6.9. highlights the determination of the four codes (i.e., 0,1,2,3), along with the results of the algorithm at each step based upon a small grid of pixels.

While fairly simple by design, it produces a powerful algorithm capable of recognizing objects, labeling the boundaries and calculating a variety of form parameters (i.e., perimeter, area, centroid, moments of inertia, etc.) which can be utilized for classification purposes. These form parameters are based upon the image moments of a recognized object, are automatically defined during the tracing of its contour and ideally, are independent of orientation, position and scale (i.e., distance of the object to the image sensor). The definition of a moment for a two-dimensional 2D

Table 6.2: Moment calculations based upon determined crack code

Code 0	Code 1
$M_{00} = M_{00}$ - y $M_{01} = M_{01}$ - Sum_y $M_{02} = M_{02}$ - Sum_{y^2} x = x - 1 $Sum_x = Sum_x$ - x $Sum_{x^2} = Sum_{x^2}$ - x^2 $M_{11} = M_{11}$ - ($xSum_y$)	$Sum_y = Sum_y$ + y $Sum_{y^2} = Sum_{y^2}$ + y^2 y = y + 1 $M_{10} = M_{10}$ - Sum_x $M_{20} = M_{20}$ - Sum_{x^2}
Code 2	**Code 3**
$M_{00} = M_{00}$ + y $M_{01} = M_{01}$ + Sum_y $M_{02} = M_{02}$ + Sum_{y^2} $M_{11} = M_{11}$ + ($xSum_y$) $Sum_x = Sum_x$ + x $Sum_{x^2} = Sum_{x^2}$ + x^2 x = x + 1	y = y - 1 $Sum_y = Sum_y$ - y $Sum_{y^2} = Sum_{y^2}$ - y^2 $M_{10} = M_{10}$ + Sum_x $M_{20} = M_{20}$ + Sum_{x^2}

continuous function is shown in equation 6.2,

$$M_{ij} = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} x^i y^j f(x,y)\, dx\, dy \tag{6.2}$$

where x and y are the current pixel locations, $f(x,y)$ is the 2D continuous function and i and j represent a particular moment. Image moments are the weighted averages of an object's pixel intensities, which is represented by equation 6.3.

$$M_{ij} = \sum_x \sum_y x^i y^j I(x,y) \tag{6.3}$$

Here, x and y are the current pixel locations, while $I(x,y)$ is the pixel intensity (i.e., '0' or '1' for a binary image) and i and j once again represent a particular moment. For example, M_{00} is the area of the object, or the number of while pixels contained within a binary image.

While implementing the crack code algorithm, each code realized affects the values of applicable moments and other variables used to calculate critical form parameters. In Table 6.2, the effect each code has on these values has been highlighted. As indicated by the tables, when a code has been determined, re-evaluating the moments and corresponding variables is a simple task that requires little mathematical processing. Upon fully realizing an object's contour, each of the image moments will be formulated and the required form parameters are calculated. In the case of tracking the IR light source, the two most critical features are the area and centroid (equation 6.4). Where $\overline{x}$ and $\overline{y}$ are the x and y pixel locations of the center of the object (i.e., centroid), M_{00} is the object's area in pixels and M_{10} and M_{01} are the raw image moments corresponding to the weighted sum of x pixel locations and y pixel locations containing a 1, respectively. These are capable of disregarding an entity of negligible size (i.e., noise present in the image) and defining a relative location of the center of the object within the image space.

$$\overline{x} = \frac{\overline{M_{10}}}{\overline{M_{00}}}, \quad \overline{y} = \frac{\overline{M_{01}}}{\overline{M_{00}}} \tag{6.4}$$

With these two parameters defined the algorithm relating to the automated targeting of an object can be pursued. It consists of utilizing the centroid and discrete values of the VCAs and forming a mathematical model which can produce two new digital positions, resulting in the centroid of the object being placed in the center of the image (Chapter 7). However, since the system is designed to be stored on a single FPGA chip, all of the required algorithms must be designed in hardware. This task requires the construction of a number of subsystems capable of working in parallel to determine the contour of an object and ultimately define its form parameters. Nonetheless, before discussing the contour tracking architecture, a brief overview of the hardware camera system and its functionality must be detailed.

6.4 Development of Identification and Characterization Techniques in VHDL

Due to the restrictive nature of hardware development, creating image processing algorithms is much more involved than high-level programming. Therefore, a large, interconnection of subsystems was designed with the aim of gathering an image, storing it in memory, isolating an object, defining its parameters within the image frame and outputting the findings through mathematical and visual means. The following section will detail these systems and their role in obtaining the necessary information in order to optimally follow the IR light source.

6.4.1 Hardware-Based Image Sensing System

Prior to employing either image processing technique, the pixel information must first be gathered from the image sensor and stored in memory which is suitable for hardware design and image manipulation. Therefore, a simplified form of the topology of the entire sensing and storage system designed in VHDL is shown in Fig. 6.10. As indicated, there are numerous modules involved in obtaining the pixel data and determining the parameters associated with a region of interest. Specified by the nature of HDL, each model executes upon the rising (falling) edge of a clock signal operating at a high frequency of 50 MHz.

To better illustrate its functionality, a run-through of each module is a necessity. Dictated by the architecture, read and write operations occur in parallel via the control of two static random access memory (SRAM) chips which act as data buffers for the image data. For the discussion, it will be assumed that *SRAM Controller 1* is entering a write state, while *SRAM Controller 2* is in a read.

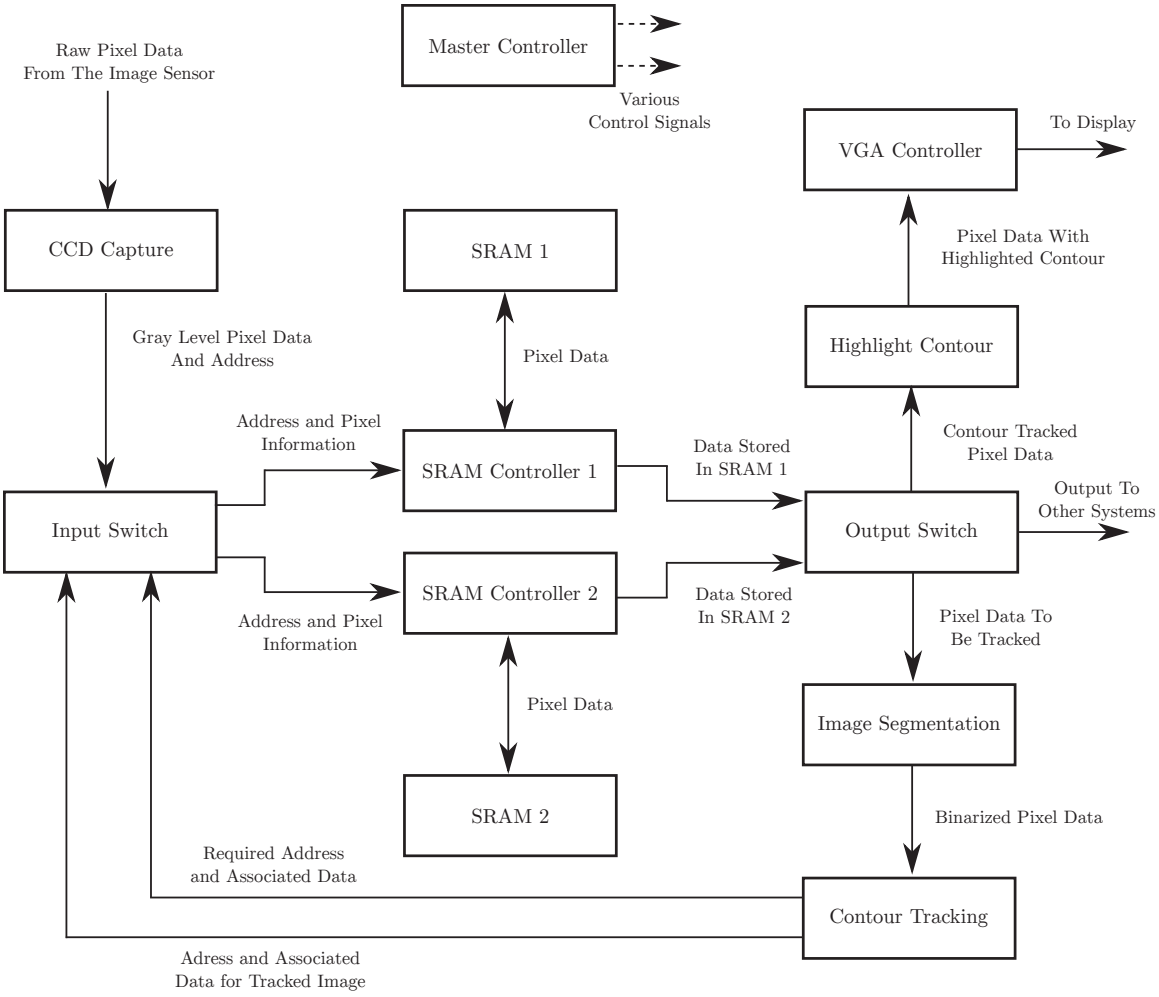


Figure 6.10: Hardware camera system topology.

The *Master Controller* module is considered the "brain" of the entire structure as it controls the capturing of an image frame, when contour tracking is executed and which state (i.e., read or write) each *SRAM Controller* should correspond to. Though connections were not included in Fig. 6.10 to avoid confusion, there are numerous control signals (i.e., clock, ready, mode, etc.) linking the *Master Controller*, to each subsystem.

Stepping through the design, the *CCD Capture* block begins gathering the raw pixel data, synthesizes the RGB value into an intensity (i.e., grayscale) representation

and outputs the modified data along with corresponding addresses to the *Input Switch*. This system, when signaled by the *Master Controller*, clocks the address and data along to *SRAM Controller 1*, a single address at a time. Since *SRAM Controller 1* is in write mode, it systematically stores the data to the memory of *SRAM1* and continues this process until all pixel information has been written.

As previous discussed, the parallel nature of the architecture permits the values stored in *SRAM2* to be accessed by other modules while *SRAM1* is being filled with data. At this point in the algorithm, the data being read from *SRAM2* is being processed by the *Contour Tracking* module. Note, the details pertaining to this system are discussed in section 6.4.2. Nonetheless, the *Contour Tracking* block requests data from a specified address in *SRAM2* which is then communicated to the *Output Switch*. As this segment of the algorithm is currently in the read state, the *Output Switch* passes the information along to the *Image Segmentation* subroutine, which binarizes the gray-level pixel data based upon a user-defined threshold.

The newly configured image data is processed by the *Contour Tracking* subsystem, with new data being requested until the entire image has been scanned for potential objects. When the boundary of an object is discovered the *Contour Tracking* module changes the data from '1' to a specific value relating to a color code utilized by the *Highlight Contour* block. This value is communicated to the *Input Switch* which passes it to *SRAM Controller 2*, overwriting the number in memory with the color code data. The procedure continues until the entire image is processed and upon completion, all data contained within *SRAM2* is systematically transmitted to the *Output Switch* once again. Since these pixels have been correctly modified, the pixel values on the boundary of all located objects are colorized by the *Highlight Contour* module and finally, the resultant image is displayed on an external monitor by way of the *VGA Controller* routine. This entire section of the algorithm finalizes before the data has

been written to *SRAM1* to ensure *SRAM2* will be finished with all the frame data before being overwritten.

6.4.2 VHDL Contour Tracking Architecture

In similar fashion to the overall camera system, Fig. 6.11 highlights a simplified version of the contour tracking VHDL architecture. Each block has a very specific role in the overall functionality of the contour tracking algorithm. While some modules have little effect on the algorithm itself, they provide a visual means to validate the results of the design. The parallel nature and complexity of the contour tracking architecture prevents a discussion of the algorithm as a step-by-step process. Therefore, each of the subsystems will be individually detailed to give a better understating of the overall system. Furthermore, many connections were not included in the topology to allow visual clarity of the design, though notable signals are still mentioned within the discussion of each module.

Generate Scan Addresses: The aim of this module is to increase speed and overall functionally of the algorithm by disregarding the majority of pixel data to be examined within an image frame. Restricting object scanning to a selection of rows, with the spacing between rows dependent upon a user-defined value, prevents the wasteful process of checking each pixel. Furthermore, this technique reduces the number of tiny objects identified, which are usually identified as noise. Upon defining the desired address, it delivers it the *Output Controller*, in turn transmitting it externally to the *Input Switch* of the sensor system. Note, when the final address is reached, it communicates a "done" signal to the *Master Controller*, allowing the information to be safely deleted from the corresponding SRAM.

Generate Labels: The primary objective of this routine is to select a color for the

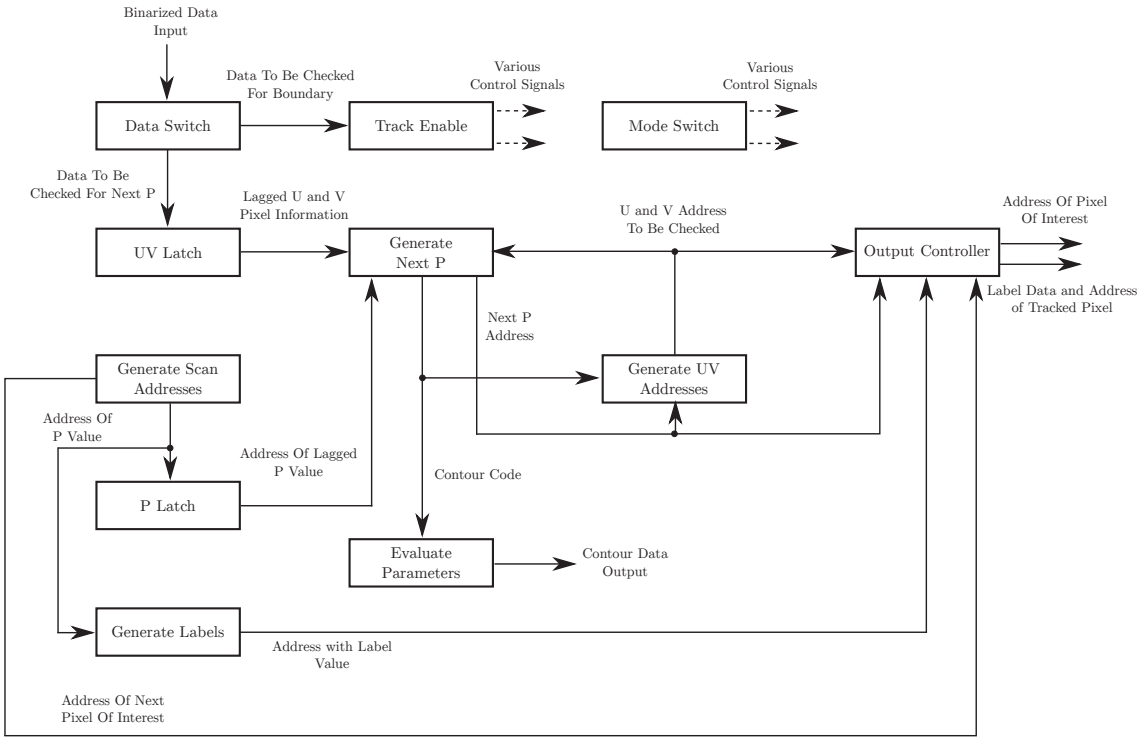


Figure 6.11: Topology of the hardware-based contour tracking architecture.

boundary of the tracked object by assigning it a 8-bit number. If more than one object has been recognized in the current set of data, it simply increments the value accordingly. The number is delivered via the *Output Controller* module which sends it externally for use in the image sensing display modules (i.e., *Highlight Contour* and *VGA Controller*).

Track Enable: The pixel data corresponding to the address generated by *Generate Scan Addresses* is inputted into this block via the *Data Switch* routine, essentially scanning all of the incoming data until an object is found (i.e., a '0' value transitioning to '1'). Upon recognizing a variation in the binary data, a signal is outputted to *Generate Labels* to ensure it begins producing the label colors pertaining to the object's border. In addition, it triggers a signal in *Mode Switch* to indicate to start of contour tracking. Due to the reliance on clock triggering in the algorithm, the *Track Enable*

module lags behind the *Generate Scan Addresses* subsystem by two clock cycles. Therefore, when *Track Enable* identifies an object, the corresponding address relates to two pixels behind the current address being considered. However, to compensate, *P Latch* holds the address from two clock cycles prior, ensuring contour tracking begins and continues by utilizing the correct address.

Mode Switch: Receiving the command from *Track Enable*, this module's function is to identify which state the contour tracking algorithm should be in; either border following or object scanning. Upon defining the mode, it generates a control signal which is delivered to a number of subsystems including the *Track Enable*, *Generate Scan Addresses*, *Generate Next P* etc., forcing them into the correct functionality.

Generate Next P: This module contains the fundamental design behind contour tracking as it is primarily responsible for generating the next crack code based upon the values of U and V, with respect to location of P in the image. It receives these addresses, which are lagged behind the P currently being selected as previously discussed, from the *UV Latch* and *P Latch* routines, respectively. Upon determining their locations in the image frame, the appropriate crack code is identified as detailed in section 6.4.1. This is communicated to the *Generate UV Addresses* and *Evaluate Parameters* modules for further processing. In addition, the next P address under consideration is determined and delivered to the *Generate UV Addresses* and *Output Controller* subsystems to proceed in the tracing of the border. Finally, if the P address is found to be the starting address, a "done" signal is transmitted to a number of modules, resetting the algorithm, ensuring it continues to scan for additional objects.

Generate UV Addresses: Upon receiving the P address and contour code from the *Generate Next P* routine, this module formulates the appropriate addresses of U and V for the purpose of determining the value of these locations in memory. This

information is transmitted to the *Generate Next P* block to be utilized in determining the next P address to be considered. Furthermore, the U and V addresses are delivered to the *Output Controller* which requests the pixel data at these locations from the memory.

Output Controller: The *Output Controller* block is the gateway between the contour tracking architecture and the image sensor architecture. In essence, its primary function is to request addresses and data information dependent on the current state of the algorithm and output the traced boundary information.

Evaluate Parameters: The *Evaluate Parameters* module is responsible for generating the parameters which are the primary focus of the contour tracking algorithm. Receiving the contour code from the *Generate Next P* routine, it evaluates all of the pertinent moment information of the object undergoing border following. Upon completely defining the boundary, the calculated values are transmitted outside the contour tracking architecture to be implemented by other functions. More specifically, the centroid and area of the object is utilized by the ATM. Note, to reduce resource costs, a number of variables and moments are not formulated as they are unneeded to produce the required parameters.

Fig. 6.12 showcases the results of a recognized object (i.e., the LED light spot) with its contour highlighted. Note, its large size was mandatory to showcase the contour tracing results. Nonetheless, the contour tracking for this particular image frame resulted in an x and y centroid value of 480 pixels and 493 pixels, respectively, with its area being 4463 pixels^2. Finally, with the moment data determined, the values are communicated to the microcontroller via the shared memory architecture, allowing for the further development of the ATM.

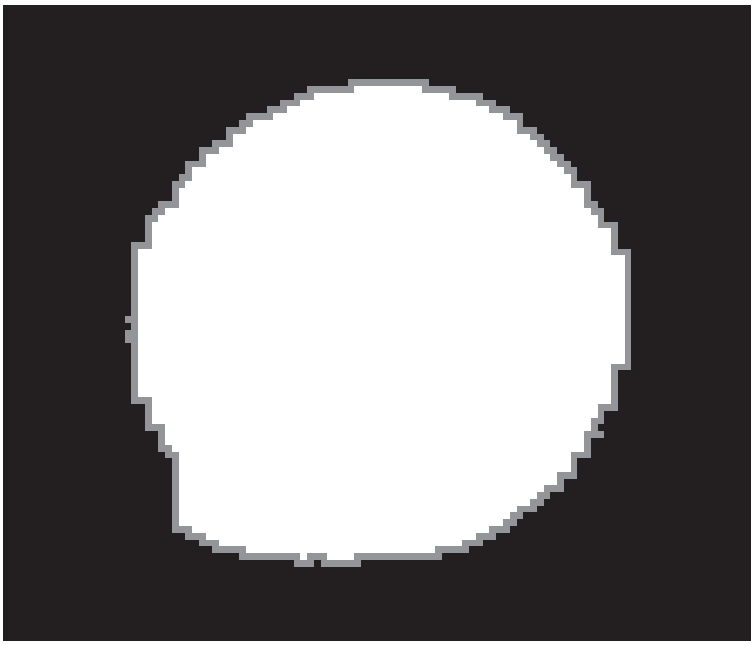


Figure 6.12: Object with highlighted border resulting from the contour tracking algorithm.

6.5 Conclusions

Utilizing the capabilities and reliability of the FC-Micro PCB, hardware based image processing techniques were employed with the express purpose of identifying a region of interest and its characteristics in real-time. In particular, image segmentation was performed on the grayscale modification of an RGB image resulting in an ideal method for isolating the object of interest from the background pixel information. Building upon these achievements, a contour tracking technique, known as the crack code algorithm, was generated in VHDL which provided vital characteristics of the isolated region of interest (i.e., the light spot). By doing so, the location of the centroid of a light spot relative to the image's coordinate frame was realized, allowing for targeting of an IR light source at high rates to be pursued.

Chapter 7

Modeling an Automated Targeting Mechanism Utilizing Design of Experiments Methodology

A system capable of isolating a moving object and sustaining a continual, accurate fix requires exceptionally fast positioning and processing functionally. By taking advantage of the highly dynamic POM architecture and the embedded nature of the FC-Micro PCB, a robust mechanism capable of maintaining a localized lock on an object was assembled. Utilizing the power of DOE methodology, a system of non-linear equations were generated by relating the VCA locations and centroid of an object to the discrete actuator values which result in the object being positioned in the center of the image frame. Due to the complex nature of the equations, the communication link between the FPGA and microcontroller devices was employed to deliver the image characteristics to the microcontroller. Justification of the mathematical model was determined by comparing the centroid produced by the adjusted actuator positions with the center point of the coordinate frame. Correspondingly, the dynamics of the system was validated through the targeting of a moving object while the system underwent rapid displacements, resulting in a agile, accurate targeting mechanism.

7.1 Introduction

Automated object targeting utilizing highly dynamic architecture is an essential optomechatronic application with many examples provided in the literature [5,26,91,157]. In particular, mechanisms composed of PKM/POM devices in contrast of commonly used gimbals-based mechanisms has become a recurring theme [37,38]. While there are many available off-the-shelf systems capable of performing rudimentary targeting, many fail when agility and precision is necessary. Correspondingly, maintaining a precise lock on a mobile object while the ATM experiences disturbances is a very complex problem as there are two conflicting motion profiles to consider. In response, a high speed, extremely accurate system must be employed to ensure all motion is corrected..

The proposed real-time targeting mechanism contains three specific functions that are fundamental to its design. To begin, the ability to recognize, isolate and formulate essential characteristics of an object in a predefined FOV; a task accomplished in Chapter 6. Secondly, the capacity to maintain a localized fix on the recognized object based upon the defined parameters. Finally, the quick and accurate control of multiple VCAs for the purpose of manipulating the POM's mobile platform.

Inspired by the high dynamic nature of the POM structures, the stand-alone sensing board discussed in (Chapter 5) was integrated into their mobile platforms for the implementation of an ATM. Three configurations were considered, two 2DOF POMs containing a 5 mm [143] and 50 mm [158] lens respectively, and the 3DOF POM with the same 5 mm lens. The object chosen to be recognized and ultimately targeted, was an infrared light source, as it is easily isolated from common wavelengths and for its abundant use in FSOC systems. While the kinematic model of the system was realized through camera calibration techniques, it was determined that

this method resulted in inaccuracies due to the resolution of the image sensor, lens distortion and the parasitic nature of the POM. Therefore, utilizing the parameter information garnered from Chapter 6, a mathematical model of the system was defined via design of experiment methodology. These complex equations were reconfigured to be implemented within the microcontroller. The object characteristics, VCA positions and model were connected by way of the memory controller on the FC-Micro board to produce a fast, highly functional system which is also capable of solving high order, non-linear equations.

Combining the structure and algorithms, a precise, high speed, self-contained ATM was realized. The device boasts the ability to position an IR source in the center of the image sensor's FOV, while actively compensating for self-experienced motion. The HDL and microcontroller algorithms as well as the mechanism's model and configuration will be detailed in the following sections.

7.2 Modeling the ATM with DOE

The statistical design of experiments is a systematic method implemented to define the cause-and-effect relationship between the interaction of multiple variables (i.e., factors, predictors, etc.) on a system, in addition to the response of the output of the system [159]. The starting point of a DOE study begins with determining the objectives of the experiment and choosing the process factors and desired outcomes. This information is required in order to optimize the output and formulate an appropriate mathematical model to relate the input variables to the system's response. As a more in-depth discussion of DOE is beyond the scope of this thesis, please see [160] for more information.

Table 7.1: DOE parameters.

Factors	Responses
Actuator One's Current Position (ADC Counts)	D1 (ADC Counts)
Actuator Two's Current Position (ADC Counts)	D2 (ADC Counts)
Object's X Center Point (Pixels)	
Object's Y Center Point (Pixels)	

7.2.1 2DOF POM Model Generation with 5 mm Lens

The goal of pursuing a DOE study was to generate a system of equations capable of formulating a set of discrete VCA positions to place the centroid of an IR light spot (i.e., the object) in the center of the image frame. However, the current VCA and centroid locations must be factored into the equation to determine the correct response. Thus, four inputs (i.e., actuator one and two's discrete position and the object's x and y center point locations) and two outputs (i.e., VCA one and two's desirable positions) were required to execute the experiment. Correspondingly, the upper and lower bounds for each actuator were chosen to be 55,000 and 10,000 ADC counts, respectively, in order to avoid any potential positioning errors near the ends points of the PSD. The limits of the x and y center point locations were simply the size of the image frame in pixels, or 0-1023 for the x and 0-767 for the y. The experiments were generated by employing a response surface study, using an optimal design type as it is more suited for higher order systems (i.e., greater than quadratic). Finally, the inputs, outputs, upper and lower bounds were placed into the Design Expert 10.0 software, with Table 7.1 showing the factors and responses of the experiment.

To perform the analysis, a target was manufactured from acrylic via a laser cutting machine to ensure accurate reference points during the experimentation (Fig. 7.1). It was securely fastened to a frame composed of 80/20 aluminum railings and positioned approximately two feet away from the 2DOF POM. Furthermore, the POM was

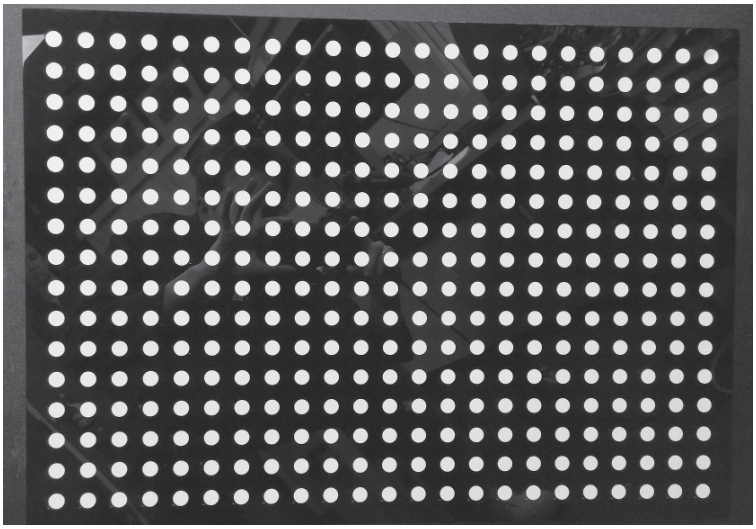


Figure 7.1: Laser etched acylic sheet utilized in model determination and experimenation.

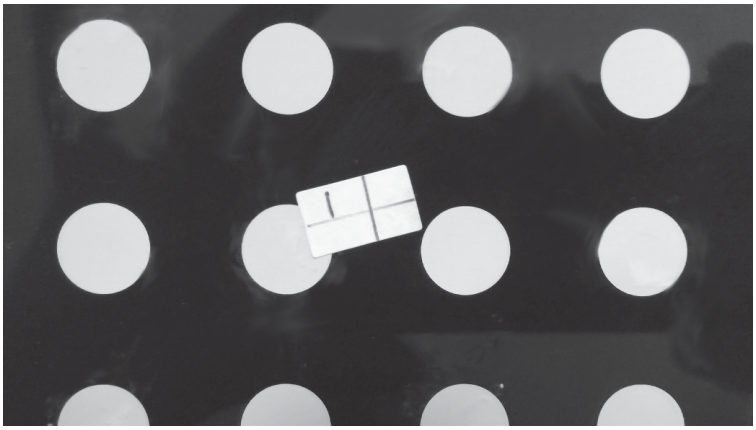


Figure 7.2: Sticker containing a cross-shape for model generation.

securely fixed to a heavy table ensuring unwanted displacement and vibrations did not affect the results.

At the start of each test, the actuators were displaced to the locations specified by Design Expert. Upon settling, the discrete positions were recorded to ensure no discrepancy was present in the VCA location in comparison with the DOE generated values. Subsequently, the pixel data gathered by the image sensor was stored as a 1024x768 image in order to determine the whereabouts of the center point (generated by DOE) in question via Matlab. Upon obtaining the desired position in the image

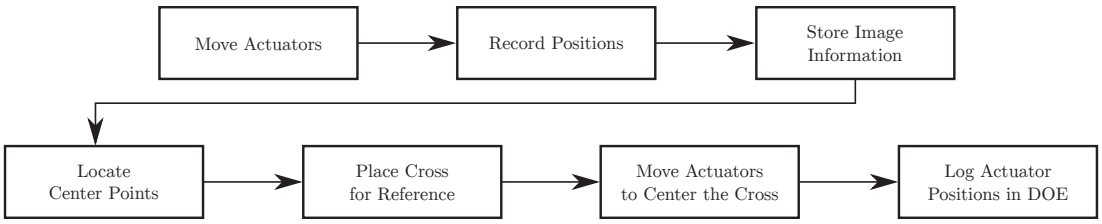


Figure 7.3: Flow chart of the experimental procedure.

Table 7.2: Statistical regression results of DOE modeling with the 2DOF, 5mm arrangement

Order of Model	Actuator One			Actuator Two		
	σ	R^2	Predicted R^2	σ	R^2	Predicted R^2
Linear	5,550.68	0.8815	0.8463	3,935.82	0.9604	0.9492
Quadratic	4,163.43	0.9422	0.8102	2,919.46	0.9811	0.9476
Cubic	1,366.82	0.9957	0.8854	1,023.75	0.9984	0.9403
Quartic	280.31	0.9999	0.9619	723.67	0.9998	0.9660

Note: σ = standard deviation in ADC counts.

frame, a cross was added to the target to garner an accurate point of reference (Fig. 7.2). The linear motors were then repositioned to place the midpoint of the cross in the center of the image displayed on an external monitor. Upon completion, the new actuator values were logged and correspondingly entered into the Design Expert framework. The entire process was repeated 80 times in order to fulfill the requirements generated by the software. A flow chart of the experimental steps is shown in Fig. 7.3.

Finalizing all tests resulted in a variety of systems of equations capable of relating the discrete position of each VCA and centroid of an object to adjusted VCA locations, centering the object in the image frame. To select the ideal model, Table 7.2 highlights the more noteworthy statistics under consideration, which were gathered from the software.

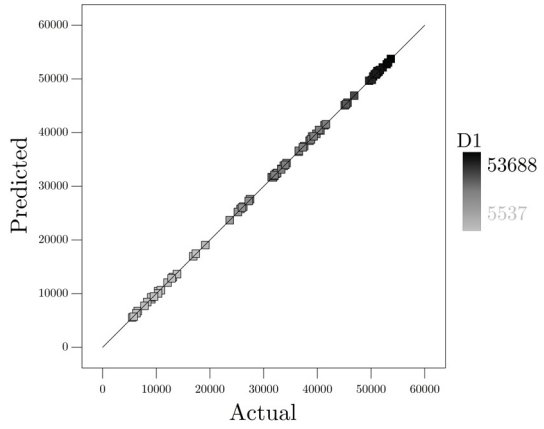
As shown, the quartic models seem the most promising, due to its low standard deviation and high R^2 and predicted R^2 values. Correspondingly, it was selected as

the optimal set of equations to serve the ATM's needs. The complexity of the quartic model relating to actuator one is partially displayed equation 7.1, where $D1$ and $D2$ are the current actuator locations and X and Y are the center points of the object.

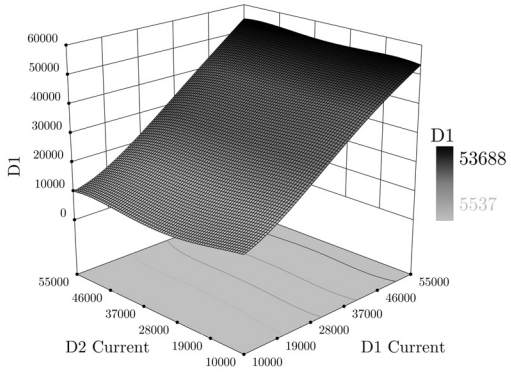
$$
\begin{aligned}
&D1_{NEW} = \\
&73025.18 + 0.38D1 - 1.68D2 - 250.50X - 111.40Y + 3.07e^{-5}D1D2 + 0.19XY + 2.21e^{-5}D1^2 \\
&- 2.290e^{-5}D2^2 + 0.57X^2 - 0.07Y^2 + 3.79e^{-8}D1D2X + 4.22e^{-8}D1D2Y + 3.86e^{-6}D1XY \\
&+ ...41\ terms... \\
&- 1.31e^{-9}D1X^3 + 7.406e^{-9} + 6.20e^{-9}D2X^3 - 5.63e^{-9}D2Y^3 + 5.69e^{-8}X^3Y \\
&+ 7.60e^{-7}XY^3 + 6.97e^{-15}D1^4 - 1.21e^{-14}D2^4 + 2.216e^{-7}X^4 - 5.16e^{-7}Y^4 \quad (7.1)
\end{aligned}
$$

While models in the following sections produce similar lengthy equations, they will not be included in the thesis to prevent tedium and repetition. However, equation 7.1 was added to highlight the complexity of the models and the extreme difficulty an FPGA would have performing the calculations. Nonetheless, Fig. 7.4 presents the predicted versus actual and the response surface method (RSM) 3D plot formulated from the results of the model equations.

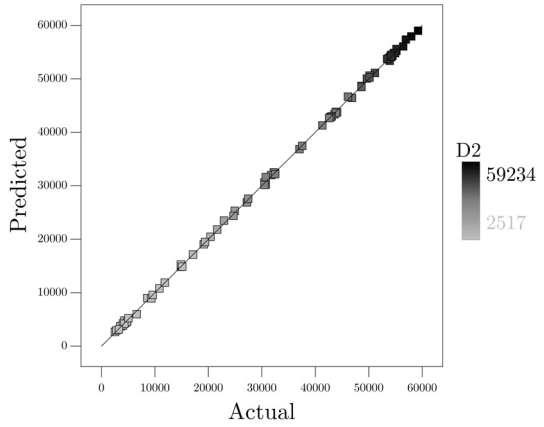
The figures highlight the reaction both actuator positions (i.e., *D1 Current* and *D2 Current*) have on the outcome of the equations (i.e., *D1* and *D2*). Similar results can also be concluded when considering the effect of the x and y center points. However, presenting all factor combinations does not further validate the model. Note, all other plots referring to the DOE outcomes will use these parameters for consistency and to prevent tedium. Nonetheless, as indicated by Fig. 7.4, the model-predicted actuator positions are very similar to the original values recorded while testing. More in-depth validation of these model equations is described in section 7.3. Note, henceforth,



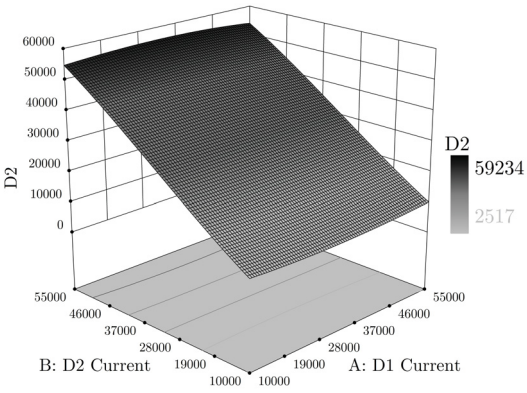
(a) Predicted values generated by the model of actuator one with respect to the actual values recorded during experimentation.



(b) Response surface relating actuator one's current position to its discrete position resulting of centering of an object.



(c) Model's predicted results of actuator two's location with respect to the actual values.



(d) 3D surface plot relating VCA two's current position to its discrete location.

Figure 7.4: Results of the DOE quartic models pertaining the the 2DOF POM containing the 5 mm lens.

to prevent confusion and monotony, the model representations of the 2DOF, 5 mm lens configuration, the upcoming 2DOF, 50 mm lens and the 3DOF, 5 mm lens arrangements will be referred to as the 2DOF-5, 2DOF-50 and 3DOF-5, respectively.

Table 7.3: Results of DOE model generation for the 3DOF-5 configuration

Order of Model	Actuator One		Actuator Two		Actuator Three	
	σ	R^2	σ	R^2	σ	R^2
Linear	5,758.71	0.7722	6,457.10	0.8853	6,361.92	0.8593
Quadratic	5,093.76	0.8423	5,907.68	0.9151	5,708.85	0.8998
Cubic	4,551.40	0.9124	4,935.61	0.9588	5,363.74	0.9385
Quartic	4,753.45	0.9881	4,703.90	0.9953	2,929.47	0.997

Note: σ = standard deviation in ADC counts.

7.2.2 3DOF POM Model Formation

As identified in Chapter 3, the 3DOF outperforms the 2DOF in many aspects. However, due to its extremely coupled nature, the orientation of a point in space can be reached by a number of combinations of the three actuator positions. Therefore, developing a reliable model of the system is extremely problematic as multiple inputs can generate the same output. Nonetheless, for comparison, validation purposes and to prove its lack of dependability, modeling was pursued. Since the additional linear motor corresponds to an extra input, Design Expert required 136 experimental runs in contrast with the 80 for the 2DOF representation. Mimicking the tests of the 2DOF-5 experiment, the trials were completed with extremely unimpressive results, as shown in Table 7.3.

As theorized, all models result in poor performance, with large standard deviation in the outcome and generally low R^2 values. Note, the predicted R^2 values were not included but were inferior to the 2DOF-5 tests. Nonetheless, as a means to refine the model, an additional 50 runs (186 total) were added to the experiment and completed thereafter. Unfortunately, the extra effort did not drastically effect the results, providing worst outcomes in many cases, (Table 7.4), further verifying the ineffectiveness of the 3DOF POM for this particular procedure.

Table 7.4: Parameters defined by the additional runs in the 3DOF-5 model formulation

Order of Model	Actuator One		Actuator Two		Actuator Three	
	σ	R^2	σ	R^2	σ	R^2
Linear	5,475.64	0.7610	8,613.28	0.7860	6,141.24	0.8576
Quadratic	4,932.42	0.8223	8,438.86	0.8117	5,626.97	0.8904
Cubic	4,722.64	0.8716	8,308.73	0.8562	5,224.69	0.9256
Quartic	3,073.88	0.9749	8,222.26	0.9350	4,889.44	0.9699

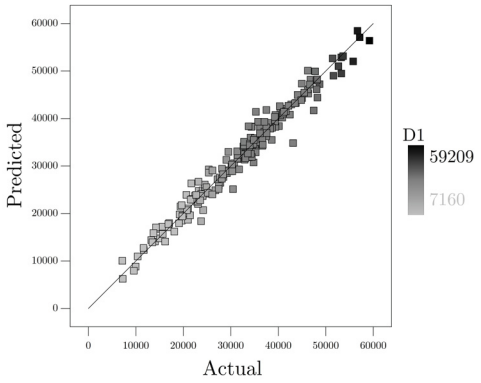
Note: σ = standard deviation in ADC counts.

From the results of additional experimentation, the standard deviation and R^2 were poorer overall despite the additional runs, indicating the impracticality of generating workable models in conjunction with the 3DOF POM. Nevertheless, the quartic models relating to each actuator for the initial experimentation (i.e., less runs) have the optimal response, though, only by a tiny margin. Thus, these were selected as the candidate equations. As a visual comparison to the 2DOF-5 models, the predicted versus actual and response surface plots for each actuator are presented in Fig. 7.5.

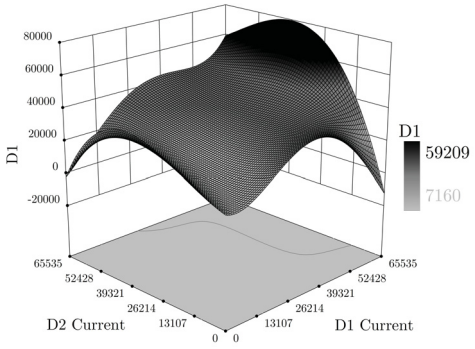
As indicated, the predicated outcomes of the model fail in comparison to the 2DOF results, with many outliers and large deviations. Correspondingly, the RSM plot is extremely non-linear, proving targeting is inaccurate. Nonetheless, despite the unimpressive performance, a number of test procedures were completed as a final validation of the poor operation of the model. The outcomes are detailed in section 7.3.

7.2.3 2DOF Narrow FOV Lens Model

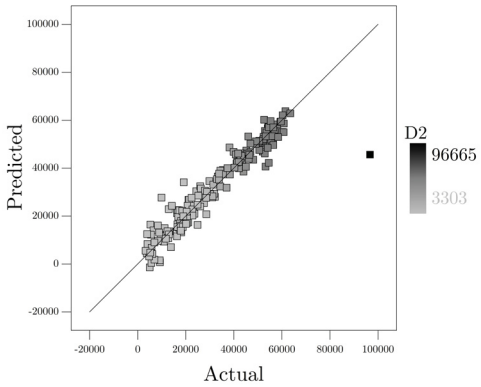
While the results of the 2DOF-5 model were promising, ultimately a narrow FOV lens, with a larger focal length must be employed in conjunction with the FSOC system to increase the distance of the transmission (Chapter 8). Therefore, the 5 mm lens attached to the image senor board was replaced with a 50 mm rendition. With the new lens incorporated, Design Expert was utilized once more to produce a series of



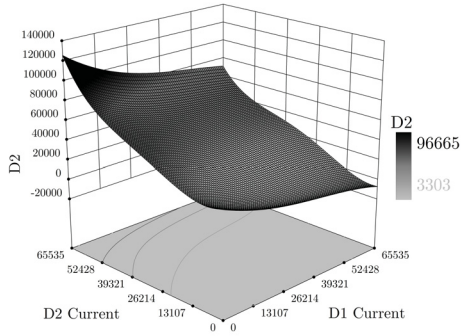
(a) Predicted values for actuator one in comparison to the recorded positions.



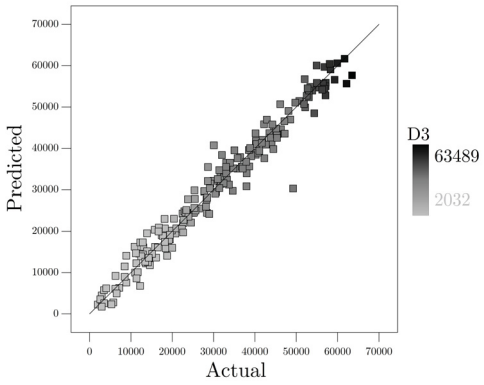
(b) 3D plot referring the new actuator position to the current locations.



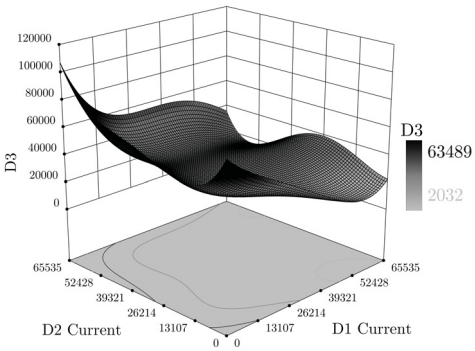
(c) VCA two's predicted outcomes versus the experimental data.



(d) Response surface showcasing actuator two's updated position.



(e) Actuator three predictions by the model with respect to the locations logged during testing.



(f) 3D surface plot highlighting the effect of the current VCA locations on the outcome of actuator three's model.

Figure 7.5: 3DOF-5 quartic model results generated by Design Expert.

Table 7.5: DOE statistical regression results of the 2DOF-50 arrangement

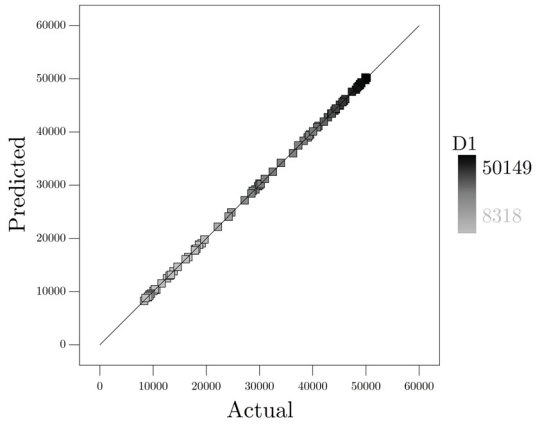
Order of Model	Actuator One			Actuator Two		
	σ	R^2	Predicted R^2	σ	R^2	Predicted R^2
Linear	172.48	0.9999	0.9998	136.70	0.9999	0.9999
Quadratic	159.59	0.9999	0.9998	141.42	0.9999	0.9999
Cubic	156.79	0.9999	0.9998	140.96	0.9999	0.9999
Quartic	147.34	0.9999	0.9960	125.62	0.9999	0.9974

Note: σ = standard deviation in ADC counts.

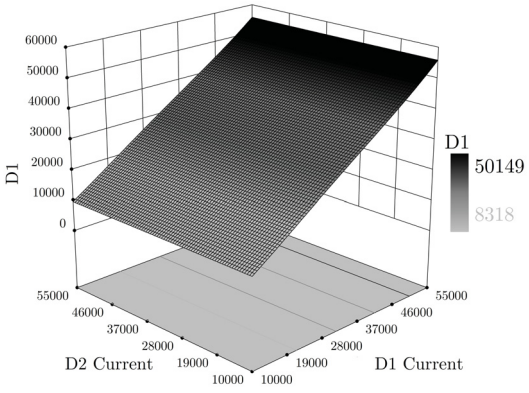
tests similar to section 7.2.1. However, due to the zoomed in nature of the 50 mm lens, a small adjustment in either actuator resulted in significant displacement of the image sensor's FOV. In response, the POM was situated before a large, blank wall as a replacement for the acrylic target. With the setup in place and following the procedure dictated in section 7.2.1, the 80 tests were completed with the outcomes shown in Table 7.5.

Unexpectedly, the results far outclass both the 3DOF-5 and 2DOF-5 versions, with all models generating optimal equations for both VCAs. The unanticipated findings likely stem from the notation that a tiny actuator displacement relates to a tremendous adjustment in the image sensor's FOV. Therefore, the linear motors move very little when situating the object in the center of the frame, preventing non-linearity from appearing in the model. Despite the outcomes of the DOE modeling declaring the quartic equations as generally ideal, verification involving both linear models was also pursued (section 7.3) as comparison in performance. Nonetheless, the optimal results were chosen for visual representation as depicted in Fig. 7.6.

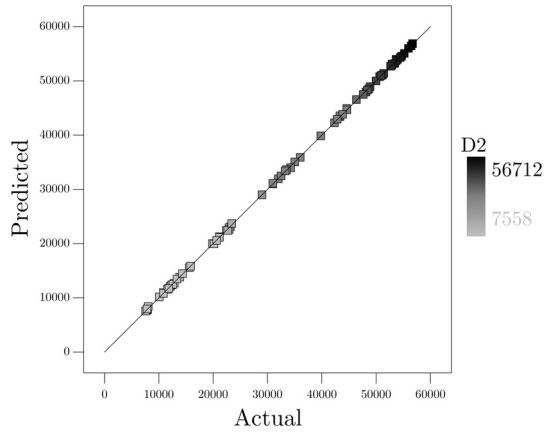
As expected, the predicted values closely match the actual recorded discrete positions. Correspondingly, the contour and RSM figures are linear in nature, suggesting that the linear models may be a suitable fit. Furthermore, these plots resemble the



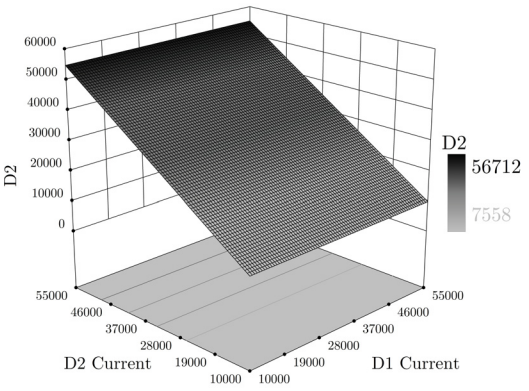
(a) Predicted values of actuator one versus the actual values recorded during experimentation.



(b) Current actuator positions and their effect on the outcome of VCA one.



(c) VCA two predicted values with respect to the data obtained while testing.



(d) 3D plot relating the actuator two's current positions to its discrete position.

Figure 7.6: Quartic model results relating to the 2DOF POM with integrated 50 mm lens.

results of the 2DOF-5 model and once again indicate the linear relation between the actuators and mobile platform of the 2DOF POM.

7.3 System Verification and Specifications

Though the results from the DOE methodology seemed impressive for the 2DOF architecture, physical experimentation must be completed in order to validate the models. Correspondingly, a series of tests were instantiated to verify each model's capacity to correctly center the object in the image frame. Furthermore, an important factor under consideration was ensuring that the model's accuracy is independent of scale (i.e., the targets distance from the image sensor). Thus, the 2DOF-5 lens equations were tested with the acrylic target being located at three different distances from the image sensor: 12 inches, 24 inches and 60 inches.

At each interval, a varied set of 20 positions corresponding to each actuator, in addition to 20, x and y values representative of the centroid of an object in the image (i.e., the center of an IR light spot), were generated by way of the Latin Hypercube to ensure near-randomness in the data set. Each of these values was entered into the non-linear equations defined by the DOE modeling (section 7.2.1) resulting in two discrete positions which would relocate the object to the center of the image. Furthermore, to ensure noise was not a factor, the VCAs were displaced to these 20 positions three times for each distance; giving a total data set of 60 values per interval.

The testing procedure mirrored the DOE experimental runs (section 7.2.1) up to and including placing the cross on the target. Subsequently, utilizing the outcome of the DOE model, the linear motors were relocated to the intended positions and upon coming to rest, their discrete locations was recorded to ensure error in positioning was not an factor in experimentation. Furthermore, the image sensor gathered the pixel

Table 7.6: 2DOF-5 model's determined accuracy obtained from three different distances

Parameters	Results at Various Target Distance's From Image Sensor		
	12 inches	24 inches	60 inches
X Average (pixels)	13 (2.49)	15 (2.96)	9 (1.81)
Y Average (pixels)	14 (3.57)	19 (5.00)	10 (2.70)
X Max (pixels)	33 (6.45)	35 (6.84)	21 (4.10)
Y Max (pixels)	37 (9.64)	44 (11.46)	24 (6.25)
X σ (pixels)	9 (1.78)	10 (2.04)	7 (1.34)
Y σ (pixels)	11 (2.94)	11 (2.73)	6 (1.44)

Note: the values in brackets correspond to the distance each pixel varies from the center point as a percentage.

Table 7.7: 3DOF-5 model accuracy results

Parameter	Experimental Results from Quartic Models
X Average (pixels)	219 (42.73)
Y Average (pixels)	174 (45.39)
X Max (pixels)	464 (90.63)
Y Max (pixels)	330 (85.94)
X σ (pixels)	113 (22.17)
Y σ (pixels)	105 (27.50)

Note: the values in brackets correspond to the distance each pixel varies from the center point as a percentage.

information, storing it once again. Finally, the location of the center point of the cross in the image was compared with the x and y center values of the coordinate frame. For this sensor, this equates to $x = 512$ and $y = 384$. Note, the 3DOF-5 and 2DOF-50 were tested in similar fashion, but did not undergo tests at a variety of distances. Upon the completion of each models experimentation, the data was analyzed with the results presented in Tables 7.6, 7.7 and 7.8.

For each model, the average and maximum value which the x and y center points differ from the midpoint of the image frame were formulated. In addition, the standard deviation pertaining to each model was also defined. As shown in the tables, these values are presented in both pixel and percentage to give a more thorough understanding of the systems.

Table 7.8: 2DOF-50 model accuracy results for two distinct models

Parameters	Results at Different Order of Model Equations	
	Both Linear	Both Quartic
X Average (pixels)	27 (5.38)	41 (8.10)
Y Average (pixels)	14 (3.76)	67 (17.47)
X Max (pixels)	52 (10.16)	172 (33.59)
Y Max (pixels)	48 (12.50)	152 (39.58)
X σ (pixels)	17 (3.32)	50.1 (9.79)
Y σ (pixels)	11 (2.86)	44.2 (11.53)

Note: the values in brackets correspond to the distance each pixel varies from the center point as a percentage.

The 2DOF-5 performed extremely well and was not affected by scaling as indicated by the comparable values delivered at each distance. Both 2DOF-50 models were very accurate as well, with the linear equations outclassing the quartic renditions slightly. Proving that the system is better approximated by a linear model, likely due to short VCA motions relating to large displacements of the image sensor. Nonetheless, its accuracy is less than the 2DOF-5 which is likely the result of the extra weight and size from the larger lens, increasing the payload and negatively effecting the systems dynamics and controller performance. Finally, it was theorized that the 3DOF would be incapable of precise targeting employing DOE methodology, which is confirmed in Table 7.7. As indicated, the x and y center point locations vary significantly, with and average of over 55% and 38% for the test scenario, validating the choice to pursue a ATM comprised of the 2DOF POM.

7.4 Targeting Algorithm Implementation

Combining the non-linear equations relating to the 2DOF-5 model, with the contour tracing's ability to identify an object and determine its characteristics, the real-time automated targeting of objects was capable. As the model equation (7.1) contains

Table 7.9: VCA positions during scanning mode.

	B.Left	T.Left	B.Right	T. Right
VCA 1	15,000	15,000	45,000	45,000
VCA 2	15,000	45,000	15,000	45,000

Note: All values are in ADC counts.)

an abundance of multiplications it is too resource intensive to develop on the FPGA. Therefore, the majority of the targeting algorithm is designed in C code to take advantage of its ability to process non-linear algebra efficiently. Furthermore, the communication link between the FPGA and microcontroller enables the effortless transmission of information between the devices. The algorithm primary consists of three segments; the identification of a desirable object and the determination of its form parameters, calculation of the new discrete actuator positions to center the object in the image frame and the movement and control of the VCAs to these new locations. This section will discuss these steps, as well as provide detailed information on the inner workings of the algorithm.

The process begins by placing the actuators at their mid-points, positioning the image sensor at a centralized location. Prior to recognizing an object, the algorithm enters "scan" mode by exciting both linear motors to a number of positions (Table 7.9) to cover as much visual space as possible, while attempting to identify an object. This essentially relates to the "corners" of the visible range of the image sensor.

As detailed, the VCAs are not permitted to reach their maximum range (i.e., 7,500 and 52,500 reliably in regards to the 2DOF POM) since any object located beyond these positions, in either the x or y direction, is incapable of being targeted. In addition, the tighter values promote a tinier bounding box allowing for faster scanning. The algorithm continues to search for objects until one is recognized with an area (M_{00}) greater than 500 pixels, as anything below has been identified as noise.

Upon locating an object and defining its boundary, the moment information obtained from the crack code procedure is placed into the memory of the shared memory controller within FC-Micro architecture. Subsequently, the C code designed for the microcontroller uses this data to determine the area of the object and most notably, the x and y pixel locations of its centroid (6.4). Since there is division and multiplication present in the equation, it is preferable to perform the calculations within the microcontroller code, as it is well suited for this task.

During each iteration of the targeting loop, the current VCA positions are read by the microcontroller from the shared memory and stored as $D1_{old}$ and $D2_{old}$ in the C code. At this time, the algorithm formulates the new linear motor locations relating to the centering of the object utilizing the model equations defined by the DOE results. However, since these are comprised of numerous variables which are squared, cubed, etc., it is considerably more efficient to perform these calculations once and simply input the results into the model. Therefore, before formulating the new positions, $D1$ and $D2$, each variable containing a power (i.e., X^2, X^3, etc.) is defined beforehand with the model equation rearranged to conform to the changes.

While the VCA positions can be determined and updated during each iteration through the loop, it is undesirable to move extremely small distances. Therefore, to prevent jittery motion, the discrete locations are only updated if equation 7.2 holds true,

$$D1_{new}, D2_{new} = \begin{cases} D1_{old}, D2_{old}, & 482 <= x <= 542 \; AND \; 354 <= y <= 414 \\ D1, D2, & otherwise \end{cases} \tag{7.2}$$

where $D1_{new}$ and $D2_{new}$ are the updated actuator positions, $D1_{old}$ and $D2_{old}$ are the current actuator positions, $D1$ and $D2$ are the newly calculated locations and x and y

are the center points of the object. This simple check ensures that while the object is located within 30 pixels of the center of the coordinate frame in either the x or y direction, the actuators will remain stationary. Additionally, they are constrained by upper and lower bounds (i.e., 7,500 and 52,500 ADC counts) to ensure they do not venture outside of their optimal, functioning range. Upon correctly configuring the new positions, they are communicated to the FPGA by way of the memory controller and are used to relocate the VCAs via the cascade PID-PID controller, essentially targeting the desired object.

Though the model equations contain a substantial number of variables, through experimentation it was determined that it requires only 3 ms to complete the computation of both complex equations. As the camera's frame rate is restricted to 38 frames per second, the large equations do not pose a bottleneck on the system. Finally, the targeting algorithm was set to execute every 70 ms, as greater rates resulted in undesirable effects (i.e., overshoot and circling of the object), primarily due to the contour tracking architecture being unable to define the moment information quickly.

7.5 Automated Targeting of an Object in Motion

Upon the verification of the 2DOF-5 and 2DOF-50, the automated targeting capabilities of the architectures were left to be validated. Note, the size of the available testing space only permitted the testing of 2DOF-5. Therefore, the discussion and results in this section pertain to the aforementioned model only. To garner a finer understanding of the capacity of the entire system, a pendulum was chosen as the object to be targeted as it follows a defined path at a repeatable frequency. However, since the ultimate goal was to track an IR light, employing a standard pendulum comprised of a ball-shaped weight attached to a string was not applicable, due to its freedom to

Figure 7.7: Pendulums laser cut from acrylic with integrated IR LEDs and added magnets for weight.

rotate. Thus, a rigid pendulum was constructed to ensure only planar motions are achieved. The design was laser cut from acrylic containing holes which allowed for the simple fastening of LEDs and for connecting to a frame. Two pendulums measuring 15 cm and 30 cm from the pivot point to center of the suspended mass (Fig. 7.7) were fabricated to grant variation in an array of experiments.

The the equation pertaining to the period of a pendulum is defined as:

$$T = 2\pi\sqrt{\frac{L}{g}} \tag{7.3}$$

where L is the distance between the pivot point and center of mass of the suspended weight and g is the acceleration due to gravity. To ensure the equation remains true, the mass of its suspended section must be significantly greater then the mass of the segment connecting it to its pivot point. Therefore, heavy magnets were added to

Table 7.10: Parameters relating to both pendulums

Parameters	Pendulum Lengths	
	15 cm	30 cm
Rod Mass (g)	5.65	12.05
Suspended Mass (g)	6.92	6.90
Suspended Mass with Magnets (g)	105.60	112.95
Period (s)	0.7766	1.0982

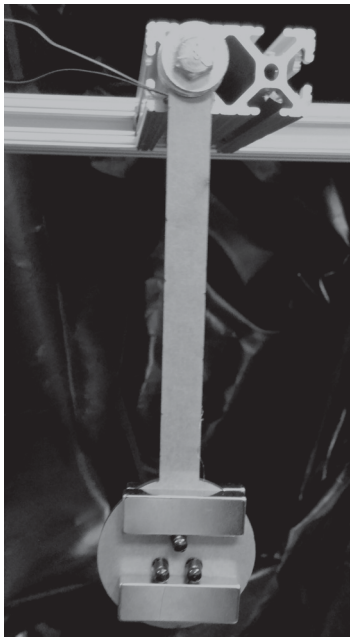


Figure 7.8: Experimental setup containing pendulum.

hanging portion to guarantee equation 7.3 remains valid, with each pendulums mass and approximate frequency characteristics displayed in Table 7.10. To promote a reliable experimentation arrangement, each pendulum was attached to a simple frame designed from 80/20 aluminum, shown in Fig. 7.8.

With the pendulum in place, to achieve robust experimentation it was mandatory to devise a motion platform with the following abilities: it must be capable of randomized movement, the variations in position must be recorded in some manner and the platform must be able to sustain the weight of the 2DOF POM. Unfortunately, a mechanism with these characteristics was unavailable for use, thus a more simplistic

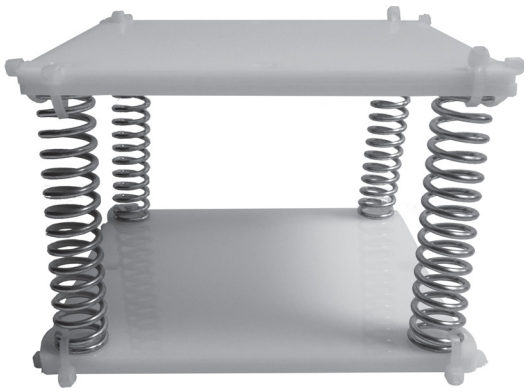


Figure 7.9: Simplistic motion platform fabricated via acrylic and stiff springs.

motion platform was developed and is shown in Fig. 7.9.

The top and bottom sections are comprised of laser cut acrylic and are connected by stiff springs (i.e., spring constant of 492 Nm) to ensure the weight of the POM does not cause extreme reactions when excited. To gather information on the displacement relating to the platform, an accelerometer was attached to the center of the bottom side of the top section. This ensured the accelerations pertaining to the x, y and z directions were gathered within the architecture of microcontroller, whose capabilities permit the storing of data on a personal computer. Finally, the 2DOF POM was firmly secured to the top platform with its center aligning with the center of the accelerometer, to ensure accelerations were accurately recorded. The motion platform with accelerometer and POM attached can be viewed in Fig. 7.10.

To obtain a varied set of data, a series of five separate tests were completed: the first two consisted of keeping the POM stationary while providing motion to the 15 cm and 30 cm pendulums, the third provided a variety of displacements to the motion platform with the POM attached while targeting a non-mobile object, while the final two entailed exciting the two pendulums while simultaneously imparting motion to the POM on the movable platform.

Using the frequencies calculated by equation 7.3 as comparison, the object's x and

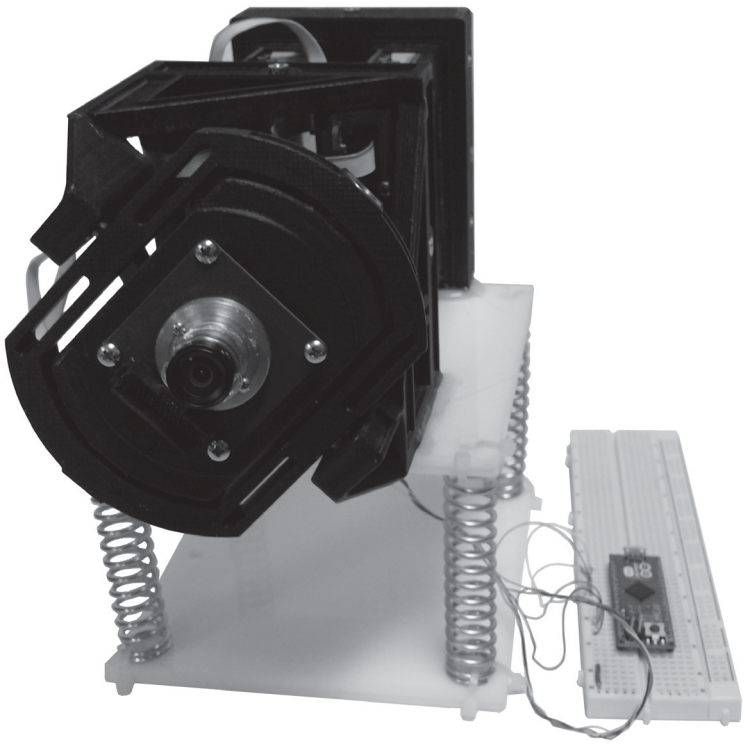
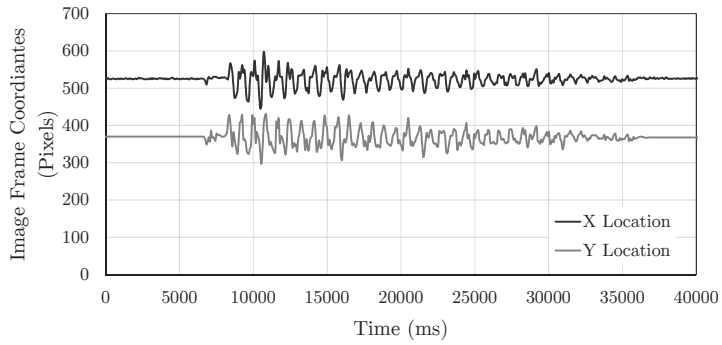


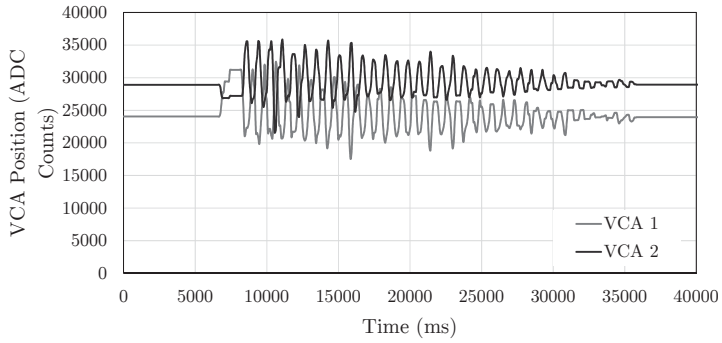
Figure 7.10: Experimental motion platform with 2DOF POM and accelerometer integrated for data acquisition.

y centroid positions as well as the motions of each VCA were recorded and plotted for each experiment. To diversify the data set further and ensure randomization in the data is accounted for, multiple displacement techniques were instigated. This resulted in 10 different motions being applied to the system for the first two trials. Four were impacts to each of its four sides, the next two consisted of rotating the platform in clockwise and counterclockwise positions and then releasing the platform, while the final two involved pulling the platform to the front and back and releasing it. In each case the platform was allowed to stabilize before continuing. Fig. 7.11 and 7.12 highlight the motions obtained from the first two trials; fixing the position of the 2DOF POM and providing motion to the 15 cm and 30 cm pendulums, respectively.

Both the centroid determined by the contour tracking algorithm and the positions



(a) Centroid locations during the 15 cm pendulum displacement.

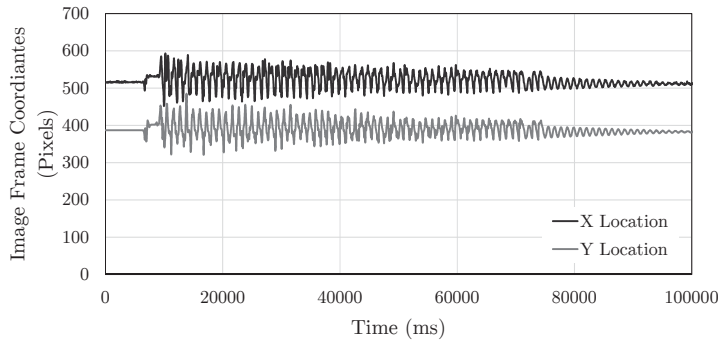


(b) Discrete VCA locations during the targeting of the 15 cm pendulum.

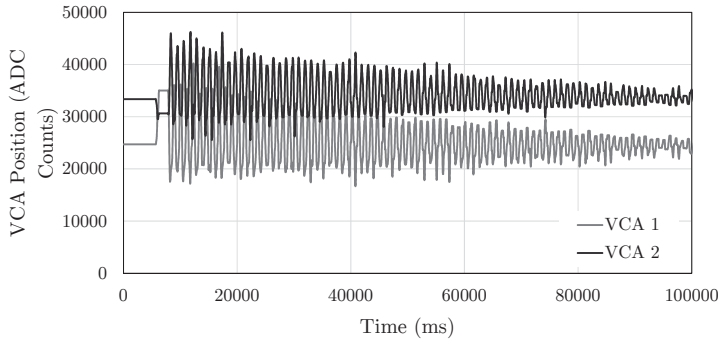
Figure 7.11: Centroid and discrete VCA locations during the targeting of the 15 cm pendulum undergoing displacement.

of both VCAs follow a sinusoidal pattern; mimicking the oscillations of the pendulum. This data is indicative of the POMs capacity to track the motion of the pendulum. Furthermore, upon analyzing the recorded data, the centroid's average location and range (i.e., minimum and maximum values obtained during tracking with respect to the center of the image frame), in addition to each VCA's range and the period of actuator one were calculated and are shown in Table 7.11. Note, actuator two's period was very similar and was not included to prevent tedium.

As determined, the frequencies of each characteristic at specific times throughout the pendulums translation closely match the value determined by equation 7.3. Note, equation 7.3 becomes increasingly accurate when the maximum angle that the



(a) X and Y centroid locations of the pendulum during experimentation.



(b) VCA locations while targeting the 30 cm pendulum.

Figure 7.12: Centroid and VCA displacements recorded while targeting a 30 cm pendulum in motion.

Table 7.11: Targeting the moving pendulums with POM fixed

Parameters	Pendulum Lengths	
	15 cm	30 cm
X centroid starting location (pixels)	525	515
Y centroid starting location (pixels)	370	387
X centroid range (pixels)	446-598	452-592
Y centroid range (pixels)	297-430	322-479
X centroid average (pixels)	523	522
Y centroid average (pixels)	367	387
Actuator one range (ADC counts)	17,553-32,406	16,671-40,131
Actuator two range (ADC counts)	21,595-35,829	25,516-46,207
Period at ≈25% of motion (s)	0.791	1.16
Period at ≈75% of motion (s)	0.766	1.11

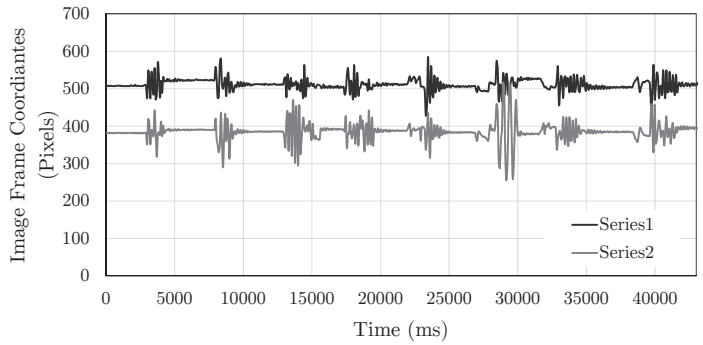
pendulum displaces from vertical (i.e., the amplitude) becomes smaller, as defined the frequency equation of a pendulum. Thus, nearing the end of the its motion (i.e.,

≈75%), the centroid and VCA frequencies more accurately represent the number calculated in 7.3. Furthermore, the centroid's range remained close to the center of the image, with the average nearly matching the starting positions, highlighting the functionality of the targeting algorithm. Finally, the 30 cm trials resulted in greater ranges being present in the VCA locations due to the larger motion of the pendulum. However, the centroid locations were quite comparable to the 15 cm tests, showcasing its targeting capabilities. Note, while the x centroid range is smaller than the y, this was due to a larger displacement of the pendulum in the vertical axis, than the horizontal.

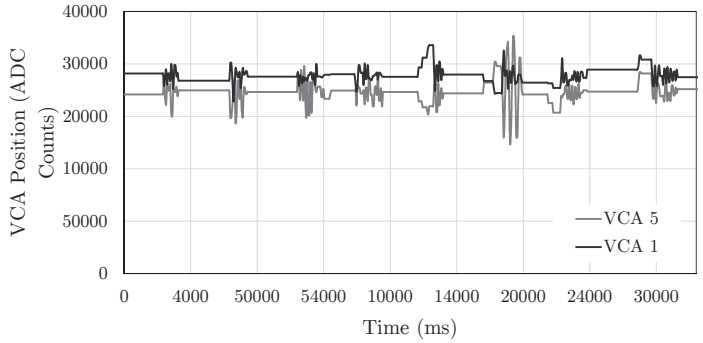
Upon completing the preliminary experiments, the next trial consisted of disturbing the POM while maintaining a lock on a fixed target (i.e., the stationary pendulum). Fig. 7.13 displays the centroid locations and VCAs movements, along with the acceleration information pertaining to the motion of the POM.

Once more, the VCA and centroid locations mirror the displacement of the POM as the targeting system tracks the motionless object, even in the presence of accelerations beyond 1 g. The evaluated outcomes of the test are favorable, as indicated by Table 7.12. In this scenario, the more violent nature of the trials resulted in a larger discrepancy in the minimum and maximum values of the centroid, in addition to larger displacements of the VCAs. However, the average pixel values still remain close to the starting positions, proving the targeting system's capability to correct for intense, quick motions.

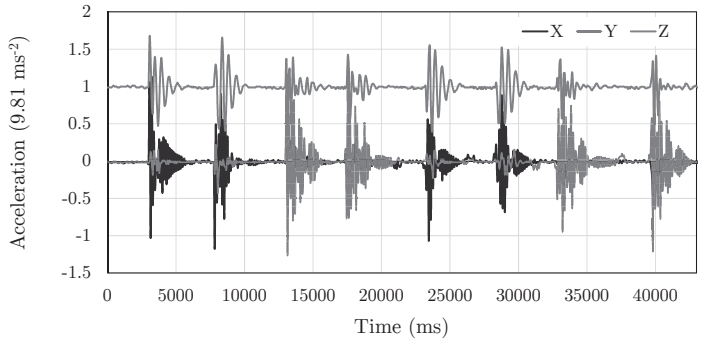
Following the promising results, the final two tests were executed as previously discussed, with the results displayed in Fig. 7.14 and 7.15 for the 15 cm and 30 cm pendulums, respectively. As indicated by the figures and the results in Table 7.13, these experiments pushed the ATM to its limits as not only was it following the translation of the pendulums, but also attempting to adjust for self-motion. As the



(a) X and Y centroid locations of the target while the POM is disturbed.



(b) Actuator values while maintaining a lock on the fixed target.



(c) Accelerations gathered during displacement of the POM.

Figure 7.13: Centroid and actuator positions in addition to the accelerations obtained during the targeting of a fixed object while the 2DOF POM underwent displacement.

figures indicate, the centroid and VCA locations resemble that of the acceleration data and more notably, the pendulum oscillations. However, there is a much larger degree of discrepancy in the x and y location of the center points of the object than in

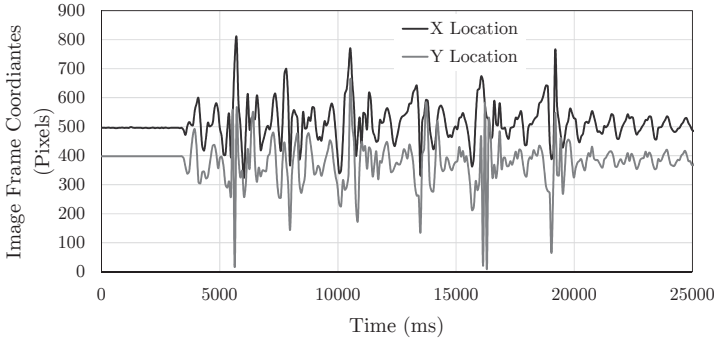
Table 7.12: Targeting a stationary object while the POM experiences disturbances

Parameter	Results
X centroid starting location (pixels)	507
Y centroid starting location (pixels)	382
X centroid range (pixels)	428-584
Y centroid range (pixels)	256-510
X centroid average (pixels)	511
Y centroid average (pixels)	385
Actuator one range (ADC counts)	24,826-45,286
Actuator two range (ADC counts)	32,817-43,580

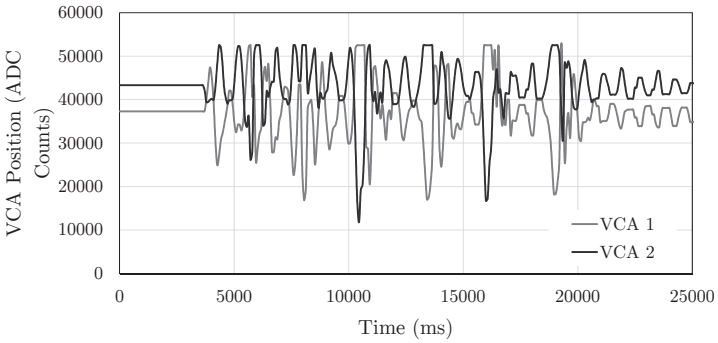
Table 7.13: Targeting the moving pendulums while the 2DOF POM is displaced

Parameters	Pendulum Lengths	
	15 cm	30 cm
X centroid starting location (pixels)	496	512
Y centroid starting location (pixels)	398	393
X centroid range (pixels)	314-796	299-828
Y centroid range (pixels)	25-678	22-741
X centroid average (pixels)	515	519
Y centroid average (pixels)	372	374
Actuator one range (ADC counts)	16,876-52,500	12,307-52,500
Actuator two range (ADC counts)	11,814-52,500	10,606-52,500
Period at ≈25% of motion (s)	0.813	1.11
Period at ≈75% of motion (s)	0.767	1.14

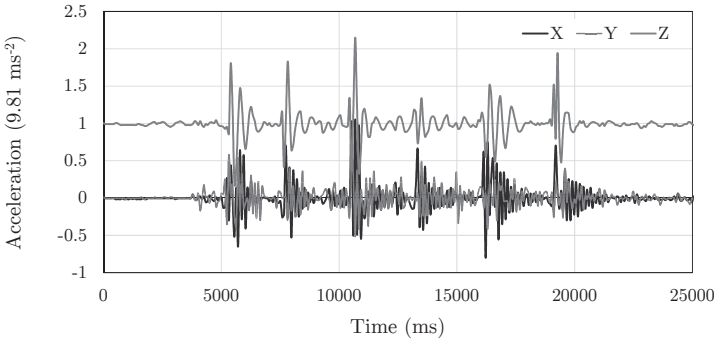
previous tests, which is relative to the combination of the acceleration and pendulum motions. In addition, the camera's update rate poses a strict bottleneck on the system as the object, with disturbances included, moves much faster than camera's ability to determine the centroid of the entity. However, despite the large errors in the center points and the camera's frame rate, they are corrected within 100 ms of the displacement. Nonetheless, the results show that the system can indeed follow the target despite the forceful rotations, albeit delayed slightly. Furthermore, these two trials were an extreme example of a real world application. It is unlikely an object would move so rapidly in a camera's FOV while large disturbances are ongoing in the ATM.



(a) Locations of centroid of the mobile, 15 cm pendulum while the POM was disturbed.



(b) Locations of each VCA during the targeting of the moving pendulum while being displaced.

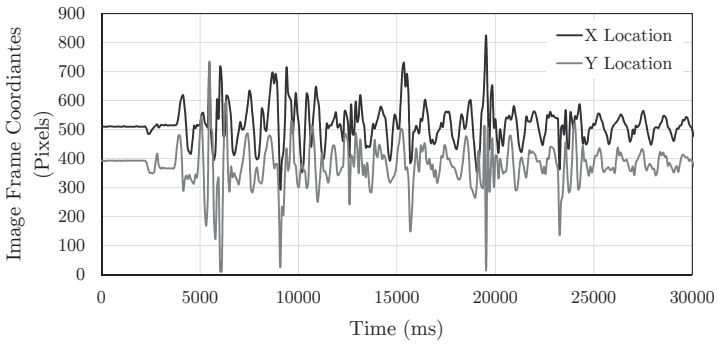


(c) Accelerations experienced by the 2DOF POM.

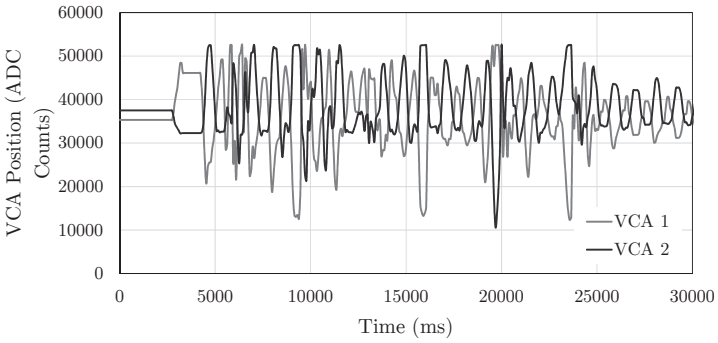
Figure 7.14: Central locations of the object in the image frame, discrete VCA values and accelerations during the experimentation of targeting a 15 cm pendulum in motion while the ATM is disturbed.

7.6 Conclusions

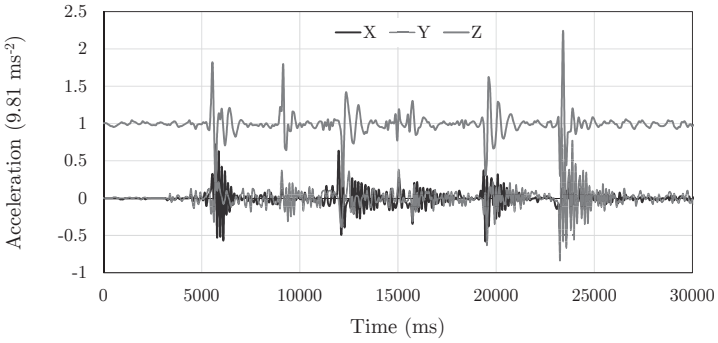
The targeting of an object undergoing rapid maneuvers is non-trivial in nature due to the inter-connectivity and reliance on a variety of systems. However, building upon



(a) X and Y centroid locations of the 30 cm pendulum in motion while the POM is disturbed.



(b) Discrete values of each VCA under motion while targeting the 30 cm pendulum



(c) Disturbances experienced by the POM recorded in ms^{-2}.

Figure 7.15: Centroid and VCA locations, together with the logged accelerations experienced by the 2DOF POM while targeting the 30 cm pendulum.

the existing architecture presented in the earlier chapters of this thesis, the 2DOF POM and FC-micro PCB were combined to form a mechanism capable of reliable targeting. By implementing DOE methodology, a system of non-linear equations were

generated which position an IR light spot in the center of an image frame by assigning discrete positions to each actuator in a POM configuration. As these equations are too resource intensive and complex to easily calculate in VHDL, the object parameters were communicated to the microcontroller for processing. To justify the model equations and validate its targeting potential, a series of tests were performed by recording the adjusted center point location with respect to the center of the image frame. Correspondingly, to identify its dynamic qualities, the system was forced to follow a moving object while it experienced disturbances. The result is a reliable ATM, capable of maintaining a fix on a target in motion while undergoing self-displacement.

Chapter 8

Design and Verification of a Free Space Optical Communication System

Due to the rise in security concerns and the dependence on high speed data transmission, FSOC has become more prominent in many military applications. The protocol is applicable for both long and short range communication. However, as line-of-sight is mandatory it suffers from signal loss due to the misalignment of the transmitter and receiver. Thus, a mechanism capable of automatically discovering a transmission signal and aligning a sensor to receive the light is extremely beneficial to FSOC. Transmission and receiving circuits were constructed from simple electronic components, with algorithms composed in a hardware based environment utilizing the embedded design of the F-Micro board. To increase transmission distance, the photodiode contained within the receiver design was situated behind a narrow FOV lens. In addition, using beam splitter technology, the lens was modified to include a cube beam splitting device which enabled transmission of light to the image sensor while a portion was reflected towards the receiving device. Employing the FSOC system with the system developed in the previous chapter resulted in a mechanism capable of targeting and communicating with a single light source.

8.1 Introduction

The concept of free space optical communication is not necessarily new, with origins relating back to the late 1800s [161]. However, as semiconductor laser technology became a reality in the 1970s and 1980s, FSOC was employed for a varitey of high powered (i.e., 1-200 W), long range (i.e., 50-1,000 km) applications [12, 161]. Though, in more recent years, shorter range (i.e., 100-500 m) moderately powered (i.e., 10-100 mW) systems have been developed [12]. Fundamentally, FSOC is a technology utilizing light propagation through the atmosphere, or "free-space," to obtain wireless, fast, data transmission for short and long range communication purposes. In contrast to wired systems, such as optical fiber cabling, "free-space" refers to information transference through air, underwater, outer space or any region absent of physical obstruction. The technology promotes a varied set of air-to-air and air-to-ground applications which are currently dominated by systems composed of RF and Wi-Fi technology. However, FSOC offers advantages over RF such as a higher bandwidth, typically 10 Mbits per second to 100 GBits per second [11], has a large available spectrum compared to a more crowed RF one [162] and FSOC is not easily intercepted or jammed [11]. The advanateges over Wi-Fi include a much longer range, up to 10 km as a opposed to hundreds of meters [163] but most prominately mirror RF as Wi-Fi is easily intercepted and is prone to jamming problems [164]. This is especially concerning when associated with military and highly covert applications, in addition to communication with unmanned aerial systems (UASs) and autonomous underwater vehicles (AUVs).

As mentiond an FSOC link is naturally license-free and is capable of providing a high bandwidth, low power, and secure communication protocol for various autonomous systems and ground nodes, including both mobile and fixed stations [11, 102]. However,

unlike RF and Wi-Fi, optical communication is highly sensitive to misalignment and platform instability which result in unavoidable communication interruptions leading to loss of data transmission [10]. Nonetheless, developing a receiver which is capable of maintaining a continual up-link with a transmitter, results in a greatly reduced bit error rate, increasing both functionality and dependability of the FSOC architecture.

A proposed solution to remedy these issues stems from a mechanism with the ability to maintain a precise lock with the transmitting section of the FSOC system; an especially complex task when employing both air-to-air or air-to-ground applications due to maneuverability of aerial vehicles. Furthermore, this complexity becomes increasingly prominent when the ground station is not fixed, as the motions of two unconnected systems must be compensated for. However, by utilizing the exceptional abilities of the ATM described in Chapter 7, a mechanism capable of correcting tiny and large fluctuations in displacement is attainable.

In FSOC systems, the rate at which the light source shifts states from "on" to "off" is crucial, as it primary factor the in overall speed of the data transmission. There are many methods which can be implemented to instantiate a pulse, such as the use of a microcontroller or a timing circuit, but to achieve extreme rates, a combination of an FPGA in addition to high speed transistors is a more viable option. Controlling the position of a transistor via the output pin of an FPGA, results in ability to turn a light source "on" and "off" exceptionally fast. Additionally, the configuration consumes little power, as the source will be "on" and conducting a significant amount of current for a short period of time while pulsing, reducing the overall power usage of the system.

To adhere to the system on a chip methodology and SWaP requirements, the FSOC algorithms were developed in VHDL and unified into the existing architecture. Separate transmitter and receiver circuitry were designed for integration with the FPGAs I/O pins. In addition they were constructed to be as miniature and compact

as possible. The FSOC system takes advantage of beam splitter technology, allowing for targeting and communication to occur via a single IR light source. This improves reliability, greatly fulfills SWaP requirements and results in a compact, highly responsive mechanism with a multitude of applications. Finally, the joining of the FSOC technology with the ATM formed the realization of a mechanism with optical communication and automated targeting characteristics.

8.2 Circuit Designs for the FSOC System

When considering FSOC, the primary component in its architecture is the circuity which provides the high speed data transmission. There are many systems capable of sending and accepting light over exceeding long distances (i.e., tens of kilometers) and at significantly fast rates (i.e., gigabits per second) [165]. However, to meet these specifications, the systems are considerably bulky, cumbersome and quite heavy (i.e., weighing kilograms). Furthermore, they require a high-powered voltage source as they employ laser devices for the generation of light. As payload is a concern for the majority of autonomous systems, attaching FSOC transmitters capable of extremely long range and high data rates is not feasible. Therefore, a miniaturized, lightweight approach was chosen via the utilization of light emitting diodes for use in the transmitter and a photodiode as the receiver. This ensures the payload limitations of an autonomous vehicle are not violated while providing a realistic scope for the outcomes of the thesis. Thus, a maximum data rate of 500 kbits per second (i.e 500 kHz) and a transmittal range of 30 feet ($\approx$ 914 cm) were selected in the pursuit of the FSOC system to be integrated with the ATM. While these values are low, they are still considerable for short range communication between autonomous vehicles, in addition to autonomous vehicles to ground stations due to the miniature, low-powered

characteristics of the design.

There are two distinct elements to consider in the realization of a functional FSOC architecture; the transmitter and the receiver. As suggested by their designation, they have the responsibility of transmitting coded light sequences and receiving and distinguishing pulses, respectively. Therefore, a two-staged approach was taken while developing the circuitry behind the FSOC system, beginning with the receiver.

8.2.1 FSOC Receiver Circuit Implementation

The receiver circuit is composed of four sections; light detection, voltage amplification, comparison and restriction. Each segment is critical in correctly distinguishing the presence, or lack thereof, of the pulsed light being communicated. Though a variety of components are capable of light detection, a device which is extremely sensitive and responsive to the fluctuation in light patterns is mandatory to achieve the conditions set forth by the system. Therefore, a photodiode was selected due to its compact form factor, ease of integration and most notably, its high transition rates.

A photodiode is a simple semiconductor which absorbs photons and converts these into a small amount of current, even in the absence of light. As many FSOC systems operate in the IR light spectrum ([10,166]), one which excites in this band was chosen; specifically, the SFH-206-K [167] was selected due its bandwidth of 400-1100 nm and its extreme responsiveness, 20 ns. Integrating a resistor in series with this diode, generates a voltage relating to the presence of light.

Since the F-Micro PCB was designed with 3.3 V LVTTL, a minimum of 1.7 V must be introduced to the input pin to generate a “high” signal, with a “low” realized at 0.8 V and below (Chapter 5). While operating within the confines of this configuration, it is undesirable for input voltages to exist within 0.8 V - 1.7 V. Thus, to

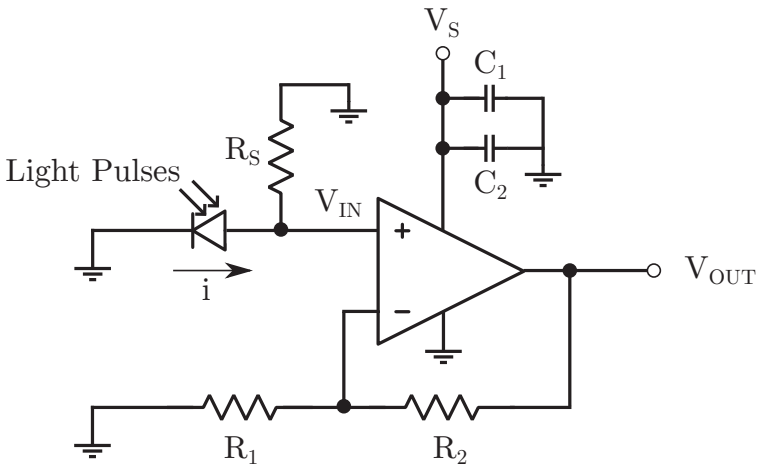


Figure 8.1: Non-Inverting op-amp configuration for amplification of the voltage corresponding to the received light.

conform to the conditions, 2 V was selected as the minimum value which corresponds to the identification of light by the photodiode. To ensure this functionality was present, the voltage across the series resistor was drastically increased via a non-inverting operational amplifier. This circuit, along with the photodiode in reverse bias orientation is seen in Fig. 8.1, with equation 8.1 pertaining to the output of the op-amp.

$$V_{OUT} = V_{IN}(1 + \frac{R_2}{R_1}) \tag{8.1}$$

When light is present, the photodiode generates a tiny current which in turn is converted to a voltage across R_S. This voltage is amplified according to the R_1 and R_2 values, with a maximum obtainable voltage limited by the supply voltage V_S.

To achieve fast data rates, the AD8066 [168] was chosen as a suitable op-amp for its high slew rate of 180 Vμs^{-1}. Furthermore, it contains two distinct op-amps in one chip, requires a single supply voltage source and is manufactured in through hole and surface mount packaging, ideal for prototype configurations.

Dictated by the characteristics of the photodiode, current is generated in low-light

conditions; even when blocked by an appropriate IR filter. Therefore, it is imperative that the voltage representation of the current is not depicted as a "high" signal after amplification. Though, the circuit still must be sensitive enough to detect light from a distance of 30 feet. Therefore, a number of resistor values were selected and tested to determine the optimal value to be placed in series with the photodiode to achieve the specifications. Additionally, each resistor composing the non-inverting op-amp must be appropriately chosen to eliminate noise and low-light current generation from being identified as a "high" voltage.

Upon experimentation, it was concluded that $R_S = 2.2k\Omega$, and R_1 and R_2 equaling 100 Ω and 33 kΩ, respectively, results in the optimal light detection up to a range of 30 feet. Note, $V_S = 10V$ while the capacitors were used for filtering with values of $C_1 = 1\ \mu$F and $C_2 = 0.1\ \mu$F. Furthermore, due to the characteristics of the electronics for the receiver and transmitter (discussed in the following section) circuits, it was determined that light pulses of 1 MHz could be achieved. This is twice the rate of the initially chosen 500 kHz. Nonetheless, the amplified voltage pertaining to the non-inverting op-amp for a single light pulse was obtained via an oscilloscope and is displayed in Fig.8.2.

With the signal amplification achieved, it was necessary to ensure variations in light intensity would not result in negative effects or be the cause of a higher BER. Therefore, a non-inverting comparator circuit utilizing a Schmitt trigger configuration (Fig. 8.3) was used via the second op-amp on the AD8066 chip, with equation 8.2 referring the arrangement's output.

$$V_{OUT} = \begin{cases} 0, & V_{IN} < 2V \\ V_{IN}, & V_{IN} >= 2V \end{cases} \tag{8.2}$$

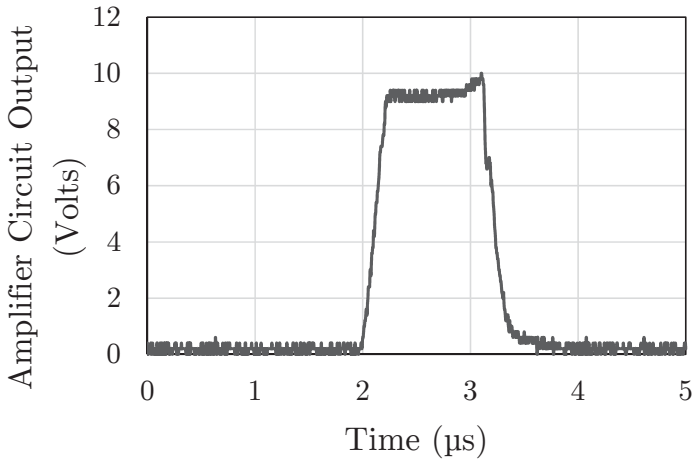


Figure 8.2: Amplified voltage relating to a single light pulse received at 1 MHz.

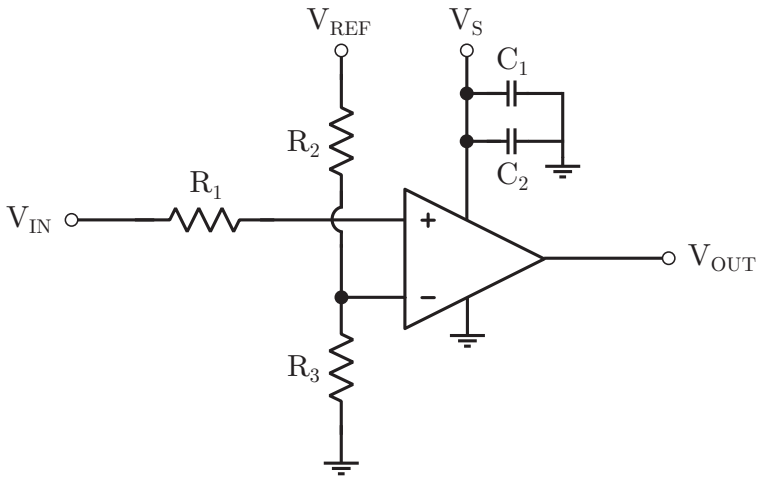


Figure 8.3: Comparator circuit ensuring the correct voltages are delivered to the FPGA.

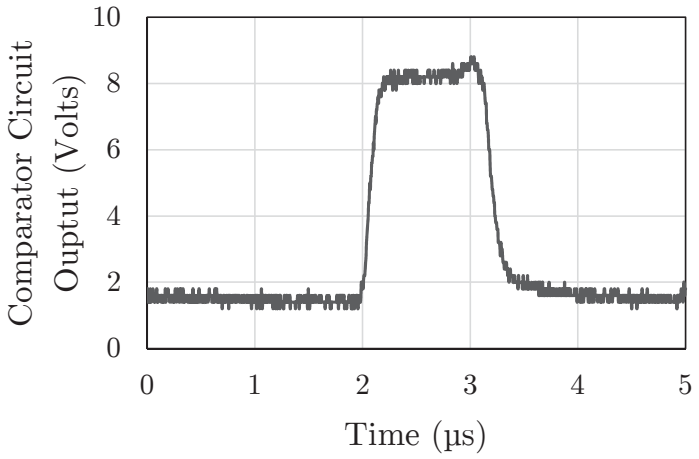


Figure 8.4: Comparator circuit output for a single light pulse.

The output of the circuit is defined by the voltage entering the negative lead of the op-amp. If the value supplied to the positive terminal is greater than the negative, V_{OUT} equates to this value, otherwise it is zero, essentially generating a square wave. For this setup, the filtering capacitors used are $C_1 = 1\ \mu$F and $C_2 = 0.1\ \mu$F, while the supply voltage $V_S = 10V$, $R_1 = 100\Omega$ and $V_{REF} = 5V$ which is generated by a 5 V regulator. This voltage is divided appropriately between $R_2 = 150\Omega$ and $R_3 = 100\Omega$ to present 2 V to the negative pin. The amplified light is placed in the positive side, and if greater than 2 V, it is passed through the circuit, otherwise a zero voltage is produced. This not only eliminates noise, but avoids over-saturation of the signal when there is an abundance of light present (i.e., the light is very intense or close to the sensor). Fig. 8.4 showcases the waveform generated for a single light pulse.

Finally, the last segment of the receiver circuit is added in to prevent damage to the FPGA. Since these devices are sensitive to overloading voltages, it is critical to limit the input voltage to the specifications of the defined LVTTL standard; in this case, 3.6 V. Therefore, a simple solution to this problem is to place a Zener diode, rated at 3.3 V, between the input line on the FPGA and ground to ensure the voltage

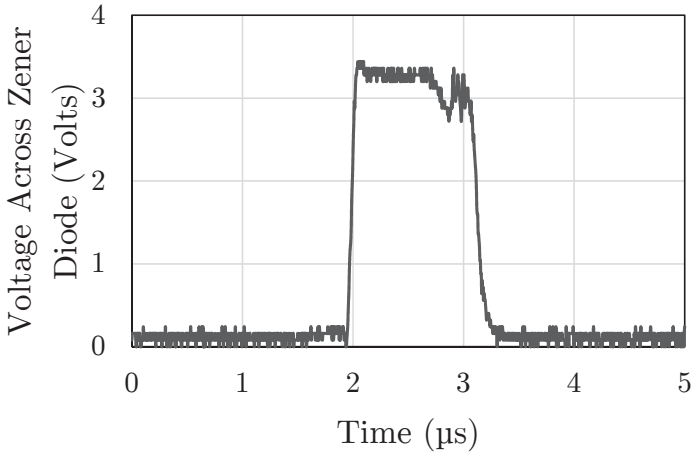


Figure 8.5: Voltage across the Zener diode which is experienced by the FPGA input pin.

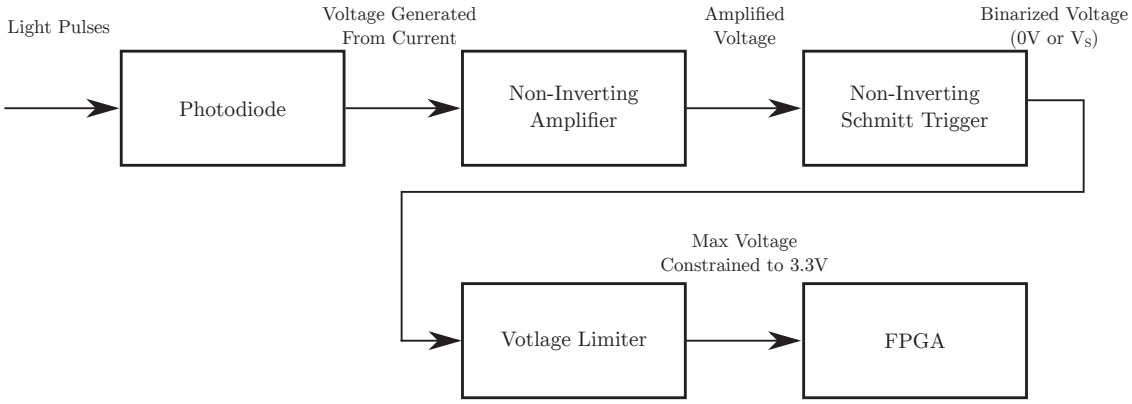
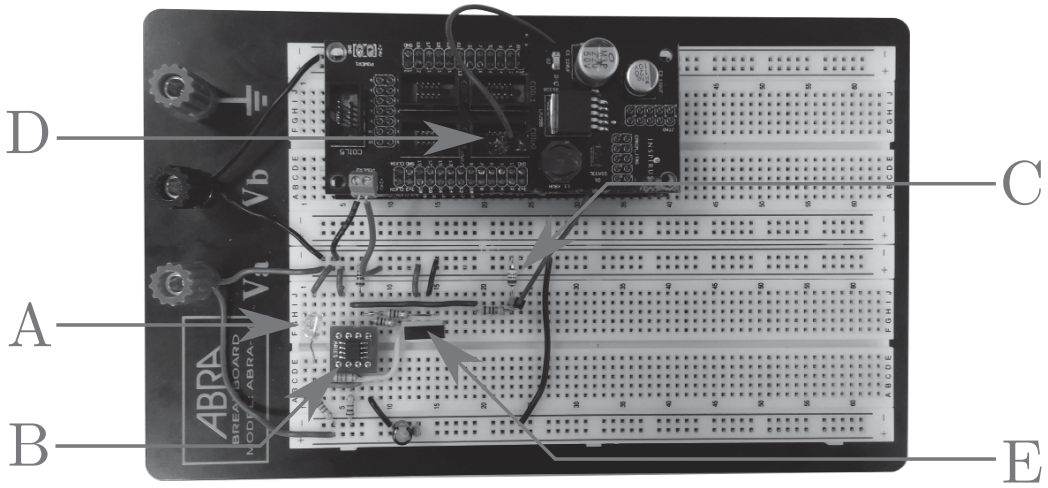


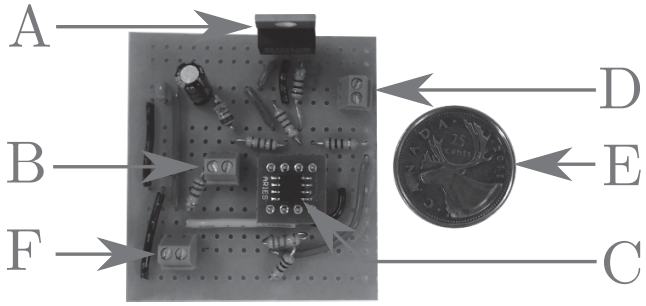
Figure 8.6: Flow of the FSOC receiver architecture.

output from the comparator will remain at 3.3 V as long as the Zener is functioning correctly (Fig. 8.5). With this in place, the flow of the receiver circuit is shown in the block diagram seen in Fig. 8.6. Furthermore, the prototype and final representation of the circuit's physical realization are displayed in Fig. 8.7a and 8.7b, respectively.

As shown, the resultant circuit is very tiny and compact, requires a single ended, 5 V source, ground connection and an output line which interfaces to the FPGA. For ease of connectivity, termination blocks were added to the board, but in a finalized revision, this would not be required.



(a) Prototype receiver circuit configuration. A: Data input on the FPGA. B: Photodiode. C: Op-amp. D: Zener diode. E: Voltage regulator.



(b) Receiver design soldered to a protoboard. A: Voltage regulator. B: Photodiode connection. C: Power and ground input lines. D: FPGA input for receiving data. E: Canadian quarter for size reference. F: Op-amp

Figure 8.7: FSOC receiver circuit realization.

Unfortunately, due to time constrains a surface mount PCB was not able to be manufactured. However, a circuit model was constructed in the EagleCAD software to showcase the compactness of the circuit when implemented with surface mount technology. The entire circuit is constrained to a mere 0.8 x 0.95 inches shown in Fig. 8.8. Finally, all experimental testing and results of this design are discussed in section 8.4.

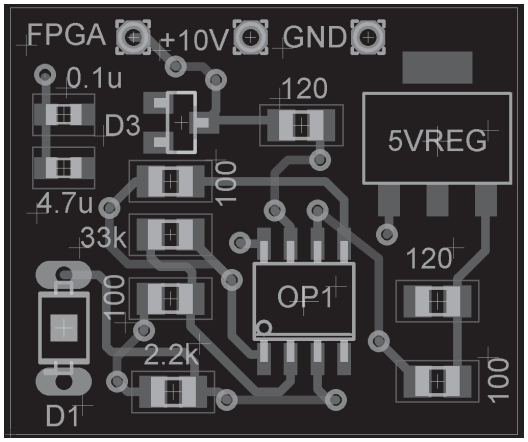


Figure 8.8: Surface mount rendition of the FSOC receiver circuit designed in EagleCAD

8.2.2 Design of a Transmitter Circuit for the FSOC System

Designing a reliable transmitting circuit is critical to the development of FSOC as it is the primary factor in defining the speed and distance requirements identified from the outset. While many transmission circuits employ laser devices to generate light pulses, these are bulky, require high power and are generally very expensive. An alternative to such a configuration, is the light emitting diode (LED), which is tiny, operates on low power and is very inexpensive. While a vast selection of diodes exist, FSOC technology demands a device with specific capabilities. In particular, it must exhibit high surge current characteristics, produce large radiant intensities and have extreme switching qualities. Furthermore, it must generate light within the same wavelength specified by the photodiode. The surge current conducted by the diode without failure is much greater than its forward current, generating intense beams when pulsed rapidly, resulting in a farther transmission distances. Generally, diodes capable of producing higher radiant intensities are very focused, resulting in a narrow beam; whereas ones emitting lower intensities tend to have larger half angles, reducing alignment issues. Therefore, a number of LEDs were explored in order to determine

Table 8.1: Selected LED diode specifications

Parameter	SFH-4550 [169]	SFH-4556 [170]
Radiant Intensity (mW/sr)	1,100	145
Surge Current (A)	1	1
Spectral Wavelength (nm)	860	860
Half Angle (deg)	±3	±20
Rise and Fall Time (ns)	12	12

Note: the radiant intensity is in regards to a pulse width of 20 ms at 100 mA.

the optimal light source for the FSOC system. From the plethora of options, two were selected, with an overview of the relevant specifications described in Table 8.1. As shown, the fundamental difference between each device are their radiant intensities and half angles.

Utilizing a LED to generate a light pulse requires a circuit which can excite and stop the current flowing through the diode rapidly and on command. This effect was accomplished by employing the service of an FPGA's I/O pins. Within the VHDL design, setting a pin to '1' results in a "high," or 3.3 V output on the corresponding line, while '0' relates to "low," or a 0 V response. Configuring electrical components dependent on this notion is a relatively simple task, however, FSOC cannot be achieved by this alone. Since the FPGA is only capable of producing current in the milliamp scale, additional circuitry must be exploited to permit large currents to flow through the diode. Therefore, a metaloxidesemiconductor field-effect transistor (MOSFET) was integrated into the design due to its high-rate switching capabilities and capacity to operate during surge current conditions. In particular, the PSMN022-30PL, n-channel MOSFET [171] was chosen for this application due to its high transition speeds, compatibility with logic level voltage and maximum current rating. With the inclusion of extra electronics, the transmitter circuit was realized with a schematic of its design displayed in Fig. 8.9.

The supply voltage V_S, and power resistor R_{POW}, incorporated for its high power

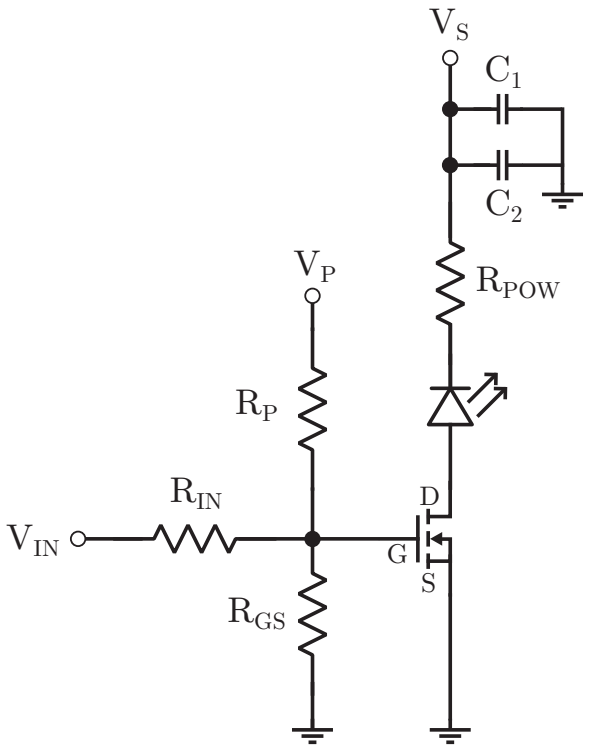
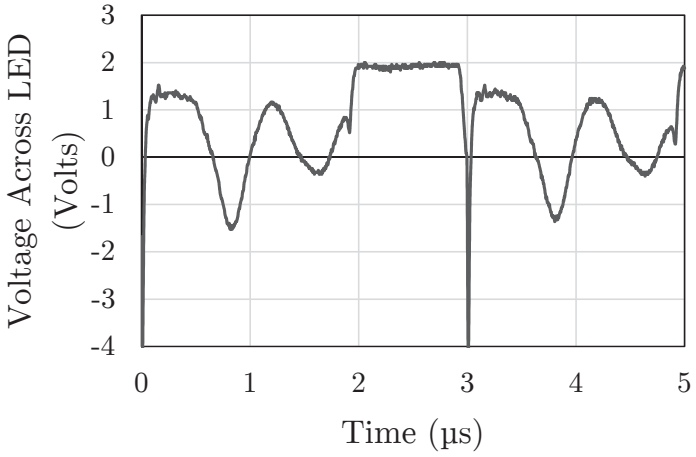


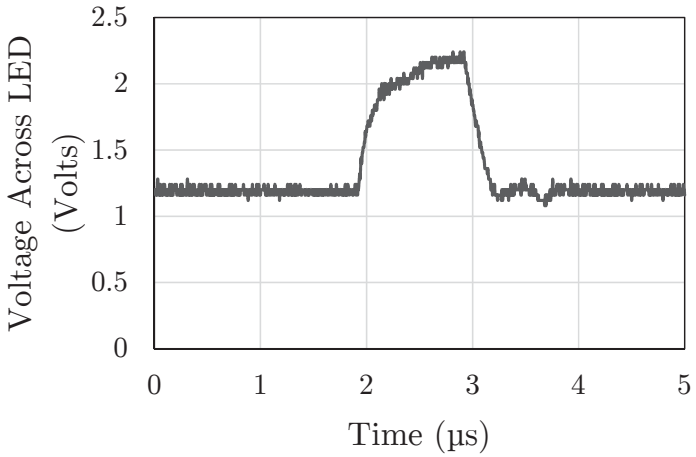
Figure 8.9: Transmitter circuitry utilizing MOSFET technology.

rating, are the controlling elements of the current experienced by the diode when the MOSFET is active. The values of these parameters are discussed in section 8.4. The capacitors are the same as the previous circuits, $C_1 = 1$ μF and $C_2 = 0.1$ μF, while V_{IN} is the voltage representation of the data bits from the FPGA output pin, 0 V for a '0' and 3.3 V for a '1'. The voltage $V_P = 3.3V$ is supplied by the F-Micro PCB and the resistors R_{IN}, R_P, R_{GS} are connected to the gate of the MOSFET to ensure the voltage (current) delivered by the FPGA pin is optimal. In particular, R_P and R_{GS} force the gate to be at consistent voltage at all times, preventing noise, oscillations and coupling.

Upon experimentation it was determined that $R_{IN} = 560\Omega$, $R_P = 330\Omega$, $R_{GS} = 560\Omega$ resulted in the correct switching of the LED. Fig. 8.10 showcases the effect these resistors have on the voltage across the LED during switching. As indicated,



(a) Voltage measured across the LED without resistors connected to the gate of the MOSFET.



(b) Voltage experienced by the LED when appropriate resistors are attached to the MOSFET gate.

Figure 8.10: Effect of resistors connected to the MOSFET gate on the switching capabilities of the LED.

without including either of the resistors the diode experiences significant ringing causing undesirable effects. However, with the addition of ideal resistors, the LED switches off and on rapidly while being void of oscillations.

The flow of the transmitter circuit is shown in Fig. 8.11, while the preliminary and final representation of the circuit's physical realization is shown in Fig. 8.12a and 8.12b, respectively. Mirroring the receiver design, this circuit is both compact and

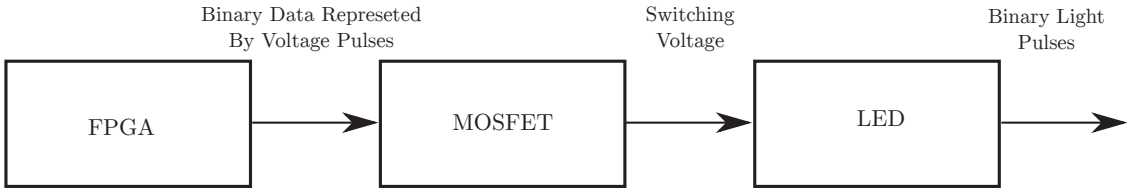
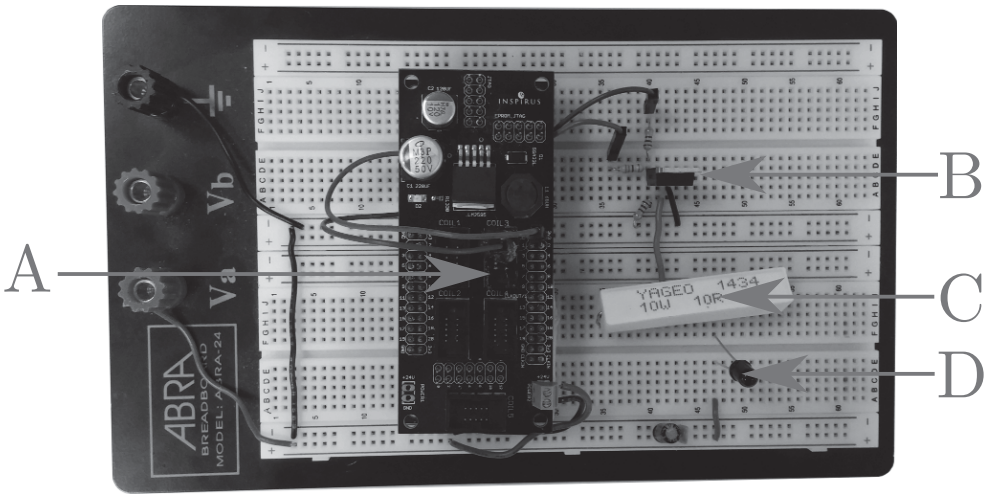
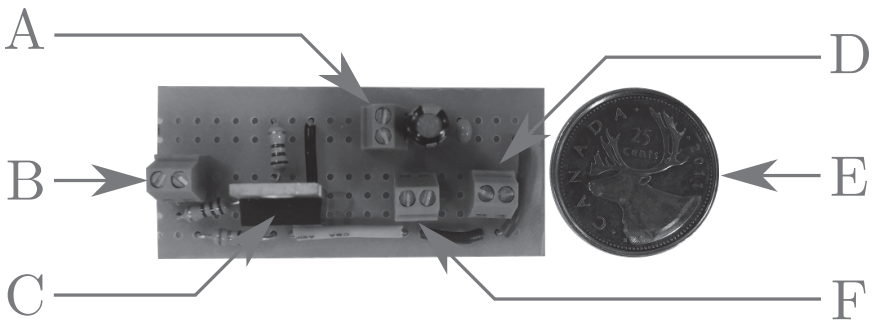


Figure 8.11: Transmitter circuit topology.



(a) Initial design of the transmitter circuit. A: FPGA output pin. B: MOSFET circuitry. C: Power resistor. D: LED for transmitting light pulses.



(b) Final design of the FSOC transmitter circuitry soldered to a protoboard. A: Power input. B: FPGA connection. C: MOSFET. D: Connection for LED. E: Canadian quarter for scale. F: Terminal block for attaching power resistor.

Figure 8.12: Transmitter circuit designs of the FSOC system.

miniature and requires connections for power, ground and the output from the FPGA. Headers were included in the design to allow the quick removal of power sources and LEDs so testing could be accomplished more readily.

Similarly to the receiver circuit, due to time limitations a PCB was unable to

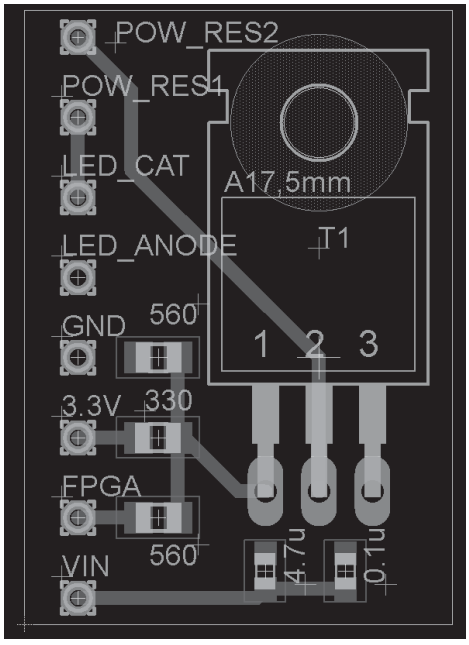


Figure 8.13: EagleCAD surface mount representation of the transmitter circuitry.

be manufactured. Nonetheless, the transmitter circuit was designed in EagleCAD (Fig. 8.13) to provide a visual means of the circuit's surface mount realization resulting in a tiny PCB measuring 1.15 x 0.8 inches. The design achieves the SWaP requirements specified, with analysis and experimentation of the transmitter circuit discussed in section 8.4.

8.3 HDL Algorithm Development

The formation of a robust communication protocol is essential to ensure efficient delivery of data while being indiscernible, to prevent interception. Unfortunately, this is especially problematic as dictated by the design of FSOC, the transmitter and receiver operate on isolated platforms and have no means of connectivity. However, a communication link between these two system can be realized by dissolving the transmittable data into segments and adding known values to the beginning and end

of the buffer to guarantee a means of interpretation upon receiving the packet.

Utilizing the parallelism of an FPGA to construct the FSOC protocol has many benefits, including high switching rates, low power requirements and a small form factor. However, implementing VHDL algorithms is a time consuming process caused by extensive build times and the strictness of the architecture. Nonetheless, to meet SWaP conditions, VHDL code was pursued as an avenue to transmit and receive data serially at rates of 1 Mbits per second.

8.3.1 Transmitter Protocol In HDL

Developing a transmission protocol is very complex when attempting to overcome the issues experienced by FSOC, such as atmospheric turbulence [9, 10, 105]. However, to construct a proof-of-concept system, these issues were not taken into consideration. Thus, a more simplistic approach was taken based upon the universal asynchronous receiver/transmitter (UART) protocol to ensure the goals of the thesis were achieved.

The transmitter algorithm was constructed with two specific functions: packetize a collection of values to form an efficient data buffer and transmit the data in serial fashion based upon a specified frequency, via an I/O pin on the FPGA. While this is easily accomplished, it is of utmost importance to correctly define the structure of the packet to generate reliable transmission. Nonetheless, the architecture was designed to obtain three, 16-bit numbers and concatenate them in big-endian style (i.e., placing the first byte (or bit) in the most significant position of the register). Note, the total transmittable bits during one transmission phase was selected for testing purposes and can easily be expanded. Nevertheless, upon combining the binary data into a single register, a start byte and stop byte were positioned at the beginning and end of the data. The hexadecimal values of these bytes were chosen to be CD ("11001101"

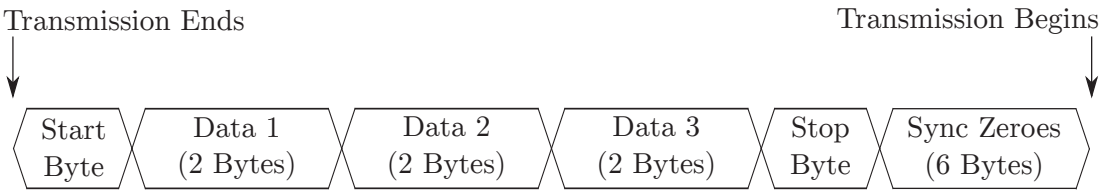


Figure 8.14: Packetized data to be transmitted.

in binary) and A9 ("10101001" in binary), respectively. While techniques such as data byte stuffing are more optimal, this process is a simplistic method to allow the receiver a means of identifying the data component of the buffer, enabling basic error checking and synchronization functionality.

To complete the protocol, 48 bits containing a value of '0' were padded to the end of the packet. This addition was primarily implemented to grant the receiver a means of conveniently synchronizing the transmitted information. Furthermore, it permits the LED to remain in a "off" state for a period of time, ensuring heat resulting from power dissipation does not damage the system. In particular, if the data bits equal '1' for a long time interval, the diode will remain active indefinitely, potential harming the circuitry. Finally, beginning with the lowest bit, the packet is transmitted serially at a rate of 1 Mbits per sec. A representation of the realized packet is shown in Fig. 8.14.

The packet size during transmission is 112 bits, with only 48 containing relevant information, resulting in an overhead of 64 bits or approximately 57% of the bit stream. This is rather high in comparison with traditional communication formats such as RS-232. Nonetheless, upon arrangement of the packet, each bit is sent to the output pin of the FPGA at a rate of 1 Mbits per second. Here, ones and zeroes in the bit stream correspond to high voltage levels (i.e 3.3 V) and low voltages levels (i.e., 0 V), respectively. By connecting the line to the MOSFET gate connection (Fig. 8.9), the FET activates (opens) when the FPGA transmits a '1' and deactivates (closes) at the outputting of a '0', pulsing the diode based on the data in the packet. An example

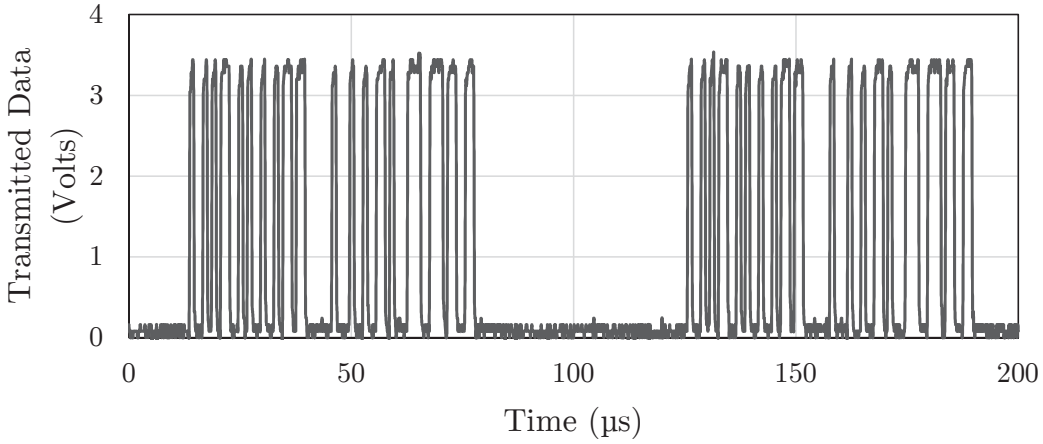


Figure 8.15: Voltage representation of the packet being transmitted.

of data being transmitted by the algorithm is shown in Fig. 8.15. Here, two sets of identical data have been sent, with the padded zeroes identified at the middle portion of the signal. Upon defining the transmitter design and data protocol, the receiver algorithm can now be identified.

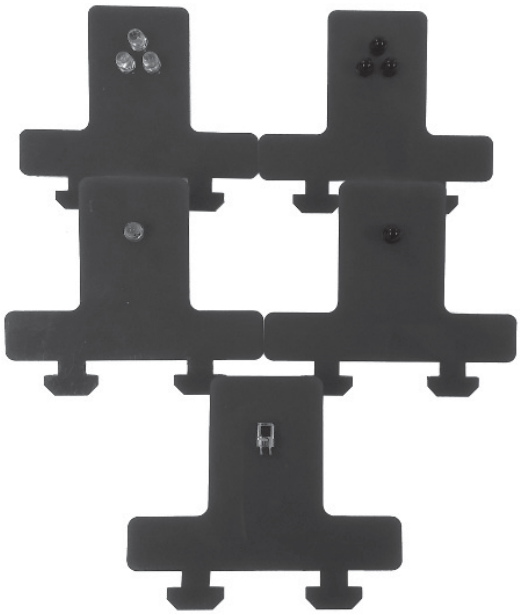
8.3.2 Hardware-Based Receiving Algorithm

With the transmission protocol realized, a receiver algorithm which can successfully filter and synchronize the serial data stream, decode the data and perform error checking is needed. Synchronization of the transmitter and receiver algorithms is mandatory but exceptionally difficult as they exist in isolation. However, checking the incoming data at a frequency 10 times faster (i.e., 10 Mbits per second) than the rate of the transmission, permits the receiver to identify the initial transition of a bit from low to high at extreme speeds. Upon locating a switch, the receiver begins gathering data after waiting an additional five clock signals at the higher frequency. This ensures it obtains the value of each bit in the data stream during the middle of its transmission.

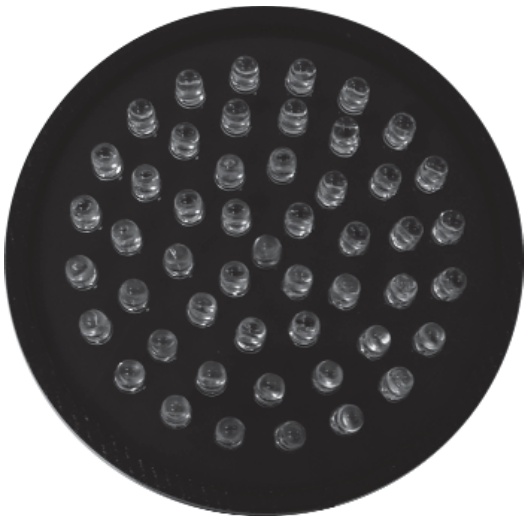
As the data streams in, each identified bit is planted into a register beginning with the lowest and ending with the highest, mirroring the transmitter protocol. The algorithm continues to record all information until 64 bits, or the length of the data stream, noninclusive of the padded zeros is obtained. With the recognized packet stored into a register, the top and bottom bytes are compared to the start and stop bytes defined in the transmission algorithm. If all bits in these locations match the start and stop bytes, the bits are considered valid data and are outputted to external modules in the VHDL architecture. For testing purposes, each of the 16 bit numbers were placed into the shared memory, giving the microcontroller access to the information.

8.4 FSOC System Verification

To prove that the circuitry and algorithms were capable of communication, trials were undertaken with little space existing between the transmitter and receiver (i.e., a maximum range of 200 cm). Additionally, they were utilized as a validation tool to garner the optimal LED arrangement for the transmitter. Note, for ease of testing, the series resistor, R_S, was reduced from $2.2k\Omega$ to 100 Ω during this experimental phase to guarantee light intensities at close range would not result in large voltages. To ensure alignment of the light pulse with the sensor within photodiode, holders were cut from acrylic permitting simple, but accurate fastening of the devices. Mounting "legs" were included in their design to promote connectivity to 80/20 aluminum bars to be employed as an alignment instrument for the transmitter and receiver. Furthermore, as distance is a key performance metric in a FSOC system, an array of 10 parallel branches of five LEDs in series was constructed as a means to generate extreme light intensity to boost range and increase synchronization. Fig. 8.16 gives visual reference



(a) Photodiode and various LED configurations utilized for experimentation as follows: three SFH-4550 (top left), three SFH-4556 (top right), one SFH-4550 (middle left), one SFH-4556 (middle right), photodiode (bottom)

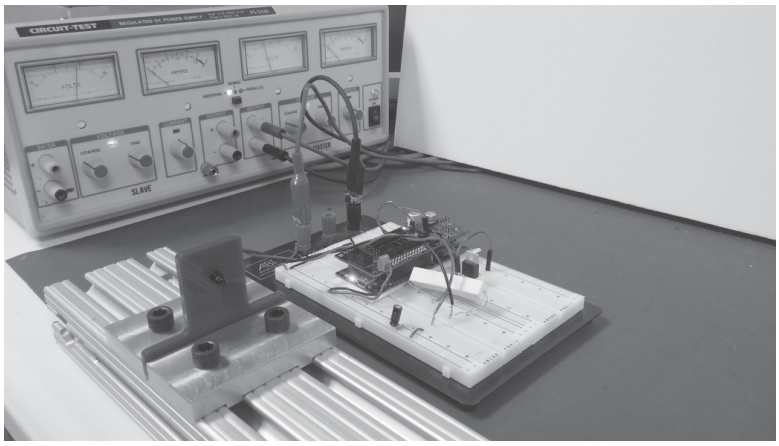


(b) LED array designed for optimal performance of the FSOC system.

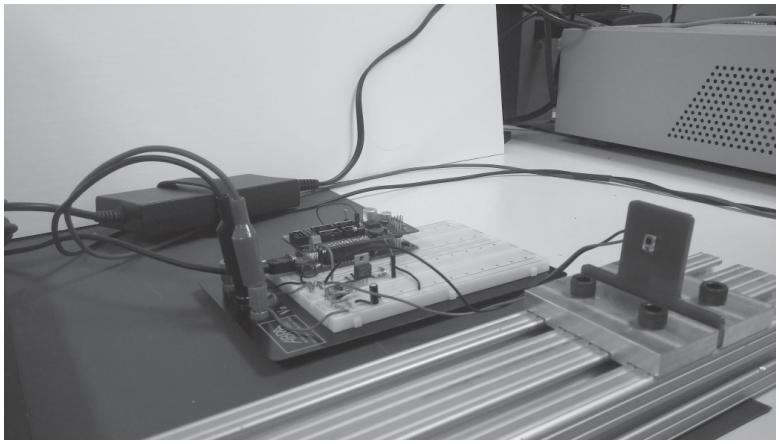
Figure 8.16: Photodiode and LED configurations fabricated for experimental purposes.

to the holders and array, while Fig.8.17 showcases an example of the experimental framework.

To perform the experimentation, three known, 16-bit values were packetized in



(a) Transmitter circuit during testing.



(b) Experimental setup of the receiver circuit.

Figure 8.17: FSOC validation experimental configuration.

accordance to the protocol and communicated at a frequency of 1 MHz. The photodiode remained stationary, while the LED(s) under consideration was displaced along a single eight foot length of 80/20 aluminum. The distance between the transmitter and receiver was broadened until the identified data was lost (i.e., all zeroes received) or erroneous. The trial results pertaining to the various LED configurations at different current values are shown in Table 8.2. Note, V_S and R_{POW} refer to the values in Fig. 8.9.

For all scenarios, a larger current (i.e., high voltage at lower resistance) equates

Table 8.2: Short range FSOC validation

Diode Combinations	V_S (V)	R_{POW} (Ω)	Range (cm)
SFH-4556	10.004	10	18
SFH-4556	10.001	5	18.7
SFH-4550	9.998	10	54.5
SFH-4550	9.996	5	57.6
3 SFH-4556	15.001	10	33.6
3 SFH-4556	14.999	5	35.4
3 SFH-4550	15.001	10	77.4
3 SFH-4550	15.003	5	81.3
LED Array	15.004	10	117.4
LED Array	14.997	5	121.2
LED Array	19.999	5	152.4

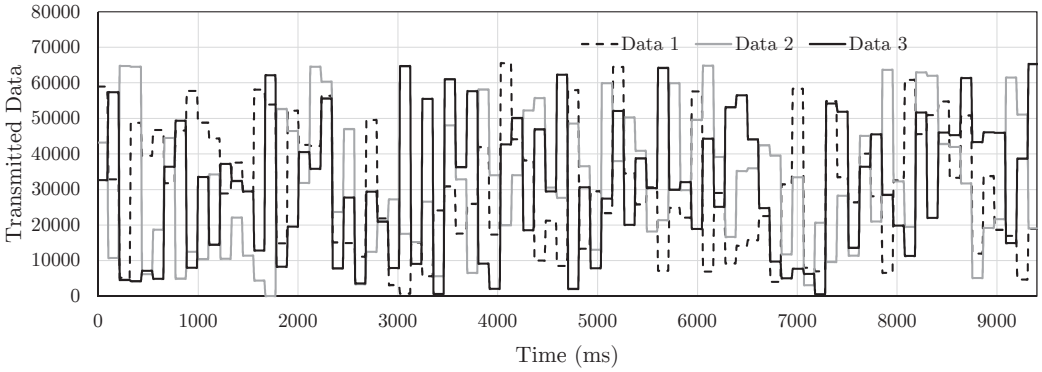
to greater distance as light intensity is dependent on the current flowing through the LED(s). Additionally, the diodes with higher radiant intensities (i.e., SFH-4550) are far superior in comparison to the variation promoting better half angles. Furthermore, increasing the diode count results in increased performance. Though the SFH-4550 performed exceptionally well, its narrow beam caused alignment issues even with the inclusion of the experimental setup. Nonetheless, using this LED in the array formation promoted both exceptional range and ease of synchronization as theorized.

Upon validating the functionality of the algorithms and electronics, R_S in Fig. 8.1 was changed back to $2.2k\Omega$ for long distance verification, with testing repeated in similar fashion. However, since the transmission gap would be far greater, multiple 80/20 bars were arranged to ensure the photodiode and LEDs remained aligned over the expanse. The results from these trials are highlighted in Table 8.3. As expected, the range obtained for all configurations has increased significantly with the array outperforming all designs once more.

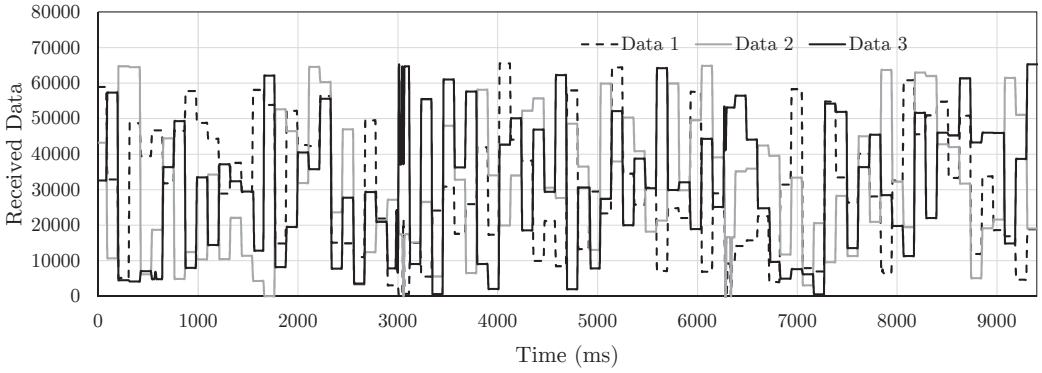
To evaluate the performance of the FSOC system, a parameter to consider is the bit error rate, or the number of bits in error divided by the total number of transmitted bits over a specified time interval. To determine this metric, a series of three randomly

Table 8.3: Experimental results of the long range testing of the FSOC system

Diode Combinations	V_S (V)	R_{POW} (Ω)	Range (cm)
SFH-4556	10.002	10	147.0
SFH-4556	10.002	5	187.5
SFH-4550	9.997	10	449.2
SFH-4550	9.996	5	457.5
3 SFH-4556	15.010	10	268.2
3 SFH-4556	15.011	5	279.4
3 SFH-4550	15.004	10	644.8
3 SFH-4550	15.005	5	670.3
LED Array	14.998	10	731.1
LED Array	14.992	5	801.6
LED Array	20.008	5	874.7



(a) Transmitter data for experimentation.



(b) Data received for a short period of time.

Figure 8.18: Random numbers being transmitted and received by the FSOC architecture.

generated 16-bit values were packetized in the defined arrangement and transmitted at a distance of 20 feet utilizing the array configuration.

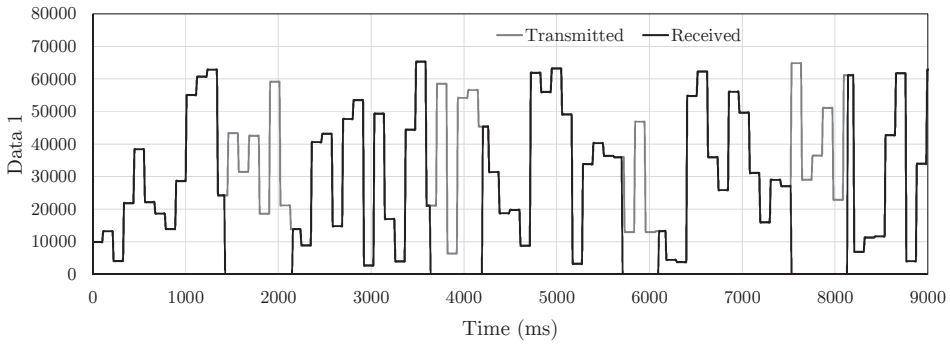


Figure 8.19: Random number transmission with interruptions in the signal propagation.

Each sequence of bits were communicated 10 times, with a delay of 10 milliseconds between each transmission to allow for the slower logging rate of the microcontroller. To formulate the BER, the values were recorded before transmission and compared with the bits identified by the receiver. While the testing resulted in a BER of nearly zero, the worst case scenario for a short time interval was selected to showcase its bits in error. Fig. 8.18 highlights the transmitted and received data of the trial during this short time interval.

As shown, the data received is nearly identical to that transmitted with the largest discrepancies visible at approximately 3,000 ms and 6,300 ms. Analyzing the data revealed only 113 bits were in error (i.e., received differently than transmitted) out of 40,727 data bits being sent, resulting in a low BER of 0.2806.

The ability to resynchronize the bit stream after the occurrence of an interruption is vital to an optical communication system. Thus, for final validation, a set of three, 16-bit numbers were once again randomly determined and broadcasted. However, for the trial, the light pulses were obstructed, severing the line-of-sight link between transmitter and receiver. Upon waiting for a short period of time, the light was permitted to reach the photodiode once more, restoring communication. The results of the test were visualized in Fig. 8.19.

As displayed, at intervals 1,450, 3,650, 5,700 and 7,500 the receiver identifies zero for all three 16-bit numbers in accordance to the light being blocked. However, data immediately returns to the correct transmission values upon restoration of the link, validating the system's capacity to quickly synchronize upon loss of communication.

8.5 Targeting and Communicating Via a Single Light Source

Achieving communication and automated targeting via a single light source holds significant merit with respect to a variety of optomechatronic applications. While fastening a photodiode near the aperture of the lens is a potential method to produce these results, it presents a number of limitations. To begin, the image sensor and diode will not be correctly aligned, thus the photodiode will not sense what is targeted at all times. Secondly, the light will be focused on the sensor and not the diode, resulting in light pulses being received at a reduced intensity. Finally, packaging the system becomes problematic as any misalignment while attaching the diode will cause negative effects. Taking these issues into consideration, a device permitting the focus of a single beam on both sensors was identified as an optimal approach.

8.5.1 Beam Splitter Container Design

To ensure targeting remains robust, the light entering the image sensor must remain focused and centered upon striking its surface. Correspondingly, the light received by the photodiode is expected to be extremely intense to achieve maximum performance from the FSOC system. However, positioning both sensors behind a single lens is ineffective as it focuses the light in a straight, narrow beam.

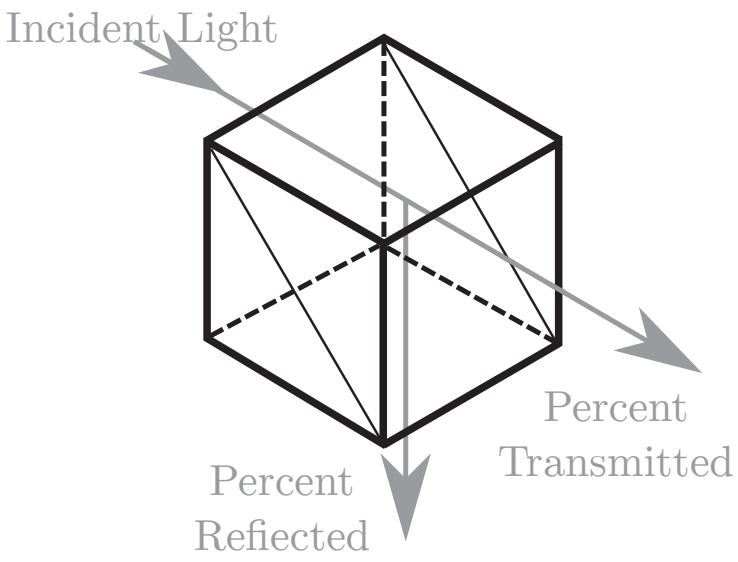


Figure 8.20: Operation of a beam splitter.

The immediate solution is to segment the light beam into two separate streams, with one hitting the image sensor while the other being absorbed by the photodiode. Dividing light in such a manner is relatively simple task when utilizing the functionality of a beam splitter device. When a beam enters the device, a portion will transmit through it while the other is reflected on an angle defined by its construction. A visual description of light entering and exiting a beam splitter is shown in Fig. 8.20.

Beam splitters are manufactured in a wide variety of shapes and sizes (e.g. plate, cube, circular, smooth, polka-dot, etc.) with each having its own advantages. However, the cube-shaped design [172] was selected as the appropriate device to be integrated in the desired mechanism for many reasons. It is capable of light filtering in the infrared and near-infrared spectrum, its shape permits simple incorporation into a system with little alignment concerns, it is able to reflect light at 45° angle and it is available in a small form factor (i.e., 12.5 mm x 12.5 mm).

Positioning the splitter behind a lens and placing a sensor below and on its side allows for each device to collect light from the same source. As maximum distance

Figure 8.21: 50 mm lens segmented into its optics and threaded sections.

achieved is a key metric in the performance of FSOC, a narrow FOV, 50 mm lens was chosen as the ideal optics for its "zoomed" perspective. Note, this lens was utilized for the modeling of the targeting system in Chapter 7. However, incorporating the beam splitter in close proximity to the exit of the lens is problematic as its size forced the image sensor beyond focusing bounds. Therefore, an unrequired section of the lens was removed, segmenting it into two sections to allow optimal integration of the splitter (Fig. 8.21).

Combining the sensors, beam splitting cube and the lens into a compact package is necessary to ensure payload is not a concern when actuating the component with a POM. However, upon investigating a selection of containers, none were identified which would permit the arrangement of these devices into a suitable design. To ensure the photodiode receives maximum light, the gap between the lens' point of entry and surface of the image sensor resulting in near-perfect focusing is required, as this value equates to the optimal concentration of light onto the diode. The distance was measured to be 34 mm and using this as a guide, a holder including the segmented lens, image sensor, photodiode and beam splitter was modeled with a prototype generated from PC-ABS. Its physical realization is shown in Fig. 8.22.

To promote the theory that supplying focused light to the diode is the optimal approach, a holder device with the photodiode in very close proximity to the cube

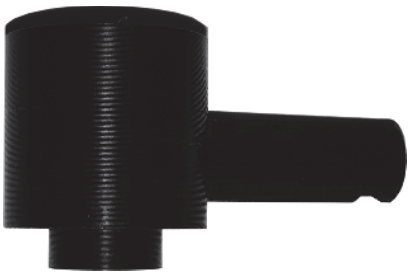


Figure 8.22: Beam splitter holder fabricated from PC-ABS.

Figure 8.23: Beam splitter holders with integrated sensors and lens. The left rendition is the offset model, while the right corresponds to the photodiode being placed next to the cube.

was produced. The light received for this configuration will not be focused, but will also not be prone to potential alignment issues. The fully constructed holders are displayed in Fig. 8.23.

8.5.2 Beam Splitter Experimentation in Conjunction with the FSOC System

Building upon the experimental results detailed in section 8.4, trials to determine the FSOC system's maximum achievable range with both beam splitter container designs were conducted. As the results of the previous tests highlighted the large variation in performance with different LED configurations, only five were selected for the experiments. The distance obtained for each holder is shown in Table 8.4.

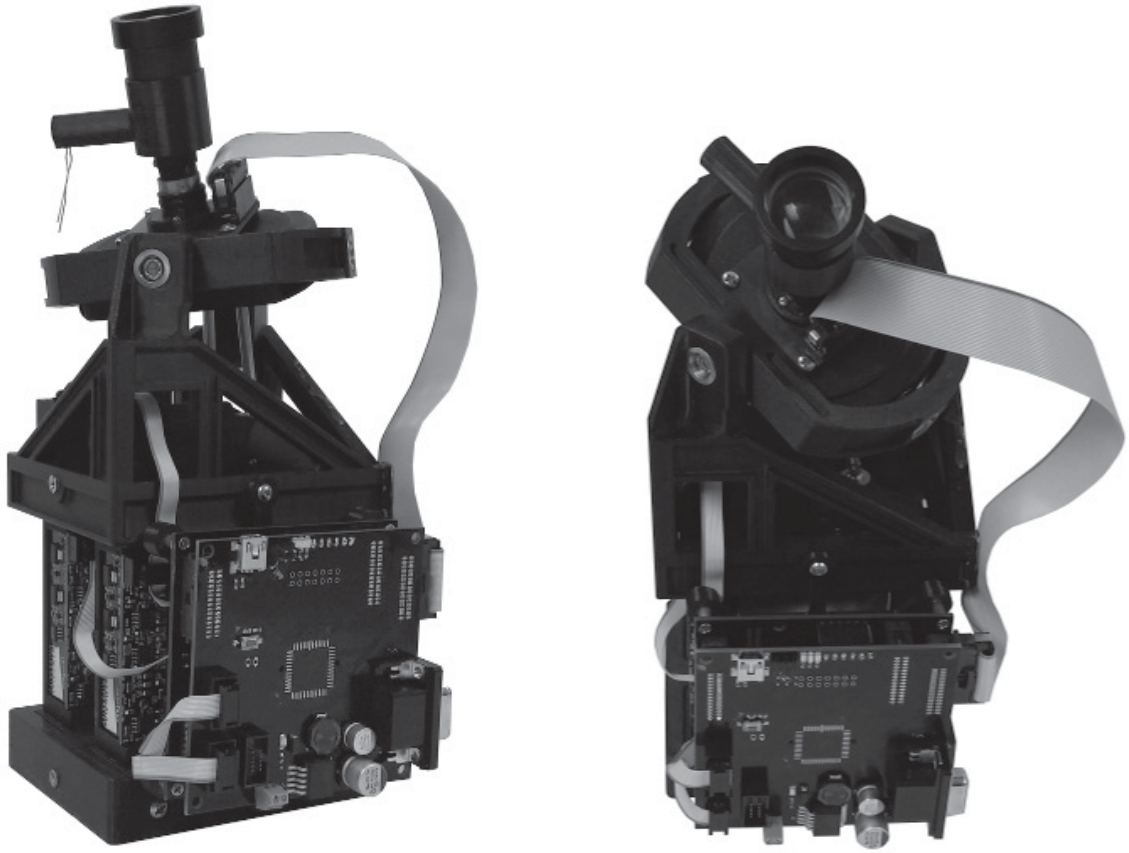
Table 8.4: Distance achieved by both holder designs during the experimental validation of the FSOC architecture

Diode combinations	Voltage (V)	Resistor (Ω)	Container design's achievable range (cm)	
			Next to cube	Offset from cube
SFH-4556	10.002	5	164.4	263
SFH-4550	9.996	5	615.0	802
3 SFH-4556	15.011	5	407.3	532
3 SFH-4550	15.005	5	685.5	>914
LED Array	14.998	10	>914	>914

As indicated by the results, despite a 55% loss in light from the transmission characteristics of the beam splitting cube, each of the designs out perform the configuration in absence of a lens. This not only validates the improvement resulting from the of incorporation of a lens and beam splitter, but greatly expands upon the capabilities of the FSOC system. Nonetheless, it is clear that the holder which focuses the light on the surface of the photodiode is far superior than its counterpart, proving a concentrated beam is of utmost importance for achieving maximum range. With conclusive evidence backing the abilities of the beam splitter technology, the final stage of the thesis can be pursued.

8.6 System Capable of FSOC and Tracking of a Single Light Source

The ultimate aim of the thesis was the generation of a mechanism capable of automatically targeting and achieving a reliable, high-speed optical communication link via the same infrared light source. Integrating the VCA inspired 2DOF POM, cascade PID-PID control architecture, FC-Micro PCB, VHDL object recognition and parameter identification algorithms, the targeting models and finally, the FSOC system with



(a) Side view of the fully realized ATM.

(b) Top-down perspective of the ATM.

Figure 8.24: Fully realized ATM with targeting and optical communication capabilities.

beam splitter technology, finalized the construction of this mechanism. Unfortunately, due to time constraints, the entire structure was not adequately refined. However, preliminary experimentation was conducted to ensure the system was indeed capable of achieving the outcomes defined at the outset of the thesis. Therefore, to test the validity of the system, the optimal container designed in the previous section was incorporated into the 2DOF POM as shown in Fig. 8.24.

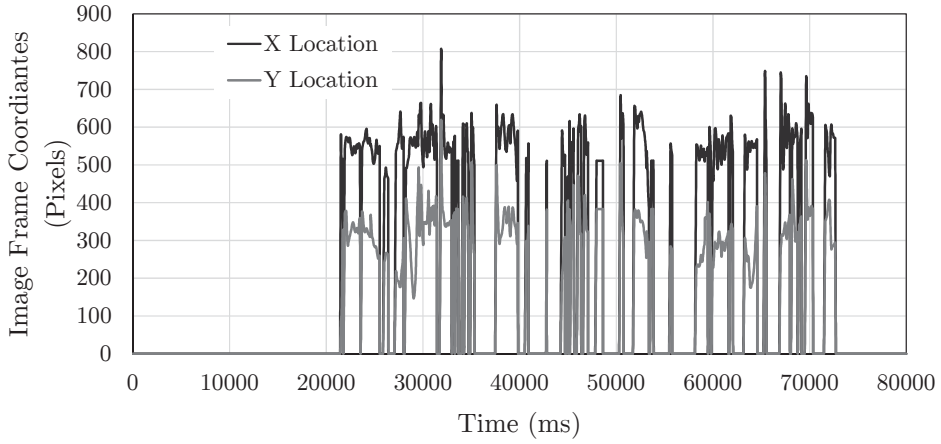
As the holder containing the additional components is much heavier than the 5 mm lens, in addition to the limited testing space and bottleneck imposed by the frame rate of the camera, the targeting system was unable to maintain a reliable lock on the pendulums described in Chapter 7. Therefore, to perform rudimentary testing of the

system, the LED array was manually displaced within a one meter area, at a distance of 25 feet from the targeting mechanism. Furthermore, the transmitter was configured to send three, arbitrarily chosen, 16-bit values (i.e., 26,921, 37,123 and 52,780), while the information received, centroid of the targeted array and VCA discrete positions were logged in tandem. The results of the experimentation can be viewed in Fig. 8.25.

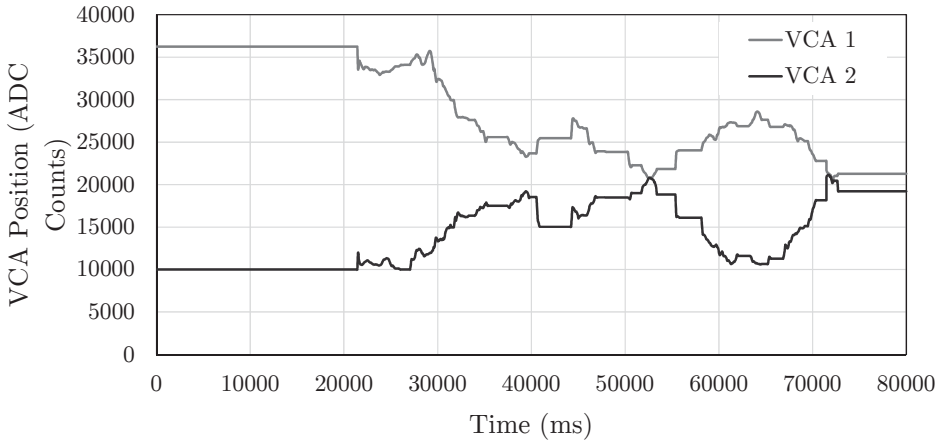
As shown, the error contained within the FSOC system is significantly greater than the results determined in section 8.4. Furthermore, despite the motions of the VCA indicating targeting, the centroid of the LED array fluctuates greatly from being near the center of the image frame to being undefined (i.e., zero). This directly affects to the performance of the FSOC, since when the centroid is zero, the image sensor is not detecting light and correspondingly, neither is the photodiode. This is likely a result of the lack of available testing space which permitted the image sensor from correctly identifying the object. As the sensor was too close to the IR source, the image was completely white when light entered the lens. Furthermore, the increased payload of the beam slitter holder negatively affected the accuracy and speed of the control methodology. However, despite the issues, the ATM did follow the LED array and communicate with it during many intervals. Nonetheless, with further refinement of the system via miniaturization of the beam splitter holder and adopting a more robust control strategy, improved outcomes would be achieved. Additionally, a larger test environment would ensure the system to be fully realized, resulting in a novel mechanism providing a plethora of optomechatronic applications.

8.7 Conclusions

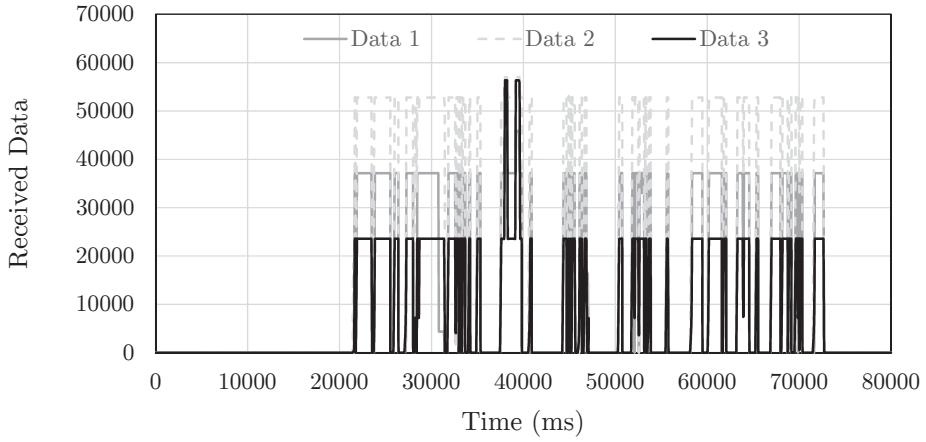
Electronic systems fulfilling SWaP requirements and providing high-rate transmission and receiving capabilities are very advantageous in optomechatronic applications. To



(a) Centroid locations of the LEDs during experimentation.



(b) Discrete VCA position recorded during the targeting of the transmitted light.



(c) Data logged while the transmitter was being targeted.

Figure 8.25: Experimental results of the ATM with FSOC capabilities.

this end, receiving and transmitting technologies were developed using off-the-shelf components with algorithms pertaining to each generated in VHDL via the F-Micro PCB. A simple, but effective communication protocol was realized allowing for reliable data synchronization upon signal loss. Additionally, the communication distance was drastically increased by introducing a narrow FOV lens to the receiver design. Furthermore, employing beam splitter technology to a modified lens enabled light transmission from a single source to be gathered by an image sensor and absorbed by the photodiode of the receiving circuit. Combining these devices with the targeting system developed in the previous chapter resulted in a novel mechanism. However, while it was capable of communicating and maintaining a constant fix on a single light source, limitations such as increased payload and testing space prevented the mechanism from reaching its full potential.

Chapter 9

Conclusions

From the outset, the desired outcomes of the thesis were to design and construct a reliable, dynamic and precise system capable of object recognition and automatic targeting while actively delivering a fast data link in free space. In consideration of the literature, it was determined that a systematic ground-up approach was best suited to achieve a mechanism of such complexity, primarily due to the ineffectiveness of assimilating multiple commercially available components. While pursuing this path could indeed prove to be optimal in nature, it required a significant amount of effort in contrast to simple system integration. Nevertheless, steps were taken to ensure no design was without merit and that each subsystem was fully realized before pursuing the next goal. Throughout the process, the desire to identify new knowledge in the form of technologies and applications was focused upon as evident in the final results. Each system was thoroughly tested to validate design philosophies as well as prove the efficiency of the ground-up strategy. Ultimately, the primary goals were accomplished as the mechanism theorized came to fruition.

9.1 Review of the Contributions

As specified in section 1.3, the contributions of this thesis relate to the design, development and experimentation of an ATM with FSOC functionality undertaken from a ground-up perspective. As such, the results pertaining to each individual subsystem will be discussed sequentially as their realization define the thesis outcomes.

As demonstrated by the results of the thesis, the need for dynamic, precise actuation in an extremely integrated design is key for optomechatronic applications. The feedback circuitry coupled with near frictionless linear guidance devices has produced a system capable of linear accuracy in the micron range. Additionally, the intense magnetic field generated by the modified Halbach arrays, combined with the high current potential of the PCB voice coil, generates considerable actuation forces in a extremely compact design. Furthermore, the self-contained planar construction of the VCA ensures simple integration into mechanisms while adhering to the strict constraints of SWaP. Thus, in the pursuit of optomechatronic applications multiple POM architectures were composed, resulting in the precise orientation of a mobile platform. Despite the more optimal nature of the 3DOF structure, the 2DOF was recognized as the ideal architecture for the ATM. This was primarily due to the coupling of the 3DOF, resulting in the orientation of a point in space being achievable by a number of combinations of the three actuator positions. Ultimately, the performance metrics accomplished by the VCA and both POMs showcase the exceptional functionality of these mechanisms, especially with respect to optomechatroinc applications.

Initially, it was theorized that the PID algorithm was incapable of providing accurate, robust control of the highly dynamic VCA due to is simplistic composition and inability to cope with sudden motion transitions. As such, to confirm the assumption, a digitally designed PID control loop was established and verified accordingly. In

response to the unsatisfactory results, an enhanced variation to the PID architecture known as the cascade PID-PID controller was tailored in VHDL to remedy the situation. Utilizing the fundamental principle of this algorithm, in addition to the change in position being corrected, its derivation or velocity is subsequently rectified. The hardware-based fabrication was not exclusively contrasted to PID control but was compared to the significantly more powerful but convoluted ADRC architecture. Through experimentation involving the alternation of the VCA's moving mass, it was confirmed that the ADRC in effect outperform both control schemes; a hypothesis originally developed. However, while the PID loop was drastically surpassed, the cascade rendition was quite comparable to the ADRC in many aspects, despite its relatively uncomplex nature. Thus, the cascade PID-PID scheme was chosen as a valid alternative for the control of the ATM, though it was bettered by ADRC in some regards.

The architecture for compiling algorithms on small-scale, portable devices include very stringent constraints on size, power consumption, weight and reliability. While FPGA-based hardware is naturally capable of delivering a system within these confines, the multipurpose construction of off-the-shelf designs and the restrictive nature of VHDL infers significant challenges. In addition, the complexity of optomechatronic applications predominantly requires hardware functionality absent from generalized boards. In this regard, Chapter 5 presents PCB layouts encompassing FPGA architecture, microcontroller technology and image sensing capabilities. Situating these devices on a solitary board increases reliable and bolsters robustness as the integration of multiple components is not required. Each design was rigorously validated through application specific experimentation resulting in customizable hardware, which allows for efficient integration into a variety of systems. Promoting the ability to control multiple linear actuators, a communication link between digital design and high-level

programming, the capacity to effortlessly solve complex mathematical equations, the potential of storing and manipulating image information and finally, granting regulated power to all devices via a single source, results in designs which are extremely beneficial for optomechatronic applications.

The real-time characterization of an object (i.e., light spot) achieving high maneuverability is non-trivial due to the complex, time-sensitive nature of the scenario. However, utilizing the power and parallelism of VHDL, a set of techniques were established permitting a region of interest to be classified in real-time. More specifically, converting the gathered pixel information from the color spectrum to a grayscale representation, followed by the image segmentation of data into binary values, an object was successfully segregated from its background. Exploiting these results, the crack code, contour tracking algorithm was implemented during the systematic scanning of the image to calculate a comprehensive set of independent form parameters corresponding to the region of interest. In particular, the procedure is formulated to provide the object's area and centroid location relative to the image frame's coordinate system. Communicating the results obtained from these methods to the microcontroller, act as the foundation of targeting system's functionality. The power of these techniques are a great boon to any object targeting device with mandatory SWaP and real-time constraints.

The orientation of a mobile platform with the strict focus of maintaining a lock on an object undergoing high dynamics is challenging to accomplish, primarily as a consequence of the real-time collaboration between a multitude of integral components. However, inspired by the performance of the POM architecture and the success of the hardware-based object identification algorithms, a system promoting the agile adjustment of a platform while exhibiting image recognition capabilities was formed. Furthermore, to define a robust target model, a set of non-linear equations were

generated by employing design of experiments methodology. These equations were created to relate the discrete location's of the linear actuators and centroid position of the determined object to actuator values resulting in object centering in the camera's FOV. Communicating the object's parameters to the microcontroller, applying these to the mathematical model and sharing the results to the FPGA resulted in the automatic targeting of the particular object. The system's accuracy was experimentally proven through static and dynamic object targeting. In addition, the mechanism's ability to follow moving objects while experiencing self-disturbance was validated, resulting in an reliable ATM for deployment in many application specific technologies.

The communication of extensive amounts of data at extreme rates has become a necessity in devices corresponding to the aerospace and underwater industries. More specifically, secure, high speed wireless communication links have been recognized as critical additions in an abundance of applications. In this regard, the thesis highlights a low-powered FSOC system fabricated by the assimilation of simple electronics accompanied by algorithms constructed in VHDL. Employing beam splitter technology into the receiving architecture produced huge improvements in transmission distance, even with an unrefined design. While the data rate and range were not extremely impressive, they were more than adequate in recognizing the system's potential and can be improved upon with straightforward additions to the circuitry. Correspondingly, the architecture's synchronization capabilities were explored and an approximation of the worst case scenario, BER was determined. Finally, as a testament to the outcomes of the thesis, the receiver framework was incorporated into the mobile platform of the ATM. The final conglomeration of these systems generated a mechanism with the ability to locate and target an infrared light source while simultaneous providing data transmission via its FSOC functionality. The prototype architecture was tested, revealed promising outcomes and with additional refinement

would result in an exceptionally versatile optomechatronic mechanism.

9.2 Limitations of the Reported Research

At the dawn of any considerable research collaboration, it is of extreme importance to envision a strict set of achievable goals to remain focused and vigilant. Furthermore, becoming absorbed in the investigation and overreaching when unnecessary is a pitfall which must be avoided at all costs. In contrast, devising objectives which are unambitious is equally as concerning as the pursuit of generating new knowledge should be of utmost importance. However, as time passes, issues unaccounted for arise and the ability to pivot seamlessly from one idea to the next must be practiced in response. Nevertheless, no matter how well the path is traveled, limitations will undoubtedly surface within any study being pursued. In response, the determination and discussion of these limitations must be explored to fully realize the long-term accomplishments of the research.

The technologies theorized by this study were constructed within the confines of a university environment; thus, it is understandable that the majority of the systems did not reach a state of ready deployment. While the results of extensive experimentation proved extremely promising, testing procedures were predominately restricted to laboratory environments. Without knowledge acquired from real-world test conditions (i.e., extreme weather and temperature settings) the validation of the technology cannot be fully substantiated. This was particularly evident in consideration of the lack of viable testing capacity when attempting to determine the maximum achievable distance of the FSOC.

Time limitations are one of the most fundamental concerns prohibiting the results of many projects. No matter how stringent a path is defined, how often research is

being pursued or how capable an individual may be, time will undoubtedly effect the achievable goals of any study. This thesis proved comparable as time was the greatest constraint on its results. Most notably, it greatly affected the development and cultivation of the stand-alone FSOC hardware and refinement of the FSOC capable ATM. Despite the promising outcomes of the prototype mechanisms, it was the absence time which prevented higher standards being realized.

Finally, technical limitations of the methodologies utilized in the majority of research and development endeavors have an effect on their outcomes. As many of the components comprising the ATM are realized through the use of FDM, mechanical tolerances can be tightened through a more robust manufacturing process. The chosen control method can be improved or replaced, increasing pointing accuracy of the ATM. The image sensor employed in the design lacks high resolution and reduces accuracy in the tracking and targeting algorithms. Furthermore, the resulting frame rate imposes a significant time limitation on the targeting algorithm. Lastly, the FSOC protocol was designed swiftly and would benefit from a redesign using fundamental transmission standards.

9.3 Recommendations for Future Research

While the majority of the technologies presented in this thesis performed exceptionally well, in any design there is always an opportunity for enhancement. For instance, the image sensor and corresponding storage devices integrated into the completed system are an aging technology. Replacing the sensor with a HDMI functional, high resolution device and the SRAM chips with double data rate (DDR) memory will have a vast improvement on the image sensing and object recognition capabilities.

The communication convention employed by the optical communication system was

created promptly to pursue simple data transmission and reliable data synchronization. However, this was at the expense of an efficient protocol which would give rise to optimal transmission rates. Correspondingly, configuring a more idealistic synchronization algorithm which systematically checks for receivable data at the bit level, in comparison to packet scanning, will undoubtedly increase effectiveness.

As range is a fundamental metric in the performance of FSOC, the cube incorporated within the beam splitter device can be exchanged with a more optically efficient plate structure. This configuration is capable of redirecting a substantial portion of the light to the photodiode in contrast to an even split between both sensors. Considering the intensity of light absorbed greatly affects the quality of the FSO link, it is realistic to assume that this replacement will have an particularly beneficial effect on the outcomes of the FSOC system.

Another interesting prospect for FSOC experimentation would be to delve into the study of parallel FSOC. A transmission device can be fabricated in an array of alternating infrared diodes capable of generating light at a variety of wavelengths. The transmitting algorithm can be accomplished by breaking a data packet into sections and assigning each segment to diodes of a specific wavelength. By pulsing all diodes during one cycle, while simultaneously receiving and decoding each pulse with a photodiode corresponding to the wavelength, a communication link can be formed. A system such of this would be capable of transmitting data in pseudo-parallel fashion, drastically increased the output of the system.

Finally, the sequential nature of the thesis dictated that the ATM with FSOC functionality could only be developed at the final stages of the study, resulting in a proof-of-concept mechanism. Correspondingly, little refinement was accomplished and time prevented the amount of validation it received in contrast to the many subsystems forming its composition. Thus, further improvement by bettering the beam splitter

container, replacing the current image sensing hardware and devising more robust test scenarios would be a tremendous boon in discovering the true potential of such a novel mechanism.

9.4 Final Remarks

The precise, dynamic capabilities of the novel VCA were established by its ability to achieve micron accuracy and velocities above 1.3 ms^{-1}. To compliment this performance, a hardware-based cascade PID-PID control scheme was completed demonstrating average settling times of 23 ms, with an average steady state error of 125 ADC counts while being under the influence of heavy payloads. Additionally, to remain with the confines of strict SWaP requirements, customized PCBs fixed with FPGA, microcontroller and image sensing technologies were created. Despite their stand-alone achievements a shared memory controller provided a fast, reliable communication link between the FPGA and microcontroller, further increasing the PCBs functionality. Utilizing its capabilities, a set of algorithms were designed to isolate and characterize form parameters of a localized object in the image sensor's FOV. This resulted in the real-time object recognition and targeting at update rates of 70 ms. Correspondingly, combining the 2DOF POM with the object identification algorithms, non-linear equations were devised to allow for automatic targeting to be pursued. Furthermore, a power efficient FSOC system was created along with beam splitting technology resulting in reliable free space communication with transmission rates of 1 Mbits per second at ranges greater than 30 feet (maximum testable range). Finally, all of the systems were assimilated to form a mechanism capable of precise, agile automated targeting and fast, reliable communication with a single IR light source opening an avenue to a plethora of optomechatronic applications; thus achieving the initial goals

envisioned for this thesis.

9.5 Publication List

The following is a list of contributions and patents provided by and in-part by the author during the development of the thesis goals:

- D. Hicks, T. Rahman, and N. Krouglicof, "A High Performance Voice Coil Actuator for Optomechantronic Applications," ASME Journal of Mechanisms and Robotics, 2017 [in press].

- N. Krouglicof, M. Morgan, N. Pansare, T. Rahman, and D. Hicks, "Development of a novel pcb-based voice coil actuator for opto-mechatronic applications," in *Intelligent Robots and Systems (IROS), 2013 IEEE/RSJ International Conference on.* IEEE, 2013, pp. 5834-5840.

- T. Rahman, D. Hicks, M. R. Hossain, and N. Krouglicof, "Digital hardware implementation of an active disturbance rejection controller for a highly dynamic parallel orientation manipulator," in *Robotics and Automation (ICRA), 2014 IEEE International Conference on.* IEEE, 2014, pp. 5750-5757.

- N. Krouglicof, T. Rahman, and D. Hicks, "Parallel kinematic mechanism and bearings and actuators thereof," U.S. Patent and Trademark Office Patent Application 61 700 080, September, 2012.

Table of Abbreviations

Acronym	Definition
FSOC	free space optical communication
VCA	voice coil actuator
SWaP	size, weight and power
ATM	automatic tracking mechanism
POM	parallel orientation manipulator
PID	proportional-integral-derivative
FPGA	field programmable gate array
ADRC	active disturbance rejection controller
HDL	hardware description language
PCB	printed circuit board
FOV	field of view
DOE	design of experiments
RF	radio frequency
INSPIRUS	Intelligent Sensor Platforms for Remotely Piloted Vehicles
MUN	Memorial University of Newfoundland
SoC	system-on-a-chip
VHSIC	very high speed integrated circuits
VHDL	very high speed integrated circuits hardware description language
UAV	unmanned aerial vehicles
MIR	mid-infrared
SNR	signal to noise ratio
BER	bit error rate

Continued on next page

Table of Abbreviations – *Continued from previous page*

Acronym	Definition
PSD	position sensitive detector
1D	one-dimensional
VCSEL	vertical cavity surface emitting laser
ADC	analog-to-digital converter
Op-Amp	operational amplifiers
PC-ABS	polycarbonate-acrylonitrile butadiene styrene
FDM	fused deposition modeling
CMM	coordinate measuring machine
CI	confidence interval
DOF	degrees of freedom
3D	three-dimensional
CAD	computer aided design
PWM	pulse width modulation
PD	proportional-derivative
ESO	extended state observer
CPLD	complex programmable logic device
IDE	integrated development environment
I/O	input-output
FTDI	Future Technology Devices International
2D	two-dimensional
SRAM	static random access memory
VGA	video graphics array
VDAC	video digital-to-analog converter

Continued on next page

Table of Abbreviations – *Continued from previous page*

Acronym	Definition
API	application programming interface
GUI	graphical user interface
PC	personnel computer
RGB	red-green-blue
IR	infrared
UAS	unmanned aerial systems
AUV	autonomous underwater vehicles
LED	light emitting diode
MOSFET	metaloxidesemiconductor field-effect transistor
DDR	double data rate

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