Electrical transport in ultrathin Cs layers on Si(001)

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Electrical transport in ultrathin Cs layers on Si(001) has been studied combining macroscopic conductivity measurements with low-energy electron diffraction, energy loss spectroscopy, and measurements of the work function. At temperatures around 150 K, growth of the first three atomic layers proceeds layer-by-layer. The completion of each layer correlates with stepwise increases of the surface sheet conductance with coverage. Calibrating the Cs coverage by combined conductivity and work function measurements, the areal density of a single atomic layer is determined as 0.5 monolayers (3.39×10^{14} cm^{-2}). Electron spectroscopy reveals a semiconductor-metal transition of the surface upon completion of the first atomic layer, which correlates with the onset of a macroscopically measured sheet conductance in the 10^{-5} Ω^{-1} range. While the conductance can be ascribed to electrical transport within surface states, its dependence on temperature indicates an activation barrier, which, most likely, is due to domain boundaries. At coverages of one monolayer and beyond, the Cs/Si(001) surface exhibits a high metal-like conductance in the 10^{-3} Ω^{-1} range.

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I. INTRODUCTION

Studies of alkali metal (AM) layers deposited on semiconductor surfaces have been stimulated by technological prospects, e.g., the use of alkali layers as easy-to-remove promoters of oxidation (see Refs. 1 and 2 and references therein), as well as by fundamental interest in properties of two-dimensional metallic systems and metal-semiconductor interfaces. AM layers are regarded as model systems for the surface metalization upon metal deposition, and their investigation has led to some pivotal observations. For example, the formation of one-dimensional metallic chains had been suggested by the observation of an azimuthal anisotropy of the surface plasmon dispersion for K/Si(001) (Ref. 3). Later a two-dimensional Mott insulator-to-metal transition was identified for the Cs/GaAs(011) interface.[4] Meanwhile electron spectroscopies have also revealed a Mott insulating ground state on K/Si(111)-($\sqrt{3}\times\sqrt{3}$)R30°-B (Ref. 5) and electronic phase transitions for sub-monolayer coverages of Na and Cs on Si(001) or Si(111) (Refs. 6 and 7). Despite the seeming simplicity of the alkali metal adsorption and the wealth of information about atomic and electronic structure that has been collected by many surface science techniques, even fundamental issues like, e.g., the AM saturation coverage at room temperature have been an issue of long debate until recently[8–11] so that some keys for a detailed understanding of the electronic properties are still missing.

Combining macroscopic measurements of electrical conductivity at variable temperatures with low-energy electron diffraction (LEED), energy loss spectroscopy (EELS), and measurements of the work function, we aim at identifying correlations between structure and electrical transport at the surface of ultra thin Cs layers on Si(001). At temperatures around 150 K we find that growth proceeds layer-by-layer up to three atomic layers. Jumps of the surface sheet conductance as a function of coverage are clearly correlated with structural transitions of the surface. Measured on a macroscopic scale, conduction through surface states is expected to be strongly affected by surface defects like steps or domain boundaries. EELS, on the other hand, is a local probe, providing information on electronic excitations within the domains. A full account of our combined studies will be given in this paper. It will be demonstrated that a metallic surface phase in the submonolayer regime, previously identified by electron spectroscopy, opens a channel for electrical transport in surface states and we will propose a method for calibrating the Cs coverage on Si(001) by measurements of the surface conductivity.

II. EXPERIMENT

The experiments were carried out in ultrahigh vacuum (base pressure below 5×10^{-9} Pa) using four-probe surface conductance measurements and an ELS-LEED system which may be considered as LEED with high energy resolution (typically 10 meV full width at half maximum) or as EELS with high momentum resolution (experimentally limited by the quality of the sample surface, best achieved resolution 0.04 nm^{-1}). Details of the ELS-LEED system can be found elsewhere.[12] The Si(001) substrate samples, $0.3\times10\times15$ mm^3 in size, were cut from a phosphorus-doped wafer of high resistivity (>1000 Ω cm) and mounted on a liquid nitrogen cooling stage. The substrate surfaces were prepared by repeated rapid direct current heating to 1100 °C while keeping the ambient pressure below 2×10^{-7} Pa. The surface quality was monitored by LEED.

For conductance measurements, electrical current was sent through tantalum clamps fixed at both ends of the sample. In order to ensure good electrical contact between clamps and sample, as well as to obtain a highly symmetrical variation of the electrical potential across the sample, titanium silicide pads were generated on both ends of the substrate. Cs was evaporated both onto the bare parts of the substrate and onto the titanium silicide pads. In the center two Ta tips were pressed onto the substrate by a springy metal wire for voltage measurements. The distance between

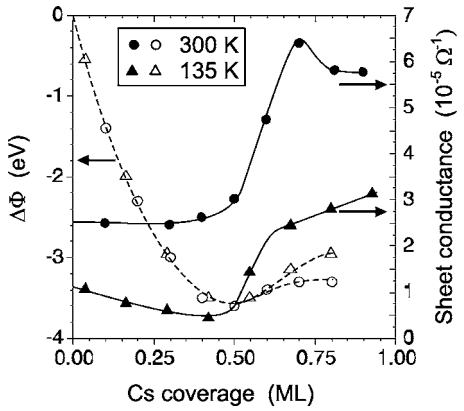

FIG. 1. Simultaneous measurement of sheet conductance (filled symbols) and change in work function (open symbols) during Cs deposition at 135 K (triangles) and at room temperature (circles), resp. The deposition was interrupted for each measurement of the work function. The Cs coverage is calibrated via the minimum of the work function. Lines are meant as guide to the eyes.

both tips on the sample surface was 8 mm. Using direct current in the range 30–100 μA, the sheet conductance was determined by averaging over the ratio U/I measured at both polarities.

Cs was deposited from well-outgassed chromate dispensers (SAES getters) keeping the pressure in the 10^{-8} Pa regime. A relative measure of the work function was taken from the onset of current in I-V curves of an electron beam diode, which was set up using the LEED gun. For ELS-LEED and work function measurements the deposition of Cs had to be interrupted due to the geometry of the ELS-LEED system, while conductance measurements could be performed also during alkali deposition.

III. RESULTS AND DISCUSSION

A. Calibration of coverage

First, the calibration of Cs coverage shall be addressed. Figure 1 shows the sheet conductance (solid lines) and changes of the work function ($\Delta\Phi$, dotted curves) depending on the amount of Cs deposited on the clean Si substrate at two different temperatures (300 and 135 K). Cs was deposited in steps with fixed increments of coverage. Sheet conductance and work function were measured after each step. In order to keep the amount of deposited material the same for each step within either series of depositions, the procedure for starting the dispenser and the total amount of deposition time for each step were kept the same for either series. Both work function curves exhibit a distinct minimum at $\Delta\Phi=-3.5$ eV, which we take as an indicator of a Cs coverage of 0.5 monolayer (ML) according to a calibration of coverage by Auger electron spectroscopy.[1] Here one monolayer denotes the density of atoms in the top layer of a Si(001) surface, i.e., 6.783×10^{14} atoms/cm^2.

The minimum of $\Delta\Phi$ coincides with the onset of a stepwise increase of the sheet conductance by 2 to 4 $\times10^{-5}$ Ω^{-1}. Observing this stepwise increase in the whole range of temperatures of our experiments and for different samples, we have calibrated the amount of deposited material for all measurements in the following via the onset of the conductance increase in the 10^{-5} Ω^{-1} range.

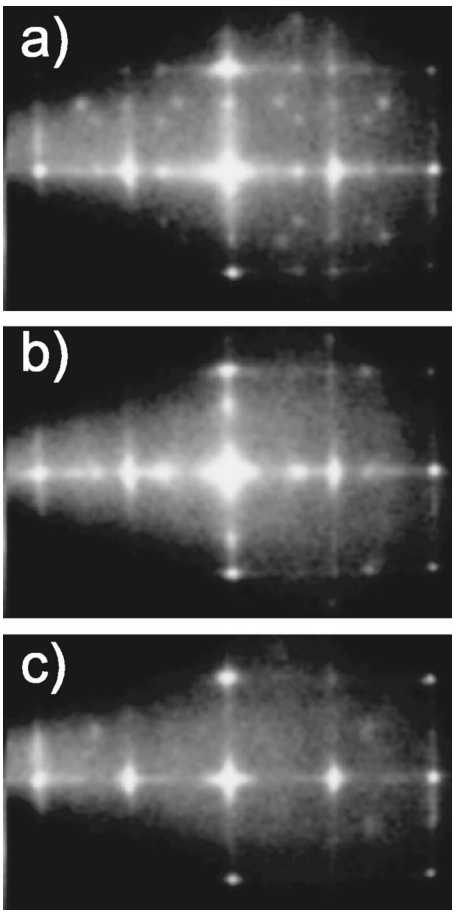

FIG. 2. LEED (primary energy 59 eV) of Cs/Si(001)-(2×1) for submonolayer coverages (a) 0.15 ML, (b) 0.33 ML, and (c) 0.66 ML (deposition and measurement at 165 K). All patterns exhibit the specular reflection in the center and first integer order spots on the right and the left side of the field of view.

B. Surface structure

Based on an unambiguous determination of Cs coverage, we can identify structural transitions of the Cs/Si(001) surface that correlate with jumps of the surface sheet conductance as a function of Cs coverage. Before demonstrating these correlations for the coverage range up to a few monolayers, first our LEED and EELS results will be presented. Their discussion within the context of previously published experimental work and surface structure models shall give an overview of the encountered Cs/Si(001) surface structures.

Several ordered surface phases have been reported for Cs/Si(001) in the submonolayer regime.[13] Figure 2 shows LEED patterns that we obtained for three different submonolayer coverages of Cs deposited at a temperature of 165 K. Besides bright spots due to the 2×1 dimer row reconstruction, spots due to 3×4 symmetry can be identified for 0.15 ML coverage [Fig. 2(a)] while 3×2 spots appear for 1/3 ML coverage [Fig. 2(b)]. At around half monolayer coverage

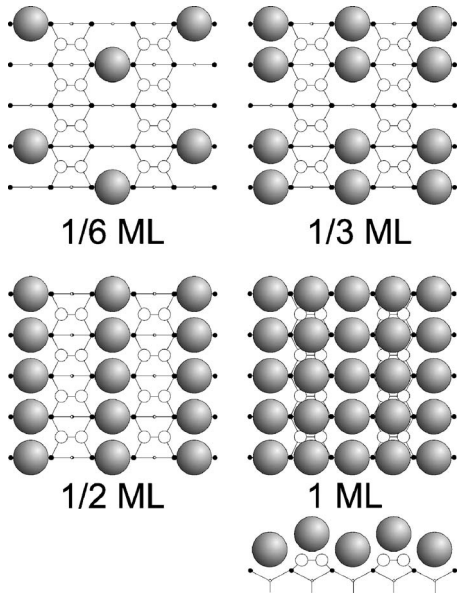

FIG. 3. Schematics of assumed structure of Cs/Si(001) for various coverages in the submonolayer regime based on results of Refs. 11 and 14. For the model of 1 ML coverage, also a side view is shown.

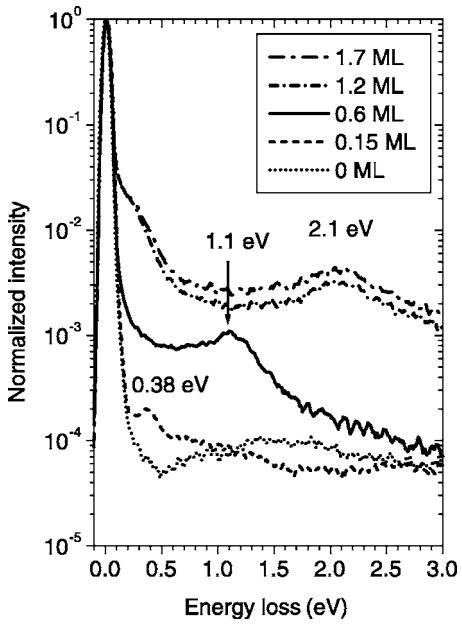

FIG. 4. EELS of clean Si(001) substrate and after deposition of 0.15, 0.6, 1.2, and 1.7 ML Cs, resp. Deposition and measurement were carried out at a temperature of 165 K. Intensities are normalized to maximum intensity.

we find only 2×1 spots in LEED. At around 2/3 ML coverage the recurrence of weak intensity close to (2/3,1/4) positions is observed which may indicate some short-range 3×4 order. However, up to the Cs deposition of 1 ML and more, the LEED pattern is dominated by 2×1 spots.

Comparing these results with previous LEED and photoelectron diffraction measurements on single domain surfaces[14] and with scanning tunneling microscopy (STM) data[15] we find reasonable correspondence. At a temperature of 320 K Abukawa *et al.* identified three ordered phases at 1/6, 1/3, and 1/2 ML coverage.[14] For 1/6 ML coverage they report streaky LEED spots at third-order positions instead of the 3×4 symmetry observed in our experiments, and proposed a structure composed of one-dimensional Cs arrays along the Si(001) dimer rows with Cs atoms placed on each third lattice site. We suggest that at 165 K weak interaction between the proposed one-dimensional arrays may lead to the condensation of two-dimensional domains of zigzag chains perpendicular to the dimer rows, exhibiting 3×4 symmetry as depicted schematically in Fig. 3. We do not observe the 3×4 reconstruction when depositing Cs at 125 K, which indicates that at temperatures below ≈130 K diffusion is not high enough for the ordering of adsorbates. For this reason Abukawa *et al.* had always annealed the surface up to 270 K when studying Cs/Si(001) surface phases at 110 K. Provided that the surface was not quenched too quickly after annealing up to 270 K, their observation of, again, a streaky $\times3$ pattern at 110 K indicates that the 3×4 reconstruction is a metastable surface structure.

For 1/3 ML coverage Abukawa *et al.* observed a 2×3 reconstruction at 320 K in accordance with our results. Coinciding with a 2×3 LEED pattern, Xu *et al.* found chains of Cs atoms oriented perpendicular to the Si dimer rows and separated by 3 lattice constants in STM images. Their structure model for a coverage of 1/3 ML is depicted schematically in Fig. 3 as well as structure models for 1/2 and 1 ML coverage based on Refs. 9, 14, and 15. Initial Cs adsorption is assumed to take place on T3 sites in the troughs between dimer rows, taking also into account recent results of He ion scattering spectroscopy.[11,16] The structure models are shown here as a quick reference for the following discussion of electrical transport and electronic structure.

As first approach, one may guess, simply by counting the valence electrons within a surface unit cell, that the surfaces with 1/2 ML coverage should be metallic while the 3×2 structure for 1/3 ML coverage is probably insulating because the number of valence electrons is even. In fact, a corresponding semiconductor—metal transition with increasing Cs coverage in the submonolayer regime was identified by EELS at room temperature.[17] By counting valence electrons one would also guess that the 3×4 structure at 1/6 ML may be insulating, too. However, in accordance with Ref. 17 we also find at 165 K a loss feature at ≈380 meV at around 1/6 ML coverage (Fig. 4), which was ascribed to plasmons of Cs 6*s* electrons occupying an empty substrate surface band.[17] The disappearance of this loss with increasing coverage indicates that the surface becomes insulating up to a coverage of 0.5 ML. After depositing ≈0.6 ML we find an energy loss at 1.1 eV in the spectra which was ascribed to overlayer plasmons.[17,18] It should be noted here that, as demonstrated in Ref. 17, the 1.1 eV plasmon loss can already be observed in EELS when the work function is at its minimum, i.e., at a coverage of 0.5 ML.

With increasing amount of deposited Cs, we find that at 165 K the 1.1 eV feature becomes very broad and finally turns into a loss peak at 2.1 eV after deposition of 1 ML Cs, in contrast to the results obtained by Lee and Chung at room temperature.[17] The loss may represent a transversal plasmon

of a thin Cs overlayer, because its energy is close to that of the Cs surface plasmon. This plasmon is expected at $\omega_B/\sqrt{2}=2.05$ eV, with $\omega_B=2.9$ eV as Cs bulk plasmon energy.[19] It has been experimentally found at 1.99 eV (Ref. 20).

Comparing the observed Cs/Si(001) plasmon frequencies (0.38, 1.1, and 2.1 eV, respectively) it is striking that their ratio corresponds to the ratio of the corresponding Cs coverages (1/6, 1/2, 1 ML, resp.). The observation suggests that up to 1 ML Cs coverage, the charge carrier density in the conduction band of ordered metallic surface phases is directly proportional to the Cs coverage. However, the plasmon frequency does not vary continuously with coverage, and the surface is nonmetallic at 1/3 ML coverage. Consequently, there is not a single metallic surface state band, being continuously filled by electrons donated by adsorbed Cs.

We do not observe a significant Drude tail in our spectra, probably because of the high momentum resolution of the ELS-LEED system. The spectra in Fig. 4 represent scattering without momentum transfer parallel to the surface. For all coverages any low-energy loss appears clearly separated from the elastic peak.

Summarizing the structural information so far, the surface exhibits metallic phases at around 1/6 and above 1/2 ML Cs coverage, respectively, while the surface is nonmetallic at around 1/3 ML coverage. At 1/2 ML coverage the Cs/Si(001) surface is probably composed of Cs chains in the troughs between the substrate dimer rows while at 1 ML coverage it is probably composed of a double layer chain structure. In fact, the shift of the plasmon frequency upon deposition of 1 ML Cs observed at a temperature of 165 K indicates a structural transition while the symmetry of the surface reconstruction remains 2×1. Correlations between surface structure and electrical transport within the surface will be demonstrated in the following.

C. Electrical transport

1. Correlations with surface structure

The sheet conductance during Cs deposition measured at four different deposition temperatures around 150 K is shown in Fig. 5. The horizontal axis refers to the amount of deposited material. Since the vapor pressure of Cs is in the range of 10^{-13} Pa at a temperature of 170 K, we assume the sticking coefficient to be close to 1 up to that temperature so that the horizontal axis should also represent the coverage. Due to imperfections of the electrical contacts and due to irradiation by the heated dispenser (dark red glow), sudden changes and variations of the sheet conductance (σ) of the order of $10^{-6}\ \Omega^{-1}$ were observed when the shutter was opened for Cs deposition. Therefore, from all measuring curves represented in Fig. 5 the respective conductance value at 0.3 ML coverage $[\sigma(\Theta=0.3\ \mathrm{ML})]$ was subtracted so that Fig. 5 shows $\Delta\sigma=\sigma-\sigma(\Theta=0.3\ \mathrm{ML})$. The inset reveals, on a smaller scale, details of the four measuring curves in the coverage range up to 1 ML. Below 0.5 ML coverage, the conductance does not vary significantly above the level of data scattering due to imperfections of the electrical contacts. All curves, however, exhibit stepwise increases in the

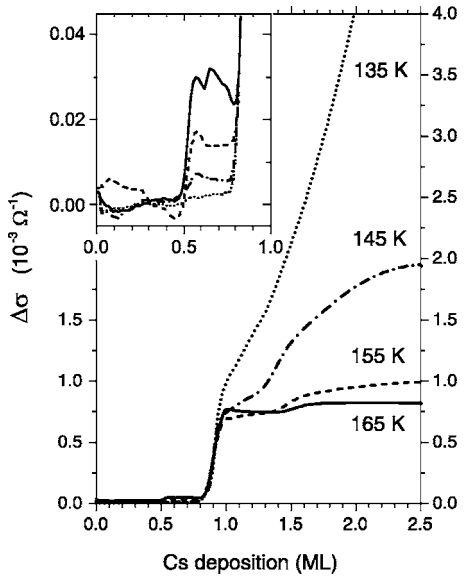

FIG. 5. Sheet conductance during Cs deposition at temperatures of 135 K (dotted lines), 145 K (dashed-dotted), 155 K (dashed), and 165 K (solid lines), resp. The inset shows details of the conductance curves in the coverage range below 1 ML.

$10^{-5}\ \Omega^{-1}$ range after completion of 0.5 ML and show a local maximum at around 0.58 ML. With respect to coverage, the conductance increases right after the work function exhibits its minimum, which coincides with the appearance of emission at the Fermi edge in photoelectron spectroscopy[18] and of the 1.1 eV plasmon loss in EELS.

Upon further increase of Cs coverage, but before the completion of 1 ML coverage, the conductance rises again in a step-like manner. While the conductance reaches a maximum of $0.8\times10^{-3}\ \Omega^{-1}$ at 1 ML coverage at a temperature of 165 K, it increases monotonously upon further Cs deposition at temperatures of 135 K and below. At the same time the LEED pattern becomes diffuse, i.e., the background intensity increases, while the diffraction spots become weaker. At temperatures of 165 K and higher, the LEED pattern always exhibits clear spots of a 2×1 reconstruction during continued deposition. Obviously, the conductance curves measured at 145 and 155 K mark a transition between two growth regimes. For temperatures $\leqslant$135 K Cs grows as a continuous, but probably polycrystalline three-dimensional film, while at temperatures of 165 K and higher a wetting layer of limited thickness is formed, on top of which either separated three-dimensional islands build up or additional Cs does not stick. As mentioned before, given the low vapor pressure of Cs of 10^{-13} Pa at 170 K, it seems reasonable to assume that additional Cs does condense onto the surface, forming, however, no percolated path for electrical transport, but three-dimensional islands.

A rough estimate shows that the order of magnitude of sheet conductance measured for 1 ML Cs/Si(001) is as high as expected for metallic Cs: The conductivity of bulk Cs at 160 K is $\approx10^5\ \Omega^{-1}\ \mathrm{cm}^{-1}$ (Ref. 21). If bulk properties could simply be scaled down to atomic dimensions, then a metallic Cs layer with a sheet conductance of $10^{-3}\ \Omega^{-1}$ had a thickness of 0.1 nm, which is a reasonable order of magnitude for

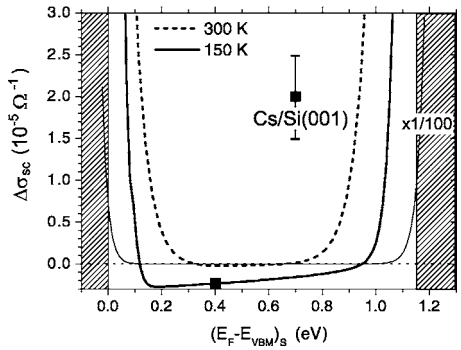

FIG. 6. Surface conductance of the space charge layer calculated as a function of the Fermi level position at the surface with respect to the valence band maximum for temperatures 150 K (solid line) and 300 K (dashed line). The thin solid line represents the result for 150 K scaled by a factor of 1/100. The ordinate indicates the excess conductivity with respect to the flat band condition. The data points mark the position of E_F at the surface as determined by Refs. 6 and 27 for the clean substrate and for Cs/Si(001) at room temperature and at saturation coverage, resp. The right data point is shown with error bars denoting the range of measured surface conductance of Cs/Si(001) in the coverage range $0.5<\theta<1$ (see Fig. 5).

the thickness of a single monolayer. The increase of conductance at 1 ML coverage coincides with the formation of the 2.1 eV Cs overlayer plasmon loss in EELS. While the loss spectra do not change significantly upon further Cs deposition, the conductance curve at 165 K shows a slight decrease at coverages above one monolayer, probably due to electron scattering at surface roughness caused by Cs adatoms or islands. All four conductance curves exhibit an increase and a change of slope at around 1.3–1.5 ML coverage, which we take as a fingerprint of the completion of an additional atomic layer. Please note that here a single "atomic layer" of Cs is defined as having an areal density of 0.5 ML. The magnitude of the increment of conductance at $\approx$1.5 ML coverage decreases as the deposition temperature is increased. Furthermore, at 165 K the increment is small compared to the conductance increase observed when the double layer structure is formed at 1 ML coverage. Consequently, the sheet conductance as a function of coverage indicates that growth proceeds layer-by-layer up to the third atomic layer at around 150 K, but the third layer is probably far from being well-ordered.

2. Surface contribution to the sheet conductance

The completion of the Cs overlayer at 1 ML coverage and the formation of the metallic Cs/Si(001) surface phase at 1/2 ML coverage clearly correlate with jumps of the sheet conductance as a function of coverage. Apart from electrical transport within the metal layer or substrate surface states altered by the adsorbate, $\Delta\sigma$ may contain a significant contribution from a substrate space charge layer at the surface. In order to elucidate that contribution, it was calculated according to Refs. 22 and 23. Figure 6 shows the change of the conductance through the space charge layer $\Delta\sigma_{sc}$ with respect to the flat band condition as function of the Fermi level position at the surface $(E_F)_S$. E_{VBM} denotes the energy of the valence band maximum. While the result for 300 K is shown as dashed line, the result for 150 K is shown as solid line with the thin solid curve being scaled by a factor of 1/100. For the calculation we estimated the donor density of our *n-type* substrate as 4.5×10^{12} cm^{-3}, which corresponds to a Fermi level position in the bulk of 0.94 eV above the valence band maximum (VBM) at 150 K and of 0.63 eV above VBM at 300 K, respectively.[24] For the charge carrier mobilities, values of bulk Si have been taken. In this way we obtain an upper limit for the space charge layer conductance because the mobilities at the surface are always reduced with respect to the bulk values due to scattering at surface roughness.[25,26]

At the clean dimerized Si(001) surface the Fermi level is pinned by surface defects[28] at 0.4 eV above VBM.[27] The band bending upon Cs adsorption was estimated from photo emission spectroscopy data by Chao *et al.*[18] As Si core level spectra show, the Fermi level shifts by 0.15 eV towards VBM after initial Cs deposition and then by 0.45 eV towards the conduction band minimum till the saturation coverage at room temperature is reached. Combining the results of Refs. 27 and 18, the Fermi level position at the surface at saturation coverage is obtained as $(E_F)_S=E_{VBM}+0.7$ eV. While it has been debated controversially whether the saturation coverage is one monolayer at room temperature as assumed by Chao *et al.*, it is clearly beyond the coverage where the work function minimum occurs. The work function saturates at coverages above 0.6 ML, rendering significant charge transfer from the Cs layer to the Si substrate unexpected for higher coverages. Consequently, we take $(E_F)_S=E_{VBM}+0.7$ eV as the maximum value for the Fermi level position at the surface. When the Fermi level position at the surface is changed from $(E_F)_S-E_{VBM}=0.4$ eV to $(E_F)_S-E_{VBM}=0.7$, the estimated increase of the conductance of the space charge layer is less than $10^{-6}\,\Omega^{-1}$ in the temperature range 150–300 K. So the observed increase in conductance above 0.5 ML coverage must be mainly due to electrical transport through Cs/Si(001) surface states.

3. Dependence on temperature

For a Cs deposition experiment in the submonolayer regime the dependence of sheet conductance on temperature is shown in Fig. 7. Curve *a* shows the conductance of the clean Si substrate in the temperature range 130–270 K. At 140 K a significant fraction of donors is ionized and phonon scattering leads to a decrease of the conductance as the temperature is increased. At around 250 K the conductance increases again due to an increasing number of intrinsic charge carriers in the conduction band. Curve *b* shows the sheet conductance after deposition of $\approx$0.6 ML Cs on the Si substrate. Cs was deposited at 188 K (dashed line) until the first stepwise increase of conductance was observed and the maximum was reached. Then the surface was annealed up to 290 K and cooled down to 125 K (curve *b*). The conductance changed reversibly upon subsequent heating and cooling. The magnitude of surface conductance in Fig. 7 is significantly lower than in the experimental data of Fig. 5, probably due to in-

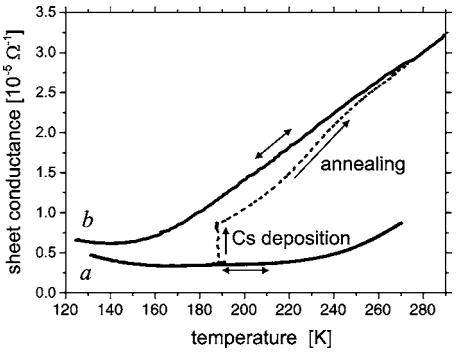

FIG. 7. Dependence of sheet conductance σ of substrate (solid curve *a*) and of 0.6 ML Cs on that substrate (solid curve *b*) on temperature (both curves reversible upon heating and cooling). Dashed curve represents Cs deposition at 188 K (terminated at first maximum of σ) and subsequent annealing up to 290 K.

creased substrate surface roughness due to variations in substrate preparation.

Figure 8 shows the difference between curves *b* and *a* of Fig. 7 in order to extract the Cs/Si(001) surface contribution to the sheet conductance. As demonstrated earlier, the contribution by the substrate space charge layer is negligible. Apart from the substrate bulk conductance, however, electrical transport within the surface states of clean Si(001) may contribute to curve *a*. In fact, the surface state conductance of a clean SOI(001) surface has been determined by Yoo and Weitering[25,26] as $\approx 2.5\times10^{-6}\ \Omega^{-1}$ at a temperature of 200 K, showing a clear signature of the $c(4\times2)\rightarrow2\times1$ order-disorder phase transition at about 200 K and an increase by a factor of 3 as the temperature is decreased to 140 K. While the absolute value of the sheet conductance of our clean Si(001) substrate is on the order of the result of Refs. 25 and 26 for the surface state contribution, our data show no sign of the structural phase transition, and the sheet conductance varies by only $\approx$20% in the temperature range 140–220 K. Furthermore, we do not observe significant changes of the conductance upon the deposition of the first 0.5 ML Cs, which would be expected if the Si(001) surface states contributed significantly. Therefore, curve *a* must be dominated by the substrate bulk conductance so that Fig. 8 represents

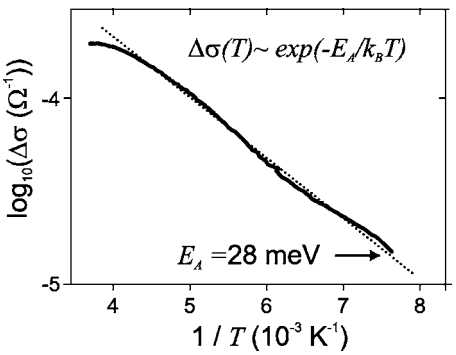

FIG. 8. Difference $\Delta\sigma$ between curves *b* and *a* of Fig. 7, representing Cs/Si(001) surface state conductance including a minor contribution from the space charge layer. The Arrhenius plot yields an activation barrier of 28 meV for electrical transport.

the Cs/Si(001) surface state contribution to the sheet conductance. The Arrhenius plot yields an activation barrier of 28 meV for electrical transport in the temperature range 130–240 K.

4. Supersaturation fraction and activation barrier

The stepwise increase of the conductance as well as the minimum of the work function at 0.5 ML coverage indicate the transition from ionic bonding between alkali atoms and the Si substrate to the formation of delocalized surface states in the Cs/Si adlayer, which promote electrical transport. Available photoemission spectroscopy data taken at room temperature[18,29] do show increased emission at the Fermi edge at coverages above 0.5 ML but, unfortunately, do not reveal a dispersing surface state band crossing the Fermi level to which the observed conductance channel could be ascribed. Lee and Chung speculate on a $6s-6p_z$ hybridization band that forms with the *s* electrons of excess Cs on top of the Cs chains at 0.5 ML coverage. The plasmon spectrum indicates that the surface is metallic already at 0.5 ML coverage. So the single atomic Cs layer on Si(001) is not a Mott insulator as observed, e.g., for single layers of K on Si(111) (Refs. 5 and 30) or for Cs on GaAs(011) (Refs. 4 and 31). However, macroscopic electrical transport requires thermal activation and, with respect to coverage, the conductance exhibits a maximum for coverages slightly higher than 0.5 ML. At this stage, the reasons for the activation barrier and the required supersaturation fraction can only be speculated on:

(1) The anisotropy of the chain-like submonolayer structure of Cs/Si(001) may play an important role if it induces a quasi one-dimensional metallic surface conductance as demonstrated by micro-probe measurements on Si(111) (4×1)-In (Ref. 32) and Si(557)-Au (Ref. 33), and by macroscopic measurements for Pb monolayers on highly anisotropic Si(557) substrates.[34] For the latter it was shown that electrical transport across Pb chains requires thermal activation, while along the chains it does not. Since, on the macroscopic scale, the Si(001) surface is never free of atomic steps and 2×1 and 1×2 domains coexist, macroscopic conductance measurements will always be affected by electrical transport across Cs/Si(001) chains, which may require thermal activation. The Cs supersaturation fraction beyond 0.5 ML, which is required for the onset of significant surface conductance, may then be needed to reduce the conductance anisotropy of single terraces by providing sites for electron hopping from one Cs chain to the next.

(2) One-dimensional defects like steps and domain boundaries may impose barriers for two-dimensional electrical transport within surface states, as noted by Henzler.[22] Four-point microprobe measurements at room temperature on Si(111)$(\sqrt{3}\times\sqrt{3})$-Ag (Refs. 35 and 36) have demonstrated that the conductance across a bunch of steps is reduced by almost an order of magnitude when compared to the surface state conductance across a terrace. To our knowledge, the electron scattering mechanism at the steps has not been identified, yet. Yokoyama and Takayanagi[37] have shown that a quantum well barrier for Si(001) surface states is generated by a single Al adatom chain across the substrate dimer rows. Analyzing standing wave patterns of an unoccu-

pied Si(001) surface state, the quantum well barrier can be modeled as 0.4 nm wide and infinitely high.

If single substrate steps act as barriers between metallic Cs/Si(001) 2×1 and 1×2 domains, then, on a macroscopic scale, electrical transport would appear thermally activated, like a hopping mechanism. In fact, variations of the step density via variations of the surface preparation had a clear influence on the magnitude of the surface state conductance. However, they hardly changed the coverage at which the surface conductance exhibited a maximum. So the Cs supersaturation fraction beyond 0.5 ML is obviously not required to decorate structural defects like monatomic steps. The role of domain boundaries and the supersaturation amount of Cs will be elucidated in forthcoming experiments on highly vicinal and single domain substrates.

IV. CONCLUSIONS

Step-like increases of the surface sheet conductance of Cs layers on Si(001) with increasing coverage can be interpreted as fingerprints of structural transitions of the surface from a semiconducting substrate with ionically bonded adatoms to a chain-like metallic adlayer and to a continuous Cs wetting layer. Combined conductance, LEED, and work function measurements suggest that, when grown in the temperature range 120–200 K, the Cs wetting layer is composed of three atomic layers, each with a nominal coverage of 0.5 ML with respect to the substrate surface. While previous experimental work at room temperature is abundant, detailed information on atomic and electronic structure of the low-temperature Cs/Si(001) phases and the wetting layer is still missing. The apparent sensitivity of the sheet conductance of the Cs wetting layer to surface roughness indicates a large electron mean free path with respect to the layer thickness.

In the submonolayer coverage regime, electrical transport via one of the metallic Cs/Si(001) surface phases previously identified by EELS has been observed for the first time on a macroscopic scale. Given the low Cs coverage, the conductance channel must involve a surface state band of the Cs/Si(001) adlayer. While, so far, the origin of this surface band remains unclear, it will probably reflect the one-dimensional nature of the Cs chain structure. The macroscopic conductance measurements reveal a supersaturation fraction of Cs above 0.5 ML coverage which is required for the onset of significant surface conductance. This supersaturation fraction may be required to promote electrical transport across the chain-like surface structure within a single domain.

The dependence of the sheet conductance in the submonolayer coverage regime on temperature reveals an activation barrier of 28 meV for electrical transport, which appears to be inconsistent with the metallic nature of the surface, but may have its origin in transport barriers at domain boundaries. The role of the anisotropy within single domains and of domain boundaries on electrical transport will be elucidated in future experiments on vicinal and single-domain surfaces.

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