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Lumped Electro-Thermal Model of On-chip Interconnects

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Abstract— **The paper proposes a compact but accurate electro-thermal model of a long on-chip interconnect embedded in a ULSI circuit. The model is well suited to be interfaced with the commercially available tools employed in ICs design for interconnect parasitic extraction.**

I. Introduction

In modern nanometer ULSI circuits interconnects play a dominant role in determining the timing behavior of the digital systems [1]. The verification of system performance and the analysis of signal integrity need the employment of specific simulation tools for the extraction of interconnect parasitics and thus for the estimation of interconnect propagation delay [2], [3].

Simultaneously the aggressive scaling down of devices dimension and the increase of operating frequency has dramatically magnified the electrical power density leading to a significant temperature increase in the substrate and in the metal interconnects. The increase of temperature determines, among other effects, an increase of electrical resistivity of metal interconnect and thus a degradation of propagation delay. In high-performance digital systems the nonuniform nature of power dissipation and of boundary conditions imposed by packaging and cooling mechanism can be such that relevant temperature gradients appear on the substrate [4]. In this condition, the thermally-induced degradation of a long interconnect depends on the path followed by the line over the substrate.

Recently a method for the analysis of nonuniform substrate thermal effects in ULSI interconnects has been presented [5]. The proposed method follows an analytical approach and employs a one dimensional distributed model of the interconnect and closed form expressions of substrate temperature profiles as interconnect boundary conditions. The analytical method is suited to explore the qualitative shape of temperature profile in the interconnect but is not suited to be interfaced with the tools that are commonly employed in ICs design. Parasitic extractor tools in fact model interconnections by discretizing them in a set of elementary subsections and thus they supply lumped RC models [3]. In addition, the layout of ULSI circuits is very complicated and a reliable thermal analysis can be accomplished only numerically; as a consequence temperature profile over the chip substrate is available only in a set of discrete points.

To cope with these aspects, in this work we propose an alternative approach to electro-thermal analysis of long ULSI interconnects that is able to handle as an input the RC lumped model supplied by extraction tools. The proposed method exploits an interconnect lumped electro-thermal model that employs as boundary condition the substrate temperature profile derived by a numerical thermal analysis (or alternatively through on chip measurements). The compact model allows the designer to evaluate the temperature increase in the interconnect and the effective propagation delay as a function of interconnect path over the substrate. It is shown that in high-performance processors interconnect layouts that are equivalent from a purely electrical point of view can have significantly different propagation delay due to thermally-induced degradation.

II. Background: Interconnect Electrical Model for Timing Analysis

We start with by considering an on-chip interconnection embedded in a ULSI layout, Fig. 1 shows the typical shape of such an interconnect.

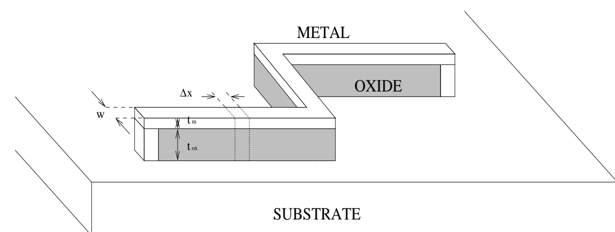

Fig. 1. Interconnect line

The common approach to on-chip interconnection analysis is done by determining the parasitic elements associated to the net and thus building up an equivalent purely electrical model. In commercially available extraction tools, this is accomplished through the following steps: a) the interconnect is first fractured in subsections accordingly to internal rules (such as the presence of crossing nets or at line corners); b) for each subsection the electrical resistance and the parasitic capacitance is computed. As a result a ladder RC electrical model of the interconnect is deduced where C_{E_k} and $R^0_{E_k}$ are the parasitic capacitance and the electrical resistance

respectively of the k-th section, see Fig. 2. It is worthwhile observing here that the $R^0_{E_k}$ electrical resistance associated to the section is determined by considering the resistivity of metal at a reference temperature and that the variation of such value due the increase of temperature and to temperature gradient is commonly not considered. The purely electrical model is further employed in the timing analysis of electrical system to estimate the time delay introduced by the interconnect. To such a purpose we consider here a line connected to an input driver with on-resistance R_{dr} and junction capacitance C_{dr} and terminated by a load capacitance C_L. The delay D for signal propagation through the line can be written using the distributed RC $Elmore$ $delay$ $model$

$$D = R_{dr}\left(\sum_{i=1}^{n} C_{E_i} + C_L\right) + \sum_{i=1}^{n} R_{E_i}\left(\sum_{j=i}^{n} C_{E_j} + C_L\right) \tag{1}$$

where C_{E_i} and R_{E_i} are the capacitances and resistances evaluated by the extraction tool for each elementary section [6].

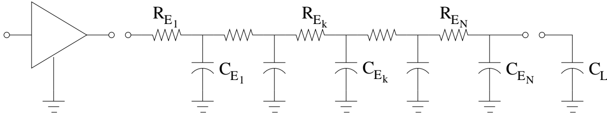

Fig. 2. Electrical RC model of the interconnect line

III. Electro-thermal analysis

The on-chip interconnect is embedded into the complex geometry of the chip layout so that the temperature distribution along interconnect is the result of two different heating mechanisms: a) the mutual heating of active devices integrated over the chip substrate; b) the interconnect self heating due to Joule effect. The chip layout is described by placing and connecting over the substrate a set of standard elementary circuit layout, referred to as standard cells. From the circuit layout we know the location of each standard cell and the average dissipated electrical power. From this information we first determine the steady-state temperature distribution over the whole substrate. To such a purpose we formulate the discretized heat equation into the geometry of the chip substrate and determine an equivalent thermal network by following the well known approach. The substrate is discretized with a finite difference grid into elementary volumes and for each volume a node into the thermal network is introduced. Each node is connected to all the the nodes of the neighborhood volumes through the thermal resistance that accounts for the heat diffusion mechanism. The thermal exchange between the chip and external environment is described through external thermal resistors that are deduced from the boundary exchange conditions. Note that we are interested only in steady-state DC temperature profile and thus dynamic thermal capacitors are not considered. The average power dissipated by each cell is injected as an equivalent (current) source into the thermal node corresponding to the standard cell volume. We remark that generally, due to the huge number of standard cells that form a layout, each elementary volume of the thermal discretization contains many standard cells volumes. In this case the standard cells are grouped together to form a single equivalent source and their average powers are accumulated. The steady-state solution of substrate temperature allows to compute the temperature distribution in the substrate along the path that is obtained projecting the interconnect geometry over the substrate. This substrate temperature distribution along the line path becomes the boundary condition to use when analyzing the self heating into the interconnect.

We concentrate now on the electro-thermal model of the interconnect. To derive the interconnect electro-thermal model we consider the interconnect line (Fig. 1), of length L, width w running over the substrate surface at a distance t_{ox} and connected to the substrate through vias at its two ends.
As said before the interconnection line is partitioned in elementary sections from the parasitic extractor tool that supplies an RC electrical model.
Digital circuits operate at very high frequency and electrical time constants are several order of magnitudes smaller than thermal ones. Thus in order to determine the steady-state temperature profile we limit to consider the average power dissipated by each line section. Calling I_{rms}, the root mean square amplitude of the current that flows in the line, we assume that the root mean square current is constant in all sections. The electrical power dissipated in the k-th section of the interconnect is thus given by:

$$P_k = R_{E_k} I^2_{rms} \tag{2}$$

On the other hand the local electrical resistance R_{E_k}, depends on the local temperature of the interconnect section as follows:

$$R_{E_k} = R^0_{E_k}(1 + \beta \cdot (T_{line_k} - T_0)) \tag{3}$$

where $R^0_{E_k}$ is the electrical resistance supplied by the parasitic extraction tool and computed at reference temperature T_0, β is the temperature coefficient of electrical resistivity [1/°C], and T_{line_k} is the temperature of the k-th elementary section; $T_k = T_{line_k} - T_0$ is the temperature increase over reference temperature.
Therefore, power dissipation can be rewritten as follows:

$$P_{E_k} = R^0_{E_k}(1+\beta \cdot T_k) \cdot I^2_{rms} = R^0_{E_k} \cdot I^2_{rms} + R^0_{E_k} \cdot \beta \cdot T_k \cdot I^2_{rms} \tag{4}$$

The power effectively dissipated by each section is composed of two contributions the first of which depends only on the effective value of current flowing into the line while the second one depends in turn on the increase of temperature in the interconnect section. The compact electro-thermal model of the interconnect is presented in Fig. 3. The electrically dissipated power is injected into the thermal nodes through two current sources, the first one is an independent current source of value $R^0_{E_k} \cdot I^2_{rms}$, the second one is a temperature-controlled current source of value $R^0_{E_k} \cdot \beta \cdot T_k \cdot I^2_{rms}$. Heat

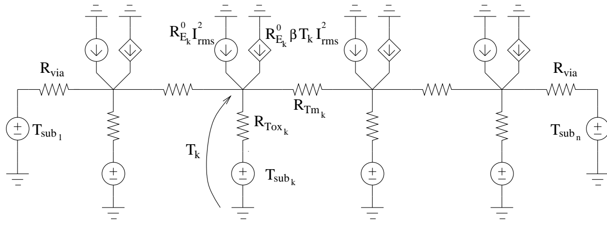

Fig. 3. Interconnect electro-thermal model

diffusion into the line is described by thermal resistors R_{Tm_k}

$$R_{Tm_k} = \frac{1}{k_m} \frac{\Delta x_k}{w \ t_m} \tag{5}$$

where k_m is the metal thermal conductivity and Δx_k is the length of k-th interconnect section.

Heat exchange toward the underneath substrate is modeled through an equivalent resistor R_{Tox_k} and an equivalent temperature source imposing the local substrate temperature T_{sub_k} determined by the previously described substrate thermal analysis. For what concerns the oxide thermal resistance it can be written as follows:

$$R_{Tox_k} = \frac{1}{k^*_{ox}} \frac{t_{ox}}{w \ \Delta x_k} \tag{6}$$

where k^*_{ox} is the effective oxide thermal conductivity and t_{ox} is the oxide thickness.

The effective oxide thermal conductivity k^*_{ox} is a shape-dependent parameter which considers the geometrical configuration of the heat conducting body on the thermal conductivity.

For the case of a rectangular shape parallel to an infinite plate with dimension that satisfy the condition $w/t_{ox} > 0.4$ we use a Bilotti's estimation [7], in the other case, when this condition is not satisfied (like the geometrical configuration of the interconnect in deep submicron technologies) we use a more accurate expression for k^*_{ox} introduced by Andrews [8]:

$$k^*_{ox} = k_{ox} \cdot \frac{t_{ox}}{w} \cdot 1.685 \cdot \left[log\left(1 + \frac{t_{ox}}{w}\right)\right]^{-0.59} \cdot \left(\frac{t_{ox}}{t_m}\right)^{-0.078} \tag{7}$$

At the two ends of the interconnect there are two vias that connected the line to the substrate. The thermal resistance of the vias are calculated as follows:

$$R_{via} = \frac{1}{k_m} \frac{t_{ox}}{w \ \Delta x} \tag{8}$$

For a given chip and interconnect layouts, the solution of electro-thermal model allows to determine the temperature increase in each section of the interconnection and thus from (1) to deduce the following thermal-aware delay propagation

$$D = R_{dr}\left(\sum_{i=1}^{n} C_{E_i} + C_L\right) + \tag{9}$$

$$\sum_{i=1}^{n} (R^0_{E_i} + R^0_{E_i} \beta T_i) \left(\sum_{j=i}^{n} C_{E_j} + C_L\right) \tag{10}$$

where C_{E_i} and R_{E_i} are the capacitances

IV. Numerical results

We consider an high-performance microprocessor manufactured in 150 nm HCMOS technology and integrated in the frame of a ULSI chip. The layout of the sole microprocessor is composed of about 200,000 transistors and is described by about 20,000 standard cells; the microprocessor occupies a chip area of of 0.216 mm^2 (dimensions 0.47 mm x 0.46 mm) that is referred to as $active\ area$ in Fig. 4. The average power dissipated, the geometry and the coordinates of each cell forming the microprocessor is available from the layout description language and is thus an input data. The microprocessor on the whole dissipates an electrical power of 0.9 W that is distributed in a nonuniform way over the active area being significantly greater near the bottom-right corner. The microprocessor is placed over a silicon die of thickness 100 μm.

First we compute the temperature distribution over the substrate by considering a simulation domain of 1.27 mm x 1.26 mm containing the microprocessor and we impose adiabatic condition on the later walls of the domain and a uniform heat exchange coefficient h=10000 W/m^2 on the bottom face of the domain. Fig. 4 shows the computed steady-state temperature distribution over the chip substrate; you see that the maximum temperature of 83 °C is reached near the bottom-right side of the active area and that a gradient of 36 °C establishes on the chip.

After that we take two different interconnect lines belonging to the first Metal layer and connecting points A an B over the chip through two different paths $path$-I and $path$-II. Fig. 5 reports the computed temperature profiles over the substrate along Path-I and Path-II. Note that the temperature gradient along Path-I (about 30 °C) is much larger than the one along Path-II.

The two lines have the same geometry, they have length $L = 993\mu m$, width $w = 0.4\mu m$ and thickness $tm = 0.55\mu m$ and are placed at a distance $tox = 1.33\mu m$ over the substrate. The two lines are drawn in the layout according to the electrical design rules and from a purely electrical point of view they are absolutely equivalent. As we are going to show they are not equivalent when thermal effects are taken into account. The IC extractor tool supplies a ladder RC interconnect models formed of many cells corresponding to a total electrical resistance of 122 Ω and a total parasitic capacitance of 91.9 fF. The two lines drive a load capacitance C_L = 40 fF. We employ such RC models and the numerically-computed temperature map to form the compact electro-thermal interconnects models as described in section 3. Then we assume a root mean square interconnect current I_{rms} = 5 mA and we employ the compact electro-thermal model to estimate the temperature profiles along the interconnects. The electro-thermal model is formed of 55 sections. Fig. 6 shows the temperature into the interconnects. From the interconnect temperature we determine the interconnect resistances as modified by heating effect and then we deduce the thermal-aware

propagation delay according to *RC Elmore delay model* (9).

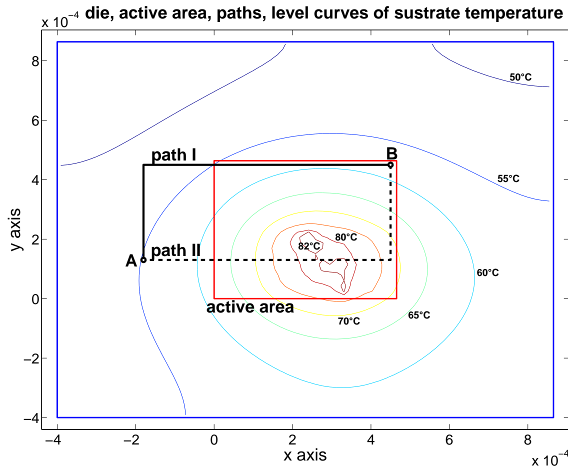

Fig. 4. Chip domain and path I and path II from point A to point B on a substrate with temperature distribution

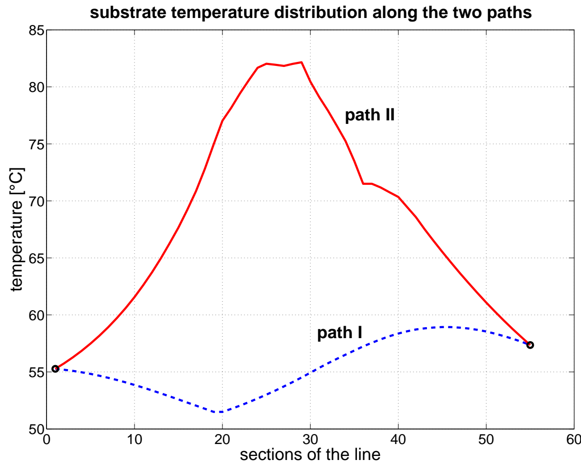

Fig. 5. Substrate temperature profile along the interconnects paths

Fig. 7 reports the estimated delay along the two different paths for the cases: a) employing the compact electro-thermal model; b) considering a constant temperature T_0 = 27 °C.

The total propagation delay from point A to point B estimated through a purely electrical analysis at T_0 temperature is $D_0 = 10.5{\cdot}10^{-12}$ s. While when the electro-thermal effect is considered the total delays are $D_1 = 12.14 \cdot 10^{-12}$ s and $D_2 = 12.76 \cdot 10^{-12}$ s for the cases of *path I* and *path II* (hottest path) respectively. Neglecting heating effect leads thus to underestimate the propagation delay of about 22% with respect the effective delay. The degradation induced by heating effect is relevant and can not be disregarded in the design phase. When thermal effects are considered we see that the difference

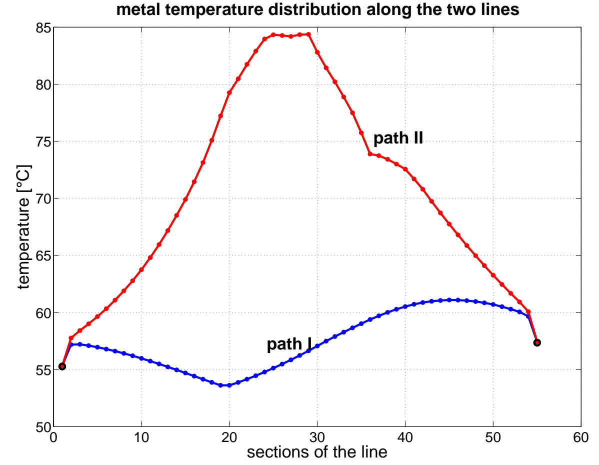

Fig. 6. Temperature profile along the interconnects

between the delay along path-I and path-II corresponds to $\Delta D = 6.1 \cdot 10^{-13}$ sec and to a relative difference of about 5%. This information results to be important to optimize interconnect placement in order to minimize skew effect.

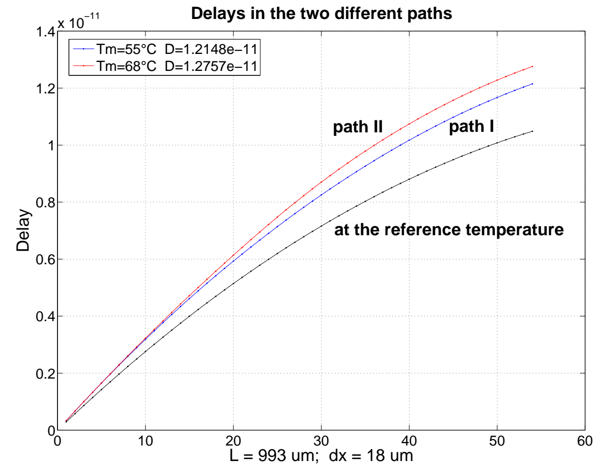

Fig. 7. Delay profile along the interconnects lines end along the line at the reference temperature

V. Conclusion

The paper presents a numerical approach to compute the temperature profile in long ULSI interconnects accounting for both mutual effect induced by active devices and self heating due to Joule effect. The method uses the interconnect lumped model extracted by ICs design tools and the numerically computed substrate temperature map as determined by a numerical thermal analysis. The model is compact in that it accounts for electro-thermal feedback mechanism through equivalent sources. For a given chip layout and interconnect path over the substrate the proposed model allows the designer to evaluate the temperature increase in the line and the propagation delay.

References

[1] H. D. Lee, D. M. Kim, and M. J. Jang, ”On-chip characterization of interconnect parameters and time delay in 0.18 μm CMOS technology for ULSI circuit applications,” *IEEE Trans. Electron Devices*, vol. 47, pp. 1073-1079, May 2000.

[2] F. Caignet, S. Delmas-Bendhia, and E. Sicard, ”The challenge of signal integrity in deep-submicrometer CMOS technology,” *Proc. IEEE*, vol. 89, pp. 556-573, Apr. 2001.

[3] A. Brambilla, P. Maffezzoni, P., L. Bortesi, L. Vendrame, ”Measurements and extractions of parasitic capacitances in ULSI layouts,” *IEEE Trans. on Electron Devices*, Vol. 50 , No. 1, pp. 2236-2247, Nov. 2003.

[4] A. H. Ajami, K. Banerjee, M. Pedram, and L. P. P. P. van Ginneken, ”Analysis of nonuniform temperature-dependent interconnect performance in high-performance ICs,” *Proc. Design Automation Conf.*, pp. 567-572, 2001.

[5] Ajami A.H., Banerjee K., Pedram M., ”Modeling and Analysis of Nonuniform Substrate Temperature Effects on Global ULSI Interconnects,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, issue 6, pp. 849-861, 2005.

[6] B. Kahng Andrew, and Sudhakar Muddu, ”An Analytical Delay Model for RLC Interconnects,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, n. 12, pp. 1507-1514, 1997.

[7] Bilotti A. A., ”Static temperature distribution in IC chips with isothermal heat sources,” *IEEE Trans. Electron Devices*, vol. ED-21, no. 3, pp. 217-226, Mar. 1974.

[8] Andrews R. V., ”Solving conductive heat transfer problems with electrical-analogue shape factors,” *Chem. Eng. Prog.*, vol. 51, no. 2, pp. 67-71, 1955.